HANOI UNI. OF SCI. AND TECH. FACULTY OF MATH. AND INFORMATICS

FINAL TEST, FALL 2024 Course: CS365 - Intro. to COA Duration: 60 minutes	Student name: [redacted] Student Id: [redacted] Order: Class Id: CS365

Assessors' name and signature	Examiners' name and signature	Total score
[redacted]		

Test Id: 2 **This test consists of 10 questions.** ***No document is allowed.***

Questions with one correct answer

Question 1. What is the binary number corresponding to this hexadecimal number `0xBF4`?

☐ 111011110100 ☐ 101111110100 ☐ 101011110100 ☐ 110111110100

Question 2. What decimal number is represented by the following IEEE 754 single precision float?

1011 1111 0100 0000 0000 0000 0000 0000

☐ -1.75 ☐ -0.75 ☐ 0.375 ☐ -0.375

Question 3. Which of the following statements is correct?

☐ Pipelining reduces the time it takes to complete an individual instruction
☐ Pipelining reduces instruction throughput
☐ Pipelining increases the number of simultaneously executing instructions
☐ Pipelining improves individual instruction execution time

Question 4. Which of the following terms is abbreviated as GPU?

☐ Graphic processing unit
☐ Graphical processing unit
☐ General processing unit
☐ Graphics processing unit

Question 5. What is the Verilog code that creates a 32-bit value with the pattern 0101 . . . 01?

☐ `{2{16'b01}}` ☐ `{16'b01,16'b01}` ☐ `{2{16'h5555}}` ☐ `32'b01`

Question 6. Which of the following statements is correct?

☐ The output of a flip-flop is not equal to the value of its stored state
☐ A CAM is a circuit that combines comparison and storage in a single device
☐ SRAM is a memory where data is stored dynamically
☐ DRAMs are faster than SRAMs, but less dense and more expensive per bit

Constructed-response questions

Question 7. Add comments to the following MIPS code and describe in one sentence what it computes.

```
lwc1    $f0, x($sp)     .....
lwc1    $f1, y($sp)     .....
div.s   $f2, $f0, $f1   .....
swc1    $f2, z($sp)     .....
```

Question 8. Given the CPU performance equation:

CPU time = Instruction count × Average CPI/(Clock rate)

Explain why optimizing the instruction set architecture can help to improve the CPU performance.

Question 9. Give a short introduction to your group project (i.e. the project that your group has taken in this course) and your own contribution.

Question 10. Draw the combinational logic circuit described by the following Verilog module.

```
module func {A, B, C, S, D};
  input A, B, C;
  output S, D;
  assign S=A&B&C;
  assign D=(A^B)|(B^C)|(C^A);
endmodule
```