

QL-EOS-S3 breakout

Variant: [No Variations]

10/6/2020

RevB

Release Candidate

Page Index

1	COVER PAGE
2	BLOCK DIAGRAM
3	MICROCONTROLLER
4
5
6
7
8
9
10

Page Index

11
12
13
14
15
16
17
18
19
20

Page Index

21
22
23
24
25
26
27
28
29
30

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

DESIGN NOTE:
Example text for critical design notes.

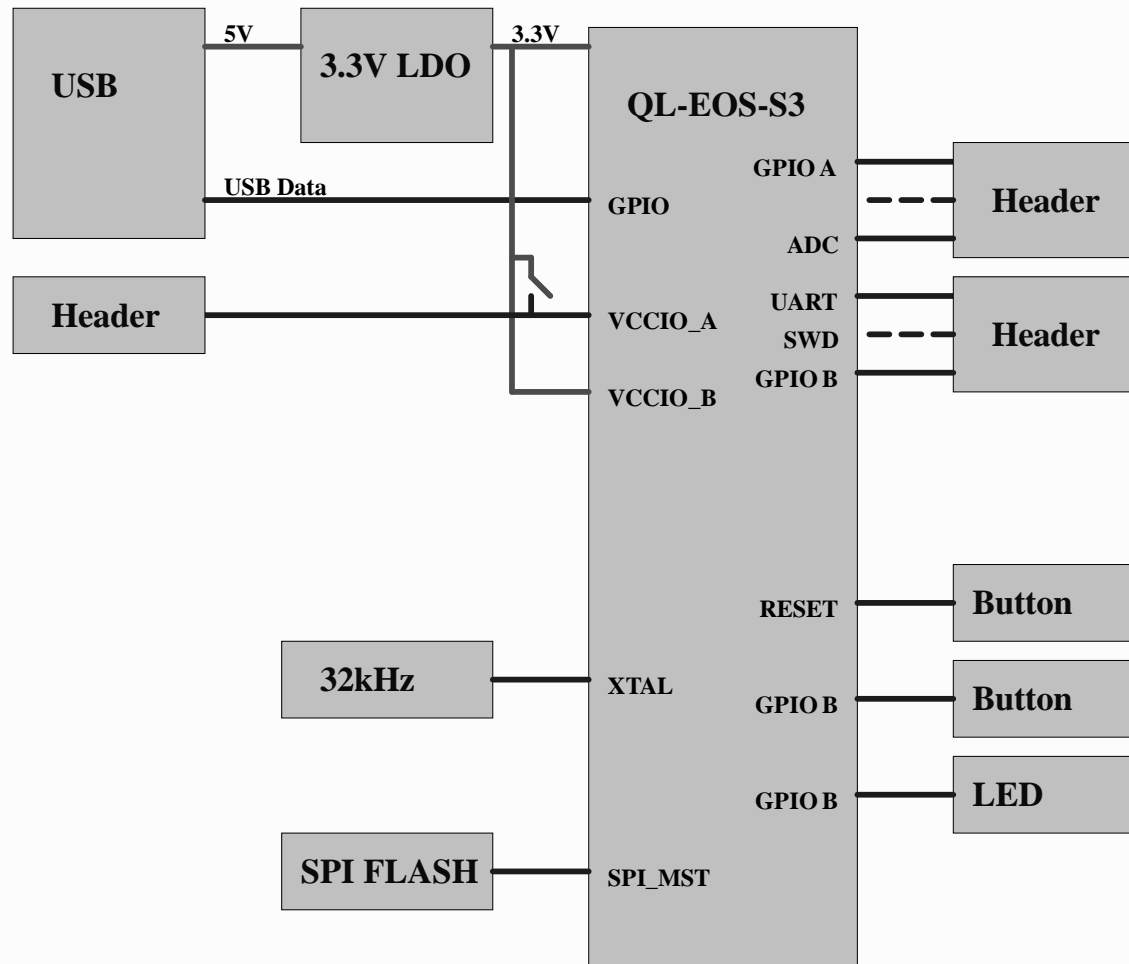
DESIGN NOTE:
Example text for cautionary design notes.


LAYOUT NOTE:
Example text for critical layout guidelines.

Title: *		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevB	
Date: 10/6/2020	Time: 6:37:07 PM	Sheet 1 of 4

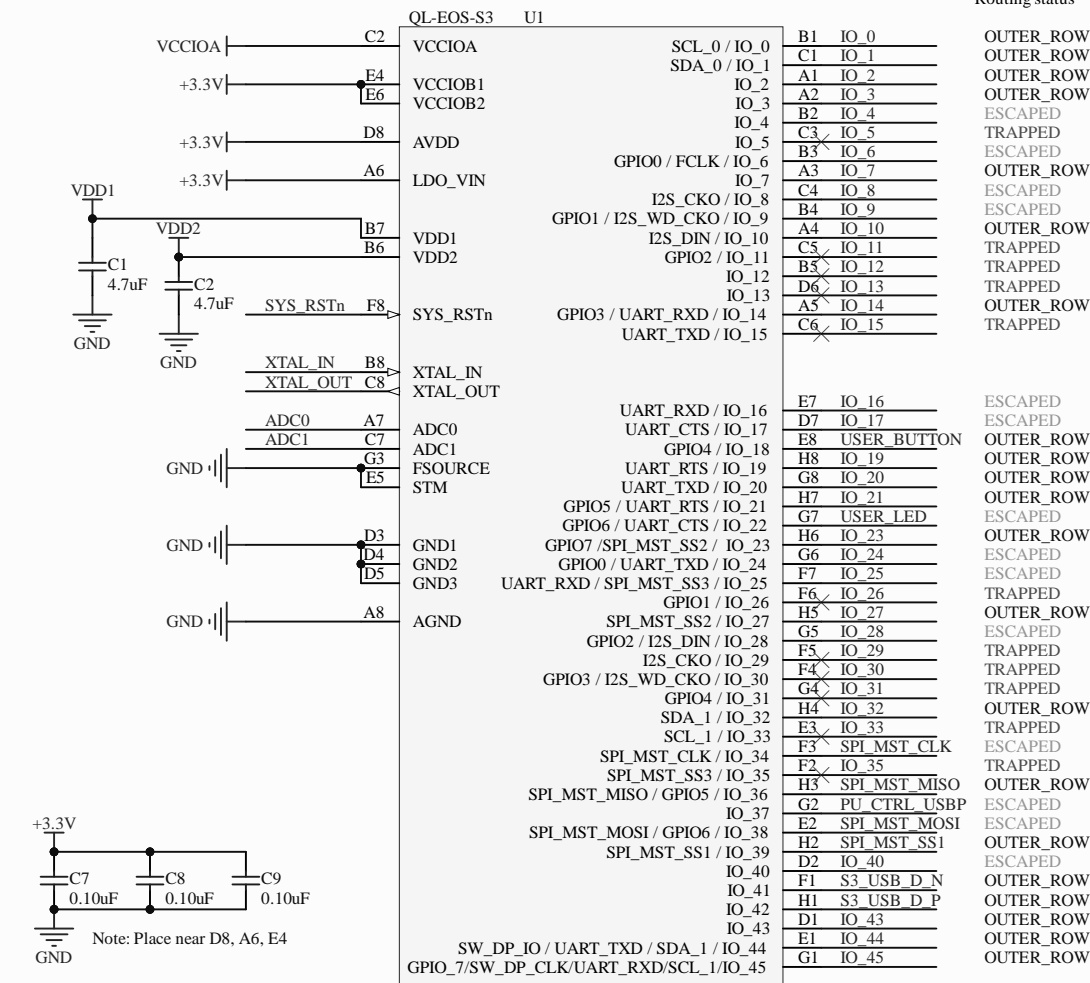


QL-EOS-S3 breakout



Title: Block Diagram		
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevB	
Date: 10/6/2020 Time: 6:37:07 PM	Sheet 2 of 4	

MCU/FPGA



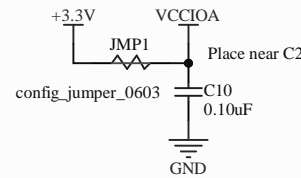
QL-EOS-S3 breakout

Design intent:
 -Low-cost, minimum viable ARM+FPGA design that is breadboard compatible
 -Footprint, power, UART pin compatibility with Teensy 3.2.
 -All pins on Bank A placed in a group, so that they can have their IO voltage set with an external reference
 -Bootstrap, SPI flash, and reset pins placed in non-breadboardable location to avoid inadvertent interference with application circuit
 -Pins with multiple IO functions preferred over FPGA only pins
 -Pins in ascending order by FPGA IO number when possible

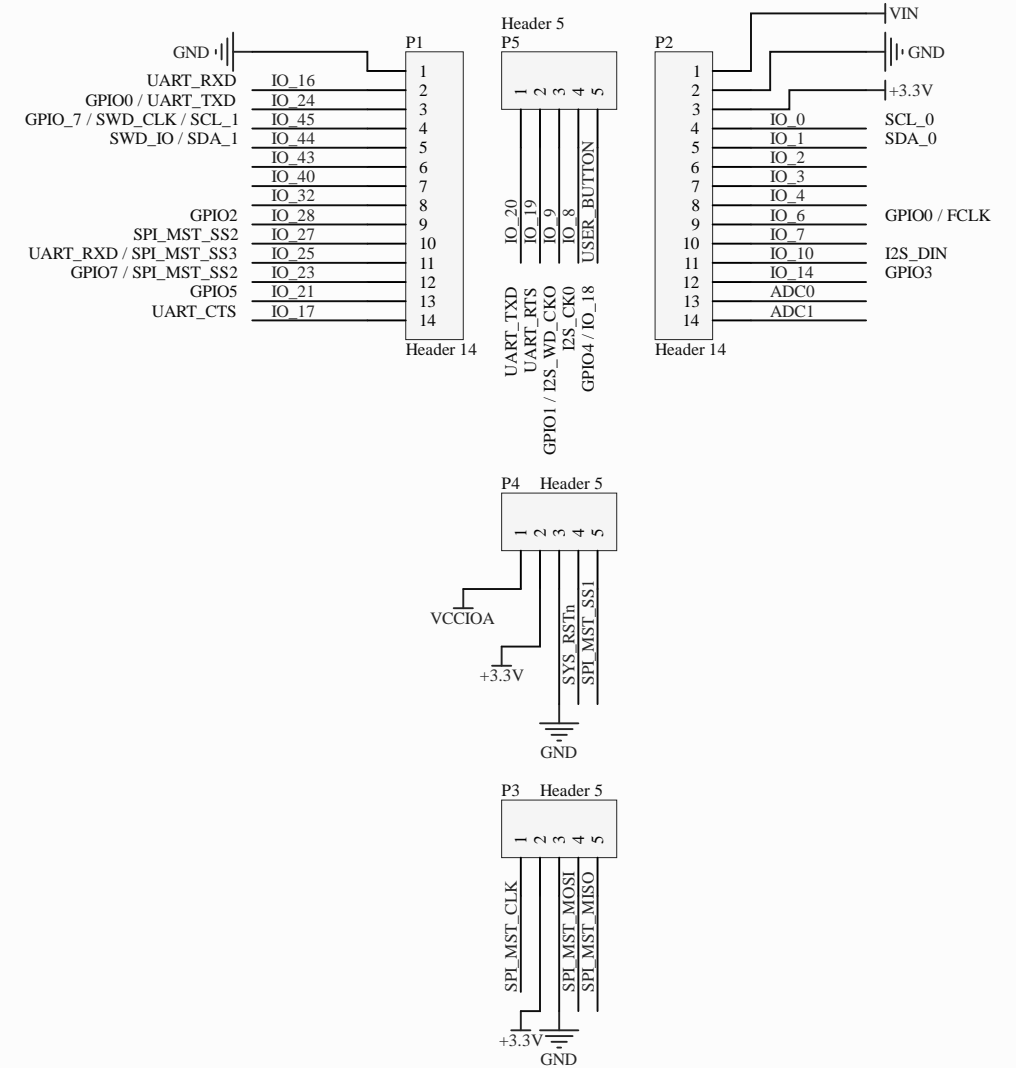
Useful connections:
 -Bridge VCCIOA to 3.3V if the jumper was cut
 -Bridge SYS_RSTn to GND to put processor in reset for external SPI Flash programming
 -Bridge IO_19 to 3.3V to enable JTAG SWD on boot

I/O Bank A reference voltage

Cut jumper JMP1 and provide 1.2-3.3V (?) reference voltage on VCCIOA pin

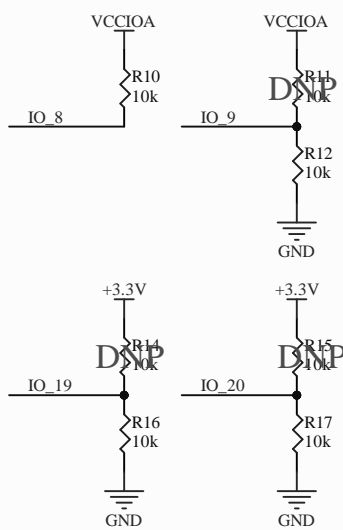


I/O Pins



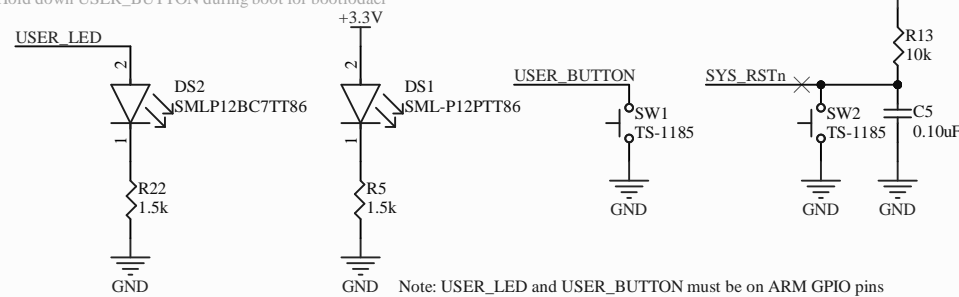
Bootstrap Configuration

IO_8: SWD pin assignment: pull down for 14/15 (default), up for 44/45
 IO_8/IO_9: High speed oscillator selection; both pulled up for external oscillator, otherwise internal oscillator
 IO_19: Enable SWD: pull down to disable, up to enable
 IO_20: Boot mode: pull down for host (boot from SPI flash), pull up for companion (boot from external processor)



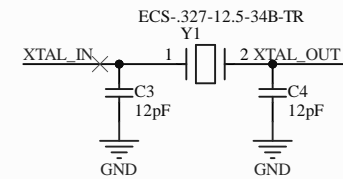
Status indication and feedback

Hold down USER_BUTTON during boot for bootloader



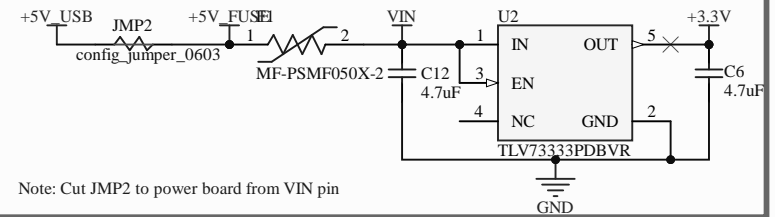
32.768k oscillator

Used for RTC and as a reference for the main clock



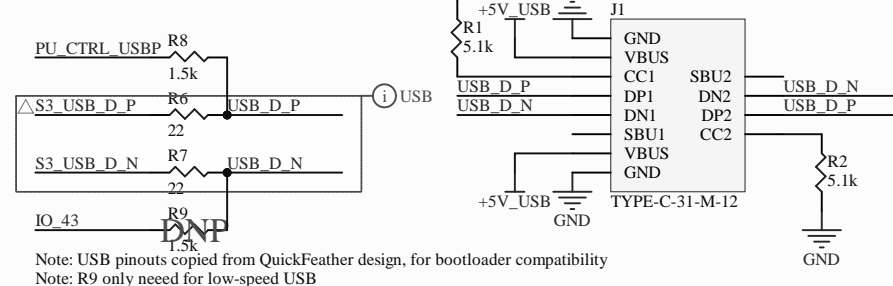
3.3V regulator

300mA max

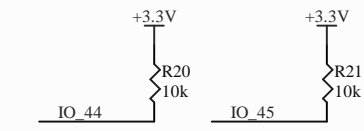


USB connection

USB is implemented as an FPGA soft core

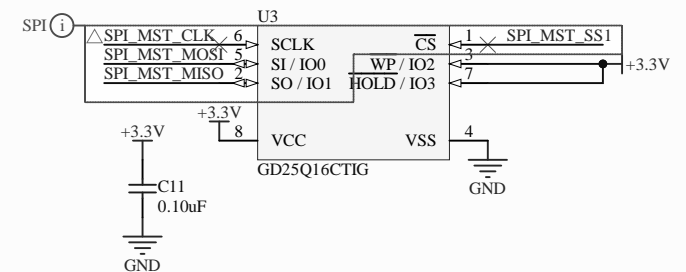


JTAG pull-ups

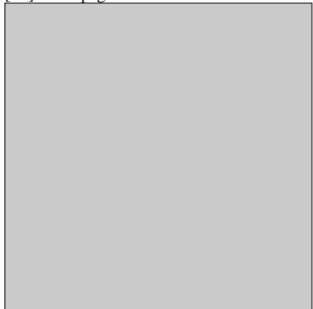


SPI Flash

Program memory loaded from SPI flash at boot



Designator
[01] cover page.SchDoc



Designator
[02] Block Diagram.SchDoc



Designator
[03] SOC.SchDoc



A

A

B


B

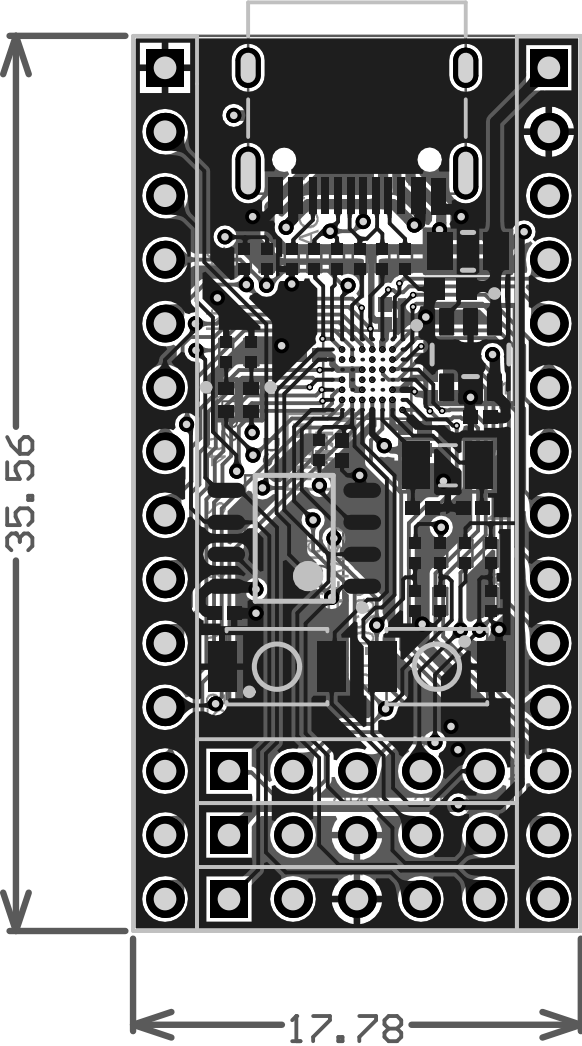
C

C

D

D

Title: *			
Project: QL-EOS-S3-breakout.PrjPcb	Revision: RevB		
Date: 10/6/2020	Time: 6:37:07 PM	Sheet 4 of 4	



Layer	Name	Material	Thickness	Constant
	Top Overlay			
	Top Solder	SM-001	0.013mm	4
1	Top Layer	Copper	0.035mm	
	Dielectric 2	PP-022	0.200mm	4.6
2	Layer 1	Copper	0.018mm	
	Dielectric 3	Core-039	0.665mm	4.8
3	Layer 2	Copper	0.018mm	
	Dielectric 4	PP-022	0.200mm	4.6
4	Bottom Layer	Copper	0.035mm	
	Bottom Solder	SM-001	0.013mm	4
	Bottom Overlay			

Total board thickness: 1.195mm

Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Blinkinlabs-Repos\QL-EOS-S3-breakout\pcb\QL-EOS-S3-b

Warnings 0
Rule Violations 330

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.152mm) (All),(All)	0
Clearance Constraint (Gap=0.127mm) (istrack or ((ObjectKind = 'Via') And (AsMils(ViaDiameter)	0
Clearance Constraint (Gap=0.152mm) (InComponent('JMP1') or	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Short-Circuit Constraint (Allowed=Yes) (InComponent('JMP1') or	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.152mm) (Max=0.406mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor	0
Width Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Hole To Hole Clearance (Gap=0.25mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	281
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	44
Silk to Silk (Clearance=0.254mm) (All),(All)	4
Net Antennae (Tolerance=0mm) (All)	1
Board Clearance Constraint (Gap=0mm) (IsPolygon)	0
Room [03] SOC (Bounding Region = (144.78mm, 45.72mm, 172.72mm, 86.36mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	330

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)

Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C10-1(10mm,24.89mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C1-1(10.81mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C11-1(4.015mm,12.625mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C1-2(11.59mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C1-2(11.59mm,20mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.229mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.228mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-2(11.95mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.223mm < 0.254mm) Between Pad C12-2(11.95mm,25.5mm) on Top Layer Anc
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C2-1(11.81mm,22.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.177mm < 0.254mm) Between Pad C2-2(12.59mm,22.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.178mm < 0.254mm) Between Pad C2-2(12.59mm,22.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C3-1(13.11mm,16.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C4-1(11.89mm,16.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.227mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.227mm < 0.254mm) Between Pad C5-2(8.3mm,19.49mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad C5-2(8.3mm,19.49mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C6-1(14.19mm,20.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C7-1(12.59mm,21.2mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C8-1(11.59mm,19.1mm) on Bottom Layer
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C9-1(6.61mm,22.9mm) on Bottom Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A1/B12(12.115mm,29.19mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad J1-A1/B12(12.115mm,29.19mm) on Top
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A12/B1(5.665mm,29.198mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.176mm < 0.254mm) Between Pad J1-A12/B1(5.665mm,29.198mm) on Top
Minimum Solder Mask Sliver Constraint: (0.203mm < 0.254mm) Between Pad J1-A4/B9(11.34mm,29.198mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A5(10.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A5(10.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A6(9.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A6(9.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A6(9.14mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A7(8.64mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A8(7.64mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.14mm < 0.254mm) Between Pad J1-A8(7.64mm,29.198mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.203mm < 0.254mm) Between Pad J1-A9/B4(6.44mm,29.198mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R10-1(13.2mm,15.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(10.8mm,27.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-1(10.8mm,27.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R11-1(14.2mm,15.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad R1-2(10.8mm,26.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R12-1(14.2mm,13.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R13-1(7.4mm,18.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R14-1(12.2mm,15.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R15-1(11.2mm,15.4mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R16-1(12.2mm,13.5mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R17-1(11.2mm,13.5mm) on Top Layer And

Pad

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)

Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G5(8.3mm,21.9mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G6(8.3mm,21.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G7(8.3mm,21.1mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.212mm < 0.254mm) Between Pad U1-G8(8.3mm,20.7mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-G8(8.3mm,20.7mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H1(7.9mm,23.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H2(7.9mm,23.1mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H3(7.9mm,22.7mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H4(7.9mm,22.3mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H5(7.9mm,21.9mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H6(7.9mm,21.5mm) on Top Layer And
Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad U1-H7(7.9mm,21.1mm) on Top Layer And
Pad

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (13.165mm,11.5mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (2.9mm,21.6mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Arc (4.615mm,9.5mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Arc (5.461mm,21.603mm) on Top Overlay And Pad
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad C12-1(13.25mm,25.5mm) on Top Layer
SILK To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Pad C5-1(8.3mm,18.71mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-12(1.27mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-13(1.27mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.233mm < 0.254mm) Between Pad P1-14(1.27mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.218mm < 0.254mm) Between Pad P2-12(16.51mm,6.35mm) on Multi-Layer
SILK To Solder Mask Clearance Constraint: (0.214mm < 0.254mm) Between Pad P2-13(16.51mm,3.81mm) on Multi-Layer
SILK To Solder Mask Clearance Constraint: (0.211mm < 0.254mm) Between Pad P2-14(16.51mm,1.27mm) on Multi-Layer
SILK To Solder Mask Clearance Constraint: (0.199mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P3-1(3.81mm,1.27mm) on Multi-Layer And
SILK To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-2(6.35mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-2(6.35mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P3-3(8.89mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P3-4(11.43mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.235mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P3-5(13.97mm,1.27mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.199mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.2mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
SILK To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P4-1(3.81mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.219mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-2(6.35mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-3(8.89mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.248mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.249mm < 0.254mm) Between Pad P4-4(11.43mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.236mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.238mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.234mm < 0.254mm) Between Pad P4-5(13.97mm,3.81mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.204mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.203mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.201mm < 0.254mm) Between Pad P5-1(3.81mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.251mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.219mm < 0.254mm) Between Pad P5-2(6.35mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.246mm < 0.254mm) Between Pad P5-3(8.89mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.244mm < 0.254mm) Between Pad P5-4(11.43mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.241mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.24mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And
Silk To Solder Mask Clearance Constraint: (0.253mm < 0.254mm) Between Pad P5-5(13.97mm,6.35mm) on Multi-Layer And

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.178mm < 0.254mm) Between Text "BLIN

KIN**LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(6.12mm,20.55mm) on B**

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.248mm < 0.254mm) Between Text "BLIN

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,17.55mm)(9.12mm,17.55mm) on B

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.108mm < 0.254mm) Between Text "BLIN

KIN

LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (6.12mm,20.55mm)(9.12mm,20.55mm) on B

Silk to Silk (Clearance=0.254mm) (All),(All)

Silk To Silk Clearance Constraint: (0.192mm < 0.254mm) Between Text "BLIN

KIN

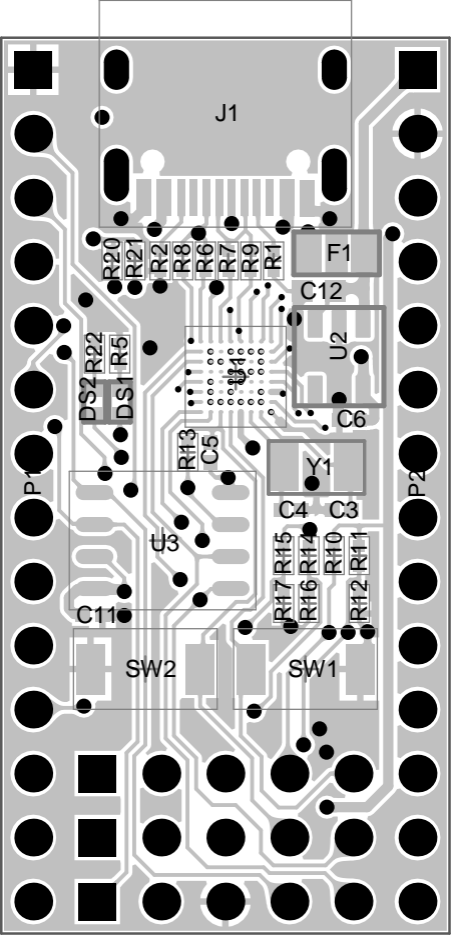
LABS" (9.12mm,20.55mm) on Bottom Overlay And Track (9.12mm,17.55mm)(9.12mm,20.55mm) on B

Net Antennae (Tolerance=0mm) (All)

Net Antennae: Track (6.235mm,32.385mm)(7.735mm,32.385mm) on Bottom Layer

Electrical Rules Check Report

Class	Document	Message
Warning	[03] SOC.SchDoc	Un-Designated Part L?



J1

R20
R21
R2
R8
R6
R7
R9
R1

F1

C12

U2

DS2 R22
DS1 R5

U1

C6

R13
C5

Y1

U3
C11

C4 C3

R17 R15
R16 R14
R10
R12 R11

SW2

SW1

P1

P2

