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1 Introduction

1.1 Document overview

This document provides a comprehensive overview of the software architecture design, outlining the system's structure, key components, and their interactions. It aims to define the architectural framework, highlight design principles, and serve as a reference for development, integration, and maintenance. The document includes logical architecture, functional modules, data flow, and interface definitions, ensuring clarity and alignment among stakeholders.

1.2 Abbreviations and Glossary

Item	Definition
BSL	Bootstrap Loader
BLE	Bluetooth Low Energy, a Bluetooth protocol (4.0 and higher) that incorporates efficient energy saving features
Flash	a type of non-volatile RAM
IPG	Implantable Pulse Generator
OAD	Over the Air Download
RAM	Random Access Memory
SRAM	Static RAM, a type of volatile RAM

1.3 References

- CAR-208 IPG Software Requirements Specification (v1.0)
- HNT-TECH-14-HPD Protocol Description (v1.0)
- IPG-schematic-layout (v1.0)
- Stimulation Circuit Overview
- Stimulation Waveforms Overview
- Impedance Measurement Strategy
- VNSb Hornet FW and HW interaction description v1.0
- XLboard Commands v1.0

2 Architecture

2.1 Architecture overview

Operating platform:

✧ Microcontroller							
Part No.	STM32U585QII6Q	SRAM	786 KB	Flash	2 MB	Package	UFBGA 132-7x7 P0.5 mm
Core	ARM Cortex M33	Clock	160 MHz	Supplier	STMicroelectronics		
✧ Embedded software							
Item	Software			Version	Supplier		
STM32 HAL Library	STM32Cube_FW_U5			1.7.0	STMicroelectronics		

✧ Microcontroller							
Part No.	nRF52810-CAAA	RAM	24 KB	Flash	192 KB	Supplier	Nordic
Core	ARM Cortex M4	Clock	64 MHz		Package	WLCSP 33-2.48x2.46 P0.5 mm	
✧ Embedded software							
Item	Software		Supplier		Version		
SDK	nRF5 SDK		Nordic		17.1.0		
	S112 SoftDevice				7.2.0		

The software architecture has 8 units based on functions

- **Authentication**
  Authentication functions related to ECDSA, such as User class authentication and image file authentication during firmware update.
- **BLE**
  Manage BLE advertising, pairing, connection, disconnection and security through communication with the BLE chip.
- **Command**
  Management of the composition, parsing and execution of commands.
- **Log**
  Manage the generation, writing, searching and reading of various log data.
- **Measurement**
  Used to control the hardware used for measurements, including enabling or disabling hardware and voltage measurement and conversion.
- **Parameter**
  Manage the reading, writing, conversion, and range determination of various parameters.
- **State Machine**
  Manages the triggering conditions for all transitions between operating states and modes of the system.
- **Stimulation**
  Management of electrical stimulation related hardware, including electrical stimulation waveform, amplitude, output channel and duration.

2.2 Logical architecture overview

The system's logical architecture is divided into four layers, ranging from high-level application functionalities to low-level hardware abstraction. This structure clearly delineates the roles and interactions of each layer.

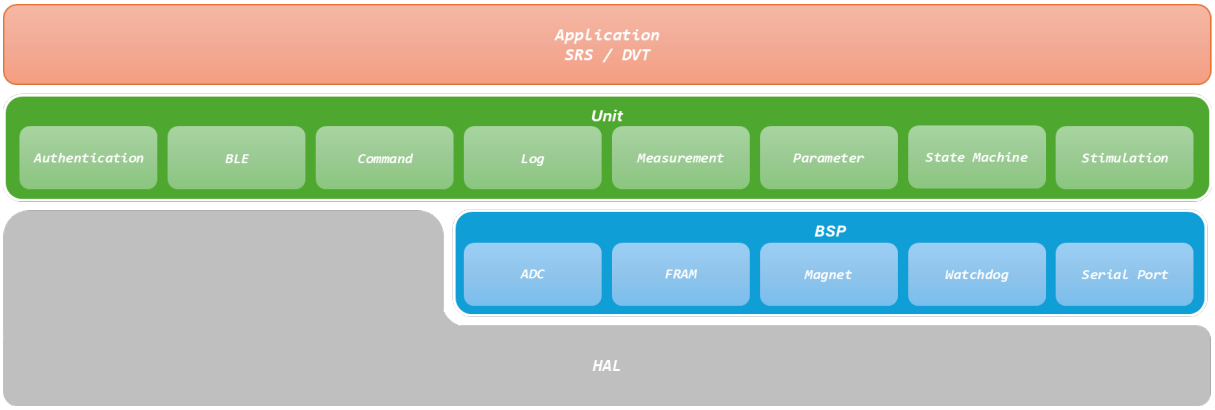
1. **Application Layer**
   - Positioned at the top, this layer handles the implementation of application-specific logic.
   - It directly interacts with the Unit layer to perform high-level tasks and meet user requirements.
2. **Unit Layer**
   - This layer contains multiple core functional modules, each responsible for specific logic or runtime functionalities, including:
     - **Authentication**: Manages user or device authentication.
     - **BLE**: Handles Bluetooth Low Energy communication.
     - **Command**: Manages the parsing and execution of commands.
     - **Log**: Implements system logging.
     - **Measurement**: Provides data measurement functionalities.
     - **Parameter**: Manages the configuration and access of system parameters.
     - **State Machine**: Defines and controls state transitions within the system.
     - **Stimulation**: Handles the generation and control of stimulation signals.
   - This layer serves as the core functionality provider, supporting the Application layer with essential services.
3. **BSP Layer (Board Support Package)**
   - This layer interacts directly with the hardware, encapsulating hardware details and providing standardized interfaces. Key modules include:
     - **ADC**: Analog-to-Digital Converter for processing sensor data.
     - **FRAM**: Manages operations related to non-volatile memory.
     - **Magnet**: Controls magnet-related functionalities.
     - **Watchdog**: Handles watchdog timer operations.
     - **Serial Port**: Provides serial communication support.
4. **HAL Layer (Hardware Abstraction Layer)**
   - Located at the bottom, this layer abstracts hardware-specific implementations, providing a uniform hardware interface for the BSP layer.

Module Interactions and Layered Relationships

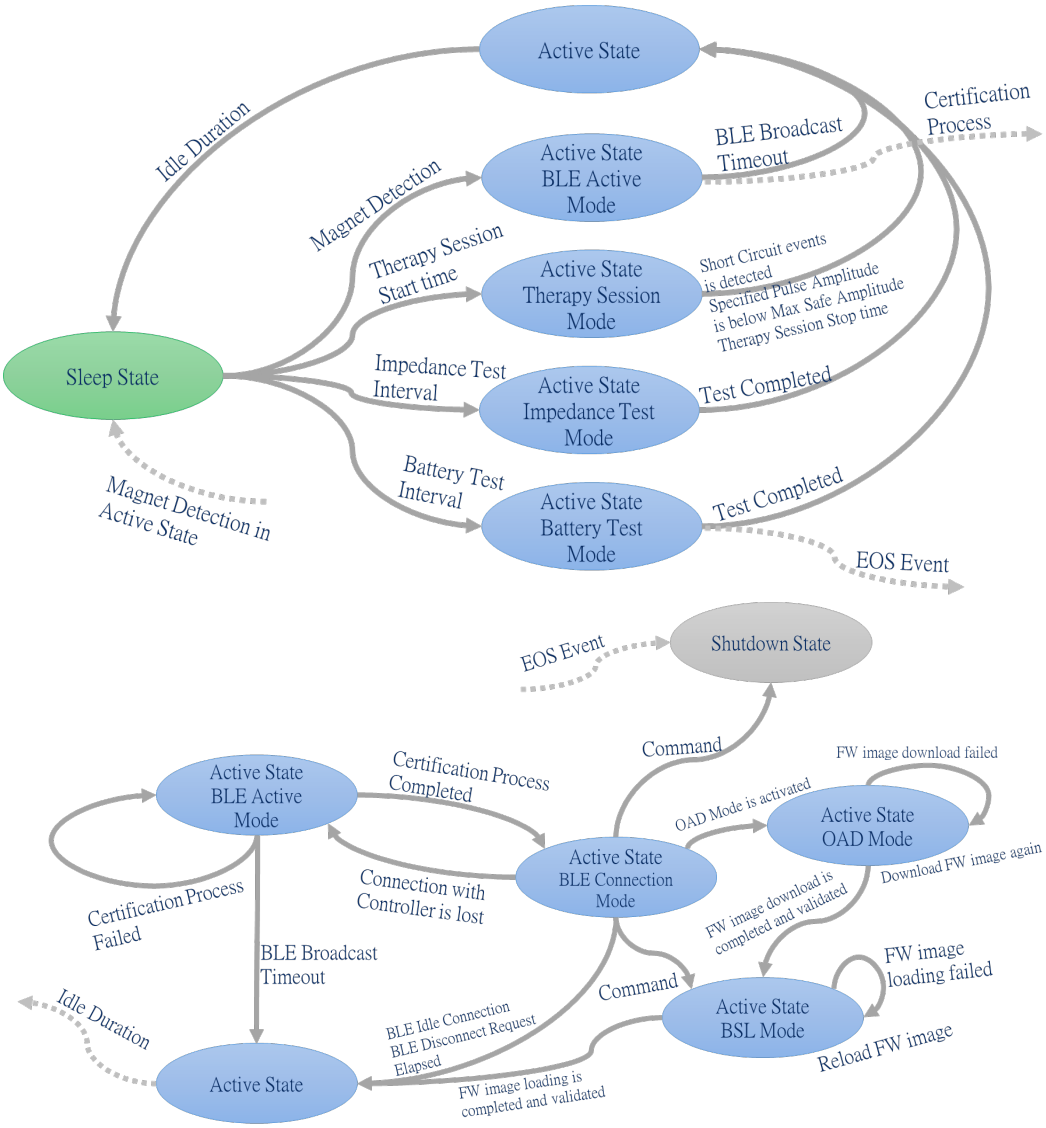
- **Layered Structure**: The architecture follows a layered design to ensure that higher-level modules (e.g., Application Layer) are not directly dependent on low-level hardware implementations, enhancing system scalability and maintainability.
- **Functional Decoupling**: The Unit layer separates core functionalities into distinct modules, with well-defined interfaces to minimize inter-module coupling.
- **Hardware Abstraction**: The BSP and HAL layers encapsulate hardware details, facilitating portability across different hardware platforms.

2.3 Software architecture picture

1. Software architecture



2. Finite-state machine



The firmware following states based on the 3 states defined by SRS, the active state has 8 operating modes. Please refer to Document "CAR-208 IPG Software Requirements Specification" for detailed definitions.

- **Shutdown State**
- **Sleep State**
- **Active State**
  - BLE Active Mode
  - BLE Connection Mode
  - Therapy Session Mode
  - Impedance Test Mode
  - Battery Test Mode
  - OAD Mode
  - BSL Mode
  - DVT Mode (For testing purposes only, this document does not contain)

REVISION HISTORY

Rev.	Date	Description
01	25/03/11	Software Architecture Design version 1