HORNET-1-IPG

Revision Log

Ver	Date	Description	Author	Reviewer
1.0.A	2024-04-30	HORNET 1 initial version built upon HORNET 0.	J. Evia	A. Ríos
1.1.A	2024-05-09	Apply minor fixes after RushPCB's DFM and DFA comments.	J. Evia	A. Ríos
1.2.A	2024-05-10	Increase the minimum clearance to 2mil.	M. Ferreira	A. Ríos
1.3.A	2024-05-14	Increase hole to hole clearance to 9mil.	M. Ferreira	A. Ríos
1.4.A	2024-05-16	Apply impedance fixes after RushPCB's DFM comments.	M. Ferreira	A. Ríos
1.5.A	2024-06-13	Improve Draftsman readability.	J. Evia	A. Ríos

Mechanical & Miscellaneous

Fiducial Markers

BOTTOM

- X1 FIDUCIAL
- X2 FIDUCIAL
- X3 FIDUCIAL

TOP

- X4 FIDUCIAL
- X5 FIDUCIAL
- X6 FIDUCIAL

Mounting holes

- X7 HOLE, UNPLATED
- X8 HOLE, UNPLATED
- X9 HOLE, UNPLATED

Power Net Reference

WPT and Bat charge

VCARR VRECT VCHG_RAIL

Battery 1

VBAT1R VBAT1F VBAT1SW

Stim. Power Supplies

HVIN HVOUT VPP

Battery 2

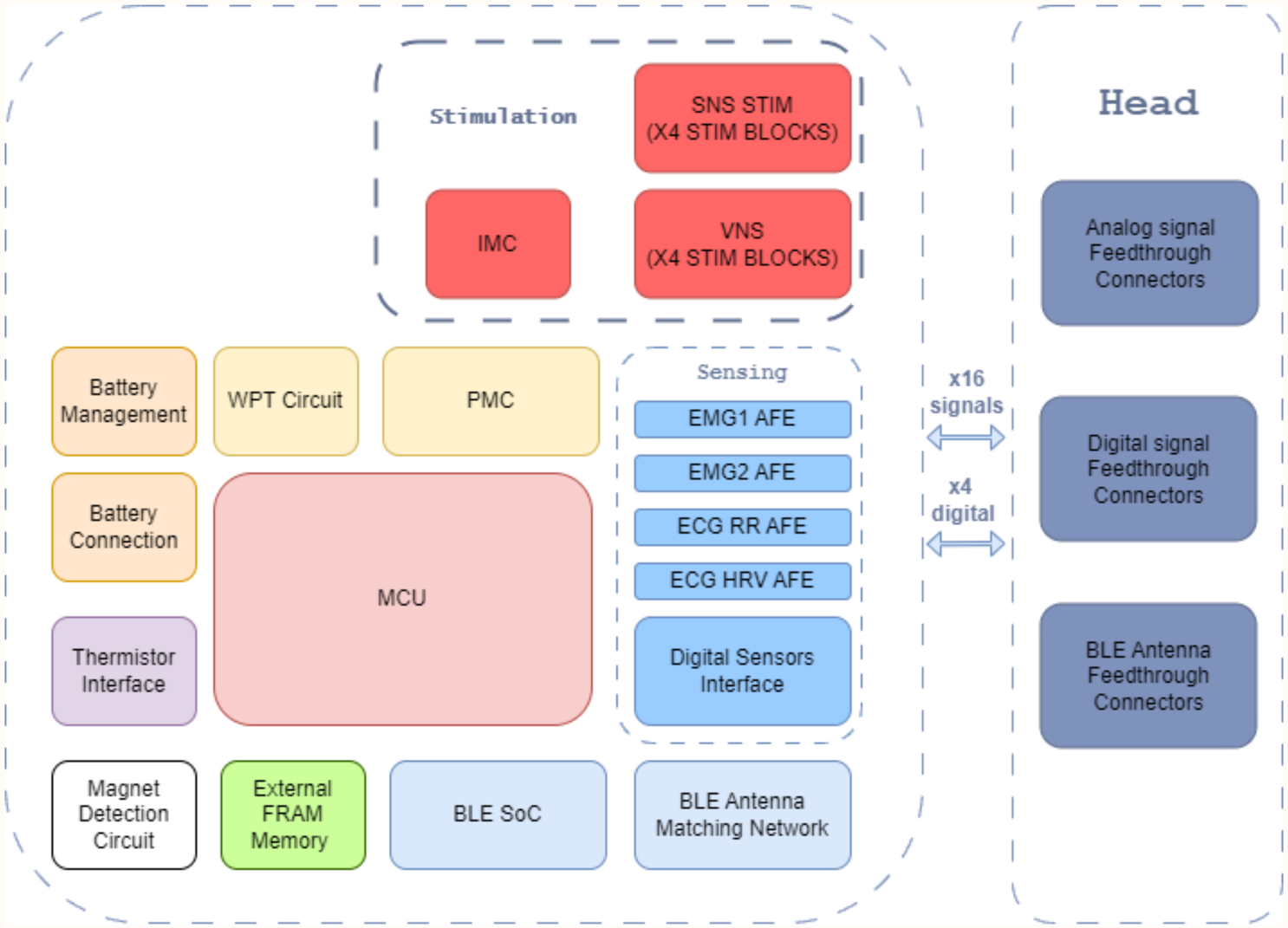
VBAT2R VBAT2F VBAT2SW

3.3 V Power Supplies

DVDD VDDA VDDS V_UNREG

Design considerations

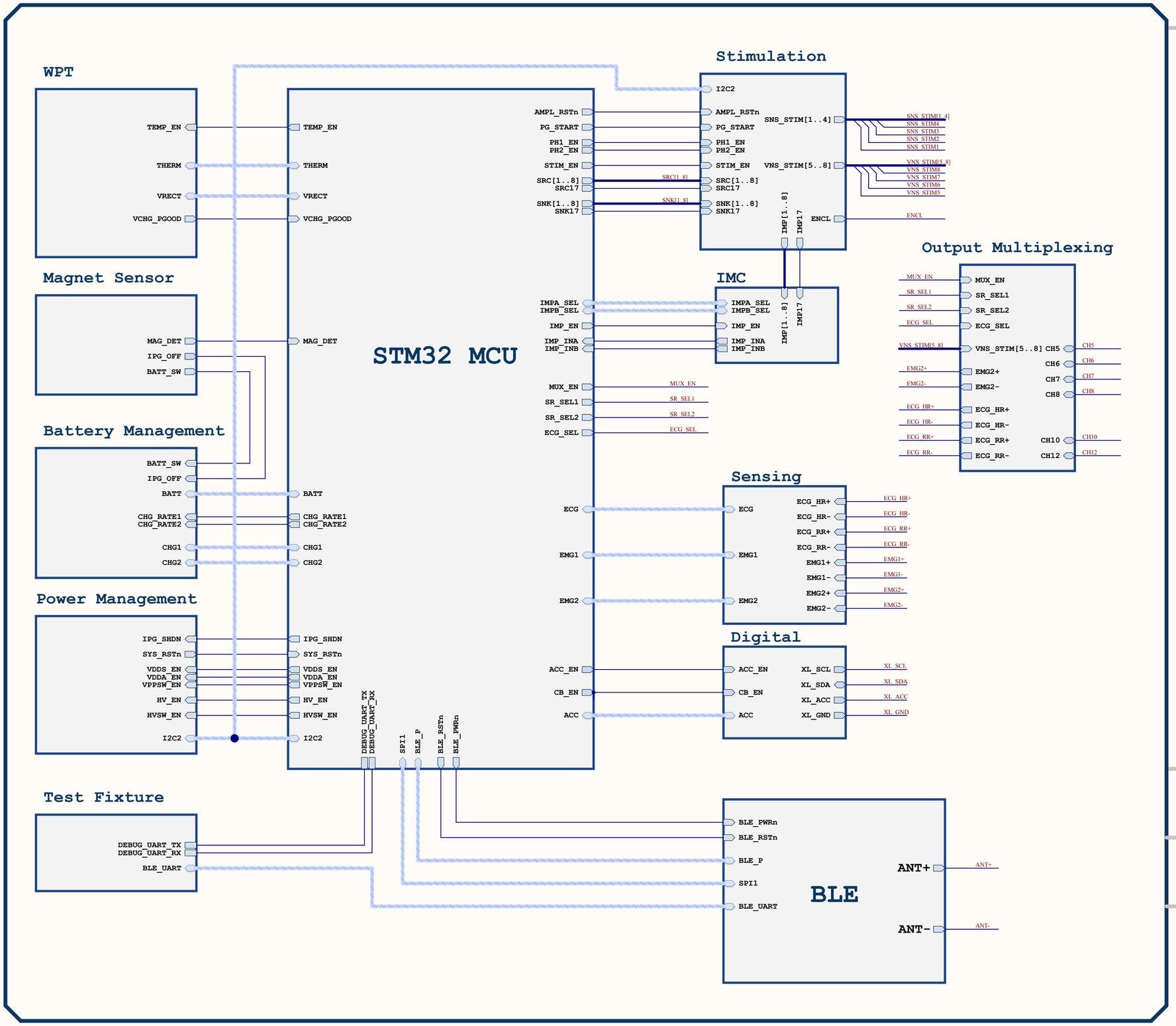
High Level Block Diagram



Page Index

FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Cover Page**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments:	

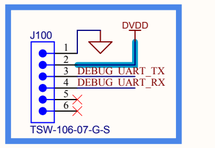
System Block Diagram



FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **System Block Diagram**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments:	

STM32U5 MCU

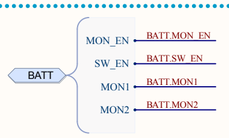
Serial Debug Interface



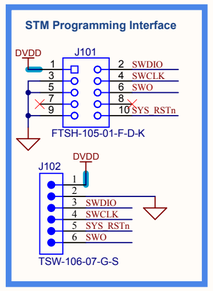
DEBUG_UART_TX — DEBUG_UART_TX

DEBUG_UART_RX — DEBUG_UART_RX

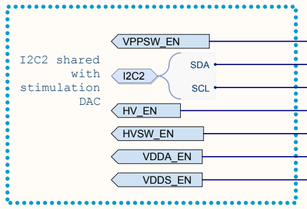
Batt Monitor



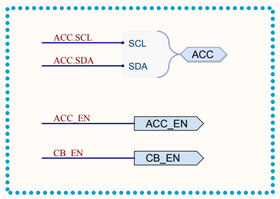
Microcontroller



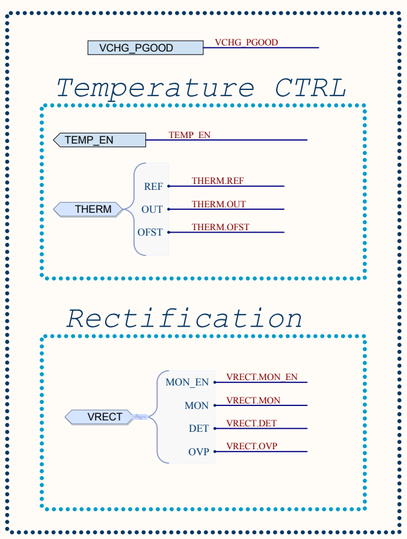
Power Management

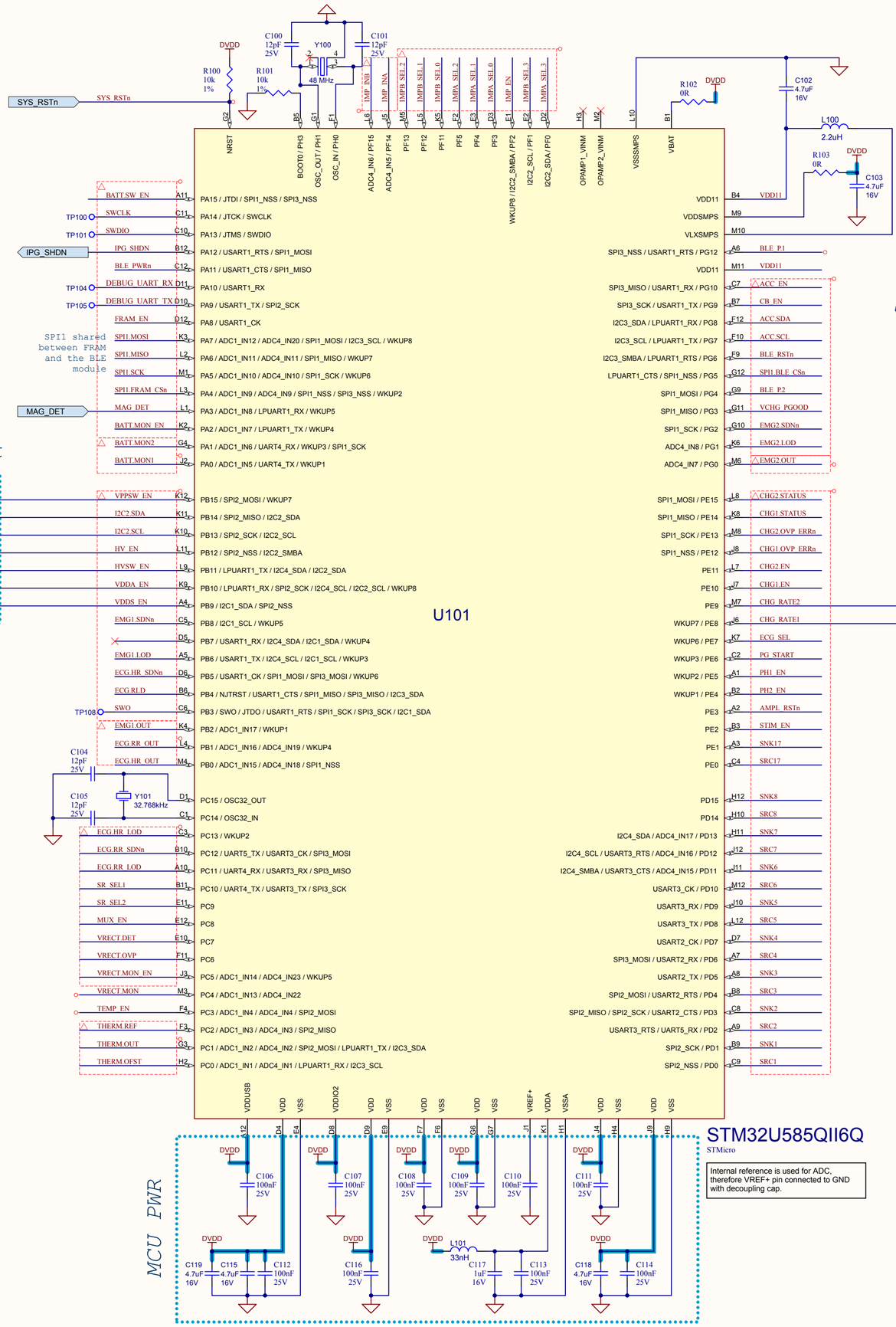


Digital Sense

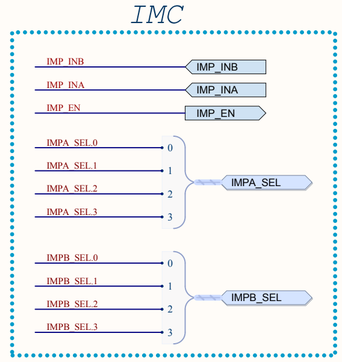


Wireless Power Transfer

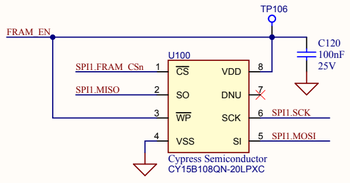




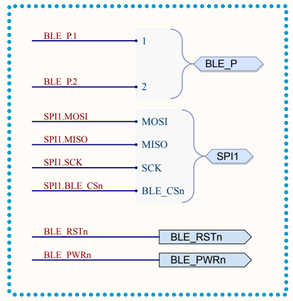
IMC



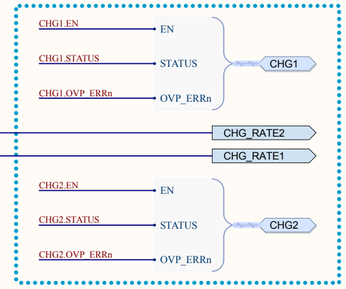
Serial FRAM



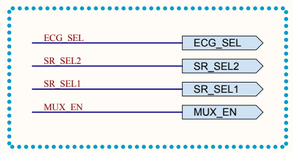
BLE



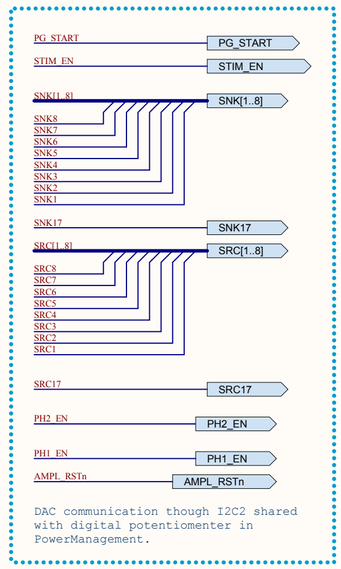
Charge control



MUX Control

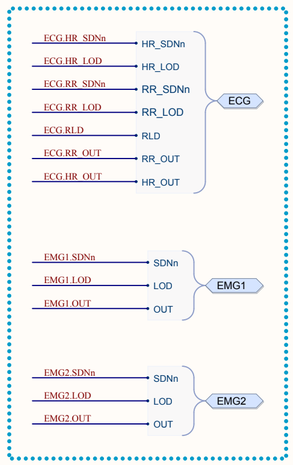


Stimulation



DAC communication though I2C2 shared with digital potentiomenter in PowerManagement.

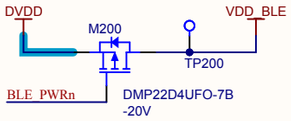
Sensing



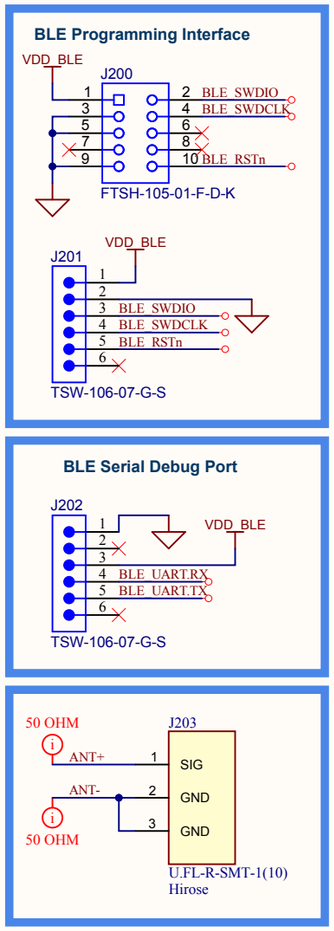
FOCUS	Project: HORNET-1-IPG.PrjPcb	
Schematic: **MCU**		Ver: 1 .5
Design by: **Julian Evia**		Date: **2024-06-13**
Reviewed by: **Alvaro Rios**		Date: **2024-06-13**
Comments: MCU Connections and adjasent circuit		

BLE Transceiver

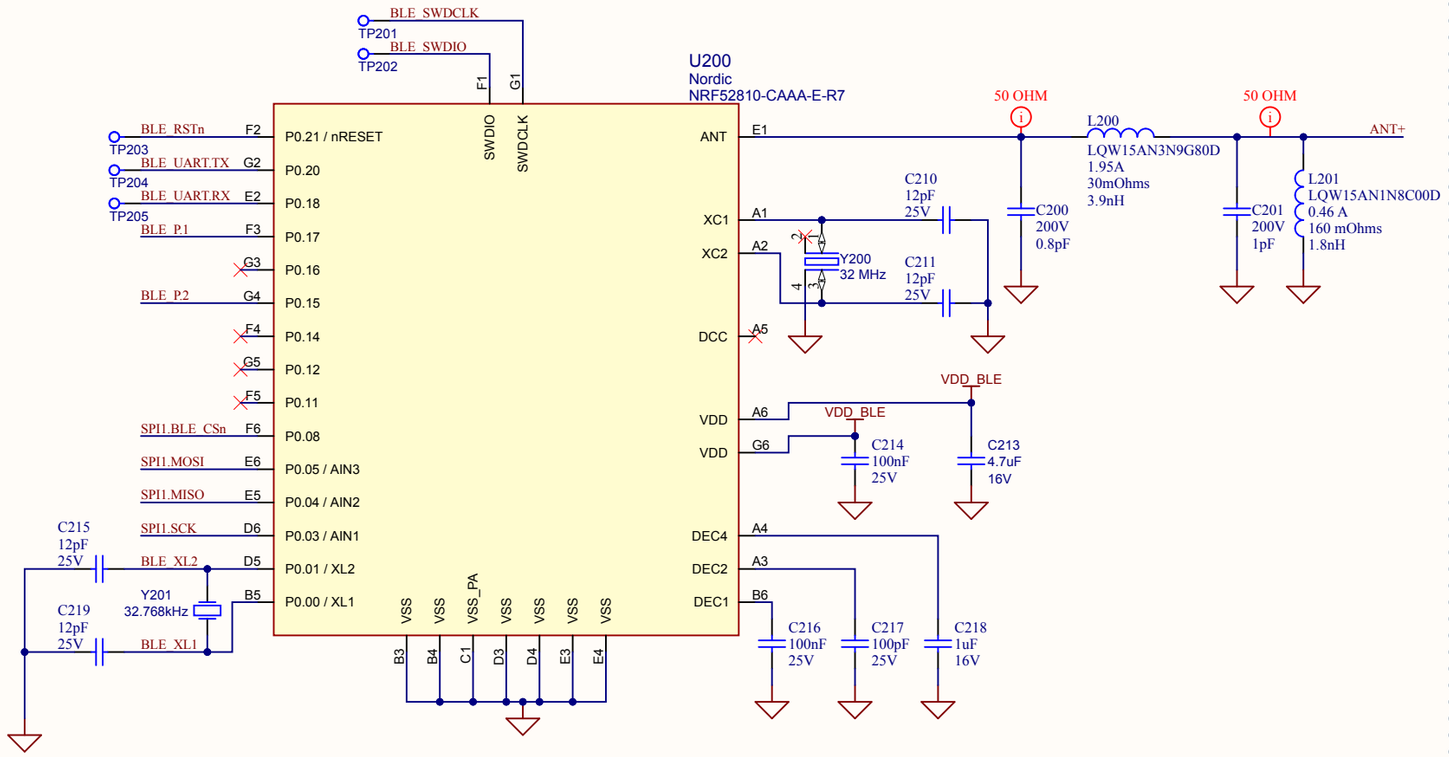
BLE PWR Control



Debug Interface

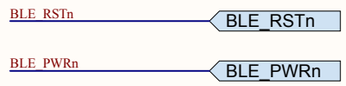


Communication dedicated SOC

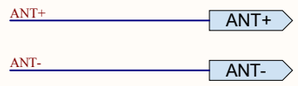


Interconnect

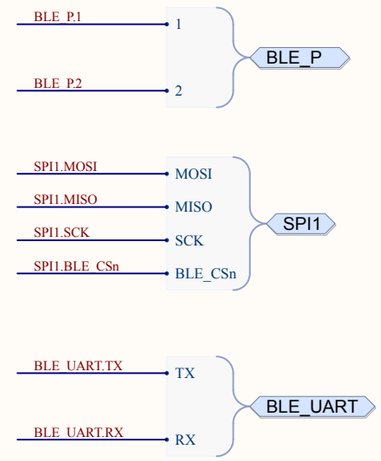
Inputs



Outputs



Communication



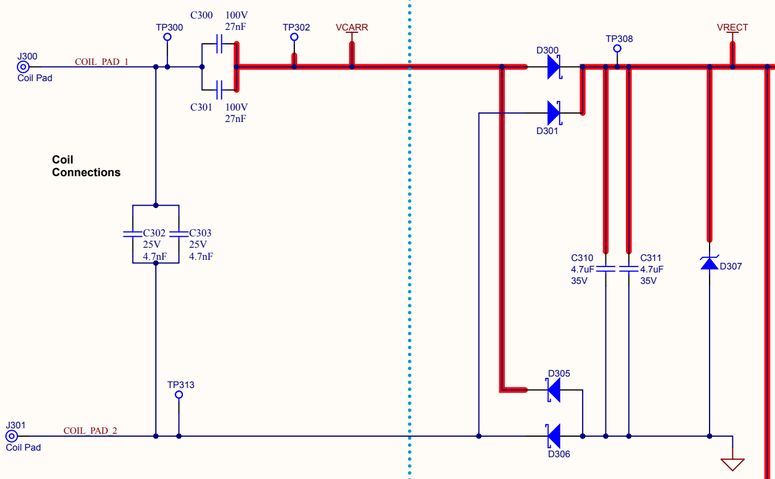
FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **BLE Transreciver**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: BLE dedicated MCU and mathcing network.	

Wireless Power Transfer

Antenna and rectification

Coil Tuning

Rectifier

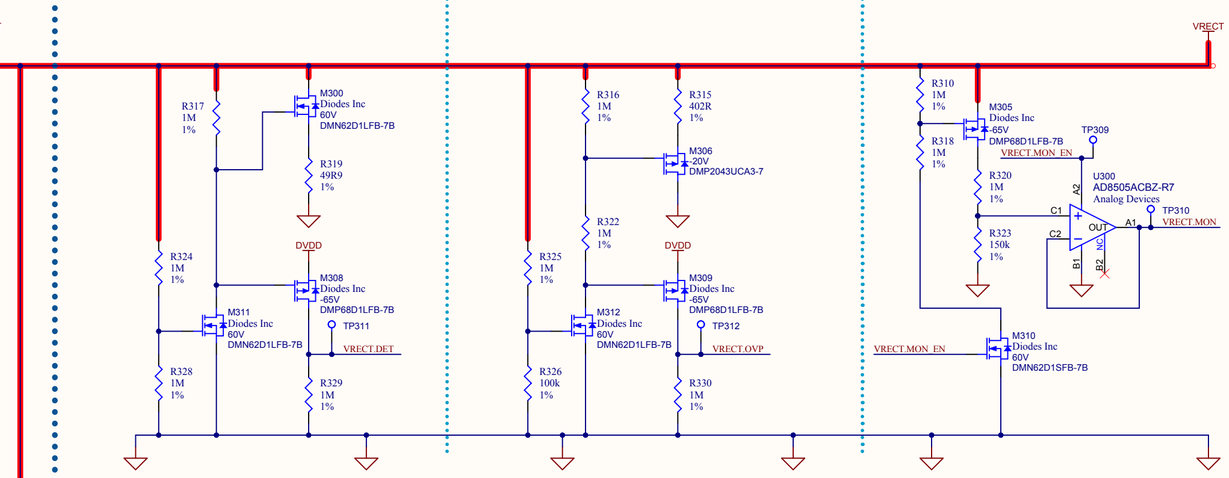


Protections

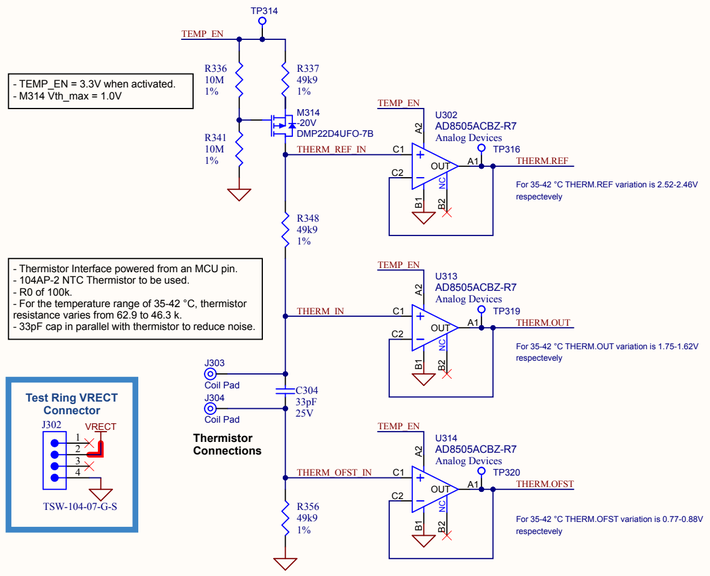
Dummy Load

VRECT Over-Voltage Protect

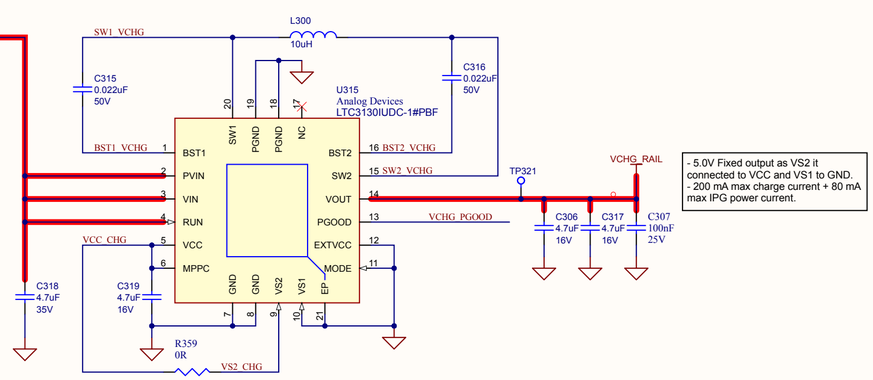
VRECT Monitor



Thermistor Interface



VCHG_RAIL Supply



Interconnect

Outputs

VCHG_PGOOD → VCHG_PGOOD

VRECT Mon Interface

VRECT.MON_EN → MON_EN
VRECT.MON → MON
VRECT.DET → DET
VRECT.OVP → OVP
(MON_EN, MON, DET, OVP) → VRECT

Thermal CTRL Interface

THERM.REF → REF
THERM.OUT → OUT
THERM.OFST → OFST
(REF, OUT, OFST) → THERM

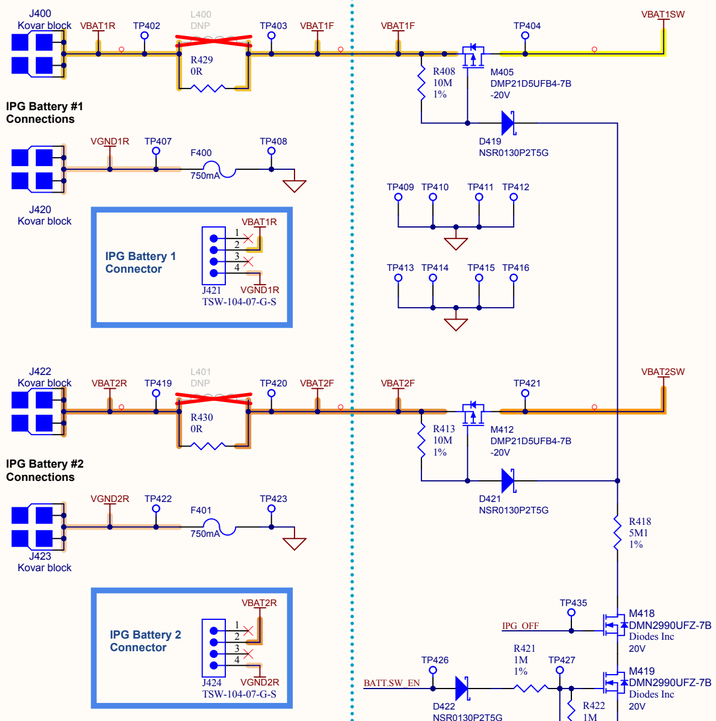
TEMP_EN → TEMP_EN

FOCUS	Project: HORNET-1-IPG.PrjPcb	
Schematic: **Wireless Power Transfer**		Ver: 1 .5
Design by: **Julian Evia**		Date: **2024-06-13**
Reviewed by: **Alvaro Rios**		Date: **2024-06-13**
Comments: WPT Rx circuit, thermistor interface and line regulation		

Battery Management

Batteries

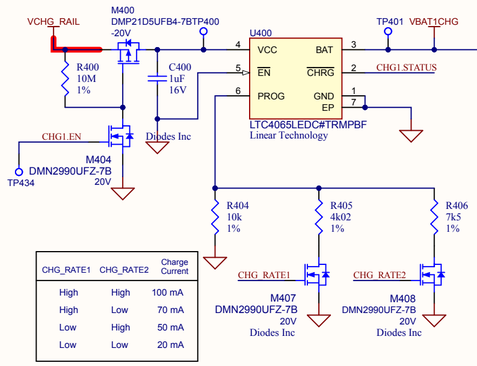
Battery Interface



Battery Connect Switches

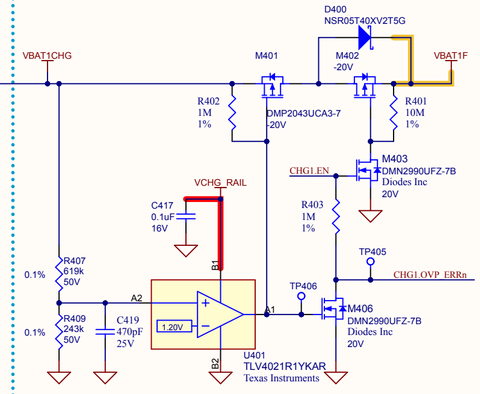
Charge control

Charge Controller 1

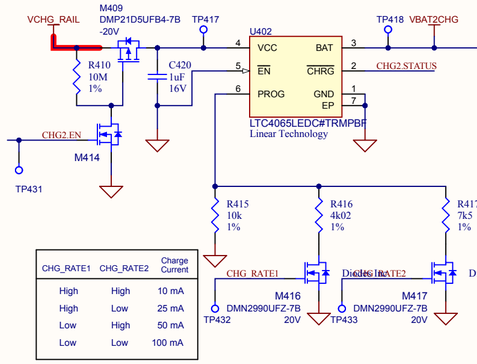


CHG_RATE1	CHG_RATE2	Charge Current
High	High	100 mA
High	Low	70 mA
Low	High	50 mA
Low	Low	20 mA

Battery 1 Over-Voltage Protection

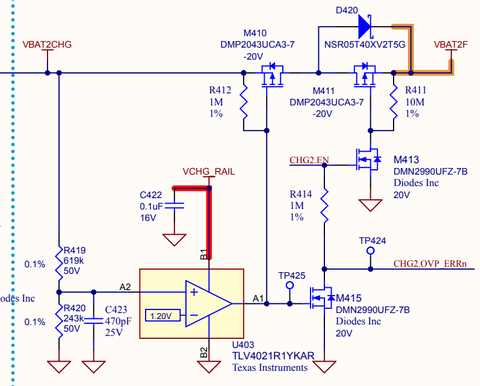


Charge Controller 2

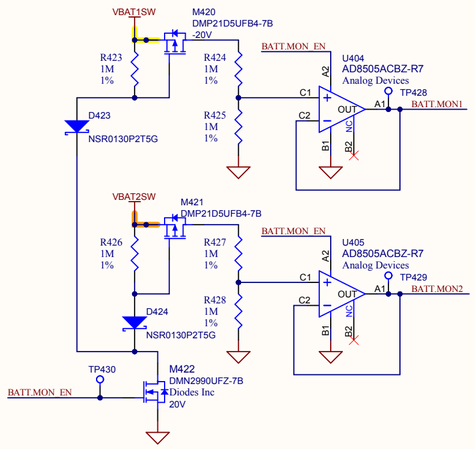


CHG_RATE1	CHG_RATE2	Charge Current
High	High	10 mA
High	Low	25 mA
Low	High	50 mA
Low	Low	100 mA

Battery 2 Over-Voltage Protection

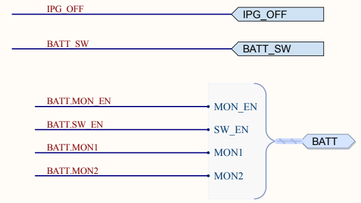


IPG Battery Monitor

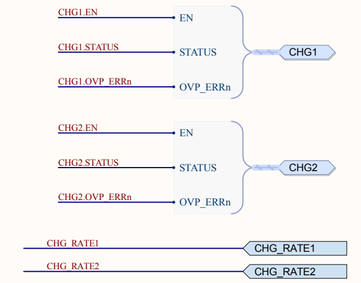


Interconnect

Batteries control interface

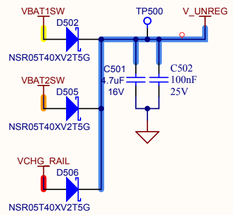


Charge control interface



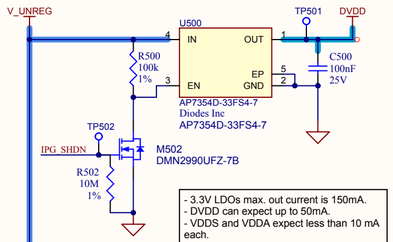
FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Battery Management**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Battery charge control and IPG main power switch.	

Main supplies



DVDD Supply

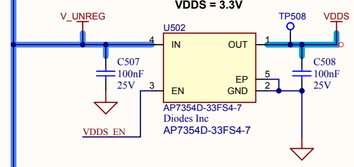
DVDD = 3.3V



- 3.3V LDOs max. out current is 150mA.
- DVDD can expect up to 50mA.
- VDDS and VDDA expect less than 10 mA each.

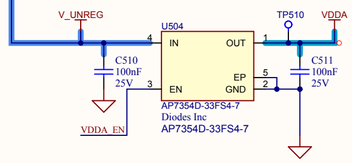
VDDS Supply

VDDS = 3.3V



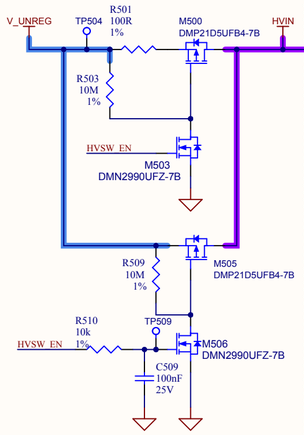
VDDA Supply

VDDA = 3.3V

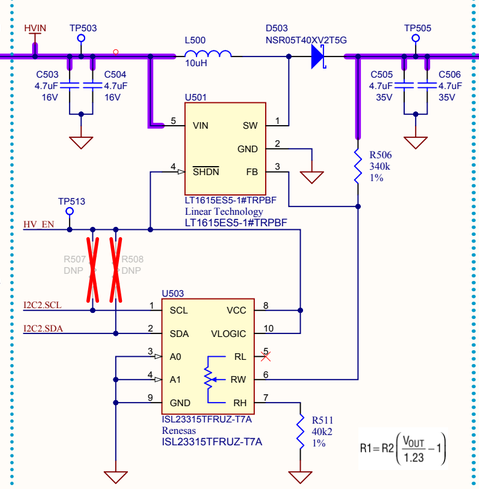


HV Input Switch

Soft start circuit. When HVSW is turned high, M506 has a 361 us delay to be turned on.

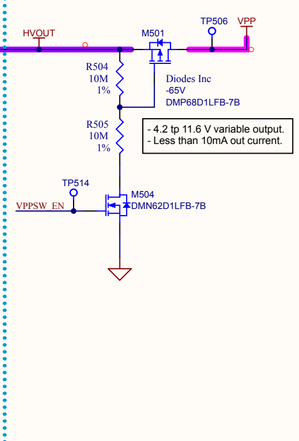


HV Supply



- Digipot drived by MCU pin since max expected supply current is 250uA.
- I2C address is 0x50.
- RW-RH 100k max. resistance.
- R1 = 340k, R2 = RW-RH + 40.2k.
- When RW-RH is 100k, output voltage is 4.2V. When RW-RH is 0, output voltage is 11.6V.

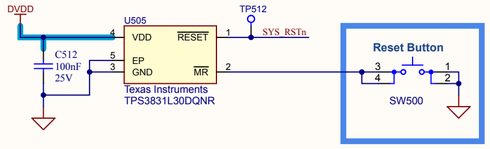
HV Switch



- 4.2 tp 11.6 V variable output.
- Less than 10mA out current.

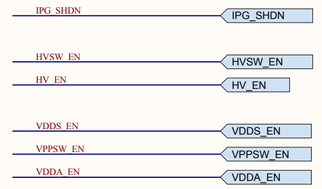
Reset monitor

Reset Threshold = 2.63V



Interconnect

Inputs

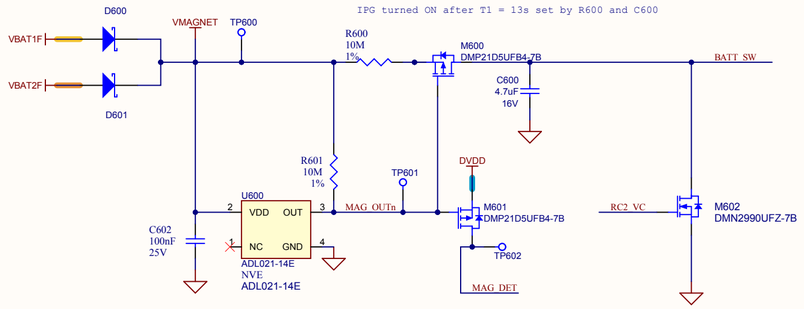


Outputs

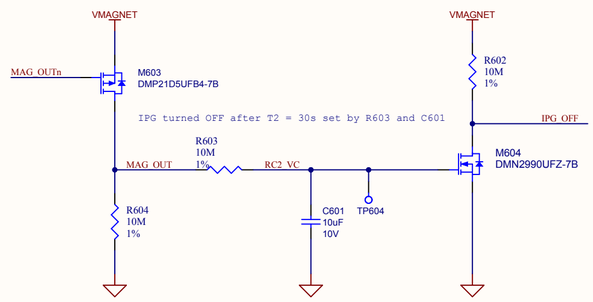
Communication

FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Power Management**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: 3.3V LDOs for digital and analog, and stimulation HV supply.	

Magnet Sensor



IPG SHDN



Interconnect

Inputs

Outputs

MAG_DET — MAG_DET

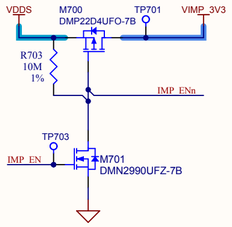
IPG_OFF — IPG_OFF

BATT_SW — BATT_SW

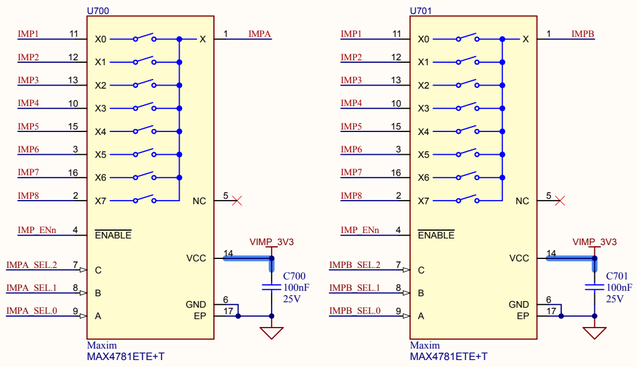
FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Magnet Sensor**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Magnet detection IPG automatic power switch.	

Impedance Measurement

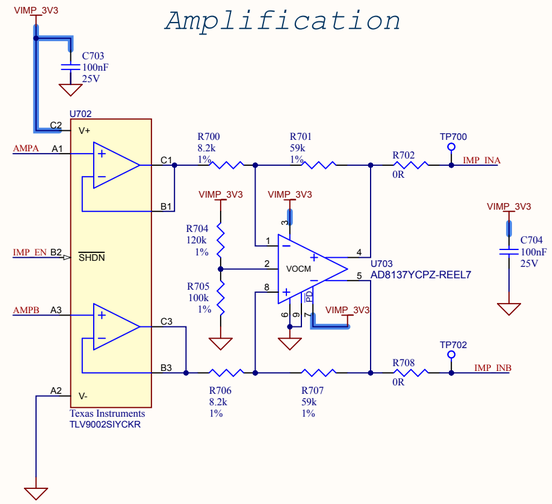
Supply CTRL



Channel selection

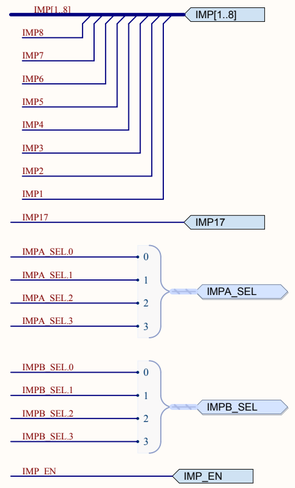


Amplification

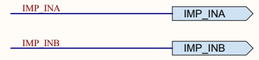


Interconnect

Inputs



Outputs

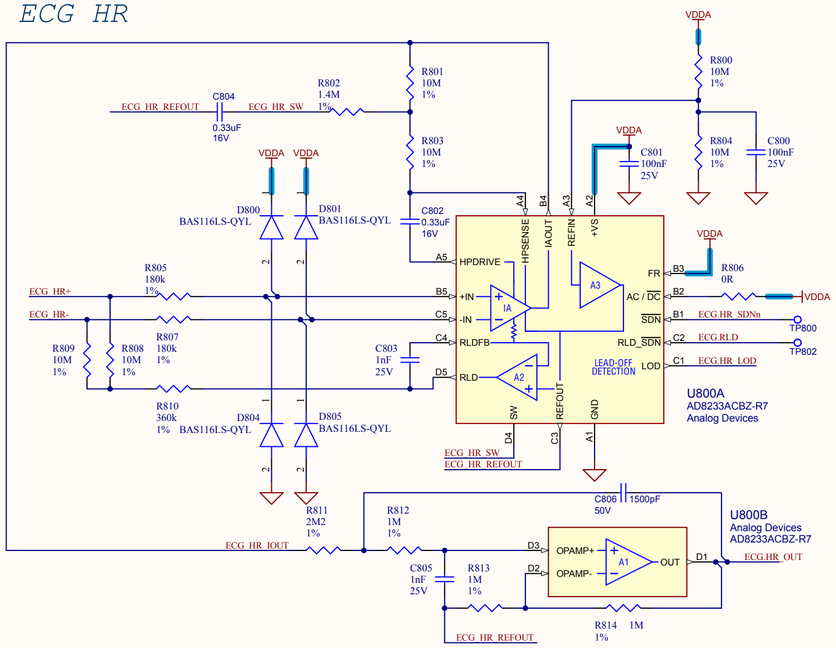


FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Impedance Measurement Circuit**	Ver: 1.5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Impedance Measurement Circuit.	

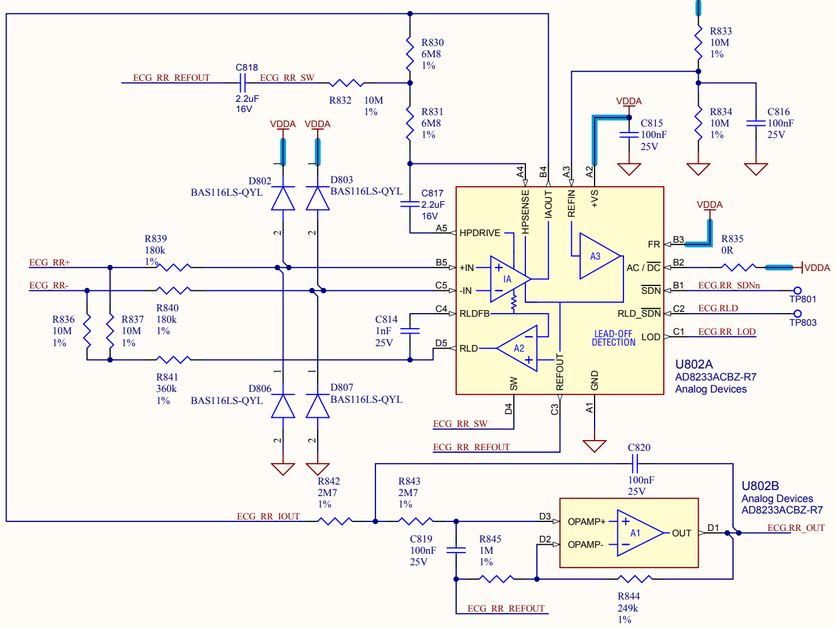
Sense Channels

Electrocardiograph

ECG HR

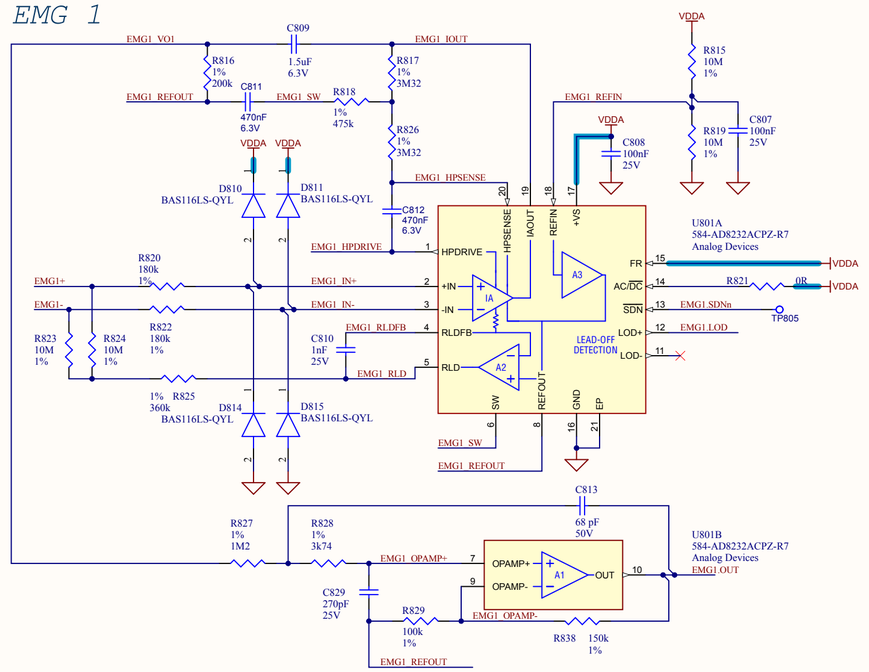


ECG RR

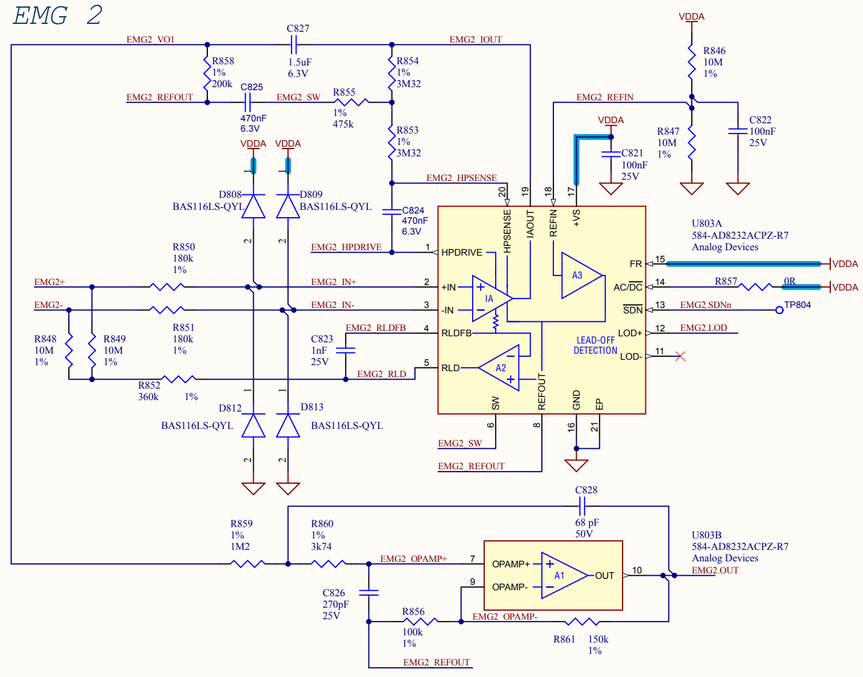


Electromyograph

EMG 1

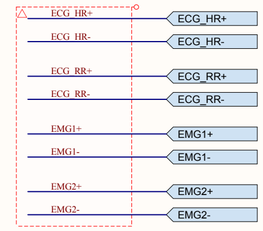


EMG 2



Interconnect

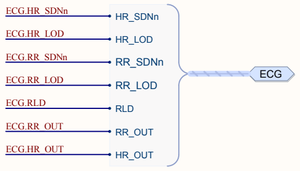
Inputs



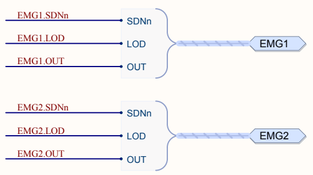
Outputs

Interfaces

ECG Monitors



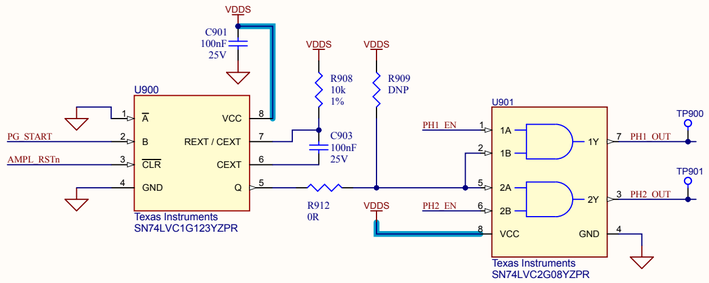
EMG Monitors



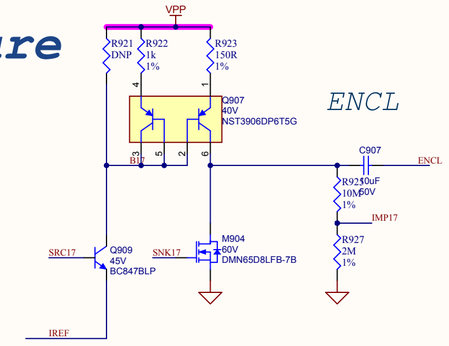
FOCUS	Project: HORNET-1-IPG.PrjPcb	
Schematic: **Sensing**		Ver: 1 .5
Design by: **Julian Evia**		Date: **2024-06-13**
Reviewed by: **Alvaro Rios**		Date: **2024-06-13**
Comments: EMG and ECGs Analog Front End.		

Stimulation

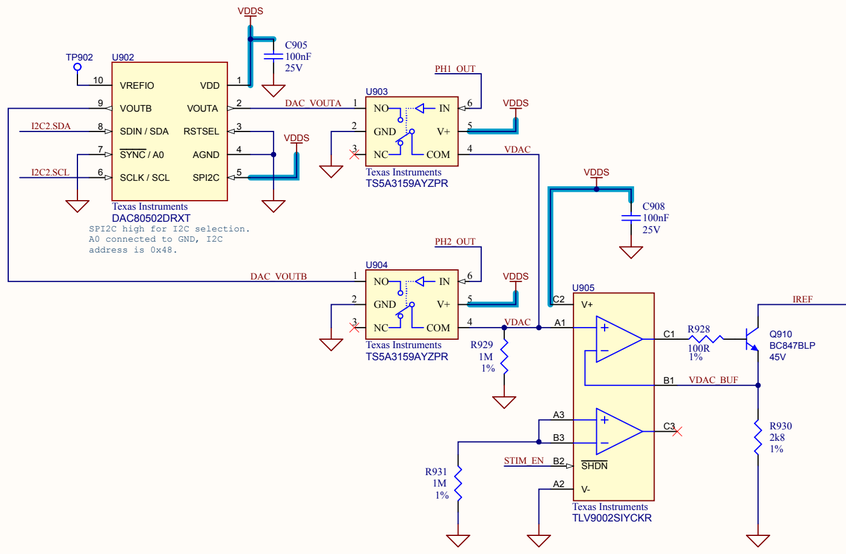
Pulse Guard



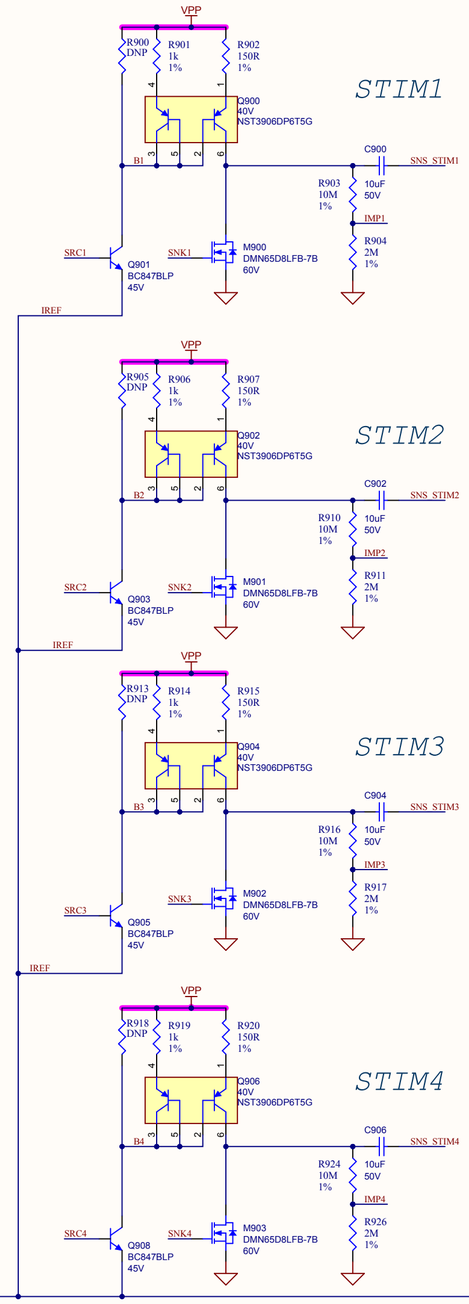
Enclosure



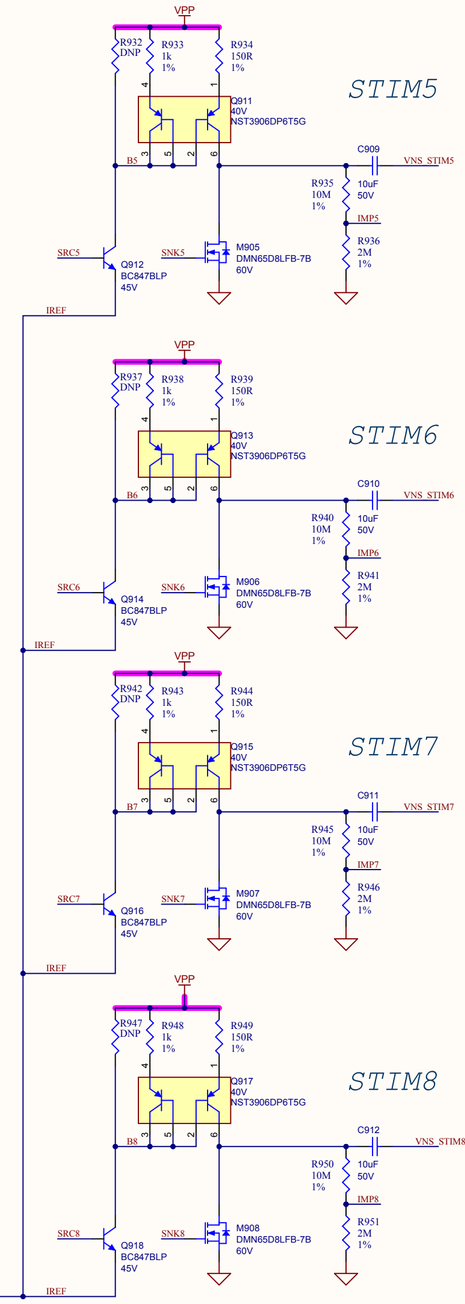
Stim Amplitude Control



Spinal Cord Stimulation CHs



Vagus Nerve Stimulation CHs

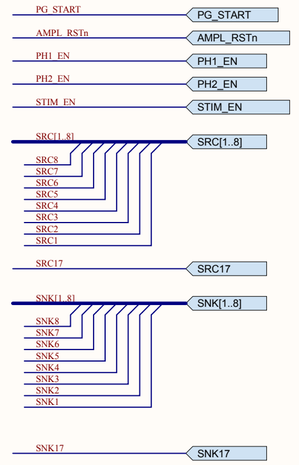


STIM CH 1-4

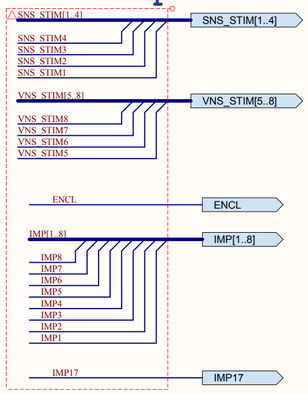
STIM CH 5-8

Interconnect

Inputs



Outputs



Communication

FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Stimulation**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Vague and sacral nerve stimulation channels.	

Electrodes

Interconnect

Enclosure

ENCL — ENCL

Channels

SNS_STIM1 — SNS_STIM1
SNS_STIM2 — SNS_STIM2
SNS_STIM3 — SNS_STIM3
SNS_STIM4 — SNS_STIM4
CH5 — CH5
CH6 — CH6
CH7 — CH7
CH8 — CH8
EMG1+ — EMG1+
EMG1- — EMG1-
CH10 — CH10
CH12 — CH12
XL_SCL — XL_SCL
XL_SDA — XL_SDA
XL_ACC — XL_ACC
XL_GND — XL_GND

CH1-CH4
SNS only stim CH

ENCL
SNS_STIM1 — J1001 FT pad — CH1
D1000 PESD5V0S1BLD,315 — C1000 680pF 100V — DEFIB_COMMON
SNS_STIM3 — J1005 FT pad — CH3
D1004 PESD5V0S1BLD,315 — C1004 680pF 100V — DEFIB_COMMON
SNS_STIM2 — J1009 FT pad — CH2
D1008 PESD5V0S1BLD,315 — C1008 680pF 100V — DEFIB_COMMON
SNS_STIM4 — J1013 FT pad — CH4
D1012 PESD5V0S1BLD,315 — C1012 680pF 100V — DEFIB_COMMON

CH5-CH8
VNS Stim CH and ENG

ENCL
CH5 — J1007 FT pad — CH5
D1006 PESD5V0S1BLD,315 — C1007 680pF 100V — DEFIB_COMMON
CH7 — J1015 FT pad — CH7
D1014 PESD5V0S1BLD,315 — C1014 680pF 100V — DEFIB_COMMON
CH6 — J1011 FT pad — CH6
D1010 PESD5V0S1BLD,315 — C1010 680pF 100V — DEFIB_COMMON
CH8 — J1003 FT pad — CH8
D1002 PESD5V0S1BLD,315 — C1002 680pF 100V — DEFIB_COMMON

VNSA
VNSB

CH9-CH12

ENCL
EMG1+ — J1002 FT pad — CH9
D1001 PESD5V0S1BLD,315 — C1001 680pF 100V — DEFIB_COMMON
EMG1- — J1006 FT pad — CH11
D1005 PESD5V0S1BLD,315 — C1005 680pF 100V — DEFIB_COMMON
CH10 — J1010 FT pad — CH10
D1009 PESD5V0S1BLD,315 — C1009 680pF 100V — DEFIB_COMMON
CH12 — J1014 FT pad — CH12
D1013 PESD5V0S1BLD,315 — C1013 680pF 100V — DEFIB_COMMON

Enclosure

ENCL
J1000 FT pad — ENCL
2.4GHz GND-ENCL Return path capacitor — C1016 25V 68pF
D1016 PESD5V0S1BLD,315 — DEFIB_COMMON

J1017
ENCL — 1 — 2
105-0753-001

CH13-CH16

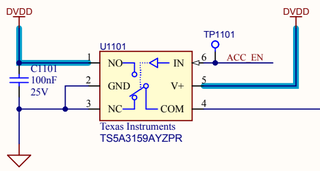
XL_SCL — J1004 FT pad — CH13
D1003 PESD5V0S1BLD,315 — C1003 680pF 100V — DEFIB_COMMON
XL_SDA — J1008 FT pad — CH15
D1007 PESD5V0S1BLD,315 — C1006 680pF 100V — DEFIB_COMMON
XL_ACC — J1012 FT pad — CH14
D1011 PESD5V0S1BLD,315 — C1011 680pF 100V — DEFIB_COMMON
XL_GND — J1016 FT pad — CH16
D1015 PESD5V0S1BLD,315 — C1015 680pF 100V — DEFIB_COMMON

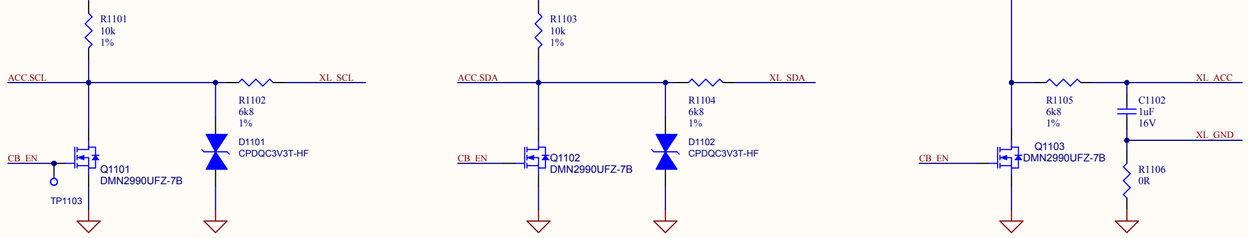
External Tip Jack Interface

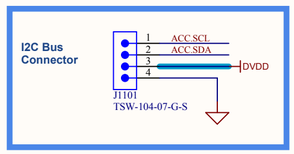
SNS_STIM1 — J1018 — 105-0753-001	CH8 — J1020 — 105-0753-001	EMG1+ — J1019 — 105-0753-001	XL_SCL — J1021 — 105-0753-001
SNS_STIM3 — J1022 — 105-0753-001	CH5 — J1024 — 105-0753-001	EMG1- — J1023 — 105-0753-001	XL_SDA — J1025 — 105-0753-001
SNS_STIM2 — J1026 — 105-0753-001	CH6 — J1028 — 105-0753-001	CH10 — J1027 — 105-0753-001	XL_ACC — J1029 — 105-0753-001
SNS_STIM4 — J1030 — 105-0753-001	CH7 — J1032 — 105-0753-001	CH12 — J1031 — 105-0753-001	XL_GND — J1033 — 105-0753-001

FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Electrodes**	Ver: 1 .5
Design by: **Julian Evia**	Date: **2024-06-13**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Feedthrough electrode connection with defibrilation and EMI protections.	

Digital Sense Channel







Interconnect

Inputs

ACC_EN → ACC_EN

CB_EN → CB_EN

Outputs

XL_SCL → XL_SCL

XL_SDA → XL_SDA

XL_ACC → XL_ACC

XL_GND → XL_GND

Communication

ACC SCL → SCL

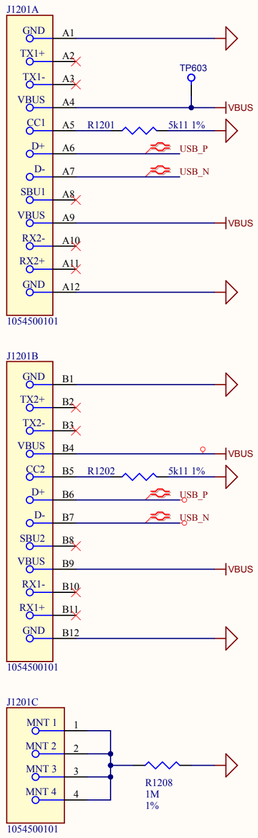
ACC SDA → SDA

ACC

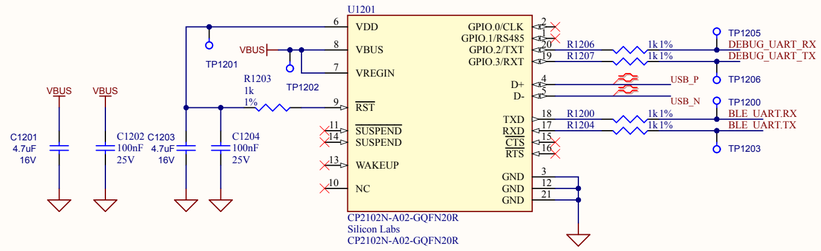
FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Digital Sense Channel**	Ver: 1 .5
Design by: **Julian Evia**	Date: **18/12/2023**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: External digital accelerometers I2C channel.	

Test Fixture

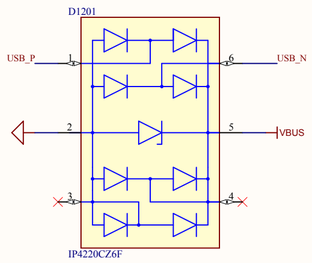
USB-C Connector



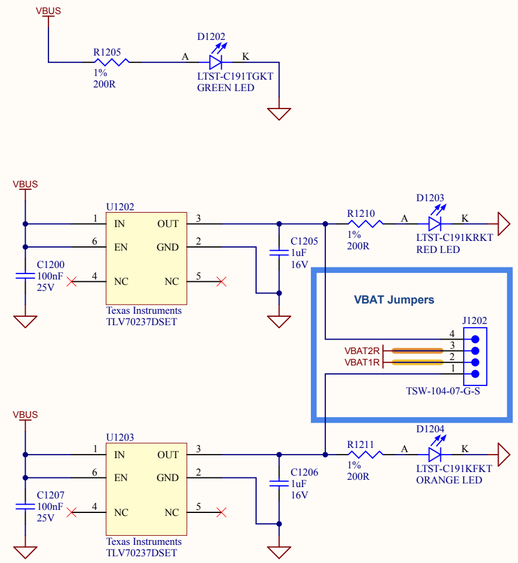
USB to Serial adaptor



ESD Protections

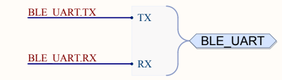


3.7V LDOs

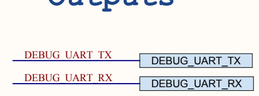


Interconnect

Inputs



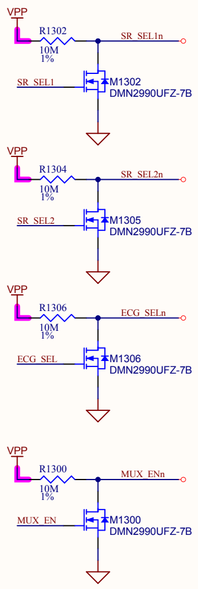
Outputs



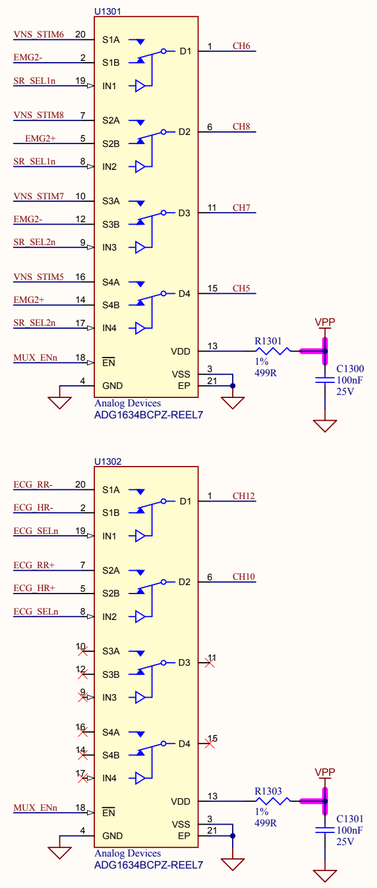
FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Test Fixture**	Ver: 1 .5
Design by: **Julian Evia**	Date: **26/12/2023**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: External text fixture for the IPG.	

Output Multiplexing

Level shifters

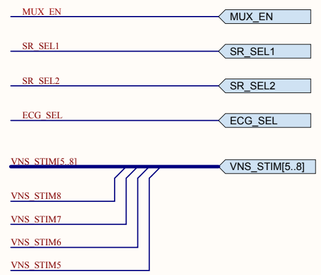


MUXs

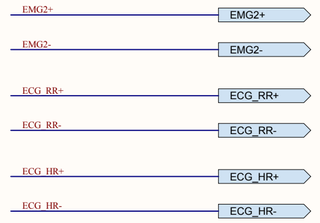


Interconnect

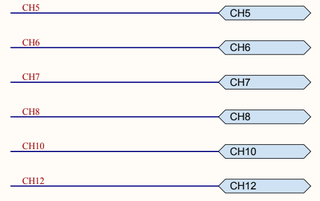
Inputs



Outputs



Outputs



FOCUS	Project: HORNET-1-IPG.PrjPcb
Schematic: **Output Multiplexing**	Ver: 1 .5
Design by: **Julian Evia**	Date: **29/12/2023**
Reviewed by: **Alvaro Rios**	Date: **2024-06-13**
Comments: Output/Input stage for the sensing and stim. channels	