HORNET-IPG

Revision Log

Ver	Date	Description	Author	Reviewer
2.0.A	2025-04-02	HORNET 2 initial version built upon HORNET 1.	M. Ferreira	J. Evia
2.1.A	2025-04-10	Fix battery PTH position after MedAlly feedback.	M. Ferreira	J. Evia
2.1.B	2025-05-09	Implement DFM recommedations.	M. Ferreira	J. Evia

Mechanical & Miscellaneous

Fiducial Markers

BOTTOM

- X100 FIDUCIAL
- X101 FIDUCIAL
- X102 FIDUCIAL

TOP

- X103 FIDUCIAL
- X104 FIDUCIAL
- X105 FIDUCIAL

Mounting holes

- X106 HOLE, UNPLATED
- X107 HOLE, UNPLATED
- X108 HOLE, UNPLATED

Power Net Reference

WPT and Bat charge

+VCARR +VRECT +VCHG_RAIL

Battery 1

+VBAT1R +VBAT1F +VBAT1SW

Stim. Power Supplies

+HVIN +HVOUT +VPP

Battery 2

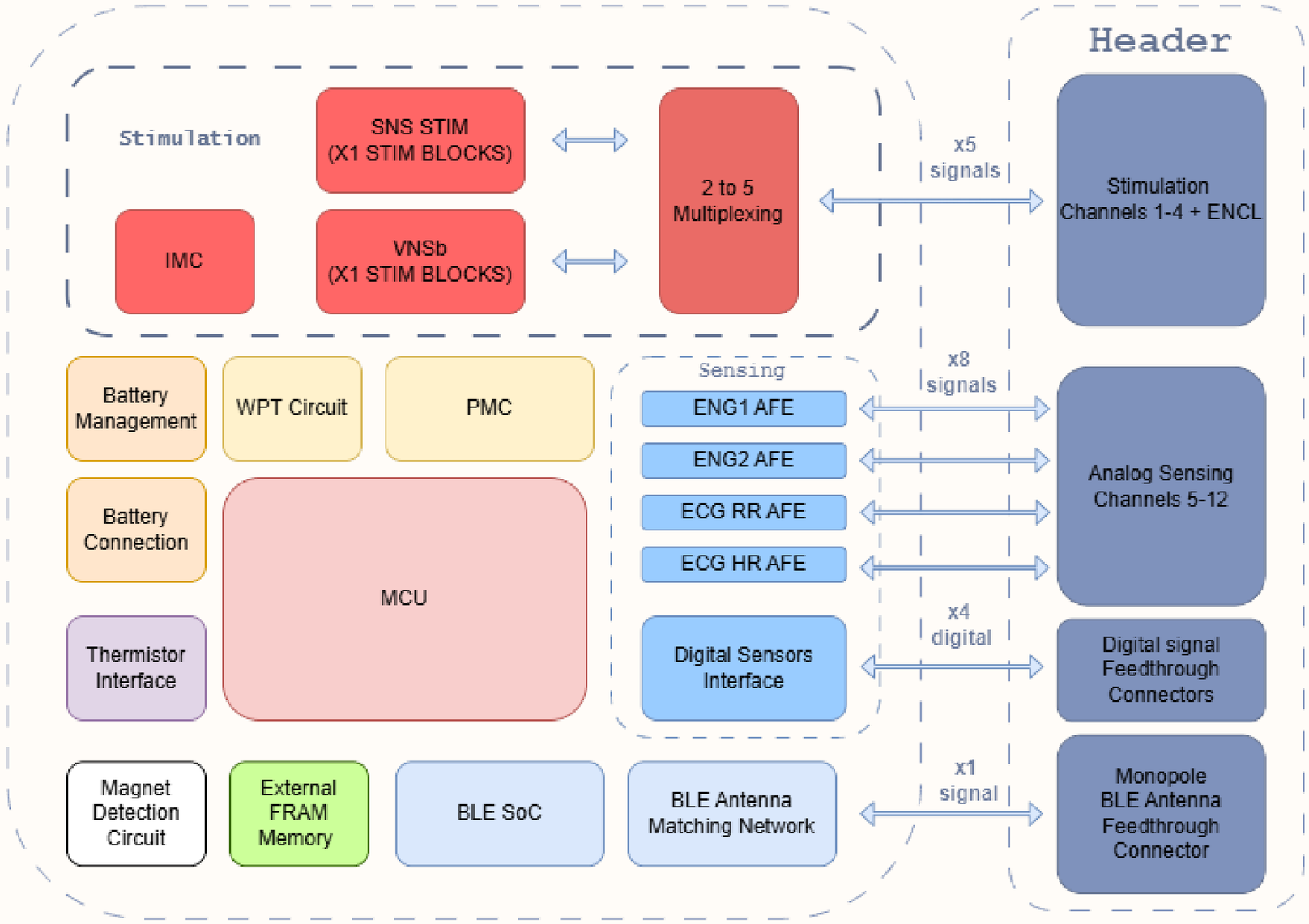
+VBAT2R +VBAT2F +VBAT2SW

3.3 V Power Supplies

+DVDD +VDDA +VDDS +V_UNREG

Design considerations

High Level Block Diagram



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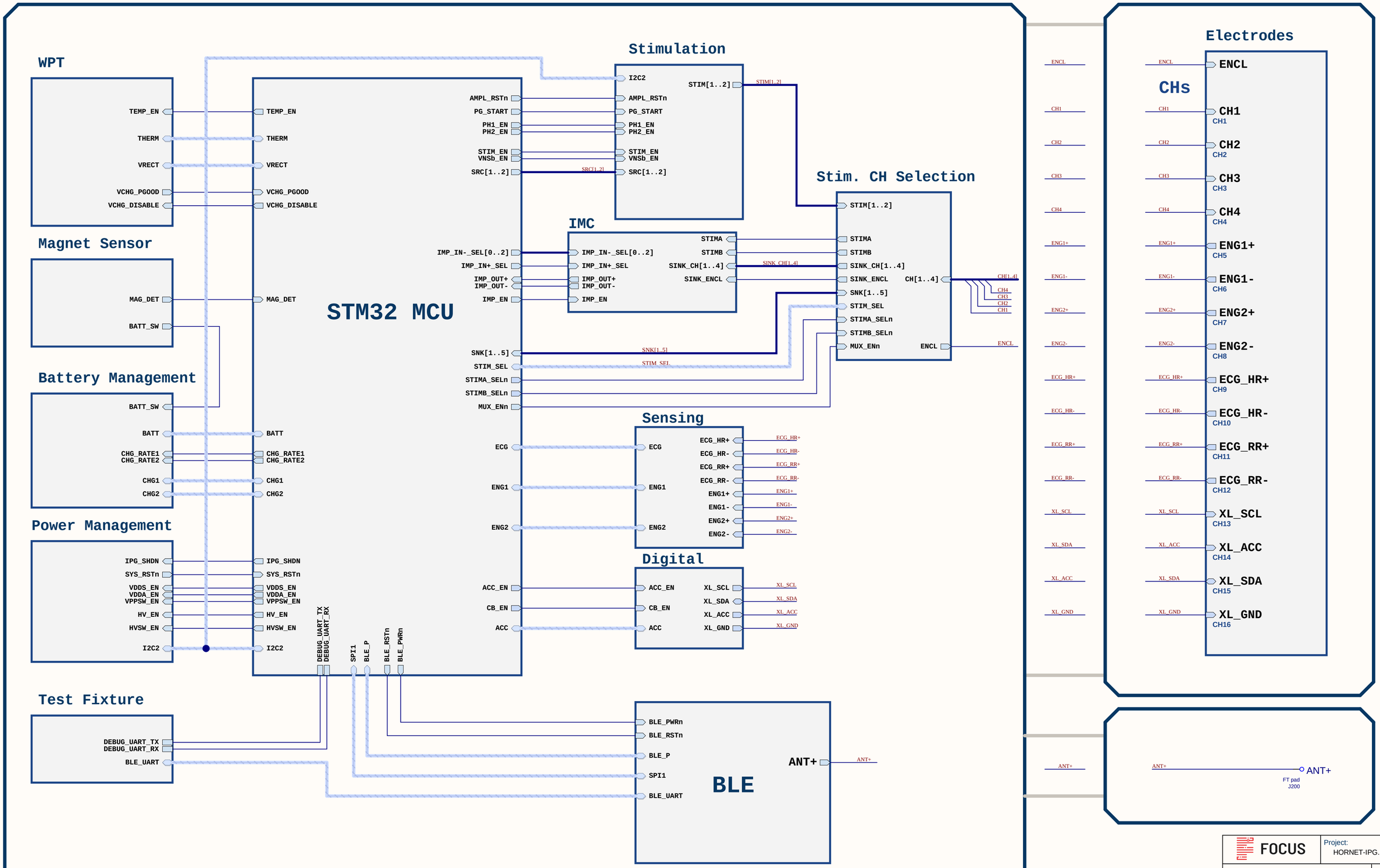
FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Cover Page**	Ver: 2.1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments:	

System Block Diagram



FOCUS		Project: HORNET-IPG.PrjPcb	
Schematic: **System Block Diagram**		Ver: 2 .1	
Design by: **M. Ferreira**		Date: **2025-05-09**	
Reviewed by: **J. Evia**		Date: **2025-05-09**	
Comments:			

STM32U5 MCU

Serial Debug Interface

DEBUG_UART_TX ↔ DEBUG_UART_TX
DEBUG_UART_RX ↔ DEBUG_UART_RX

Batt Monitor

BATT: MON_EN → BATT.MON_EN, SW_EN → BATT.SW_EN, MON1 → BATT.MON1, MON2 → BATT.MON2

Microcontroller

STM Programming Interface — J301 FTSH-105-01-F-D-K

+DVDD	1	2	SWDIO → TP300
	3	4	SWCLK → TP301
	5	6	SWO → TP305
	7	8	
	9	10	SYS_RSTn

Power Management

I2C2 shared with stimulation DAC: I2C2 (SDA, SCL), VPPSW_EN, HV_EN, HVSW_EN, VDDA_EN, VDDS_EN

Digital Sense

ACC.SCL, ACC.SDA → ACC (SCL, SDA)
ACC_EN → ACC_EN
CB_EN → CB_EN

Wireless Power Transfer

VCHG_DISABLE → VCHG_DISABLE
VCHG_PGOOD → VCHG_PGOOD

Temperature CTRL

TEMP_EN → TEMP_EN
THERM: REF → THERM.REF, OUT → THERM.OUT, OFST → THERM.OFST

Rectification

VRECT: MON_EN → VRECT.MON_EN, MON → VRECT.MON, DETn → VRECT.DETn, OVPn → VRECT.OVPn

+DVDD
C300 12pF 25V
C301 12pF 25V
Y300 48 MHz
R300 10k 1%
R301 10k 1%
SYS_RSTn → SYS_RSTn

IMP_OUT-, IMP_OUT+, IMP_IN-_SEL2, IMP_IN-_SEL1, IMP_EN, IMP_IN-_SEL0, IMP_IN+_SEL

R302 0R
C302 4.7uF 16V
L300 2.2uH
R303 0R
C303 4.7uF 16V

VDDSMPS is used. If R103 is not populated, M9 pin should be connected to GND.

NRST, BOOT0 / PH3, OSC_OUT / PH1, OSC_IN / PH0, ADC4_IN6 / PF15, ADC4_IN5 / PF14, PF13, PF12, PF11, PF5, PF4, PF3, WKUP8 / I2C2_SMBA / PF2, I2C2_SCL / PF1, I2C2_SDA / PF0, OPAMP1_VINM, OPAMP2_VINM, VSSSMPS, VBAT

U301

BATT.SW_EN	A11	PA15 / JTDI / SPI1_NSS / SPI3_NSS	
SWCLK	C11	PA14 / JTCK / SWCLK	
SWDIO	C10	PA13 / JTMS / SWDIO	
IPG_SHDN	B12	PA12 / USART1_RTS / SPI1_MOSI	
BLE_PWRn	C12	PA11 / USART1_CTS / SPI1_MISO	
TP302 DEBUG_UART_RX	D11	PA10 / USART1_RX	
TP303 DEBUG_UART_TX	D10	PA9 / USART1_TX / SPI2_SCK	
FRAM_EN	D12	PA8 / USART1_CK	
SPI1 shared between FRAM and the BLE module: SPI1.MOSI	K3	PA7 / ADC1_IN12 / ADC4_IN20 / SPI1_MOSI / I2C3_SCL / WKUP8	
SPI1.MISO	L2	PA6 / ADC1_IN11 / ADC4_IN11 / SPI1_MISO / WKUP7	
SPI1.SCK	M1	PA5 / ADC1_IN10 / ADC4_IN10 / SPI1_SCK / WKUP6	
SPI1.FRAM_CSn	L3	PA4 / ADC1_IN9 / ADC4_IN9 / SPI1_NSS / SPI3_NSS / WKUP2	
MAG_DET	L1	PA3 / ADC1_IN8 / LPUART1_RX / WKUP5	
BATT.MON_EN	K2	PA2 / ADC1_IN7 / LPUART1_TX / WKUP4	
BATT.MON2	G4	PA1 / ADC1_IN6 / UART4_RX / WKUP3 / SPI1_SCK	
BATT.MON1	J2	PA0 / ADC1_IN5 / UART4_TX / WKUP1	
VPPSW_EN	K12	PB15 / SPI2_MOSI / WKUP7	
I2C2.SDA	K11	PB14 / SPI2_MISO / I2C2_SDA	
I2C2.SCL	K10	PB13 / SPI2_SCK / I2C2_SCL	
HV_EN	L11	PB12 / SPI2_NSS / I2C2_SMBA	
HVSW_EN	L9	PB11 / LPUART1_TX / I2C4_SDA / I2C2_SDA	
VDDA_EN	K9	PB10 / LPUART1_RX / SPI2_SCK / I2C4_SCL / I2C2_SCL / WKUP8	
VDDS_EN	A4	PB9 / I2C1_SDA / SPI2_NSS	
ENG1.SDNn	C5	PB8 / I2C1_SCL / WKUP5	
	D5	PB7 / USART1_RX / I2C4_SDA / I2C1_SDA / WKUP4	
ENG1.LOD	A5	PB6 / USART1_TX / I2C4_SCL / I2C1_SCL / WKUP3	
ECG.HR_SDNn	D6	PB5 / USART1_CK / SPI1_MOSI / SPI3_MOSI / WKUP6	
ECG.RLD	B6	PB4 / NJTRST / USART1_CTS / SPI1_MISO / SPI3_MISO / I2C3_SDA	
SWO	C6	PB3 / SWO / JTDO / USART1_RTS / SPI1_SCK / SPI3_SCK / I2C1_SDA	
ENG1.OUT	K4	PB2 / ADC1_IN17 / WKUP1	
ECG.RR_OUT	L4	PB1 / ADC1_IN16 / ADC4_IN19 / WKUP4	
ECG.HR_OUT	M4	PB0 / ADC1_IN15 / ADC4_IN18 / SPI1_NSS	
C305 12pF 25V, C306 12pF 25V, Y301 32.768kHz	D1	PC15 / OSC32_OUT	
	C1	PC14 / OSC32_IN	
ECG.HR_LOD	C3	PC13 / WKUP2	
ECG.RR_SDNn	B10	PC12 / UART5_TX / USART3_CK / SPI3_MOSI	
ECG.RR_LOD	A10	PC11 / UART4_RX / USART3_RX / SPI3_MISO	
VRECT.MON_EN	B11	PC10 / UART4_TX / USART3_TX / SPI3_SCK	
VCHG_PGOOD	E11	PC9	
VCHG_DISABLE	E12	PC8	
VRECT.DETn	E10	PC7	
VRECT.OVPn	F11	PC6	
TEMP_EN	J3	PC5 / ADC1_IN14 / ADC4_IN23 / WKUP5	
VRECT.MON	M3	PC4 / ADC1_IN13 / ADC4_IN22	
	F4	PC3 / ADC1_IN4 / ADC4_IN4 / SPI2_MOSI	
THERM.REF	F3	PC2 / ADC1_IN3 / ADC4_IN3 / SPI2_MISO	
THERM.OUT	G3	PC1 / ADC1_IN2 / ADC4_IN2 / SPI2_MOSI / LPUART1_TX / I2C3_SDA	
THERM.OFST	H2	PC0 / ADC1_IN1 / ADC4_IN1 / LPUART1_RX / I2C3_SCL	
	B4	VDD11	VDD11
	M9	VDDSMPS	VDDSMPS
	M10	VLXSMPS	VLXSMPS
	A6	SPI3_NSS / USART1_RTS / PG12	BLE_P1
	M11	VDD11	VDD11
	C7	SPI3_MISO / USART1_RX / PG10	ACC_EN
	B7	SPI3_SCK / USART1_TX / PG9	CB_EN
	F12	I2C3_SDA / LPUART1_RX / PG8	ACC.SDA
	F10	I2C3_SCL / LPUART1_TX / PG7	ACC.SCL
	F9	I2C3_SMBA / LPUART1_RTS / PG6	BLE_RSTn
	G12	LPUART1_CTS / SPI1_NSS / PG5	SPI1.BLE_CSn
	G9	SPI1_MOSI / PG4	BLE_P2
	G11	SPI1_MISO / PG3	
	G10	SPI1_SCK / PG2	ENG2.SDNn
	K6	ADC4_IN8 / PG1	ENG2.LOD
	M6	ADC4_IN7 / PG0	ENG2.OUT
	L8	SPI1_MOSI / PE15	CHG2.STATUS
	K8	SPI1_MISO / PE14	CHG1.STATUS
	M8	SPI1_SCK / PE13	CHG2.OVP_ERRn
	J8	SPI1_NSS / PE12	CHG1.OVP_ERRn
	L7	PE11	CHG2.EN
	J7	PE10	CHG1.EN
	M7	PE9	CHG_RATE2
	J6	WKUP7 / PE8	CHG_RATE1
	K7	WKUP6 / PE7	MUX_ENn
	C2	WKUP3 / PE6	PG_START
	A1	WKUP2 / PE5	PH1_EN
	B2	WKUP1 / PE4	PH2_EN
	A2	PE3	AMPL_RSTn
	B3	PE2	STIM_EN
	A3	PE1	VNSb_EN
	C4	PE0	
	H12	PD15	
	H10	PD14	
	H11	I2C4_SDA / ADC4_IN17 / PD13	STIMB_SELn
	J12	I2C4_SCL / USART3_RTS / ADC4_IN16 / PD12	STIMA_SELn
	J11	I2C4_SMBA / USART3_CTS / ADC4_IN15 / PD11	STIM_SEL.ENCLn
	M12	USART3_CK / PD10	STIM_SEL.CH4n
	J10	USART3_RX / PD9	STIM_SEL.CH3n
	L12	USART3_TX / PD8	STIM_SEL.CH2n
	D7	USART2_CK / PD7	STIM_SEL.CH1n
	A7	SPI3_MOSI / USART2_RX / PD6	SNK5
	A8	USART2_TX / PD5	SNK4
	B8	SPI2_MOSI / USART2_RTS / PD4	SNK3
	C8	SPI2_MISO / SPI2_SCK / USART2_CTS / PD3	SNK2
	A9	USART3_RTS / UART5_RX / PD2	SRC2
	B9	SPI2_SCK / PD1	SNK1
	C9	SPI2_NSS / PD0	SRC1

VDDUSB, VDD, VSS, VDDIO2, VDD, VSS, VDD, VSS, VDD, VSS, VREF+, VDDA, VSSA, VDD, VSS, VDD, VSS

MCU PWR

+DVDD
C307 100nF 25V
C308 100nF 25V
C309 100nF 25V
C310 100nF 25V
C311 100nF 25V
C312 100nF 25V
C313 4.7uF 16V
C314 4.7uF 16V
C315 100nF 25V
C316 100nF 25V
L301 33nH
C317 1uF 16V
C318 100nF 25V
C319 4.7uF 16V
C320 100nF 25V

STM32U585QII6Q

STMicro

Internal reference is used for ADC, therefore VREF+ pin connected to GND with decoupling cap.

IMC

IMP_OUT+ → IMP_OUT+
IMP_OUT- → IMP_OUT-
IMP_EN → IMP_EN
IMP_IN-_SEL[0..2] → IMP_IN-_SEL[0..2]
IMP_IN-_SEL2
IMP_IN-_SEL1
IMP_IN-_SEL0
IMP_IN+_SEL → IMP_IN+_SEL

Serial FRAM

FRAM_EN → TP304
C304 100nF 25V
U300 Cypress Semiconductor CY15B108QN-20LPXC
SPI1.FRAM_CSn → CS
SPI1.MISO → SO
WP
SCK → SPI1.SCK
SI → SPI1.MOSI
VSS
VDD
DNU

BLE

BLE_P1 → 1
BLE_P2 → 2
BLE_P
SPI1.MOSI → MOSI
SPI1.MISO → MISO
SPI1.SCK → SCK
SPI1.BLE_CSn → BLE_CSn
SPI1
BLE_RSTn → BLE_RSTn
BLE_PWRn → BLE_PWRn

Charge control

CHG1: CHG1.EN → EN, CHG1.STATUS → STATUS, CHG1.OVP_ERRn → OVP_ERRn
CHG_RATE2
CHG_RATE1
CHG2: CHG2.EN → EN, CHG2.STATUS → STATUS, CHG2.OVP_ERRn → OVP_ERRn

Stimulation

PG_START → PG_START
STIM_EN → STIM_EN
VNSb_EN → VNSb_EN
SNK[1..5] → SNK[1..5]
SNK5
SNK4
SNK3
SNK2
SNK1
SRC[1..2] → SRC[1..2]
SRC2
SRC1
PH2_EN → PH2_EN
PH1_EN → PH1_EN
AMPL_RSTn → AMPL_RSTn

DAC communication though I2C2 shared with digital potentiomenter in PowerManagement.

Sensing

ECG: ECG.HR_SDNn → HR_SDNn, ECG.HR_LOD → HR_LOD, ECG.RR_SDNn → RR_SDNn, ECG.RR_LOD → RR_LOD, ECG.RLD → RLD, ECG.RR_OUT → RR_OUT, ECG.HR_OUT → HR_OUT
ENG1: ENG1.SDNn → SDNn, ENG1.LOD → LOD, ENG1.OUT → OUT
ENG2: ENG2.SDNn → SDNn, ENG2.LOD → LOD, ENG2.OUT → OUT

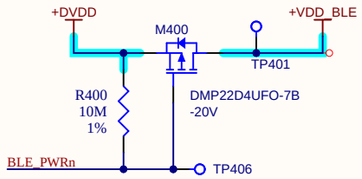
Output Multiplexing

STIM_SEL: STIM_SEL.CH1n → CH1n, STIM_SEL.CH2n → CH2n, STIM_SEL.CH3n → CH3n, STIM_SEL.CH4n → CH4n, STIM_SEL.ENCLn → ENCLn
STIMA_SELn → STIMA_SELn
STIMB_SELn → STIMB_SELn
MUX_ENn → MUX_ENn

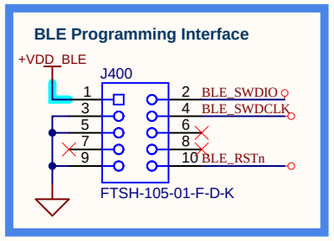
FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **MCU**	Ver: 2.1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: MCU Connections and adjasent circuit	

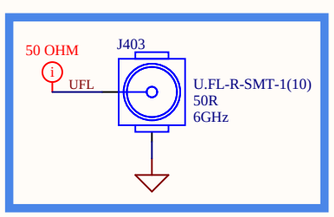
BLE Transceiver

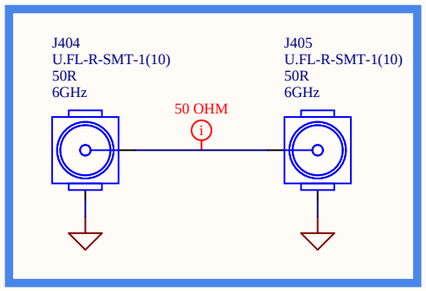
BLE PWR Control

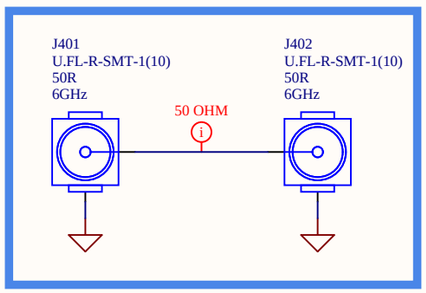


Debug Interface

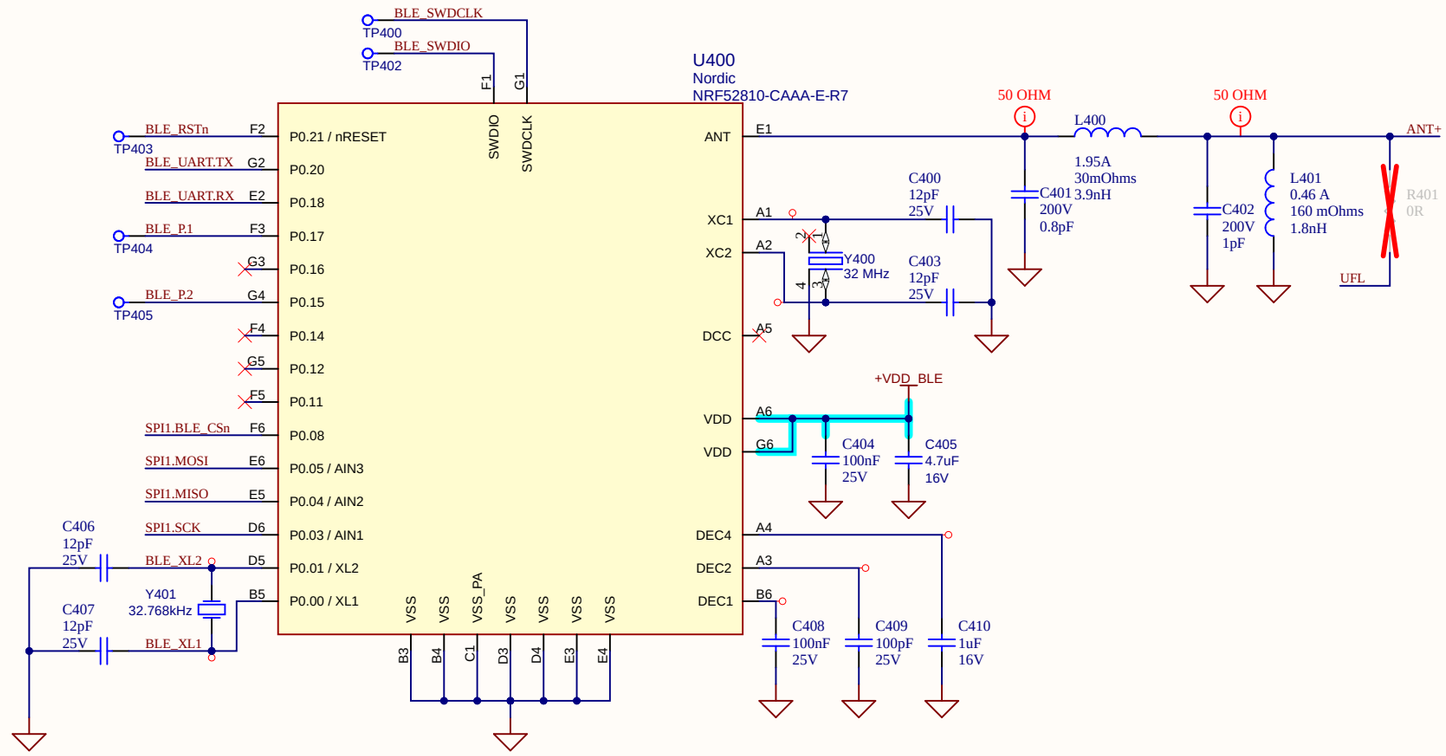






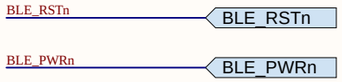


Communication dedicated SOC



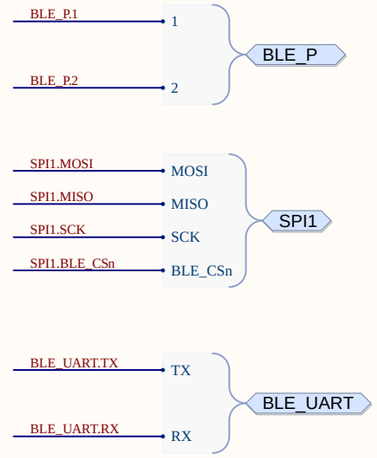
Interconnect

Inputs



Outputs

Communication

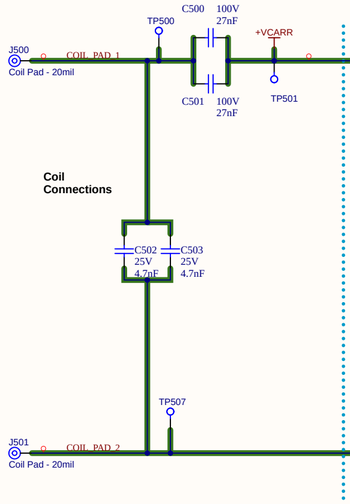


FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **BLE Transreciver**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: BLE dedicated MCU and mathcing network.	

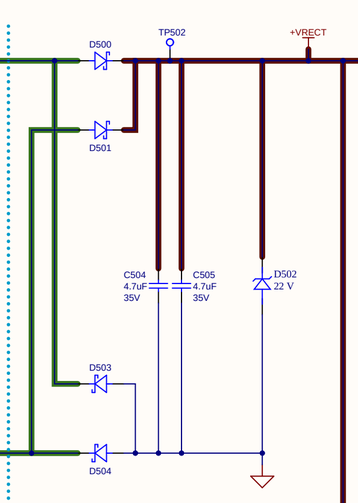
Wireless Power Transfer

Antenna and rectification

Coil Tuning

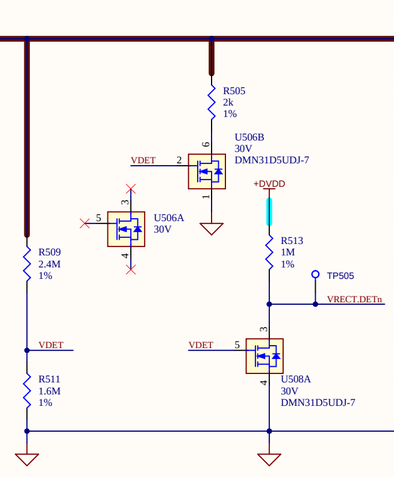


Rectifier

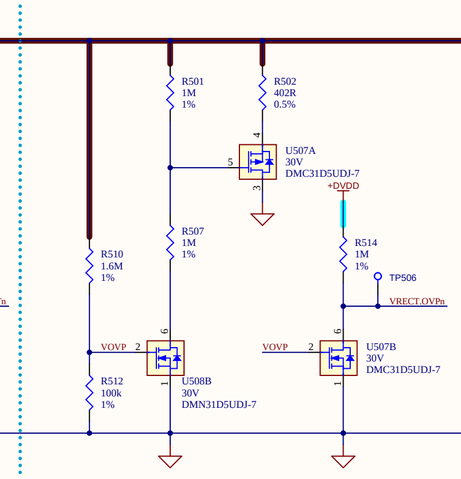


Protections

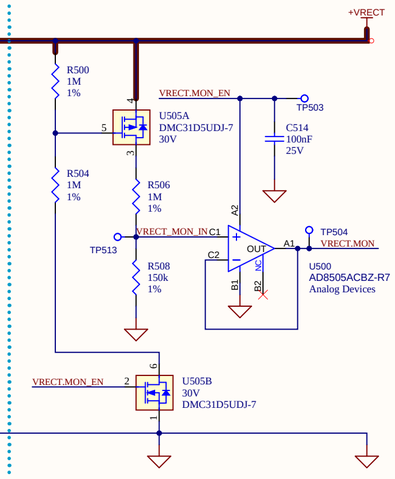
Dummy Load



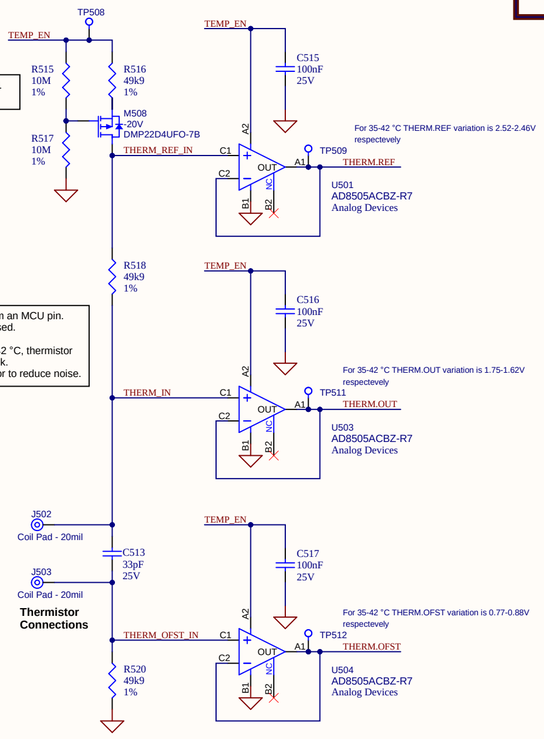
VRECT Over-Voltage Protect



VRECT Monitor



Thermistor Interface

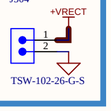


- TEMP_EN = 3.3V when activated.
- M314 Vth_max = 1.0V

- Thermistor Interface powered from an MCU pin.
- 104AP-2 NTC Thermistor to be used.
- R0 of 100k.
- For the temperature range of 35-42 °C, thermistor resistance varies from 62.9 to 46.3 k.
- 33pF cap in parallel with thermistor to reduce noise.

Test Ring VRECT Connector

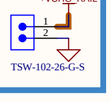
J504



TSW-102-26-G-S

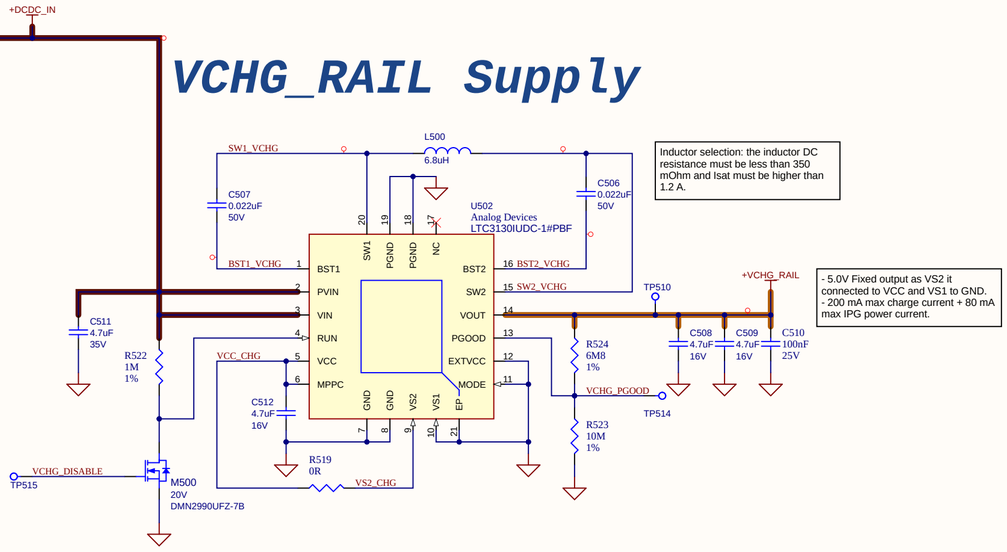
Test Ring VCHG_RAIL Connector

J505



TSW-102-26-G-S

VCHG_RAIL Supply



Inductor selection: the inductor DC resistance must be less than 350 mOhm and Isat must be higher than 1.2 A.

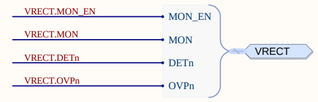
- 5.0V Fixed output as VS2 it connected to VCC and VS1 to GND.
- 200 mA max charge current + 80 mA max IPG power current.

Interconnect

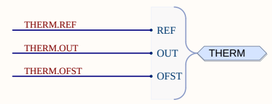
Inputs

Outputs

VRECT Mon Interface



Thermal CTRL Interface

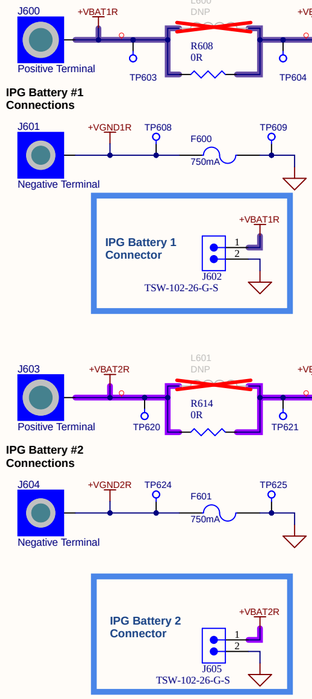


FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Wireless Power Transfer**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: WPT Rx circuit, thermistor interface and line regulation	

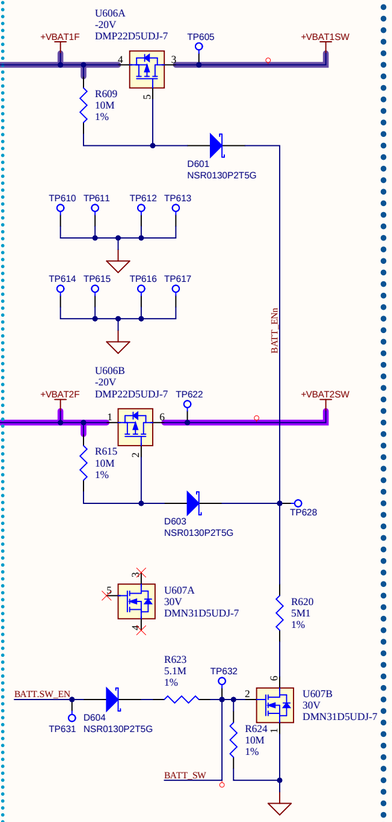
Battery Management

Batteries

Battery Interface

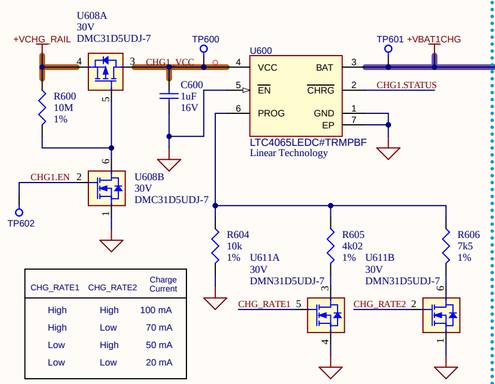


Battery Connect Switches



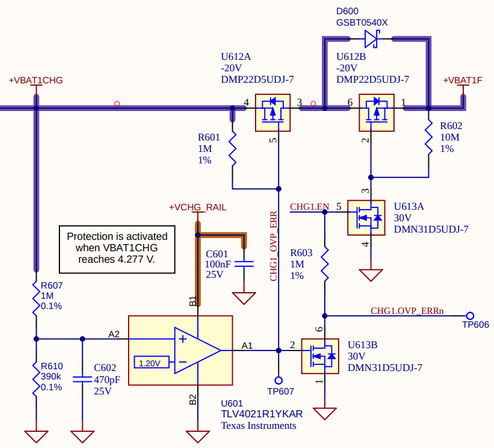
Charge control

Charge Controller 1

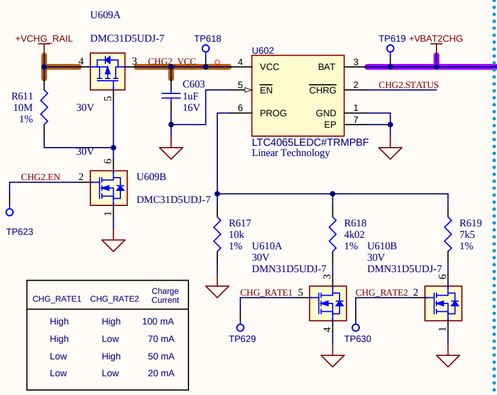


CHG_RATE1	CHG_RATE2	Charge Current
High	High	100 mA
High	Low	70 mA
Low	High	50 mA
Low	Low	20 mA

Battery 1 Over-Voltage Protection

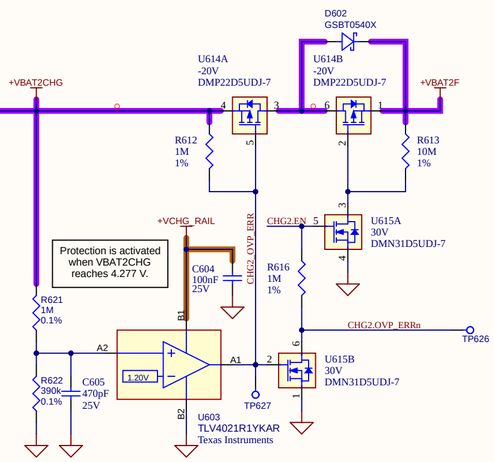


Charge Controller 2

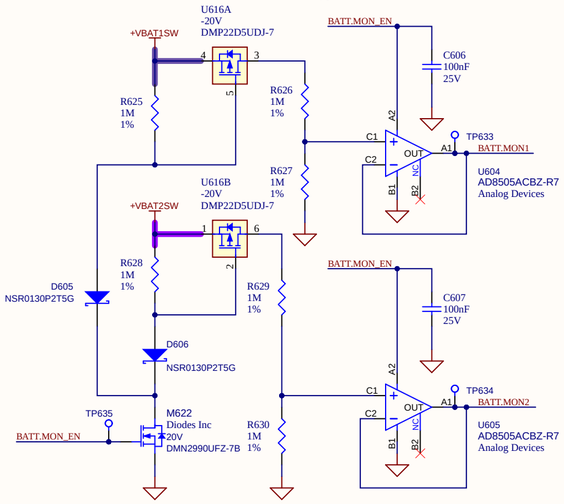


CHG_RATE1	CHG_RATE2	Charge Current
High	High	100 mA
High	Low	70 mA
Low	High	50 mA
Low	Low	20 mA

Battery 2 Over-Voltage Protection

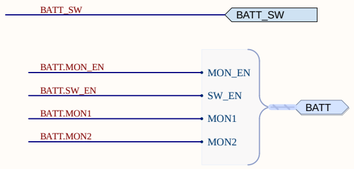


IPG Battery Monitor

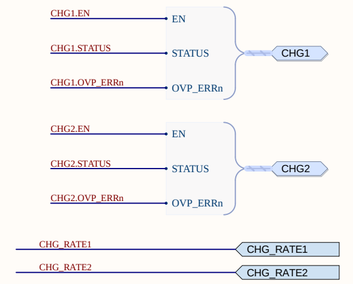


Interconnect

Batteries control interface



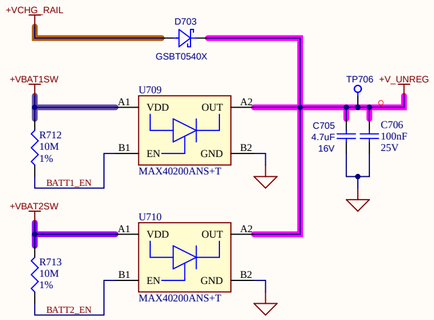
Charge control interface



FOCUS	Project: HORNET-IPG.PrjPcb	
Schematic: **Battery Management**		Ver: 2 .1
Design by: **M. Ferreira**		Date: **2025-05-09**
Reviewed by: **J. Evia**		Date: **2025-05-09**
Comments: Battery charge control and IPG main power switch.		

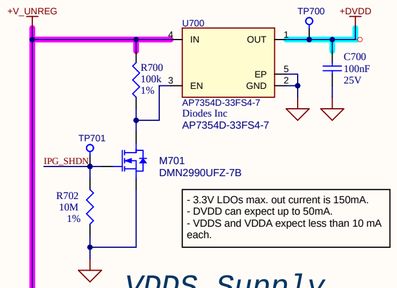
Main supplies

Power Supply Selection



DVDD Supply

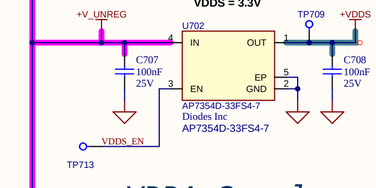
DVDD = 3.3V



- 3.3V LDOs max. out current is 150mA.
- DVDD can expect up to 50mA.
- VDDS and VDDA expect less than 10 mA each.

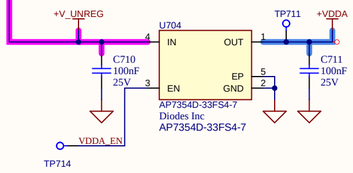
VDDS Supply

VDDS = 3.3V



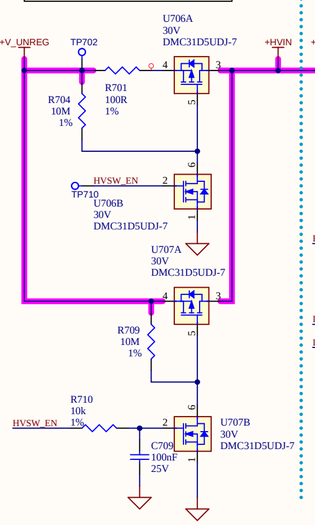
VDDA Supply

VDDA = 3.3V

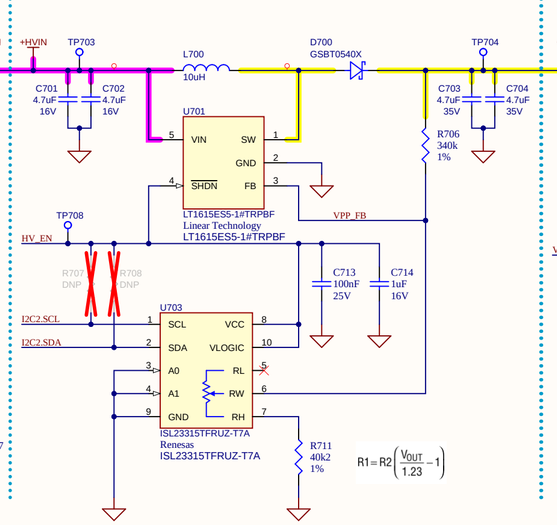


HV Input Switch

Soft start circuit. When HVSW is turned high, M506 has a 361 us delay to be turned on.



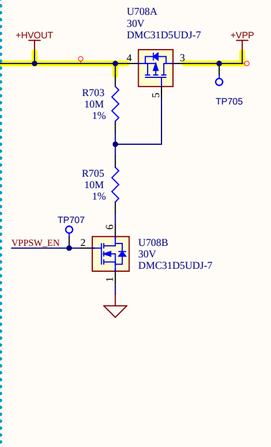
HV Supply



- Digipot drived by MCU pin since max expected supply current is 250uA.
- I2C address is 0x50.
- RW-RH 100k max. resistance.
- R1 = 340k, R2 = RW-RH + 40.2k.
- When RW-RH is 100k, output voltage is 4.2V. When RW-RH is 0, output voltage is 11.6V.

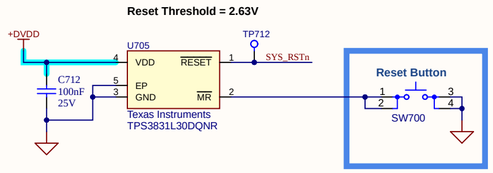
HV Switch

- 4.2 to 11.6 V variable output.
- Less than 10mA out current.



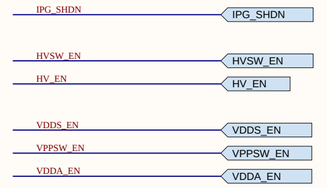
Reset monitor

Reset Threshold = 2.63V



Interconnect

Inputs

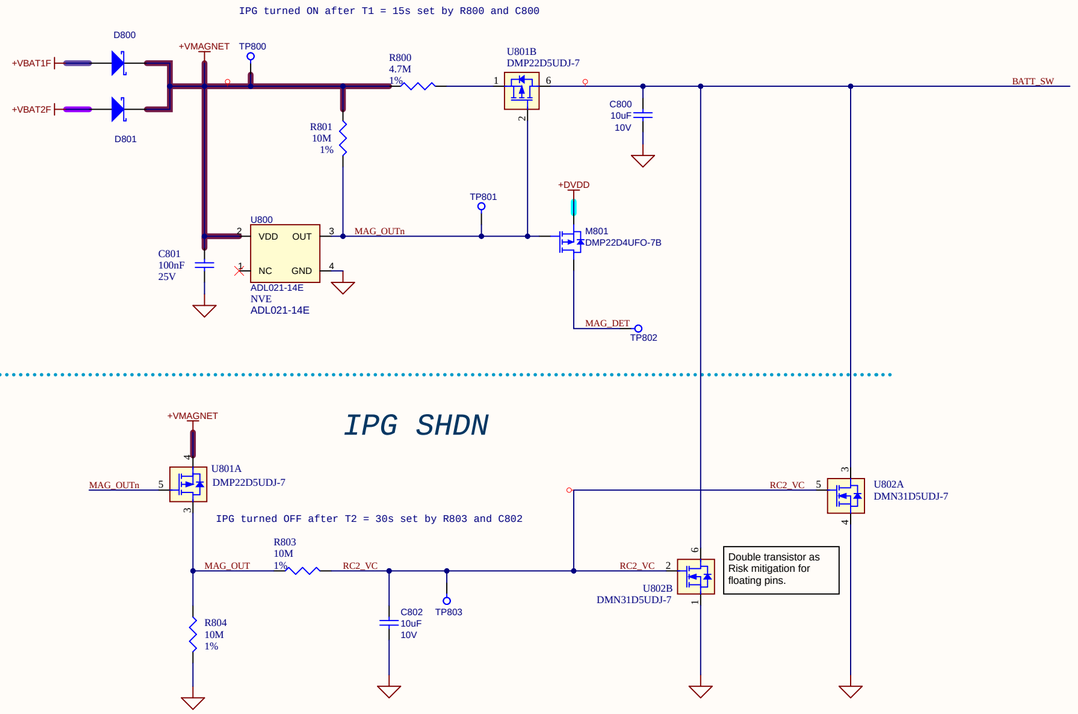


Outputs

Communication

FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Power Management**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: 3.3V LDOs for digital and analog, and stimulation HV supply.	

Magnet Sensor



Interconnect

Inputs

Outputs

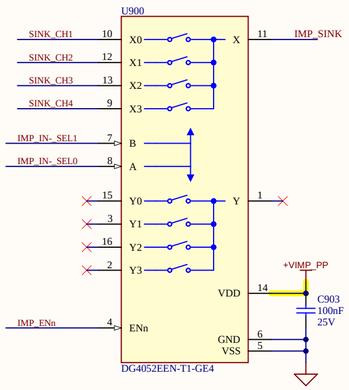
MAG_DET — MAG_DET

BATT_SW — BATT_SW

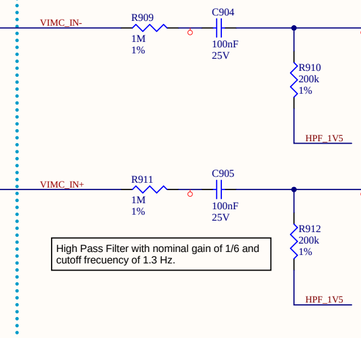
FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Magnet Sensor**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: Magnet detection IPG automatic power switch.	

Impedance Measurement

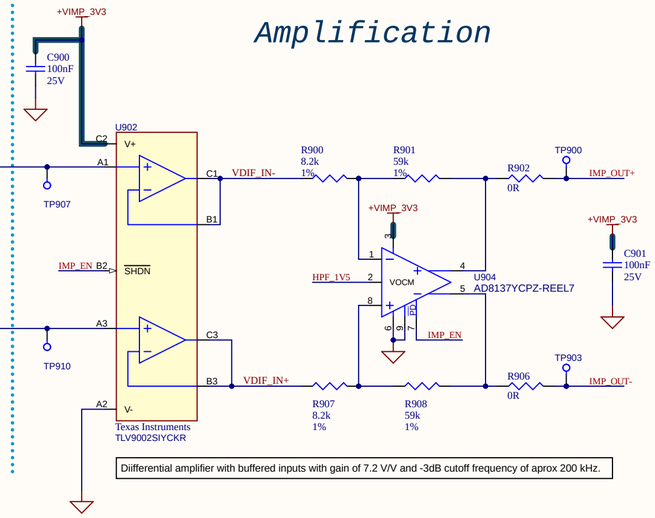
Channel selection



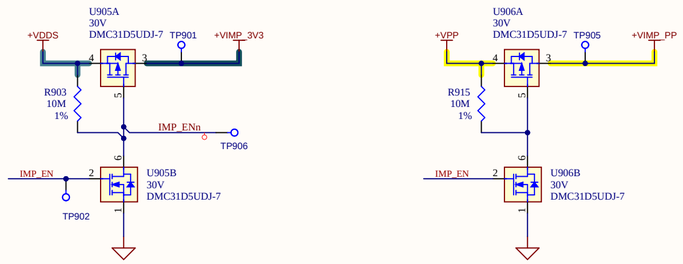
DC Filter and Input attenuation



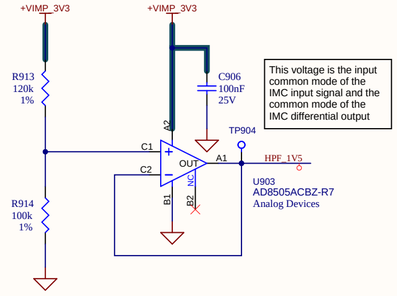
Amplification



Supply Ctrl

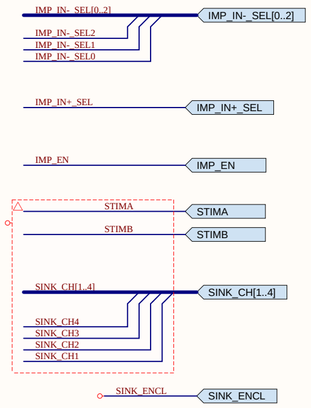


HPF IMC DC voltage

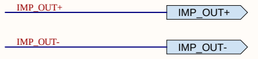


Interconnect

Inputs



Outputs

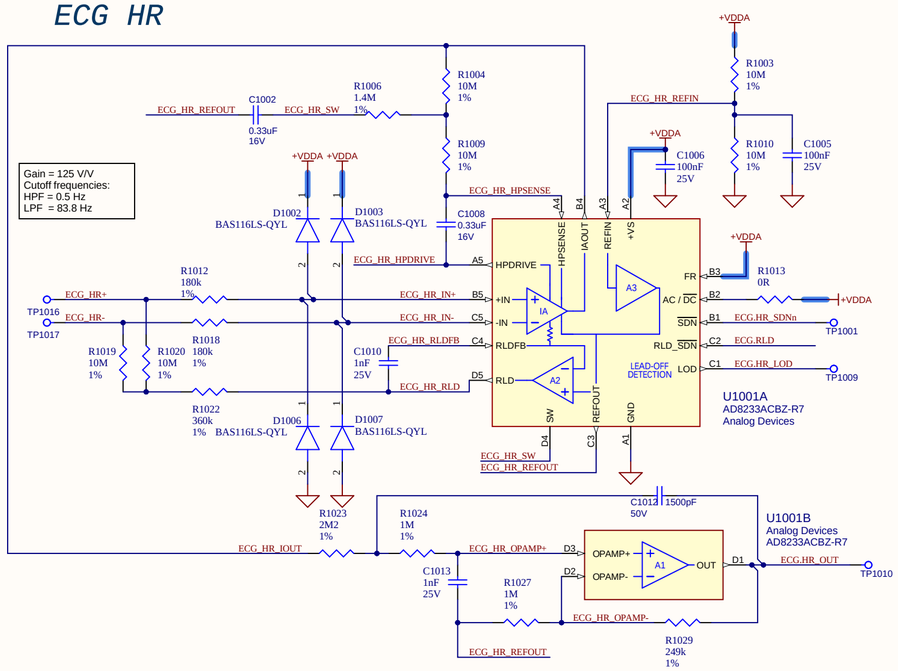


FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Impedance Measurement Circuit**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: Impedance Measurement Circuit.	

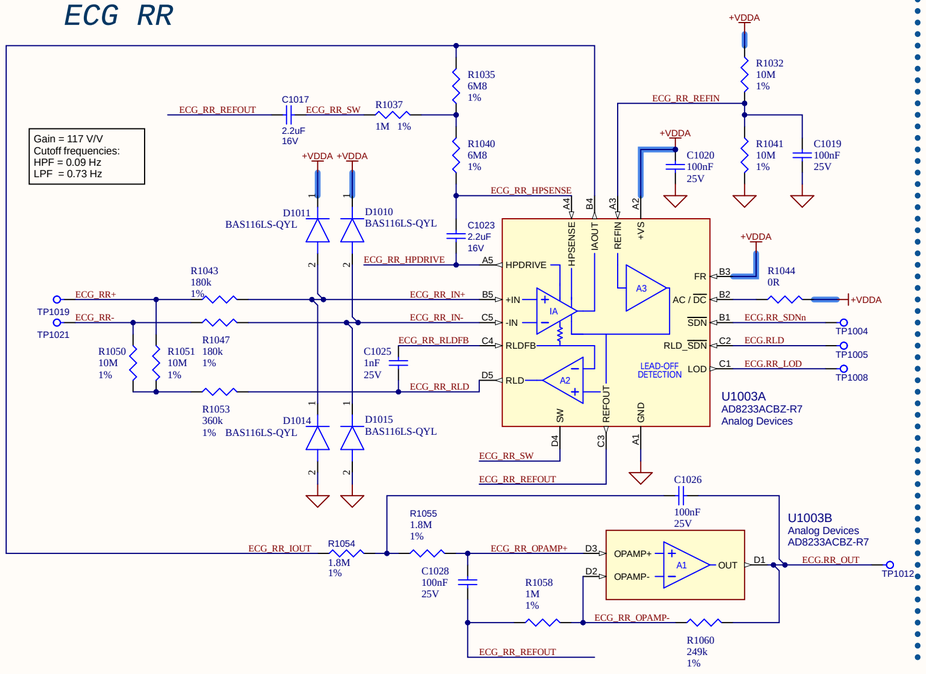
Sense Channels

Electrocardiograph

ECG HR

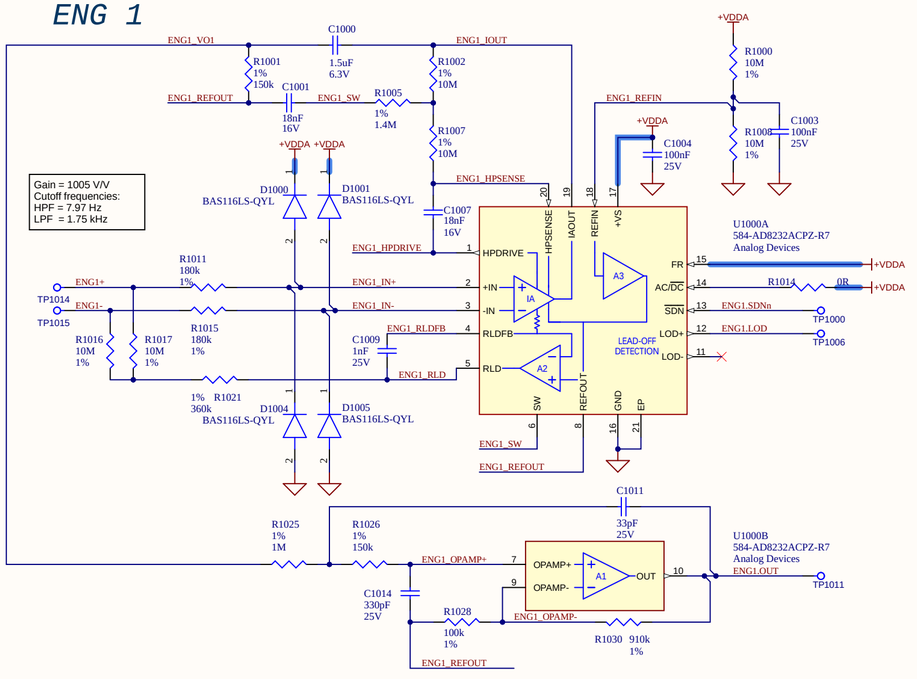


ECG RR

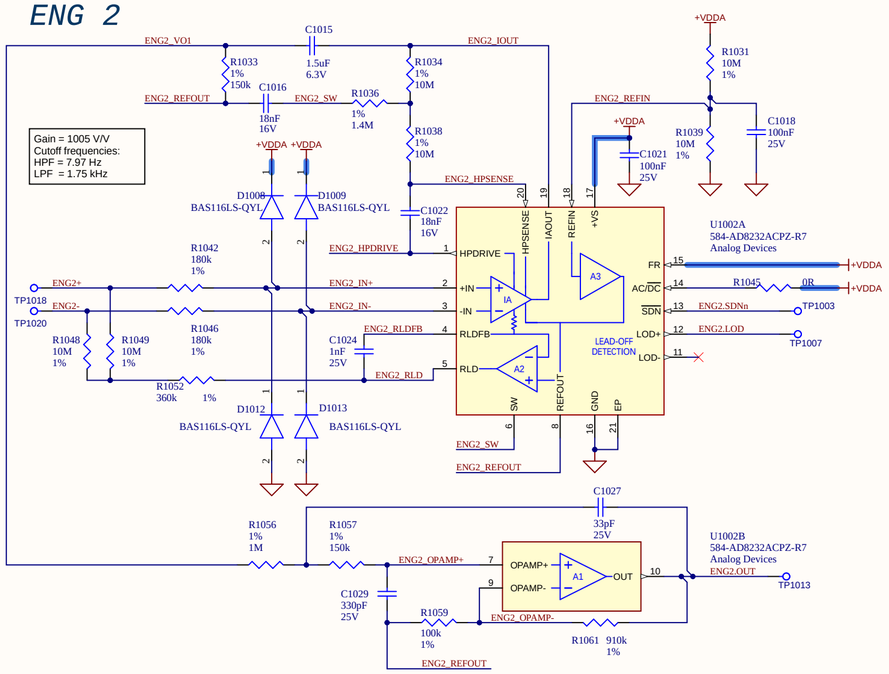


Electroneurograph

ENG 1

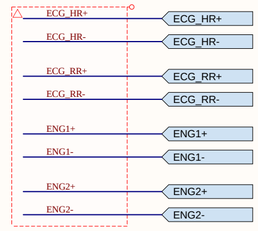


ENG 2



Interconnect

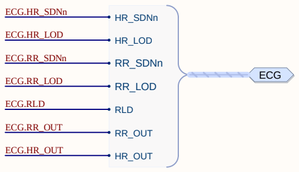
Inputs



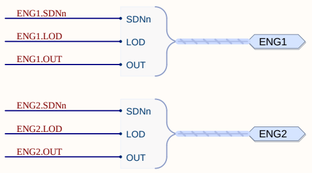
Outputs

Interfaces

ECG Monitors



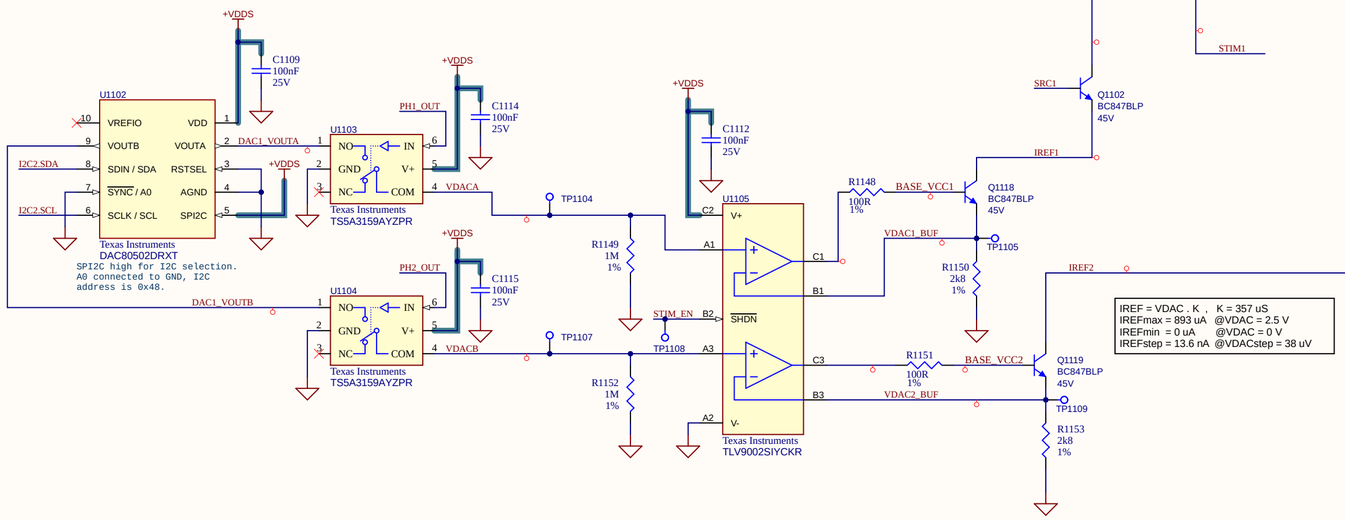
ENG Monitors



FOCUS	Project: HORNET-IPG.PrjPcb	
Schematic: **Sensing**		Ver: 2 .1
Design by: **M. Ferreira**		Date: **2025-05-09**
Reviewed by: **J. Evia**		Date: **2025-05-09**
Comments: EMG and ECGs Analog Front End.		

Stimulation

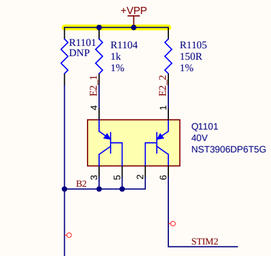
Stim Amplitude Control



Spinal Cord Stimulation

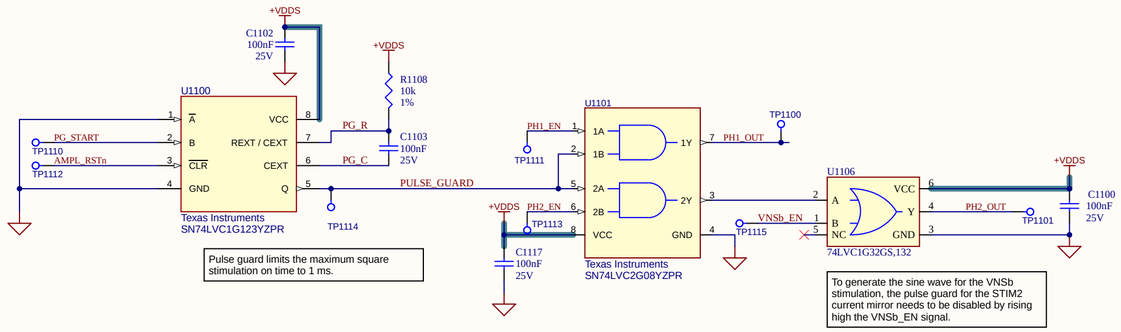
STIM1

Vagus Nerve Stimulation



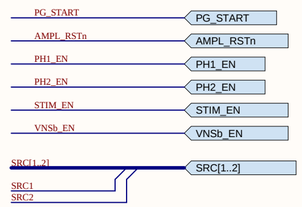
STIM2

Pulse Guard

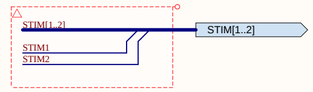


Interconnect

Inputs



Outputs

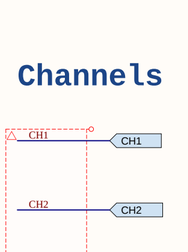


Communication

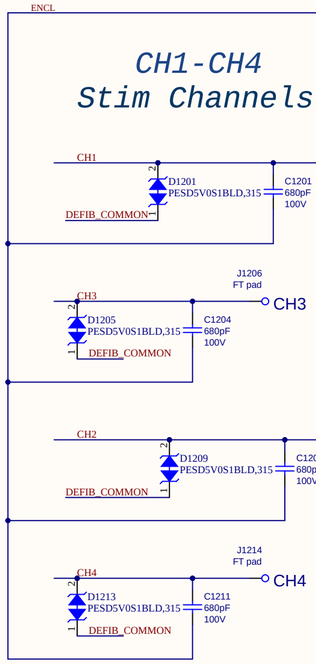
FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Stimulation**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: Vague and sacral nerve stimulation channels.	

Electrodes

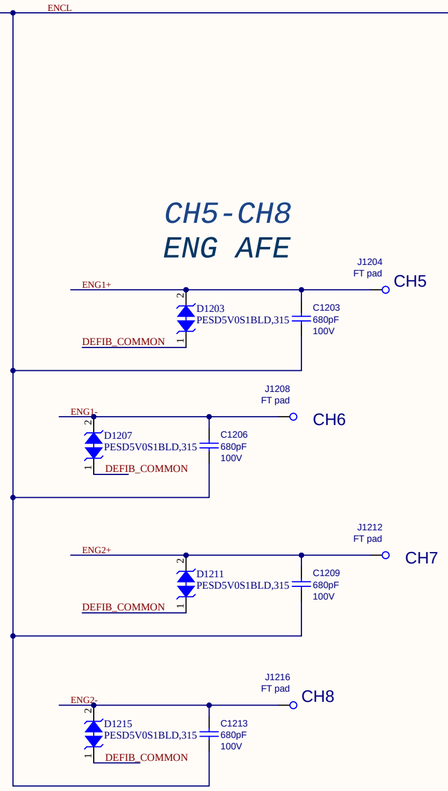
Enclosure



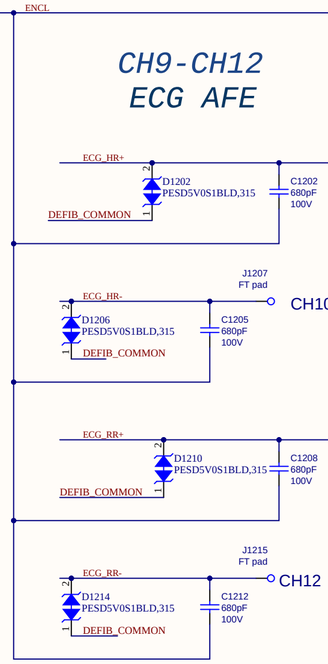
CH1-CH4 Stim Channels



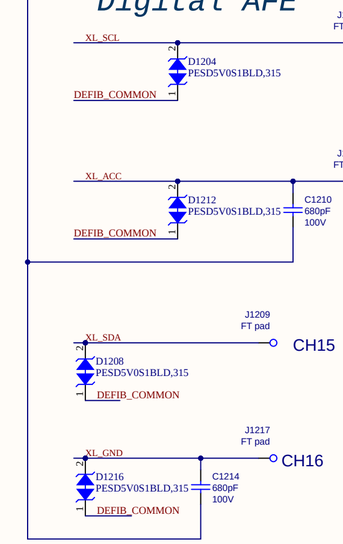
CH5-CH8 ENG AFE



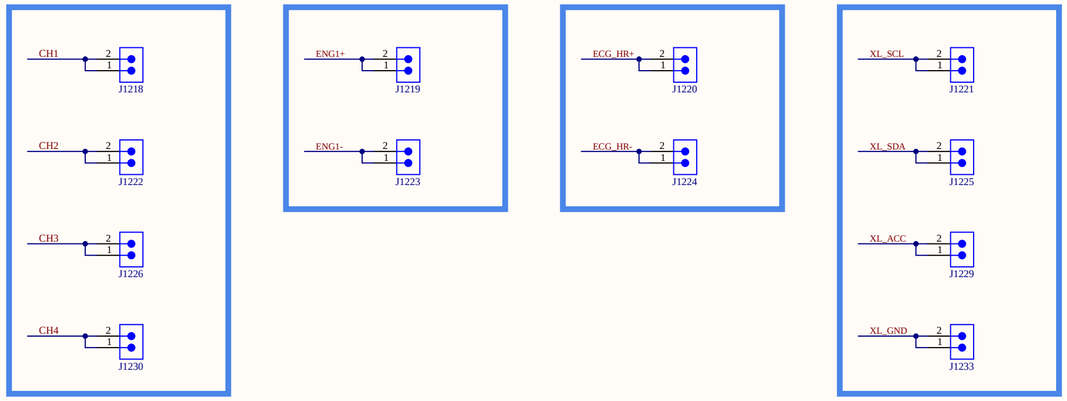
CH9-CH12 ECG AFE



CH13-CH16 Digital AFE



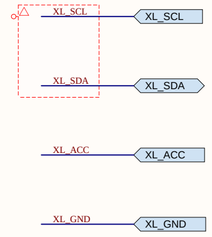
External Tip Jack Interface



Interconnect

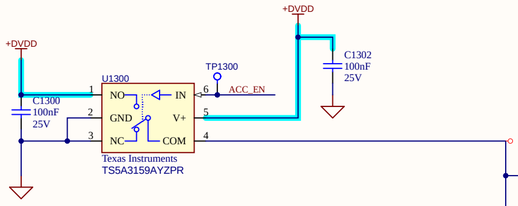
Enclosure

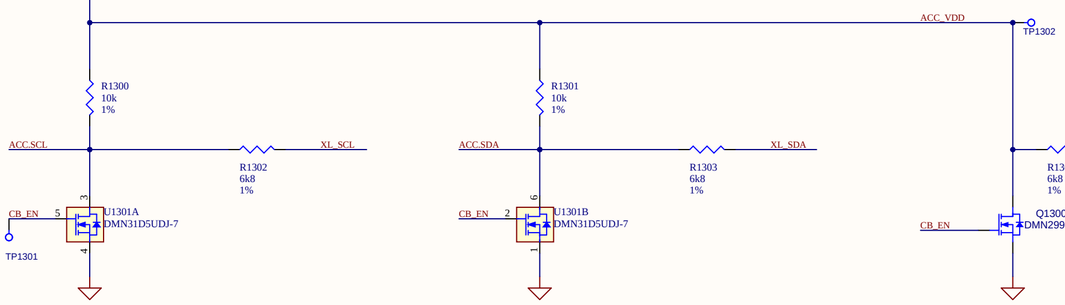
Channels

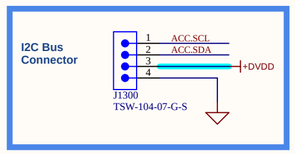


FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Electrodes**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **2025-05-09**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: Feedthrough electrode connection with defibrilation and EMI protections.	

Digital Sense Channel



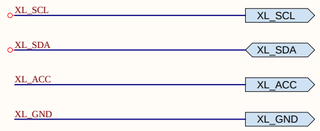




Interconnect

Inputs

Outputs

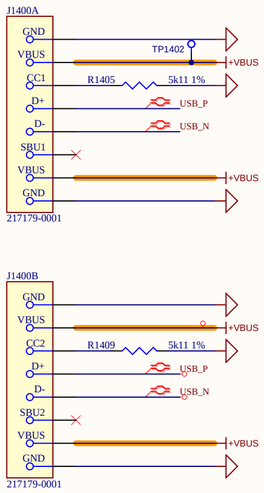


Communication

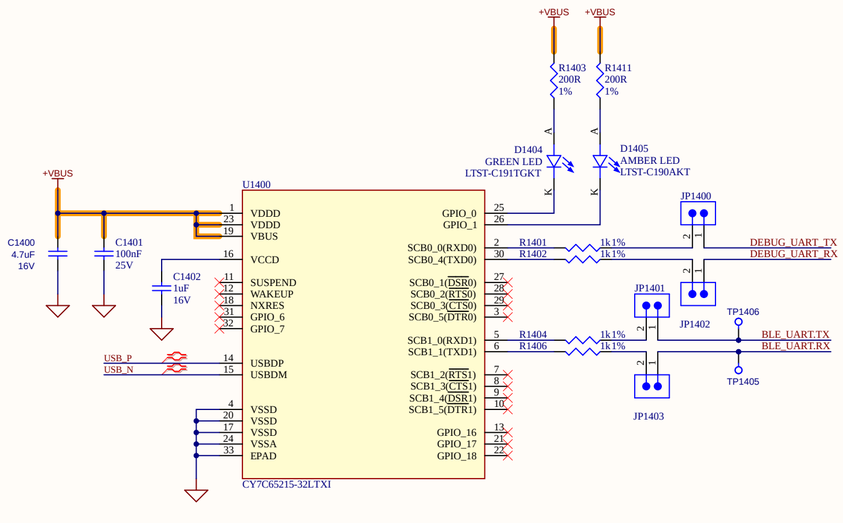
FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Digital Sense Channel**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **18/12/2023**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: External digital accelerometers I2C channel.	

Test Fixture

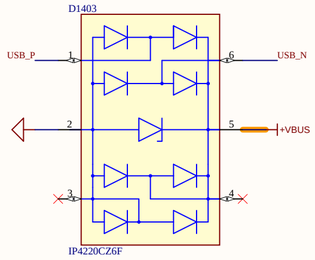
USB-C Connector



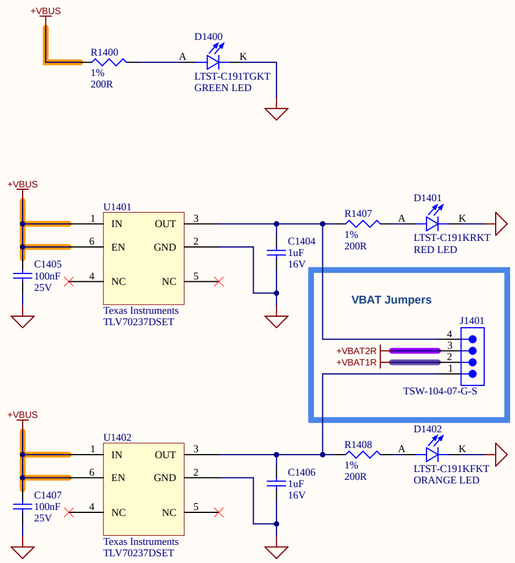
USB to Serial adaptor

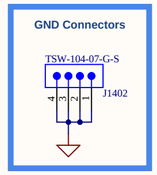


ESD Protections



3.7V LDOs





Interconnect

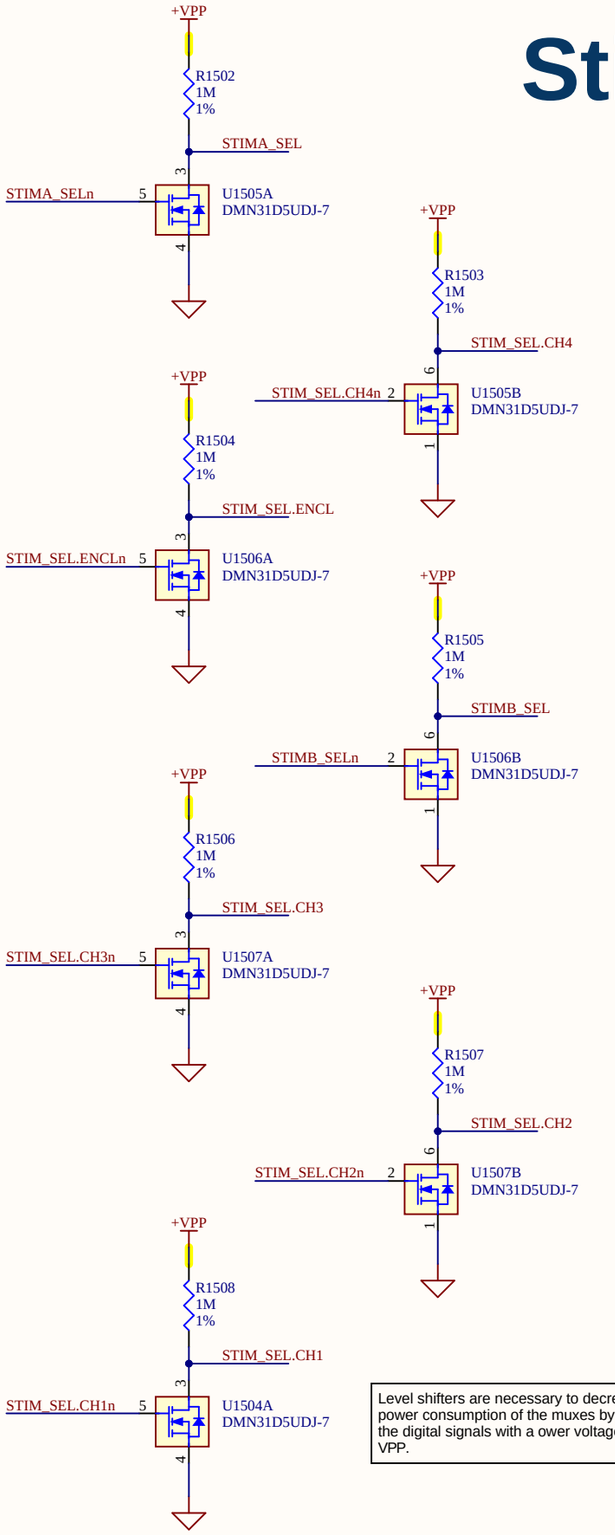
Inputs

Outputs

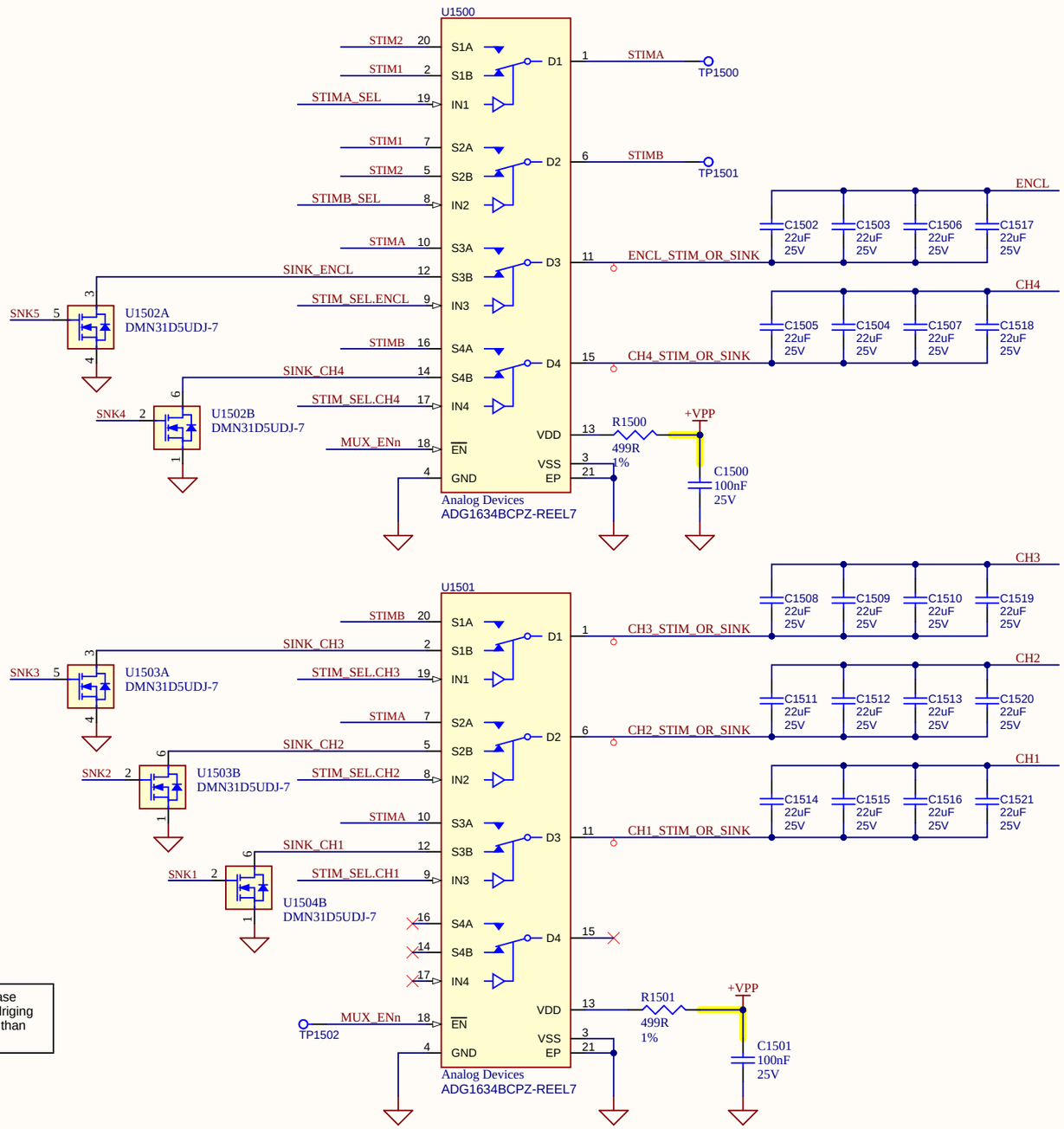
FOCUS	Project: HORNET-IPG.PrjPcb	
Schematic: **Test Fixture**		Ver: 2 .1
Design by: **M. Ferreira**		Date: **26/12/2023**
Reviewed by: **J. Evia**		Date: **2025-05-09**
Comments: External text fixture for the IPG.		

Stimulation channel selection

Output Muxes



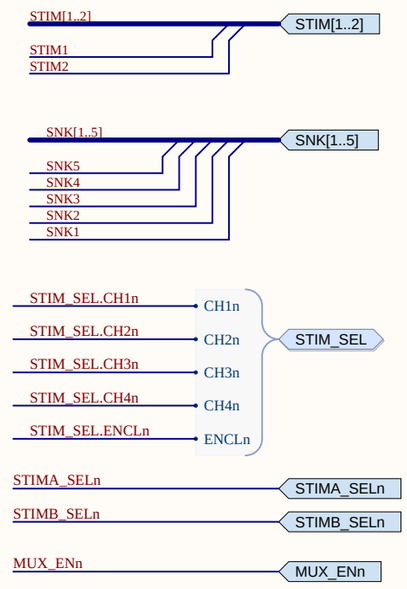
Level shifters are necessary to decrease power consumption of the muxes by driging the digital signals with a ower voltage than VPP.



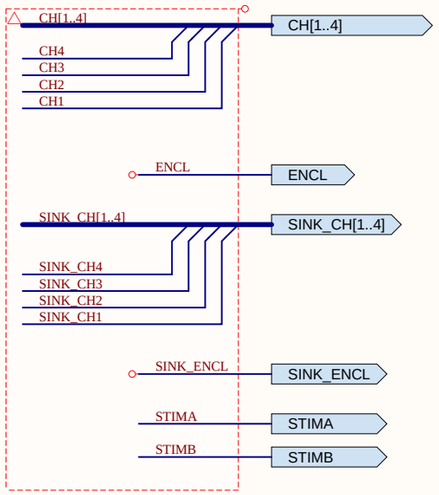
Mux Digital Lvl Shifters

Interconnect

Inputs

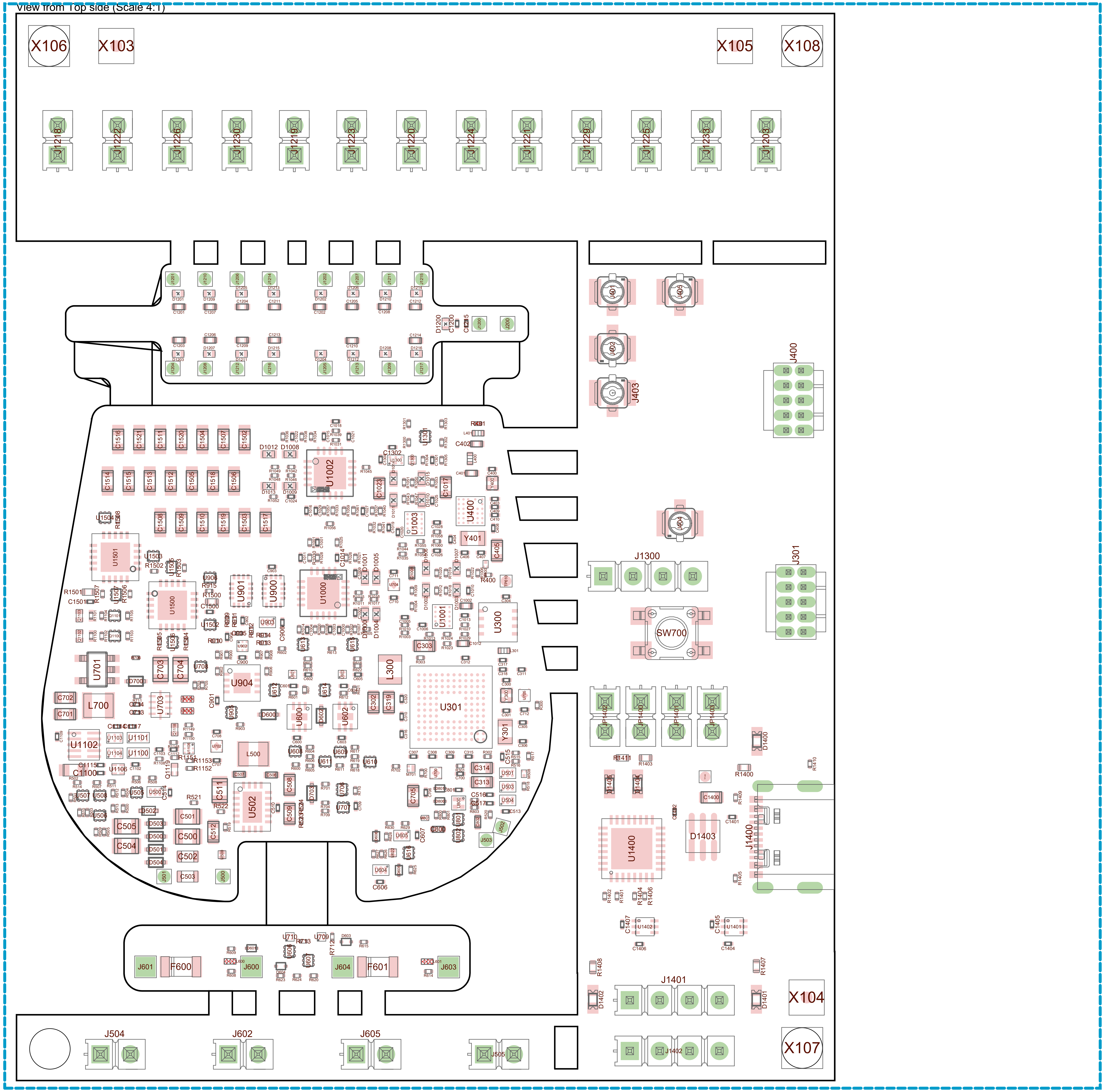


Outputs



FOCUS	Project: HORNET-IPG.PrjPcb
Schematic: **Output Multiplexing**	Ver: 2 .1
Design by: **M. Ferreira**	Date: **29/12/2023**
Reviewed by: **J. Evia**	Date: **2025-05-09**
Comments: Output/Input stage for the sensing and stim. channels	

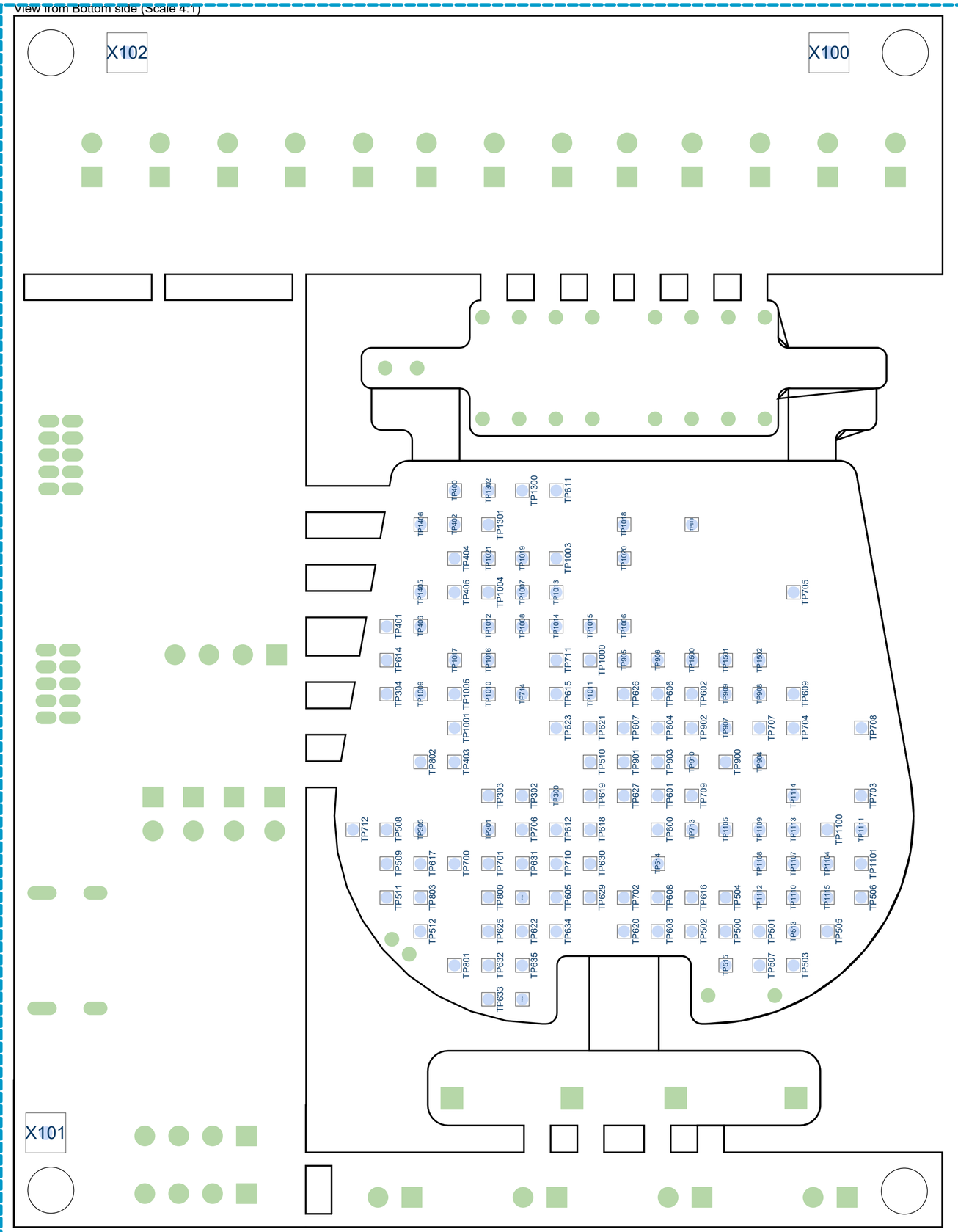
View from Top side (Scale 4:1)



Assembly Reference Top

FOCUS	Project: HORNET-IPG.PrjPcb
Title: Draftman	Ver: 2.1
Design by: M. Ferreira	Date: *
Reviewed by: J. Evia	Date: 2025-05-09
Comments:	

View from Bottom side (Scale 4:1)



Assembly Reference Bottom

FOCUS	Project: HORNET-IPG.PrjPcb	
Title: **Draftman**		Ver: 2 .1
Design by: **M. Ferreira**		Date: *
Reviewed by: **J. Evia**		Date: **2025-05-09**
Comments:		

Inspection and Acceptance Criteria

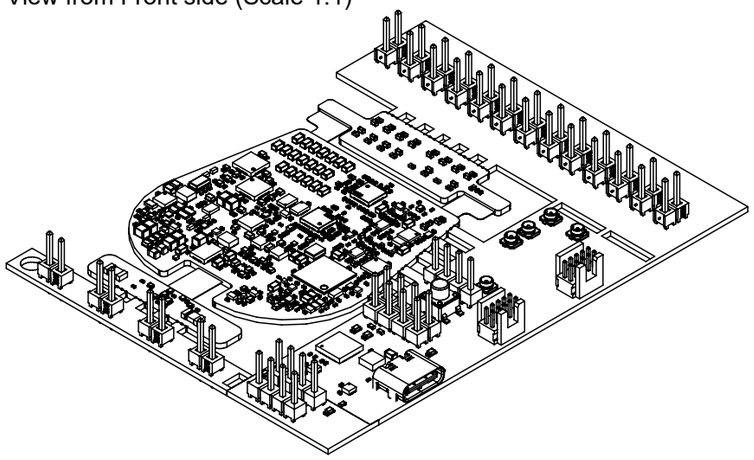
14. Acceptance criteria for PCBAs shall be per IPC-A-610 Class 2.
15. A 100% visual inspection shall be made per visual criteria in IPC-610 for class 2 assemblies.

Packaging & Shipping/Handling

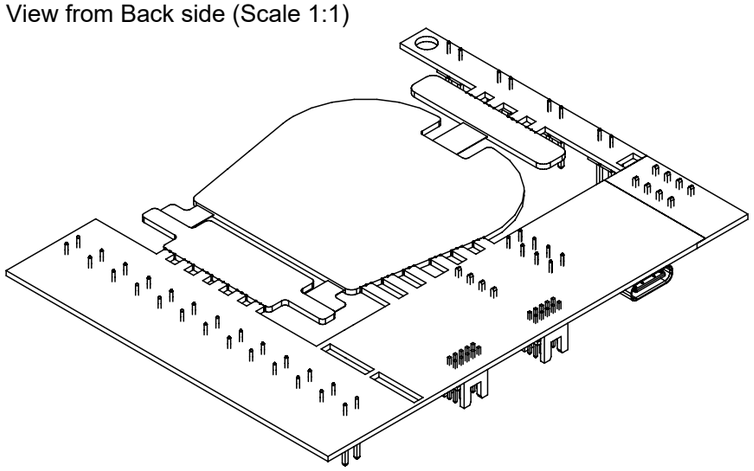
16. Shipping preparation shall be in accordance with the best industry practice to provide adequate protection against damage and contamination.
17. Shall be individually packaged in ESD-safe materials, labeled as follows. Format is DATE-QUANTITY-LOT_NUMBER-HORNET-2-IPG-2.1.B. QUANTITY is the amount of assembled PCBs in the package. For example, 2025-01-17_05_0001_HORNET-2-IPG-2.1.B.
18. The PCBs shall be packaged to provide adequate protection against damage, contaminations or degradation during handling/storage/shipping.

Isometric Views

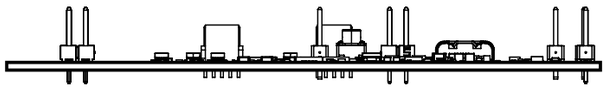
View from Front side (Scale 1:1)



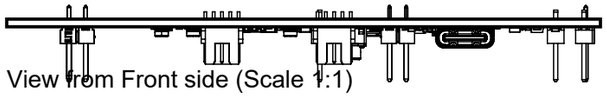
View from Back side (Scale 1:1)



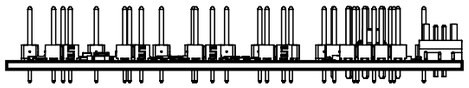
View from Left side (Scale 1:1)



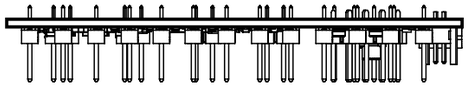
View from Right side (Scale 1:1)



View from Front side (Scale 1:1)

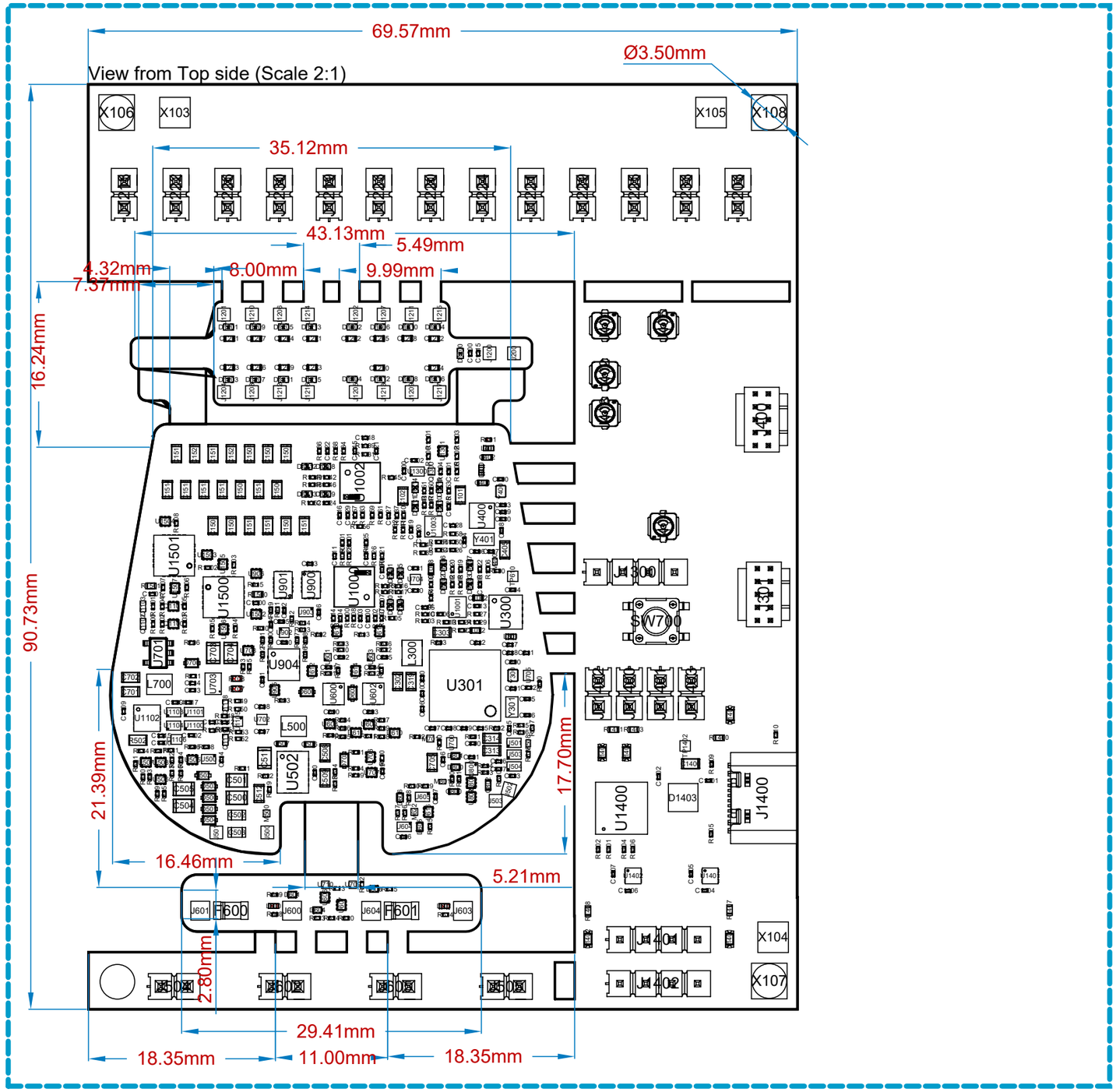


View from Back side (Scale 1:1)



FOCUS	Project: HORNET-IPG.PrjPcb
Title: **Draftman**	Ver: 2 .1
Design by: **M. Ferreira**	Date:*
Reviewed by: **J. Evia**	Date:**2025-05-09**
Comments:	

Dimensions



FOCUS	Project: HORNET-IPG.PrjPcb
Title: **Draftman**	Ver: 2.1
Design by: **M. Ferreira**	Date:*
Reviewed by: **J. Evia**	Date:**2025-05-09**
Comments:	