REV	DESCRIPTION	DATE	BY
A	FEATURE CHANGES 1. Added 4 port LS/FS/HS HUB to provide four USB Host ports. 2. Made connection for the 1.8V rail on the USB PHY to go to VAUX2. 3. Added camera connector that is compatible to the Leopard Imaging Camera modules. 4. Added power rmanagement capabilities to allow shut dowm of serial port, DVI-D, and power LED. 5. Switched to DM3730 processor and 512MB memory. 6. Added ability to turn off 26MHZ oscillator. 7. Increased overall board size to accomodate the changes. 8. Changed serial connector to a female DB9. 9. Added a 10/100 Ethernet port.	8/31/09	GC
A1	1. Disabled the DVI-D powerdown due to use of wrong GPIO pin. Pin is in the MMC group and it cannot be switched to 1.8V without impacting the SD card slot. 2. Disables HUB reset due to a timing issue with SW. When active the LAN9514 would not work correctly and the Ethernet function is broken.	5/13/10	GC
A2	1. Changed C9 to DNI and changed R34, 4.7K to installed to enable the S-Video operation.	6/15/10	GC
A3	NO MAJOR FEATURE CHANGES. 1. PCB Layout changes. 2. Added R157 in series with MMC2_CLK. 3. Added R158 to isolate shunt FET to reduce power in DC mode. 4. Added optional pullup resistors on I2C2_SCL and I2C_SDA into the layout. 5. Moved DVI_PUP signal to TPS65950. Previous location could not be used due to a conflict with the MMC function on the pins.	6/23/10	GC
B	NO MAJOR FEATURE CHANGES. 1. Changed DM3730 from an ES1.0 to a ES1.1.	10/26/2010	GC
C	REPLACED OVERVOLTAGE CIRCUIT 1. Deleted U19, U31, and U32. 2. Deleted C214 and C212. 3. Added new U31 and U32, a NCP349MNAE overvoltage protection device. ADDED DC POWER DETECTION 1. Moved Q2A to level shift nUSB_PWR. 2. Connected Q2A output to the TPS65950 GPIO as indication that the board is DC powered when LOW. CHANGED SD CONNECTOR DUE TO EOL OF CURRENT PART. 1. Replaced uSD connector with new part number. 2. Delete C188, R131, R133,R132,R134,R152,R153,R15,R144,R120,C211. CHANGED PROCESSOR TO ES1.2 CHANGED USB HUB DEFAULT MODE 1. Changed DC control of HUB to come up OFF. Requires SW to activate.	12/7/2010	GC

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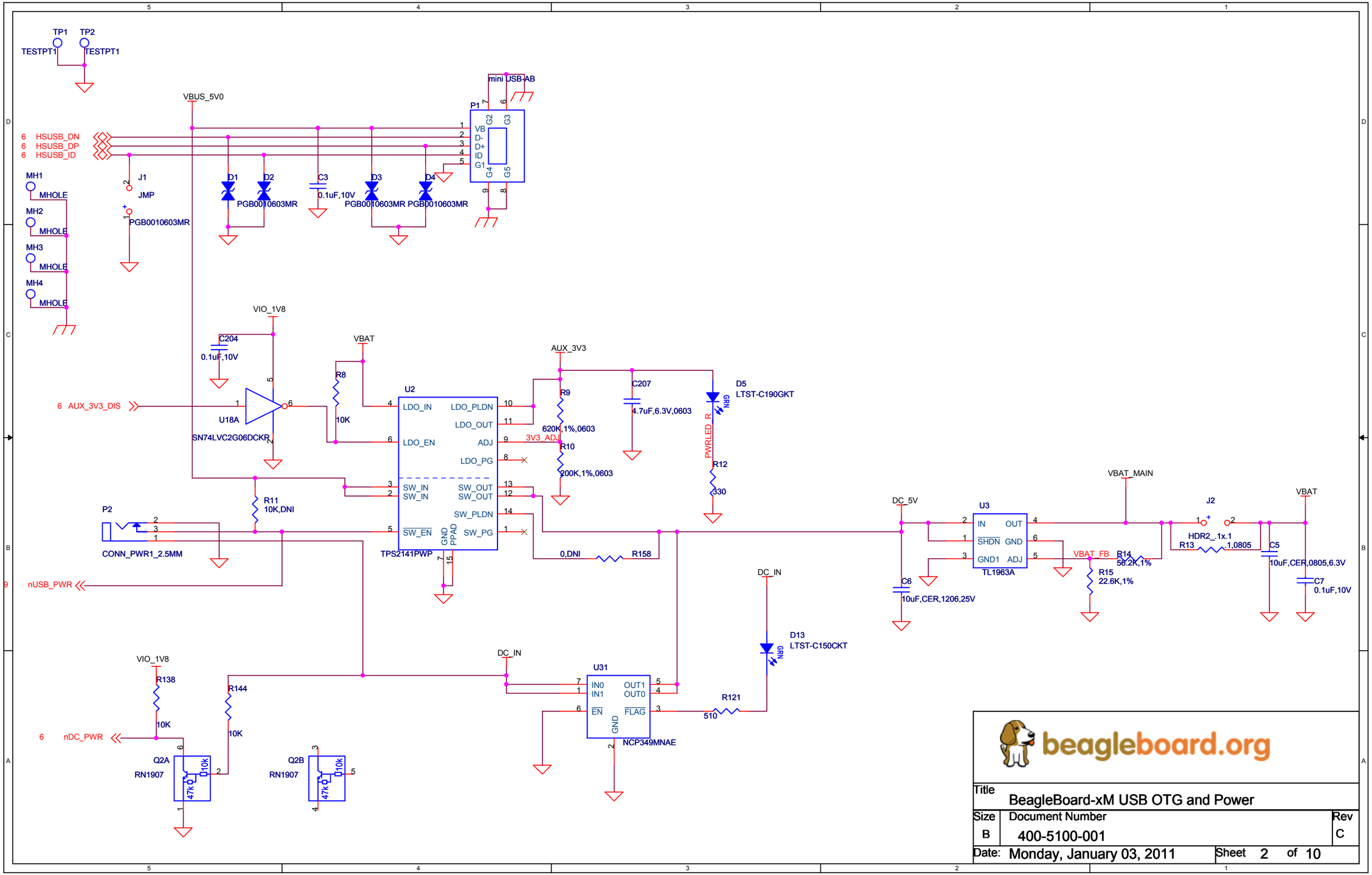

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Title	BeagleBoard-xM USB OTG and Power	
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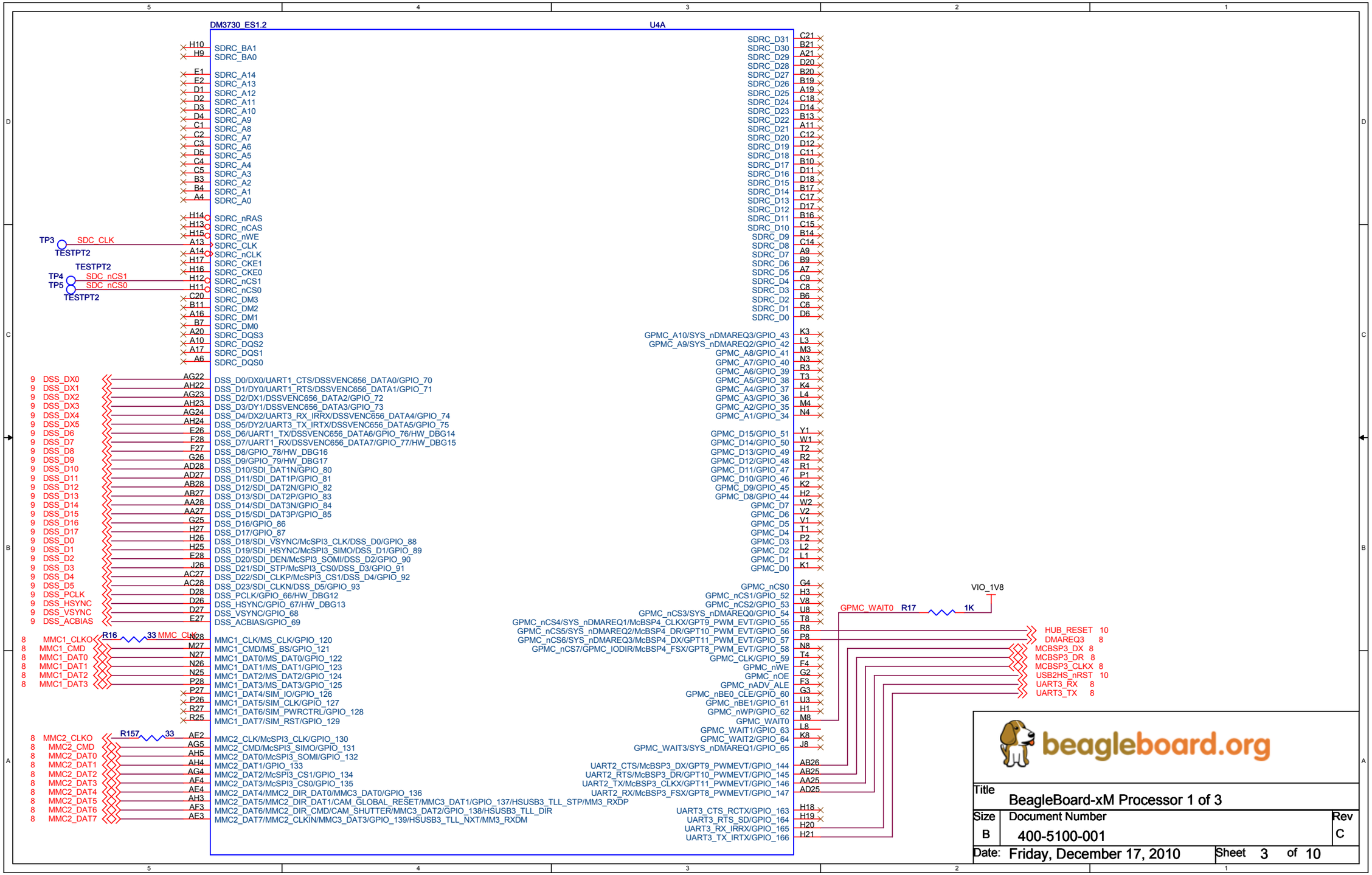
DM3730_ES1.2
U4A
SDRC_BA1
SDRC_BA0
SDRC_A14
SDRC_A13
SDRC_A12
SDRC_A11
SDRC_A10
SDRC_A9
SDRC_A8
SDRC_A7
SDRC_A6
SDRC_A5
SDRC_A4
SDRC_A3
SDRC_A2
SDRC_A1
SDRC_A0
SDRC_nRAS
SDRC_nCAS
SDRC_nWE
SDRC_CLK
SDRC_nCLK
SDRC_CKE1
SDRC_CKE0
SDRC_nCS1
SDRC_nCS0
SDRC_DM3
SDRC_DM2
SDRC_DM1
SDRC_DM0
SDRC_DQS3
SDRC_DQS2
SDRC_DQS1
SDRC_DQS0
TP3
SDC_CLK
TESTPT2
TESTPT2
TP4
SDC_nCS1
TP5
SDC_nCS0
TESTPT2
DSS_D0/DX0/UART1_CTS/DSSVENC656_DATA0/GPIO_70
DSS_D1/DY0/UART1_RTS/DSSVENC656_DATA1/GPIO_71
DSS_D2/DX1/DSSVENC656_DATA2/GPIO_72
DSS_D3/DY1/DSSVENC656_DATA3/GPIO_73
DSS_D4/DX2/UART3_RX_IRRX/DSSVENC656_DATA4/GPIO_74
DSS_D5/DY2/UART3_TX_IRTX/DSSVENC656_DATA5/GPIO_75
DSS_D6/UART1_TX/DSSVENC656_DATA6/GPIO_76/HW_DBG14
DSS_D7/UART1_RX/DSSVENC656_DATA7/GPIO_77/HW_DBG15
DSS_D8/GPIO_78/HW_DBG16
DSS_D9/GPIO_79/HW_DBG17
DSS_D10/SDI_DAT1N/GPIO_80
DSS_D11/SDI_DAT1P/GPIO_81
DSS_D12/SDI_DAT2N/GPIO_82
DSS_D13/SDI_DAT2P/GPIO_83
DSS_D14/SDI_DAT3N/GPIO_84
DSS_D15/SDI_DAT3P/GPIO_85
DSS_D16/GPIO_86
DSS_D17/GPIO_87
DSS_D18/SDI_VSYNC/McSPI3_CLK/DSS_D0/GPIO_88
DSS_D19/SDI_HSYNC/McSPI3_SIMO/DSS_D1/GPIO_89
DSS_D20/SDI_DEN/McSPI3_SOMI/DSS_D2/GPIO_90
DSS_D21/SDI_STP/McSPI3_CS0/DSS_D3/GPIO_91
DSS_D22/SDI_CLKP/McSPI3_CS1/DSS_D4/GPIO_92
DSS_D23/SDI_CLKN/DSS_D5/GPIO_93
DSS_PCLK/GPIO_66/HW_DBG12
DSS_HSYNC/GPIO_67/HW_DBG13
DSS_VSYNC/GPIO_68
DSS_ACBIAS/GPIO_69
R16
33
MMC_CLK
MMC1_CLK/MS_CLK/GPIO_120
MMC1_CMD/MS_BS/GPIO_121
MMC1_DAT0/MS_DAT0/GPIO_122
MMC1_DAT1/MS_DAT1/GPIO_123
MMC1_DAT2/MS_DAT2/GPIO_124
MMC1_DAT3/MS_DAT3/GPIO_125
MMC1_DAT4/SIM_IO/GPIO_126
MMC1_DAT5/SIM_CLK/GPIO_127
MMC1_DAT6/SIM_PWRCTRL/GPIO_128
MMC1_DAT7/SIM_RST/GPIO_129
R157
33
MMC2_CLK/McSPI3_CLK/GPIO_130
MMC2_CMD/McSPI3_SIMO/GPIO_131
MMC2_DAT0/McSPI3_SOMI/GPIO_132
MMC2_DAT1/GPIO_133
MMC2_DAT2/McSPI3_CS1/GPIO_134
MMC2_DAT3/McSPI3_CS0/GPIO_135
MMC2_DAT4/MMC2_DIR_DAT0/MMC3_DAT0/GPIO_136
MMC2_DAT5/MMC2_DIR_DAT1/CAM_GLOBAL_RESET/MMC3_DAT1/GPIO_137/HSUSB3_TLL_STP/MM3_RXDP
MMC2_DAT6/MMC2_DIR_CMD/CAM_SHUTTER/MMC3_DAT2/GPIO_138/HSUSB3_TLL_DIR
MMC2_DAT7/MMC2_CLKIN/MMC3_DAT3/GPIO_139/HSUSB3_TLL_NXT/MM3_RXDM
SDRC_D31
SDRC_D30
SDRC_D29
SDRC_D28
SDRC_D27
SDRC_D26
SDRC_D25
SDRC_D24
SDRC_D23
SDRC_D22
SDRC_D21
SDRC_D20
SDRC_D19
SDRC_D18
SDRC_D17
SDRC_D16
SDRC_D15
SDRC_D14
SDRC_D13
SDRC_D12
SDRC_D11
SDRC_D10
SDRC_D9
SDRC_D8
SDRC_D7
SDRC_D6
SDRC_D5
SDRC_D4
SDRC_D3
SDRC_D2
SDRC_D1
SDRC_D0
GPMC_A10/SYS_nDMAREQ3/GPIO_43
GPMC_A9/SYS_nDMAREQ2/GPIO_42
GPMC_A8/GPIO_41
GPMC_A7/GPIO_40
GPMC_A6/GPIO_39
GPMC_A5/GPIO_38
GPMC_A4/GPIO_37
GPMC_A3/GPIO_36
GPMC_A2/GPIO_35
GPMC_A1/GPIO_34
GPMC_D15/GPIO_51
GPMC_D14/GPIO_50
GPMC_D13/GPIO_49
GPMC_D12/GPIO_48
GPMC_D11/GPIO_47
GPMC_D10/GPIO_46
GPMC_D9/GPIO_45
GPMC_D8/GPIO_44
GPMC_D7
GPMC_D6
GPMC_D5
GPMC_D4
GPMC_D3
GPMC_D2
GPMC_D1
GPMC_D0
GPMC_nCS0
GPMC_nCS1/GPIO_52
GPMC_nCS2/GPIO_53
GPMC_nCS3/SYS_nDMAREQ0/GPIO_54
GPMC_nCS4/SYS_nDMAREQ1/McBSP4_CLKX/GPT9_PWM_EVT/GPIO_55
GPMC_nCS5/SYS_nDMAREQ2/McBSP4_DR/GPT10_PWM_EVT/GPIO_56
GPMC_nCS6/SYS_nDMAREQ3/McBSP4_DX/GPT11_PWM_EVT/GPIO_57
GPMC_nCS7/GPMC_IODIR/McBSP4_FSX/GPT8_PWM_EVT/GPIO_58
GPMC_CLK/GPIO_59
GPMC_nWE
GPMC_nOE
GPMC_nADV_ALE
GPMC_nBE0_CLE/GPIO_60
GPMC_nBE1/GPIO_61
GPMC_nWP/GPIO_62
GPMC_WAIT0
GPMC_WAIT1/GPIO_63
GPMC_WAIT2/GPIO_64
GPMC_WAIT3/SYS_nDMAREQ1/GPIO_65
UART2_CTS/McBSP3_DX/GPT9_PWMEVT/GPIO_144
UART2_RTS/McBSP3_DR/GPT10_PWMEVT/GPIO_145
UART2_TX/McBSP3_CLKX/GPT11_PWMEVT/GPIO_146
UART2_RX/McBSP3_FSX/GPT8_PWMEVT/GPIO_147
UART3_CTS_RCTX/GPIO_163
UART3_RTS_SD/GPIO_164
UART3_RX_IRRX/GPIO_165
UART3_TX_IRTX/GPIO_166
VIO_1V8
GPMC_WAIT0
R17
1K
HUB_RESET
DMAREQ3
MCBSP3_DX
MCBSP3_DR
MCBSP3_CLKX
USB2HS_nRST
UART3_RX
UART3_TX
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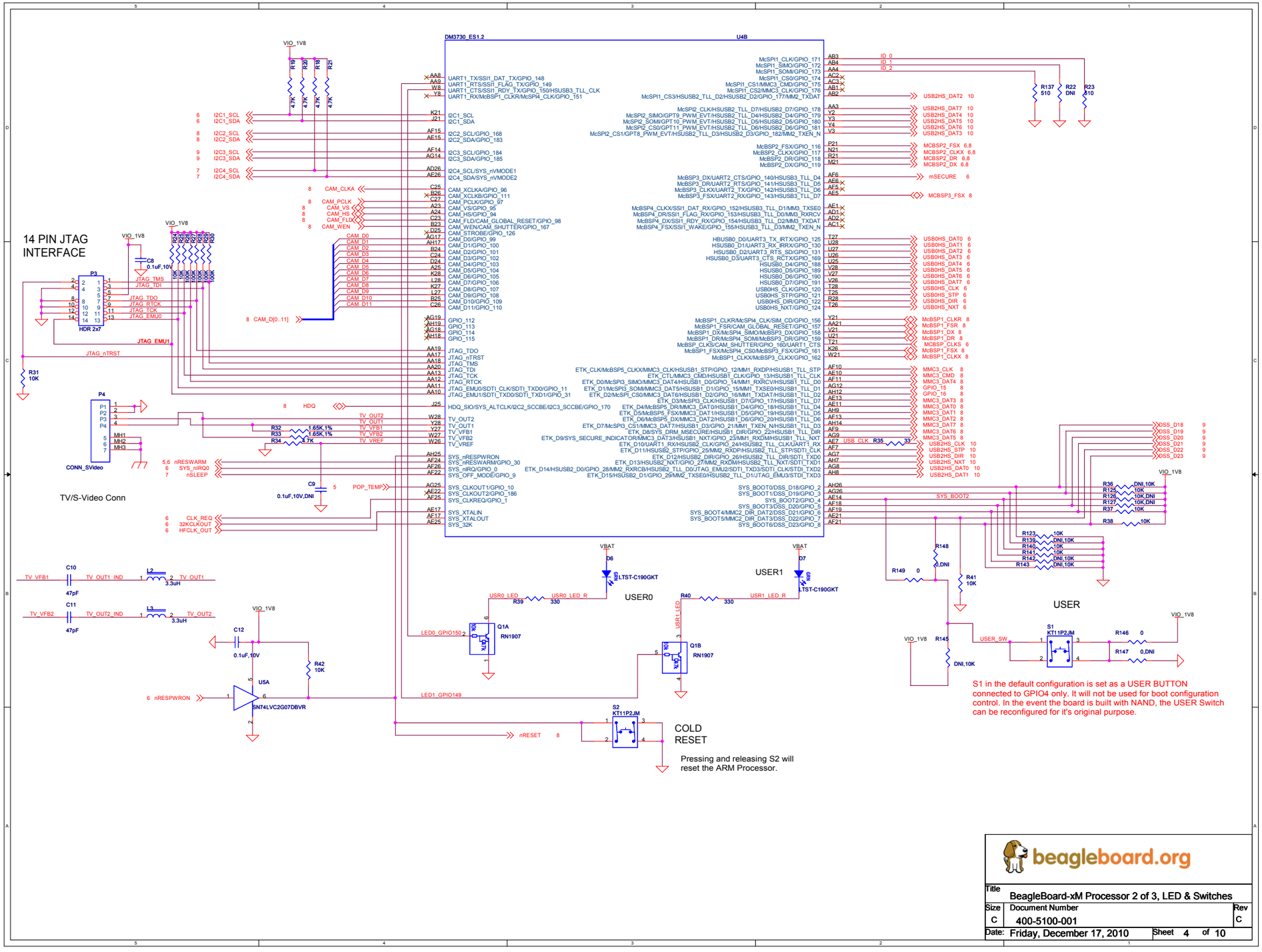
14 PIN JTAG INTERFACE
TV/S-Video Conn
USER
COLD RESET
Pressing and releasing S2 will reset the ARM Processor.
S1 in the default configuration is set as a USER BUTTON connected to GPIO4 only. It will not be used for boot configuration control. In the event the board is built with NAND, the USER Switch can be reconfigured for it's original purpose.
beagleboard.org
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BeagleBoard-xM Processor 2 of 3, LED & Switches
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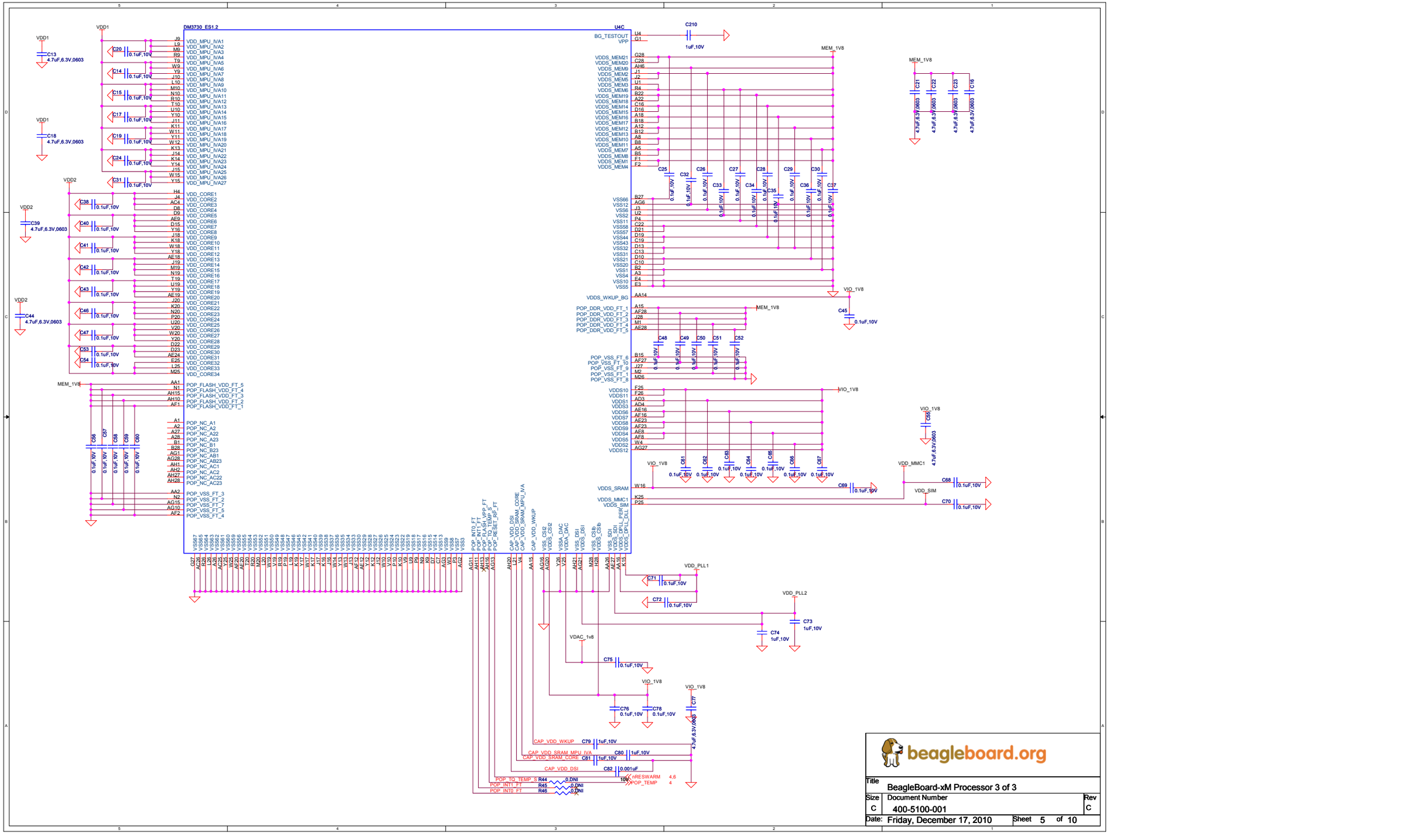
DM3730_ES1.2
U4C
VDD1
VDD2
MEM_1V8
VIO_1V8
VDD_MMC1
VDD_SIM
VDD_PLL1
VDD_PLL2
VDAC_1v8
BG_TESTOUT
VPP
VDDS_WKUP_BG
VDDS_SRAM
VDDS_MMC1
VDDS_SIM
POP_TO_TEMP_S
POP_INT1_FT
POP_INT0_FT
nRESWARM
POP_TEMP
CAP_VDD_WKUP
CAP_VDD_SRAM_MPU_IVA
CAP_VDD_SRAM_CORE
CAP_VDD_DSI
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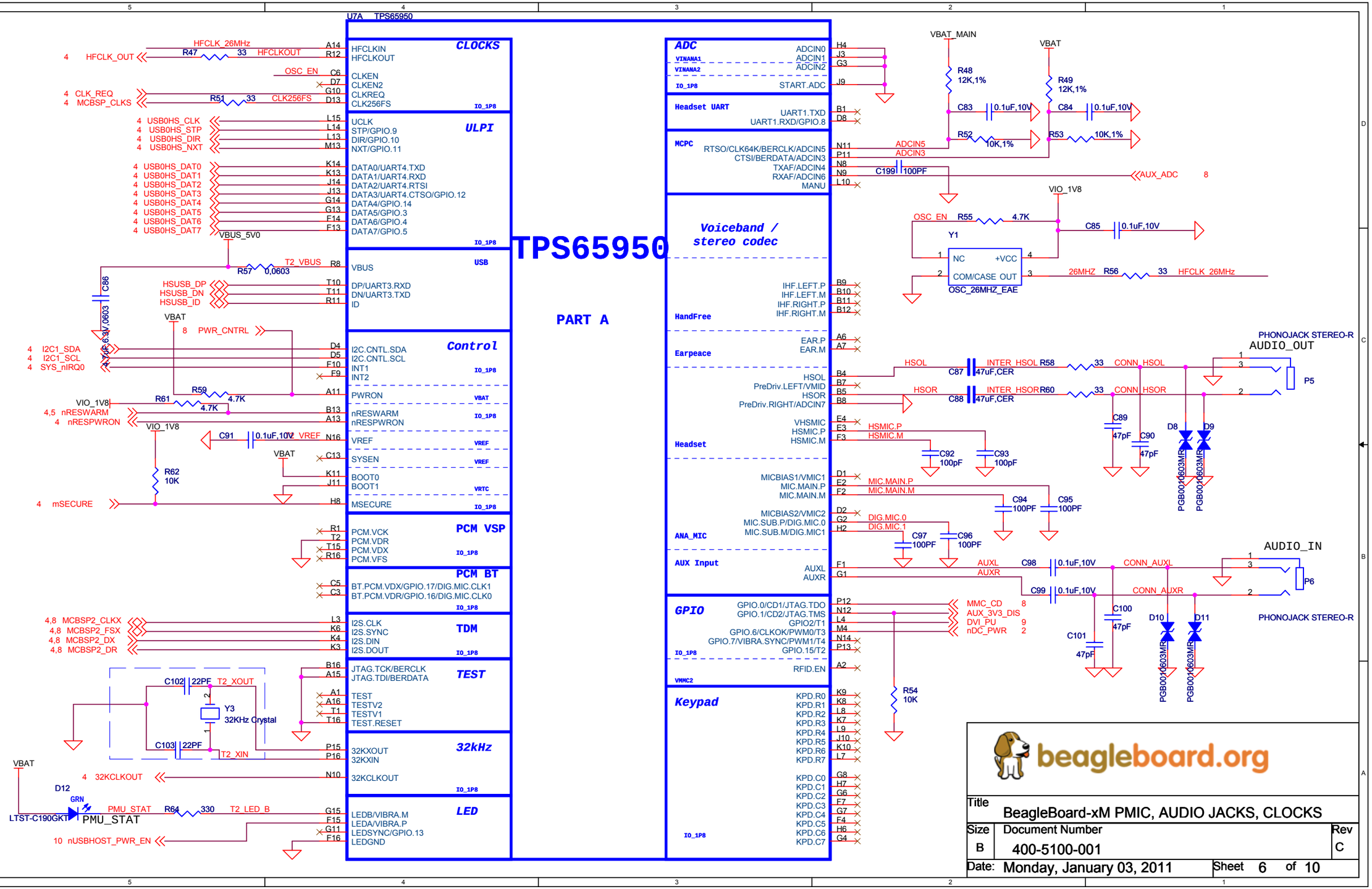
U7A TPS65950
TPS65950
PART A
CLOCKS
HFCLKIN
HFCLKOUT
CLKEN
CLKEN2
CLKREQ
CLK256FS
ULPI
UCLK
STP/GPIO.9
DIR/GPIO.10
NXT/GPIO.11
DATA0/UART4.TXD
DATA1/UART4.RXD
DATA2/UART4.RTSI
DATA3/UART4.CTSO/GPIO.12
DATA4/GPIO.14
DATA5/GPIO.3
DATA6/GPIO.4
DATA7/GPIO.5
USB
VBUS
DP/UART3.RXD
DN/UART3.TXD
ID
Control
I2C.CNTL.SDA
I2C.CNTL.SCL
INT1
INT2
PWRON
nRESWARM
nRESPWRON
VREF
SYSEN
BOOT0
BOOT1
MSECURE
PCM VSP
PCM.VCK
PCM.VDR
PCM.VDX
PCM.VFS
PCM BT
BT.PCM.VDX/GPIO.17/DIG.MIC.CLK1
BT.PCM.VDR/GPIO.16/DIG.MIC.CLK0
TDM
I2S.CLK
I2S.SYNC
I2S.DIN
I2S.DOUT
TEST
JTAG.TCK/BERCLK
JTAG.TDI/BERDATA
TEST
TESTV2
TESTV1
TEST.RESET
32kHz
32KXOUT
32KXIN
32KCLKOUT
LED
LEDB/VIBRA.M
LEDA/VIBRA.P
LEDSYNC/GPIO.13
LEDGND
ADC
ADCIN0
ADCIN1
ADCIN2
START.ADC
Headset UART
UART1.TXD
UART1.RXD/GPIO.8
MCPC
RTSO/CLK64K/BERCLK/ADCIN5
CTSI/BERDATA/ADCIN3
TXAF/ADCIN4
RXAF/ADCIN6
MANU
Voiceband / stereo codec
HandFree
IHF.LEFT.P
IHF.LEFT.M
IHF.RIGHT.P
IHF.RIGHT.M
Earpeace
EAR.P
EAR.M
Headset
HSOL
PreDriv.LEFT/VMID
HSOR
PreDriv.RIGHT/ADCIN7
VHSMIC
HSMIC.P
HSMIC.M
ANA_MIC
MICBIAS1/VMIC1
MIC.MAIN.P
MIC.MAIN.M
MICBIAS2/VMIC2
MIC.SUB.P/DIG.MIC.0
MIC.SUB.M/DIG.MIC.1
AUX Input
AUXL
AUXR
GPIO
GPIO.0/CD1/JTAG.TDO
GPIO.1/CD2/JTAG.TMS
GPIO2/T1
GPIO.6/CLKOK/PWM0/T3
GPIO.7/VIBRA.SYNC/PWM1/T4
GPIO.15/T2
RFID.EN
Keypad
KPD.R0
KPD.R1
KPD.R2
KPD.R3
KPD.R4
KPD.R5
KPD.R6
KPD.R7
KPD.C0
KPD.C1
KPD.C2
KPD.C3
KPD.C4
KPD.C5
KPD.C6
KPD.C7
HFCLK_26MHz
HFCLK_OUT
HFCLKOUT
OSC_EN
CLK_REQ
MCBSP_CLKS
CLK256FS
USB0HS_CLK
USB0HS_STP
USB0HS_DIR
USB0HS_NXT
USB0HS_DAT0
USB0HS_DAT1
USB0HS_DAT2
USB0HS_DAT3
USB0HS_DAT4
USB0HS_DAT5
USB0HS_DAT6
USB0HS_DAT7
VBUS_5V0
T2_VBUS
HSUSB_DP
HSUSB_DN
HSUSB_ID
VBAT
PWR_CNTRL
I2C1_SDA
I2C1_SCL
SYS_nIRQ0
VIO_1V8
nRESWARM
nRESPWRON
VREF
mSECURE
MCBSP2_CLKX
MCBSP2_FSX
MCBSP2_DX
MCBSP2_DR
Y3
32KHz Crystal
T2_XOUT
T2_XIN
32KCLKOUT
D12
LTST-C190GKT
PMU_STAT
T2_LED_B
nUSBHOST_PWR_EN
VBAT_MAIN
VBAT
AUX_ADC
VIO_1V8
OSC_26MHZ_EAE
26MHZ
HFCLK_26MHz
PHONOJACK STEREO-R
AUDIO_OUT
P5
HSOL
HSOR
CONN_HSOL
CONN_HSOR
HSMIC.P
HSMIC.M
MIC.MAIN.P
MIC.MAIN.M
DIG.MIC.0
DIG.MIC.1
AUDIO_IN
P6
AUXL
AUXR
CONN_AUXL
CONN_AUXR
MMC_CD
AUX_3V3_DIS
DVI_PU
nDC_PWR
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BeagleBoard-xM PMIC, AUDIO JACKS, CLOCKS
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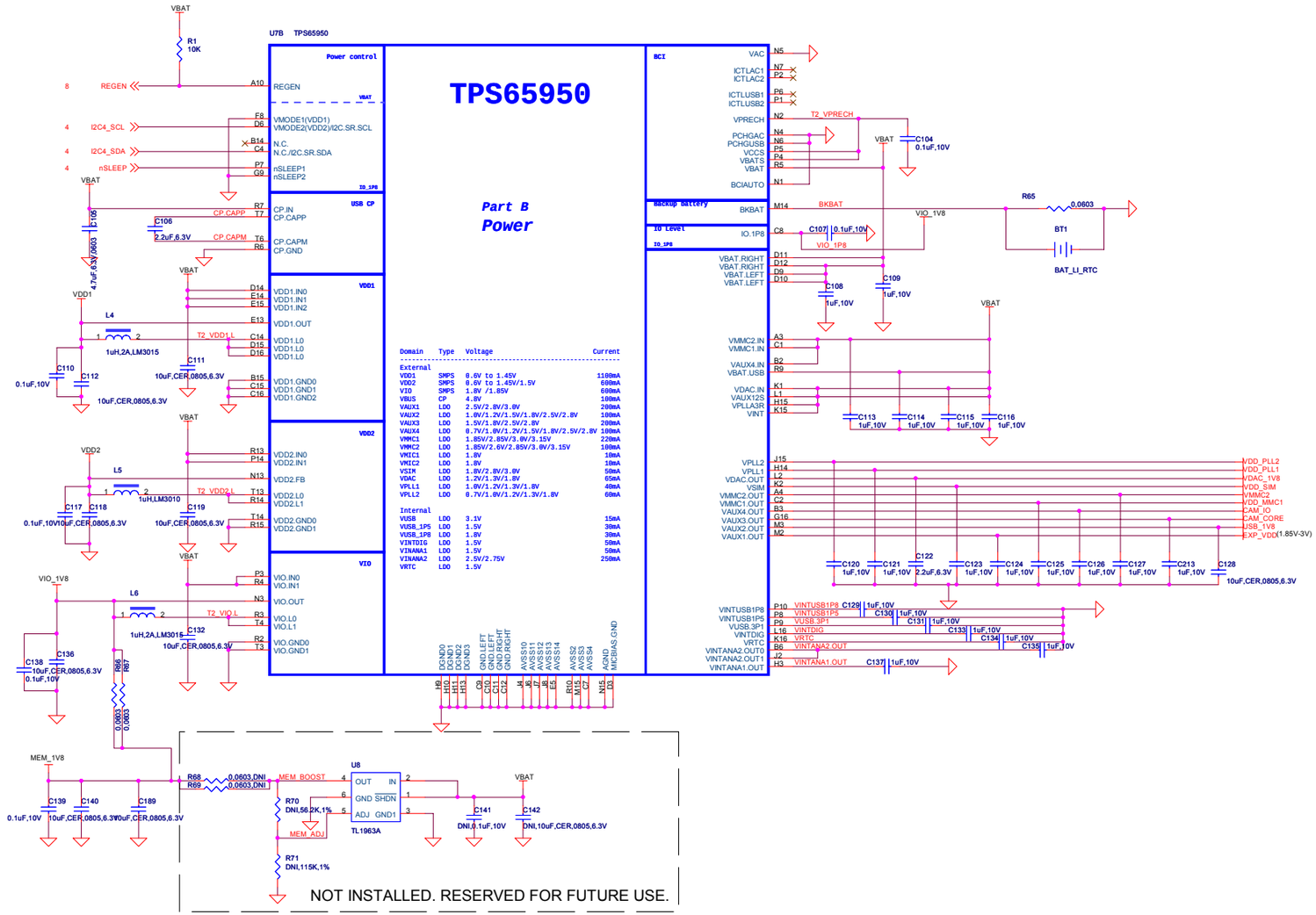
TPS65950
Part B
Power
U7B TPS65950
Power control
USB CP
VDD1
VDD2
VIO
BCI
Backup Battery
IO Level
Domain Type Voltage Current
External
VDD1 SMPS 0.6V to 1.45V 1100mA
VDD2 SMPS 0.6V to 1.45V/1.5V 600mA
VIO SMPS 1.8V /1.85V 600mA
VBUS CP 4.8V 100mA
VAUX1 LDO 2.5V/2.8V/3.0V 200mA
VAUX2 LDO 1.0V/1.2V/1.5V/1.8V/2.5V/2.8V 100mA
VAUX3 LDO 1.5V/1.8V/2.5V/2.8V 200mA
VAUX4 LDO 0.7V/1.0V/1.2V/1.5V/1.8V/2.5V/2.8V 100mA
VMMC1 LDO 1.85V/2.85V/3.0V/3.15V 220mA
VMMC2 LDO 1.85V/2.6V/2.85V/3.0V/3.15V 100mA
VMIC1 LDO 1.8V 10mA
VMIC2 LDO 1.8V 10mA
VSIM LDO 1.8V/2.8V/3.0V 50mA
VDAC LDO 1.2V/1.8V/1.8V 65mA
VPLL1 LDO 1.0V/1.2V/1.3V/1.8V 40mA
VPLL2 LDO 0.7V/1.0V/1.2V/1.3V/1.8V 60mA
Internal
VUSB LDO 3.1V 15mA
VUSB_1P5 LDO 1.5V 30mA
VUSB_1P8 LDO 1.8V 30mA
VINTDIG LDO 1.5V 50mA
VINANA1 LDO 1.5V 50mA
VINANA2 LDO 2.5V/2.75V 250mA
VRTC LDO 1.5V
NOT INSTALLED. RESERVED FOR FUTURE USE.
TL1963A
BAT_LI_RTC
beagleboard.org
BeagleBoard-xM PMIC POWER RAILS
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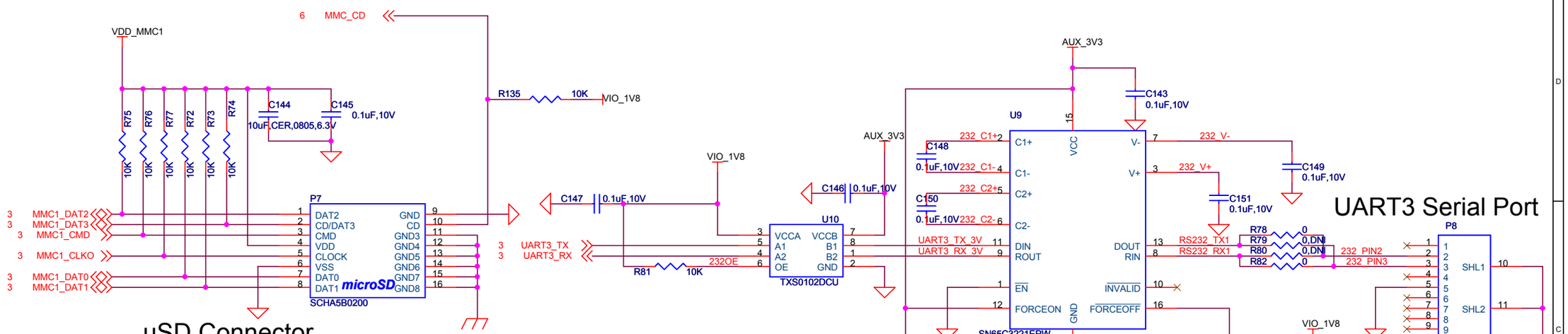

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Title	BeagleBoard-xM uSD, CAMERA, EXPANSION, & UART	
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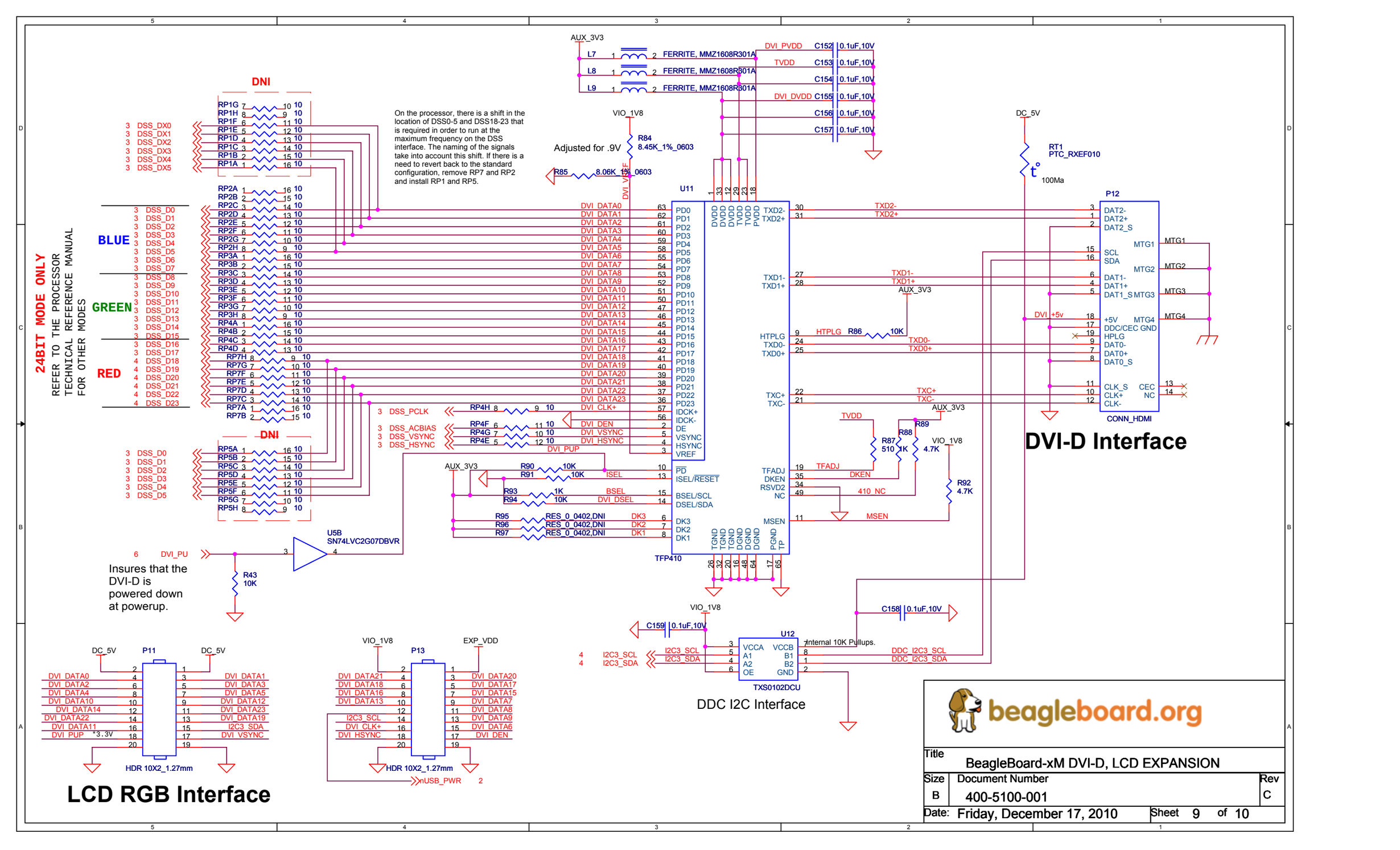
24BIT MODE ONLY
REFER TO THE PROCESSOR TECHNICAL REFERENCE MANUAL FOR OTHER MODES
BLUE
GREEN
RED
DNI
On the processor, there is a shift in the location of DSS0-5 and DSS18-23 that is required in order to run at the maximum frequency on the DSS interface. The naming of the signals take into account this shift. If there is a need to revert back to the standard configuration, remove RP7 and RP2 and install RP1 and RP5.
Adjusted for .9V
R84 8.45K_1%_0603
R85 8.06K_1%_0603
DVI_VREF
U11
TFP410
U5B SN74LVC2G07DBVR
Insures that the DVI-D is powered down at powerup.
R43 10K
DVI_PUP
ISEL
BSEL
DVI_DSEL
DK3
DK2
DK1
RES_0_0402,DNI
AUX_3V3
VIO_1V8
DC_5V
FERRITE, MMZ1608R301A
DVI_PVDD
TVDD
DVI_DVDD
RT1 PTC_RXEF010
100Ma
P12
CONN_HDMI
DVI +5v
HTPLG
TFADJ
DKEN
MSEN
410_NC
TXD0+
TXD0-
TXD1+
TXD1-
TXC+
TXC-
DVI Interface
U12
TXS0102DCU
Internal 10K Pullups.
DDC I2C Interface
P11
P13
HDR 10X2_1.27mm
LCD RGB Interface
nUSB_PWR
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Title
BeagleBoard-xM DVI-D, LCD EXPANSION
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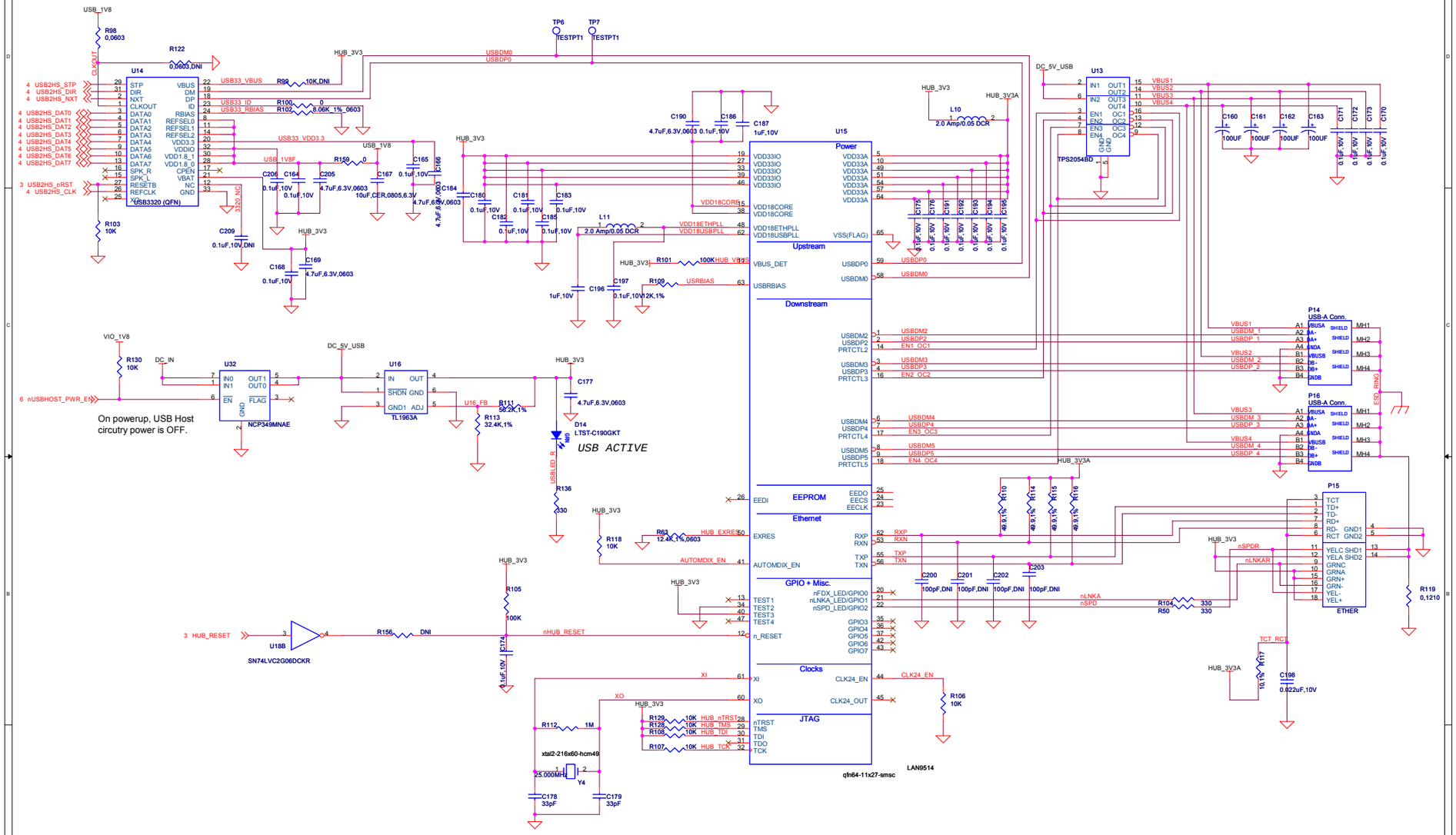

Title	BeagleBoard-xM USB HOST, HUB, ETHERNET	
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