Performance evaluation of measured time stretching approach for event timer

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***Abstract*—Time and time interval measurements are in high demand in many scientific and engineering fields. This work investigates the feasibility of using the time stretching technique in combination with available off-the-shelf time to digital converters (TDC) as a means of improving its functionality. The paper compares different time measurement techniques and concludes with the initial test results of the time stretching test board.**

***Index Terms*—event timer, TDC, ToF, TAC, TVC, time interval, time measurements**

I. Introduction

Time measurements (time-code transformations) have always belonged to the class of the most demanded measurements since it is advisable to measure many different physical quantities together with the time of its appearance. Among the time measurements, measurements of time intervals (TI) are most in-demand. For a significant part of the experiments, the research object is the temporal relationships between the initialising and second events. Often called Time of Flight (ToF), the TI measurements are crucial in magnetic resonance angiography (MRA), Satellite Laser Ranging, mass spectrometry, 3D imaging, and many others.

There are several methods of time to digital converters (TDC) classification in different literature. The classification, which categorises all TDC by measurement technique, e.i, direct or indirect, is used in this work [1].

A. Direct technique

By far, the simplest direct method of time measurement is counter. The counter counts reference clock edges between two events. The advantage is in the simplicity of implementation. However, the main limitation is resolution and quantisation errors, but their impact can be reduced by using multisampling and averaging techniques or by increasing the reference clock frequency. Due to this and other disadvantages, this method in modern TDC is used primarily as a coarse time counter.

Another direct method is when delay lines are used in TDC. In recent years, this technique has gained more and more popularity because it can be easily implemented in Field Programmable Gate Arrays (FPGA) [2] [3]. The major drawback in the delay line TDC is its resolution because it directly depends on the delay of the buffer. To improve delay line TDC resolution, Vernier delay line TDC is used in [4].

Adding feedback to the delay line forms a ring oscillator. The study [5] uses two such controllable oscillators with different oscillating periods to create Verner ring oscillator TDC. When implemented in FPGA, this technique is more area efficient than the simple Verner delay line. Vernier TDC is preferred in fine time interpolation because it trades latency for resolution and area for range. Moreover, the TDC as variety of 2D Vernier time to digital converter, based on gated ring oscillators is also introduces for complementary metal-oxide-semiconductor (CMOS) based converter [6].

In "Wave Union" TDC event triggers a train of pulses or *wave union* launched in a regular delay line of TDC where multiple measurements occur [7]. This architecture of TDC is specifically designed to be used in FPGA.

Other TDCs that is implemented using a direct technique should be mentioned are delta-sigma ($\Sigma\Delta$) [8], pulse shrinking [9], and several flavours of TDC based on ring oscillators [10] [11] [12].

B. Indirect technique

In the 1970s first TDC appeared where time-domain conversion to voltage or amplitude domain was used to measure the time between two events [13]. Nowadays, the sub-picosecond resolution requirements are standard for many applications, and to achieve this goal, designers look back to classical schematics and implement them using modern analogue components.

A Time to voltage (TVC) or time to Amplitude Converter (TAC) converts time interval into a voltage. This functionality usually is implemented as a constant current integrator where a capacitor is charged with a constant current. An ADC then quantises the voltage and passes it to the interpolator to convert its value to time.

A counter or other TDC can be used instead of ADC to determine TI between two events. The main limitation of such a method is the resolution that can be enhanced by stretching the time. In this method, the schematic contains two current sources. One is constantly slowly discharging the capacitor with a small current, but the other is quickly charging with a significantly higher current. The charging of the capacitor

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happens only between the start and stop events. The resulting voltage on the capacitor is a triangle where the rising slope is proportional to the time between two events.

C. Event timers

Recently the technology of event timing, based on the registration of the moments of events (time-tag, time-stamp) relative to a discrete time scale, has found more and more widespread use in SLR [14] [15], Time Transfer and absolute gravimeter [16].

For a long time, the development of event timing technology was constrained by the need to record large format and volume data, which is no longer a significant limitation for modern electronics. Historically, the equipment for implementing event timing is called event timers (although there is an unavoidable conflict with the generally accepted terminology, where it is conventional to call a timer not a meter, but a device that generates a signal at a given moment in time).

The operation principle of most Event timers is the same. The coarse time counter is responsible for tracking the time scale and synchronising it with the reference signal. Fine time detection is responsible for the interpolator, which precisely calculates phase shift between event and coarse time clock. The interpolation methods are the main difference in all event timers, but almost all detect phase shifts between the coarse time clock and the event.

Time-stretching is a well-established technique for time interval measurements, and it has the advantage of providing flexibility in the form of the stretching factor. This allows the user to select the optimal operating mode and adjust the “dead time” and resolution of the interpolator to the specific needs of the experiment. When used as an interpolator in asynchronous interval measurements together with TDC, this time interval measurement technique can be used as one of the key blocks of the event timer.

This paper starts with an introduction to the principles of event timing. Chapter II gives an overview of the interpolation methods currently used in event timers. The concept of using time stretching interpolation is presented in Chapter 3. The paper concludes in Chapter IV, discussing how the presented interpolation method can be used in event timers in combined with off-the-shelf available TDC.

II. Principles of Event timer operation

Event timers, in a sense, are a unique class of measurement devices. The main difference between general-purpose TDC or Time of Flight ToF and Event timers is its ability to register events in a discrete time scale. The main advantage between TI meters and event timers is their ability to measure the overlapped time intervals between Start and Stop events and register several Stop events initiated by one Start event.

As applied to the event timing technology, measurement of time intervals is no more than a special case of determining the difference between two registered moments of events, which are the moments of generation of the TI start and stop signals. The event timing technology makes it possible to solve problems that go beyond the capabilities of traditional methods for measuring TI, for example, to measure multi-stop TI (when one initiating pulse corresponds to several second responses). The classical use of event timers is Satellite Laser Ranging (SLR), where in combination with high-speed interfaces (USB3 or SpaceWire™), opens up previously unavailable opportunities for continuous time-stamping of events streams in time [17].

Of the newest applications is quantum astronomy, where information about cosmic objects can be obtained by studying the correlation of photon fluxes from the object under study [18].

A. Structure of event timer

The operation principle of most Event timers is the same. The resulting time tag is a combination of two timers – coarse time and a fine time. In Fig. 1, a sample block diagram of event timer build is shown according to the scheme” two inputs - one measurement channel,” where the name suggests - both input signals are registered by one measurement channel. The coarse time counter module tracks the time scale and keeps it synchronised with the reference signal. A discrete time scale module responsible for coarse time usually is implemented using the direct TDC method, i.e., counter. The interpolator is responsible for the fine time code conversion. It precisely calculates phase shift between event and coarse time clock.

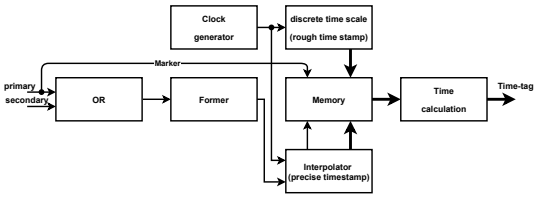

Fig. 1. Block diagram of a two-input event timer.

Precise event timing implementation requires the interpolation of the coarse timing of the event within the clock generator period. Interpolation consists of precise phase measurement of the moment of input event arrival relative to the moments of clock pulse generation.

The former in Fig. 1 performs a logic level converting function, and the pulse signal associated with the event from an input is passed to the interpolator through it. The interpolator outputs fine time code and organises consistent reading of coarse time code. Using fine and coarse event time codes is then possible to calculate complete event timing.

B. Interpolation methods

A large number of interpolation methods are historically known. However, many of them, for example, the TDC based on the Vernier principle, are practically not used at present due to the considerable dead time. The most widespread now are two principles of interpolation, based on two different approaches to measuring the phase of the arrival of an input event relative to clock pulses.

One of the interpolation methods involves detecting and measuring the so-called asynchronous interval between the arrival of the input event and the generation of the first (usually second) clock pulse that is closest in time and converting this interval into a voltage level. This method is based on the indirect TDC implementation method TVC/TAC mentioned in the introduction section of this work. The node for separating the asynchronous interval and generating the coarse-scale readout signal is called a synchroniser, shown in Fig. 4.

1) Tapped delay line interpolator: This modern interpolation method assumes the generation of an additional thin time scale on the delay elements within the clock generator period and reading the state of this scale at the time of the event. This method makes it possible to obtain a short (within a few nanoseconds) dead time of timing with precision from units to tens of picoseconds, depending on the implementation of delays. A good example is the Texas Instruments ASIC THS788 [19], which has a coarse-scale of an 833ps clock and a fine-scale of 13ps in the form of 64 PECL gates daisy-chained to achieve RMS precision of 8ps single-shot TI. Such characteristics allow obtaining very low dead time and Event Input Rate up to 200MHz. Currently, the possibilities of implementing similar principles on FPGA are actively explored.

2) Analogue memory interpolator: This interpolation method is distinguished primarily because it does not require the extraction of the asynchronous interval. The technique can be interpreted as ”memorising” the moment of an event in the form of a known form analogue signal, tied in time to the moment of the event. The input pulse corresponding to the moment of the event triggers the generation of a triangular analogue signal with a duration of 2-3 clock periods Fig. 2. Initially, the analogue signal level is outside the operating range of the ADC, so the conversion output codes are zero. When the first significant ADC code arrives, it is written to memory, and this code displays the phase shift between the moment the input signal arrives and the coarse clock signal edge. The value of the corresponding discrete time scale is written in memory.

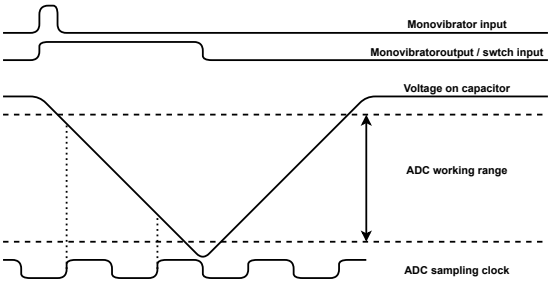

Fig. 2. Analog ”memory” interpolator’s timing diagram.

In known implementations [20], the generated analogue signal can be more complex, for example, Surface Acoustic Wave (SAW) with multiple ADCs readouts shown in Fig. 3.

This increases the dead time but allows for higher precision (however, it should be taken to account that each subsequent readout has lower efficiency, since due to noise, as the analogue signal is generated, the “memory” of the moment of the input event is lost).

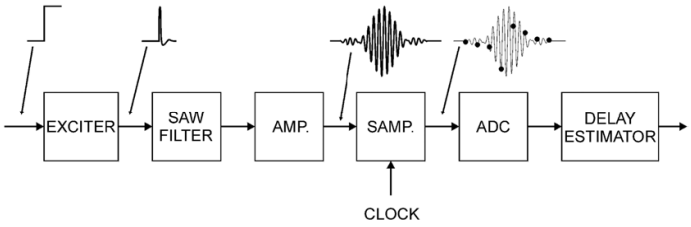

Fig. 3. Block scheme of the time measurement device based on a SAW filter. [20].

The interpolation method’s key benefit is that it does not require explicitly allocating the asynchronous interval (when allocating the asynchronous interval, one has to reckon with the possibility of the anomalous behaviour of logic when exposed asynchronous signals).

An “analogue memory” interpolator method allows the event timer A033-ET to operate with 2.5-3ps RMS single-shot precision [21]. This method’s downside is 50ns ”dead time” used to process the event and prepare the system for receiving the next event. Higher precision is theoretically achievable by stretching secondary analogue signals, but this approach will increase ”dead time.” In the same way, a shorter ”dead time” is possible by making a sharper triangular secondary signal, but this will affect precision. One more critical parameter that affects the precision and dead time of the timer is the clock’s generator frequency used in the coarse time counter.

Electronic components are continuously evolving. This statement is true to almost all components of the interpolator. Beyond that, different Application-Specific Integrated Circuits (ASIC) are available in the market, and they can be used instead of ADC. The Texas Instruments THS788 Integrated circuit (IC) [19] is one of them, but it also has lower-class analogue TDC7200 [22]. TDC-GPX2 [23] is one more alternative time measurement IC. Each of those ICs has a unique internal structure, precision, and range and can be used in fine time interpolation replacing the classical approach that uses ADC.

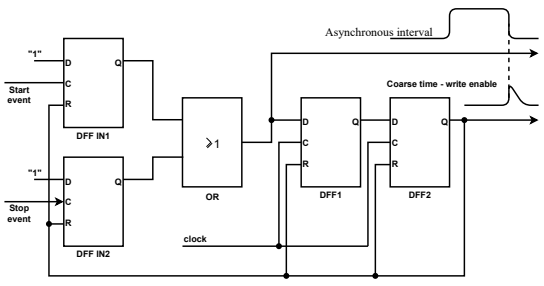

Fig. 4. Two input synchroniser.

3) Synchroniser: In Fig. 4, the rising edge of the asynchronous interval is triggered by the Start or Stop event.

The falling edge of the interval is made synchronous to the following (usually second) reference clock edge.

A practical synchroniser needs to use two D Flip Flops (DFF) for the falling edge synchronisation instead of one. The reason for this is that the propagation delay of a DFF increases when its setup time is violated, which can, in an extreme case, lead to metastability when the Start or Stop event edge and the reference clock edge coincide [24].

When the synchroniser uses two DFFs, the propagation delay of the first DFF can increase by a maximum of one reference clock period without introducing any measurement errors. The additional DFF also adds an offset of one reference clock. As shown in Fig. 5, the minimum and maximum durations of the asynchronous interval are matched to the coarse time scale clock signal. Its length is proportional to the voltage on the capacitor.

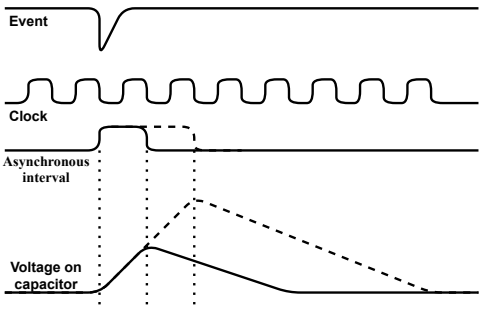

Fig. 5. Asynchronous interval's time-stretching principle.

4) Time stretching interpolator: The time-stretching interpolation method uses a constant current source for the duration of the asynchronous interval to charge the capacitor and slowly discharge with a lower current source. This way, the asynchronous interval is stretched, the value of stretched time interval is determined by the ratio of the charge and discharge currents of the capacitor (Fig. 5). Stretched time intervals are converted to code using one of direct TDC. The timer's overall resolution is increased by the time-stretching factor when measuring the stretched/multiplied asynchronous interval duration. In this case, high precision is achieved, but the time spent on interpolation causes a large dead time of timing.

III. Experimental setup

Time stretching interpolation was already described in section II. Fast current switch schematic width minimal active elements used in A033-ET event timer has well proven itself. The time-stretching circuits are built applying the same principles – simplicity and a minimal amount of active elements. To use TDC as an interpolator, the measurement schematic must extract asynchronous interval. If comparing analogue memory interpolation schematic and time-stretching schematic, they are very similar. One of the fundamental changes is monovibrator replacement by synchroniser to mitigate DFF metastability problem when an event occurs during clocking of DFF and its setup times are violated.

In Fig. 4 is shown a schematic of an asynchronous interval extractor. An event pulse is passed to the first DFF clock input after conversion to Positive Emitter Coupled Logic (PECL) levels. DFF reset happens after the second rising edge of the coarse time clock. The output of this first DFF is our asynchronous interval that needs to be stretched and consequently transferred to fine time code.

In the current research it has been decided not to use any new or untested TDC to evaluate the quality of time stretching circuitry properly. Instead, event timer A033-ET will be used as a TDC. It has 2-3ps RMS single-shot precision, and in this way, the measurement method will minimally affect final data results.

After the asynchronous interval is extracted, it is passed to fast current switches. The process is identical to analogue memory interpolation, only in this interpolation method, charging and discharging time need to be adjusted, and as a result, triangular signal changes in size. Its size is proportional to the length of the asynchronous interval.

To use A033-ET, the test PCB must provide a stop pulse at the end of time stretching when the voltage on a capacitor reached initial levels. The reference voltage generator provides a threshold voltage to output logic.

A. The measurement setup

Fig. 6 is displayed the measurement setup for the experiment. The arbitrary waveform generator from Textronix generates the main 100MHz clock signal for PECL logic and event pulse. By changing the event pulse delay from the main clock, the secondary signal – triangle will be changing in size (Fig. 5).

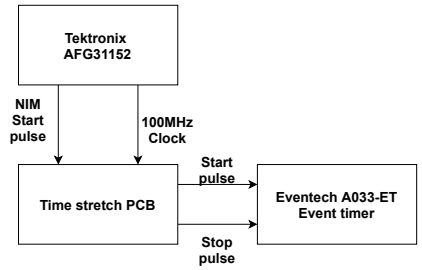

Fig. 6. Test setup of the experiment.

Output logic uses a simple monovibrator built on PECL DFF. When triggered, PECL signals are passed to operational amplifiers that can power a 50Ω terminated transmission line to generate a NIM pulse.

In Fig. 7 is a block diagram of the test PCB, which was designed for this experiment. An arbitrary function generator generates the main clock signal and start pulse (Fig. 6). Logic level converters convert the event to differential PECL pulse and pass it to the synchroniser when receiving the start event. Synchroniser receives input event pulse, and the main clock then extracts asynchronous interval Fig. 5. This extracted interval still is with PECL logical levels. Then extracted asynchronous interval with a minimal length of one clock

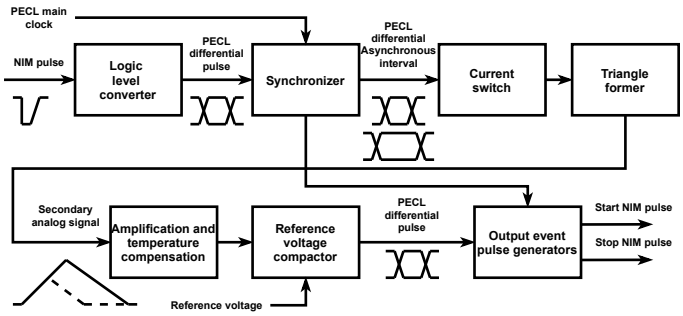

Fig. 7. Block schematics of Test PCB.

period and a maximum length of two clock periods is passed to the Current switch and output event pulse generator. The falling edge of extracted asynchronous interval pulse will trigger the output start event. Current switches will return to the initial state, and the charging capacitor in the triangle former will have its maximal value.

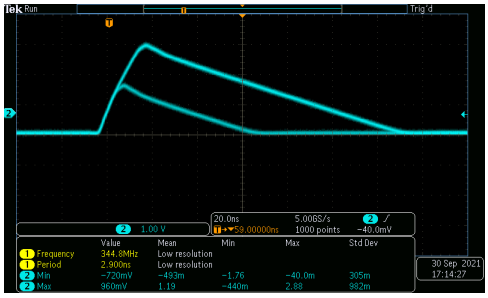

Fig. 8. Minimal and maximal secondary triangle shape signal when stretching factor is 6.56

When current switches are turned off at the falling edge of the asynchronous interval charging capacitor starts discharging with a constant current. As a result, in the Triangle former's output is a secondary analogue signal with a triangle shape, in which height is proportional to the length of the synchronous interval Fig. 8. This triangle signal is passed to a comparator that compares its level with the reference voltage. When the voltage on the analogue triangle drops below the reference voltage comparator triggers a differential event pulse, which generates the output stop event. In this way, PCB outputs two event pulses first one when the triangle has its maximum and charging current is switched off, and the second one when the circuit returns to an initial state. The time interval between those pulses is proportional to the length of the asynchronous interval. By adjusting the discharge current, it is possible to stretch this time interval.

There are no ideal current sources, and all currents – charging and discharging will have a noise component. The fact that time is stretched means that the stretching mechanism will significantly impact measurement results. Higher is stretching coefficient larger the noise impact will be on the measurement result due to the multiplicative relationship between asynchronous interval and its stretched equivalent.

B. Measurement results

Fig. 9 is displayed three measurement sessions with different discharge current values. The measurements of the asynchronous interval were performed by changing the delay of the event pulse in 500ps steps. In Fig. 5, it can be seen that asynchronous interval length is between 10ps and 20ps. In Fig. 9, can be seen that the measured interval and asynchronous interval have a linear relationship.

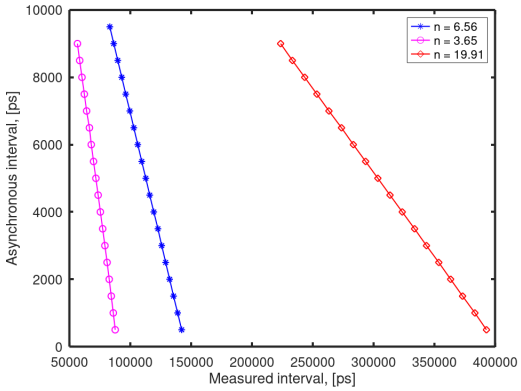

Fig. 9. Asynchronous interval measurements with three different time-stretching factors, where n is stretching factor and also the ratio between charging and discharging currents

Every individual asynchronous interval that is measured is stretched with the same factor. This multiplicative relationship between time interval and constant stretch factor results in a multiplicative stretch of standard deviation spread. In Fig. 10, the measured RMS values from measurements are divided by the stretch factor.

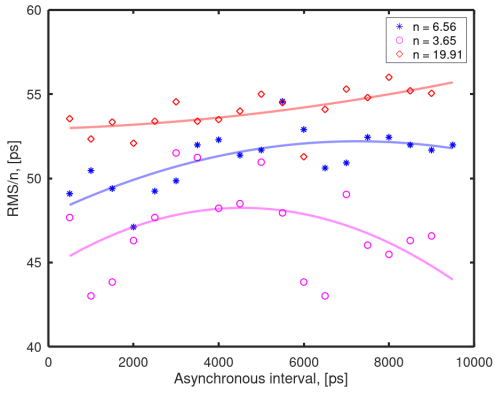

Fig. 10. Asynchronous interval vs RMS of measurement divided by stretch factor n

Fig. 11 is a captured histogram of the start pulse from an arbitrary function generator used to initiate secondary analogue signal - triangle generation. Unfortunately, due to high ambient noise in the laboratory, this high-class generator can only provide around 30ps RMS precision of start pulse generation. This, of course, does not allow an evaluation of the quality of time stretching circuitry fully.

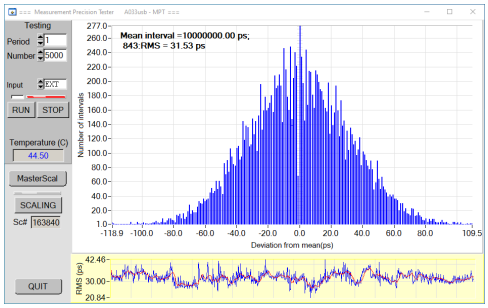

Fig. 11. RMS of start pulse generated by an arbitrary function generator

Comparing measured values from Fig. 10 with RMS around 50ps and source RMS – 30ps, the overall result is promising considering that the same ambient noise affects test PCB.

In current observations and measurements, the ambient noise is a significant factor limiting this interpolator implementation. In the successive iterations, it is planned that critical components will be equipped with additional shielding. The measurements will be performed in for this use case adopted chamber to limit noise effects on measurements.

IV. Conclusion

The classical method of asynchronous interval measurement using the time to amplitude converter and the time-stretching technique is proposed in this paper. In combination with modern off-the-shelf available time to digital converter, this method allows significantly improved resolution of time interval measurements and allows measure time interval that is shorter than the minimal measurement range of the integrated circuit. In combination with the time stretching technique, the off-the-shelf components allow building low-cost time interval meters with improved and adaptive measurement parameters that otherwise will be available only in high-end analogues Also, in combination with other methods like the counter method is possible to develop low-cost Event timers or long-range time interval meters. By increasing the stretching factor, the RMS of the resulting measurements are more stable, but due to the multiplicative nature of time stretching, additional noise is added to the result. Great care needs to be done to limit the noise in key nodes of the circuit, like, fast current switches, current sources, reference voltage, and comparators.

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References

[1] Z. Wang, C. Huang, and J. Wu, "A review of CMOS time-to-digital converter," *Journal of Circuits, Systems, and Computers*, vol. 23, no. 07, p. 1430001, 2014.

[2] E. Bayer and M. Traxler, "A High-Resolution (<10ps RMS) 48-Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA)," *IEEE Transactions on nuclear science*, vol. 58, no. 4, pp. 1547–1552, 2011.

[3] J. Torres, A. Aguilar, R. Garcia-Olcina, P. Martı, J. Martos, J. Soret, J. Benlloch, P. Conde, A. González, F. Sanchez *et al.*, "Time-to-digital converter based on FPGA with multiple channel capability," *IEEE Transactions on Nuclear Science*, vol. 61, no. 1, pp. 107–114, 2013.

[4] P. Dudek, S. Szczepanski, and J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 2, pp. 240–247, 2000.

[5] M. P. Mattada and H. Guhilot, "Area efficient vernier Time to Digital Converter (TDC) with improved resolution using identical ring oscillators on FPGA," in *INTERNATIONAL CONFERENCE ON SMART STRUCTURES AND SYSTEMS-ICSSS'13*. IEEE, 2013, pp. 125–130.

[6] M. Jurgo and R. Navickas, "Comparison of tdc parameters in 65 nm and 0.13 μm cmos," in *2017 5th IEEE Workshop on Advances in Information, Electronic and Electrical Engineering (AIEEE)*. IEEE, 2017, pp. 1–4.

[7] J. Wu and Z. Shi, "The 10-ps wave union TDC: Improving FPGA TDC resolution beyond its cell delay," in *2008 IEEE Nuclear Science Symposium Conference Record*. IEEE, 2008, pp. 3440–3446.

[8] Y. J. Park, P. Parekh, and F. Yuan, "All-digital $\Delta\Sigma$ time-to-digital converter with Bi-Directional gated delay line time integrator," *Microelectronics Journal*, vol. 81, pp. 179–191, 2018.

[9] P. Chen, S.-L. Liu, and J. Wu, "A CMOS pulse-shrinking delay element for time interval measurement," *IEEE Transactions on Circuits and Systems II: Analog and digital signal processing*, vol. 47, no. 9, pp. 954–958, 2000.

[10] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator TDC with first-order noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, 2009.

[11] Y. Mingyan, Z. Shixin *et al.*, "A temperature stabilized multi-path gated ring oscillator based TDC," in *2012 International Conference on Computer Science and Information Processing (CSIP)*. IEEE, 2012, pp. 703–708.

[12] J. P. Caram, J. Galloway, and J. S. Kenney, "Harmonic ring oscillator time-to-digital converter," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2015, pp. 161–164.

[13] B. Turko, "A modular 125ps resolution time interval digitizer for 10MHz stop burst rates and 33ms range," *IEEE Transactions on Nuclear Science*, vol. 26, no. 1, pp. 737–745, 1979.

[14] Y. Artyukh, V. Bespal'ko, K. Lapushka, and A. Rybakov, "Event timing system for Riga SLR station," in *Proceedings of the 15th International Workshop on Laser Ranging*, vol. 2, 2008, pp. 306–310.

[15] H. Sun, H.-F. Zhang, Z.-P. Zhang, and B. Wu, "Experiment on diffuse reflection laser ranging to space debris and data analysis," *Research in Astronomy and Astrophysics*, vol. 15, no. 6, p. 909, 2015.

[16] W. Zhang, X. Wang, W. Ye, J. Shen, X. Hao, and M. Zhong, "Application of event timer in small fast absolute gravimeter," *Journal of Geodesy and Geodynarnics (in Chinese)*, vol. 32, no. 1, pp. 149–151, 2012.

[17] W. Peiyuan, K. Franz, K. Georg, and S. Michael, "Contributions to sub-MHz SLR in Graz," in *ILRS Technical Workshop Stuttgart*, 2019.

[18] C. Gouiffes, C. Barbieri, P. Bouchet, G. Kannbach, C. Motch, H. Pedersen, and A. Shearer, "Fifty years of high time resolution astrophysics at la silla: results and prospects," *The La Silla Observatory-From the Inauguration to the Future*, p. 12, 2019.

[19] Texas Instruments, "THS788 Quad-Channel Time Measurement Unit (TMU) datasheet (Rev. D)," *Texas Instruments*, 2015.

[20] P. Panek, I. Prochazka, and J. Kodet, "Time measurement device with four femtosecond stability," *Metrologia*, vol. 47, no. 5, p. L13, 2010.

[21] V. Bespal'ko and A. Rybakov, "Correlation method for estimation of event timing precision," *Automatic Control and Computer Sciences*, vol. 47, no. 1, pp. 38–47, 2013.

[22] Texas Instruments, "TDC7200 Time-to-Digital Converter for Time-of-Flight Applications in LIDAR, Magnetostrictive and Flow Meters datasheet (Rev. D)," *Texas Instruments*, 2016.

[23] Sciosense B.V., "TDC-GPX2 4-Channel Time-to-Digital Converter," *Sciosense B.V.*, 2017.

[24] P. KERNEN, "High precision time-to-digital converters for applications requiring a wide measurement range," *University of Oulu Graduate School, University of Ouluensis*, 2016.