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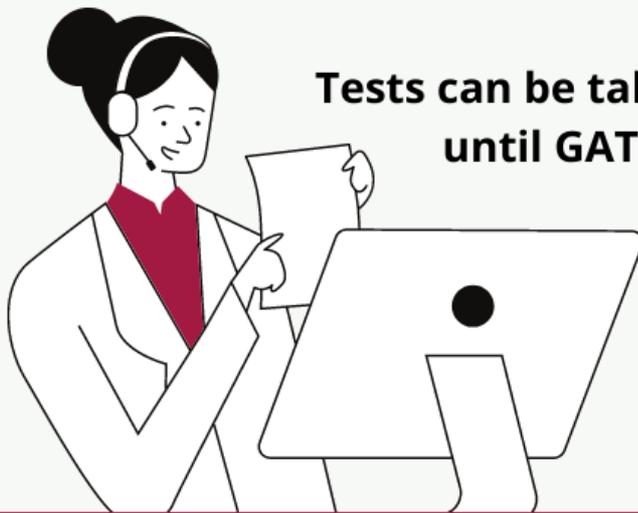


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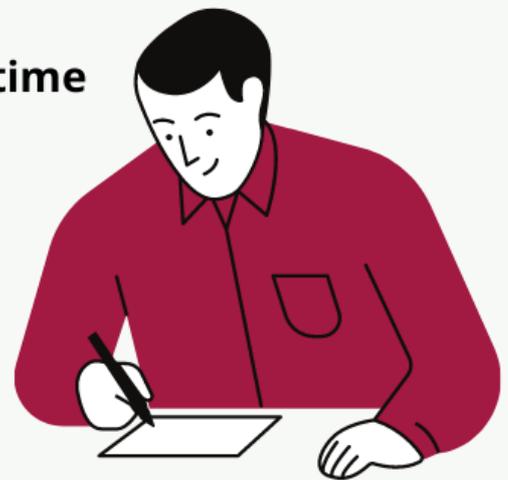
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Machine instructions and Addressing modes. ALU, data-path and control unit. Instruction pipelining. **Pipeline hazards**, Memory hierarchy: cache, main memory and secondary storage; I/O interface (Interrupt and DMA mode)

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	1	2	3	2	2	2	0	1	1	0	1.5	3
2 Marks Count	2	2	4	1	3	4	3	2	5	1	2.8	5
Total Marks	5	6	11	4	8	10	6	5	11	4	7.3	11

1.1.1 Addressing Modes: GATE CSE 1987 | Question: 1-V [top](#)

<https://gateoverflow.in/80194>



The most relevant addressing mode to write position-independent codes is:

- A. Direct mode
- B. Indirect mode
- C. Relative mode
- D. Indexed mode

gate1987 co-and-architecture addressing-modes

Answer [?](#)

1.1.2 Addressing Modes: GATE CSE 1988 | Question: 9iii [top](#)

<https://gateoverflow.in/94388>



In the program scheme given below indicate the instructions containing any operand needing relocation for position independent behaviour. Justify your answer.

```

Y = 10
MOV X(R0), R1
MOV X, R0
MOV 2(R0), R1
MOV Y(R0), R5
.
.
.
X: WORD 0, 0, 0

```

gate1988 normal descriptive co-and-architecture addressing-modes

Answer [?](#)

1.1.3 Addressing Modes: GATE CSE 1989 | Question: 2-ii [top](#)

<https://gateoverflow.in/87078>



Match the pairs in the following questions:

(A) Base addressing	(p) Reentrancy
(B) Indexed addressing	(q) Accumulator
(C) Stack addressing	(r) Array
(D) Implied addressing	(s) Position independent

gate1989 match-the-following co-and-architecture addressing-modes easy

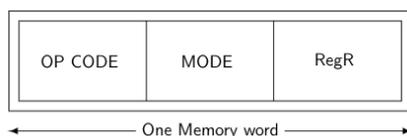
Answer [?](#)

1.1.4 Addressing Modes: GATE CSE 1993 | Question: 10 [top](#)

<https://gateoverflow.in/2307>



The instruction format of a CPU is:



Mode and RegR together specify the operand. RegR specifies a CPU register and Mode specifies an addressing mode. In particular, Mode = 2 specifies that 'the register RegR contains the address of the operand, after fetching the operand, the contents of RegR are incremented by 1'.

An instruction at memory location 2000 specifies Mode = 2 and the RegR refers to program counter (PC).

- A. What is the address of the operand?
- B. Assuming that is a non-jump instruction, what are the contents of PC after the execution of this instruction?

gate1993 co-and-architecture addressing-modes normal descriptive

Answer

1.1.5 Addressing Modes: GATE CSE 1996 | Question: 1.16, ISRO2016-42 top

<https://gateoverflow.in/2720>



Relative mode of addressing is most relevant to writing:

- A. Co – routines
- B. Position – independent code
- C. Shareable code
- D. Interrupt Handlers

gate1996 co-and-architecture addressing-modes easy isro2016

Answer

1.1.6 Addressing Modes: GATE CSE 1998 | Question: 1.19 top

<https://gateoverflow.in/1656>



Which of the following addressing modes permits relocation without any change whatsoever in the code?

- A. Indirect addressing
- B. Indexed addressing
- C. Base register addressing
- D. PC relative addressing

gate1998 co-and-architecture addressing-modes easy

Answer

1.1.7 Addressing Modes: GATE CSE 1999 | Question: 2.23 top

<https://gateoverflow.in/1500>



A certain processor supports only the immediate and the direct addressing modes. Which of the following programming language features cannot be implemented on this processor?

- A. Pointers
- B. Arrays
- C. Records
- D. Recursive procedures with local variable

gate1999 co-and-architecture addressing-modes normal multiple-selects

Answer

1.1.8 Addressing Modes: GATE CSE 2000 | Question: 1.10 top

<https://gateoverflow.in/633>



The most appropriate matching for the following pairs

X: Indirect addressing 1: Loops
 Y: Immediate addressing 2: Pointers
 Z: Auto decrement addressing 3: Constants

is

- A. $X - 3, Y - 2, Z - 1$
- B. $X - 1, Y - 3, Z - 2$
- C. $X - 2, Y - 3, Z - 1$
- D. $X - 3, Y - 1, Z - 2$

gate2000-cse co-and-architecture normal addressing-modes

Answer

1.1.9 Addressing Modes: GATE CSE 2001 | Question: 2.9 top

<https://gateoverflow.in/727>



Which is the most appropriate match for the items in the first column with the items in the second column:

X. Indirect Addressing	I. Array implementation
Y. Indexed Addressing	II. Writing relocatable code
Z. Base Register Addressing	III. Passing array as parameter

- A. (X, III), (Y, I), (Z, II)
- B. (X, II), (Y, III), (Z, I)
- C. (X, III), (Y, II), (Z, I)
- D. (X, I), (Y, III), (Z, II)

gate2001-cse co-and-architecture addressing-modes normal

Answer

1.1.10 Addressing Modes: GATE CSE 2002 | Question: 1.24 top

<https://gateoverflow.in/829>



In the absolute addressing mode:

- A. the operand is inside the instruction
- B. the address of the operand is inside the instruction
- C. the register containing the address of the operand is specified inside the instruction
- D. the location of the operand is implicit

gate2002-cse co-and-architecture addressing-modes easy

Answer

1.1.11 Addressing Modes: GATE CSE 2004 | Question: 20 top

<https://gateoverflow.in/1017>



Which of the following addressing modes are suitable for program relocation at run time?

- I. Absolute addressing
 - II. Based addressing
 - III. Relative addressing
 - IV. Indirect addressing
- A. I and IV
 - B. I and II
 - C. II and III
 - D. I, II and IV

gate2004-cse co-and-architecture addressing-modes easy

Answer



Consider a three word machine instruction

$ADDA[R_0], @B$

The first operand (destination) " $A[R_0]$ " uses indexed addressing mode with R_0 as the index register. The second operand (source) " $@B$ " uses indirect addressing mode. A and B are memory addresses residing at the second and third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is:

- A. 3
- B. 4
- C. 5
- D. 6

gate2005-cse co-and-architecture addressing-modes normal

Answer



Match each of the high level language statements given on the left hand side with the most natural addressing mode from those listed on the right hand side.

- | | |
|--------------------------------|-------------------------|
| (1) $A[I] = B[J]$ | (a) Indirect addressing |
| (2) <code>while (*A++);</code> | (b) Indexed addressing |
| (3) <code>int temp = *x</code> | (c) Auto increment |

- A. (1, c), (2, b), (3, a)
- B. (1, c), (2, c), (3, b)
- C. (1, b), (2, c), (3, a)
- D. (1, a), (2, b), (3, c)

gate2005-cse co-and-architecture addressing-modes easy

Answer



Which of the following is/are true of the auto-increment addressing mode?

- I. It is useful in creating self-relocating code
- II. If it is included in an Instruction Set Architecture, then an additional ALU is required for effective address calculation
- III. The amount of increment depends on the size of the data item accessed

- A. I only
- B. II only
- C. III only
- D. II and III only

gate2008-cse addressing-modes co-and-architecture normal isro2009

Answer



Consider a hypothetical processor with an instruction of type $LW\ R1, 20(R2)$, which during execution reads a $32 - bit$ word from memory and stores it in a $32 - bit$ register $R1$. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register $R2$. Which of the following best reflects the addressing mode implemented by this instruction for the operand in memory?

- A. Immediate addressing
- B. Register addressing
- C. Register Indirect Scaled Addressing

D. Base Indexed Addressing

1.1.16 Addressing Modes: GATE CSE 2017 Set 1 | Question: 11 top



Consider the C struct defined below:

```
struct data {
    int marks [100];
    char grade;
    int cnumber;
};
struct data student;
```

The base address of student is available in register $R1$. The field student.grade can be accessed efficiently using:

- A. Post-increment addressing mode, $(R1)+$
- B. Pre-decrement addressing mode, $-(R1)$
- C. Register direct addressing mode, $R1$
- D. Index addressing mode, $X(R1)$, where X is an offset represented in $2'$ s complement $16 - bit$ representation

1.1.17 Addressing Modes: GATE IT 2006 | Question: 39, ISRO2009-42 top



Which of the following statements about relative addressing mode is FALSE?

- A. It enables reduced instruction size
- B. It allows indexing of array element with same instruction
- C. It enables easy relocation of data
- D. It enables faster address calculation than absolute addressing

1.1.18 Addressing Modes: GATE IT 2006 | Question: 40 top



The memory locations 1000, 1001 and 1020 have data values 18, 1 and 16 respectively before the following program is executed.

```
MOVI     $R_s, 1$            ; Move immediate
LOAD     $R_d, 1000(R_s)$     ; Load from memory
ADDI     $R_d, 1000$          ; Add immediate
STOREI   $0(R_d), 20$        ; Store immediate
```

Which of the statements below is TRUE after the program is executed ?

- A. Memory location 1000 has value 20
- B. Memory location 1020 has value 20
- C. Memory location 1021 has value 20
- D. Memory location 1001 has value 20

Answers: Addressing Modes

1.1.1 Addressing Modes: GATE CSE 1987 | Question: 1-V top



- ✓ (C) Relative Mode since we can just change the content of base register if we wish to relocate.

REFERENCE: <https://gateoverflow.in/155280/self-doubt-computer-organization?show=155312>

References



26 votes

classroom.gateover

-- srestha (85.2k points)

1.1.2 Addressing Modes: GATE CSE 1988 | Question: 9iii top

<https://gateoverflow.in/94388>



MOV instructions here are problematic for Position Independent behaviour if they use Indexed addressing mode and the base address is loaded using some Absolute value.

I'm assuming R_0 is having some relative address. So, the first two MOV instructions are fine for Position Independent behaviour.

But MOV $2(R_0), R_1$

is not fine for position independent behaviour as the source operand address here is $2 + R_0 = 2 + X$ which remains the same even when program is loaded to a new address. So, it should catch invalid content when program is loaded to a new address.

Similarly the last MOV will also cause problem.

5 votes

-- Arjun Suresh (332k points)

1.1.3 Addressing Modes: GATE CSE 1989 | Question: 2-ii top

<https://gateoverflow.in/87078>



✓

(A) Base addressing	(s) Position independent (By changing the value in base register, location of address can be changed)
(B) Indexed addressing	(r) Array
(C) Stack addressing	(p) Reentrancy (Whenever code happens to be used again, address need not be the same)
(D) Implied addressing	(q) Accumulator (If an address is not specified, it is assumed/implied to be the Accumulator)

32 votes

-- Prashant Singh (47.2k points)

1.1.4 Addressing Modes: GATE CSE 1993 | Question: 10 top

<https://gateoverflow.in/2307>



✓

- Address of the operand = content of PC = 2001 as PC holds the address of the next instruction to be executed and instruction size is 1 – word as given in the diagram.
- After execution of the current instruction PC will be automatically incremented by 1 when the next instruction is fetched. Also one extra increment will be done by operand fetch. So, PC = 2003 supposing next instruction is fetched. If we assume next instruction fetch is not done (this should be the default here), it should be 2002.

31 votes

-- Arjun Suresh (332k points)

1.1.5 Addressing Modes: GATE CSE 1996 | Question: 1.16, ISRO2016-42 top

<https://gateoverflow.in/2720>



✓

Answer is (B).

Relative mode addressing is most relevant to writing a position-independent code.

Reference: http://en.wikipedia.org/wiki/Addressing_mode#PC-relative

References



26 votes

-- Rajarshi Sarkar (27.9k points)

1.1.6 Addressing Modes: GATE CSE 1998 | Question: 1.19 top

https://gateoverflow.in/1656



- ✓ (D) PC relative addressing is the best option. For Base register addressing, we have to change the address in the base register while in PC relative there is absolutely no change in code needed.

36 votes

-- Arjun Suresh (332k points)

1.1.7 Addressing Modes: GATE CSE 1999 | Question: 2.23 top

https://gateoverflow.in/1500



- ✓ Pointer access requires indirect addressing which can be simulated with indexed addressing or register indirect addressing but not with direct and immediate addressing. An array and record access needs a pointer access. So, options (A), (B) and (C) cannot be implemented on such a processor.

Now, to handle recursive procedures we need to use stack. A local variable inside the stack will be accessed as $*(SP + \text{offset})$ which is nothing but a pointer access and requires indirect addressing. Usually this is done by moving the **SP** value to Base register and then using Base Relative addressing to avoid unnecessary memory accesses for indirect addressing- but not possible with just direct and immediate addressing.

So, options (A), (B), (C) and (D) are correct.

70 votes

-- Arjun Suresh (332k points)

1.1.8 Addressing Modes: GATE CSE 2000 | Question: 1.10 top

https://gateoverflow.in/633



- ✓ (C) is the most appropriate one.

General instruction format: **opcode|Mode|Address Field|**

Pointer dereference → Indirect addressing, $E.A = M$ [Value stored in address field]

Operating with a constant → Immediate addressing, $E.A = \text{Address field of the instruction}$.

Loop iteration counter check → Auto decrement addressing $R1 = R1 - 1$; $E.A = R1$

E.A = Effective address, where the required operand will be found.

28 votes

-- Bhagirathi Nayak (11.7k points)

1.1.9 Addressing Modes: GATE CSE 2001 | Question: 2.9 top

https://gateoverflow.in/727



- ✓ (A) is the answer.

Array implementation can use Indexed addressing.

While passing array as parameter we can make use of a pointer (as in (C)) and hence can use Indirect addressing.

Base Register addressing can be used to write relocatable code by changing the content of Base Register.

49 votes

-- Arjun Suresh (332k points)

1.1.10 Addressing Modes: GATE CSE 2002 | Question: 1.24 top

https://gateoverflow.in/829



- ✓ (B) is the answer. Absolute addressing mode means address of operand is given in the instruction.

option (A), operand is inside the instruction → immediate addressing

option (C), register containing the address is specified in operand → register Indirect addressing

option (D), the location of operand is implicit → implicit addressing

60 votes

-- gatecse (63.3k points)

1.1.11 Addressing Modes: GATE CSE 2004 | Question: 20

https://gateoverflow.in/1017



✓ Answer: (C)

A displacement type addressing should be preferred. So, (I) is not the answer.

Indirect Addressing leads to extra memory reference which is not preferable at run time. So, (IV) is not the answer.

33 votes

-- Rajarshi Sarkar (27.9k points)

1.1.12 Addressing Modes: GATE CSE 2005 | Question: 65

https://gateoverflow.in/1388

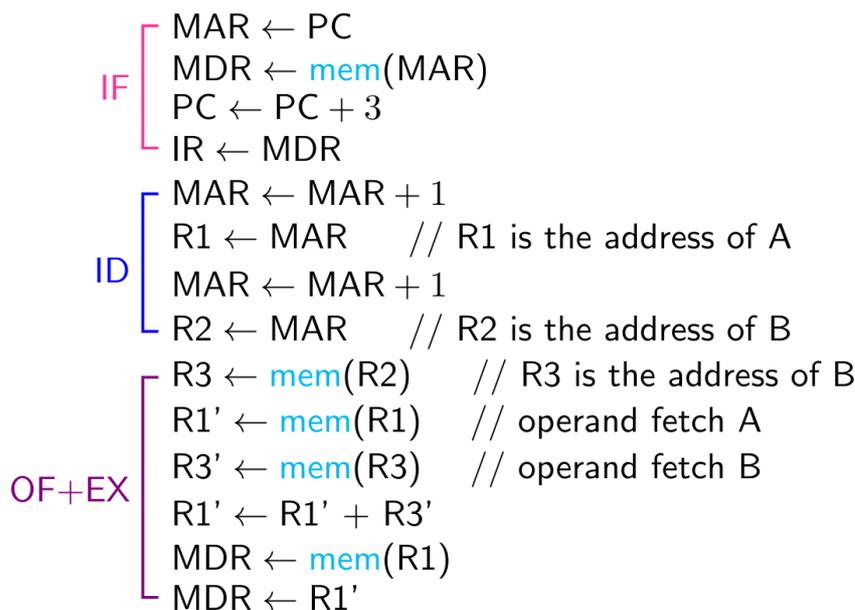


- ✓ 1 memory read to get the first operand from memory address $A + R_0$ (A is given as part of instruction)
- 1 memory read to get the address of the second operand (since second uses indirect addressing)
- 1 memory read to get the second operand from the address given by the previous memory read
- 1 memory write to store to first operand (which is the destination)

So, total of 4 memory cycles once the instruction is fetched.

The second and third words of the instruction are loaded as part of the Instruction fetch and not during the execute stage.

Reference: <http://www.cs.iit.edu/~cs561/cs350/fetch/fetch.html>



Correct Answer: B

References



gateoverflow.in

gateoverflow.in

classroom.gateover

121 votes

-- Arjun Suresh (332k points)

1.1.13 Addressing Modes: GATE CSE 2005 | Question: 66

https://gateoverflow.in/1389



✓ C is the answer.

- $A[i] = B[j]$; Indexed addressing

- while (*A ++); Auto increment
- temp =* x; Indirect addressing

👍 32 votes

-- Arjun Suresh (332k points)

1.1.14 Addressing Modes: GATE CSE 2008 | Question: 33, ISRO2009-80 [top](#)

<https://gateoverflow.in/444>



- ✓ In auto increment addressing mode, the base address is incremented after operand fetch. This is useful in fetching elements from an array. But this has no effect in self-relocating code (where code can be loaded to any address) as this works on the basis of an initial base address.

An additional ALU is desirable for better execution especially with pipelining, but never a necessity.

Amount of increment depends on the size of the data item accessed as there is no need to fetch a part of a data.

So, answer must be C only.

👍 79 votes

-- Arjun Suresh (332k points)

1.1.15 Addressing Modes: GATE CSE 2011 | Question: 21 [top](#)

<https://gateoverflow.in/2123>



- ✓ Answer is (D).

Base Index Addressing, as the content of register R2 will serve as the index and 20 will be the Base address.

👍 49 votes

-- Rajarshi Sarkar (27.9k points)

1.1.16 Addressing Modes: GATE CSE 2017 Set 1 | Question: 11 [top](#)

<https://gateoverflow.in/118291>



- ✓ Answer is option (D).

Displacement Mode :-

Similar to index mode, except instead of an index register a base register will be used. Base register contains a pointer to a memory location. An integer (constant) is also referred to as a displacement. The address of the operand is obtained by adding the contents of the base register plus the constant. The difference between index mode and displacement mode is in the number of bits used to represent the constant. When the constant is represented a number of bits to access the memory, then we have index mode. Index mode is more appropriate for array accessing; displacement mode is more appropriate for structure (records) accessing.

Reference:

<http://www.cs.iit.edu/~cs561/cs350/addressing/addsclm.html>

References



👍 50 votes

-- Niraj Raghuvanshi (263 points)

1.1.17 Addressing Modes: GATE IT 2006 | Question: 39, ISRO2009-42 [top](#)

<https://gateoverflow.in/3578>



- ✓
- A. is true as instead of absolute address we can use a much smaller relative address in instructions which results in smaller instruction size.

B. By using the base address of array as displacement and index in a base register (base relative addressing mode) we can index array elements using relative addressing.

Ref: http://service.scs.carleton.ca/sivarama/asm_book_web/Instructor_copies/ch5_addrmodes.pdf

C. is true as we only need to change the base address in case of relocation- instructions remain the same.

D. is false. Relative addressing cannot be faster than absolute addressing as absolute address must be calculated from relative address. With specialized hardware unit, this can perform equally as good as absolute addressing but not faster.

Correct Answer: D

References



overflow.in

gateoverflow.in

classroom.gateover

71 votes

-- Arjun Suresh (332k points)

1.1.18 Addressing Modes: GATE IT 2006 | Question: 40 top

<https://gateoverflow.in/3581>



- Before the execution of the program, the memory contents are-

18	1000
1	1001
16	1020

Memory

Now, let's execute the program instructions one by one-

1. **Instruction-01: MOVI $R_s, 1$**

- This instruction uses immediate addressing mode.
- The instruction is interpreted as $R_s \leftarrow 1$.
- Thus, value = 1 is moved to the register R_s .

2. **Instruction-02: LOAD $R_d, 1000(R_s)$**

- This instruction uses indexed addressing mode.
- The instruction is interpreted as $R_d \leftarrow [1000 + [R_s]]$.
- Value of the operand = $[1000 + [R_s]] = [1000 + 1] = [1001] = 1$.
- Thus, value = 1 is moved to the register R_d .

3. **Instruction-03: ADDI $R_d, 1000$**

- This instruction uses immediate addressing mode.
- The instruction is interpreted as $R_d \leftarrow [R_d] + 1000$.
- Value of the operand = $[R_d] + 1000 = 1 + 1000 = 1001$.
- Thus, value = 1001 is moved to the register R_d .

4. **Instruction-04: STOREI $0(R_d), 20$**

- This instruction uses indexed addressing mode.
- The instruction is interpreted as $0 + [R_d] \leftarrow 20$.
- Value of the destination address = $0 + [R_d] = 0 + 1001 = 1001$.
- Thus, value = 20 is moved to the memory location 1001.

Hence, after the program execution is completed, memory location 1001 has a value 20.

Option D is correct.

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classroom.gateover

39 votes

-- Sambhrant Maurya (2.6k points)

D is the answer. Memory location 1001 has value 20.

$R_s \leftarrow 1$ (Immediate Addressing)

$R_d \leftarrow 1$ (Indexed Addressing, value at memory location $1 + 1000 = 1001$ is loaded to R_d which is 1)

$R_d \leftarrow 1001$ (R_d becomes $1 + 1000$)

store in address $1001 \leftarrow 20$

49 votes

-- Abhinav Rana (723 points)

1.2

Cache Memory (63) top 5

1.2.1 Cache Memory: GATE CSE 1987 | Question: 4b top 5

https://gateoverflow.in/81360



What is cache memory? What is rationale of using cache memory?

gate1987

co-and-architecture

cache-memory

descriptive

goclasses.in

tests.gatecse.in

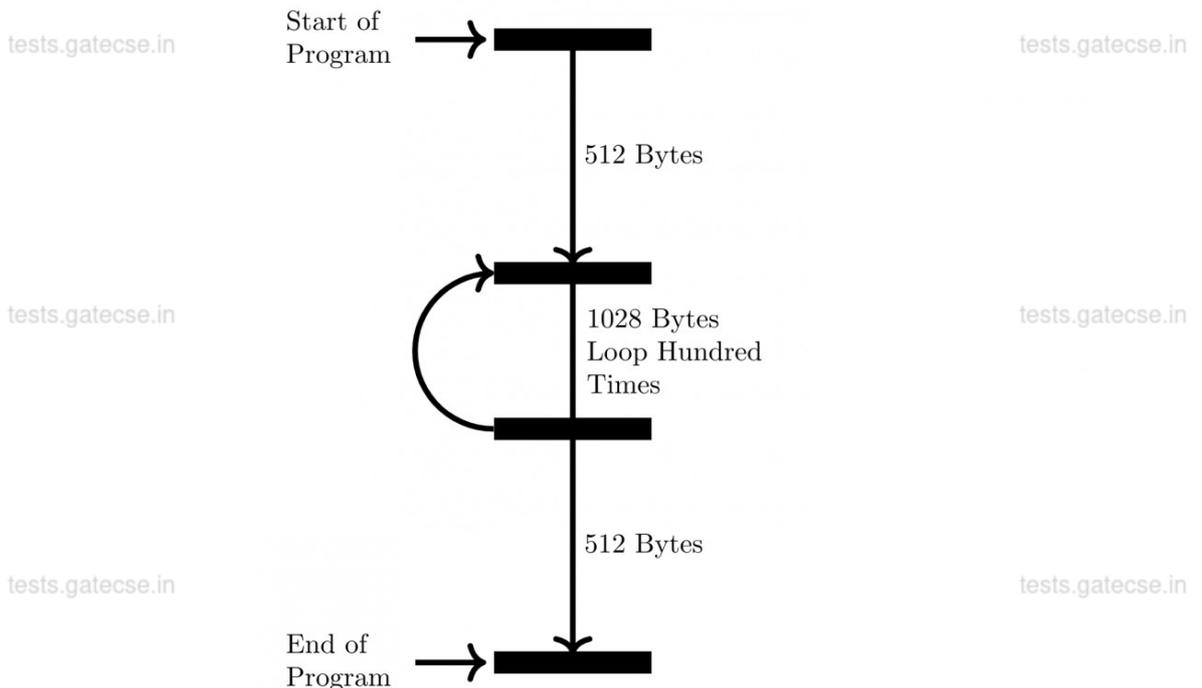
Answer

1.2.2 Cache Memory: GATE CSE 1989 | Question: 6a top 5

https://gateoverflow.in/88557



A certain computer system was designed with cache memory of size 1 Kbytes and main memory size of 256 Kbytes. The cache implementation was fully associative cache with 4 bytes per block. The CPU memory data path was 16 bits and the memory was 2-way interleaved. Each memory read request presents two 16-bit words. A program with the model shown below was run to evaluate the cache design.



Answer the following questions:

- What is the hit ratio?
- Suggest a change in the program size of model to improve the hit ratio significantly.

gate1989

descriptive

co-and-architecture

cache-memory

Answer



A block-set associative cache memory consists of 128 blocks divided into four block sets. The main memory consists of 16,384 blocks and each block contains 256 eight bit words.

1. How many bits are required for addressing the main memory?
2. How many bits are needed to represent the TAG, SET and WORD fields?

gate1990 descriptive co-and-architecture cache-memory

Answer



The access times of the main memory and the Cache memory, in a computer system, are 500 n sec and 50 nsec, respectively. It is estimated that 80% of the main memory request are for read the rest for write. The hit ratio for the read access only is 0.9 and a write-through policy (where both main and cache memories are updated simultaneously) is used. Determine the average time of the main memory (in ns).

gate1992 co-and-architecture cache-memory normal numerical-answers

Answer



In the three-level memory hierarchy shown in the following table, p_i denotes the probability that an access request will refer to M_i .

Hierarchy Level (M_i)	Access Time (t_i)	Probability of Access (p_i)	Page Transfer Time (T_i)
M_1	10^{-6}	0.99000	0.001 sec
M_2	10^{-5}	0.00998	0.1 sec
M_3	10^{-4}	0.00002	---

If a miss occurs at level M_i , a page transfer occurs from M_{i+1} to M_i and the average time required for such a page swap is T_i . Calculate the average time t_A required for a processor to read one word from this memory system.

gate1993 co-and-architecture cache-memory normal descriptive

Answer



The principle of locality justifies the use of:

- A. Interrupts
- B. DMA
- C. Polling
- D. Cache Memory

gate1995 co-and-architecture cache-memory easy

Answer



A computer system has a $4K$ word cache organized in block-set-associative manner with 4 blocks per set, 64 words per block. The number of bits in the SET and WORD fields of the main memory address format is:

- A. 15, 40
- B. 6, 4
- C. 7, 2
- D. 4, 6

Answer

1.2.8 Cache Memory: GATE CSE 1996 | Question: 26 [top](#)

<https://gateoverflow.in/2778>



A computer system has a three-level memory hierarchy, with access time and hit ratios as shown below:

Level 1 (Cache memory) Access time = $50n\text{sec}/\text{byte}$ Level 2 (Main memory) Access time = $200n\text{sec}/\text{byte}$

Size	Hit ratio
8M bytes	0.80
16M bytes	0.90
64M bytes	0.95

Size	Hit ratio
4M bytes	0.98
16M bytes	0.99
64M bytes	0.995

Level 3 Access time = $5\mu\text{sec}/\text{byte}$

Size	Hit ratio
260M bytes	1.0

- What should be the minimum sizes of level 1 and 2 memories to achieve an average access time of less than $100n\text{sec}$?
- What is the average access time achieved using the chosen sizes of level 1 and level 2 memories?

Answer

1.2.9 Cache Memory: GATE CSE 1998 | Question: 18 [top](#)

<https://gateoverflow.in/1732>



For a set-associative Cache organization, the parameters are as follows:

t_c	Cache Access Time
t_m	Main memory access time
l	Number of sets
b	Block size
$k \times b$	Set size

Calculate the hit ratio for a loop executed 100 times where the size of the loop is $n \times b$, and $n = k \times m$ is a non-zero integer and $1 \leq m \leq l$.

Give the value of the hit ratio for $l = 1$.

Answer

1.2.10 Cache Memory: GATE CSE 1999 | Question: 1.22 [top](#)

<https://gateoverflow.in/1475>



The main memory of a computer has 2 cm blocks while the cache has 2 c blocks. If the cache uses the set associative mapping scheme with 2 blocks per set, then block k of the main memory maps to the set:

- $(k \bmod m)$ of the cache
- $(k \bmod c)$ of the cache
- $(k \bmod 2c)$ of the cache
- $(k \bmod 2\text{ cm})$ of the cache

Answer

1.2.11 Cache Memory: GATE CSE 2001 | Question: 1.7, ISRO2008-18 [top](#)

<https://gateoverflow.in/700>



More than one word are put in one cache block to:

- exploit the temporal locality of reference in a program
- exploit the spatial locality of reference in a program
- reduce the miss penalty
- none of the above

gate2001-cse co-and-architecture easy cache-memory isro2008

Answer

1.2.12 Cache Memory: GATE CSE 2001 | Question: 9 [top](#)

<https://gateoverflow.in/750>



A CPU has 32 – *bit* memory address and a 256 *KB* cache memory. The cache is organized as a 4 – *way* set associative cache with cache block size of 16 bytes.

- A. What is the number of sets in the cache?
- B. What is the size (in bits) of the tag field per cache block?
- C. What is the number and size of comparators required for tag matching?
- D. How many address bits are required to find the byte offset within a cache block?
- E. What is the total amount of extra memory (in bytes) required for the tag bits?

gate2001-cse co-and-architecture cache-memory normal descriptive

Answer

1.2.13 Cache Memory: GATE CSE 2002 | Question: 10 [top](#)

<https://gateoverflow.in/863>



In a C program, an array is declared as `float A[2048]`. Each array element is 4 Bytes in size, and the starting address of the array is `0x00000000`. This program is run on a computer that has a direct mapped data cache of size 8 Kbytes, with block (line) size of 16 Bytes.

- A. Which elements of the array conflict with element `A[0]` in the data cache? Justify your answer briefly.
- B. If the program accesses the elements of this array one by one in reverse order i.e., starting with the last element and ending with the first element, how many data cache misses would occur? Justify your answer briefly. Assume that the data cache is initially empty and that no other data or instruction accesses are to be considered.

gate2002-cse co-and-architecture cache-memory normal descriptive

Answer

1.2.14 Cache Memory: GATE CSE 2004 | Question: 65 [top](#)

<https://gateoverflow.in/1059>



Consider a small two-way set-associative cache memory, consisting of four blocks. For choosing the block to be replaced, use the least recently used (LRU) scheme. The number of cache misses for the following sequence of block addresses is:

8, 12, 0, 12, 8.

- A. 2
- B. 3
- C. 4
- D. 5

gate2004-cse co-and-architecture cache-memory normal

Answer

1.2.15 Cache Memory: GATE CSE 2005 | Question: 67 [top](#)

<https://gateoverflow.in/1390>



Consider a direct mapped cache of size 32 *KB* with block size 32 *bytes*. The *CPU* generates 32 *bit* addresses. The number of bits needed for cache indexing and the number of tag bits are respectively,

- A. 10, 17
- B. 10, 22
- C. 15, 17
- D. 5, 17

gate2005-cse co-and-architecture cache-memory easy

Answer



Consider two cache organizations. First one is 32 KB 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has latency of 0.6 ns while a k -bit comparator has latency of $\frac{k}{10}$ ns. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2 .

The value of h_1 is:

- A. 2.4 ns
- B. 2.3 ns
- C. 1.8 ns
- D. 1.7 ns

gate2006-cse

co-and-architecture

cache-memory

normal

Answer



Consider two cache organizations. First one is 32 kB 2-way set associative with 32 byte block size, the second is of same size but direct mapped. The size of an address is 32 bits in both cases. A 2-to-1 multiplexer has latency of 0.6 ns while a k -bit comparator has latency of $\frac{k}{10}$ ns. The hit latency of the set associative organization is h_1 while that of direct mapped is h_2 .

The value of h_2 is:

- A. 2.4 ns
- B. 2.3 ns
- C. 1.8 ns
- D. 1.7 ns

gate2006-cse

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cache-memory

normal

Answer



A CPU has a 32KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512 × 512 with elements that occupy 8-bytes each. Consider the following two C code segments, P_1 and P_2 .

P_1 :

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

P_2 :

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

P_1 and P_2 are executed independently with the same initial state, namely, the array A is not in the cache and i ,

j ,

x are in registers. Let the number of cache misses experienced by P_1 be M_1 and that for P_2 be M_2 .

The value of M_1 is:

- A. 0
- B. 2048
- C. 16384
- D. 262144

gate2006-cse

co-and-architecture

cache-memory

normal

Answer



A CPU has a 32 KB direct mapped cache with 128 byte-block size. Suppose A is two dimensional array of size 512×512 with elements that occupy 8 – bytes each. Consider the following two C code segments, $P1$ and $P2$.

$P1$:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[i] [j];
    }
}
```

$P2$:

```
for (i=0; i<512; i++)
{
    for (j=0; j<512; j++)
    {
        x +=A[j] [i];
    }
}
```

$P1$ and $P2$ are executed independently with the same initial state, namely, the array A is not in the cache and i, j, x are in registers. Let the number of cache misses experienced by $P1$ be $M1$ and that for $P2$ be $M2$.

The value of the ratio $\frac{M1}{M2}$:

- A. 0
- B. $\frac{1}{16}$
- C. $\frac{1}{8}$
- D. 16

co-and-architecture cache-memory normal gate2006-cse

Answer



Consider a 4-way set associative cache consisting of 128 lines with a line size of 64 words. The CPU generates a 20 – bit address of a word in main memory. The number of bits in the TAG, LINE and WORD fields are respectively:

- A. 9, 6, 5
- B. 7, 7, 6
- C. 7, 5, 8
- D. 9, 5, 6

gate2007-cse co-and-architecture cache-memory normal

Answer



Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

How many data misses will occur in total?

- A. 48
- B. 50
- C. 56
- D. 59

gate2007-cse co-and-architecture cache-memory normal

Answer



Consider a machine with a byte addressable main memory of 2^{16} bytes. Assume that a direct mapped data cache consisting of 32 lines of 64 bytes each is used in the system. A 50×50 two-dimensional array of bytes is stored in the main memory starting from memory location $1100H$. Assume that the data cache is initially empty. The complete array is accessed twice. Assume that the contents of the data cache do not change in between the two accesses.

Which of the following lines of the data cache will be replaced by new blocks in accessing the array for the second time?

- A. line 4 to line 11
- B. line 4 to line 12
- C. line 0 to line 7
- D. line 0 to line 8

gate2007-cse co-and-architecture cache-memory normal

Answer

1.2.23 Cache Memory: GATE CSE 2008 | Question: 35 [top](#)

<https://gateoverflow.in/446>



For inclusion to hold between two cache levels L_1 and L_2 in a multi-level cache hierarchy, which of the following are necessary?

- I. L_1 must be write-through cache
- II. L_2 must be a write-through cache
- III. The associativity of L_2 must be greater than that of L_1
- IV. The L_2 cache must be at least as large as the L_1 cache

- A. IV only
- B. I and IV only
- C. I, II and IV only
- D. I, II, III and IV

gate2008-cse co-and-architecture cache-memory normal

Answer

1.2.24 Cache Memory: GATE CSE 2008 | Question: 71 [top](#)

<https://gateoverflow.in/43490>



Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
    for(j = 0; j < 1024; j++)
        ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array ARR is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array ARR .

The total size of the tags in the cache directory is:

- A. 32 Kbits
- B. 34 Kbits
- C. 64 Kbits
- D. 68 Kbits

gate2008-cse co-and-architecture cache-memory normal

Answer

1.2.25 Cache Memory: GATE CSE 2008 | Question: 72 [top](#)

<https://gateoverflow.in/43490>



Consider a machine with a 2-way set associative data cache of size 64 Kbytes and block size 16 bytes. The cache is managed using 32 bit virtual addresses and the page size is 4 Kbytes. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
```

```
for(i = 0; i < 1024; i++)
  for(j = 0; j < 1024; j++)
    ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array *ARR* is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array *ARR*.

Which of the following array elements have the same cache index as *ARR*[0][0]?

- A. *ARR*[0][4]
- B. *ARR*[4][0]
- C. *ARR*[0][5]
- D. *ARR*[5][0]

gate2008-cse co-and-architecture cache-memory normal

Answer 

1.2.26 Cache Memory: GATE CSE 2008 | Question: 73 [top](#)

<https://gateoverflow.in/43491>



Consider a machine with a 2-way set associative data cache of size 64 *Kbytes* and block size 16 *bytes*. The cache is managed using 32 *bit* virtual addresses and the page size is 4 *Kbytes*. A program to be run on this machine begins as follows:

```
double ARR[1024][1024];
int i, j;
/*Initialize array ARR to 0.0 */
for(i = 0; i < 1024; i++)
  for(j = 0; j < 1024; j++)
    ARR[i][j] = 0.0;
```

The size of double is 8 bytes. Array *ARR* is located in memory starting at the beginning of virtual page $0xFF000$ and stored in row major order. The cache is initially empty and no pre-fetching is done. The only data memory references made by the program are those to array *ARR*.

The cache hit ratio for this initialization loop is:

- A. 0%
- B. 25%
- C. 50%
- D. 75%

gate2008-cse co-and-architecture cache-memory normal

Answer 

1.2.27 Cache Memory: GATE CSE 2009 | Question: 29 [top](#)

<https://gateoverflow.in/1315>



Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks are in the following order:

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Which one of the following memory block will NOT be in cache if LRU replacement policy is used?

- A. 3
- B. 8
- C. 129
- D. 216

gate2009-cse co-and-architecture cache-memory normal

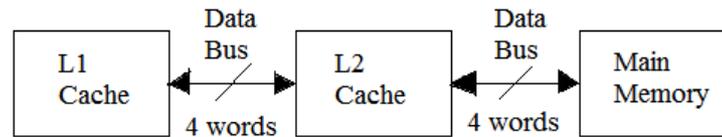
Answer 

1.2.28 Cache Memory: GATE CSE 2010 | Question: 48 [top](#)

<https://gateoverflow.in/2352>



A computer system has an *L1* cache, an *L2* cache, and a main memory unit connected as shown below. The block size in *L1* cache is 4 words. The block size in *L2* cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for *L1* cache, *L2* cache and the main memory unit respectively.



When there is a miss in $L1$ cache and a hit in $L2$ cache, a block is transferred from $L2$ cache to $L1$ cache. What is the time taken for this transfer?

- A. 2 nanoseconds
- B. 20 nanoseconds
- C. 22 nanoseconds
- D. 88 nanoseconds

gate2010-cse co-and-architecture cache-memory normal barc2017

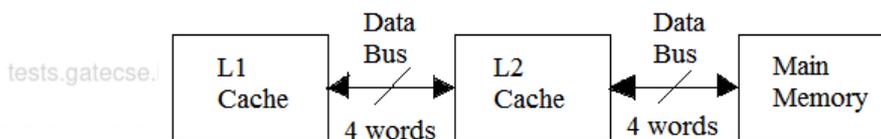
Answer

1.2.29 Cache Memory: GATE CSE 2010 | Question: 49 [top](#)

<https://gateoverflow.in/43329>



A computer system has an $L1$ cache, an $L2$ cache, and a main memory unit connected as shown below. The block size in $L1$ cache is 4 words. The block size in $L2$ cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for $L1$ cache, $L2$ cache and the main memory unit respectively.



When there is a miss in both $L1$ cache and $L2$ cache, first a block is transferred from main memory to $L2$ cache, and then a block is transferred from $L2$ cache to $L1$ cache. What is the total time taken for these transfers?

- A. 222 nanoseconds
- B. 888 nanoseconds
- C. 902 nanoseconds
- D. 968 nanoseconds

gate2010-cse co-and-architecture cache-memory normal

Answer

1.2.30 Cache Memory: GATE CSE 2011 | Question: 43 [top](#)

<https://gateoverflow.in/2145>



An 8KB direct-mapped write-back cache is organized as multiple blocks, each size of 32-bytes. The processor generates 32-bit addresses. The cache controller contains the tag information for each cache block comprising of the following.

- 1 valid bit
- 1 modified bit
- As many bits as the minimum needed to identify the memory block mapped in the cache.

What is the total size of memory needed at the cache controller to store meta-data (tags) for the cache?

- A. 4864 bits
- B. 6144 bits
- C. 6656 bits
- D. 5376 bits

gate2011-cse co-and-architecture cache-memory normal

Answer



A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32-Bytes. The processor sends 32-bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The number of bits in the tag field of an address is

- A. 11
- B. 14
- C. 16
- D. 27

gate2012-cse co-and-architecture cache-memory normal

Answer



A computer has a 256-KByte, 4-way set associative, write back data cache with block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is:

- A. 160 Kbits
- B. 136 Kbits
- C. 40 Kbits
- D. 32 Kbits

normal gate2012-cse co-and-architecture cache-memory

Answer



In a k -way set associative cache, the cache is divided into v sets, each of which consists of k lines. The lines of a set are placed in sequence one after another. The lines in set s are sequenced before the lines in set $(s + 1)$. The main memory blocks are numbered 0 onwards. The main memory block numbered j must be mapped to any one of the cache lines from

- A. $(j \bmod v) * k$ to $(j \bmod v) * k + (k - 1)$
- B. $(j \bmod v)$ to $(j \bmod v) + (k - 1)$
- C. $(j \bmod k)$ to $(j \bmod k) + (v - 1)$
- D. $(j \bmod k) * v$ to $(j \bmod k) * v + (v - 1)$

gate2013-cse co-and-architecture cache-memory normal

Answer



An access sequence of cache block addresses is of length N and contains n unique block addresses. The number of unique block addresses between two consecutive accesses to the same block address is bounded above by k . What is the miss ratio if the access sequence is passed through a cache of associativity $A \geq k$ exercising least-recently-used replacement policy?

- A. $\left(\frac{n}{N}\right)$
- B. $\left(\frac{1}{N}\right)$
- C. $\left(\frac{1}{A}\right)$
- D. $\left(\frac{k}{n}\right)$

gate2014-cse-set1 co-and-architecture cache-memory normal

Answer 

1.2.35 Cache Memory: GATE CSE 2014 Set 2 | Question: 43 [top](#) 

<https://gateoverflow.in/2009>



In designing a computer's cache system, the cache block (or cache line) size is an important parameter. Which one of the following statements is correct in this context?

- A. A smaller block size implies better spatial locality
- B. A smaller block size implies a smaller cache tag and hence lower cache tag overhead
- C. A smaller block size implies a larger cache tag and hence lower cache hit time
- D. A smaller block size incurs a lower cache miss penalty

gate2014-cse-set2

co-and-architecture

cache-memory

normal

Answer 

1.2.36 Cache Memory: GATE CSE 2014 Set 2 | Question: 44 [top](#) 

<https://gateoverflow.in/2010>



If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

- A. Width of tag comparator
- B. Width of set index decoder
- C. Width of way selection multiplexer
- D. Width of processor to main memory data bus

gate2014-cse-set2

co-and-architecture

cache-memory

normal

Answer 

1.2.37 Cache Memory: GATE CSE 2014 Set 2 | Question: 9 [top](#) 

<https://gateoverflow.in/1963>



A 4-way set-associative cache memory unit with a capacity of 16 KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is _____

gate2014-cse-set2

co-and-architecture

cache-memory

numerical-answers

normal

Answer 

1.2.38 Cache Memory: GATE CSE 2014 Set 3 | Question: 44 [top](#) 

<https://gateoverflow.in/2078>



The memory access time is 1 nanosecond for a read operation with a hit in cache, 5 nanoseconds for a read operation with a miss in cache, 2 nanoseconds for a write operation with a hit in cache and 10 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 100 instruction fetch operations, 60 memory operand read operations and 40 memory operand write operations. The cache hit-ratio is 0.9. The average memory access time (in nanoseconds) in executing the sequence of instructions is _____.

gate2014-cse-set3

co-and-architecture

cache-memory

numerical-answers

normal

Answer 

1.2.39 Cache Memory: GATE CSE 2015 Set 2 | Question: 24 [top](#) 

<https://gateoverflow.in/8119>



Assume that for a certain processor, a read request takes 50 nanoseconds on a cache miss and 5 nanoseconds on a cache hit. Suppose while running a program, it was observed that 80% of the processor's read requests result in a cache hit. The average read access time in nanoseconds is _____.

gate2015-cse-set2

co-and-architecture

cache-memory

easy

numerical-answers

Answer 

1.2.40 Cache Memory: GATE CSE 2015 Set 3 | Question: 14 [top](#) 

<https://gateoverflow.in/8410>



Consider a machine with a byte addressable main memory of 2^{20} bytes, block size of 16 bytes and a direct mapped cache having 2^{12} cache lines. Let the addresses of two consecutive bytes in main memory be $(E201F)_{16}$ and $(E2020)_{16}$. What are the

tag and cache line addresses (in hex) for main memory address $(E201F)_{16}$?

- A. $E, 201$
- B. $F, 201$
- C. $E, E20$
- D. $2, 01F$

gate2015-cse-set3 co-and-architecture cache-memory normal

Answer

1.2.41 Cache Memory: GATE CSE 2016 Set 2 | Question: 32 top

<https://gateoverflow.in/39622>



The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is _____ bits.

gate2016-cse-set2 co-and-architecture cache-memory normal numerical-answers

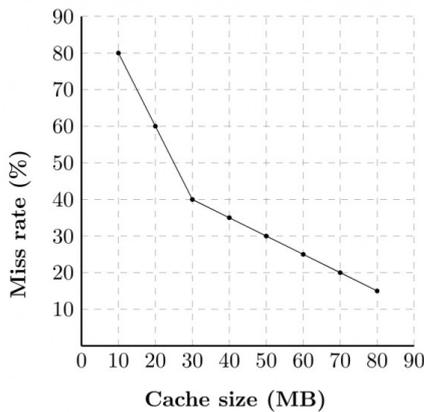
Answer

1.2.42 Cache Memory: GATE CSE 2016 Set 2 | Question: 50 top

<https://gateoverflow.in/39592>



A file system uses an in-memory cache to cache disk blocks. The miss rate of the cache is shown in the figure. The latency to read a block from the cache is 1 ms and to read a block from the disk is 10 ms. Assume that the cost of checking whether a block exists in the cache is negligible. Available cache sizes are in multiples of 10 MB.



The smallest cache size required to ensure an average read latency of less than 6 ms is _____ MB.

gate2016-cse-set2 co-and-architecture cache-memory normal numerical-answers

Answer

1.2.43 Cache Memory: GATE CSE 2017 Set 1 | Question: 25 top

<https://gateoverflow.in/118305>



Consider a two-level cache hierarchy with $L1$ and $L2$ caches. An application incurs 1.4 memory accesses per instruction on average. For this application, the miss rate of $L1$ cache is 0.1; the $L2$ cache experiences, on average, 7 misses per 1000 instructions. The miss rate of $L2$ expressed correct to two decimal places is _____.

gate2017-cse-set1 co-and-architecture cache-memory numerical-answers

Answer

1.2.44 Cache Memory: GATE CSE 2017 Set 1 | Question: 54 top

<https://gateoverflow.in/118748>



A cache memory unit with capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is _____ bits.

gate2017-cse-set1 co-and-architecture cache-memory normal numerical-answers

Answer

1.2.45 Cache Memory: GATE CSE 2017 Set 2 | Question: 29

<https://gateoverflow.in/118371>



In a two-level cache system, the access times of L_1 and L_2 caches are 1 and 8 clock cycles, respectively. The miss penalty from the L_2 cache to main memory is 18 clock cycles. The miss rate of L_1 cache is twice that of L_2 . The average memory access time (AMAT) of this cache system is 2 cycles. The miss rates of L_1 and L_2 respectively are

- A. 0.111 and 0.056
- B. 0.056 and 0.111
- C. 0.0892 and 0.1784
- D. 0.1784 and 0.0892

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gate2017-cse-set2 cache-memory co-and-architecture normal

Answer

1.2.46 Cache Memory: GATE CSE 2017 Set 2 | Question: 45

<https://gateoverflow.in/118597>



The read access times and the hit ratios for different caches in a memory hierarchy are as given below:

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Cache	Read access time (in nanoseconds)	Hit ratio
I-cache	2	0.8
D-cache	2	0.9
L2-cache	8	0.9

The read access time of main memory is 90 nanoseconds. Assume that the caches use the referred-word-first read policy and the write-back policy. Assume that all the caches are direct mapped caches. Assume that the dirty bit is always 0 for all the blocks in the caches. In execution of a program, 60% of memory reads are for instruction fetch and 40% are for memory operand fetch. The average read access time in nanoseconds (up to 2 decimal places) is _____

gate2017-cse-set2 co-and-architecture cache-memory numerical-answers

Answer

1.2.47 Cache Memory: GATE CSE 2017 Set 2 | Question: 53

<https://gateoverflow.in/118613>



Consider a machine with a byte addressable main memory of 2^{32} bytes divided into blocks of size 32 bytes. Assume that a direct mapped cache having 512 cache lines is used with this machine. The size of the tag field in bits is _____

gate2017-cse-set2 co-and-architecture cache-memory numerical-answers

goclasses.in

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Answer

1.2.48 Cache Memory: GATE CSE 2018 | Question: 34

<https://gateoverflow.in/204108>



The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K-way set-associative cache memory, the length (in number of bits) of the tag field is

- A. $P - N - \log_2 K$
- B. $P - N + \log_2 K$
- C. $P - N - M - W - \log_2 K$
- D. $P - N - M - W + \log_2 K$

tests.gatecse.in

goclasses.in

tests.gatecse.in

gate2018-cse co-and-architecture cache-memory normal

Answer

1.2.49 Cache Memory: GATE CSE 2019 | Question: 1

<https://gateoverflow.in/302847>



A certain processor uses a fully associative cache of size 16 kB. The cache block size is 16 bytes. Assume that the main

memory is byte addressable and uses a 32-bit address. How many bits are required for the *Tag* and the *Index* fields respectively in the addresses generated by the processor?

- A. 24 bits and 0 bits
- B. 28 bits and 4 bits
- C. 24 bits and 4 bits
- D. 28 bits and 0 bits

gate2019-cse co-and-architecture cache-memory normal

Answer

1.2.50 Cache Memory: GATE CSE 2019 | Question: 45 top

<https://gateoverflow.in/302803>



A certain processor deploys a single-level cache. The cache block size is 8 words and the word size is 4 bytes. The memory system uses a 60-MHz clock. To service a cache miss, the memory controller first takes 1 cycle to accept the starting address of the block, it then takes 3 cycles to fetch all the eight words of the block, and finally transmits the words of the requested block at the rate of 1 word per cycle. The maximum bandwidth for the memory system when the program running on the processor issues a series of read operations is $\text{_____} \times 10^6$ bytes/sec

gate2019-cse numerical-answers co-and-architecture cache-memory

Answer

1.2.51 Cache Memory: GATE CSE 2020 | Question: 21 top

<https://gateoverflow.in/333210>



A direct mapped cache memory of 1 MB has a block size of 256 bytes. The cache has an access time of 3 ns and a hit rate of 94%. During a cache miss, it takes 20 ns to bring the first word of a block from the main memory, while each subsequent word takes 5 ns. The word size is 64 bits. The average memory access time in ns (round off to 1 decimal place) is _____.

gate2020-cse numerical-answers co-and-architecture cache-memory

Answer

1.2.52 Cache Memory: GATE CSE 2020 | Question: 30 top

<https://gateoverflow.in/333201>



A computer system with a word length of 32 bits has a 16 MB byte- addressable main memory and a 64 KB, 4-way set associative cache memory with a block size of 256 bytes. Consider the following four physical addresses represented in hexadecimal notation.

- A1 = 0x42C8A4,
- A2 = 0x546888,
- A3 = 0x6A289C,
- A4 = 0x5E4880

Which one of the following is TRUE?

- A. A1 and A4 are mapped to different cache sets.
- B. A2 and A3 are mapped to the same cache set.
- C. A3 and A4 are mapped to the same cache set.
- D. A1 and A3 are mapped to the same cache set.

gate2020-cse cache-memory

Answer

1.2.53 Cache Memory: GATE CSE 2021 Set 1 | Question: 22 top

<https://gateoverflow.in/357429>



Consider a computer system with a byte-addressable primary memory of size 2^{32} bytes. Assume the computer system has a direct-mapped cache of size 32 KB (1 KB = 2^{10} bytes), and each cache block is of size 64 bytes.

The size of the tag field is _____ bits.

gate2021-cse-set1 co-and-architecture cache-memory numerical-answers

Answer



Consider a set-associative cache of size 2KB ($1\text{KB} = 2^{10}$ bytes) with cache block size of 64 bytes. Assume that the cache is byte-addressable and a 32-bit address is used for accessing the cache. If the width of the tag field is 22 bits, the associativity of the cache is _____

gate2021-cse-set2 numerical-answers co-and-architecture cache-memory

Answer



Assume a two-level inclusive cache hierarchy, $L1$ and $L2$, where $L2$ is the larger of the two. Consider the following statements.

- S_1 : Read misses in a write through $L1$ cache do not result in writebacks of dirty lines to the $L2$
- S_2 : Write allocate policy *must* be used in conjunction with write through caches and no-write allocate policy is used with writeback caches.

Which of the following statements is correct?

- S_1 is true and S_2 is false
- S_1 is false and S_2 is true
- S_1 is true and S_2 is true
- S_1 is false and S_2 is false

gate2021-cse-set2 co-and-architecture cache-memory

Answer



Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 1 ns , 10 ns , and 500 ns respectively. The hit rates of Level 1 and Level 2 caches are 0.8 and 0.9, respectively. What is the average access time of the system ignoring the search time within the cache?

- 13.0
- 12.8
- 12.6
- 12.4

gate2004-it co-and-architecture cache-memory normal isro2016

Answer



Consider a fully associative cache with 8 cache blocks (numbered 0 – 7) and the following sequence of memory block requests:

4, 3, 25, 8, 19, 6, 25, 8, 16, 35, 45, 22, 8, 3, 16, 25, 7

If LRU replacement policy is used, which cache block will have memory block 7?

- 4
- 5
- 6
- 7

gate2004-it co-and-architecture cache-memory normal

Answer



Consider a 2-way set associative cache memory with 4 sets and total 8 cache blocks (0 – 7) and a main memory with 128 blocks (0 – 127). What memory blocks will be present in the cache after the following sequence of memory block references if LRU policy is used for cache block replacement. Assuming that initially the cache did not have any memory block from the current

job?

0 5 3 9 7 0 16 55

- A. 0 3 5 7 16 55
- B. 0 3 5 7 9 16 55
- C. 0 5 7 9 16 55
- D. 3 5 7 9 16 55

gate2005-it co-and-architecture cache-memory normal

Answer

1.2.59 Cache Memory: GATE IT 2006 | Question: 42 top

https://gateoverflow.in/3585



A cache line is 64 bytes. The main memory has latency 32 ns and bandwidth 1 GBytes/s. The time required to fetch the entire cache line from the main memory is:

- A. 32 ns
- B. 64 ns
- C. 96 ns
- D. 128 ns

gate2006-it co-and-architecture cache-memory normal

Answer

1.2.60 Cache Memory: GATE IT 2006 | Question: 43 top

https://gateoverflow.in/3586



A computer system has a level-1 instruction cache (I-cache), a level-1 data cache (D-cache) and a level-2 cache (L2-cache) with the following specifications:

	Capacity	Mapping Method	Block Size
I-Cache	4K words	Direct mapping	4 words
D-Cache	4K words	2-way set associative mapping	4 words
L2-Cache	64K words	4-way set associative mapping	16 words

The length of the physical address of a word in the main memory is 30 bits. The capacity of the tag memory in the I-cache, D-cache and L2-cache is, respectively,

- A. 1 K x 18-bit, 1 K x 19-bit, 4 K x 16-bit
- B. 1 K x 16-bit, 1 K x 19-bit, 4 K x 18-bit
- C. 1 K x 16-bit, 512 x 18-bit, 1 K x 16-bit
- D. 1 K x 18-bit, 512 x 18-bit, 1 K x 18-bit

gate2006-it co-and-architecture cache-memory normal

Answer

1.2.61 Cache Memory: GATE IT 2007 | Question: 37 top

https://gateoverflow.in/3470



Consider a Direct Mapped Cache with 8 cache blocks (numbered 0 – 7). If the memory block requests are in the following order

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24.

Which of the following memory blocks will not be in the cache at the end of the sequence ?

- A. 3
- B. 18
- C. 20
- D. 30

gate2007-it co-and-architecture cache-memory normal

Answer



Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

The number of bits in the TAG, SET and WORD fields, respectively are:

- A. 7, 6, 7
- B. 8, 5, 7
- C. 8, 6, 6
- D. 9, 4, 7

gate2008-it

co-and-architecture

cache-memory

normal

Answer



Consider a computer with a 4-ways set-associative mapped cache of the following characteristics: a total of 1 MB of main memory, a word size of 1 byte, a block size of 128 words and a cache size of 8 KB.

While accessing the memory location $0C795H$ by the CPU, the contents of the TAG field of the corresponding cache line is:

- A. 000011000
- B. 110001111
- C. 00011000
- D. 110010101

gate2008-it

co-and-architecture

cache-memory

normal

Answer

Answers: Cache Memory



A CPU cache is a hardware cache used by the central processing unit (CPU) of a computer to reduce the average cost (time or energy) to access data from the main memory.

A cache is a smaller, faster memory, located closer to a processor core, which stores copies of the data from frequently used main memory locations. Most CPUs have different independent caches, including instruction and data caches, where the data cache is usually organized as a hierarchy of more cache levels.

Source :- https://en.wikipedia.org/wiki/CPU_cache

References



8 votes

-- Satbir Singh (21k points)



Total number of block access = $(512/4 + 100 \times 1028/4 + 512/4) = 25956$

All the blocks above and below the loop region can be assumed to be cache misses.

It is given that the cache is fully associative but the replacement policy is not mentioned. Let's assume it is FIFO. Also, for simplicity let's assume that there's no reuse within a cache block.

In the first loop access every cache access will be a miss. Since the loop body size is 1028 and we assumed FIFO, the last cache block will replace the first one. In the second iteration, first cache block access will be a miss and this will replace the second cache block. Going like this every cache block access will be a miss.

(i) So, hit ratio = 0.

(ii) By just reducing the loop body size by 4 bytes, all the loop accesses from second iteration of the loop will be a hit. So, we can get a hit ratio of $\frac{99 \times 1024}{101 \times 1024} = 98.01\%$

0 votes

-- gatecse (63.3k points)

1.2.3 Cache Memory: GATE CSE 1990 | Question: 7a top 5

<https://gateoverflow.in/85403>



✓ For main memory, there are 2^{14} blocks and each block size is 2^8 bytes (A byte is an eight-bit word)

1. Size of main memory = $2^{14} \times 2^8 = 4MB$ (22 – bits required for addressing the main memory).
2. For WORD field, we require 8 – bits, as each block contains 2^8 words.

As there are 4 blocks in 1 set, 32 sets will be needed for 128 blocks. Thus SET field requires 5 – bits.

Then, TAG field requires $22 - (5 + 8) = 9$ – bits

9-bits (for tag)	5- bits (for set)	8-bits (for word)
------------------	-------------------	-------------------

46 votes

-- kirti singh (2.6k points)

1.2.4 Cache Memory: GATE CSE 1992 | Question: 5-a top 5

<https://gateoverflow.in/584>



✓ Average memory access time = Time spend for read + Time spend for write

= Read time when cache hit + Read time when cache miss + Write time when cache hit + Write time when cache miss

$$= 0.8 \times 0.9 \times 50 + 0.8 \times 0.1 \times (500 + 50)$$

(assuming hierarchical read from memory and cache as only simultaneous write is mentioned in question)

$$+ 0.2 \times 0.9 \times 500 + 0.2 \times 0.1 \times 500 \quad (\text{simultaneous write mentioned in question})$$

$$= 36 + 44 + 90 + 10 = 180 \text{ ns.}$$

Reference: <http://www.howardhuang.us/teaching/cs232/24-Cache-writes-and-examples.pdf>

References



61 votes

-- Arjun Suresh (332k points)

1.2.5 Cache Memory: GATE CSE 1993 | Question: 11 top 5

<https://gateoverflow.in/2308>



✓ We are given the probability of access being a hit in each level (clear since their sum adds to 1).

So, we can get the average access time as:

$$\begin{aligned} t_A &= 0.99 \times 10^{-6} + 0.00998 \times (10^{-6} + 10^{-5} + 0.001) \\ &+ 0.00002 \times (10^{-6} + 10^{-5} + 10^{-4} + 0.1 + 0.001) \\ &\approx (0.99 + 10 + 2) \times [10^{-6}] = 13\mu s \end{aligned}$$

We can also use the following formula- for 100% of accesses M_1 is accessed, whenever M_1 is a miss, M_2 is accessed and when both misses only M_3 is accessed. So, average memory access time,

$$t_A = 10^{-6} + (1 - 0.99) \times (10^{-5} + 0.001) + 0.00002 \times (10^{-4} + 0.1) = 1 + 10.01 + 2\mu s = 13.01\mu s.$$

37 votes

-- Arjun Suresh (332k points)

Quick Cache Maths:-

Suppose that in 250 memory references there are 30 misses in L1 and 10 misses in L2.

$$\text{Miss rate of L1} = \frac{30}{250}$$

Miss rate of L2 = $\frac{10}{30}$ (In L1 we miss 30 requests, so at L2 we have 30 requests, but it misses 10 out of 30)

See this [question](#).

Here, Probabilities are given, We need to convert it into Hit ratios.

$p_1 = 0.99000$, it says we hit 0.99 times in M_1 but we miss 0.01 times. Here hit rate is same as probability $H_1 = 0.99$

$p_2 = 0.00998$, it says we hit 0.00998 times out of 0.01 requests (0.01 misses from M_1), $H_2 = \frac{0.00998}{0.01} = 0.998$

(H_3 is of course 1. we hit 0.00002 times in M_3 out of 0.00002 misses from M_2)

$H_1 = 0.99$, $H_2 = 0.998$, $H_3 = 1$. t_i is Access time, and T_i is page transfer time.

$$t_A = t_1 + (1 - H_1) \times \text{Miss penalty 1}$$

$$\text{Miss penalty 1} = (t_2 + T_1) + (1 - H_2) \times \text{Miss penalty 2}$$

$$\text{Miss penalty 2} = (t_3 + T_2)$$

Ref: question 3 here

<https://www.cs.utexas.edu/~fussell/courses/cs352.fall98/Homework/old/Solution3.ps>

References



69 votes

-- Sachin Mittal (15.8k points)

1.2.6 Cache Memory: GATE CSE 1995 | Question: 1.6 top

<https://gateoverflow.in/2593>



✓ Answer is (D).

Locality of reference is actually the frequent accessing of any storage location or some value. We can say in simple language that whatever things are used more frequently, they are stored in the locality of reference. So we have cache memory for the purpose.

30 votes

-- Gate Keeda (15.9k points)

1.2.7 Cache Memory: GATE CSE 1995 | Question: 2.25 top

<https://gateoverflow.in/2638>



✓ Number of sets = $\frac{4K}{(64 \times 4)} = 16$

So, we need 4-bits to identify a set \Rightarrow SET = 4 bits.

64 words per block mean WORD is 6-bits.

So, the answer is an option (D).

29 votes

-- Arjun Suresh (332k points)

1.2.8 Cache Memory: GATE CSE 1996 | Question: 26 top

<https://gateoverflow.in/2778>



✓ The equation for access time can be written as follows (assuming a, b are the hit ratios of level 1 and level 2 respectively).

$$T = T_1 + (1 - a)T_2 + (1 - a) \times (1 - b)T_3$$

Here $T \leq 100$, $T_1 = 50ns$, $T_2 = 200ns$ and $T_3 = 5000ns$. On substituting the a, b for the first case we get

$$T = 95ns \text{ for } a = 0.8 \text{ and } b = 0.995. \text{ i.e., } L1 = 8M \text{ and } L2 = 64M.$$

$$T = 75ns \text{ for } a = 0.9 \text{ and } b = 0.99. \text{ i.e., } L1 = 16M \text{ and } L2 = 4M$$

B.

- $L_1 = 8M, a = 0.8, L_2 = 4M, b = 0.98$. So,
 $T = 50 + 0.2 \times 200 + 0.2 \times 0.02 \times 5000 = 50 + 40 + 20 = 110ns$
- $L_1 = 16M, a = 0.9, L_2 = 16M, b = 0.99$. So,
 $T = 50 + 0.1 \times 200 + 0.1 \times 0.01 \times 5000 = 50 + 20 + 5 = 75ns$
- $L_1 = 64M, a = 0.95, L_2 = 64M, b = 0.995$. So,
 $T = 50 + 0.05 \times 200 + 0.05 \times 0.005 \times 5000 = 50 + 10 + 1.25 = 61.25ns$

classroom.gateoverflow.in

👍 23 votes

-- kireeti (1k points)

1.2.9 Cache Memory: GATE CSE 1998 | Question: 18 top ⤴

https://gateoverflow.in/1732



Size of the loop = $n \times b = k \times m \times b$

Size of a set = $k \times b$ (k -way associative)

Here, size of the loop is smaller than size of cache as $m \leq l$. So we are guaranteed that the entire loop is in cache without any replacement. (Here we assumed that the memory size of $n \times b$ used by the loop is contiguous, or else we could have a scenario where the entire loop size gets mapped to the same set causing cache replacement).

For the first iteration:

No. of accesses = $n \times b$

No. of misses = n as each new block access is a miss and loop body has n blocks each of size b for a total size of $n \times b$.

For, the remaining 99 iterations:

No. of accesses = $n \times b$

No. of misses = 0

So, total no. of accesses = $100nb$

Total no. of hits = Total no. of accesses – Total no. of misses

= $100nb - n$

So, hit ratio = $\frac{100nb - n}{100nb} = 1 - \frac{1}{100b}$

The hit ratio is independent of l , so for $l = 1$ also we have hit ratio = $1 - \frac{1}{100b}$

👍 33 votes

classroom.gateoverflow.in
 -- Arjun Suresh (332k points)

1.2.10 Cache Memory: GATE CSE 1999 | Question: 1.22 top ⤴

https://gateoverflow.in/1475



- ✓ Number of cache blocks = $2c$

Number of sets in cache = $\frac{2c}{2} = c$ since each set has 2 blocks. Now, a block of main memory gets mapped to a set (associativity of 2 just means there are space for 2 memory blocks in a cache set), and we have $2cm$ blocks being mapped to c sets. So, in each set $2m$ different main memory blocks can come and block k of main memory will be mapped to $k \bmod c$.

Correct Answer: B.

👍 39 votes

-- Arjun Suresh (332k points)

1.2.11 Cache Memory: GATE CSE 2001 | Question: 1.7, ISRO2008-18 top ⤴

https://gateoverflow.in/700



- ✓ Exploit the spatial locality of reference in a program as, if the next locality is addressed immediately, it will already be in the cache.

Consider the scenario similar to cooking, where when an ingredient is taken from cupboard, you also take the near by ingredients along with it- hoping that they will be needed in near future.

Correct Answer: B

👍 84 votes

-- Arjun Suresh (332k points)

✓ **What is the number of sets in the cache**

$$\begin{aligned} \text{Number of sets} &= \frac{\text{Cache memory}}{(\text{set associativity} \times \text{cache block size})} \\ &= \frac{256KB}{(4 \times 16B)} \\ &= 4096 \end{aligned}$$

What is the size (in bits) of the tag field per cache block?

Memory address size = 32-bit

Number of bits required to identify a particular set = 12 (Number of sets = 4096)

Number of bits required to identify a particular location in cache line = 4 (cache block size = 16)

Size of tag field = 32 - 12 - 4 = 16-bit

What is the number and size of comparators required for tag matching?

We use 4-way set associate cache. So, we need 4 comparators each of size 16-bits

<http://ece.colorado.edu/~ecen2120/Manual/caches/cache.html>

How many address bits are required to find the byte offset within a cache block?

Cache block size is 16-byte. so 4-bits are required to find the byte offset within a cache block.

What is the total amount of extra memory (in bytes) required for the tag bits?

size of tag = 16-bits

Number of sets = 4096

Set associativity = 4

Extra memory required to store the tag bits = $16 \times 4096 \times 4\text{-bits} = 2^{18}$ bits = 2^{15} bytes.

References

👍 42 votes

-- suraj (4.8k points)

✓ **A. Data cache size = 8 KB.**

Block line size = 16 B.

Since each array element occupies 4 B, four consecutive array elements occupy a block line (elements are aligned as starting address is 0)

$$\text{Number of cache blocks} = \frac{8 KB}{16 B} = 512.$$

$$\text{Number of cache blocks needed for the array} = \frac{2048}{4} = 512.$$

So, all the array elements has its own cache block and there is no collision.

We can also explain this with respect to array address.

Starting address is $0x00000000 = 0_b0000 \dots 0(32 \text{ 0's})$.

Ending address is $0x00001FFF = 0_b0000 \dots 011111111111(4 \times 2048 = 8192 \text{ locations}), 0 - 8191$.

Here, the last 4 bits are used as OFFSET bits and the next 9 bits are used as SET bits. So, since the ending address is not extending beyond these 9 bits, all cache accesses are to diff sets.

B. If the last element is accessed first, its cache block is fetched. (which should contain the previous 3 elements of the array also since each cache block hold 4 elements of array and 2048 is an exact multiple of 4). Thus, for every 4 accesses, we will have a cache miss \Rightarrow for 2048 accesses we will have 512 cache misses. (This would be same even if we access array in forward order).

46 votes

-- Arjun Suresh (332k points)

1.2.14 Cache Memory: GATE CSE 2004 | Question: 65 top

<https://gateoverflow.in/1059>



✓ We have 4 blocks and 2 blocks in a set

\Rightarrow there are 2 sets. So blocks will go to sets as follows:

Set Number	Block Number
0	0,8,12
1	gateoverflow.in

Since the lowest bit of block address is used for indexing into the set, so 8, 12 and 0 first miss in cache with 0 replacing 8 (there are two slots in each set due to 2-way set) and then 12 hits in cache and 8 again misses. So, totally 4 misses.

Correct Answer: C

25 votes

-- Arjun Suresh (332k points)

1.2.15 Cache Memory: GATE CSE 2005 | Question: 67 top

<https://gateoverflow.in/1390>



✓ Number of blocks = $\frac{\text{cache size}}{\text{block size}} = \frac{32\text{-KB}}{32} = 1024\text{-Bytes}$.

So, indexing requires 10-bits. Number of OFFSET bits required to access 32-bit block = 5.

So, number of TAG bits = $32 - 10 - 5 = 17$.

So, answer is (A).

36 votes

-- Arjun Suresh (332k points)

1.2.16 Cache Memory: GATE CSE 2006 | Question: 74 top

<https://gateoverflow.in/1851>



✓ Cache size is 32 KB and cache block size is 32 B. So,

$$\begin{aligned} \text{Number of sets} &= \frac{\text{cache size}}{\text{no. of blocks in a set} \times \text{block size}} \\ &= \frac{32 \text{ KB}}{2 \times 32 \text{ B}} = 512 \end{aligned}$$

So, number of index bits needed = 9 (since $2^9 = 512$). Number of offset bits = 5 (since $2^5 = 32 \text{ B}$ is the block size and assuming byte addressing). So, number of tag bits = $32 - 9 - 5 = 18$ (as memory address is of 32 bits).

So, time for comparing the data

$$= \text{Time to compare the data} + \text{Time to select the block in set} = 0.6 + 18/10 \text{ ns} = 2.4 \text{ ns}$$

(Two comparisons of tag bits need to be done for each block in a set, but they can be carried out in parallel and the succeeding one multiplexed as the output).

Reference: <https://courses.cs.washington.edu/courses/cse378/09au/lectures/cse378au09-19.pdf>

Correct Answer: A

References



69 votes

-- Arjun Suresh (332k points)

1.2.17 Cache Memory: GATE CSE 2006 | Question: 75 top

<https://gateoverflow.in/43565>



✓

$$\text{number of sets} = \frac{\text{cache size}}{\text{no. of blocks in a set} \times \text{block size}}$$

$$= \frac{32KB}{1 \times 32B} = 1024$$

So, number of index bits = 10, and

number of tag bits = $32 - 10 - 5 = 17$.

$$\text{So, } h_2 = \frac{17}{10} = 1.7 \text{ ns}$$

Correct Answer: *D*

20 votes

-- Arjun Suresh (332k points)

1.2.18 Cache Memory: GATE CSE 2006 | Question: 80 top

<https://gateoverflow.in/1854>



✓ Code being C implies array layout is row-major.
http://en.wikipedia.org/wiki/Row-major_order

When $A[0][0]$ is fetched, 128 consecutive bytes are moved to cache. So, for the next $\frac{128}{8} - 1 = 15$ memory references there won't be a cache miss.

For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for P_1 is

$$= \frac{512}{16} \times 512$$

$$= 32 \times 512$$

$$= 2^{14} = 16384$$

Correct Answer: *C*

References



51 votes

-- Arjun Suresh (332k points)

1.2.19 Cache Memory: GATE CSE 2006 | Question: 81 top

<https://gateoverflow.in/43517>



✓

$$\text{Number of Cache Lines} = \frac{2^{15} B}{128B} = 256$$

$$\text{In 1 Cache Line} = \frac{128B}{8B} = 16 \text{ elements}$$

$$P_1 = \frac{\text{total elements in array}}{\text{elements in a cache line}}$$

$$= \frac{512 \times 512}{16} = 2^{14} = 16384.$$

$$P_2 = 512 \times 512 = 2^{18}$$

$$\frac{P_1}{P_2} = \frac{16384}{512 \times 512}$$

$$= 2^{14-18} = 2^{-4} = \frac{1}{16}$$

It is so, because for P_1 for every line there is a miss, and once a miss is processed we get 16 elements in memory. So, another miss happens after 16 elements.

For P_2 for every element there is a miss because storage is row major order (by default) and we are accessing column wise.

Hence, answer is option B.

41 votes

-- Amar Vashishth (25.2k points)

Code being C implies array layout is row-major.

http://en.wikipedia.org/wiki/Row-major_order

When $A[0][0]$ is fetched, 128 consecutive bytes are moved to cache. So, for the next $128/8 - 1 = 15$ memory references there won't be a cache miss. For the next iteration of i loop also the same thing happens as there is no temporal locality in the code. So, number of cache misses for P_1

$$= \frac{512}{16} \times 512$$

$$= 32 \times 512$$

$$= 2^{14} = 16384$$

In the case of P_2 , the memory references are not consecutive. After $A[0][0]$, the next access is $A[1][0]$ which is after $512 * 8$ memory locations. Since our cache block can hold only 128 contiguous memory locations, $A[1][0]$ won't be in cache after $A[0][0]$ is accessed. Now, the next location after $A[0][0]$ is $A[0][1]$ which will be accessed only after 512 iterations of the inner loop - after 512 distinct memory block accesses. In our cache we have only space for $32 \text{ KB} / 128 \text{ B} = 256$ memory blocks. So, by the time $A[0][1]$ is accessed, its cache block would be replaced. So, each of the memory access in P_2 results in a cache miss. Total number of cache miss

$$= 512 \times 512$$

$$\text{So, } \frac{M_1}{M_2} = \frac{32 \times 512}{512 \times 512} = \frac{1}{16}$$

References



63 votes

-- Arjun Suresh (332k points)

1.2.20 Cache Memory: GATE CSE 2007 | Question: 10 top

<https://gateoverflow.in/1208>



✓

$$\text{Number of sets} = \frac{\text{cache size}}{(\text{size of a block} * \text{No. of blocks in a set})}$$

$$= \frac{128 * 64}{(64 * 4)} \quad (\text{4 way set associative means 4 blocks in a set})$$

$$= 32.$$

So, number of index (LINE) bits = 5 and number of WORD bits = 6 since cache block (line) size is 64.

So, number of TAG bits = $20 - 6 - 5 = 9$.

Answer is (D) choice

27 votes

-- Arjun Suresh (332k points)



✓ Bits used to represent the address = $\log_2 2^{16} = 16$

Each cache line size = 64 bytes; means offset requires 6-bits

Total number of lines in cache = 32; means line # requires 5-bits

So, tag bits = $16 - 6 - 5 = 5$

We have a 2D-array each of its element is of size = 1 Byte;

Total size of this array = $50 \times 50 \times 1 \text{ Byte} = 2500 \text{ Bytes}$

So, total number of lines it will require to get contain in cache

$$= \frac{2500B}{64B} = 39.0625 \approx 40$$

Starting address of array = $1100H = 00010\ 00100\ 000000$

The group of bits in middle represents Cache Line number \implies array starts from cache line number 4,

We require 40 cache lines to hold all array elements, but we have only 32 cache lines

Lets group/partition our 2500 array elements in those 40 array lines, we call this first array line as A_0 which will have 64 of its elements.

This line(group of 64 elements) of array will be mapped to cache line number 4 as found by analysis of starting address of array above.

This all means that among those 40 array lines some array lines will be mapped to same cache line, coz there are just 32 cache lines but 40 of array lines.

This is how mapping is:

0 A_{28}

1 A_{29}

2 A_{30}

3 A_{31}

4 $A_0\ A_{32}$

5 $A_1\ A_{33}$

6 $A_2\ A_{34}$

7 $A_3\ A_{35}$

8 $A_4\ A_{36}$

9 $A_5\ A_{37}$

10 $A_6\ A_{38}$

11 $A_7\ A_{39}$

12 A_8

⋮

30 A_{26}

31 A_{27}

So, if we access complete array twice we get = $32 + 8 + 8 + 8 = 56$ miss because only 8 lines from cache line number 4 to 11 are miss operation, rest are **Hits(not counted) or Compulsory misses(first 32)**.

Hence, answer is option (C).

👍 250 votes

-- Amar Vashishth (25.2k points)

$2^{16} = 64 \text{ KB}$ main memory is mapped to 32 lines of 64 bytes. So, number of offset bits = 6 (to identify a byte in a line) and number of indexing bits = 5 (to identify the line).

Size of array = $50 * 50 = 2500 \text{ B}$. If array is stored in row-major order (first row, second-row..), and if elements are also accessed in row-major order (or stored and accessed in column-major order), for the first 64 accesses, there will be only 1 cache miss, and for 2500 accesses, there will be $2500/64 = 40$ cache misses during the first iteration.

We have 5 index bits and 6 offset bits. So, for 2^{11} ($5 + 6 = 11$) continuous memory addresses there wont be any cache conflicts as the least significant bits are offset bits followed by index bits.

So, number of array elements that can be accessed without cache conflict = 2048 (as element size is a byte). The next 452 elements conflict with the first 452 elements. This means $452/64 = 8$ cache blocks are replaced. (We used ceil, as even if one element from a new block is accessed, the whole block must be fetched).

So, during second iteration we incur misses for the first 8 cache blocks as well as for the last 8 cache blocks. So, total data cache misses across 2 iterations = $40 + 8 + 8 = 56$.

39 votes

-- Arjun Suresh (332k points)



✓ Cache Organization:

Starting Address = $1100H = 16^3 + 16^2 + 0 + 0 = 4352B$ is the starting address.

We need to find Starting block = $\frac{4352 B}{64 B} = 68^{th}$ block in main memory from where array start storing elements.

$50 \times 50 B = \text{array size} = 50 \times \frac{50 B}{64 B} = 39.0625$ blocks needed ≈ 40 blocks

68,69,70....107 block we need = 40 blocks

Starting block is $68 \pmod{32} = 4^{th}$ cache block and after that in sequence they will be accessed. As shown in below table, line number 4 to 11 has been replaced by array in second time

Cache Block Number	First Cycle	Second cycle
0	96	
1	97	
2	98	
3	99	
4	68 // 100	68
5	69 // 101	69
6	70//102	70
7	71//103	71
8	72//104	72
9	73//105	73
10	74/106	74
11	75//107	75
12	76	
13	77	
14	78	
15	79	
16	80	
17	81	
18	82	
19	83	
20	84	
21	85	
22	86	
23	87	
24	88	
25	89	
26	90	
27	91	
28	92	
29	93	
30	94	
31	95	

Correct Answer: A

👍 52 votes

-- papesh (18k points)

1.2.23 Cache Memory: GATE CSE 2008 | Question: 35 top<https://gateoverflow.in/446>

✓ 1st is not correct as data need not to be exactly same at the same point of time and so write back policy can be used in this.

2nd is not needed when talking only about L1 and L2.

For 3rd, associativity can be equal.

So, only 4th statement is Necessarily true - (A) choice.

👍 49 votes

-- Shaun Patel (6.1k points)

1.2.24 Cache Memory: GATE CSE 2008 | Question: 71 top<https://gateoverflow.in/494>

$$\begin{aligned} \checkmark \quad \text{Number of sets} &= \frac{\text{cache size}}{\text{size of a set}} \\ &= \frac{64 \text{ KB}}{(16 \text{ B} \times 2)} \quad (\text{two blocks per set}) \\ &= 2 \text{ K} = 2^{11} \end{aligned}$$

So, we need 11-bits for set indexing.

Number of **WORD** bits required = 4 as a cache block consists of 16 bytes and we need 4-bits to address each of them.

So, number of tag bits = $32 - 11 - 4 = 17$

Total size of the tag = $17 \times$ Number of cache blocks

$$\begin{aligned} &= 17 \times 2^{11} \times 2 \quad (\text{since each set has 2 blocks}) \\ &= 68 \text{ Kbits} \end{aligned}$$

Answer is option D) 68 Kbits

We use the top 17-bits for tag and the next 11-bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

$ARR[0][0]$ is located at virtual address $0x \text{ FF000 } 000$. (FF000 is page address and 000 is page offset).
So, index bits are 00000000000

Address of $ARR[0][4] = 0x \text{ FF000 } + 4 \times \text{sizeof}(\text{double})$
 $= 0x \text{ FF000 } 000 + 4 \times 8 = 0x \text{ FF000 } 020$ (32 = 20 in hex) (index bits differ)

Address of $ARR[4][0] = 0x \text{ FF000 } + 4 \times 1024 \times \text{sizeof}(\text{double})$
[since we use row major storage]
 $= 0x \text{ FF000 } 000 + 4096 \times 8 = 0x \text{ FF000 } 000 + 0x \text{ 8000} = 0x \text{ FF008 } 000$
(index bits matches that of $ARR[0][0]$ as both read 000 0000 0000)

Address of $ARR[0][5] = 0x \text{ FF000 } + 5 \times \text{sizeof}(\text{double}) = 0x \text{ FF000 } 000 + 5 \times 8 = 0x \text{ FF000 } 028$ (40 = 28 in hex)
(index bits differ)

Address of $ARR[5][0] = 0x \text{ FF000 } + 5 \times 1024 \times \text{sizeof}(\text{double})$ [since we use row major storage]
 $= 0x \text{ FF000 } 000 + 5120 \times 8 = 0x \text{ FF000 } 000 + 0x \text{ A000} = 0x \text{ FF00A } 000$ (index bits differ)

So, only $ARR[4][0]$ and $ARR[0][0]$ have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50 (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

1.2.25 Cache Memory: GATE CSE 2008 | Question: 72 top

<https://gateoverflow.in/43490>



✓ Number of sets = cache size/ size of a set
 = 64 KB/(16 B × 2) (two blocks per set)
 = 2 K = 2¹¹
 So, we need 11 bits for set indexing.

Number of WORD bits required = 4 as a cache block consists of 16 bytes and we need 4 bits to address each of them.

So, number of tag bits = 32 – 11 – 4 = 17

Total size of the tag = 17 × Number of cache blocks
 = 17 × 2¹¹ × 2 (since each set has 2 blocks)
 = 68 KB

We use the top 17 bits for tag and the next 11 bits for indexing and next 4 for offset. So, for two addresses to have the same cache index, their 11 address bits after the 4 offset bits from right must be same.

ARR[0][0] is located at virtual address 0x FF000 000. (FF000 is page address and 000 is page offset). So, index bits are 00000000000

Address of ARR[0][4] = 0xFF000 + 4 × sizeof(double) = 0xFF000000 + 4 × 8 = 0xFF000 020 (32 = 20 in hex)
 (index bits differ)

Address of ARR[4][0] = 0xFF000 + 4 × 1024 × sizeof(double) [since we use row major storage]
 = 0xFF000 000 + 4096 × 8 = 0xFF000 000 + 0x8000 = 0xFF008 000 (index bits matches that of ARR [0][0] as both read 000 0000 0000)

Address of ARR[0][5] = 0xFF000 + 5 × sizeof(double) = 0xFF000 000 + 5 × 8 = 0xFF000 028 (40 = 28 in hex)
 (index bits differ)

Address of ARR[5][0] = 0xFF000 + 5 × 1024 × sizeof(double) [since we use row major storage]
 = 0xFF000 000 + 5120 × 8 = 0xFF000 000 + 0xA000 = 0xFF00A 000 (index bits differ)

So, only ARR[4][0] and ARR[0][0] have the same cache index.

The inner loop is iterating from 0 to 1023, so consecutive memory locations are accessed in sequence. Since cache block size is only 16 bytes and our element being double is of size 8 bytes, during a memory access only the next element gets filled in the cache. i.e.; every alternative memory access is a cache miss giving a hit ratio of 50%. (If loops i and j are reversed, all accesses will be misses and hit ratio will become 0).

Correct Answer: B

1.2.26 Cache Memory: GATE CSE 2008 | Question: 73 top

<https://gateoverflow.in/43491>



✓ Block size = 16B and one element = 8B.
 So, in one block 2 element will be stored.

For 1024 × 1024 element num of block required = $\frac{1024 \times 1024}{2} = 2^{19}$ blocks required.

In one block the first element will be a miss and second one is hit (since we are transferring two unit at a time)

$$\begin{aligned} \Rightarrow \text{hit ratio} &= \frac{\text{Total hit}}{\text{Total reference}} \\ &= \frac{2^{19}}{2^{20}} \\ &= \frac{1}{2} = 0.5 \end{aligned}$$

$$= 0.5 \times 100 = 50\%$$

Correct Answer: *C*

👍 26 votes

-- asutosh kumar Biswal (8k points)

1.2.27 Cache Memory: GATE CSE 2009 | Question: 29 [top](#)

<https://gateoverflow.in/1315>



- ✓ 16 blocks and sets with 4 blocks each means there are 4 sets. So, the lower 2 bits are used for getting a set and 4-way associative means in a set only the last 4 cache accesses can be stored.

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155

mod 4 gives,

0, 3, 1, 0, 3, 0, 1, 3, 0, 1, 3, 0, 0, 0, 1, 0, 3

Now for each of 0..3, the last 4 accesses will be in cache.

So, {92, 32, 48, 8}, {155, 63, 159, 3}, {73, 129, 133, 1} and {} will be in cache.

So, the missing element from choice is 216.

Correct Answer: *D*

👍 60 votes

-- Arjun Suresh (332k points)

1.2.28 Cache Memory: GATE CSE 2010 | Question: 48 [top](#)

<https://gateoverflow.in/2352>



- ✓ Ideally the answer should be 20 ns as it is the time to transfer a block from *L2* to *L1* and this time only is asked in question. But there is confusion regarding access time of *L2* as this means the time to read data from *L2* till CPU but here we need the time till *L1* only. So, I assume the following is what is meant by the question.

A block is transferred from *L2* to *L1*. And *L1* block size being 4 words (since *L1* is requesting we need to consider *L1* block size and not *L2* block size) and data width being 4 bytes, it requires one *L2* access (for read) and one *L1* access (for store). So, time = 20 + 2 = 22 ns.

Correct Answer: *C*

👍 106 votes

-- Arjun Suresh (332k points)

1.2.29 Cache Memory: GATE CSE 2010 | Question: 49 [top](#)

<https://gateoverflow.in/4329>



- ✓ The transfer time should be $4 * 200 + 20 = 820$ ns. But this is not in option. So, I assume the following is what is meant by the question.

L2 block size being 16 words and data width between memory and *L2* being 4 words, we require 4 memory accesses (for read) and 4 *L2* accesses (for store). Now, we need to send the requested block to *L1* which would require one more *L2* access (for read) and one *L1* access (for store). So, total time

$$= 4 * (200 + 20) + (20 + 2)$$

$$= 880 + 22$$

$$= 902 \text{ ns}$$

Correct Answer: *C*

👍 119 votes

-- Arjun Suresh (332k points)

1.2.30 Cache Memory: GATE CSE 2011 | Question: 43 [top](#)

<https://gateoverflow.in/2145>



- ✓
$$\text{Number of cache blocks} = \frac{\text{cache size}}{\text{size of a block}}$$

$$= \frac{8 \text{ KB}}{32 \text{ B}}$$

$$= 256$$

So, we need 8-bits for indexing the 256 blocks of the cache. And since a block is 32 bytes we need 5 WORD bits to address each byte. So, out of the remaining 19-bits (32 - 8 - 5) should be tag bits.

So, a tag entry size = 19 + 1(valid bit) + 1(modified bit) = 21 bits.

$$\begin{aligned} \text{Total size of metadata} &= 21 \times \text{Number of cache blocks} \\ &= 21 \times 256 \\ &= 5376 \text{ bits} \end{aligned}$$

Correct Answer: *D*

👍 46 votes

-- Arjun Suresh (332k points)

1.2.31 Cache Memory: GATE CSE 2012 | Question: 54 top 5

<https://gateoverflow.in/2192>



✓ Total cache size = 256 KB
Cache block size = 32 Bytes
So, number of cache entries = $\frac{256 K}{32} = 8 K$

Number of sets in cache = $\frac{8 K}{4} = 2 K$ as cache is 4-way associative.

So, $\log(2048) = 11$ bits are needed for accessing a set. Inside a set we need to identify the cache entry.

No. of memory block possible = $\frac{\text{Memory size}}{\text{Cache block size}}$

$$= \frac{2^{32}}{32} = 2^{27}$$

So, no. of memory block that can go to a single cache set

$$= \frac{2^{27}}{2^{11}}$$

$$= 2^{16}$$

So, we need 16 tag bits along with each cache entry to identify which of the possible 2^{16} blocks is being mapped there.

Correct Answer: *C*

👍 41 votes

-- Arjun Suresh (332k points)

1.2.32 Cache Memory: GATE CSE 2012 | Question: 55 top 5

<https://gateoverflow.in/43311>



✓ Total cache size = 256 KB
Cache block size = 32 Bytes
So, number of cache entries = $\frac{256 K}{32} = 8 K$

Number of sets in cache = $\frac{8 K}{4} = 2 K$ as cache is 4-way associative.

So, $\log(2048) = 11$ bits are needed for accessing a set. Inside a set we need to identify the cache entry.

Total number of distinct cache entries = $\frac{2^{32}}{\text{cache entry size}} = \frac{2^{32}}{32} = 2^{27}$

Out of this 2^{27} , each set will be getting only $\frac{2^{27}}{2^{11}} = 2^{16}$ possible distinct cache entries as we use the first 11 bits to identify a set. So, we need 16 bits to identify a cache entry in a set, which is the number of bits in the tag field.

Size of cache tag directory = Size of tag entry \times Number of tag entries
= 16 + (2 + 1 + 1) bits (2 valid, 1 modified, 1 replacement as given in question) \times 8 K

= 208 = 160 Kbits

Not needed for this question, still:

Valid bit: Tells if the memory referenced by the cache entry is valid. Initially, when a process is loaded all entries are invalid. Only when a page is loaded, its entry becomes valid.

Modified bit: When processor writes to a cache location its modified bit is made 1. This information is used when a cache entry is replaced- entry 0 means no update to main memory needed. Entry 1 means an update is needed.

Replacement bit: This is needed for the cache replacement policy. Explained in the below link:

<https://www.seas.upenn.edu/~cit595/cit595s10/handouts/LRUreplacementpolicy.pdf>

Correct Answer: A

References



37 votes

-- Arjun Suresh (332k points)

1.2.33 Cache Memory: GATE CSE 2013 | Question: 20 [top](#)

<https://gateoverflow.in/1442>



✓ Number of sets in cache = v .

The question gives a sequencing for the cache lines. For set 0, the cache lines are numbered $0, 1, \dots, k - 1$. Now for set 1, the cache lines are numbered $k, k + 1, \dots, k + k - 1$ and so on.

So, main memory block j will be mapped to set $(j \bmod v)$, which will be any one of the cache lines from $(j \bmod v) * k$ to $(j \bmod v) * k + (k - 1)$.

(Associativity plays no role in mapping- k -way associativity means there are k spaces for a block and hence reduces the chances of replacement.)

Correct Answer: A

80 votes

-- Arjun Suresh (332k points)

1.2.34 Cache Memory: GATE CSE 2014 Set 1 | Question: 44 [top](#)

<https://gateoverflow.in/1922>



✓ There are N accesses to cache.

Out of these n are unique block addresses.

Now, we need to find the number of misses. (min. n misses are guaranteed whatever be the access sequence due to n unique block addresses).

We are given that between two consecutive accesses to the same block, there can be only k unique block addresses. So, for a block to get replaced we can assume that all the next k block addresses goes to the same set (given cache is set-associative) which will be the worst case scenario (they may also go to a different set but then there is lesser chance of a replacement). Now, if associativity size is $\geq k$, and if we use LRU (Least Recently Used) replacement policy, we can guarantee that these k accesses won't throw out our previously accessed cache entry (for that we need at least k accesses). So, this means we are at the best-cache scenario for cache replacement -- out of N accesses we miss only n (which are unique and can not be helped from getting missed and there is no block replacement in cache). So, miss ratio is n/N .

PS: In question it is given "bounded above by k ", which should mean k unique block accesses as k is an integer, but to ensure no replacement this must be ' $k - 1$ '. Guess, a mistake in question.

Correct Answer: A

122 votes

-- Arjun Suresh (332k points)

1.2.35 Cache Memory: GATE CSE 2014 Set 2 | Question: 43 [top](#)

<https://gateoverflow.in/2009>



✓
A. A smaller block size means during a memory access only a smaller part of near by addresses are brought to cache-

meaning spatial locality is reduced.

- B. A smaller block size means more number of blocks (assuming cache size constant) and hence index bits go up and offset bits go down. But the tag bits remain the same.
- C. A smaller block size implying larger cache tag is true, but this can't lower cache hit time in any way.
- D. A smaller block size incurs a lower cache miss penalty. This is because during a cache miss, an entire cache block is fetched from next lower level of memory. So, a smaller block size means only a smaller amount of data needs to be fetched and hence reduces the miss penalty (Cache block size can go til the size of data bus to the next level of memory, and beyond this only increasing the cache block size increases the cache miss penalty).

Correct Answer: *D*

👍 111 votes

-- Arjun Suresh (332k points)

1.2.36 Cache Memory: GATE CSE 2014 Set 2 | Question: 44 top

<https://gateoverflow.in/2010>



- ✓ If associativity is doubled, keeping the capacity and block size constant, then the number of sets gets halved. So, width of set index decoder can surely decrease - **(B)** is false.
Width of way-selection multiplexer must be increased as we have to double the ways to choose from- **(C)** is false

As the number of sets gets decreased, the number of possible cache block entries that a set maps to gets increased. So, we need more tag bits to identify the correct entry. So, **(A)** is also false.

(D) is the correct answer- main memory data bus has nothing to do with cache associativity- this can be answered without even looking at other options.

👍 51 votes

-- Arjun Suresh (332k points)

1.2.37 Cache Memory: GATE CSE 2014 Set 2 | Question: 9 top

<https://gateoverflow.in/1963>



- ✓ Number of sets = $\frac{\text{cache size}}{\text{size of a set}}$

Size of a set = blocksize \times no. of blocks in a set
= 8 words \times 4 (4-way set-associative)
= $8 \times 4 \times 4$ (since a word is 32 bits = 4 bytes)
= 128 bytes.

So, number of sets = $\frac{16 \text{ KB}}{(128 \text{ B})} = 128$

Now, we can divide the physical address space equally between these 128 sets.

So, the number of bytes each set can access

$$= \frac{4 \text{ GB}}{128}$$

= 32 MB

$$= \frac{32}{4} = 8 \text{ M words} = 1 \text{ M blocks. } (2^{20} \text{ blocks})$$

So, we need 20 tag bits to identify these 2^{20} blocks.

👍 47 votes

-- Arjun Suresh (332k points)

1.2.38 Cache Memory: GATE CSE 2014 Set 3 | Question: 44 top

<https://gateoverflow.in/2078>



- ✓ The question is to find the time taken for,

$$\frac{100 \text{ fetch operations and } 60 \text{ operand read operations and } 40 \text{ memory operand write operations}}{\text{total number of instructions}}$$

Total number of instructions = $100 + 60 + 40 = 200$

Time taken for 100 fetch operations(fetch = read) = $100 * ((0.9 * 1) + (0.1 * 5))$

1 corresponds to time taken for read when there is cache hit = 140 ns

0.9 is cache hit rate

Time taken for 60 read operations,

$$= 60 * ((0.9 * 1) + (0.1 * 5)) \\ = 84 \text{ ns}$$

Time taken for 40 write operations

$$= 40 * ((0.9 * 2) + (0.1 * 10)) \\ = 112 \text{ ns}$$

Here, 2 and 10 are the times taken for write when there is cache hit and no cache hit respectively.

So, the total time taken for 200 operations is,

$$= 140 + 84 + 112 \\ = 336 \text{ ns}$$

Average time taken = time taken per operation

$$= \frac{336}{200} \\ = 1.68 \text{ ns}$$

👍 52 votes

-- Divya Bharti (8.8k points)

Fetch is also a memory read operation.

$$\text{Avg access time} = \frac{160(0.9 \times 1 + 0.1 \times 5) + 40(0.9 \times 2 + 0.1 \times 10)}{200} = \frac{160 \times 1.4 + 40 \times 2.8}{200} = \frac{336}{200} = 1.68$$

👍 32 votes

-- aravind90 (389 points)

1.2.39 Cache Memory: GATE CSE 2015 Set 2 | Question: 24 top

<https://gateoverflow.in/8119>



✓ Answer is: $14 \text{ ns} = 0.8(5) + 0.2(50)$

PS: Here instead of cache and main memory access times, time taken on a cache hit and miss are directly given in question. So,

$$\text{Average Access Time} = \text{Hit Rate} \times \text{Hit Time} + \text{Miss Rate} \times \text{Miss Time}$$

👍 48 votes

-- Vikrant Singh (11.2k points)

1.2.40 Cache Memory: GATE CSE 2015 Set 3 | Question: 14 top

<https://gateoverflow.in/39622>



✓ Block size of 16 bytes means we need 4 offset bits. (The lowest 4 digits of memory address are offset bits)

Number of sets in cache (cache lines) = 2^{12} so the next lower 12 bits are used for set indexing.

The top 4 bits (out of 20) are tag bits.

So, answer is A.

👍 37 votes

-- Arjun Suresh (332k points)

1.2.41 Cache Memory: GATE CSE 2016 Set 2 | Question: 32 top

<https://gateoverflow.in/39622>



✓ Physical Address = 40

- Tag + Set + Block Offset = 40
- $T + S + B = 40 \rightarrow (1)$

We have: Cache Size = number of sets \times blocks per set \times Block size

- $512 \text{ KB} = \text{number of sets} \times 8 \times \text{Block size}$
- Number of sets \times Block size = $\frac{512}{8} \text{ KB} = 64 \text{ KB}$
- $S + B = 16 \rightarrow (2)$

From (1), (2)

$T = 24$ bits (Ans)

Second way :

Cache Size = 2^{19}

MM size = 2^{40}

This means, We need to map $\frac{2^{40}}{2^{19}} = 2^{21}$ Blocks to one line. And a set contain 2^3 lines.

Therefore, 2^{24} blocks are mapped to one set.

Using Tag field, I need to identify which one block out of 2^{24} blocks are present in this set.

Hence, 24 bits are needed in Tag field.

👍 94 votes

-- Himanshu Agarwal (12.4k points)

In question block size has not been given,so we can assume block size 2^x Byte.

$$\text{Number of Blocks:- } \frac{512 \times 2^{10}}{2^x} = 2^{19-x}$$

$$\text{Number of sets:- } \frac{2^{19-x}}{8} = 2^{16-x}$$

So number of bits for sets = $16 - x$

Let number of bits for Tag = T

And we have already assumed block size 2^x Byte,therefore number of bits for block size is x

And finally,

$$T + (16 - x) + x = 40$$

$$T + 16 = 40$$

$$T = 24.$$

👍 54 votes

-- ajit (2.5k points)

1.2.42 Cache Memory: GATE CSE 2016 Set 2 | Question: 50 top

<https://gateoverflow.in/39592>



✓ Look aside Cache Latency = 1ms

Main Memory Latency = 10ms

- Lets try with 20 MB

Miss rate = 60% , Hit rate = 40%

$$\text{Avg} = 0.4(1) + 0.6(10)$$

$$= 0.4 + 6 = 6.4 \text{ ms} > 6 \text{ ms}$$

- Next Take 30 MB

Miss rate = 40% , Hit rate = 60%

$$\text{Avg} = 0.6(1) + 0.4(10)$$

$$= 0.6 + 4 = 4.6 \text{ ms} < 6 \text{ ms}$$

So answer is 30 MB

64 votes

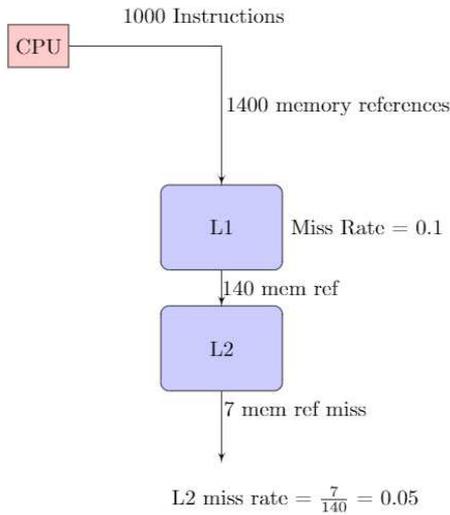
-- Akash Kanase (36k points)

1.2.43 Cache Memory: GATE CSE 2017 Set 1 | Question: 25

<https://gateoverflow.in/118305>



✓ Answer = 0.05.



169 votes

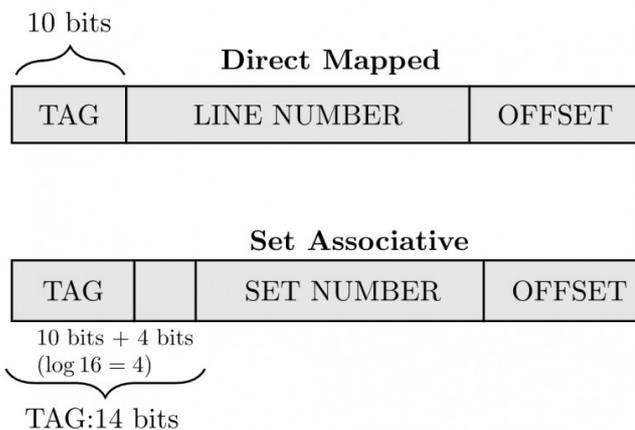
-- Debashish Deka (40.8k points)

1.2.44 Cache Memory: GATE CSE 2017 Set 1 | Question: 54

<https://gateoverflow.in/118748>



✓



In set-associative 1 set = 16 lines. So the number of index bits will be 4 less than the direct mapped case. So, Tag bits increased to 14 bits.

65 votes

-- Ahwan Mishra (10.2k points)

1.2.45 Cache Memory: GATE CSE 2017 Set 2 | Question: 29

<https://gateoverflow.in/118371>



✓ In two-level memory system (hierarchical), it is clear that the second level is accessed only when first level access is a miss. So, we must include the first level access time in all the memory access calculations. Continuing this way for any level, we must include that level access time (without worrying about the hit rate in that level), to all memory accesses coming to that level (i.e., by just considering the miss rate in the previous level). So, for the given question, we can get the following equation:

$$\text{AMAT} = \text{L1 access time}$$

+L1 miss rate \times L2 access time
 +L1 miss rate \times L2 miss rate \times Main memory access time

$$2 = 1 + x \times 8 + 0.5x^2 \times 18$$

$$\Rightarrow 9x^2 + 8x - 1 = 0$$

$$\Rightarrow x = \frac{-8 \pm \sqrt{64 + 36}}{18} = \frac{2}{18} = 0.111.$$

So, Answer is option (A).

👍 79 votes

-- Arjun Suresh (332k points)

1.2.46 Cache Memory: GATE CSE 2017 Set 2 | Question: 45 top

<https://gateoverflow.in/118597>



✓ L2 cache is shared between Instruction and Data (is it always?, see below)

So, average read time

= Fraction of Instruction Fetch \times Average Instruction fetch time + Fraction of Data Fetch \times Average Data Fetch Time

Average Instruction fetch Time = L1 access time + L1 miss rate \times L2 access time + L1 miss rate \times L2 miss rate \times Memory access time

$$= 2 + 0.2 \times 8 + 0.2 \times 0.1 \times 90$$

$$= 5.4 \text{ ns}$$

Average Data fetch Time = L1 access time + L1 miss rate \times L2 access time + L1 miss rate \times L2 miss rate \times Memory access time

$$= 2 + 0.1 \times 8 + 0.1 \times 0.1 \times 90$$

$$= 3.7 \text{ ns}$$

So, average memory access time

$$= 0.6 \times 5.4 + 0.4 \times 3.7 = 4.72 \text{ ns}$$

Now, why L2 must be shared? Because we can otherwise use it for either Instruction or Data and it is not logical to use it for only 1. Ideally this should have been mentioned in question, but this can be safely assumed also (not enough merit for Marks to All). Some more points in the question:

Assume that the caches use the referred-word-first read policy and the writeback policy

Writeback policy is irrelevant for solving the given question as we do not care for writes. Referred-word-first read policy means there is no extra time required to get the requested word from the fetched cache line.

Assume that all the caches are direct mapped caches.

Not really relevant as average access times are given

Assume that the dirty bit is always 0 for all the blocks in the caches

Dirty bits are for cache replacement- which is not asked in the given question. But this can mean that there is no more delay when there is a read miss in the cache leading to a possible cache line replacement. (In a write-back cache when a cache line is replaced, if it is dirty then it must be written back to main memory).

👍 96 votes

-- Arjun Suresh (332k points)

1.2.47 Cache Memory: GATE CSE 2017 Set 2 | Question: 53 top

<https://gateoverflow.in/118613>



✓ No. of blocks of main Memory = $\frac{2^{32}}{2^5} = 2^{27}$

And there are $512 = 2^9$ lines in Cache Memory.

Tag bits tell us to how many blocks does 1 line in Cache memory points to

$$1 \text{ cache line points to } \frac{2^{27}}{2^9} = 2^{18} \text{ lines}$$

So, 18 bits are required as TAG bits.

👍 48 votes

-- Manish Joshi (20.5k points)

1.2.48 Cache Memory: GATE CSE 2018 | Question: 34 top

<https://gateoverflow.in/204108>



- ✓ Physical Address Space = 2^P Bytes i.e. P bits to represent size of total memory.
Cache Size = 2^N Byte i.e., N bits to represent Cache memory.
Tag size = 2^X Bytes i.e., X bits to represent Tag.
Cache is K -way associative.

$$(\text{Size of Tag}) \times \frac{\text{Cache Size}}{K} = \text{Total Memory Size}$$

$$\Rightarrow 2^X \times \frac{2^N}{K} = 2^P$$

$$\Rightarrow 2^{X+N-\log(K)} = 2^P$$

$$\Rightarrow 2^X = 2^{P-N+\log(K)}$$

$$\Rightarrow X(\text{Size of Tag in bits}) = P - N + \log(K)$$

Correct Answer: B

👍 34 votes

-- Digvijay (44.9k points)

1.2.49 Cache Memory: GATE CSE 2019 | Question: 1 top

<https://gateoverflow.in/302847>



- ✓ Given that cache is Fully Associative.

Tag Bits	Block Offset
28	4

There are no index bits in fully associative cache because every main memory block can go to any location in the cache
 \Rightarrow Index bits = 0.

Given that memory is byte addressable and uses 32-bit address.

Cache Block size is 16 Bytes \Rightarrow Number of bits required for Block Offset = $\lceil \log_2 16 \rceil = 4$ bits

\therefore Number of Tag bits = $32 - 4 = 28$.

Answer is (D).

👍 50 votes

-- Shaik Masthan (50.4k points)

1.2.50 Cache Memory: GATE CSE 2019 | Question: 45 top

<https://gateoverflow.in/302803>



- ✓ Time to transfer a cache block = $1 + 3 + 8 = 12$ cycles.

i.e., 4 bytes $\times 8 = 32$ bytes in 12 cycles.

$$\text{So, memory bandwidth} = \frac{32}{12 \text{ cycle time}} = \frac{32}{12/(60 \times 10^6)} = 160 \times 10^6 \text{ bytes/s}$$

👍 44 votes

-- Arjun Suresh (332k points)

Answer : $160 \times 10^6 \frac{\text{Bytes}}{\text{sec}}$

Explanation :

Given frequency = 60 MHz

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This means that the processor completes 60×10^6 cycles in 1 second.

∴ One cycle is completed in $\frac{1}{60 \times 10^6}$ seconds

Now,

To service a cache miss, number of cycles needed

= 1 cycle (to accept starting address of the block) + 3 cycles (to fetch all the 8 words of the blocks) + $\frac{8 \times 1}{1}$ cycles (to
∴ 1 word per cycle

Note : Total data is the data which is used for transmitting the words of the requested block at the rate of 1 word per cycle
= 8 words × 4 Byte (Size of each word)

$$\begin{aligned}\therefore \text{Bandwidth} &= \frac{\text{Total Data}}{12 \text{ cycle time}} \\ &= \frac{8 \times 4 \text{ Bytes}}{12 \text{ cycles} \times 1 \text{ cycle time}} \\ &= \frac{32}{12 \times \frac{1}{60 \times 10^6}} \\ &= \frac{32 \times 60^5 \times 10^6}{12^1} \\ &= 5 \times 32 \times 10^6 \\ &= 160 \times 10^6 \frac{\text{Bytes}}{\text{sec}}\end{aligned}$$

∴ $160 \times 10^6 \frac{\text{Bytes}}{\text{sec}}$ is the correct answer.

👍 16 votes

-- Jeet (15.3k points)

1.2.51 Cache Memory: GATE CSE 2020 | Question: 21 top ⤴

https://gateoverflow.in/333210



✓ Block size is 256 Bytes, word size is 64 bits or 8 bytes. So Block size in words is 8 words.

Number of words per block=32

Time to fetch a word from main-memory to cache is: $20 + 31 \times 5 = 175$ ns because first word takes 20ns and rest each subsequent words take 5ns each.

So average Memory access time is

$$0.94(3) + 0.06(3 + 175) = 13.5 \text{ ns}$$

👍 23 votes

-- Ayush Upadhyaya (28.4k points)

1.2.52 Cache Memory: GATE CSE 2020 | Question: 30 top ⤴

https://gateoverflow.in/333201



✓ Block size is 256 Bytes. Number of sets in cache = 2^6 so Set offset bits=6 and word offset bits=8.

So check for set, check for the rightmost 4 digits of each physical address. (Last two byte denote the word address)

$$A1=C8A4 = C8 = 11001000$$

$$A2=6888 = 68 = 01101000$$

$$A3=289C = 28 = 00101000$$

$$A4=4880 = 48 = 01001000$$

Now look for lowest order 6 bits in the highlighted part of Each physical address (corresponds to set number).

8 and 8 match and 6=0110 and 2=0010 two low order bits of 6 and 2 match, So A2 and A3 go to same set.

So answer-B

16 votes

-- Ayush Upadhyaya (28.4k points)

1.2.53 Cache Memory: GATE CSE 2021 Set 1 | Question: 22

<https://gateoverflow.in/357429>



✓ Tag bits = $PAS_{bits} - \log_2(\text{Cache Size}) + \log_2(K)$ (where K is associativity)

$$= 32 - 15 + 0 = 17 \text{ bits}$$

5 votes

-- Nikhil Dhama (2.5k points)

1.2.54 Cache Memory: GATE CSE 2021 Set 2 | Question: 19

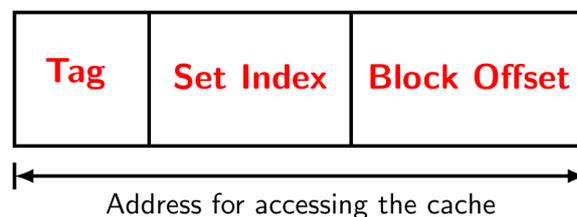
<https://gateoverflow.in/357521>



✓ 32 bit address is used for accessing the cache.

It is given that cache is Set-Associative.

The address bits get split as follows:



Block Size = $64B \implies$ Block offset = 6 bits.

Given that Tag field width = 22 bits.

Therefore, width of Set Index field = $32 - 22 - 6 = 4 \implies 2^4 = 16$ sets in the cache.

Cache size is $2KB$ and Block size = $64B \implies 2^5 = 32$ blocks present in the cache.

16 sets contain 32 blocks \implies 2 blocks per set or associativity = 2.

Correct Answer: 2

5 votes

-- Shaik Masthan (50.4k points)

1.2.55 Cache Memory: GATE CSE 2021 Set 2 | Question: 27

<https://gateoverflow.in/357513>



✓ S_1 : Read Miss in a write through $L1$ cache results in read allocate. **No write back** is done here, as in a write through $L1$ cache, both $L1$ and $L2$ caches are updated during a write operation (no dirty blocks and hence no dirty bits as in a write back cache). So during a Read miss it will simply bring in the missed block from $L2$ to $L1$ which may replace one block in $L1$ (this replaced block in $L1$ is already updated in $L2$ and so needs no write back). So, S_1 is TRUE.

S_2 : This statement is FALSE. Both write-through and write-back policies can use either of these write-miss policies, but usually they are paired in this way.

- No write allocation during write through as $L1$ and $L2$ are accessed for each write operation (subsequent writes to same location gives no advantage even if the location is in $L1$ cache).
- In write back we can do write allocate in $L1$ after a write operation hoping for subsequent writes to the same location which will then hit in $L1$ and thus avoiding a more expensive $L2$ access.

Correct Answer: A.

[Cache Writing Policies](#)

References



👍 1 votes

-- Arjun Suresh (332k points)

1.2.56 Cache Memory: GATE IT 2004 | Question: 12, ISRO2016-77 [top](#)

<https://gateoverflow.in/3653>



- ✓ By default we consider hierarchical access - because that is the common implementation and simultaneous access cache has great practical difficulty. But here the question is a bit ambiguous -- it says to ignore search time within the cache - usually search is applicable for an associative cache but here no such information given. So, may be they are telling to ignore the search time for $L1$ and just consider the time for $L2$ for an $L1$ miss and similarly just consider memory access time for $L2$ miss. This is nothing but simultaneous access.

Access time for hierarchical access,

$$\begin{aligned} &= t_1 + (1 - h_1) \times t_2 + (1 - h_1)(1 - h_2)t_m \\ &= 1 + 0.2 \times 10 + 0.2 \times 0.1 \times 500 \\ &= 13ns. \end{aligned}$$

Access time for simultaneous access,

$$\begin{aligned} &= h_1 \times t_1 + (1 - h_1)h_2 \times t_2 + (1 - h_1)(1 - h_2)t_m \\ &= 0.8 + 0.2 \times 0.9 \times 10 + 0.2 \times 0.1 \times 500 \\ &= 12.6ns. \end{aligned}$$

Both options in choice.

👍 70 votes

-- Arjun Suresh (332k points)

1.2.57 Cache Memory: GATE IT 2004 | Question: 48 [top](#)

<https://gateoverflow.in/3691>



- ✓ When 45 comes, the cache contents are:
4 3 25 8 19 6 16 35

LRU array (first element being least recently used)

[4 3 19 6 25 8 16 35].

So, 45 replaces 4.

45 3 25 8 19 6 16 35 [3 19 6 25 8 16 35 45]

Similarly, 22 replaces 3 to give:

45 22 25 8 19 6 16 35 [19 6 25 8 16 35 45 22]

8 hits in cache.

45 22 25 8 19 6 16 35 [19 6 25 16 35 45 22 8]

3 replaces 19

45 22 25 8 3 6 16 35 [6 25 16 35 45 22 8 3]

16 and 25 hits in cache.

45 22 25 8 3 6 16 35 [6 35 45 22 8 3 16 25]

Finally, 7 replaces 6, which is in block 5.

So, answer is **(B)**.

👍 34 votes

-- Arjun Suresh (332k points)

1.2.58 Cache Memory: GATE IT 2005 | Question: 61 [top](#)

<https://gateoverflow.in/3822>



- ✓ 128 main memory blocks are mapped to 4 sets in cache. So, each set maps 32 blocks each. And in each set there is place for two blocks (2-way set).

Now, we have 4 sets meaning 2 index bits. Also, 32 blocks going to one set means 5 tag bits.

Now, these 7 bits identify a memory block and tag bits are placed before index bits. (otherwise adjacent memory references- spatial locality- will hamper cache performance)

So, based on the two index bits (lower 2 bits) blocks will be going to sets as follows:

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Set Number	Block Numbers
0	0, 16
1	5, 9
2	
3	3, 7, 55

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Since, each set has only 2 places, 3 will be thrown out as it is the least recently used block. So, final content of cache will be

0 5 7 9 16 55

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(C) choice.

👍 46 votes

-- Arjun Suresh (332k points)

1.2.59 Cache Memory: GATE IT 2006 | Question: 42 top

<https://gateoverflow.in/3585>



✓ Answer is C.

For 1 sec it is 10^9 bytes (Note - by looking at the options, it can be decided that 1GB should be considered as 10^9 , but not as 2^{30} , and in general, if bandwidth is given, then we consider 1 Giga = 10^9)

So, for 64 bytes?

It is $\frac{64 \times 1}{10^9}$ so it is 64 ns but mm latency is 32.

So, total time required to place cache line is $64 + 32 = 96$ ns.

👍 57 votes

-- K Rajashekar (997 points)

1.2.60 Cache Memory: GATE IT 2006 | Question: 43 top

<https://gateoverflow.in/3586>



✓ 1. I-cache

- Number of blocks in cache = $\frac{4K}{4} = 2^{10}$ blocks.
- Bits to represent blocks = 10
- Number of words in a block = $4 = 2^2$ words.
- Bits to represent words = 2.
- tag bits = $30 - (10 + 2) = 18$.
- Each block will have its own tag bits. So total tag bits = $1K \times 18$ bits.

2. D-cache

- Number of blocks in cache = $\frac{4K}{4} = 2^{10}$ blocks.
- Number of sets in cache = $\frac{2^{10}}{2} = 2^9$ sets.
- Bits to represent sets = 9.
- Number of words in a block = $4 = 2^2$ words.
- Bits to represent words = 2
- tag bits = $30 - (9 + 2) = 19$
- Each block will have its own tag bits. So total tag bits = $1K \times 19$ bits.

3. L2 cache

- Number of blocks in cache = $\frac{64K}{16} = 2^{12}$ blocks.
- Number of sets in cache = $\frac{2^{12}}{4} = 1024$ sets.
- Bits to represent sets = 10

- Number of words in cache = $16 = 2^4$ words.
- Bits to represent words = 4.
- tag bits = $30 - (10 + 4) = 16$
- Each block will have its own tag bits. So total tag bits = $2^{12} \times 16\text{-bits} = 4K \times 16\text{-bits}$.

Option (A).

👍 38 votes

-- Viral Kapoor (1.9k points)

1.2.61 Cache Memory: GATE IT 2007 | Question: 37 [top](#)

<https://gateoverflow.in/3470>



✓ Answer is **(B)**.

Cache location (memory block) = block req mod number of cache blocks. Since each block has only one location (associativity is 1) the last mod 8 request will be in cache (no need of any replacement policy as mapping is direct).

3, 5, 2, 8, 0, 63, 9, 16, 20, 17, 25, 18, 30, 24, 2, 63, 5, 82, 17, 24

Block 0 – 8, 0, 16, 24, 24. At end contains 24.

1- 9, 17, 25, 17.

2- 2, 18, 2, 82.

3- 3.

4- 20.

5- 5, 5.

6- 30.

7- 6363.

So, memory block 18 is not in cache while 3, 20 and 30 are in cache.

👍 23 votes

-- K Rajashekar (997 points)

1.2.62 Cache Memory: GATE IT 2008 | Question: 80 [top](#)

<https://gateoverflow.in/3403>



✓ Number of cache blocks = $\frac{8KB}{(128 \times 1)} = 64$

Number of sets in cache = $\frac{\text{Number of cache blocks}}{4 \text{ (4-way set)}} = \frac{64}{4} = 16$

So, number of SET bits required = 4 (as $2^4 = 16$, and with 4 bits we can get 16 possible outputs)

We can now straight away choose (D) as answer but for confirmation can proceed further.

Since, only physical memory information is given we can assume cache is physically tagged (which is anyway the common case even in case of virtual memory).

So, we can divide the physical memory into 16 regions so that, each set maps into only its assigned region.

So, size of a region a set can address = $\frac{1MB}{16} = 2^{16}$ Bytes = $\frac{2^{16}}{128} = 2^9$ cache blocks (as cache block size is 128 words = 128 bytes).

So, when an access comes to a cache entry, it must be able to determine which out of the 2^9 possible physical block it is. In short, it needs 9 bits for TAG.

Now, cache block size is 128 words and so to identify a word we need 7 bits for WORD.

👍 26 votes

-- Arjun Suresh (332k points)

1.2.63 Cache Memory: GATE IT 2008 | Question: 81 [top](#)

<https://gateoverflow.in/3405>



✓ As shown in https://gateoverflow.in/3403/gate2008-it_80

We have 16 sets in cache and correspondingly 16 regions in physical memory to which each set is mapped. Now, WORD bit size is 7 as we need 7 bits to address 128 possible words in a cache block.

So, the lowest 7 bits of 0C795H will be used for this giving us the remaining bits as 0000 1100 0111 1

Of these bits, the lower 4 are used for addressing the 16 possible sets, giving us the tag bits: 0000 1100 0 in **(A) choice**.

References



20 votes

-- Arjun Suresh (332k points)

1.3

Cisc Risc Architecture (2) top

1.3.1 Cisc Risc Architecture: GATE CSE 1999 | Question: 2.22 top

<https://gateoverflow.in/1499>



The main difference(s) between a CISC and a RISC processor is/are that a RISC processor typically

- A. has fewer instructions
- B. has fewer addressing modes
- C. has more registers
- D. is easier to implement using hard-wired logic

gate1999 co-and-architecture normal cisc-risc-architecture multiple-selects

Answer

1.3.2 Cisc Risc Architecture: GATE CSE 2018 | Question: 5 top

<https://gateoverflow.in/204079>



Consider the following processor design characteristics:

- I. Register-to-register arithmetic operations only
- II. Fixed-length instruction format
- III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

- A. I and II only
- B. II and III only
- C. I and III only
- D. I, II and III

gate2018-cse co-and-architecture cisc-risc-architecture easy

Answer

Answers: Cisc Risc Architecture

1.3.1 Cisc Risc Architecture: GATE CSE 1999 | Question: 2.22 top

<https://gateoverflow.in/1499>



✓ All are properties of the RISC processor.

- <http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/whatis/index.html>
- <http://cs.stanford.edu/people/eroberts/courses/soco/projects/risc/riscisc/index.html>
- http://homepage3.nifty.com/alpha-1/computer/Control_E.html

References



26 votes

-- Digvijay (44.9k points)



✓ (D) All of these

Hardwired control units are implemented through use of combinational logic units, featuring a finite number of gates that can generate specific results based on the instructions that were used to invoke those responses. Their design uses a **fixed architecture**—it requires changes in the wiring if the instruction set is modified or changed. This architecture is **preferred in reduced instruction set computers (RISC)** as they use a simpler instruction set.

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Instructions length cannot vary in RISC usually it's 32 bit. For CISC it can be between 16 to 64 bits.

The hardwired control unit is used when instructions are fixed.

Register to register operations is always possible in RISC. CISC can have memory to memory instructions also.

References: <https://www-cs-faculty.stanford.edu/~eroberts/courses/soco/projects/2000-01/risc/riscisc/>

https://en.wikipedia.org/wiki/Control_unit#Hardwired_control_unit

References



👍 26 votes

-- Subham Mishra (11.4k points)

1.4

Clock Frequency (2) top

1.4.1 Clock Frequency: GATE CSE 1992 | Question: 01-iii top

https://gateoverflow.in/547



Many microprocessors have a specified lower limit on clock frequency (apart from the maximum clock frequency limit) because _____

gate1992 normal co-and-architecture clock-frequency fill-in-the-blanks

Answer

1.4.2 Clock Frequency: GATE IT 2007 | Question: 36 top

https://gateoverflow.in/3469



The floating point unit of a processor using a design D takes $2t$ cycles compared to t cycles taken by the fixed point unit. There are two more design suggestions D_1 and D_2 . D_1 uses 30% more cycles for fixed point unit but 30% less cycles for floating point unit as compared to design D . D_2 uses 40% less cycles for fixed point unit but 10% more cycles for floating point unit as compared to design D . For a given program which has 80% fixed point operations and 20% floating point operations, which of the following ordering reflects the relative performances of three designs? ($D_i > D_j$ denotes that D_i is faster than D_j)

- A. $D_1 > D > D_2$
- B. $D_2 > D > D_1$
- C. $D > D_2 > D_1$
- D. $D > D_1 > D_2$

gate2007-it co-and-architecture normal clock-frequency

aoclasses.in

tests.gatecse.in

Answer

Answers: Clock Frequency

1.4.1 Clock Frequency: GATE CSE 1992 | Question: 01-iii top

https://gateoverflow.in/547



✓ Clock frequency becomes low means time period of clock becomes high. When this time period increases beyond the time period in which the volatile memory contents must be refreshed, we lose those contents. So, clock frequency can't go

below this value.

Reference: <https://gateoverflow.in/261/microprocessors-specified-frequency-frequency->

References



26 votes

-- Rajarshi Sarkar (27.9k points)

1.4.2 Clock Frequency: GATE IT 2007 | Question: 36 top

<https://gateoverflow.in/3469>



✓ (B) is correct.

$$T = 0.8 \times \text{time taken in fixed point} + 0.2 \times \text{time taken in floating point}$$

$$D = 0.8 \times t + 0.2 \times 2t = 1.2t$$

$$D_1 = 0.8 \times 1.3t + 0.2 \times 0.7 \times 2t = 1.04t + .28t = 1.32t$$

$$D_2 = 0.8 \times 0.6t + 0.2 \times 1.1 \times 2t = 0.48t + .44t = 0.92t$$

So, D_2 is the best design for this given program followed by D and then D_1 . Option B.

45 votes

-- Vicky Bajoria (4.1k points)

1.5

Conflict Misses (1) top

1.5.1 Conflict Misses: GATE CSE 2017 Set 1 | Question: 51 top

<https://gateoverflow.in/118745>



Consider a 2-way set associative cache with 256 blocks and uses *LRU* replacement. Initially the cache is empty. Conflict misses are those misses which occur due to the contention of multiple blocks for the same cache set. Compulsory misses occur due to first time access to the block. The following sequence of access to memory blocks :

$\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$

is repeated 10 times. The number of *conflict misses* experienced by the cache is _____ .

gate2017-cse-set1 co-and-architecture cache-memory conflict-misses normal numerical-answers

Answer

Answers: Conflict Misses

1.5.1 Conflict Misses: GATE CSE 2017 Set 1 | Question: 51 top

<https://gateoverflow.in/118745>



✓ $\{0, 128, 256, 128, 0, 128, 256, 128, 1, 129, 257, 129, 1, 129, 257, 129\}$

1st Iteration:

For $\{0, 128, 256, 128, 0, 128, 256, 128\}$

Block ID	Type	Set 0 content
0	Compulsory Miss	0
128	Compulsory Miss	0 128
256	Compulsory Miss	128 256
128	Hit	256 128
0	Conflict miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128

Total number of conflict misses = 2;

Similarly for $\{1, 129, 257, 129, 1, 129, 257, 129\}$, total number of conflict misses in $set1 = 2$

Total number of conflict misses in 1^{st} iteration = $2 + 2 = 4$

2^{nd} iteration:

for $\{0, 128, 256, 128, 0, 128, 256, 128\}$

Block ID	Type	Set 0 content
0	Conflict Miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128
0	Conflict miss	128 0
128	Hit	0 128
256	Conflict miss	128 256
128	Hit	256 128

Total number of conflict misses = 4.

Similarly for $\{1, 129, 257, 129, 1, 129, 257, 129\}$, total number of conflict misses in $set1 = 4$

Total Number of conflict misses in 2^{nd} iteration = $4 + 4 = 8$

Note that content of each set is same, before and after 2^{nd} iteration. Therefore each of the remaining iterations will also have 8 conflict misses.

Therefore, overall conflict misses = $4 + 8 * 9 = 76$

👍 104 votes

-- suraj (4.8k points)

1.6

Control Unit (1) [top](#)

1.6.1 Control Unit: GATE CSE 1987 | Question: 1-vi [top](#)

<https://gateoverflow.in/80199>



A microprogrammed control unit

- A. Is faster than a hard-wired control unit.
- B. Facilitates easy implementation of new instruction.
- C. Is useful when very small programs are to be run.
- D. Usually refers to the control unit of a microprocessor.

gate1987 co-and-architecture control-unit microprogramming

Answer [👤](#)



- A. is wrong. Microprogrammed Control Unit (CU) can never be faster than hardwired CU. Microprogrammed CU it has an extra layer on top of hardwired CU and hence can only be slower than hardwired CU.
- B. is a suitable answer as we can add new instruction by changing the content of control memory.
- C. is not correct as when only small programs are there, hardwired control makes more sense.
- D. control unit can also be hardwired, so this is also not correct.

Reference: [Slides](#)

Correct Answer: *B*

References

[gateoverflow.in](#)[gateoverflow.in](#)[classroom.gateover](#)

27 votes

-- Arjun Suresh (332k points)



Consider the following code sequence having five instructions from I_1 to I_5 . Each of these instructions has the following format.

OP Ri, Rj, Rk

Where operation OP is performed on contents of registers Rj and Rk and the result is stored in register Ri.

I_1 : ADD R1, R2, R3

I_2 : MUL R7, R1, R3

I_3 : SUB R4, R1, R5

I_4 : ADD R3, R2, R4

I_5 : MUL R7, R8, R9

Consider the following three statements.

S1: There is an anti-dependence between instructions I_2 and I_5

S2: There is an anti-dependence between instructions I_2 and I_4

S3: Within an instruction pipeline an anti-dependence always creates one or more stalls

Which one of the above statements is/are correct?

- A. Only S1 is true
 B. Only S2 is true
 C. Only S1 and S3 are true
 D. Only S2 and S3 are true

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Answer



Data forwarding techniques can be used to speed up the operation in presence of data dependencies. Consider the following replacements of LHS with RHS.

- i. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2, R1 \rightarrow Loc$
- ii. $R1 \rightarrow Loc, Loc \rightarrow R2 \equiv R1 \rightarrow R2$
- iii. $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R1 \rightarrow Loc$
- iv. $R1 \rightarrow Loc, R2 \rightarrow Loc \equiv R2 \rightarrow Loc$

In which of the following options, will the result of executing the RHS be the same as executing the LHS irrespective of the instructions that follow ?

- A. i and iii
- B. i and iv
- C. ii and iii
- D. ii and iv

gate2007-it data-dependences co-and-architecture

Answer

Answers: Data Dependences

1.7.1 Data Dependences: GATE CSE 2015 Set 3 | Question: 47 [top](#)

<https://gateoverflow.in/8556>



✓ Answer should be **(B)**.

Anti-dependence can be overcome in pipeline using register renaming. So, "always" in S3 makes it false. Also, if I_2 is completed before I_4 (execution stage of MUL), then also there won't be any stall.

👍 55 votes

-- ppm (543 points)

1.7.2 Data Dependences: GATE IT 2007 | Question: 39 [top](#)

<https://gateoverflow.in/3472>



✓

- i. is true. Both LOC and $R2$ are getting the value of $R1$ in LHS and RHS .
- ii. false, because $R2$ gets the correct data in both LHS and RHS , but LOC is not updated in RHS .
- iii. is wrong because $R2$ is writing last, not $R1$ in LHS , but not in RHS .
- iv. is true. The first write to LOC in LHS is useless as it is overwritten by the next write.

So, answer is **(B)**.

👍 38 votes

-- Vicky Bajoria (4.1k points)

1.8

Data Path (6) [top](#)

1.8.1 Data Path: GATE CSE 1990 | Question: 8a [top](#)

<https://gateoverflow.in/8569>



A single bus CPU consists of four general purpose register, namely, R_0, \dots, R_3 , ALU, MAR, MDR, PC, SP and IR (Instruction Register). Assuming suitable microinstructions, write a microroutine for the instruction, ADD R_0, R_1 .

gate1990 descriptive co-and-architecture data-path

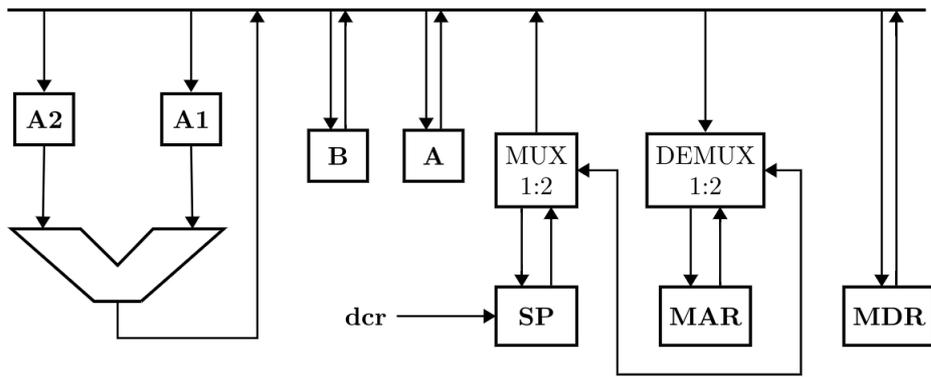
Answer

1.8.2 Data Path: GATE CSE 2001 | Question: 2.13 [top](#)

<https://gateoverflow.in/731>



Consider the following data path of a simple non-pipelined CPU. The registers A, B, A_1, A_2 , MDR, the bus and the ALU are 8-bit wide. SP and MAR are 16-bit registers. The MUX is of size $8 \times (2 : 1)$ and the DEMUX is of size $8 \times (1 : 2)$. Each memory operation takes 2 CPU clock cycles and uses MAR (Memory Address Register) and MDR (Memory Date Register). SP can be decremented locally.



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The CPU instruction "push r" where, $r = A$ or B has the specification

- $M[SP] \leftarrow r$
- $SP \leftarrow SP - 1$

How many CPU clock cycles are required to execute the "push r" instruction?

- A. 2
- B. 3
- C. 4
- D. 5

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gate2001-cse co-and-architecture data-path machine-instructions normal

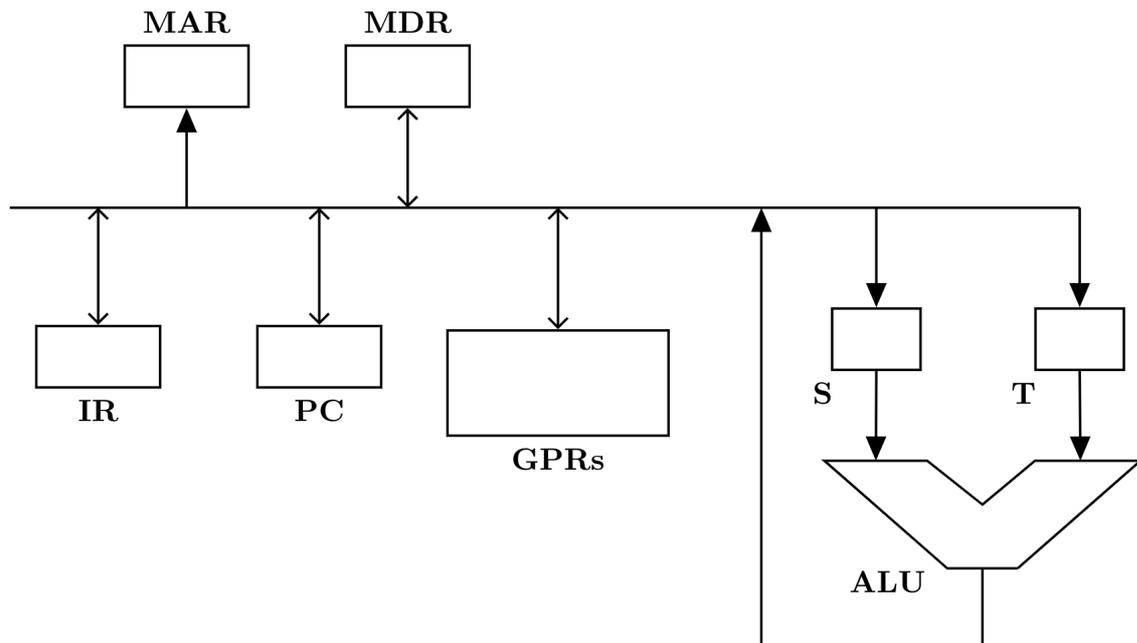
Answer

1.8.3 Data Path: GATE CSE 2005 | Question: 79 [top](#) [5](#)

<https://gateoverflow.in/1402>



Consider the following data path of a CPU.



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The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

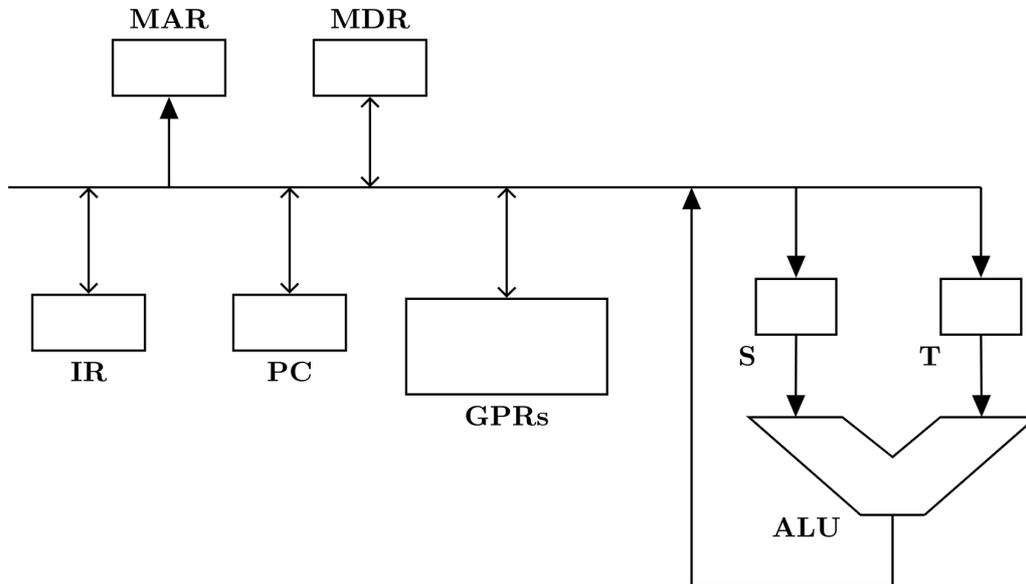
The instruction "add R0, R1" has the register transfer interpretation $R0 \leftarrow R0 + R1$. The minimum number of clock cycles needed for execution cycle of this instruction is:

- A. 2
- B. 3
- C. 4
- D. 5

Answer



Consider the following data path of a CPU.



The ALU, the bus and all the registers in the data path are of identical size. All operations including incrementation of the PC and the GPRs are to be carried out in the ALU. Two clock cycles are needed for memory read operation – the first one for loading address in the MAR and the next one for loading data from the memory bus into the MDR.

The instruction "call Rn, sub" is a two word instruction. Assuming that PC is incremented during the fetch cycle of the first word of the instruction, its register transfer interpretation is

$$R_n \leftarrow PC + 1;$$

$$PC \leftarrow M[PC];$$

The minimum number of CPU clock cycles needed during the execution cycle of this instruction is:

- A. 2
- B. 3
- C. 4
- D. 5

Answer

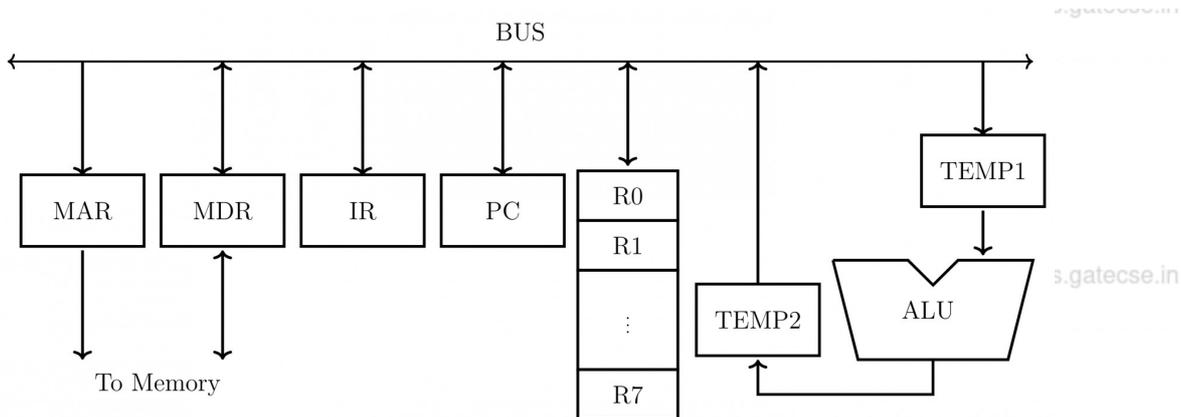


Suppose the functions F and G can be computed in 5 and 3 nanoseconds by functional units U_F and U_G , respectively. Given two instances of U_F and two instances of U_G , it is required to implement the computation $F(G(X_i))$ for $1 \leq i \leq 10$. Ignoring all other delays, the minimum time required to complete this computation is _____ nanoseconds.

Answer



Consider the following data path diagram.



Consider an instruction: $R0 \leftarrow R1 + R2$. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r, TEMP1_r, ALU_{add}, TEMP2_w$
2. $R1_r, TEMP1_w$
3. PC_r, MAR_w, MEM_r
4. $TEMP2_r, R0_w$
5. MDR_r, IR_w

Which one of the following is the correct order of execution of the above steps?

- A. 2, 1, 4, 5, 3
- B. 1, 2, 4, 3, 5
- C. 3, 5, 2, 1, 4
- D. 3, 5, 1, 2, 4

gate2020-cse co-and-architecture data-path

Answer

Answers: Data Path

1.8.1 Data Path: GATE CSE 1990 | Question: 8a top 5

<https://gateoverflow.in/85669>



```

✓
MAR ← PC
PC ← PC + 3
MDR ← MEM[MAR]
IR ← MDR
MAR ← MAR + 1
MDR ← MEM[MAR]
R0 ← MDR
MAR ← MAR + 1
MDR ← MEM[MAR]
R1 ← MDR
R0 ← R0 + R1
  
```

Reference: [CPU Datapath Diagram from Hamacher](#)

References



3 votes

classroom.gateoverflow.in gateoverflow.in classroom.gateover -- Arnab Bhadra (3.7k points)

1.8.2 Data Path: GATE CSE 2001 | Question: 2.13 top 5

<https://gateoverflow.in/731>



- ✓ A microinstruction cannot be further broken down into two or more. It can take more than a cycle if it involves a memory access. The first instruction given here is not a microinstruction. It is an assembly language instruction.

It can be broken down as:

$T1, T2 : MAR \leftarrow SP$

$T3 : MDR \leftarrow r, SP \leftarrow SP - 1$ (It is not mandatory to decrement it in this cycle. Anyway, it can be decremented locally)

$T4, T5 : M[MAR] \leftarrow MDR$

The problem says, 8-bit MDR, 8-bit data bus, 8 bit registers. Can't you see that the given CPU is 8-bit? 8 multiplexers transfer 8 bits when selection input is 0 and 1 respectively. During cycle 1, bits in even positions are moved to MAR. During cycle 2, bits in odd positions are transferred to MAR. We certainly need to move 16-bit SP to 16-bit MAR via a 8-bit bus. So, 2 cycles to get SP to MAR.

The given data path has a single bus, which requires r to be carried in a separate cycle. For the contents of r to be moved to MDR during the cycles $T1$ or $T2$, address and data bus should be separate. Here, it ain't the case.

Memory read takes 2 more cycles. In total, we need 5 of them clock cycles to execute a push.

<https://www.cise.ufl.edu/~mssz/CompOrg/CDA-proc.html>

Computer organization pal chaudari page 334-335

Computer architecture by behrooz parahmi exercise 7.6

Correct Answer: D

References



50 votes

-- Rajaneesh Polavarapu (377 points)

1.8.3 Data Path: GATE CSE 2005 | Question: 79 top 5

<https://gateoverflow.in/1402>



✓ Instruction fetch requires two cycles but the question asks for the **execution part** only!

Now for execution:

1. $R1_{out}, S_{in} \quad S \leftarrow R0 \quad - 1^{st}$ cycle
2. $R2_{out}, T_{in} \quad T \leftarrow R1 \quad - 2^{nd}$ cycle
3. $S_{out}, T_{out}, Add R0_{in} \quad R0 \leftarrow R0 + R1 \quad - 3^{rd}$ cycle

So, 3 cycles for execution.

As it is asked for only execution cycles, no of cycles required = 3.

Had it been asked for instruction cycles, then the answer will be 5.

Hence, option **B** is correct.

58 votes

-- Pooja Palod (24.1k points)

1.8.4 Data Path: GATE CSE 2005 | Question: 80 top 5

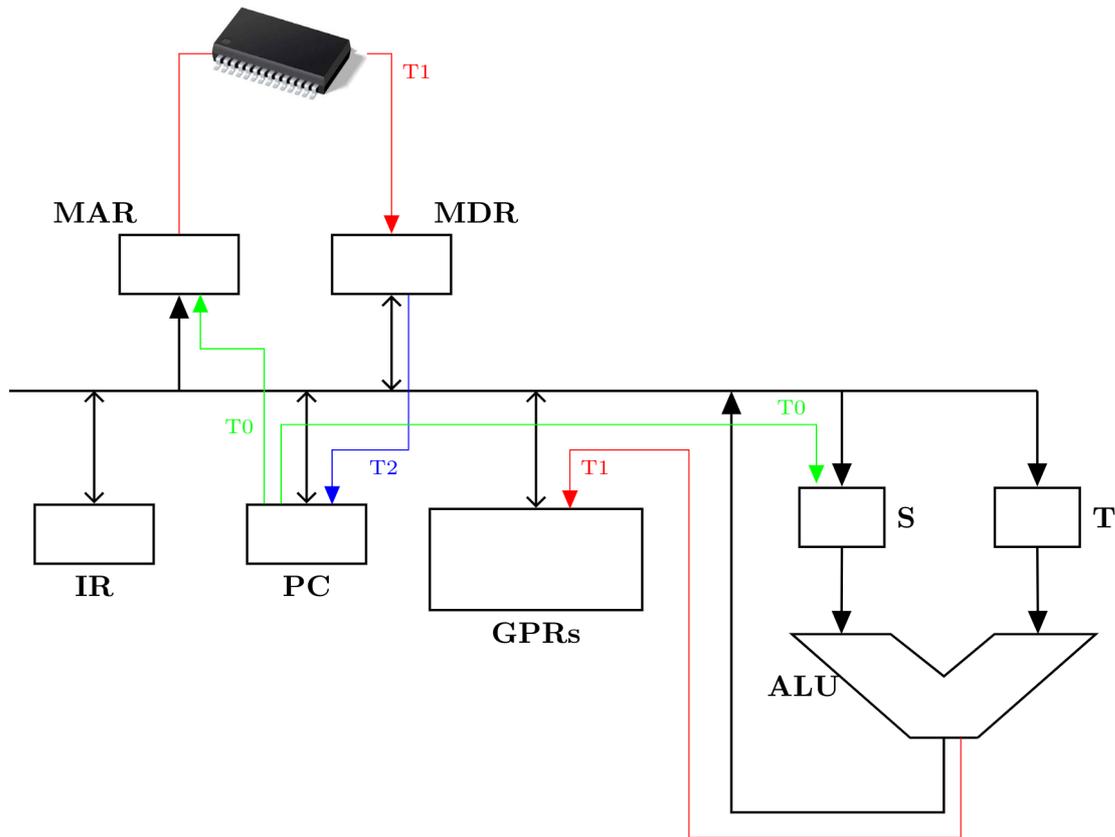
<https://gateoverflow.in/43568>



- ✓
- $MAR \leftarrow PC \quad \rightarrow 1$ cycle
 - $S \leftarrow PC$ (Since these two actions are independent they can be done in same cycle)
 - $MDR \leftarrow M[MAR] \quad \rightarrow 2^{nd}$ cycle (**System BUS**)
 - $Rn \leftarrow S + 1$ (ALU is free and the two actions are independent.) (**Internal BUS**)
 - $PC \leftarrow MDR \quad \rightarrow 3^{rd}$ cycle

Therefore 3 cycles needed.

A rough sketch:



Correct Answer: B

66 votes

-- Riya Roy(Arayana) (5.3k points)

1.8.5 Data Path: GATE CSE 2016 Set 2 | Question: 30

<https://gateoverflow.in/39627>



✓ The same concept is used in pipelining. Bottleneck here is U_F as it takes 5 ns while U_G takes 3ns only. We have to do 10 such calculations and we have 2 instances of U_F and U_G respectively. So, U_F can be done in $50/2 = 25$ nano seconds. For the start U_F needs to wait for U_G output for 3 ns and rest all are pipelined and hence no more wait. So, answer is

$$3 + 25 = 28ns.$$

89 votes

-- Arjun Suresh (332k points)

1.8.6 Data Path: GATE CSE 2020 | Question: 4

<https://gateoverflow.in/333227>



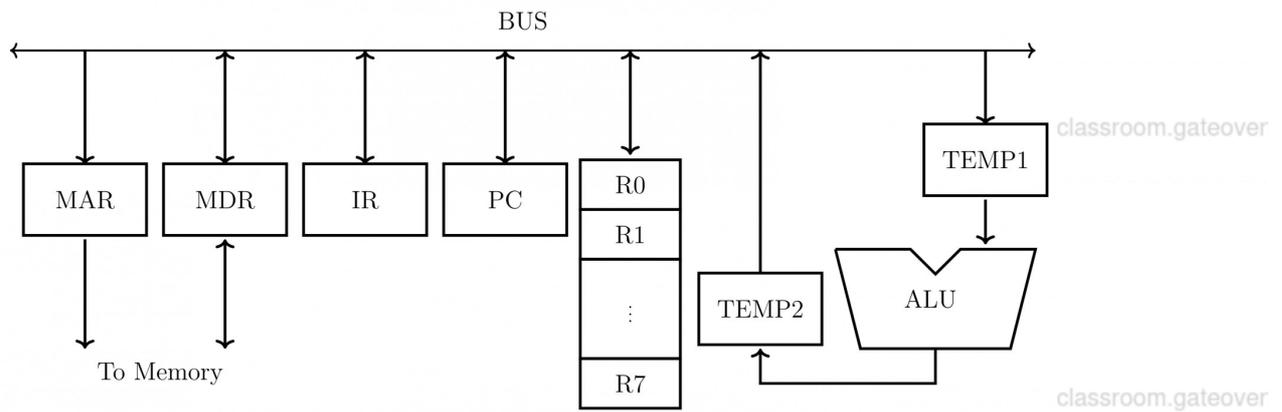
✓ 3^{rd} followed by 5^{th} are **Instruction fetch cycle** micro operations and can be elaborated as follows:

$$t_1 : MAR_w \leftarrow PC_r$$

$$t_2 : MDR_w \leftarrow Memory_r \mid PC \leftarrow PC + 1$$

$$t_3 : IR_w \leftarrow MDR_r$$

Now we need to perform **Execute cycle** micro operations. Just observe the figure and it will be very easy to identify the sequence between $1^{st}, 2^{nd}, 4^{th}$



2nd is clearly stating that we need to move R1 content to some temporary register named as TEMP1 and it is very clear that before performing ALU operation we need the content in TEMP1. Hence 2nd will be performed next after 5th.

$$\text{TEMP1}_w \leftarrow \text{R1}_r$$

Now we can perform ALU operation and can take second operand directly from R2 and the figure clearly shows us that we need to put the result of ALU back into TEMP2. All these steps are performed in 1st. So 1st will be next.

$$\text{TEMP2}_w \leftarrow \text{TEMP1}_r +_{\text{ALU}_{add}} \text{R2}_r$$

Lastly we need to put the result present in TEMP2 into R0. This step is performed by 4th.

$$\text{R0}_w \leftarrow \text{TEMP2}_r$$

Correct Answer (C) : 3, 5, 2, 1, 4

3 votes

-- KUSHAGRA गुप्ता (10.5k points)

1.9

Dma (6) top 6

1.9.1 Dma: GATE CSE 2004 | Question: 68 top 6

https://gateoverflow.in/1062



A hard disk with a transfer rate of 10 Mbytes/second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

- A. 5.0%
- B. 1.0%
- C. 0.5%
- D. 0.1%

gate2004-cse dma normal co-and-architecture

Answer 6

1.9.2 Dma: GATE CSE 2005 | Question: 70 top 6

https://gateoverflow.in/1393



Consider a disk drive with the following specifications:

16 surfaces, 512 tracks/surface, 512 sectors/track, 1 KB/sector, rotation speed 3000 rpm. The disk is operated in cycle stealing mode whereby whenever one 4 byte word is ready it is sent to memory; similarly, for writing, the disk interface reads a 4 byte word from the memory in each DMA cycle. Memory cycle time is 40 nsec. The maximum percentage of time that the CPU gets blocked during DMA operation is:

- A. 10
- B. 25
- C. 40
- D. 50

gate2005-cse co-and-architecture disks normal dma

Answer 6



On a non-pipelined sequential processor, a program segment, which is the part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

```
Initialize the address register
Initialize the count to 500
LOOP: Load a byte from device
Store in memory at address given by address register
Increment the address register
Decrement the count
If count !=0 go to LOOP
```

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

What is the approximate speed up when the DMA controller based design is used in a place of the interrupt driven program based input-output?

- A. 3.4
- B. 4.4
- C. 5.1
- D. 6.7

gate2011-cse co-and-architecture dma normal

Answer



The size of the data count register of a DMA controller is 16bits.
The processor needs to transfer a file of 29,154 kilobytes from disk to main memory.
The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is _____.

gate2016-cse-set1 co-and-architecture dma normal numerical-answers

Answer



Consider a computer system with DMA support. The DMA module is transferring one 8-bit character in one CPU cycle from a device to memory through *cycle stealing* at regular intervals. Consider a 2 MHz processor. If 0.5% processor cycles are used for DMA, the data transfer rate of the device is _____ bits per second.

gate2021-cse-set2 numerical-answers co-and-architecture dma

Answer



The storage area of a disk has the innermost diameter of 10 cm and outermost diameter of 20 cm. The maximum storage density of the disk is 1400 bits/cm. The disk rotates at a speed of 4200 RPM. The main memory of a computer has 64-bit word length and 1 μ s cycle time. If cycle stealing is used for data transfer from the disk, the percentage of memory cycles stolen for transferring one word is

- A. 0.5%
- B. 1%
- C. 5%
- D. 10%

gate2004-it co-and-architecture dma normal

Answer



✓ Clock cycle time = $\frac{1}{600 \times 10^6}$ [Frequency = 1/Time]

For DMA initiation and completion = $\frac{(900+300)}{600 \times 10^6} = 2$ microsec .

Disk Transfer rate = 10 Mbytes/sec

1 byte = $\frac{1}{10^7}$ sec

20 Kbytes = 2 milisec = 2000 micro sec

Percentage = $\left(\frac{2}{2+2000}\right) \times 100 = 0.0999 \approx 0.1\%$

option (D)

% of CPU time consume $\frac{x}{x+y}$

Now, when, use x = Data preparation time or Total cycle time used by CPU and y = Data transfer time

To calculate the fraction of CPU time to the data transfer time - we use $\frac{x}{x+y}$ it is burst mode.

👍 81 votes

-- Prashant Singh (47.2k points)



512 KB-1/50 sec

4 Byte transfer will take total : $4/(512 \times 50 \times 2^{10}) = 152.58$ ns

DMA will transfer 4B in 40nsec

So, Cpu will be blocked $(40/152.58) = 26\%$ of time

Best matching answer is (B).

👍 55 votes

-- Anurag Semwal (6.7k points)



✓

	Statement	Clock Cycles(s) Needed
	Initialize the address register	1
	Initialize the count to 500	1
LOOP:	Load a byte from device	2
	Store in memory at address given by address register	2
	Increment the address register	1
	Decrement the count	1
	If count != 0 go to LOOP	1

Interrupt driven transfer time = $1 + 1 + 500 \times (2 + 2 + 1 + 1 + 1) = 3502$

DMA based transfer time = $20 + 500 \times 2 = 1020$

Speedup = $3502/1020 = 3.4$

Correct Answer: A

👍 90 votes

-- Manu Thakur (34k points)



✓

Data count register gives the number of words the DMA can transfer in a single cycle..

Here it is 16 bits.. so max 2^{16} words can be transferred in one cycle..

Since memory is byte addressable.. 1 word = 1 byte
so 2^{16} bytes in 1 cycle..

Now for the given file..

$$\begin{aligned} \text{File size} &= 29154 \text{ KB} = 29154 \times 2^{10} \text{ B} \\ 1 \text{ cycle} &\rightarrow \text{DMA transfers } 2^{16} \text{ B} \end{aligned}$$

i.e

$$1 \text{ B transferred by DMA} \rightarrow \frac{1}{2^{16}} \text{ cycles.}$$

Now, for full file of size 29154 KB,

$$\text{minimum number of cycles} = \frac{(29154 \times 2^{10} \text{ B})}{2^{16}} = 455.53$$

But number of cycles is asked so $455.53 \rightarrow 456$.

👍 57 votes

-- Abhilash Panicker (7.6k points)



✓

Answer is 80,000.

To complete one cycle at 2 MHz it will take $\frac{1}{2 \times 10^6}$ seconds. So the total number of CPU cycles in one second will be 2×10^6 .

Now 0.5% of these cycles are taken by DMA to transfer the data.

So total number of cycles taken to transfer the data will be $\frac{0.5}{100} \times 2 \times 10^6 = 10,000$ and in each cycle 8 bits are transferred.

So, data transfer rate in bits per second = $8 \times 10000 = 80,000$.

👍 3 votes

-- JATIN MITTAL (2.1k points)



✓

In a disk all tracks have equal capacity and so data density is highest for the innermost track as it has the smallest radius.

- Maximum storage density (hence of innermost track) = 1400 bits per cm
- Track capacity $\pi \times d \times 1400 \text{ bits} = 3.14 \times 10 \times 1400 = 43960 \text{ bits}$

With 4200 rotations per minute, data transfer rate = $\frac{4200 \times 43960}{60}$ bits per second.

Therefore, to transfer 64 bits time required = $\frac{60}{4200 \times 43960} \times 64 = 20.798 \mu s$

With $1 \mu s$ memory cycle time, the disk will take one memory cycle out of $21 + 1 = \frac{1}{21 + 1} \times 100 \approx 5\%$

(PS: If we consider just one word transfer we add the memory cycle time to the disk transfer time in the denominator but for continuous DMA transfer, this is not required as when data is transferred to main memory, disk can continue reading new data)

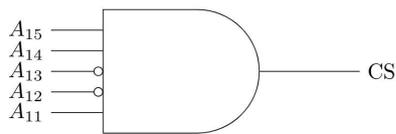
👍 16 votes

-- gatecse (63.3k points)



The chip select logic for a certain DRAM chip in a memory system design is shown below. Assume that the memory system has 16 address lines denoted by A_{15} to A_0 . What is the range of address (in hexadecimal) of the memory system that can get

enabled by the chip select (CS) signal?



- A. C800 to CFFF
- B. CA00 to CAFF
- C. C800 to C8FF
- D. DA00 to DFFF

gate2019-cse co-and-architecture dram
 Answer

Answers: Dram

1.10.1 Dram: GATE CSE 2019 | Question: 2 [top](#)

<https://gateoverflow.in/302846>



✓ $(A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9 A_8 A_7 A_6 A_5 A_4 A_3 A_2 A_1 A_0)$

According to question:

$$A_{15} = 1, A_{14} = 1, A_{13} = 0, A_{12} = 0, A_{11} = 1$$

So the possible range in binary:

$$(1100100000000000) \text{ to } (1100111111111111)$$

Converting to Hexadecimal:

$$(C800) \text{ to } (CFFF)$$

Option A.

40 votes

-- Rituraj Mohanty (3.1k points)

The memory system that can be enabled by the chip select signal

→ From this we can understand that, CS should be 1.

→ Note that it is AND gate, \implies all input lines should be 1.

$$\rightarrow A_{15} \cdot A_{14} \cdot \overline{A_{13}} \cdot \overline{A_{12}} \cdot A_{11} = 1 \implies (A_{15} = 1 \text{ and } A_{14} = 1 \text{ and } \overline{A_{13}} = 1 \text{ and } \overline{A_{12}} = 1 \text{ and } A_{11} = 1)$$

$$\rightarrow \overline{A_{13}} = 1 \implies A_{13} = 0$$

$$\rightarrow \overline{A_{12}} = 1 \implies A_{12} = 0$$

\therefore The address denoted by A_{15} to A_0 is, (Note A_{15} as MSB and A_0 as LSB)

$$(1100)(1_____)(______)(______)$$

→ For starting address, keep all 0's in the blanks, and for ending address keep all 1's in the blanks.

$$\rightarrow \text{Starting address :- } 1100\ 1000\ 0000\ 0000 \implies (C800)_H$$

$$\rightarrow \text{Ending address :- } 1100\ 1111\ 1111\ 1111 \implies (CFFF)_H$$

1.11

Instruction Execution (7) top

1.11.1 Instruction Execution: GATE CSE 1990 | Question: 4-iii top

<https://gateoverflow.in/85391>

State whether the following statements are TRUE or FALSE with reason:

The flags are affected when conditional CALL or JUMP instructions are executed.

tests.gatecse.in

gate1990 true-false co-and-architecture instruction-execution

Answer

1.11.2 Instruction Execution: GATE CSE 1992 | Question: 01-iv top

<https://gateoverflow.in/548>

Many of the advanced microprocessors prefetch instructions and store it in an instruction buffer to speed up processing. This speed up is achieved because _____

goclasses.in

tests.gatecse.in

gate1992 co-and-architecture easy instruction-execution fill-in-the-blanks

Answer

1.11.3 Instruction Execution: GATE CSE 1995 | Question: 1.2 top

<https://gateoverflow.in/2589>

Which of the following statements is true?

- A. ROM is a Read/Write memory
- B. PC points to the last instruction that was executed
- C. Stack works on the principle of LIFO
- D. All instructions affect the flags

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goclasses.in

tests.gatecse.in

gate1995 co-and-architecture normal instruction-execution

Answer

1.11.4 Instruction Execution: GATE CSE 2002 | Question: 1.13 top

<https://gateoverflow.in/817>

Which of the following is not a form of memory

- A. instruction cache
- B. instruction register
- C. instruction opcode
- D. translation look-a-side buffer

tests.gatecse.in

goclasses.in

tests.gatecse.in

gate2002-cse co-and-architecture easy instruction-execution

Answer

1.11.5 Instruction Execution: GATE CSE 2006 | Question: 43 top

<https://gateoverflow.in/1819>

Consider a new instruction named branch-on-bit-set (mnemonic bbs). The instruction “bbs reg, pos, label” jumps to label if bit in position pos of register operand reg is one. A register is 32 -bits wide and the bits are numbered 0 to 31, bit in position 0 being the least significant. Consider the following emulation of this instruction on a processor that does not have bbs implemented.

$$temp \leftarrow reg \& mask$$

Branch to label if temp is non-zero. The variable temp is a temporary register. For correct emulation, the variable mask must be generated by

- A. $mask \leftarrow 0x1 \ll pos$
- B. $mask \leftarrow 0xffffffff \ll pos$
- C. $mask \leftarrow pos$
- D. $mask \leftarrow 0xf$

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goclasses.in

tests.gatecse.in

Answer

1.11.6 Instruction Execution: GATE CSE 2017 Set 1 | Question: 49 [top](#)

<https://gateoverflow.in/118332>



Consider a RISC machine where each instruction is exactly 4 bytes long. Conditional and unconditional branch instructions use PC-relative addressing mode with Offset specified in bytes to the target location of the branch instruction. Further the Offset is always with respect to the address of the next instruction in the program sequence. Consider the following instruction sequence

Instr. No.	Instruction
i:	add R2, R3, R4
i+1:	sub R5, R6, R7
i+2:	cmp R1, R9, R10
i+3:	beq R1, Offset

If the target of the branch instruction is i , then the decimal value of the Offset is _____.

Answer

1.11.7 Instruction Execution: GATE CSE 2021 Set 2 | Question: 53 [top](#)

<https://gateoverflow.in/357484>



Consider a pipelined processor with 5 stages, Instruction Fetch(IF), Instruction Decode(ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and the register read is performed in the EX stage, The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies.

Consider the following sequence of 8 instructions:

ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The *speedup* defined as follows.

$$Speedup = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forwarding}}$$

The *Speedup* achieved in executing the given instruction sequence on the pipelined processor (rounded to 2 decimal places) is _____.

Answer

Answers: Instruction Execution

1.11.1 Instruction Execution: GATE CSE 1990 | Question: 4-iii [top](#)

<https://gateoverflow.in/85391>



False. Flags are tested during conditional call and jump not affected or changed

15 votes

-- khush tak (5.9k points)

1.11.2 Instruction Execution: GATE CSE 1992 | Question: 01-iv [top](#)

<https://gateoverflow.in/548>



✓ Because CPU is faster than memory. Fetching instructions from memory would require considerable amount of time while CPU is much faster. So, prefetching the instructions to be executed can save considerable amount of waiting time.

23 votes

-- Arjun Suresh (332k points)

1.11.3 Instruction Execution: GATE CSE 1995 | Question: 1.2 [top](#)

<https://gateoverflow.in/2589>



✓ It is (C).

Only the top of the stack can be accessed at any time. You can imagine a stack to be opened from only one side data structure. So that if we put one thing over the other, we are able to access the last thing we inserted first. That is Last in First Out (LIFO).

- ROM is Read-Only Memory.
- PC points to the next instruction to be executed.
- Not all instructions affect the flags.

👍 19 votes

-- Gate Keeda (15.9k points)

1.11.4 Instruction Execution: GATE CSE 2002 | Question: 1.13 top 5

<https://gateoverflow.in/817>



✓ The instruction opcode is a part of the instruction which tells the processor what operation is to be performed so it is not a form of memory while the others are

👍 26 votes

-- Bhagirathi Nayak (11.7k points)

1.11.5 Instruction Execution: GATE CSE 2006 | Question: 43 top 5

<https://gateoverflow.in/1819>



✓ A. $mask \leftarrow 0x1 \ll pos$

We want to check for a particular bit position say 2 (third from right). Let the number be $0xA2A7$ (last 4 bits being 0111). Here, the bit at position 2 from right is 1. So, we have to AND this with $0x0004$ as any other flag would give wrong value (may count other bits or discard the bit at position "pos"). And $0x0004$ is obtained by $0x1 \ll 2$ (by shifting 1 "pos" times to the left we get a flag with 1 being set only for the "pos" bit position).

👍 45 votes

-- Arjun Suresh (332k points)

1.11.6 Instruction Execution: GATE CSE 2017 Set 1 | Question: 49 top 5

<https://gateoverflow.in/118332>



✓ Answer is -16 .

Program Counter is updated with the address of next instruction even before the current instruction is executed.

That is why the question says that the address of the next instruction is updated with next instruction in sequence.

Before executing instruction $i + 3$, the current state looks as under:

Please note: BEQ instruction is for Branch Equal

Address		
2000	i	add R2, R3, R4
2004	i+1	sub R5, R6, R7
2008	i+2	cmp R1, R9, R10
2012	i+3	beq R1, Offset
2016	Next instruction	

Program Counter is pointing here →

Question says that the target of branch instruction is 'i' which is at 2000 in our example.

So, we need to go to address 2000 from address 2016 (which is currently pointed by PC)

$$2016 - 2000 = 16$$

So, we have to specify Offset as -16 which would mean that 16 should be subtracted from next address instruction (2016).

👍 51 votes

-- Arunav Khare (3.9k points)

1.11.7 Instruction Execution: GATE CSE 2021 Set 2 | Question: 53 top 5

<https://gateoverflow.in/357484>



✓ Correct Answer: 1.875

$$\text{Speedup}(\text{def in question}) = \frac{\text{Time without Operand Forwarding}}{\text{Time with Operand Forwarding}}$$

classroom.gateover

Without Operand Forwarding:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
ADD	IF	ID	EX	MEM	WB																						
MUL		IF	ID			EX	EX	MEM	WB																		
ADD			IF			ID				EX	MEM	WB															
MUL						IF				ID			EX	EX	MEM	WB											
ADD										IF			ID				EX	MEM	WB								
MUL													IF				ID	MEM	WB	EX	EX	MEM	WB				
ADD																	IF			ID				EX	MEM	WB	
MUL																				IF					ID		

Time taken without Operand Forwarding = 30

With Operand Forwarding:

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
ADD	IF	ID	EX	MEM	WB											
MUL		IF	ID	EX	EX	MEM	WB									
ADD			IF	ID		EX	MEM	WB								
MUL				IF		ID	EX	EX	MEM	WB						
ADD						IF	ID		EX	MEM	WB					
MUL							IF		ID	EX	EX	MEM	WB			
ADD									IF	ID		EX	MEM	WB		
MUL										IF		ID	EX	EX	MEM	WB

Time taken with Operand Forwarding = 16

$$\text{Speedup} = \frac{\text{Time without Operand Forwarding}}{\text{Time with Operand Forwarding}} = \frac{30}{16} = 1.875$$

7 votes

-- Cringe is my middle name... (885 points)

1.12 Instruction Format (7) top

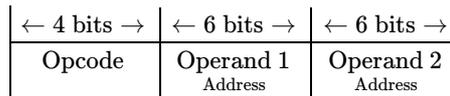
1.12.1 Instruction Format: GATE CSE 1988 | Question: 2-ii top

https://gateoverflow.in/91676



Using an expanding opcode encoding for instructions, is it possible to encode all of the following in an instruction format shown in the below figure. Justify your answer.

- 14 double address instructions
- 127 single address instructions
- 60 no address (zero address) instructions



gate1988 normal co-and-architecture instruction-format descriptive

Answer

1.12.2 Instruction Format: GATE CSE 1992 | Question: 01-vi top

https://gateoverflow.in/551



In an 11-bit computer instruction format, the size of address field is 4-bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero-address instructions it can support is

gate1992 co-and-architecture machine-instructions instruction-format normal numerical-answers

Answer

1.12.3 Instruction Format: GATE CSE 1994 | Question: 3.2 top

https://gateoverflow.in/2479



State True or False with one line explanation

Expanding opcode instruction formats are commonly employed in RISC. (Reduced Instruction Set Computers) machines.

gate1994 co-and-architecture machine-instructions instruction-format normal true-false

Answer

1.12.4 Instruction Format: GATE CSE 2014 Set 1 | Question: 9 [top](#)

<https://gateoverflow.in/1767>



A machine has a 32-bit architecture, with 1-word long instructions. It has 64 registers, each of which is 32 bits long. It needs to support 45 instructions, which have an immediate operand in addition to two register operands. Assuming that the immediate operand is an unsigned integer, the maximum value of the immediate operand is _____.

gate2014-cse-set1 co-and-architecture machine-instructions instruction-format numerical-answers normal

tests.gatecse.in

Answer

1.12.5 Instruction Format: GATE CSE 2016 Set 2 | Question: 31 [top](#)

<https://gateoverflow.in/39601>



Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____.

gate2016-cse-set2 instruction-format machine-instructions co-and-architecture normal numerical-answers

Answer

1.12.6 Instruction Format: GATE CSE 2018 | Question: 51 [top](#)

<https://gateoverflow.in/204126>



A processor has 16 integer registers (R_0, R_1, \dots, R_{15}) and 64 floating point registers (F_0, F_1, \dots, F_{63}). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R+1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is _____.

gate2018-cse co-and-architecture machine-instructions instruction-format numerical-answers

Answer

1.12.7 Instruction Format: GATE CSE 2020 | Question: 44 [top](#)

<https://gateoverflow.in/333187>



A processor has 64 registers and uses 16-bit instruction format. It has two types of instructions: I-type and R-type. Each I-type instruction contains an opcode, a register name, and a 4-bit immediate value. Each R-type instruction contains an opcode and two register names. If there are 8 distinct I-type opcodes, then the maximum number of distinct R-type opcodes is _____.

gate2020-cse numerical-answers instruction-format machine-instructions

Answer

Answers: Instruction Format

1.12.1 Instruction Format: GATE CSE 1988 | Question: 2-ii [top](#)

<https://gateoverflow.in/91676>



✓ 4 bits are for the opcode so number of 2 address instructions will be $2^4 = 16$ – so 14 double instructions are possible.

But out of 16 only 14 are used so 2 are still left which can be used for 1 address instruction. For 1 address instruction we can use not only the 2 left over but also the 6 bits of operand 1 (to make it one address) – so 6 bits that is 64. So, total 2×64 single address instructions can be supported – So, 127 single instructions are possible

But out of 128, 127 are used so 1 left which can be used for zero-address instruction. To make number of zero address we can use the operand 2 address (we already included operand 1 address) – 6 bits. So, total number possible is 64. So, total $1 \times 64 = 64$ zero address instructions are possible.

So, all encoding are possible.

👍 24 votes

-- Pavan Kumar Munnam (7.4k points)

1.12.2 Instruction Format: GATE CSE 1992 | Question: 01-vi top

<https://gateoverflow.in/551>



✓ No. of possible instruction encoding = $2^{11} = 2048$

No. of encoding taken by two-address instructions = $5 \times 2^4 \times 2^4 = 1280$

No. of encoding taken by one-address instructions = $32 \times 2^4 = 512$

So, no. of possible zero-address instructions = $2048 - (1280 + 512) = 256$

👍 64 votes

-- Arjun Suresh (332k points)

1.12.3 Instruction Format: GATE CSE 1994 | Question: 3.2 top

<https://gateoverflow.in/2479>



✓ I think the answer is **TRUE**.

RISC systems use fixed length instruction to simplify pipeline.

eg: MIPS, PowerPC: Instructions are 4 bytes long.

CISC systems use Variable-length instructions.

eg: Intel 80X86: Instructions vary from 1 to 17 bytes long.

Now the challenge is: How to fit multiple sets of instruction types into same (limited) number of bits (Fixed size instruction)?

Here comes Expanding opcode into the picture.

RISC systems commonly uses Expanding opcode technique to have fixed size instructions.

👍 39 votes

-- Sachin Mittal (15.8k points)

1.12.4 Instruction Format: GATE CSE 2014 Set 1 | Question: 9 top

<https://gateoverflow.in/1767>



✓ 64 registers means 6 bits ($\lceil \log_2 64 \rceil = 6$) for a register operand. So, 2 registers operand requires 12 bits. Now, 45 instructions require another 6 bits for opcode ($\lceil \log_2 45 \rceil = 6$). So, totally 18 bits. So, we have $32 - 18 = 14$ bits left for the immediate operand. So, the max value will be $2^{14} - 1 = 16383$ (as the operand is unsigned we do not need a sign bit and with 14 bits we can represent from 0 to $2^{14} - 1$)

👍 82 votes

-- Arjun Suresh (332k points)

1.12.5 Instruction Format: GATE CSE 2016 Set 2 | Question: 31 top

<https://gateoverflow.in/39601>



✓ **Answer: 500 bytes**

Number of registers = 64

Number of bits to address register = $\lceil \log_2 64 \rceil = 6$ - bits

Number of Instructions = 12

Opcode size = $\lceil \log_2 12 \rceil = 4$

Opcode(4)	reg1(6)	reg2(6)	reg3(6)	Immediate(12)
-----------	---------	---------	---------	---------------

Total bits per instruction = 34

Total bytes per instruction = 4.25

Due to byte alignment we cannot store 4.25 bytes, without wasting 0.75 bytes.

So, total bytes per instruction = 5

Total number of instructions = 100

Total size = Number of instructions \times Size of an instruction

= $100 \times 5 = 500$ bytes



✓ We have 2-byte instruction format. So, total number of instruction encodings = 2^{16}

PS: This is not the number of different instructions but different encodings; a single instruction can have different encodings when the address part differs.

No. of bits taken by an integer operand (16 possible integer registers) = $\log_2 16 = 4$.

No. of bits taken by a floating point operand (64 possible floating point registers) = $\log_2 64 = 6$.

No. of encodings consumed by Type 1 instructions = $4 \times 2^{3 \times 4} = 2^{14}$.

No. of encodings consumed by Type 2 instructions = $8 \times 2^{2 \times 6} = 2^{15}$.

No. of encodings consumed by Type 3 instructions = $14 \times 2^{(4+6)} = 14336$.

No. of encodings left for Type 4 = $2^{16} - (2^{14} + 2^{15} + 14336) = 2048$.

No. of different instructions of Type 4 = $\frac{2048}{64} = 32$.

Answer: 32 Instructions

Explanation:

Given,

16 Integer registers. So, we need 4 bits to address any one of them.

64 Floating point registers. This requires 6 bits to uniquely identify them.

Each instruction is 16 bits long.

Type 1 Instructions:

4 instructions, each with 3 integer operands.

The 3 integers, each requires 4 bits. So, $4 * 3$ bits for operands. We are left with $16 - 12 = 4$ bits.

With 4 bits, $2^4 = 16$ opcodes are possible. Out of these we used 4 opcodes. i.e 2 bits. Let's say first two bits are fixed to 00 and next two bits are used for 4 different Type1 instructions.

00 00 ...

00 01 ...

00 10 ...

00 11 ...

Type 2 Instructions:

8 instructions, each with 2 floating point register operands.

Here we need $6 * 2$ bits for operands, and remaining $16 - 12 = 4$ bits are left for opcodes.

So using these 4 bits, we need to get 8 opcodes.

Here we can't use 00 ... for any opcode since it will not distinguish Type 2 from Type 1. So, we are left with 12 opcodes. And we are going to use 8 out of these 12 for type 2 instructions.

01 00 ...

01 01 ...

01 10 ...

01 11 ...

10 00 ...

10 01 ...

10 10 ...

10 11 ...

Type 3 Instructions:

14 instructions, with 1 integer and 1 floating type operand.

$4 + 6 = 10$ bits required for opcodes, remaining $16 - 10 = 6$ bits available for use in opcode.

The only valid combination left for this first 2 bits is 11 ... Rest have been used in Type1 and Type2 instructions.

So, we are left with 4 bits for opcodes. With these 4 bits we can have $2^4 = 16$ opcodes, out of which 14 are required. So, we use all except last two opcodes:

11 00 00 ...

11 ...

11 11 01 ...

These two opcodes are still left unassigned.

11 11 10 ...

11 11 11 ...

Type 4 Instructions:

N instructions, each with 1 floating point operand.

We have $16 - 6 = 10$ bits for opcode. Out of 10 bits, first 6 bits can be either one of the two left opcodes(above). And any combination for remaining 4 bits.

So we have $2 * 2^4$ opcodes. So, $N = 32$.

👍 103 votes

-- Rishabh Gupta (12.5k points)

1.12.7 Instruction Format: GATE CSE 2020 | Question: 44 [top](#)

<https://gateoverflow.in/333187>



✓ Instruction Length: 16 bits

To distinguish among 64 registers, we need $\log_2(64) = 6$ bits

I-type instruction format:

Opcode	Register	Immediate Value
--------	----------	-----------------

R-type instruction format:

Opcode	Register	Register
--------	----------	----------

Maximum possible encodings = 2^{16}

It is given that there are 8 *I-type* instructions. Let's assume the maximum *R-type* instructions to be x .

Therefore, $(8 \times 2^6 \times 2^4) + (x \times 2^6 \times 2^6) = 2^{16}$

$$\Rightarrow x = 16 - 2 = 14$$

👍 32 votes

-- Debasish Das (1.5k points)

1.13

Interrupts (7) [top](#)

1.13.1 Interrupts: GATE CSE 1987 | Question: 1-viii [top](#)

<https://gateoverflow.in/80274>



On receiving an interrupt from a I/O device the CPU:

- A. Halts for a predetermined time.
- B. Hands over control of address bus and data bus to the interrupting device.
- C. Branches off to the interrupt service routine immediately.
- D. Branches off to the interrupt service routine after completion of the current instruction.

gate1987 co-and-architecture interrupts

Answer [👉](#)



In a vectored interrupt:

- A. The branch address is assigned to a fixed location in memory
- B. The interrupting source supplies the branch information to the processor through an interrupt vector
- C. The branch address is obtained from a register in the processor
- D. None of the above

gate1995 co-and-architecture interrupts normal

Answer



Which of the following is true?

- A. Unless enabled, a CPU will not be able to process interrupts.
- B. Loop instructions cannot be interrupted till they complete.
- C. A processor checks for interrupts before executing a new instruction.
- D. Only level triggered interrupts are possible on microprocessors.

gate1998 co-and-architecture interrupts normal

Answer



A device employing INTR line for device interrupt puts the CALL instruction on the data bus while:

- A. \overline{INTA} is active
- B. HOLD is active
- C. READY is inactive
- D. None of the above

gate2002-cse co-and-architecture interrupts normal

Answer



A device with data transfer rate 10 KB/sec is connected to a CPU. Data is transferred byte-wise. Let the interrupt overhead be $4\mu\text{sec}$. The byte transfer time between the device interface register and CPU or memory is negligible. What is the minimum performance gain of operating the device under interrupt mode over operating it under program-controlled mode?

- A. 15
- B. 25
- C. 35
- D. 45

gate2005-cse co-and-architecture interrupts

Answer



A CPU generally handles an interrupt by executing an interrupt service routine:

- A. As soon as an interrupt is raised.
- B. By checking the interrupt register at the end of fetch cycle.
- C. By checking the interrupt register after finishing the execution of the current instruction.

D. By checking the interrupt register at fixed time intervals.

tests.gatecse.in

goclasses.in

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gate2009-cse co-and-architecture interrupts normal ugcnetjune2012iii

Answer

1.13.7 Interrupts: GATE CSE 2020 | Question: 3 top

https://gateoverflow.in/333228



Consider the following statements.

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- I. Daisy chaining is used to assign priorities in attending interrupts.
- II. When a device raises a vectored interrupt, the CPU does polling to identify the source of interrupt.
- III. In polling, the CPU periodically checks the status bits to know if any device needs its attention.
- IV. During DMA, both the CPU and DMA controller can be bus masters at the same time.

Which of the above statements is/are TRUE?

- A. I and II only
- B. I and IV only
- C. I and III only
- D. III only

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goclasses.in

tests.gatecse.in

gate2020-cse co-and-architecture interrupts

Answer

Answers: Interrupts

1.13.1 Interrupts: GATE CSE 1987 | Question: 1-viii top

https://gateoverflow.in/80274



✓ Answer should be **(D)** i.e branches off to ISR after completing current instruction.

CPU checks the status bit of interrupt at the completion of each current instruction running when there is a interrupt it service the interrupt using ISR.

<https://gateoverflow.in/18581/isro2009-78>

References



gateoverflow.in

gateoverflow.in

classroom.gateover

17 votes

-- Gate Mission (2.8k points)

1.13.2 Interrupts: GATE CSE 1995 | Question: 1.3 top

https://gateoverflow.in/2590



✓ Answer: B

A vectored interrupt is a processing technique in which the interrupting device directs the processor to the appropriate interrupt service routine. This is in contrast to a polled interrupt system, in which a single interrupt service routine must determine the source of the interrupt by checking all potential interrupt sources, a slow and relatively laborious process.

33 votes

-- Rajarshi Sarkar (27.9k points)

1.13.3 Interrupts: GATE CSE 1998 | Question: 1.20 top

https://gateoverflow.in/1657



✓ Answer is **(A)**.

Options **(B)** and **(D)** are obviously false.

A processor checks for the interrupt before **FETCHING** an instruction, so option **(C)** is also false.

44 votes

-- Hardi Shah (281 points)



- ✓ INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INTR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option.

👍 22 votes

-- Tejas Jaiswal (559 points)



- ✓ In Programmed I/O, the CPU issues a command and waits for I/O operations to complete.

So here, CPU will wait for 1 sec to transfer 10 KB of data.

overhead in programmed I/O = 1 sec

In Interrupt mode, data is transferred word by word (here word size is 1 byte as mentioned in question "Data is transferred byte-wise").

So to transfer 1 byte of data overhead is 4×10^{-6} sec

Thus to transfer 10 KB of data overhead is $4 \times 10^{-6} \times 10^4$ sec

$$\text{Performance gain} = \frac{1}{4 \times 10^{-6} \times 10^4} = \frac{1}{4 \times 10^{-2}} = 25$$

Thus, (b) is correct answer.

👍 91 votes

-- ashwini anand (231 points)



- ✓ It will be (C).

After finishing the execution of each instruction the CPU reads the interrupt pins to recognize the interrupts.

INTR = 1 = Interrupt is present.(Service the Interrupt)

INTR = 0 = Interrupt is not present.(Goto next Instruction fetch from user program)

👍 29 votes

-- Gate Keeda (15.9k points)



- ✓ Answer : C

I is true

- The **daisy-chaining** method of establishing **priority** consists of a serial connection of all devices that request an interrupt. The device with the highest **priority** is placed in the first position, followed by lower-**priority** devices up to the device with the lowest **priority**, which is placed last in the **chain**.

II. is false

- Vectored interrupts are achieved by assigning each interrupting device a unique code, typically four to eight bits in length. When a device interrupts, it sends its unique code over the data bus to the processor, telling the processor which interrupt service routine to execute.

III. is true

- The process of **periodically checking status bits** to see if it is time for the next I/O operation, is called **polling**. **Polling** is the simplest way for an I/O device to communicate with the processor the processor.

IV. is false

- Since CPU release bus only after getting request from DMA and get after DMA release the BUS.

👍 8 votes

-- Prashant Singh (47.2k points)

1.14.1 Io Handling: GATE CSE 1987 | Question: 2a top

<https://gateoverflow.in/80572>

State whether the following statements are TRUE or FALSE

In a microprocessor-based system, if a bus (DMA) request and an interrupt request arrive simultaneously, the microprocessor attends first to the bus request.

gate1987 co-and-architecture interrupts io-handling true-false

Answer

1.14.2 Io Handling: GATE CSE 1987 | Question: 2b top

<https://gateoverflow.in/80576>

State whether the following statements are TRUE or FALSE:

Data transfer between a microprocessor and an I/O device is usually faster in memory-mapped-I/O scheme than in I/O-mapped -I/O scheme.

gate1987 co-and-architecture io-handling true-false

Answer

1.14.3 Io Handling: GATE CSE 1990 | Question: 4-ii top

<https://gateoverflow.in/85390>

State whether the following statements are TRUE or FALSE with reason:

The data transfer between memory and I/O devices using programmed I/O is faster than interrupt-driven I/O.

gate1990 true-false co-and-architecture io-handling interrupts

Answer

1.14.4 Io Handling: GATE CSE 1996 | Question: 1.24 top

<https://gateoverflow.in/2728>

For the daisy chain scheme of connecting I/O devices, which of the following statements is true?

- A. It gives non-uniform priority to various devices
- B. It gives uniform priority to all devices
- C. It is only useful for connecting slow devices to a processor device
- D. It requires a separate interrupt pin on the processor for each device

gate1996 co-and-architecture io-handling normal

Answer

1.14.5 Io Handling: GATE CSE 1996 | Question: 25 top

<https://gateoverflow.in/2777>

A hard disk is connected to a 50 MHz processor through a DMA controller. Assume that the initial set-up of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 500 clock cycles for the processor. The hard disk has a transfer rate of 2000 Kbytes/sec and average block transferred is 4 K bytes. What fraction of the processor time is consumed by the disk, if the disk is actively transferring 100% of the time?

gate1996 co-and-architecture io-handling dma numerical-answers normal

Answer

1.14.6 Io Handling: GATE CSE 1997 | Question: 2.4 top

<https://gateoverflow.in/2230>

The correct matching for the following pairs is:

- | | |
|-----------------------------|--------------------|
| (A) DMA I/O | (1) High speed RAM |
| (B) Cache | (2) Disk |
| (C) Interrupt I/O | (3) Printer |
| (D) Condition Code Register | (4) ALU |

- A. A - 4 B - 3 C - 1 D - 2
 B. A - 2 B - 1 C - 3 D - 4
 C. A - 4 B - 3 C - 2 D - 1
 D. A - 2 B - 3 C - 4 D - 1

gate1997 co-and-architecture normal io-handling

Answer

1.14.7 Io Handling: GATE CSE 2008 | Question: 64, ISRO2009-13 top

<https://gateoverflow.in/487>



Which of the following statements about synchronous and asynchronous I/O is NOT true?

- A. An ISR is invoked on completion of I/O in synchronous I/O but not in asynchronous I/O
 B. In both synchronous and asynchronous I/O, an ISR (Interrupt Service Routine) is invoked after completion of the I/O
 C. A process making a synchronous I/O call waits until I/O is complete, but a process making an asynchronous I/O call does not wait for completion of the I/O
 D. In the case of synchronous I/O, the process waiting for the completion of I/O is woken up by the ISR that is invoked after the completion of I/O

gate2008-cse operating-system io-handling normal isro2009

Answer

Answers: Io Handling

1.14.1 Io Handling: GATE CSE 1987 | Question: 2a top

<https://gateoverflow.in/80572>



The HOLD input has a higher priority than the INTR or NMI interrupt inputs.

So the answer is true.

5 votes

-- mystylecse (1.8k points)

1.14.2 Io Handling: GATE CSE 1987 | Question: 2b top

<https://gateoverflow.in/80576>



True
 it will take extra time in IO mapped IO because of control signal.

0 votes

-- Arnabh Gangwar (307 points)

1.14.3 Io Handling: GATE CSE 1990 | Question: 4-ii top

<https://gateoverflow.in/85390>



- ✓ False because in programmed I/O, CPU will check the I/O devices' status according to written program. Suppose CPU requested 5 I/O devices and the program is written to check sequentially and 5th device is ready before 2nd device, then also CPU will come to check at its turn.

So, programmed I/O doesn't care about availability status of devices. it blindly works according to written program. That's why it is slow.

Interrupt driven I/O : Here, if any device is ready then it won't wait for CPU, it will say to CPU that "I am ready" by sending interrupt request and the delay here will be only "time taken in servicing the interrupt" which is less than programmed I/O.

So, the answer is **FALSE**.

40 votes

-- bharti (2.3k points)



- ✓ Daisy chaining approach tells the processor in which order the interrupt should be handled by providing priority to the devices.

In daisy-chaining method, all the devices are connected in serial. The device with the highest priority is placed in the first position, followed by lower priority devices. The interrupt pin is common to all.

So answer is option (A).

👍 46 votes

-- Ravi Singh (11.8k points)



- ✓ 2000 KB is transferred in 1 second

4 KB transfer is $(4/2000) * 1000 \text{ ms} = 2 \text{ ms}$

Total cycle required for locking and handling of interrupts after DMA transfer control

$= (1000 + 500) \text{ clock cycle} = 1500 \text{ clock cycle}$

Now, $50 \text{ Mhz} = 50 * 10^6 = 0.02 \text{ microsecond}$

So, $(1500 * 0.02) = 30 \text{ microsecond}$

$30 \mu\text{s}$ for initialization and termination and 2 ms for data transfer.

The CPU time is consumed only for initialization and termination.

Fraction of CPU time consumed $= \frac{30 \mu\text{s}}{(30 \mu\text{s} + 2 \text{ ms})} = 0.015$

👍 45 votes

-- Pooja Palod (24.1k points)



- ✓ Correct Option: B. A – 2, B – 1, C – 3, D – 4

A.	DMA I/O	2.	Disk
B.	Cache	1.	High-speed RAM
C.	Interrupt I/O	3.	Printer
D.	Condition Code Register	4.	ALU

Reason:

- *DMA I/O* - For high speed, high volume data transfer from disk without affecting the processor(in most cases).
- *Cache*-A high speed & low memory version of a RAM.
- *Interrupt I/O* - The printer sends an interrupt signal when it is ready for use.
- *Condition Code Register* - Part of the ALU, as a special purpose register, to store flag bits.

[Source - Google/Wikipedia]

👍 25 votes

-- Siddharth Mahapatra (1.2k points)



- ✓ Answer is (B).

In synchronous I/O process performing I/O operation will be placed in blocked state till the I/O operation is completed. An ISR will be invoked after the completion of I/O operation and it will place process from block state to ready state.

In asynchronous I/O, Handler function will be registered while performing the I/O operation. The process will not be placed in

the block state and process continues to execute the remaining instructions. when the I/O operation completed signal mechanism is used to notify the process that data is available.

72 votes

-- gate_asp (615 points)

1.15

Machine Instructions (19) top

1.15.1 Machine Instructions: GATE CSE 1988 | Question: 9i top

<https://gateoverflow.in/94384>



The following program fragment was written in an assembly language for a single address computer with one accumulator register:

```
LOAD B
MULT C
STORE T1
ADD A
STORE T2
MULT T2
ADD T1
STORE Z
```

Give the arithmetic expression implemented by the fragment.

gate1988 normal descriptive co-and-architecture machine-instructions

Answer

1.15.2 Machine Instructions: GATE CSE 1994 | Question: 12 top

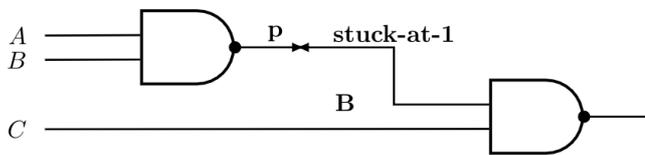
<https://gateoverflow.in/2508>



A. Assume that a CPU has only two registers R_1 and R_2 and that only the following instruction is available $XOR R_i, R_j; \{R_j \leftarrow R_i \oplus R_j, \text{ for } i, j = 1, 2\}$

Using this XOR instruction, find an instruction sequence in order to exchange the contents of the registers R_1 and R_2

B. The line p of the circuit shown in figure has stuck at 1 fault. Determine an input test to detect the fault.



gate1994 co-and-architecture machine-instructions normal descriptive

Answer

1.15.3 Machine Instructions: GATE CSE 1999 | Question: 17 top

<https://gateoverflow.in/1516>



Consider the following program fragment in the assembly language of a certain hypothetical processor. The processor has three general purpose registers R_1, R_2 and R_3 . The meanings of the instructions are shown by comments (starting with ;) after the instructions.

```
X: CMP R1, 0; Compare R1 and 0, set flags appropriately in status register
JZ Z; Jump if zero to target Z
MOV R2, R1; Copy contents of R1 to R2
SHR R1; Shift right R1 by 1 bit
SHL R1; Shift left R1 by 1 bit
CMP R2, R1; Compare R2 and R1 and set flag in status register
JZ Y; Jump if zero to target Y
INC R3; Increment R3 by 1;
Y: SHR R1; Shift right R1 by 1 bit
JMP X; Jump to target X
Z:...
```

A. Initially R_1, R_2 and R_3 contain the values 5, 0 and 0 respectively, what are the final values of R_1 and R_3 when control reaches Z?

B. In general, if R_1, R_2 and R_3 initially contain the values n, 0, and 0 respectively. What is the final value of R_3 when control reaches Z?

gate1999 co-and-architecture machine-instructions normal descriptive



Consider the following assembly language program for a hypothetical processor A , B , and C are 8-bit registers. The meanings of various instructions are shown as comments.

```

MOV B, #0      ;  $B \leftarrow 0$ 
MOV C, #8      ;  $C \leftarrow 8$ 
Z:  CMP C, #0   ; compare C with 0
    JZ X        ; jump to X if zero flag is set
    SUB C, #1   ;  $C \leftarrow C - 1$ 
    RRC A, #1   ; right rotate A through carry by one bit. Thus:
                ; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and
                ;  $c_0$  respectively, their values after the execution of this
                ; instruction will be  $c_0 a_7 \dots a_1$  and  $a_0$  respectively.
    JC Y        ; jump to Y if carry flag is set
    JMP Z       ; jump to Z
Y:  ADD B, #1   ;  $B \leftarrow B + 1$ 
    JMP Z       ; jump to Z
X:

```

If the initial value of register A is A_0 the value of register B after the program execution will be

- A. the number of 0 bits in A_0
- B. the number of 1 bits in A_0
- C. A_0
- D. 8



Consider the following assembly language program for a hypothetical processor A , B , and C are 8 bit registers. The meanings of various instructions are shown as comments.

```

MOV B, #0      ;  $B \leftarrow 0$ 
MOV C, #8      ;  $C \leftarrow 8$ 
Z:  CMP C, #0   ; compare C with 0
    JZ X        ; jump to X if zero flag is set
    SUB C, #1   ;  $C \leftarrow C - 1$ 
    RRC A, #1   ; right rotate A through carry by one bit. Thus:
                ; If the initial values of A and the carry flag are  $a_7 \dots a_0$  and
                ;  $c_0$  respectively, their values after the execution of this
                ; instruction will be  $c_0 a_7 \dots a_1$  and  $a_0$  respectively.
    JC Y        ; jump to Y if carry flag is set
    JMP Z       ; jump to Z
Y:  ADD B, #1   ;  $B \leftarrow B + 1$ 
    JMP Z       ; jump to Z

```


Answer 

1.15.8 Machine Instructions: GATE CSE 2006 | Question: 09, ISRO2009-35 [top](#)

<https://gateoverflow.in/888>



A CPU has 24-bit instructions. A program starts at address 300 (in decimal). Which one of the following is a legal program counter (all values in decimal)?

- A. 400
- B. 500
- C. 600
- D. 700

Answer 

1.15.9 Machine Instructions: GATE CSE 2007 | Question: 54 [top](#)

<https://gateoverflow.in/1252>



In a simplified computer the instructions are:

OP R_j, R_i	Perform R_j OP R_i and store the result in register R_j
OP m, R_i	Perform val OP R_i and store the result in register R_i val denotes the content of the memory location m
MOV m, R_i	Moves the content of memory location m to register R_i
MOV R_i, m	Moves the content of register R_i to memory location m

The computer has only two registers, and OP is either ADD or SUB. Consider the following basic block:

- $t_1 = a + b$
- $t_2 = c + d$
- $t_3 = e - t_2$
- $t_4 = t_1 - t_3$

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

- A. 2
- B. 3
- C. 5
- D. 6

Answer 

1.15.10 Machine Instructions: GATE CSE 2007 | Question: 71 [top](#)

<https://gateoverflow.in/1269>



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

- A. 10
- B. 11
- C. 20
- D. 21

gate2007-cse co-and-architecture machine-instructions interrupts normal

Answer

1.15.11 Machine Instructions: GATE CSE 2007 | Question: 72

<https://gateoverflow.in/43515>



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is:

- A. 100
- B. 101
- C. 102
- D. 110

gate2007-cse co-and-architecture machine-instructions interrupts normal

Answer

1.15.12 Machine Instructions: GATE CSE 2007 | Question: 73

<https://gateoverflow.in/43516>



Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in

decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction “INC R3”, what return address will be pushed on to the stack?

- A. 1005
- B. 1020
- C. 1024
- D. 1040

gate2007-cse co-and-architecture machine-instructions interrupts normal

Answer

1.15.13 Machine Instructions: GATE CSE 2008 | Question: 34

<https://gateoverflow.in/445>



Which of the following must be true for the RFE (Return From Exception) instruction on a general purpose processor?

- I. It must be a trap instruction
- II. It must be a privileged instruction
- III. An exception cannot be allowed to occur during execution of an RFE instruction

- A. I only
- B. II only
- C. I and II only
- D. I, II and III only

gate2008-cse co-and-architecture machine-instructions normal

Answer

1.15.14 Machine Instructions: GATE CSE 2015 Set 2 | Question: 42

<https://gateoverflow.in/8215>



Consider a processor with byte-addressable memory. Assume that all registers, including program counter (PC) and Program Status Word (PSW), are size of two bytes. A stack in the main memory is implemented from memory location $(0100)_{16}$ and it grows upward. The stack pointer (SP) points to the top element of the stack. The current value of SP is $(016E)_{16}$. The CALL instruction is of two words, the first word is the op-code and the second word is the starting address of the subroutine (one word = 2 bytes). The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
- Store the value of PSW register in the stack
- Load the starting address of the subroutine in PC

The content of PC just before the fetch of a CALL instruction is $(5FA0)_{16}$. After execution of the CALL instruction, the value of the stack pointer is:

- A. $(016A)_{16}$
- B. $(016C)_{16}$
- C. $(0170)_{16}$
- D. $(0172)_{16}$

gate2015-cse-set2 co-and-architecture machine-instructions easy

Answer

1.15.15 Machine Instructions: GATE CSE 2016 Set 2 | Question: 10

<https://gateoverflow.in/39547>



A processor has 40 distinct instruction and 24 general purpose registers. A 32-bit instruction word has an opcode, two registers operands and an immediate operand. The number of bits available for the immediate operand field is _____.

gate2016-cse-set2 machine-instructions co-and-architecture easy numerical-answers

Answer



Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	$R1 \leftarrow \text{MEMORY}[5000]$	4
MOV R2, (R3)	$R2 \leftarrow \text{MEMORY}[R3]$	4
ADDR2, R1	$R2 \leftarrow R1 + R2$	2
MOV (R3), R2	$\text{MEMORY}[R3] \leftarrow R2$	4
INC R3	$R3 \leftarrow R3 + 1$	2
DEC R1	$R1 \leftarrow R1 - 1$	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3020 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is _____

gate2021-cse-set1 co-and-architecture machine-instructions numerical-answers

Answer



If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and M[100] is a memory reference), then the sequence of operations

R1 \rightarrow M[100]
M[100] \rightarrow R2
M[100] \rightarrow R3

can be replaced by

- A. R1 \rightarrow R3
R2 \rightarrow M[100]
- B. M[100] \rightarrow R2
R1 \rightarrow R2
R1 \rightarrow R3
- C. R1 \rightarrow M[100]
R2 \rightarrow R3
- D. R1 \rightarrow R2
R1 \rightarrow R3
R1 \rightarrow M[100]

gate2004-it co-and-architecture machine-instructions easy

Answer



Following table indicates the latencies of operations between the instruction producing the result and instruction using the result.

Instruction producing the result	Instruction using the result	Latency
ALU Operation	ALU Operation	2
ALU Operation	Store	2
Load	ALU Operation	1
Load	Store	0

Consider the following code segment:

```
Load R1, Loc 1; Load R1 from memory location Loc1
```

```

Load R2, Loc 2; Load R2 from memory location Loc 2
Add R1, R2, R1; Add R1 and R2 and save result in R1
Dec R2;          Decrement R2
Dec R1;          Decrement R1
Mpy R1, R2, R3; Multiply R1 and R2 and save result in R3
Store R3, Loc 3; Store R3 in memory location Loc 3

```

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What is the number of cycles needed to execute the above code segment assuming each instruction takes one cycle to execute?

- A. 7
- B. 10
- C. 13
- D. 14

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gate2007-it co-and-architecture machine-instructions normal

Answer

1.15.19 Machine Instructions: GATE IT 2008 | Question: 38 [top](#)

<https://gateoverflow.in/3348>



Assume that $EA = (X)+$ is the effective address equal to the contents of location X, with X incremented by one word length after the effective address is calculated; $EA = -(X)$ is the effective address equal to the contents of location X, with X decremented by one word length before the effective address is calculated; $EA = (X)-$ is the effective address equal to the contents of location X, with X decremented by one word length after the effective address is calculated. The format of the instruction is (opcode, source, destination), which means (destination \leftarrow source op destination). Using X as a stack pointer, which of the following instructions can pop the top two elements from the stack, perform the addition operation and push the result back to the stack.

- A. ADD $(X)-, (X)$
- B. ADD $(X), (X)-$
- C. ADD $-(X), (X)+$
- D. ADD $-(X), (X)$

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gate2008-it co-and-architecture machine-instructions normal

Answer

Answers: Machine Instructions

1.15.1 Machine Instructions: GATE CSE 1988 | Question: 9i [top](#)

<https://gateoverflow.in/94384>



✓ $Z = [BC + A]^2 + (BC)$

12 votes

-- Yash wadhvani (831 points)

1.15.2 Machine Instructions: GATE CSE 1994 | Question: 12 [top](#)

<https://gateoverflow.in/2508>



✓

- $R_1 \leftarrow R_1 \text{ XOR } R_2$
- $R_2 \leftarrow R_2 \text{ XOR } R_1$
- $R_1 \leftarrow R_1 \text{ XOR } R_2$

Stuck at 0 fault:: A stuck-at fault is a particular fault model used by fault simulators and automatic test pattern generation (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0', and 'X'.

Stuck at line 1 means no matter whatever input we provide to the line the output is always 1. Now, when we take $A = 1, B = 1, C = 1$ the required output, if no fault is there should be 1.

But, since line p is stuck at logic 1 final output of $A \text{ NAND } B$ will be 1 only .So, final circuit output becomes 0.(which is wrong)

Reference : https://www.tutorialspoint.com/digital_electronics/stuckat1_fault_in_logic_circuit.asp

References

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20 votes

-- Vidhi Sethi (8.3k points)

1.15.3 Machine Instructions: GATE CSE 1999 | Question: 17 top<https://gateoverflow.in/1516>

- ✓ SHR R1 (Lower bit is lost and upper bit becomes 0 and all other bits shift right by 1)
- SHL R1 (Upper bit is lost and lower bit becomes 0 and all other bits shift left by 1)

These two operations change the value of $R1$ if its lower bit is 1. So, the given program checks the lowest bit of $R1$ in each iteration and if its 1 then only increment $R3$ and loop terminates when $R1$ becomes 0. Thus at end, $R3$ will have the count of the number of bits set to 1 in $R1$.

- a. $R1 = 0, R3 = 2$ as 101 has two 1's
- b. $R3 = \#1$ in $R1$.

27 votes

-- Arjun Suresh (332k points)

1.15.4 Machine Instructions: GATE CSE 2003 | Question: 48 top<https://gateoverflow.in/938>

- ✓ Option (B). The code is counting the number of 1 bits in A_0 . When a 1 is moved to carry, B is incremented.

30 votes

-- Arjun Suresh (332k points)

1.15.5 Machine Instructions: GATE CSE 2003 | Question: 49 top<https://gateoverflow.in/4377>

- ✓ Option (A) RRC $a, \#1$. As the 8 bit register is rotated via carry 8 times.
 - $a_7 a_6 a_5 a_4 a_3 a_2 a_1 a_0$
 - $c_0 a_7 a_6 a_5 a_4 a_3 a_2 a_1$, now a_0 is the new carry. So, after next rotation,
 - $a_0 c_0 a_7 a_6 a_5 a_4 a_3 a_2$

So, after 8 rotations, $a_6 a_5 a_4 a_3 a_2 a_1 a_0 c_0$ and carry is a_7 .

Now, one more rotation will restore the original value of A_0 .

43 votes

-- Arjun Suresh (332k points)

1.15.6 Machine Instructions: GATE CSE 2004 | Question: 63 top<https://gateoverflow.in/1058>

- ✓ Option is D.

Word size is 32 bits (4 bytes). Interrupt occurs **after execution of HALT** instruction NOT **during**. So address of next instruction will be saved on to the stack which is 1028.

(We have 5 instructions starting from address 1000, each of size 2, 1, 1, 2, 1 totaling 7 words = $7 * 4 = 28$ bytes).

$1000 + 28 = 1028$,

1028 is the starting address of NEXT Instruction .

After HALT instruction CPU enters a HALT state and if an interrupt happens the return address will be **that of the instruction after the HALT**.

References :

- https://x86.puri.sm/html/file_module_x86_id_134.html [X86 Instructors Manual]
- <http://electronics.stackexchange.com/questions/277735/what-happens-if-the-interrupt-occurs-during-the-execution-of-halt-instruction>
- [https://en.wikipedia.org/wiki/HLT_\(x86_instruction\)](https://en.wikipedia.org/wiki/HLT_(x86_instruction))

References



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85 votes

-- Vikrant Singh (11.2k points)

1.15.7 Machine Instructions: GATE CSE 2004 | Question: 64 top

<https://gateoverflow.in/43570>



✓ B. 24 cycles

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Instruction	Size	Fetch and Decode + Execute
MOV	2	$2 \times 2 + 3 = 7$
MOV	1	$2 \times 1 + 3 = 5$
ADD	1	$2 \times 1 + 1 = 3$
MOV	2	$2 \times 2 + 3 = 7$
HALT	1	$2 \times 1 + 0 = 2$
	Total	24 Cycles

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107 votes

-- Vikrant Singh (11.2k points)

1.15.8 Machine Instructions: GATE CSE 2006 | Question: 09, ISRO2009-35 top

<https://gateoverflow.in/888>



✓ Option (C). 24 bits = 3 bytes instructions. So, PC will have multiples of 3 in it.

40 votes

-- anshu (2.7k points)

1.15.9 Machine Instructions: GATE CSE 2007 | Question: 54 top

<https://gateoverflow.in/1252>



- MOV a, R_1
- ADD b, R_1
- MOV c, R_2
- ADD d, R_2
- SUB e, R_2
- SUB R_1, R_2
- MOV R_2, m

Total number of MOV instructions = 3

Correct Answer: B

75 votes

-- Gate Keeda (15.9k points)

1.15.10 Machine Instructions: GATE CSE 2007 | Question: 71 top

<https://gateoverflow.in/1269>



✓ Loop is executed 10 times and there are two memory reference in the loop (each MOV is loading 1 word, so 1 memory reference for each MOV inside the loop). So number of memory reference inside loop is

$$2(\text{MOV}) \times 10 (\text{times iteration}) \times 1 (1 \text{ word access/ MOV}) = 20 \text{ memory accesses.}$$

One memory access is outside the loop for the first instruction

MOV $R_1, (3000)$

So, totally $20 + 1 = 21$

Correct Answer: D

45 votes

-- Vicky Bajoria (4.1k points)

1.15.11 Machine Instructions: GATE CSE 2007 | Question: 72 [top](#)

<https://gateoverflow.in/43515>



✓ The loop runs 10 times.

1. When $R1 = 10$, $Memory[2000] = 110$,
2. When $R1 = 9$, $Memory[2001] = 109$,
3. When $R1 = 8$, $Memory[2002] = 108$,
4. When $R1 = 7$, $Memory[2003] = 107$,
5. When $R1 = 6$, $Memory[2004] = 106$,
6. When $R1 = 5$, $Memory[2005] = 105$,
7. When $R1 = 4$, $Memory[2006] = 104$,
8. When $R1 = 3$, $Memory[2007] = 103$,
9. When $R1 = 2$, $Memory[2008] = 102$,
10. When $R1 = 1$, $Memory[2009] = 101$,

When $R1 = 0$ the loop breaks., $Memory[2010] = 100$

Correct Answer: A

54 votes

-- Arnab Bhadra (3.7k points)

1.15.12 Machine Instructions: GATE CSE 2007 | Question: 73 [top](#)

<https://gateoverflow.in/43516>



✓ An interrupt is checked for after the execution of the current instruction and the contents of PC (address of next instruction to be executed) is pushed on to stack.

Here, address of INC, $R3 = 1000 + \frac{(2 + 1 + 1 + 1) \times 32}{8} = 1020$ and

next instruction address = $1020 + 4 = 1024$ which is pushed on to stack.

Reference: http://www.ece.utep.edu/courses/web3376/Notes_files/ee3376-interrupts_stack.pdf

Correct Answer: C

References



38 votes

-- Vicky Bajoria (4.1k points)

1.15.13 Machine Instructions: GATE CSE 2008 | Question: 34 [top](#)

<https://gateoverflow.in/445>



✓ RFE (Return From Exception) is a privileged trap instruction that is executed when exception occurs, so an exception is not allowed to execute. (D) is the correct option.

Reference: http://www.cs.rochester.edu/courses/252/spring2014/notes/08_exceptions

References



28 votes

-- Vikrant Singh (1.2k points)

1.15.14 Machine Instructions: GATE CSE 2015 Set 2 | Question: 42 [top](#)

<https://gateoverflow.in/8215>



✓ First we have to consider here memory is byte-addressable

The CALL instruction is implemented as follows:

- Store the current value of PC in the stack
PC is 2 bytes it means when we store pc in stack it will increase by 2
So current value of SP is $(016E)_{16} + 2$
- Store the value of PSW register in the stack
PSW is 2 byte it means when we store psw in stack it will increase by 2
So current value of SP is $(016E)_{16} + 2 + 2 = (0172)_{16}$

Correct Answer: *D*

71 votes

-- Anoop Sonkar (4.1k points)

1.15.15 Machine Instructions: GATE CSE 2016 Set 2 | Question: 10

<https://gateoverflow.in/39547>



- ✓ Instruction Opcode Size = $\log_2 40 = 6$

Register operand size = $\log_2 24 = 5$

Total bits available = 32

Bits required for opcode + two register operands = $6 + 2 \times 5 = 16$

Bits available for immediate operand = $32 - 16 = 16$.

54 votes

-- Akash Kanase (36k points)

1.15.16 Machine Instructions: GATE CSE 2021 Set 1 | Question: 55

<https://gateoverflow.in/357397>



- ✓ The given code is iterating 10 times and incrementing the contents of locations 3000 to $3000 + i$ by $10 - i$, for $i < 10$. Location 3010 is left untouched.

So, correct answer: 50.

7 votes

-- Arjun Suresh (332k points)

1.15.17 Machine Instructions: GATE IT 2004 | Question: 46

<https://gateoverflow.in/3689>



- ✓ Data forwarding means if CPU writes to a memory location and subsequently reads from the same memory location, the second instruction can fetch the value directly from the register used to do the write than waiting for the memory. So, this increases the performance.

Here, choices A, B and C doesn't really make any sense as the data was in R1 and it must be moved to R2, R3 and M[100]. So, (D) is the answer.

53 votes

-- Arjun Suresh (332k points)

1.15.18 Machine Instructions: GATE IT 2007 | Question: 41

<https://gateoverflow.in/3476>



- ✓ In the given question there are 7 instructions each of which takes 1 clock cycle to complete. (Pipelining may be used) If an instruction is in execution phase and any other instructions can not be in the execution phase. So, at least 7 clock cycles will be taken.
Now, it is given that between two instructions latency or delay should be there based on their operation. Ex- 1st line of the table says that between two operations in which first is producing the result of an ALU operation and the 2nd is using the result there should be a delay of 2 clock cycles.

Clock cycle	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
	I1	I2		I3	I4		I5			I6			I7

1. Load R1, Loc 1; Load R1 from memory location Loc1
Takes 1 clock cycle, simply loading R1 on loc1.

2. Load R2, Loc 2; Load R2 from memory location Loc2

↳ Takes 1 clock cycle, simply loading r2 on loc2. gateoverflow.in

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3. (Add R1, R2, R1; Add R1 and R2 and save result in R1
R1=R1+R2;

Hence, this instruction is using the result of R1 and R2, i.e. result of Instruction 1 and Instruction 2.

As instruction 1 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 1 and instruction 3, which is already there due to I2.

As instruction 2 is load operation and instruction 3 is ALU operation. So, there should be a delay of 1 clock cycle between instruction 2 and instruction 3.

4. Dec R2; Decrement R2

This instruction is dependent on instruction 2 and there should be a delay of one clock cycle between Instruction 2 and Instruction 4. As instruction 2 is load and 4 is ALU, which is already there due to Instruction 3.

5. Dec R1 Decrement R1

This instruction is dependent on Instruction 3

As Instruction I3 is ALU and I5 is also ALU so a delay of 2 clock cycles should be there between them of which 1 clock cycle delay is already there due to I4 so one clock cycle delay between I4 and I5.

6. MPY R1, R2, R3; Multiply R1 and R2 and save result in R3

R3=R1*R2;

This instruction uses the result of Instruction 5, as both instruction 5 and 6 are ALU so there should be a delay of 2 clock cycles.

7. Store R3, Loc 3 Store R3 in memory location Loc3

This instruction is dependent on instruction 6 which is ALU and instruction 7 is store so there should be a delay of 2 clock cycles between them.

Hence, a total of 13 clock cycles will be there.

Correct Answer: C

↳ 146 votes

-- Madhab Paul Choudhury (2.8k points)

1.15.19 Machine Instructions: GATE IT 2008 | Question: 38 [top](#)

<https://gateoverflow.in/3348>



✓ It should be A as $998 \leftarrow 1000 + 998$. (I am writing only memory locations for sake of brevity)

Lets say SP is 1000 initially then after it calculates the EA of source (which is 1000 as it decrements after the EA) the destination becomes 998 and that is where we want to store the result as stack is decrementing.

In case of C and D it becomes $998 \leftarrow 998 + 998$.

↳ 29 votes

-- Shaun Patel (6.1k points)

1.16

Memory Interfacing (2) [top](#)

1.16.1 Memory Interfacing: GATE CSE 2016 Set 1 | Question: 09 [top](#)

<https://gateoverflow.in/39632>



A processor can support a maximum memory of $4GB$, where the memory is word-addressable (a word consists of two bytes). The size of address bus of the processor is at least _____ bits.

gate2016-cse-set1 co-and-architecture easy numerical-answers memory-interfacing

Answer [👤](#)

1.16.2 Memory Interfacing: GATE CSE 2018 | Question: 23 [top](#)

<https://gateoverflow.in/204097>



A 32-bit wide main memory unit with a capacity of $1GB$ is built using $256 M \times 4\text{-bit}$ DRAM chips. The number of rows of memory cells in the DRAM chip is 2^{14} . The time taken to perform one refresh operation is 50 nanoseconds . The refresh period is 2 milliseconds . The percentage (rounded to the closest integer) of the time available for performing the memory read/write operations in the main memory unit is _____.

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Answer [👤](#)

1.16.1 Memory Interfacing: GATE CSE 2016 Set 1 | Question: 09 [top](#)

<https://gateoverflow.in/39632>



✓ Size of Memory = No of words (Addresses) × No of bits per word

$$2^{32} B = \text{No of words (Addresses)} \times 2B$$

$$\text{No of words (Addresses)} = 2^{31}$$

Number of Address lines = 31

👍 54 votes

-- Praveen Saini (41.9k points)

1.16.2 Memory Interfacing: GATE CSE 2018 | Question: 23 [top](#)

<https://gateoverflow.in/204097>



✓ One refresh operation takes 50ns.

$$\text{Total number of rows} = 2^{14}$$

$$\text{Total time to refresh all Rows} = 2^{14} \times 50 \text{ ns} = 819200 \text{ ns} = 0.819200 \text{ ms}$$

The Refresh Period is 2ms.

$$\begin{aligned} \% \text{ Time spent in refresh} &= \frac{\text{Total time to Refresh all Rows}}{\text{Refresh period}} * 100 \\ &= \frac{0.8192\text{ms}}{2.0\text{ms}} * 100 = 40.96\% \end{aligned}$$

$$\% \text{ Time spent in Read/Write} = 100 - 40.96 = 59.04\%$$

= 59% (Rounded to the closest Integer)

Reference: https://en.wikipedia.org/wiki/Memory_refresh

References



👍 86 votes

-- Digvijay (44.9k points)

1.17

Microprogramming (12) [top](#)

1.17.1 Microprogramming: GATE CSE 1987 | Question: 4a [top](#)

<https://gateoverflow.in/81359>



Find out the width of the control memory of a horizontal microprogrammed control unit, given the following specifications:

- 16 control lines for the processor consisting of ALU and 7 registers.
- Conditional branching facility by checking 4 status bits.
- Provision to hold 128 words in the control memory.

gate1987 co-and-architecture microprogramming descriptive

Answer [🔗](#)

1.17.2 Microprogramming: GATE CSE 1996 | Question: 2.25 [top](#)

<https://gateoverflow.in/2754>



A micro program control unit is required to generate a total of 25 control signals. Assume that during any micro instruction, at most two control signals are active. Minimum number of bits required in the control word to generate the required control signals will be:

- 2
- 2.5
- 10
- 12

gate1996 co-and-architecture microprogramming normal

Answer 

1.17.3 Microprogramming: GATE CSE 1997 | Question: 5.3 [top](#) 

<https://gateoverflow.in/2254>



A micro instruction is to be designed to specify:

- a. none or one of the three micro operations of one kind and
- b. none or upto six micro operations of another kind

The minimum number of bits in the micro-instruction is:

- A. 9
- B. 5
- C. 8
- D. None of the above

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Answer 

1.17.4 Microprogramming: GATE CSE 1999 | Question: 2.19 [top](#) 

<https://gateoverflow.in/1497>



Arrange the following configuration for CPU in decreasing order of operating speeds:

Hard wired control, Vertical microprogramming, Horizontal microprogramming.

- A. Hard wired control, Vertical microprogramming, Horizontal microprogramming.
- B. Hard wired control, Horizontal microprogramming, Vertical microprogramming.
- C. Horizontal microprogramming, Vertical microprogramming, Hard wired control.
- D. Vertical microprogramming, Horizontal microprogramming, Hard wired control.

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normal

Answer 

1.17.5 Microprogramming: GATE CSE 2002 | Question: 2.7 [top](#) 

<https://gateoverflow.in/837>



Horizontal microprogramming:

- A. does not require use of signal decoders
- B. results in larger sized microinstructions than vertical microprogramming
- C. uses one bit for each control signal
- D. all of the above

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microprogramming

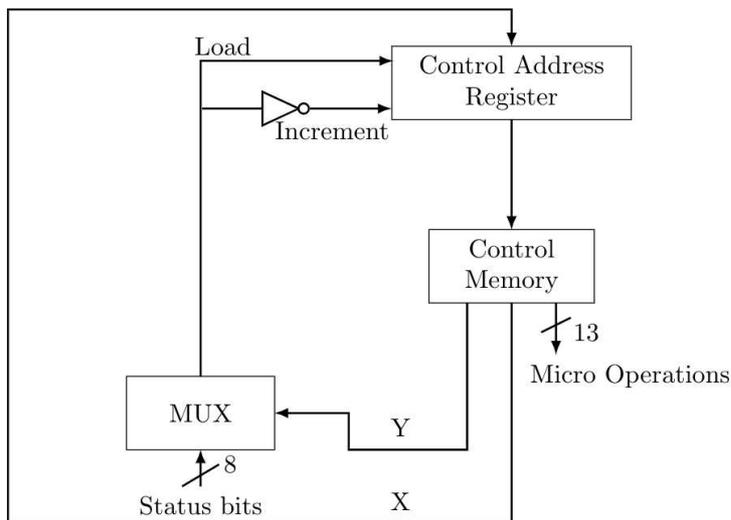
Answer 

1.17.6 Microprogramming: GATE CSE 2004 | Question: 67 [top](#) 

<https://gateoverflow.in/1061>



The microinstructions stored in the control memory of a processor have a width of 26 bits. Each microinstruction is divided into three fields: a micro-operation field of 13 bits, a next address field (X), and a MUX select field (Y). There are 8 status bits in the input of the MUX.



How many bits are there in the X and Y fields, and what is the size of the control memory in number of words?

- A. 10, 3, 1024
- B. 8, 5, 256
- C. 5, 8, 2048
- D. 10, 3, 512

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Answer

1.17.7 Microprogramming: GATE CSE 2013 | Question: 28 top

<https://gateoverflow.in/1539>



Consider the following sequence of micro-operations.

MBR ← PC MAR ← X PC ← Y Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

- A. Instruction fetch
- B. Operand fetch
- C. Conditional branch
- D. Initiation of interrupt service

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Answer

1.17.8 Microprogramming: GATE IT 2004 | Question: 49 top

<https://gateoverflow.in/3692>



A CPU has only three instructions I_1 , I_2 and I_3 , which use the following signals in time steps $T_1 - T_5$:

I_1 : T_1 : Ain, Bout, Cin
 T_2 : PCout, Bin
 T_3 : Zout, Ain
 T_4 : Bin, Cout
 T_5 : End

I_2 : T_1 : Cin, Bout, Din
 T_2 : Aout, Bin
 T_3 : Zout, Ain
 T_4 : Bin, Cout
 T_5 : End

I_3 : T_1 : Din, Aout
 T_2 : Ain, Bout
 T_3 : Zout, Ain
 T_4 : Dout, Ain

T5 : End

Which of the following logic functions will generate the hardwired control for the signal Ain ?

- A. $T1.I1 + T2.I3 + T4.I3 + T3$
- B. $(T1 + T2 + T3).I3 + T1.I1$
- C. $(T1 + T2).I1 + (T2 + T4).I3 + T3$
- D. $(T1 + T2).I2 + (T1 + T3).I1 + T3$

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Answer

1.17.9 Microprogramming: GATE IT 2005 | Question: 45

https://gateoverflow.in/3806



A hardwired CPU uses 10 control signals S_1 to S_{10} , in various time steps T_1 to T_5 , to implement 4 instructions I_1 to I_4 as shown below:

	T ₁	T ₂	T ₃	T ₄	T ₅
I ₁	S_1, S_3, S_5	S_2, S_4, S_6	S_1, S_7	S_{10}	S_3, S_8
I ₂	S_1, S_3, S_5	S_8, S_9, S_{10}	S_5, S_6, S_7	S_6	S_{10}
I ₃	S_1, S_3, S_5	S_7, S_8, S_{10}	S_2, S_6, S_9	S_{10}	S_1, S_3
I ₄	S_1, S_3, S_5	S_2, S_6, S_7	S_5, S_{10}	S_6, S_9	S_{10}

Which of the following pairs of expressions represent the circuit for generating control signals S_5 and S_{10} respectively?

$((I_j + I_k)T_n)$ indicates that the control signal should be generated in time step T_n if the instruction being executed is I_j or I_k

- A. $S_5 = T_1 + I_2 \cdot T_3$ and $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- B. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and $S_{10} = (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- C. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and $S_{10} = (I_2 + I_3 + I_4) \cdot T_2 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$
- D. $S_5 = T_1 + (I_2 + I_4) \cdot T_3$ and $S_{10} = (I_2 + I_3) \cdot T_2 + I_4 \cdot T_3 + (I_1 + I_3) \cdot T_4 + (I_2 + I_4) \cdot T_5$

gate2005-it co-and-architecture microprogramming normal

Answer

1.17.10 Microprogramming: GATE IT 2005 | Question: 49

https://gateoverflow.in/3810



An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:

Group 1 : 20 signals, Group 2 : 70 signals, Group 3 : 2 signals, Group 4 : 10 signals, Group 5 : 23 signals.

How many bits of the control words can be saved by using vertical microprogramming over horizontal microprogramming?

- A. 0
- B. 103
- C. 22
- D. 55

gate2005-it co-and-architecture microprogramming normal

Answer

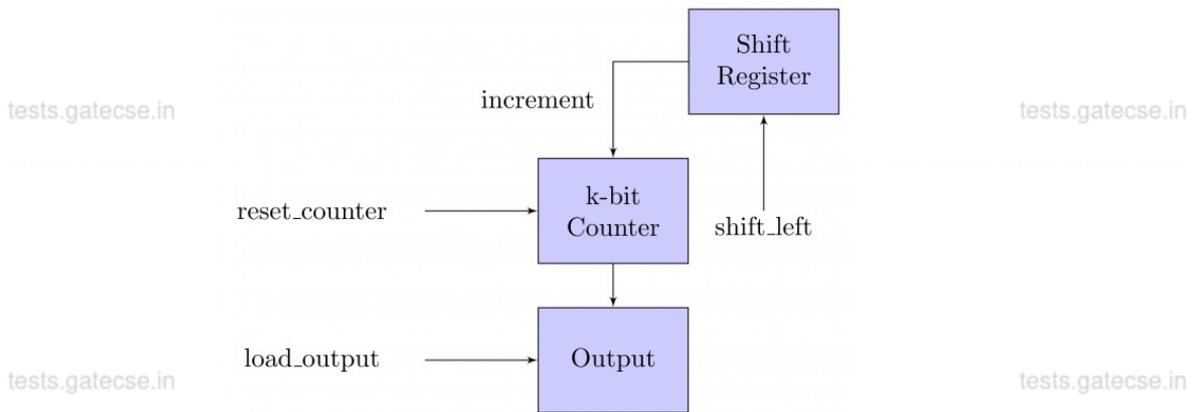
1.17.11 Microprogramming: GATE IT 2006 | Question: 41

https://gateoverflow.in/3884



The data path shown in the figure computes the number of 1s in the 32-bit input word corresponding to an unsigned even integer stored in the shift register.

The unsigned counter, initially zero, is incremented if the most significant bit of the shift register is 1.



The microprogram for the control is shown in the table below with missing control words for microinstructions I_1, I_2, \dots, I_n .

Microinstruction	Reset_Counter	Shift_left	Load_output
BEGIN	1	0	0
I_1	?	?	?
:	:	:	:
I_n	?	?	?
END	0	0	1

The counter width (k), the number of missing microinstructions (n), and the control word for microinstructions I_1, I_2, \dots, I_n are, respectively,

- A. 32, 5, 010
- B. 5, 32, 010
- C. 5, 31, 011
- D. 5, 31, 010

gate2006-it co-and-architecture microprogramming normal

Answer

1.17.12 Microprogramming: GATE IT 2008 | Question: 39

<https://gateoverflow.in/3349>



Consider a CPU where all the instructions require 7 clock cycles to complete execution. There are 140 instructions in the instruction set. It is found that 125 control signals are needed to be generated by the control unit. While designing the horizontal microprogrammed control unit, single address field format is used for branch control logic. What is the minimum size of the control word and control address register?

- A. 125, 7
- B. 125, 10
- C. 135, 9
- D. 135, 10

gate2008-it co-and-architecture microprogramming normal

Answer

Answers: Microprogramming

1.17.1 Microprogramming: GATE CSE 1987 | Question: 4a

<https://gateoverflow.in/81359>



Width of the control memory = size of a control word

- Control word = [Condition bits + control signal bits + next address]
- Condition bits = 4 $\implies \log_2 4$ -bits
- 128 words $\implies 7$ -bits for address.

In the case of horizontal micro-programming, there is 1-bit for each control signal. It is given there are 16 control signals.

⇒ Length of control word = $2 + 16 + 7 = 25$ - bits.

👍 18 votes

-- agoh (1.2k points)

1.17.2 Microprogramming: GATE CSE 1996 | Question: 2.25 top 5

<https://gateoverflow.in/2754>



- ✓ The best sense I can make of this question is that you want to transmit up to 2 simultaneous signals out of a choice of 25, and ask how many bits you need for that.

One solution would be to have 2 groups of 5 - bits, each can send one of 31 signals (or the absence of signal). But it is not optimal. The number of different states is

$$1(\text{no signal}) + 25(\text{one signal}) + (25 \times 24/2)(\text{two signals}) = 326 \text{ states.}$$

You can transmit any of these states over 9 - bits. But it is more complex to encode/ decode, adding an extra bit would probably cost less.
Hence C is correct option.

Reference: https://www.ocf.berkeley.edu/~wwu/cgi-bin/yabb/YaBB.cgi?board=riddles_cs;action=display;num=1354778770

References



👍 30 votes

-- vnc (2.1k points)

1.17.3 Microprogramming: GATE CSE 1997 | Question: 5.3 top 5

<https://gateoverflow.in/2254>



- ✓ Actually the given question incorporates the concept of horizontal μ programming (also known as decoded form of control signals) and vertical μ programming (also known as encoded form of control signals)

The (a) part says :

none or one of the three micro operations of one kind

This is referred to encoding form of vertical one since at most one signal can be active in vertical microprogramming since it involves use of external decoder to select one control signal out of the given control signals..

$$\text{No of bits required for vertical microprogramming given } n \text{ number of control signals} = \lceil (\log_2 n) \rceil$$

Here, $n = 3$

$$\text{So, no of bits required for part (a)} = \lceil (\log_2 3) \rceil = 2$$

Now coming to (b) part , it says :

none or upto six micro operations of another kind

at maximum we can have at most 6 microoperations of another kind at a time. To accommodate that we need decoded form of control signals which is horizontal signals.

So, no of bits required for (b) part

$$= \text{No of control signals of (b) kind} = 6$$

Therefore overall bits required to accommodate both (a) and (b),

$$= 2 + 6 = 8 - \text{bits}$$

Besides this, address field, flags etc are also there in a control word. That is why it is asked in the question :

minimum number of bits in the micro-instruction required

Hence, minimum no of bits required = $8 - bits$

C is the correct answer.

60 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

1.17.4 Microprogramming: GATE CSE 1999 | Question: 2.19

<https://gateoverflow.in/1497>



- ✓ Hard wired control involves only hardware, whereas microprogramming is software approach. So, hardware control should be faster than both microprogramming approaches.

Between vertical and horizontal microprogramming. Horizontal is faster because in this control signals are not encoded whereas in vertical microprogramming to save memory signals are encoded. So, it takes less time in horizontal microprogramming because decoding of signals is not required. Therefore, final order is :

hard wired control > horizontal microprogramming > vertical microprogramming

Correct Answer: B

33 votes

-- Shikhar Vashishth (3.1k points)

1.17.5 Microprogramming: GATE CSE 2002 | Question: 2.7

<https://gateoverflow.in/837>



- ✓ Option (D). All statements are true.

Reference: <http://www.cs.virginia.edu/~cs333/notes/microprogramming.pdf>

References



27 votes

-- Suvojit Mondal (291 points)

1.17.6 Microprogramming: GATE CSE 2004 | Question: 67

<https://gateoverflow.in/1061>



- ✓ $x + y + 13 = 26 \rightarrow (1)$
 $y = 3$ (y is no of bits used to represent 8 different states of multiplexer $\rightarrow (2)$)
 x is no of bits required represent size of control memory
 $x = 10$ from (1) and (2)

\therefore Size of control memory = $2^x = 2^{10} = 1024$

Correct Answer: A

48 votes

-- Digvijay (44.9k points)

1.17.7 Microprogramming: GATE CSE 2013 | Question: 28

<https://gateoverflow.in/1539>



- ✓ Here PC value is being stored in memory which is done when either CALL RETURN involved or there is Interrupt. As, we will have to come back to execute current instruction.

So, options (A), (B) are clearly incorrect.

Option (C) is incorrect because conditional branch does not require to save PC contents.

Option (D) is correct as it matches the generic Interrupt Cycle :

Interrupt Cycle:

t_1 : MBR \leftarrow (PC)
 t_2 : MAR \leftarrow (save-address)
PC \leftarrow (routine-address)
 t_3 : Memory \leftarrow (MBR)

52 votes

-- Himanshu Agarwal (12.4k points)

1.17.8 Microprogramming: GATE IT 2004 | Question: 49 top

<https://gateoverflow.in/3692>



✓ We just have to see which all options give 1 whenever A_{in} is 1 and 0 otherwise.

So, A_{in} is 1 in T_3 of I_1, I_2 and I_3 . Also during T_1 of I_1 , and T_2 and T_4 of I_3 . So, answer will be

$$T_1.I_1 + T_2.I_3 + T_4.I_3 + T_3.I_1 + T_3.I_2 + T_3.I_3$$

Since CPU is having only 3 instructions, $T_3.I_1 + T_3.I_2 + T_3.I_3$ can be replaced with T_3 (we don't need to see which instruction and A_{in} will be activated in time step 3 of all the instructions).

So, $T_1.I_1 + T_2.I_3 + T_4.I_3 + T_3$

The answer is Option (A).

46 votes

-- Arjun Suresh (332k points)

1.17.9 Microprogramming: GATE IT 2005 | Question: 45 top

<https://gateoverflow.in/3806>



✓ D. is the correct option for this question.

If we look at the table, we need to find those time-stamps and instructions which are using these control signals.

For example, $S_5 = T_1$ has used control signal S_5 for all the instructions, or we can say irrespective of the instructions. Also, S_5 is used by instructions I_2 and I_4 for the time stamp T_3 so that comes to:

$$S_5 = T_1 + I_2 \cdot T_3 + I_4 \cdot T_3 = T_1 + (I_2 + I_4) \cdot T_3$$

In the same way, we'll calculate for S_{10} .

It's an example of Hardwired CU Programming used in RISC processors. It gives accurate result, but isn't good for debugging since minor change will cause to restructure the control unit.

31 votes

-- Manu Thakur (34k points)

1.17.10 Microprogramming: GATE IT 2005 | Question: 49 top

<https://gateoverflow.in/3810>



✓ In horizontal microprogramming we need 1 bit for every control word, therefore total bits in

$$\text{Horizontal Microprogramming} = 20 + 70 + 2 + 10 + 23 = 125$$

Now let's consider vertical microprogramming, In vertical microprogramming we use Decoder (n to 2^n) and output lines are equal to number of control words. A input is given according to what control word we have to select.

Now in this question these 5 groups contain mutually exclusive signals, i.e., they can be activated one at a time for a given group, we can safely use decoder.

group 1 = $\lceil \log_2 20 \rceil = 5$ (Number of input bits for decoder, given output is number of control word in given group)

$$\text{group 2} = \lceil \log_2 70 \rceil = 7$$

$$\text{group 3} = \lceil \log_2 2 \rceil = 1$$

$$\text{group 4} = \lceil \log_2 10 \rceil = 4$$

$$\text{group 5} = \lceil \log_2 23 \rceil = 5$$

$$\text{Total bits required in vertical microprogramming} = 5 + 7 + 1 + 4 + 5 = 22$$

$$\text{So number of control words saved} = 125 - 22 = 103$$

Hence, (B) is answer.

1.17.11 Microprogramming: GATE IT 2006 | Question: 41 top

<https://gateoverflow.in/3584>



✓ Answer I_1 to I_n are microinstructions and reset_counter, shift_left and load_output are control signals to activate corresponding hardware(eg. Shift register or load output).

Counter width (k) is 5 bits as shift register uses 32 bit data Only.

The number of missing micro instructions (n) should be 31 as shift register contain Only unsigned EVEN integer. LSB Will be always 0 so no need to shift for LSB.

Control word contains:-

1 for active/enable. 0 for inactive or disabled.

Reset counter is to reset the counter so it must be 0 for all micros.

Shift_left CS should be 1 to shift the given data in shift reg.

And load output has no meaning to make **output** active for all microinstructions as it will be used in the END only so it should be 0.

1.17.12 Microprogramming: GATE IT 2008 | Question: 39 top

<https://gateoverflow.in/3349>



✓ Its answer should be (D) because 140 instructions, each requiring 7 cycles means 980 cycles which will take 10 bits.

Since it is horizontal for control word, 125 control signals + 10 bits = 135 bits will be required.

1.18

Pipelining (36) top

1.18.1 Pipelining: GATE CSE 1999 | Question: 13 top

<https://gateoverflow.in/1512>



An instruction pipeline consists of 4 stages – Fetch (F), Decode field (D), Execute (E) and Result Write (W). The 5 instructions in a certain instruction sequence need these stages for the different number of clock cycles as shown by the table below

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

gate1999 co-and-architecture pipelining normal numerical-answers

Answer

1.18.2 Pipelining: GATE CSE 2000 | Question: 1.8 top

<https://gateoverflow.in/631>



Comparing the time T_1 taken for a single instruction on a pipelined CPU with time T_2 taken on a non-pipelined but identical CPU, we can say that

- A. $T_1 \leq T_2$
- B. $T_1 \geq T_2$
- C. $T_1 < T_2$
- D. T_1 and T_2 plus the time taken for one instruction fetch cycle

gate2000-cse pipelining co-and-architecture easy

Answer



An instruction pipeline has five stages where each stage take 2 nanoseconds and all instruction use all five stages. Branch instructions are not overlapped. i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions,

- Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instruction. Ignore the fact that some branch instructions may be conditional.
- If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.

gate2000-cse co-and-architecture pipelining normal descriptive

Answer



Consider a 5-stage pipeline - IF (Instruction Fetch), ID (Instruction Decode and register read), EX (Execute), MEM (memory), and WB (Write Back). All (memory or register) reads take place in the second phase of a clock cycle and all writes occur in the first phase. Consider the execution of the following instruction sequence:

I1:	sub r2, r3, r4	/* r2 ← r3 - r4 */
I2:	sub r4, r2, r3	/* r4 ← r2 - r3 */
I3:	sw r2, 100(r1)	/* M[r1 + 100] ← r2 */
I4:	sub r3, r4, r2	/* r3 ← r4 - r2 */

- Show all data dependencies between the four instructions.
- Identify the data hazards.
- Can all hazards be avoided by forwarding in this case.

gate2001-cse co-and-architecture pipelining normal descriptive

Answer



The performance of a pipelined processor suffers if:

- the pipeline stages have different delays
- consecutive instructions are dependent on each other
- the pipeline stages share hardware resources
- All of the above

gate2002-cse co-and-architecture pipelining easy isro2008

Answer



For a pipelined CPU with a single ALU, consider the following situations

- The $j + 1^{st}$ instruction uses the result of the j^{th} instruction as an operand
- The execution of a conditional jump instruction
- The j^{th} and $j + 1^{st}$ instructions require the ALU at the same time.

Which of the above can cause a hazard

- I and II only
- II and III only
- III only
- All the three

Answer 1.18.7 Pipelining: GATE CSE 2004 | Question: 69 [top](#)<https://gateoverflow.in/1063>

A 4-stage pipeline has the stage delays as 150, 120, 160 and 140 *nanoseconds*, respectively. Registers that are used between the stages have a delay of 5 *nanoseconds* each. Assuming constant clocking rate, the total time taken to process 1000 data items on this pipeline will be:

- A. 120.4 microseconds
- B. 160.5 microseconds
- C. 165.5 microseconds
- D. 590.0 microseconds

Answer 1.18.8 Pipelining: GATE CSE 2005 | Question: 68 [top](#)<https://gateoverflow.in/1391>

A 5 stage pipelined CPU has the following sequence of stages:

- IF – instruction fetch from instruction memory
- RD – Instruction decode and register read
- EX – Execute: ALU operation for data and address computation
- MA – Data memory access – for write access, the register read at RD state is used.
- WB – Register write back

Consider the following sequence of instructions:

- $I_1: L R0, loc 1; R0 \leftarrow M[loc1]$
- $I_2: A R0, R0; R0 \leftarrow R0 + R0$
- $I_3: S R2, R0; R2 \leftarrow R2 - R0$

Let each stage take one clock cycle.

What is the number of clock cycles taken to complete the above sequence of instructions starting from the fetch of I_1 ?

- A. 8
- B. 10
- C. 12
- D. 15

Answer 1.18.9 Pipelining: GATE CSE 2006 | Question: 42 [top](#)<https://gateoverflow.in/1818>

A CPU has a five-stage pipeline and runs at 1 GHz frequency. Instruction fetch happens in the first stage of the pipeline. A conditional branch instruction computes the target address and evaluates the condition in the third stage of the pipeline. The processor stops fetching new instructions following a conditional branch until the branch outcome is known. A program executes 10^9 instructions out of which 20% are conditional branches. If each instruction takes one cycle to complete on average, the total execution time of the program is:

- A. 1.0 second
- B. 1.2 seconds
- C. 1.4 seconds
- D. 1.6 seconds

Answer 



Consider a pipelined processor with the following four stages:

- IF: Instruction Fetch
- ID: Instruction Decode and Operand Fetch
- EX: Execute
- WB: Write Back

The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions?

ADD	R2, R1, R0	$R2 \leftarrow R1 + R0$
MUL	R4, R3, R2	$R4 \leftarrow R3 * R2$
SUB	R6, R5, R4	$R6 \leftarrow R5 - R4$

- A. 7
- B. 8
- C. 10
- D. 14

gate2007-cse co-and-architecture pipelining normal isro2009

Answer



Which of the following are NOT true in a pipelined processor?

- I. Bypassing can handle all RAW hazards
 - II. Register renaming can eliminate all register carried WAR hazards
 - III. Control hazard penalties can be eliminated by dynamic branch prediction
- A. I and II only
 - B. I and III only
 - C. II and III only
 - D. I, II and III

gate2008-cse pipelining co-and-architecture normal

Answer



Delayed branching can help in the handling of control hazards

For all delayed conditional branch instructions, irrespective of whether the condition evaluates to true or false,

- A. The instruction following the conditional branch instruction is executed
- B. The first instruction in the fall through path is executed
- C. The first instruction in the taken path is executed
- D. The branch takes longer to execute than any other instruction

gate2008-cse co-and-architecture pipelining normal

Answer



Delayed branching can help in the handling of control hazards

The following code is to run on a pipelined processor with one branch delay slot:

I1: $ADD\ R2 \leftarrow R7 + R8$

I2: Sub $R4 \leftarrow R5 - R6$

I3: ADD $R1 \leftarrow R2 + R3$

I4: STORE Memory $[R4] \leftarrow R1$

BRANCH to Label if $R1 == 0$

Which of the instructions I1, I2, I3 or I4 can legitimately occupy the delay slot without any program modification?

- A. I1
- B. I2
- C. I3
- D. I4

gate2008-cse co-and-architecture pipelining normal

Answer 

1.18.14 Pipelining: GATE CSE 2009 | Question: 28 [top](#)

<https://gateoverflow.in/1314>



Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions $I1, I2, I3, I4$ in stages $S1, S2, S3, S4$ is shown below:

	S_1	S_2	S_3	S_4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

What is the number of cycles needed to execute the following loop?

For ($i = 1$ to 2) {I1; I2; I3; I4;}

- A. 16
- B. 23
- C. 28
- D. 30

gate2009-cse co-and-architecture pipelining normal

Answer 

1.18.15 Pipelining: GATE CSE 2010 | Question: 33 [top](#)

<https://gateoverflow.in/2207>



A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
t_0 : MUL R_2, R_0, R_1	$R_2 \leftarrow R_0 * R_1$
t_1 : DIV R_5, R_3, R_4	$R_5 \leftarrow R_3 / R_4$
t_2 : ADD R_2, R_5, R_2	$R_2 \leftarrow R_5 + R_2$
t_3 : SUB R_5, R_2, R_6	$R_5 \leftarrow R_2 - R_6$

- A. 13
- B. 15
- C. 17
- D. 19

gate2010-cse co-and-architecture pipelining normal

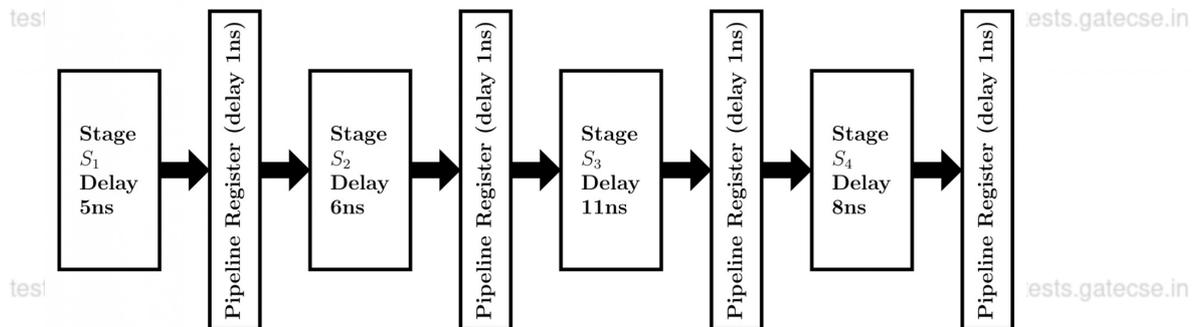
Answer

1.18.16 Pipelining: GATE CSE 2011 | Question: 41

<https://gateoverflow.in/2143>



Consider an instruction pipeline with four stages (S_1 , S_2 , S_3 and S_4) each with combinational circuit only. The pipeline registers are required between each stage and at the end of the last stage. Delays for the stages and for the pipeline registers are given in the figure.



What is the approximate speed up of the pipeline in steady state under ideal conditions when compared to the corresponding non-pipeline implementation?

- A. 4.0
- B. 2.5
- C. 1.1
- D. 3.0

gate2011-cse co-and-architecture pipelining normal

Answer

1.18.17 Pipelining: GATE CSE 2012 | Question: 20, ISRO2016-23

<https://gateoverflow.in/52>



Register renaming is done in pipelined processors:

- A. as an alternative to register allocation at compile time
- B. for efficient access to function parameters and local variables
- C. to handle certain kinds of hazards
- D. as part of address translation

gate2012-cse co-and-architecture pipelining easy isro2016

Answer

1.18.18 Pipelining: GATE CSE 2013 | Question: 45

<https://gateoverflow.in/330>



Consider an instruction pipeline with five stages without any branch prediction:

Fetch Instruction (FI), Decode Instruction (DI), Fetch Operand (FO), Execute Instruction (EI) and Write Operand (WO). The stage delays for FI, DI, FO, EI and WO are 5 ns, 7 ns, 10 ns, 8 ns and 6 ns, respectively. There are intermediate storage buffers after each stage and the delay of each buffer is 1 ns. A program consisting of 12 instructions $I_1, I_2, I_3, \dots, I_{12}$ is executed in this pipelined processor. Instruction I_4 is the only branch instruction and its branch target is I_9 . If the branch is taken during the execution of this program, the time (in ns) needed to complete the program is

- A. 132
- B. 165
- C. 176
- D. 328

gate2013-cse normal co-and-architecture pipelining

Answer



Consider a 6-stage instruction pipeline, where all stages are perfectly balanced. Assume that there is no cycle-time overhead of pipelining. When an application is executing on this 6-stage pipeline, the speedup achieved with respect to non-pipelined execution if 25% of the instructions incur 2 pipeline stall cycles is _____.

gate2014-cse-set1 co-and-architecture pipelining numerical-answers normal

Answer



An instruction pipeline has five stages, namely, instruction fetch (IF), instruction decode and register fetch (ID/RF), instruction execution (EX), memory access (MEM), and register writeback (WB) with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns, respectively (ns stands for nanoseconds). To gain in terms of frequency, the designers have decided to split the ID/RF stage into three stages (ID, RF1, RF2) each of latency $2.2/3$ ns. Also, the EX stage is split into two stages (EX1, EX2) each of latency 1 ns. The new design has a total of eight pipeline stages. A program has 20% branch instructions which execute in the EX stage and produce the next instruction pointer at the end of the EX stage in the old design and at the end of the EX2 stage in the new design. The IF stage stalls after fetching a branch instruction until the next instruction pointer is computed. All instructions other than the branch instruction have an average CPI of one in both the designs. The execution times of this program on the old and the new design are P and Q nanoseconds, respectively. The value of P/Q is _____.

gate2014-cse-set3 co-and-architecture pipelining numerical-answers normal

Answer



Consider the following processors (ns stands for nanoseconds). Assume that the pipeline registers have zero latency.

- P1: Four-stage pipeline with stage latencies 1 ns, 2 ns, 2 ns, 1 ns.
- P2: Four-stage pipeline with stage latencies 1 ns, 1.5 ns, 1.5 ns, 1.5 ns.
- P3: Five-stage pipeline with stage latencies 0.5 ns, 1 ns, 1 ns, 0.6 ns, 1 ns.
- P4: Five-stage pipeline with stage latencies 0.5 ns, 0.5 ns, 1 ns, 1 ns, 1.1 ns.

Which processor has the highest peak clock frequency?

- A. P1
- B. P2
- C. P3
- D. P4

gate2014-cse-set3 co-and-architecture pipelining normal

Answer



Consider a non-pipelined processor with a clock rate of 2.5 GHz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the internal pipeline delay, the clock speed is reduced to 2 GHz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is _____.

gate2015-cse-set1 co-and-architecture pipelining normal numerical-answers

Answer



Consider the sequence of machine instruction given below:

```
MUL  R5, R0, R1
DIV  R6, R2, R3
ADD  R7, R5, R6
SUB  R8, R7, R4
```

In the above sequence, $R0$ to $R8$ are general purpose registers. In the instructions shown, the first register shows the result of the operation performed on the second and the third registers. This sequence of instructions is to be executed in a pipelined instruction processor with the following 4 stages: (1) Instruction Fetch and Decode (IF), (2) Operand Fetch (OF), (3) Perform Operation (PO) and (4) Write back the result (WB). The IF , OF and WB stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instruction, 3 clock cycles for MUL instruction and 5 clock cycles for DIV instruction. The pipelined processor uses operand forwarding from the PO stage to the OF stage. The number of clock cycles taken for the execution of the above sequence of instruction is _____.

gate2015-cse-set2 co-and-architecture pipelining normal numerical-answers

Answer

1.18.24 Pipelining: GATE CSE 2015 Set 3 | Question: 51 [top](#)

<https://gateoverflow.in/8560>



Consider the following reservation table for a pipeline having three stages S_1 , S_2 and S_3 .

Time →					
	1	2	3	4	5
S_1	X				X
S_2		X		X	
S_3			X		

The minimum average latency (MAL) is _____.

gate2015-cse-set3 co-and-architecture pipelining difficult numerical-answers

Answer

1.18.25 Pipelining: GATE CSE 2016 Set 1 | Question: 32 [top](#)

<https://gateoverflow.in/39691>



The stage delays in a 4-stage pipeline are 800, 500, 400 and 300 picoseconds. The first stage (with delay 800 picoseconds) is replaced with a functionality equivalent design involving two stages with respective delays 600 and 350 picoseconds. The throughput increase of the pipeline is _____ percent.

gate2016-cse-set1 co-and-architecture pipelining normal numerical-answers

Answer

1.18.26 Pipelining: GATE CSE 2016 Set 2 | Question: 33 [top](#)

<https://gateoverflow.in/39580>



Consider a 3 GHz (gigahertz) processor with a three stage pipeline and stage

latencies τ_1 , τ_2 and τ_3 such that $\tau_1 = \frac{3\tau_2}{4} = 2\tau_3$.

If the longest pipeline stage is split into two pipeline stages of equal latency, the new frequency is _____ GHz, ignoring delays in the pipeline registers.

gate2016-cse-set2 co-and-architecture pipelining normal numerical-answers

Answer

1.18.27 Pipelining: GATE CSE 2017 Set 1 | Question: 50 [top](#)

<https://gateoverflow.in/118719>



Instruction execution in a processor is divided into 5 stages, *Instruction Fetch* (IF), *Instruction Decode* (ID), *Operand fetch* (OF), *Execute* (EX), and *Write Back* (WB). These stages take **5, 4, 20, 10 and 3 nanoseconds (ns)** respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of **2 ns**. Two pipelined implementation of the processor are contemplated:

- a naive pipeline implementation (NP) with 5 stages and
- an efficient pipeline (EP) where the OF stage is divided into stages $OF1$ and $OF2$ with execution times of **12 ns** and **8 ns** respectively.

The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is _____.

Answer 

1.18.28 Pipelining: GATE CSE 2018 | Question: 50 [top](#)

<https://gateoverflow.in/204125>



The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (*IF*), Instruction Decode (*ID*), Operand Fetch (*OF*), Perform Operation (*PO*) and Writeback (*WB*). The *IF*, *ID*, *OF* and *WB* stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the *PO* stage, 40 instructions take 3 clock cycles each, 35 instructions take 2 clock cycles each, and the remaining 25 instructions take 1 clock cycle each. Assume that there are no data hazards and no control hazards.

The number of clock cycles required for completion of execution of the sequence of instruction is _____.

Answer 

1.18.29 Pipelining: GATE CSE 2020 | Question: 43 [top](#)

<https://gateoverflow.in/333188>



Consider a non-pipelined processor operating at 2.5 GHz. It takes 5 clock cycles to complete an instruction. You are going to make a 5-stage pipeline out of this processor. Overheads associated with pipelining force you to operate the pipelined processor at 2 GHz. In a given program, assume that 30% are memory instructions, 60% are ALU instructions and the rest are branch instructions. 5% of the memory instructions cause stalls of 50 clock cycles each due to cache misses and 50% of the branch instructions cause stalls of 2 cycles each. Assume that there are no stalls associated with the execution of ALU instructions. For this program, the speedup achieved by the pipelined processor over the non-pipelined processor (round off to 2 decimal places) is _____.

Answer 

1.18.30 Pipelining: GATE CSE 2021 Set 1 | Question: 53 [top](#)

<https://gateoverflow.in/357398>



A five-stage pipeline has stage delays of 150, 120, 150, 160 and 140 nanoseconds. The registers that are used between the pipeline stages have a delay of 5 nanoseconds each. The total time to execute 100 independent instructions on this pipeline, assuming there are no pipeline stalls, is _____ nanoseconds.

Answer 

1.18.31 Pipelining: GATE IT 2004 | Question: 47 [top](#)

<https://gateoverflow.in/3690>



Consider a pipeline processor with 4 stages S_1 to S_4 . We want to execute the following loop:

```
for (i = 1; i <= 1000; i++)
    {I1, I2, I3, I4}
```

where the time taken (in ns) by instructions I_1 to I_4 for stages S_1 to S_4 are given below:

	S_1	S_2	S_3	S_4
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

The output of I_1 for $i = 2$ will be available after

- A. 11 ns
- B. 12 ns
- C. 13 ns
- D. 28 ns

Answer 



We have two designs $D1$ and $D2$ for a synchronous pipeline processor. $D1$ has 5 pipeline stages with execution times of 3 nsec, 2 nsec, 4 nsec, 2 nsec and 3 nsec while the design $D2$ has 8 pipeline stages each with 2 nsec execution time. How much time can be saved using design $D2$ over design $D1$ for executing 100 instructions?

- A. 214 nsec
- B. 202 nsec
- C. 86 nsec
- D. -200 nsec

gate2005-it co-and-architecture pipelining normal

goclasses.in

tests.gatecse.in

Answer



A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q)) / T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

```

ADD    R5, R0, R1    ; R5 ← R0 + R1
MUL    R6, R2, R5    ; R6 ← R2 * R5
SUB    R5, R3, R6    ; R5 ← R3 - R6
DIV    R6, R5, R4    ; R6 ← R5/R4
STORE  R6, X        ; X ← R6

```

The number of Read-After-Write (RAW) dependencies, Write-After-Read (WAR) dependencies, and Write-After-Write (WAW) dependencies in the sequence of instructions are, respectively,

- A. 2, 2, 4
- B. 3, 2, 3
- C. 4, 2, 2
- D. 3, 3, 2

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Answer



A pipelined processor uses a 4-stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage. The sequence of instructions corresponding to the statement $X = (S - R * (P + Q)) / T$ is given below. The values of variables P, Q, R, S and T are available in the registers $R0, R1, R2, R3$ and $R4$ respectively, before the execution of the instruction sequence.

```

ADD    R5, R0, R1    ; R5 ← R0 + R1
MUL    R6, R2, R5    ; R6 ← R2 * R5
SUB    R5, R3, R6    ; R5 ← R3 - R6
DIV    R6, R5, R4    ; R6 ← R5/R4
STORE  R6, X        ; X ← R6

```

The IF, ID and WB stages take 1 clock cycle each. The EX stage takes 1 clock cycle each for the ADD, SUB and STORE operations, and 3 clock cycles each for MUL and DIV operations. Operand forwarding from the EX stage to the ID stage is used. The number of clock cycles required to complete the sequence of instructions is

- A. 10
- B. 12
- C. 14
- D. 16

Answer

1.18.35 Pipelining: GATE IT 2007 | Question: 6, ISRO2011-25 [top](#)

<https://gateoverflow.in/3437>



A processor takes 12 cycles to complete an instruction I . The corresponding pipelined processor uses 6 stages with the execution times of 3, 2, 5, 4, 6 and 2 cycles respectively. What is the asymptotic speedup assuming that a very large number of instructions are to be executed?

- A. 1.83
- B. 2
- C. 3
- D. 6

Answer

1.18.36 Pipelining: GATE IT 2008 | Question: 40 [top](#)

<https://gateoverflow.in/3350>



A non pipelined single cycle processor operating at 100 MHz is converted into a synchronous pipelined processor with five stages requiring 2.5 nsec, 1.5 nsec, 2 nsec, 1.5 nsec and 2.5 nsec, respectively. The delay of the latches is 0.5 nsec. The speedup of the pipeline processor for a large number of instructions is:

- A. 4.5
- B. 4.0
- C. 3.33
- D. 3.0

Answer

Answers: Pipelining

1.18.1 Pipelining: GATE CSE 1999 | Question: 13 [top](#)

<https://gateoverflow.in/1512>



✓ Answer: 15 cycles are required.

	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}
I_1	F	D	D	E	W										
I_2		F	-	D	D	E	E	W							
I_3				F	F	D	-	E	E	E	W	W			
I_4						F	-	D	D	D	E	E	W		
I_5							F	-	-	-	D	D	E	W	W

37 votes

-- Amar Vashishth (25.2k points)

1.18.2 Pipelining: GATE CSE 2000 | Question: 1.8 [top](#)

<https://gateoverflow.in/631>



✓ Here we are comparing the execution time of only a single instruction. Pipelining in no way improves the execution time of a single instruction (the time from its start to end). It increases the overall performance by splitting the execution to multiple pipeline stages so that the following instructions can use the finished stages of the previous instructions. But in doing so, pipelining causes some problems also as given in the below link, which might slow some instructions. So, (B) is the answer.

<http://www.cs.wvu.edu/~jdm/classes/cs455/notes/tech/instrpipe.html>

References



54 votes

-- Arjun Suresh (332k points)

1.18.3 Pipelining: GATE CSE 2000 | Question: 12 top<https://gateoverflow.in/683>

✓ Each stage is $2ns$. So, after 5 time units each of $2ns$, the first instruction finishes (i.e., after $10ns$), in every $2ns$ after that a new instruction gets finished. This is assuming no branch instructions. Now, once the pipeline is full, we can assume that the initial fill time doesn't matter our calculations and average execution time for each instruction is $2ns$ assuming no branch instructions.

A. Now, we are given that 20% of instructions are branch (like JMP) and when a branch instruction is executed, no further instruction enters the pipeline. So, we can assume every 5th instruction is a branch instruction. So, with this assumption, total time to finish 5 instruction will be $5 * 2 + 8 = 18 ns$ (as when a branch instruction enters the pipeline and before it finishes, 4 pipeline stages will be empty totaling $4 * 2 = 8 ns$, as it is mentioned in question that the next instruction fetch starts only when branch instruction completes). And this is the same for every set of 5 instructions, and hence the average instruction execution time = $18/5 = 3.6 ns$

B. This is just a complex statement. But what we need is to identify the % of branch instructions which cause a branch to be taken as others will have no effect on the pipeline flow.
20% of instructions are branch instructions. 80% of branch instructions are conditional.
That means $.2 * .8 = 16%$ of instructions are conditional branch instructions and it is given that 50% of those result in a branch being taken.
So, 8% of instructions are conditional branches being taken and we also have 20% of 20% = 4% of unconditional branch instructions which are always taken.

So, percentage of instructions where a branch is taken is $8 + 4 = 12%$ instead of 20% in (A) part.

So, in 100 instructions there will be 12 branch instructions. We can do a different calculation here as compared to (A) as 12 is not a divisor of 100. Each branch instruction causes a pipeline delay of $4 * 2 = 8 ns$. So, 12 instructions will cause a delay of $12 * 8 = 96 ns$. For 100 instructions, we need $100 * 2 = 200 ns$ without any delay and with delay we require $200 + 96 = 296 ns$ for 100 instructions.

So, average instruction execution time = $296/100 = 2.96 ns$

(We can also use this method for part (A) which will give $100 * 2 + 20 * 8 = 360 ns$ for 100 instructions)

64 votes

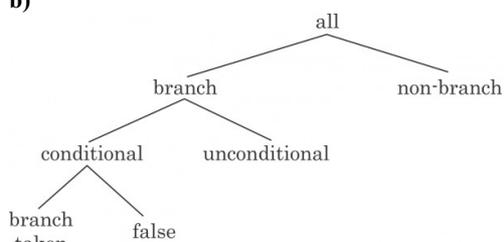
-- Arjun Suresh (332k points)

if an instruction branches then it takes $2ns \times 5 = 10ns$, coz if branch is taken then the instruction after that branch instruction is not fetched until entire current branch instruction is completed, this means it will go through all stages.

if an instruction is non-branch or branching does not happen then, it takes $2ns$ to get completed.

a) average time taken = $0.8 \times 2ns + 0.2 \times 10ns = 3.6ns$

b)



Average time taken,

$$= 0.8 \times 2ns + 0.2 \left(0.2 \times 10ns + 0.8 \left((0.5 \times 10ns + 0.5 \times 2ns) \right) \right)$$

$$= 2.96ns$$

1.18.4 Pipelining: GATE CSE 2001 | Question: 12

https://gateoverflow.in/753



✓ RAW dependencies:

1. $I_1 \leftarrow I_2$
2. $I_1 \leftarrow I_3$
3. $I_1 \leftarrow I_4$
4. $I_2 \leftarrow I_4$

WAR dependencies:

1. $I_2 \leftarrow I_1$
2. $I_4 \leftarrow I_1$
3. $I_4 \leftarrow I_2$

Consider a normal pipeline execution:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
I ₁	IF	ID	EX	MEM	WB			
I ₂		IF	ID	EX	MEM	WB		
I ₃			IF	ID	EX	MEM	WB	
I ₄				IF	ID	EX	MEM	WB

So, there are RAW hazards for I₂ and I₃ with I₁ and for I₄ with I₂. (Not all dependencies cause a hazard. Only if a dependency causes a stall in the given pipeline structure, we get a hazard) These hazards cause the following stalls in the pipeline:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁
I ₁	IF	ID	EX	MEM	WB						
I ₂		IF	–	–	ID	EX	MEM	WB			
I ₃			–	–	IF	ID	EX	MEM	WB		
I ₄				–	–	IF	–	ID	EX	MEM	WB

Now, with operand forwarding from EX – EX stage we can do as follows:

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
I ₁	IF	ID	EX ₁	MEM	WB			
I ₂		IF	ID	EX ₁	MEM	WB		
I ₃			IF	ID	EX ₃	MEM	WB	
I ₄				IF	ID	EX ₃	MEM	WB

Thus all hazards are eliminated.

Ref: <http://cseweb.ucsd.edu/classes/wi05/cse240a/pipe2.pdf>

References



1.18.5 Pipelining: GATE CSE 2002 | Question: 2.6, ISRO2008-19

https://gateoverflow.in/836



✓ Answer is D.

A: Yes. Total delay = Max (All delays) + Register Delay.

B: Yes, if data forwarding is not there.

C: Yes, like ID and EX shares ID/EX register.

👍 35 votes

-- Rajarshi Sarkar (27.9k points)

1.18.6 Pipelining: GATE CSE 2003 | Question: 10, ISRO-DEC2017-41 [top](#)

<https://gateoverflow.in/901>



- ✓ 1. Data hazard
- 2. Control hazard
- 3. Structural hazard as only one ALU is there

So, (D).

<http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/hazards.html>

References



👍 56 votes

-- Arjun Suresh (332k points)

1.18.7 Pipelining: GATE CSE 2004 | Question: 69 [top](#)

<https://gateoverflow.in/1063>



- ✓ Pipelining requires all stages to be synchronized meaning, we have to make the delay of all stages equal to the maximum pipeline stage delay which here is 160. We also have to add the intermediate register delay which here is $5ns$ which makes the clock period as $165ns$.

Time for execution of the first instruction = $165 * 4 = 660 ns$.

Now, in every 165 ns, an instruction can be completed. So,

Total time for 1000 instructions = $660 + 999 * 165 = 165.495$ microseconds

Correct Answer: C

👍 57 votes

-- Arjun Suresh (332k points)

1.18.8 Pipelining: GATE CSE 2005 | Question: 68 [top](#)

<https://gateoverflow.in/1391>



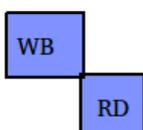
- ✓ Answer is option A.

Without data forwarding:

13 clock - WB and RD state non overlapping.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11	T12	T13
IF	RD	EX	MA	WB								
	IF				RD	EX	MA	WB				
					IF				RD	EX	MA	WB

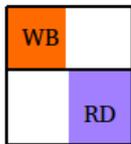
Here, WB and RD stage operate in Non-Overlapping mode.



11 clock - WB and RD states overlapping.

T1	T2	T3	T4	T5	T6	T7	T8	T9	T10	T11
IF	RD	EX	MA	WB						
	IF			RD	EX	MA	WB			
				IF			RD	EX	MA	WB

Split Phase access between WB and RD means:



WB stage produce the output during the rising edge of the clock and RD stage fetch the output during the falling edge.

In Question it is mentioned

! for write access, the register read at RD state is used.

This means that for writing operands back to memory, register read at RD state is used (no operand forward for STORE instructions).

Note

! As in any question in any subject unless otherwise stated we always consider the best case. So, do overlap - unless otherwise stated. But this is for only WB/RD

1. Why there is stall for I2 in T3 and T4 ?

RD is instruction decode and register read. IF we execute RD of I2 in T3, data from memory will not get stored to R0 hence proper operands are not available at T3. Perhaps I2 has to wait until I1 write values to memory.

2. WB of I1 and RD of I2 are operating in same clock why it is so ?

If nothing has mentioned in question. This scenario is taken into consideration by default. It is because after MA operands will be available in register so RD and WB could overlap.

With data forwarding

(Should be the case here as question says no operand forwarding for memory register for STORE instructions)

8 clock cycles

1	2	3	4	5	6	7	8	9
IF	RD	EX	MA	WB				
	IF	RD		EX	MA	WB		
		IF	RD	EX	MM	WB		

1. Why there is a stall I2 in T4 ?

Data is being forwarded from MA of I1 EX of I2 .MA operation of I1 must complete so that correct data will be available in register .

2. Why RD of I2 in T3 ? Will it not fetch incorrect information if executed before Operand are forwarded from MA of I1 ?

Yes. RD of I2 will definitely fetch INCORRECT data at T3 . But don't worry about it Operand Forwarding technique will take care of it .

3. Why can't RD of I2 be placed in T4 ?

Yes . We can place RD of I2 in T4 as well. But what is the fun in that ? pipeline is a technique used to reduce the execution time of instructions . Why do we need to make an extra stall ? Moreover there is one more problem which is discussed just below .After reading the below point Just think if we had created a stall at T3 !

4. **Why can't RD of I3 be placed at T4 ?**

This cannot be done . I3 cannot use RD because Previous instruction I2 should start next stage (EX) before current (I3) could utilize that(RD) stage . It is because data will be residing in buffers.

5. **Can an operand being forwarded from one clock cycle to same clock cycle ?**

No, the previous clock cycle must complete before data being forwarded . Unless split phase technique is used

6. **Can there be a forwarding from EX stage(T3) of I1 to EX stage(T4) of I2 ?**

This is not possible . See what is happening in I1 . It is Memory Read .So data will be available in register after memory read only .So data cannot be forwarded from EX of I1 .

7. **In some case data is forwarded from MA and some case data is forwarded from EX Why it is so ?**

Data is forwarded when it is ready . It solely depends on the type of instruction .

8. **When to use Split-Phase ?**

We can use split phase if data is readily available like between WB/RD and also when operand forwarding happens from EX-ID stage, but not from EX-EX stage. We cannot do split phase access between EX-EX because here the instruction execution may not be possible in the first phase. (This is not mentioned in any standard resource but said by Arjun Suresh by considering practical implementation and how previous year GATE questions have been formed)

[Mostly it is given in question that there is operand forwarding from A stage to B stage eg:https://gateoverflow.in/8218/gate2015-2_44]

Split-Phase can be used even when no Operand Forwarding because they aren't related.

References

- <http://web.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

Similar Questions

- https://gateoverflow.in/8218/gate2015-2_44
- <https://gateoverflow.in/2207/gate2010-33>
- <https://gateoverflow.in/34735/pipelining-without-operand-forwarding>

Discussions

- <https://gateoverflow.in/102565/operand-forwarding-in-pipeline>
- <https://gateoverflow.in/113244/doubts-in-pipelining>

References



👍 212 votes

-- Akhil Nadh PC (16.5k points)

1.18.9 Pipelining: GATE CSE 2006 | Question: 42 top 5

<https://gateoverflow.in/1818>



✓ Delay slots in the pipeline caused due to a branch instruction is 2 as after the 3rd stage of current instruction (during 4th stage) IF of next begins. Ideally, this should be during 2nd stage.

So, for total no. of instructions = 10^9 and 20% branch, we have $0.2 \times 2 \times 10^9 = 4 \times 10^8$ cycle penalty.

Since clock speed is 1 GHz and each instruction on average takes 1 cycle, total execution time in seconds will be

$$= \frac{10^9}{10^9} + 4 \times \frac{10^8}{10^9}$$

$$= 1.4$$

Correct Answer: C

👍 62 votes

-- Arjun Suresh (332k points)

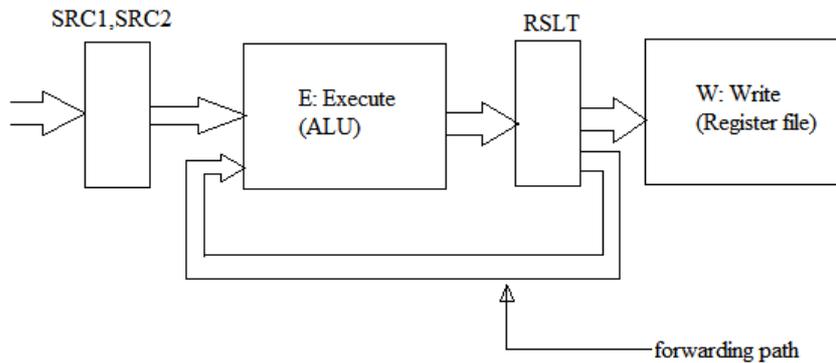


✓ **Answer: option B.**

Considering EX to EX data forwarding.

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
ADD	IF	ID	EX	WB				
MUL		IF	ID	EX	EX	EX	WB	
SUB			IF	ID			EX	WB

EX to EX data Forwarding:



Position of the source and result registers in the processor pipeline

47 votes

-- Rajarshi Sarkar (27.9k points)



✓ (B) I and III

I - False Bypassing can't handle all RAW hazard, consider when any instruction depends on the result of LOAD instruction, now LOAD updates register value at Memory Access Stage (MA), so data will not be available directly on Execute stage.

II - True, register renaming can eliminate all WAR Hazard.

III- False, It cannot completely eliminate, though it can reduce Control Hazard Penalties

81 votes

-- Prateeksha Keshari (1.7k points)



✓ Answer is A. In order to avoid the pipeline delay due to conditional branch instruction, a suitable instruction is placed below the conditional branch instruction such that the instruction will be executed irrespective of whether branch is taken or not and won't affect the program behaviour.

60 votes

-- Arjun Suresh (332k points)



✓ **What is Delayed Branching ?**

One way to maximize the use of the pipeline, is to find an instruction that can be safely executed whether the branch is taken or not, and execute that instruction. So, when a branch instruction is encountered, the hardware puts the instruction following the branch into the pipe and begins executing it, just as in predict-not-taken. However, unlike in predict-not-taken, we do not need to worry about whether the branch is taken or not, we do not need to clear the pipe because no matter whether the branch is taken or not, we know the instruction is safe to execute.

Moving I_1 after branch

- I_1 is updating the value of R_2
- R_2 which is used to determine branch condition R_1

- Value of $R2$ is available after branch
⇒ Cannot be moved

Moving I_3 after branch

- value of $R1$ is computed in this instruction
- $R1$ is the branch condition
⇒ Cannot be moved

Moving I_4 after branch

- I_4 is simple store instruction used to store $R1$ in memory
- program execution will have no effect if this is placed after conditional branch
⇒ Can be moved

Moving I_2 after branch

- It update the memory location to place the storing of conditional branch instruction $R1$
- If moved after branch, when compiler reaches I_4 program execution will stop
⇒ Cannot be moved

Hence, **option D is answer.**

👍 60 votes

-- Akhil Nadh PC (16.5k points)

1.18.14 Pipelining: GATE CSE 2009 | Question: 28 top

<https://gateoverflow.in/1314>



- ✓ Here bound of the loop are constants, therefore compiler will do the loop unrolling (If compiler won't then prefetcher will do) to increase the instruction level parallelism. And after loop unrolling 23 cycles are required for execution. Therefore, correct answer would be **(B)**.

PS: We assume the buffers between the pipeline stages can store multiple results in the form of a queue.

	C_1	C_2	C_3	C_4	C_5	C_6	C_7	C_8	C_9	C_{10}	C_{11}	C_{12}	C_{13}	C_{14}	C_{15}	C_{16}	C_{17}	C_{18}	C_{19}	C_{20}	C_{21}	C_{22}	C_{23}	
I_1	S_1	S_1	S_2	S_3	S_4																			
I_2			S_1	S_2	S_2	S_2	S_3	S_3	S_4	S_4														
I_3				S_1	S_1	-	S_2	-	S_3	-	S_4	S_4	S_4											
I_4						S_1	-	S_2	S_2	S_3	S_3	-	-	S_4	S_4									
I_1							S_1	S_1	-	S_2	S_2	S_2	S_3	S_3	-	S_4	S_4							
I_2									S_1	-	S_2	S_2	S_2	S_3	S_3	-	S_4	S_4						
I_3										S_1	S_1	-	-	S_2	-	S_3	-	-	S_4	S_4	S_4			
I_4												S_1	-	-	S_2	S_2	S_3	S_3	-	-	-	S_4	S_4	

👍 56 votes

-- suraj (4.8k points)

1.18.15 Pipelining: GATE CSE 2010 | Question: 33 top

<https://gateoverflow.in/2207>



	t_1	t_2	t_3	t_4	t_5	t_6	t_7	t_8	t_9	t_{10}	t_{11}	t_{12}	t_{13}	t_{14}	t_{15}
MUL	IF	ID	OF	PO	PO	PO	WO								
DIV		IF	ID	OF	-	-	PO	PO	PO	PO	PO	PO	WO		
ADD			IF	ID	-	-	OF	-	-	-	-	-	PO	WO	
SUB				IF	-	-	ID	-	-	-	-	-	OF	PO	WO

Operand forwarding allows an output to be passed for the next instruction. Here from the output of PO stage of DIV instruction operand is forwarded to the PO stage of ADD instruction and similarly between ADD and SUB instructions. Hence, 15 cycles required.

<http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

Correct Answer: B

References



64 votes

-- Arjun Suresh (332k points)

1.18.16 Pipelining: GATE CSE 2011 | Question: 41 [top](#)

<https://gateoverflow.in/2143>



✓ Answer is (B) 2.5

In pipeline system, Time taken is determined by the max delay at any stage i.e., 11 ns plus the delay incurred by pipeline stages i.e., 1 ns = 12 ns. In non-pipeline system,

Delay = 5 ns + 6 ns + 11 ns + 8 ns = 30 ns.

∴ The speedup is $\frac{30}{12} = 2.5$ ns.

53 votes

-- Sona Praneeth Akula (3.4k points)

1.18.17 Pipelining: GATE CSE 2012 | Question: 20, ISRO2016-23 [top](#)

<https://gateoverflow.in/52>



✓ Register renaming is done to eliminate WAR (Write after Read) and WAW (Write after Write) dependency between instructions which could have caused pipeline stalls. Hence, (C) is the answer.

Example:

I1: Read A to B

I2: Write C to A

Here, there is a WAR dependency and pipeline would need stalls. In order to avoid it register renaming is done and

Write C to A

will be

Write C to A'

WAR dependency is actually called anti-dependency and there is no real dependency except the fact that both uses same memory location. Register renaming can avoid this. Similarly WAW also.

<http://people.ee.duke.edu/~sorin/ece252/lectures/4.2-tomasulo.pdf>

References



52 votes

-- Arjun Suresh (332k points)

1.18.18 Pipelining: GATE CSE 2013 | Question: 45 [top](#)

<https://gateoverflow.in/330>



✓ After pipelining we have to adjust the stage delays such that no stage will be waiting for another to ensure smooth pipelining (continuous flow). Since we can not easily decrease the stage delay, we can increase all the stage delays to the maximum delay possible. So, here maximum delay is 10 ns. Buffer delay given is 1ns. So, each stage takes 11 ns in total.

FI of I9 can start only after the EI of I4. So, the total execution time will be

$$15 \times 11 = 165$$

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁	t ₁₂	t ₁₃	t ₁₄	t ₁₅
I1	FI	DI	FO	EI	WO										
I2		FI	DI	FO	EI	WO									
I3			FI	DI	FO	EI	WO								
I4				FI	DI	FO	EI	WO							
					stall										
						stall									
							stall								
I9								FI	DI	FO	EI	WO			
I10									FI	DI	FO	EI	WO		
I11										FI	DI	FO	EI	WO	
I12											FI	DI	FO	EI	WO

Correct Answer: B

👍 122 votes

-- gatecse (63.3k points)

1.18.19 Pipelining: GATE CSE 2014 Set 1 | Question: 43 [top](#)

<https://gateoverflow.in/1921>



✓ Time without pipeline = 6 stages = 6 cycles

Time with pipeline = 1 + stall frequency × stall cycle

$$= 1 + .25 \times 2$$

$$= 1.5$$

$$\text{Speed up} = \frac{6}{1.5} = 4$$

👍 64 votes

-- aravind90 (389 points)

1.18.20 Pipelining: GATE CSE 2014 Set 3 | Question: 43 [top](#)

<https://gateoverflow.in/2077>



✓ Five stages:

(IF), instruction decode and register fetch (ID/RF),

instruction execution (EX),

memory access (MEM), and register writeback (WB)

P old design:

with stage latencies 1 ns, 2.2 ns, 2 ns, 1 ns, and 0.75 ns

$$\text{MAX}(1 \text{ ns}, 2.2 \text{ ns}, 2 \text{ ns}, 1 \text{ ns}, \text{ and } 0.75 \text{ ns}) = 2.2 \text{ nsec}$$

AVG instruction execution time is

$$T_{\text{avg}} = (1 + \text{no of stalls} \times \text{branch penalty}) \times \text{cycle time}$$

$$= (1 + 0.20 \times 2) 2.2 \quad \{ \text{branch penalty is 2 because the next instruction pointer at the end of the EX stage in the old design.} \}$$

$$= 3.08 \text{ nsec}$$

Q :new DESIGN:

the designers decided to split the ID/RF stage into three stages (ID, RF1, RF2)

each of latency $\frac{2.2}{3}$ ns. Also, the EX stage is split into two stages

(EX1, EX2) each of latency 1 ns.

The new design has a total of eight pipeline stages.

$$\text{Time of stages in new design} = \{1 \text{ ns}, 0.73 \text{ ns}, 0.73 \text{ ns}, 0.73 \text{ ns}, 1 \text{ ns}, 1 \text{ ns}, 1 \text{ ns}, \text{ and } 0.75 \text{ ns}\}$$

(IF), instruction decode

register fetch (ID/RF) → further divided into 3 ie with latency 0.73 of each

instruction execution (EX) → further divided into 1 nsec of each)

memory access (MEM)

register writeback (WB)

MAX(1 ns, 0.73ns, 0.73ns, 0.73ns, 1ns, 1ns, 1 ns, and 0.75 ns) = 1 nsec

AVG instruction execution time is

$T_{avg} = (1 + \text{no of stalls} \times \text{branch penalty}) \times \text{cycle time}$

$= (1 + 0.20 \times 5) \times 1$ { branch penalty is 5 because the next instruction pointer at the end of the EX2 stage in the new design. }

$= 2 \text{ nsec}$

final result

$$\frac{P}{Q} = \frac{3.08}{2} = 1.54$$

👍 59 votes

-- kunal chalotra (13.6k points)

1.18.21 Pipelining: GATE CSE 2014 Set 3 | Question: 9 [top](#)

<https://gateoverflow.in/2043>



✓

$$\text{frequency} = \frac{1}{\max(\text{time in stages})}$$

for P_3 , it is $\frac{1}{1}$ GHz

for P_1 , it is $\frac{1}{2} = 0.5 \text{ GHz}$

for P_2 , it is $\frac{1}{1.5} = 0.67 \text{ GHz}$

for P_4 , it is $\frac{1}{1.1} \text{ GHz}$

Correct Answer: C

👍 41 votes

-- Arpit Dhuriya (2.9k points)

1.18.22 Pipelining: GATE CSE 2015 Set 1 | Question: 38 [top](#)

<https://gateoverflow.in/8288>



✓ Answer = 3.2.

To compute cycle time, we know that a 2.5 GHz processor means it completes 2.5 billion cycles in a second. So, for an instruction which on an average takes 4 cycles to get completed, it will take $\frac{4}{2.5}$ nanoseconds.

On a perfect pipeline (i.e., one which has no stalls) $CPI = 1$ as during it an instruction takes just one cycle time to get completed.

So,

$$\text{Speed Up} = \frac{\text{Old Execution Time of an Instruction}}{\text{New Execution Time of an Instruction}}$$

$$= \frac{CPI_{old} / CF_{old}}{CPI_{new} / CF_{new}}$$

$$= \frac{4 / 2.5 \text{ GHz}}{1 / 2 \text{ GHz}}$$

$$= 3.2$$

👍 87 votes

-- naresh1845 (1.1k points)

$$\text{Speed up} = \frac{\text{Old execution time}}{\text{New execution time}}$$

$$\text{Old execution time} = \frac{\text{CPI}}{2.5} = \frac{4}{2.5} = 1.6 \text{ ns}$$

With pipelining,

$$= \frac{\text{each instruction needs old execution time} \times \text{old frequency}}{\text{new frequency (without pipelining)}}$$

$$= \frac{1.6 \times 2.5}{2} = 2 \text{ ns}$$

There are 5 stages and when there is no pipeline stall, this can give a speed up of up to 5 (happens when all stages take same number of cycles).

In our case this time will be $\frac{2}{5} = 0.4 \text{ ns}$.

But clock frequency being 2 GHz, clock cycle is $\frac{1}{2} \text{ GHz} = 0.5 \text{ ns}$ and a pipeline stage cannot be faster than this.

So, average instruction execution time after pipelining = $\max(0.4, 0.5) = 0.5 \text{ ns}$.

$$\text{So, speed up compared to non-pipelined version} = \frac{1.6}{0.5} = 3.2$$

35 votes

-- Arjun Suresh (332k points)

1.18.23 Pipelining: GATE CSE 2015 Set 2 | Question: 44

<https://gateoverflow.in/8218>



✓

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁	t ₁₂	t ₁₃	t ₁₄	t ₁₅
I1	IF	OF	PO	PO	PO	WB									
I2		IF	OF	-	-	PO	PO	PO	PO	PO	WB				
I3			IF	-	-	-	-	-	-	-	OF	PO	WB		
I4				-	-	-	-	-	-	-	IF	-	OF	PO	WB

It is mentioned in the question that operand forwarding takes place from PO stage to OF stage and not to PO stage. So, 15 clock cycles.

But since operand forwarding is from PO-OF, we can do like make the PO stage produce the output during the rising edge of the clock and OF stage fetch the output during the falling edge. This would mean the final PO stage and OF stage can be done in one clock cycle making the total number of cycles = 13. And 13 is the answer given in GATE key.

	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈	t ₉	t ₁₀	t ₁₁	t ₁₂	t ₁₃
I1	IF	OF	PO	PO	PO	WB							
I2		IF	OF	-	-	PO	PO	PO	PO	PO	WB		
I3			IF	-	-	-	-	-	-	-	OF	PO	WB
I4				-	-	-	-	-	-	-	IF	OF	PO

Reference: <http://www.cs.iastate.edu/~prabhu/Tutorial/PIPELINE/forward.html>

References



92 votes

-- Arjun Suresh (332k points)



✓ Reference: Page 24 <http://www2.cs.siu.edu/~cs401/Textbook/ch3.pdf>

S_1 is needed at time 1 and 5, so its forbidden latency is $5 - 1 = 4$.

S_2 is needed at time 2 and 4, so its forbidden latency is $4 - 2 = 2$.

So, forbidden latency = (2, 4, 0) (0 by default is forbidden)

Allowed latency = (1, 3, 5) (any value more than 5 also).

Collision vector (4, 3, 2, 1, 0) = 10101 which is the initial state as well.

From initial state we can have a transition after "1" or "3" cycles and we reach new states with collision vectors (10101 >> 1 + 10101 = 11111) and (10101 >> 3 + 10101 = 10111) respectively.

These 2 becomes states 2 and 3 respectively. For "5" cycles we come back to state 1 itself.

From state 2 (11111), the new collision vector is 11111. We can have a transition only when we see the first 0 from the right.

So, here it happens on 5th cycle only which goes to the initial state. (Any transition after 5 or more cycles goes to initial state as we have 5 time slices).

From state 3 (10111), the new collision vector is 10111. So, we can have a transition on 3, which will give (10111 >> 3 + 10101 = 10111) third state itself. For 5, we get the initial state. Thus all the transitions are complete.

State \ Time	1	3	5
1(10101)	2	3	1
2(11111)	-	-	1
3(10111)	-	3	1

So, minimum length cycle is of length 3 either from 3-3 or from 1-3,3-1.

Not asked in the question, still.

Pipeline throughput is the number of instructions initiated per unit time.

So, with $MAL = 3$, we have 2 initiations in $1 + 3 = 4$ units of time (one at time unit 1 and another at time unit 4). So,

$$\text{throughput} = \frac{2}{4} = 0.5.$$

Pipeline efficiency is the % of time every stage of the pipeline is being used.

For the given question we can extend the reservation table and taking $MAL = 3$, we can initiate new tasks after every 3 cycles.

So, we can consider the time interval from 4-6 in the below figure. (The red color shows a stage not being used- affects efficiency).

Time →	1	2	3	4	5	6	7	8	9	10	11
S_1	X			Y	X	×	Z	Y	×	A	Z
S_2		X		X	Y	×	Y	Z		Z	A
S_3			X	×	×	Y			Z		

Here (during cycles 4 - 6), stage 1 is used $\frac{2}{3}$, stage 2 is used $\frac{2}{3}$ and stage 3 is used $\frac{1}{3}$.

$$\text{So, total stage utilization} = \frac{(2 + 2 + 1)}{9} = \frac{5}{9} \text{ and efficiency} = \frac{500}{9}\% = 55.55\%$$

For simulation, Reference: <http://www.ecs.umass.edu/ece/koren/architecture/ResTable/SimpRes/>

Similar Question

- <https://gateoverflow.in/77125/advanced-computer-architecture-collision-vector-pipeline>

References



44 votes

-- Arjun Suresh (332k points)



- ✓ In pipeline ideally $CPI = 1$
 So in 1 cycle 1 instruction gets completed
 Throughout is instructions in unit time
 In pipeline 1, cycle time = max stage delay = 800 psec
 In 800 psec, we expect to finish 1 instruction
 So, in 1ps, $\frac{1}{800}$ instructions are expected to be completed, which is also the throughput for pipeline 1.

Similarly pipeline 2, throughput = $\frac{1}{600}$
 Throughput increase in percentage

$$= \frac{\text{new-old}}{\text{old}} \times 100$$

$$= \frac{\frac{1}{600} - \frac{1}{800}}{\frac{1}{800}} \times 100$$

$$= \frac{200}{600} \times 100$$

$$= 33.33\%$$

👍 116 votes

-- Anurag Semwal (6.7k points)

! Maximum throughput of a Pipeline i.e in best case without any stalls is equal to Clock Frequency of the pipeline

In first case Clock cycle time = Max Stage Delay = Max(800,500,400 and 300) = 800.

So clock Frequency = $\frac{1}{800}$ (Ignore the units as we have to calculate percentage only)

In Second Case Clock cycle time = Max(600,350,500,400 and 300) = 600.

So clock Frequency = $\frac{1}{600}$.

Percentage increase in throughput of pipeline = percentage in Clock Frequency

$$= \frac{\left(\frac{1}{600} - \frac{1}{800}\right)}{\frac{1}{800}} \times 100 = 33.33\%$$

👍 40 votes

-- Mehak Sharma (1.2k points)



- ✓ **Answer is 4 GHz.**
 Given 3 stage pipeline, with 3 GHz processor.

$$\text{Given, } e_1 = \frac{3e_2}{4} = 2e_3$$

$$\text{Put } e_1 = 6x$$

$$\text{we get, } e_2 = 8x, e_3 = 3x$$

Now largest stage time is 8x.

So, frequency is $\frac{1}{8x}$

$$\Rightarrow \frac{1}{8x} = 3\text{GHz}$$

$$\Rightarrow \frac{1}{x} = 24\text{ GHz} \dots (1)$$

Now, we divide e_2 into two stages of $4x$ & $4x$.

New processor has 4 stages -

$6x, 4x, 4x, 3x$.

Now largest stage time is $6x$.

So, new frequency is

$$\frac{1}{6x} = \frac{24}{6} = 4\text{ GHz (Ans)} \dots \text{from (1)}$$

👍 131 votes

-- Himanshu Agarwal (12.4k points)

1.18.27 Pipelining: GATE CSE 2017 Set 1 | Question: 50 [top](#)

<https://gateoverflow.in/118719>



✓ CASE 1

Stages 5, max delay = 22 (after adding buffer delay), number of instructions = 20

CASE 2

Stages 6, (since OF is split), max delay = 14, number of instructions = 20

So, execution time is $(K + N - 1) \times \text{Max delay}$

$$\text{Speed Up} = \frac{528}{350} = 1.508 \text{ (Execution time case 1/Execution time case 2)}$$

So, answer is **1.508**

👍 42 votes

-- sriv_shubham (2.8k points)

1.18.28 Pipelining: GATE CSE 2018 | Question: 50 [top](#)

<https://gateoverflow.in/204125>



✓ Total Instruction = 100

Number of stages = 5

In normal case total cycles = $100 + 5 - 1 = 104$ cycles

Now, For PO stage 40 instructions take 3 cycles, 35 take 2 cycles and rest of the 25 take 1 cycle.

That means all other stages are perfectly fine and working with CPI (Clock Cycle Per Instruction) = 1

PO stage:

40 instructions take 3 cycles i.e. these instructions are suffering from 2 stall cycle,

35 instructions take 2 cycles i.e. these instructions are suffering from 1 stall cycle,

25 instructions take 1 cycles i.e. these instructions are suffering from 0 stall cycle,

So, extra cycle would be $40 * 2 + 35 * 1 + 25 * 0 = 80 + 35 = 115$ cycle.

Total cycles = $104 + 115 = 219$

👍 114 votes

-- Digvijay (44.9k points)

1.18.29 Pipelining: GATE CSE 2020 | Question: 43 [top](#)

<https://gateoverflow.in/333188>



✓ Time taken by non-pipelined processor to finish executing the n instructions : $\frac{5n}{2.5} = 2n$ ns

Now, for pipelined processor,

Instruction type	Number of such instructions	%Causing stalls	Number of stall cycles
Memory	$0.3n$	5% of $0.3n$	50
ALU	$0.6n$	None	0
Branch	$0.1n$	50% of $0.1n$	2

Therefore, time taken by pipelined processor:

$$0.6n(1) + 0.3n[0.05(1 + 50) + 0.95(1)] + 0.1n[0.5(1 + 2) + 0.5(1)] \text{ cycles}$$

$$= 1.85n \text{ cycles}$$

$$= \frac{1.85n}{2} \text{ ns}$$

$$= 0.925n \text{ ns}$$

$$\text{Speedup} = \frac{2n}{0.925n} = 2.162 \approx 2.16.$$

👍 19 votes

-- Debasish Das (1.5k points)

1.18.30 Pipelining: GATE CSE 2021 Set 1 | Question: 53 [top](#)

<https://gateoverflow.in/357398>



✓ For the given pipelined system:

- Total number of stages (k) = 4
- Total number of instructions, (n) = 100
- Total delay (t_p) = max(stage delay) + buffer delay
 - $\Rightarrow t_p = \max(150, 120, 150, 160, 140) + 5 \text{ ns}$
 - $\Rightarrow t_p = 160 + 5 \text{ ns}$
 - $\Rightarrow t_p = 165 \text{ ns}$

$$ET_p = [(k + (n - 1)) * t_p]$$

$$\Rightarrow ET_p = [(5 + (100 - 1)) * 165] \text{ ns}$$

$$\Rightarrow ET_p = (5 + 99) * 165 \text{ ns}$$

$$\Rightarrow ET_{\text{pipeline}} = 17160 \text{ ns}$$

∴ To execute 100 instructions in the given pipeline, 17160 ns time is required.

👍 2 votes

-- Hira (14.1k points)

1.18.31 Pipelining: GATE IT 2004 | Question: 47 [top](#)

<https://gateoverflow.in/3690>



✓

	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13
I1	s ₁	s ₂	s ₂	s ₃	s ₄	s ₄							
I2		s ₁	s ₁	s ₂	s ₃	s ₃	s ₄						
I3				s ₁	s ₂	--	s ₃	s ₃	s ₄				
I4					s ₁	s ₁	s ₂	--	s ₃	s ₃	s ₄		
I5							s ₁	--	s ₂	s ₂	s ₃	s ₄	s ₄

So, total time would be 13 ns

Option (c).

👍 47 votes

-- Suvojit Mondal (291 points)

1.18.32 Pipelining: GATE IT 2005 | Question: 44 [top](#)

<https://gateoverflow.in/3805>



✓ (B) is the correct option for this question.

Execution time for Pipeline = $(K + n - 1) * \text{execution_time}$ where k = no of stages in pipeline, n = no of instructions

Execution time = max(all stages execution time)

$$D_1 = (5 + 100 - 1) * 4 = 416$$

$$D_2 = (8 + 100 - 1) * 2 = 214$$

$$\text{Time saved using } D_2 = 416 - 214 = 202$$

👍 30 votes

-- Manu Thakur (34k points)

1.18.33 Pipelining: GATE IT 2006 | Question: 78 [top](#)

<https://gateoverflow.in/3622>



✓ (C) is the correct option for this question:

RAW

1. I1 - I2 (R5)
2. I2 - I3 (R6)
3. I3 - I4 (R5)
4. I4 - I5 (R6)

WAR

1. I2 - I3 (R5)
2. I3 - I4 (R6)

WAW

1. I1 - I3 (R5)
2. I2 - I4 (R6)

👍 51 votes

-- Manu Thakur (34k points)

1.18.34 Pipelining: GATE IT 2006 | Question: 79 [top](#)

<https://gateoverflow.in/3623>



✓

	C ₁	C ₂	C ₃	C ₄	C ₅	C ₆	C ₇	C ₈	C ₉	C ₁₀	C ₁₁	C ₁₂
ADD	IF	ID	EX ①	WB								
MUL		IF	ID ①	EX	EX	EX ①	WB					
SUB			IF	-	-	ID ①	EX ①	WB				
DIV						IF	ID ①	EX	EX	EX ①	WB	
STORE							IF	-	-	ID ①	EX	WB

- Stalls

① Operand forwarding from EX-ID using split phase

So, answer is 12.

Correct Answer: B

👍 75 votes

-- Manu Thakur (34k points)

1.18.35 Pipelining: GATE IT 2007 | Question: 6, ISRO2011-25 [top](#)

<https://gateoverflow.in/3437>



✓ For non pipeline processor we have n instruction and each instruction take 12 cycle so total 12n instruction.

For pipeline processor we have each stage strict to 6ns so time to complete

the n instruction is $6 \times 6 + (n - 1) \times 6$.

$$\lim_{n \rightarrow \infty} \frac{12n}{36 + (n - 1) \times 6} = \frac{12}{6} = 2.$$

Correct Answer: *B*

👍 62 votes

-- Arpit Dhuriya (2.9k points)

1.18.36 Pipelining: GATE IT 2008 | Question: 40 [top](#)

<https://gateoverflow.in/3350>



✓ Here we have to keep in mind the phrase:

A non-pipelined single cycle processor

This signifies that instruction in a non pipelined scenario is incurring only a single cycle to execute entire instruction. Hence no concept of stage comes in case of single cycle non pipelined system.

The cycle time can be calculated from clock frequency given in non pipelined system = 100 MHz

$$\text{Therefore clock cycle time in non pipelined system} = \frac{1}{(100 \times 10^6)} \text{sec}$$

$$= 10 \text{ ns}$$

Now cycle time in pipelined system = max(stage delay + interface delay)

$$= 2.5 + 0.5 = 3 \text{ ns}$$

Therefore,

$$\text{Speedup} = \frac{CPI_{\text{non pipeline}} \times \text{Cycle time}_{\text{non pipeline}}}{(CPI_{\text{pipeline}} \times \text{Cycle time}_{\text{pipeline}})}$$

$$= \frac{1 \times 10}{(1 \times 3)} = 3.33$$

[Since in case of non pipeline we have single cycle processor, so $CPI_{\text{non pipeline}} = 1$ and CPI_{pipeline} by default = 1]

Hence, (C) is the correct answer.

👍 63 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

1.19

Runtime Environments (2) [top](#)

1.19.1 Runtime Environments: GATE CSE 2001 | Question: 1.10, UGCNET-Dec2012-III: 36 [top](#)

<https://gateoverflow.in/703>



Suppose a processor does not have any stack pointer registers, which of the following statements is true?

- A. It cannot have subroutine call instruction
- B. It cannot have nested subroutines call
- C. Interrupts are not possible
- D. All subroutine calls and interrupts are possible

gate2001-cse co-and-architecture normal ugcnetdec2012iii runtime-environments

Answer 🗣️

1.19.2 Runtime Environments: GATE CSE 2008 | Question: 37, ISRO2009-38 [top](#)

<https://gateoverflow.in/448>



The use of multiple register windows with overlap causes a reduction in the number of memory accesses for:

- I. Function locals and parameters
 - II. Register saves and restores
 - III. Instruction fetches
- A. I only

- B. *II* only
- C. *III* only
- D. *I, II* and *III*

gate2008-cse co-and-architecture normal isro2009 runtime-environments

Answer

Answers: Runtime Environments

1.19.1 Runtime Environments: GATE CSE 2001 | Question: 1.10, UGCNET-Dec2012-III: 36 top

<https://gateoverflow.in/703>



✓ A stack pointer is a small register that stores the address of the **last program request in a stack**.

And a nested function (or nested procedure or subroutine) is a function which is defined **within another function**, the enclosing function. So if there is no stack pointer register then No nested subroutine call possible, hence option B is correct.

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-- Bikram (58.4k points)

1.19.2 Runtime Environments: GATE CSE 2008 | Question: 37, ISRO2009-38 top

<https://gateoverflow.in/448>



✓ I. Functions locals and parameters
this is true because overlapped registers eliminates the need for memory accesses. we here got to use registers instead.

II. Register saves and restores
this is false bc we need to see where memory accesses are reduced here before also we were using register as it says Register saves... later also (i.e. after using multiple register windows) registers will are referred. So NO memory accesses are reduced here.

III. Instruction fetches
it has nothing to do with reduction in memory accesses.

Hence, **option (A)** is correct.

38 votes

-- Amar Vashishth (25.2k points)

1.20

Speedup (2) top

1.20.1 Speedup: GATE CSE 2014 Set 1 | Question: 55 top

<https://gateoverflow.in/1935>



Consider two processors P_1 and P_2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P_2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P_1 . If the clock frequency of P_1 is 1GHZ, then the clock frequency of P_2 (in GHZ) is _____.

gate2014-cse-set1 co-and-architecture numerical-answers normal speedup

Answer

1.20.2 Speedup: GATE IT 2004 | Question: 50 top

<https://gateoverflow.in/790>



In an enhancement of a design of a CPU, the speed of a floating point unit has been increased by 20% and the speed of a fixed point unit has been increased by 10%. What is the overall speedup achieved if the ratio of the number of floating point operations to the number of fixed point operations is 2 : 3 and the floating point operation used to take twice the time taken by the fixed point operation in the original design?

- A. 1.155
- B. 1.185
- C. 1.255
- D. 1.285

gate2004-it normal co-and-architecture speedup

Answer

Answers: Speedup



- ✓ CPU TIME (T) = No. of Instructions (I) × No. of Cycles Per Instruction (c) × Cycle Time (t)

OR

$$\text{CPU TIME (T)} = \frac{\text{No. of Instructions (I)} \times \text{No. of Cycles Per Instruction (c)}}{\text{Clock frequency (f)}}$$

$$\rightarrow T = I_c \times CPI \times F^{-1}$$

$$\rightarrow \frac{T \times F}{CPI} = I_c$$

P_1 & P_2 executing same instruction set So,
No. of Instructions same for both = $I_1 = I_2 = I$

If P_1 takes T_1 time,

$$\rightarrow T_2 = 0.75 \times T_1 \rightarrow \frac{T_2}{T_1} = 0.75$$

If P_1 incurs C_1 clock cycles per instruction,

$$\rightarrow C_2 = 1.2 \times C_1 \rightarrow \frac{C_2}{C_1} = 1.2$$

Since I is same for both,

$$\rightarrow \frac{(f_1 \times T_1)}{c_1} = \frac{(f_2 \times T_2)}{c_2} \text{ and } f_1 = 1 \text{ GHz}$$

$$\rightarrow F_2 = \left(\frac{C_2}{C_1}\right) \times \left(\frac{T_1}{T_2}\right) \times F_1$$

$$= \frac{1.2 \times 1 \text{ GHz}}{0.75} = 1.6 \text{ GHz}$$

Hence, the clock frequency of P_2 is = 1.6 GHz.

👍 85 votes

-- Suraj Kaushal (273 points)

Execution time (T) = CPI * #instructions * time for a clock
= CPI * #instructions / clock frequency (F)

Given P_1 and P_2 execute the same set of instructions and

$$T_2 = 0.75 T_1,$$

$$CPI_2 = 1.2 CPI_1 \text{ and}$$

$$F_1 = 1 \text{ GHz.}$$

So,

$$\frac{T_1}{CPI_1} \times F_1 = \frac{T_2}{CPI_2} \times F_2$$

$$\frac{T_1}{CPI_1} \times 1 \text{ GHz} = \frac{0.75 T_1}{1.2 CPI_1} \times F_2$$

$$\Rightarrow F_2 = \frac{1.2}{0.75} \text{ GHz}$$

$$= 1.6 \text{ GHz}$$

👍 37 votes

-- Arjun Suresh (332k points)



✓
$$\text{SpeedUp} = \frac{\text{Original time taken}}{\text{new time taken}}$$

Let x be the time for a fixed point operation,

$$\text{Original time taken} = \frac{(3x + 2 \times 2x)}{5} = \frac{7x}{5}$$

$$\text{New time taken} = \frac{\left(\frac{3x}{1.1} + \frac{4x}{1.2}\right)}{5} = \frac{8x}{1.32 \times 5}$$

$$\text{So, SpeedUp} = \frac{7 \times 1.32}{8} = 1.155$$

Correct Answer: A

👍 56 votes

-- gatecse (63.3k points)

1.21

Virtual Memory (3) top ⤴

1.21.1 Virtual Memory: GATE CSE 1991 | Question: 03,iii top ⤴

https://gateoverflow.in/517



The total size of address space in a virtual memory system is limited by:

- A. the length of MAR
- B. the available secondary storage
- C. the available main memory
- D. all of the above
- E. none of the above

gate1991 co-and-architecture virtual-memory normal multiple-selects

Answer 🗃

1.21.2 Virtual Memory: GATE CSE 2004 | Question: 47 top ⤴

https://gateoverflow.in/318



Consider a system with a two-level paging scheme in which a regular memory access takes 150 *nanoseconds*, and servicing a page fault takes 8 *milliseconds*. An average instruction takes 100 nanoseconds of CPU time, and two memory accesses. The TLB hit ratio is 90%, and the page fault rate is one in every 10,000 instructions. What is the effective average instruction execution time?

- A. 645 nanoseconds
- B. 1050 nanoseconds
- C. 1215 nanoseconds
- D. 1230 nanoseconds

gate2004-cse co-and-architecture virtual-memory normal

Answer 🗃

1.21.3 Virtual Memory: GATE CSE 2008 | Question: 38 top ⤴

https://gateoverflow.in/449



In an instruction execution pipeline, the earliest that the data TLB (Translation Lookaside Buffer) can be accessed is:

- A. before effective address calculation has started
- B. during effective address calculation
- C. after effective address calculation has completed
- D. after data cache lookup has completed

gate2008-cse co-and-architecture virtual-memory normal

Answer 🗃

Answers: Virtual Memory



✓ The answer is (A) and (B).

Virtual memory concept is independent of size of main memory and depends only on the availability of the secondary storage.

MAR holds the address generated by CPU and this obviously limits the total virtual memory address space.

👍 34 votes

-- Kalpna Bhargav (2.5k points)



✓ Average Instruction execution time

= Average CPU execution time + Average time for getting data(instruction operands from memory for each instruction)

= Average CPU execution time
+ Average address translation time for each instruction
+ Average memory fetch time for each instruction
+ Average page fault time for each instruction

$$= 100 + 2 \left((0.9(0) + 0.1(2 \times 150)) \right) + 2 \times 150 + \frac{1}{10000} \times 8 \times 10^6$$

(Page Fault Rate per 10,000 instruction is directly given in question. Two memory accesses per instruction and hence we need 2 × address translation time for average instruction execution time)

[TLB access time assumed as 0 and 2 page tables need to be accessed in case of TLB miss as the system uses two-level paging]

$$= 100 + 60 + 300 + 800$$

$$= 1260ns$$

👍 140 votes

-- Arjun Suresh (332k points)



✓ C is the answer here.

Effective address is the address after applying the addressing mode like indexed, immediate etc. But this resulting address is still the virtual address, the physical address is invisible to the CPU and will be given only by the MMU when given the corresponding virtual address. Virtual address is given for TLB look up. TLB -Translation Lookaside Buffer, here Lookaside means during Address translation (from Virtual to Physical). But virtual address must be there before we look into TLB.

https://gateoverflow.in/?qa=blob&qa_blobid=15279338060050073946

References



👍 57 votes

-- Arjun Suresh (332k points)

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Answer Keys

1.1.1	C	1.1.2	N/A	1.1.3	N/A	1.1.4	N/A	1.1.5	B
1.1.6	D	1.1.7	A;B;C;D	1.1.8	C	1.1.9	A	1.1.10	B

1.1.11	C	1.1.12	B	1.1.13	C	1.1.14	C	1.1.15	D
1.1.16	D	1.1.17	D	1.1.18	D	1.2.1	N/A	1.2.2	N/A
1.2.3	22	1.2.4	180	1.2.5	N/A	1.2.6	D	1.2.7	D
1.2.8	61.25	1.2.9	N/A	1.2.10	B	1.2.11	B	1.2.12	N/A
1.2.13	N/A	1.2.14	C	1.2.15	A	1.2.16	A	1.2.17	D
1.2.18	C	1.2.19	B	1.2.20	D	1.2.21	C	1.2.22	A
1.2.23	A	1.2.24	D	1.2.25	B	1.2.26	C	1.2.27	D
1.2.28	C	1.2.29	C	1.2.30	D	1.2.31	C	1.2.32	A
1.2.33	A	1.2.34	A	1.2.35	D	1.2.36	D	1.2.37	20
1.2.38	1.68	1.2.39	14	1.2.40	A	1.2.41	24	1.2.42	30
1.2.43	0.05	1.2.44	14	1.2.45	A	1.2.46	4.7 : 4.8	1.2.47	18
1.2.48	B	1.2.49	D	1.2.50	160	1.2.51	13.49:13.59	1.2.52	B
1.2.53	17 : 17	1.2.54	2 : 2	1.2.55	A	1.2.56	C	1.2.57	B
1.2.58	C	1.2.59	C	1.2.60	A	1.2.61	B	1.2.62	D
1.2.63	A	1.3.1	A;B;C;D	1.3.2	D	1.4.1	N/A	1.4.2	B
1.5.1	76	1.6.1	B	1.7.1	B	1.7.2	B	1.8.1	N/A
1.8.2	D	1.8.3	B	1.8.4	B	1.8.5	28	1.8.6	C
1.9.1	D	1.9.2	B	1.9.3	A	1.9.4	456	1.9.5	80000 : 80000
1.9.6	C	1.10.1	A	1.11.1	False	1.11.2	N/A	1.11.3	C
1.11.4	C	1.11.5	A	1.11.6	-16.0	1.11.7	1.87 : 1.88	1.12.1	N/A
1.12.2	256	1.12.3	True	1.12.4	16383	1.12.5	500	1.12.6	32
1.12.7	14	1.13.1	D	1.13.2	B	1.13.3	A	1.13.4	A
1.13.5	B	1.13.6	C	1.13.7	C	1.14.1	True	1.14.2	True
1.14.3	False	1.14.4	A	1.14.5	1.4 : 1.5	1.14.6	B	1.14.7	B
1.15.1	N/A	1.15.2	N/A	1.15.3	N/A	1.15.4	B	1.15.5	A
1.15.6	D	1.15.7	B	1.15.8	C	1.15.9	B	1.15.10	D
1.15.11	A	1.15.12	C	1.15.13	D	1.15.14	D	1.15.15	16
1.15.16	50 : 50	1.15.17	D	1.15.18	C	1.15.19	A	1.16.1	31
1.16.2	59 : 60	1.17.1	N/A	1.17.2	C	1.17.3	C	1.17.4	B
1.17.5	D	1.17.6	A	1.17.7	D	1.17.8	A	1.17.9	D
1.17.10	B	1.17.11	D	1.17.12	D	1.18.1	15	1.18.2	B
1.18.3	N/A	1.18.4	N/A	1.18.5	D	1.18.6	D	1.18.7	C
1.18.8	A	1.18.9	C	1.18.10	B	1.18.11	B	1.18.12	A
1.18.13	D	1.18.14	B	1.18.15	B	1.18.16	B	1.18.17	C

1.18.18	B
1.18.23	13
1.18.28	219
1.18.33	C
1.19.2	A

1.18.19	4
1.18.24	3
1.18.29	2.161:2.169
1.18.34	B
1.20.1	1.6

1.18.20	1.50 : 1.60
1.18.25	33.0 : 34.0
1.18.30	17160 : 17160
1.18.35	B
1.20.2	A

1.18.21	C
1.18.26	4
1.18.31	C
1.18.36	C
1.21.1	A;B

1.18.22	3.2
1.18.27	1.50 : 1.51
1.18.32	B
1.19.1	X
1.21.2	D

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Concept of layering. OSI and TCP/IP Protocol Stacks; Basics of packet, circuit and virtual circuit-switching; Data link layer: framing, error detection, Medium Access Control, Ethernet bridging; Routing protocols: shortest path, flooding, distance vector and link state routing; Fragmentation and IP addressing, IPv4, CIDR notation, Basics of IP support protocols (ARP, DHCP, ICMP), Network Address Translation (NAT); Transport layer: flow control and congestion control, UDP, TCP, sockets; Application layer protocols: DNS, SMTP, HTTP, FTP, **Email**.

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	1	1	2	1	3	2	3	2	3	1	2	3
2 Marks Count	4	3	2	4	2	3	1	4	3	1	2.8	4
Total Marks	9	7	6	9	7	8	5	10	9	5	7.7	10

2.1

Application Layer Protocols (10) top2.1.1 Application Layer Protocols: GATE CSE 2008 | Question: 14, ISRO2016-74 top
<https://gateoverflow.in/412>


What is the maximum size of data that the application layer can pass on to the TCP layer below?

- A. Any size
- B. 2^{16} bytes - size of TCP header
- C. 2^{16} bytes
- D. 1500 bytes

gate2008-cse easy computer-networks application-layer-protocols isro2016

Answer ⬇

2.1.2 Application Layer Protocols: GATE CSE 2011 | Question: 4 top
<https://gateoverflow.in/2106>


Consider the different activities related to email.

- *m1*: Send an email from mail client to mail server
- *m2*: Download an email from mailbox server to a mail client
- *m3*: Checking email in a web browser

Which is the application level protocol used in each activity?

- A. *m1*: HTTP *m2*: SMTP *m3*: POP
- B. *m1*: SMTP *m2*: FTP *m3*: HTTP
- C. *m1*: SMTP *m2*: POP *m3*: HTTP
- D. *m1*: POP *m2*: SMTP *m3*: IMAP

gate2011-cse computer-networks application-layer-protocols easy

Answer ⬇

2.1.3 Application Layer Protocols: GATE CSE 2012 | Question: 10 top
<https://gateoverflow.in/42>


The protocol data unit (PDU) for the application layer in the Internet stack is:

- A. Segment
- B. Datagram
- C. Message
- D. Frame

gate2012-cse computer-networks application-layer-protocols easy

Answer ⬇



Which of the following is/are example(s) of stateful application layer protocol?

- i. HTTP
 - ii. FTP
 - iii. TCP
 - iv. POP3
- A. (i) and (ii) only
B. (ii) and (iii) only
C. (ii) and (iv) only
D. (iv) only

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application-layer-protocols

normal

Answer



Which of the following protocol pairs can be used to send and retrieve e-mails (in that order)?

- A. IMAP POP3
- B. SMTP, POP3
- C. SMTP MIME
- D. IMAP, SMTP

gate2019-cse

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application-layer-protocols

Answer



Assume that you have made a request for a web page through your web browser to a web server. Initially the browser cache is empty. Further, the browser is configured to send HTTP requests in non-persistent mode. The web page contains text and five very small images. The minimum number of TCP connections required to display the web page completely in your browser is _____.

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numerical-answers

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application-layer-protocols

Answer



Consider the three commands : PROMPT, HEAD and RCPT.

Which of the following options indicate a correct association of these commands with protocols where these are used?

- A. HTTP, SMTP, FTP
- B. FTP, HTTP, SMTP
- C. HTTP, FTP, SMTP
- D. SMTP, HTTP, FTP

gate2005-it

computer-networks

application-layer-protocols

normal

Answer



Assume that "host1.mydomain.dom" has an IP address of 145.128.16.8. Which of the following options would be most appropriate as a subsequence of steps in performing the reverse lookup of 145.128.16.8 ? In the following options "NS" is an abbreviation of "nameserver".

- A. Query a NS for the root domain and then NS for the "dom" domains
- B. Directly query a NS for "dom" and then a NS for "mydomain.dom" domains
- C. Query a NS for in-addr.arpa and then a NS for 128.145.in-addr.arpa domains
- D. Directly query a NS for 145.in-addr.arpa and then a NS for 128.145.in-addr.arpa domains

Answer

2.1.9 Application Layer Protocols: GATE IT 2006 | Question: 18 top

<https://gateoverflow.in/3557>



HELO and PORT, respectively, are commands from the protocols:

- A. FTP and HTTP
- B. TELNET and POP3
- C. HTTP and TELNET
- D. SMTP and FTP

Answer

2.1.10 Application Layer Protocols: GATE IT 2008 | Question: 20 top

<https://gateoverflow.in/3280>



Provide the best matching between the entries in the two columns given in the table below:

I. Proxy Server	a. Firewall
II. Kazaa, DC++	b. Caching
III. Slip	c. P2P
IV. DNS	d. PPP

- A. I-a, II-d, III-c, IV-b
- B. I-b, II-d, III-c, IV-a
- C. I-a, II-c, III-d, IV-b
- D. I-b, II-c, III-d, IV-a

Answer

Answers: Application Layer Protocols

2.1.1 Application Layer Protocols: GATE CSE 2008 | Question: 14, ISRO2016-74 top

<https://gateoverflow.in/412>



✓ **OPTION A**

Its transport layers responsibility to divide data in to fragments/ packets. Application layer need not worry about it.

👍 52 votes

-- Desert_Warrior (6k points)

2.1.2 Application Layer Protocols: GATE CSE 2011 | Question: 4 top

<https://gateoverflow.in/2106>



✓ **Answer is (C)**

Sender/Client send mail from client mailbox to server mail box with the help of SMTP protocol whereas Receiver or Server retrieve the mail from its mail box to reading using POP3 protocol.

When we want to take the help process to see email in browser in that case we HTTP. Because It creates beautiful page of mailbox with the help of process.

👍 29 votes

-- Paras Singh (8.9k points)

2.1.3 Application Layer Protocols: GATE CSE 2012 | Question: 10 top

<https://gateoverflow.in/412>



✓ **(C) Message is the answer.**

For Application, Presentation and Session layers, the PDU is message

For Transport layer, PDU is segment for TCP and datagram for UDP

For Network layer, PDU is packet

For Datalink layer, PDU is frames

For physical layer, PDU is stream of bits

👍 73 votes

-- gatecse (63.3k points)

2.1.4 Application Layer Protocols: GATE CSE 2016 Set 1 | Question: 25 top

<https://gateoverflow.in/39628>



✓ Answer is (C) part

Stateless protocol is a [communications protocol](#) in which no information is retained by either sender or receiver. (Note: The remembered information is called as the state)

HTTP (Stateless | Application Layer | Uses TCP (80)) - No information is maintained. If in some case state maintenance is required then cookies are used. Now HTTPS is HTTP over a secure connection So it is also stateless.

FTP (Stateful | Application Layer | Uses TCP (20 and 21)) server that conducts an interactive session with the user. During the session, a user is provided a means to be authenticated and set various variables (working directory, transfer mode), all stored on the server as part of the user's state.

TCP (Stateful / Transport Layer) various information related to connection is maintained.

BGP (Stateful / Application Layer / Uses TCP) Finite state Automata is used to describe the state.

POP3 (Stateful / Application Layer / Uses TCP (110))

In General if [some authorization is required then stateful design is used](#).

Refer ->

- [Link 1](#)
- [Link 2](#)

References



👍 55 votes

-- Chhotu Ram Chauhan (12k points)

2.1.5 Application Layer Protocols: GATE CSE 2019 | Question: 16 top

<https://gateoverflow.in/302832>



✓ Simple Mail Transfer Protocol (SMTP) is the standard protocol for **sending emails** across the Internet.

IMAP and POP3 are the Internet mail protocols used for **retrieving emails**.

MIME allows the users to exchange different (non-ASCII) kinds of data files in an email : audio, video, images, etc

So from the given options, **option B is the correct** one i.e. SMTP to send e-mail and POP3 to retrieve e-mail.

👍 17 votes

-- NabilSayyad (761 points)

2.1.6 Application Layer Protocols: GATE CSE 2020 | Question: 25 top

<https://gateoverflow.in/333208>



✓ In HTTP non-persistent connection, each time a request is served by the server, the connection is automatically closed by the server.

So we need 1 connection for web page and 5 for images. Thus, in total we need 6 TCP connections to fetch web page completely.

Answer: 6

👍 20 votes

-- Ayush Upadhyaya (28.4k points)

2.1.7 Application Layer Protocols: GATE IT 2005 | Question: 25 [top](#)

<https://gateoverflow.in/3770>



✓ **RCPT:** Recipient to, As the name suggests it is used in **SMTP**(Simple Mail Transfer Protocol)

HEAD: this is used in **HTTP** to get the meta-information, to decide the category of the packet.

PROMPT: turns off prompting for individual files when using the **mget** or **mput** commands. Use this command if you do not want to be prompted for each file transfer when transferring multiple files.

Correct Answer: **B**

👍 53 votes

-- nagalla pruthvi (675 points)

2.1.8 Application Layer Protocols: GATE IT 2005 | Question: 77 [top](#)

<https://gateoverflow.in/3840>



✓ The answer is (C)

A & B are clearly wrong as we are doing Reverse lookup.

C is the closest answer to the process given in RFC 1033. We need to get NS for in-addr.arpa before doing a query to 8.16.128.145.in-addr.arpa

D is not correct, it is not close to the process.

Relevant stuff from <https://tools.ietf.org/html/rfc1033>

IN-ADDR.ARPA

The structure of names in the domain system is set up in a hierarchical way such that the address of a name can be found by tracing down the domain tree contacting a server for each label of the name. Because of this 'indexing' based on name, there is no easy way to translate a host address back into its host name.

In order to do the reverse translation easily, a domain was created that uses hosts' addresses as part of a name that then points to the data for that host. In this way, there is now an 'index' to hosts' RRs based on their address. This address mapping domain is called IN-ADDR.ARPA. Within that domain are subdomains for each network, based on network number. Also, for consistency and natural groupings, the 4 octets of a host number are reversed.

For example, the ARPANET is net 10. That means there is a domain called 10.IN-ADDR.ARPA. Within this domain there is a PTR RR at 51.0.0.10.IN-ADDR that points to the RRs for the host SRI-NIC.ARPA (who's address is 10.0.0.51). Since the NIC is also on the MILNET (Net 26, address 26.0.0.73), there is also a PTR RR at 73.0.0.26.IN-ADDR.ARPA that points to the same RR's for SRI-NIC.ARPA. The format of these special pointers is defined below along with the examples for the NIC.

The PTR record is used to let special names point to some other location in the domain tree. They are mainly used in the IN-ADDR.ARPA records for translation of addresses to names. PTR's should use official names and not aliases.

For example, host SRI-NIC.ARPA with addresses 10.0.0.51 and 26.0.0.73 would have the following records in the respective zone files for net 10 and net 26:

```
51.0.0.10.IN-ADDR.ARPA. PTR SRI-NIC.ARPA.
73.0.0.26.IN-ADDR.ARPA. PTR SRI-NIC.ARPA.
```

References



👍 36 votes

-- Akash Kanase (36k points)



✓ Answer is D.

References:

- http://en.wikipedia.org/wiki/Simple_Mail_Transfer_Protocol#SMTP_transport_example
- http://en.wikipedia.org/wiki/File_Transfer_Protocol#Protocol_overview

References



gateoverflow.in

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👍 25 votes

-- Rajarshi Sarkar (27.9k points)



✓ Answer is C) I-a, II-c, III-d, IV-b

- Proxy Server ⇒ Proxy Server and Firewall can be combined. -- a. Firewall
- Kazaa, DC++ ⇒ These are P2P application. -- c. P2P
- Slip ⇒ P2P Slip is a predecessor of PPP. -- d. PPP
- DNS ⇒ DNS responses are often called -- b. Caching

👍 27 votes

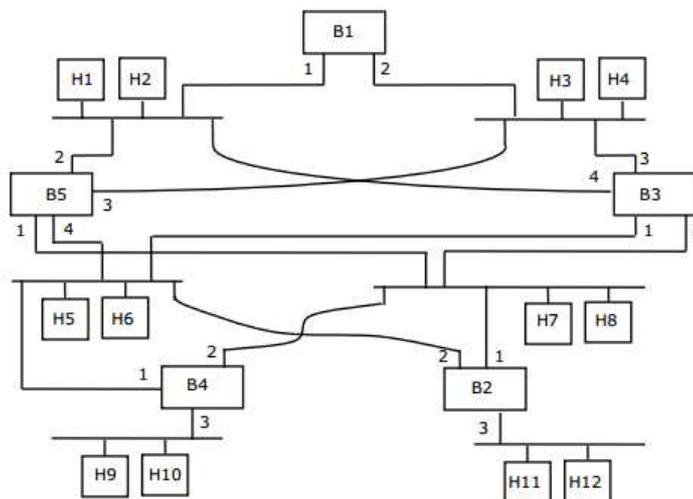
-- Akash Kanase (36k points)

2.2 Bridges (2) [top](#)



Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



For the given connection of LANs by bridges, which one of the following choices represents the depth first traversal of the spanning tree of bridges?

- A. B1, B5, B3, B4, B2
- B. B1, B3, B5, B2, B4
- C. B1, B5, B2, B3, B4
- D. B1, B3, B4, B5, B2

Answer

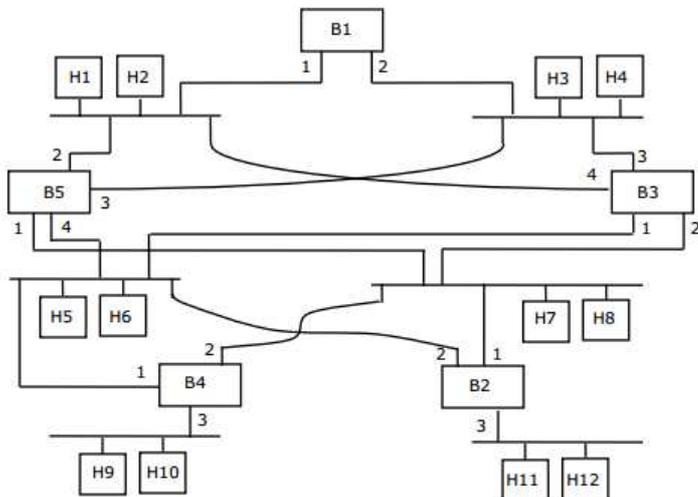
2.2.2 Bridges: GATE CSE 2006 | Question: 83

https://gateoverflow.in/79790



Consider the diagram shown below where a number of LANs are connected by (transparent) bridges. In order to avoid packets looping through circuits in the graph, the bridges organize themselves in a spanning tree. First, the root bridge is identified as the bridge with the least serial number. Next, the root sends out (one or more) data units to enable the setting up of the spanning tree of shortest paths from the root bridge to each bridge.

Each bridge identifies a port (the root port) through which it will forward frames to the root bridge. Port conflicts are always resolved in favour of the port with the lower index value. When there is a possibility of multiple bridges forwarding to the same LAN (but not through the root port), ties are broken as follows: bridges closest to the root get preference and between such bridges, the one with the lowest serial number is preferred.



Consider the spanning tree $B1, B5, B3, B4, B2$ for the given connection of LANs by bridges, that represents the depth first traversal of the spanning tree of bridges. Let host $H1$ send out a broadcast ping packet. Which of the following options represents the correct forwarding table on $B3$?

- a.

Hosts	Port
H1, H2, H3, H4	3
H5, H6, H9, H10	1
H7, H8, H11, H12	2
- b.

Hosts	Port
H1, H2	4
H3, H4	3
H5, H6	1
H7, H8, H9, H10, H11, H12	2
- c.

Hosts	Port
H3, H4	3
H5, H6, H9, H10	1
H1, H2	4
H7, H8, H11, H12	2
- d.

Hosts	Port
H1, H2, H3, H4	3
H5, H7, H9, H10	1
H7, H8, H11, H12	4

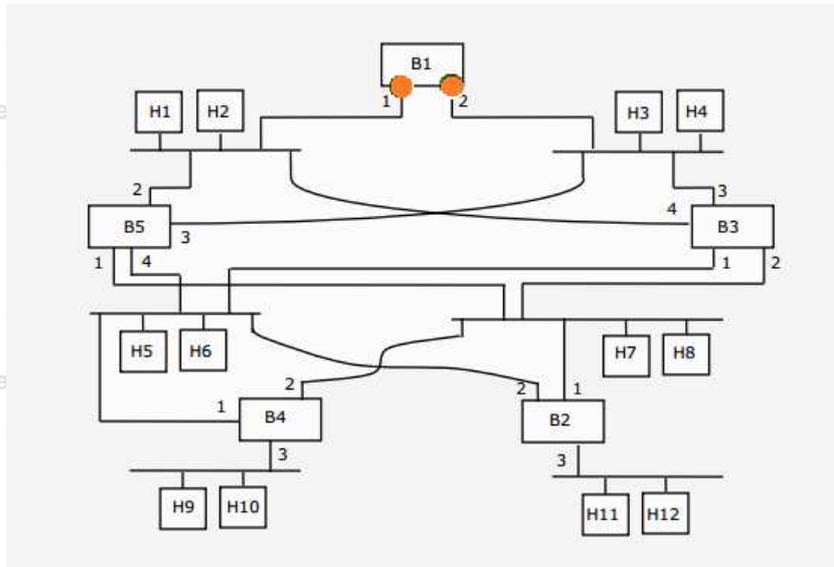
Answers: Bridges

2.2.1 Bridges: GATE CSE 2006 | Question: 82

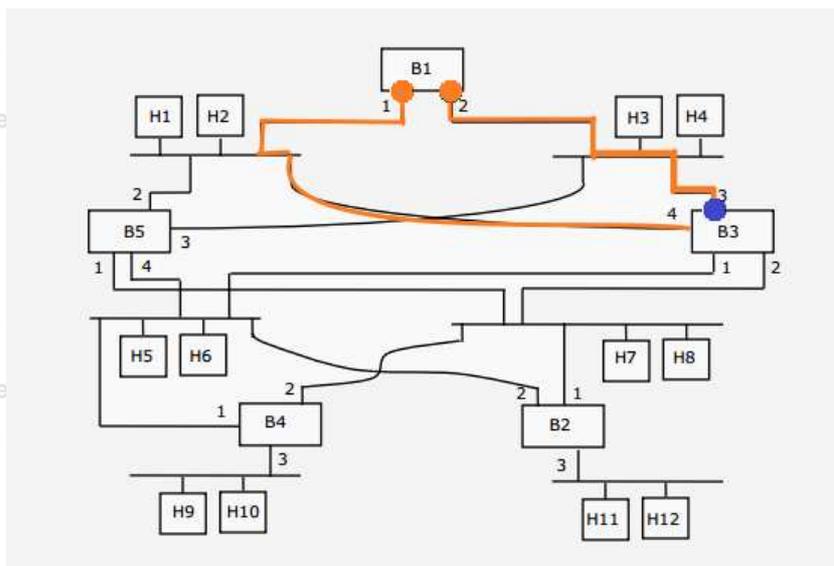
<https://gateoverflow.in/1855>



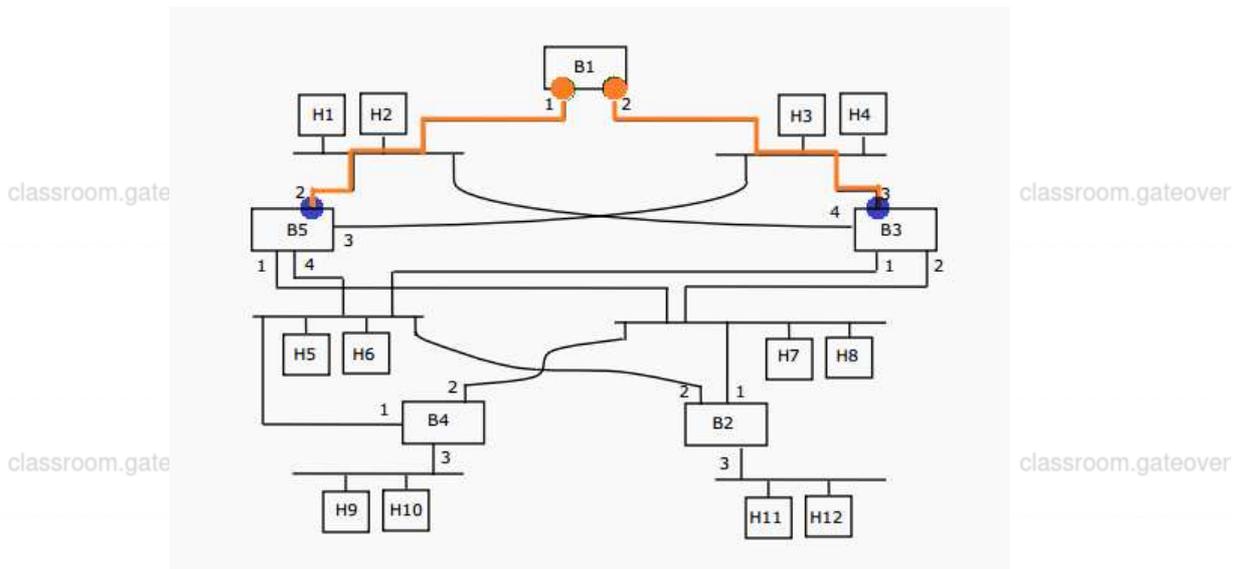
- First select $B1$ as the root bridge. This selection is based on lower serial ID as given in the question.
- All ports of root bridge are **designated ports** and they are in **forwarding state**.



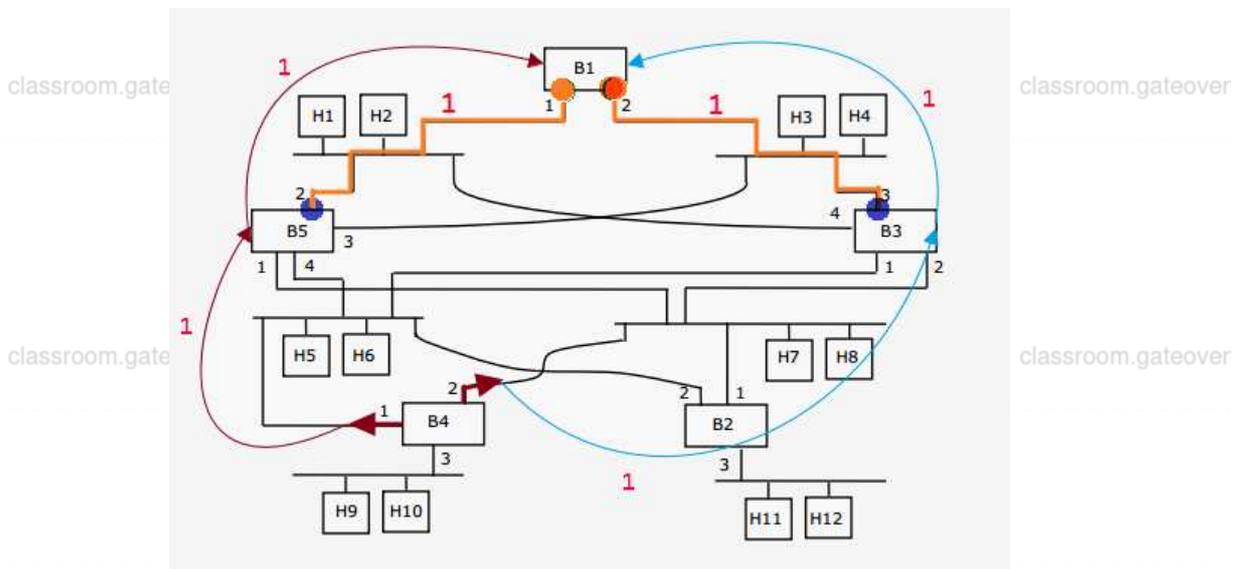
- Every non-root bridge must have a root port. All root ports are placed in **forwarding state**.
- **Root port is the port that is closest to the root bridge**
- For example, we observe bridge $B3$.
- It has two ports leading to the root bridge. If we assume bridge-to-bridge cost as 1 unit, both these paths have the same cost. Then we will select the **lower port index** as given in the question as the root port for the bridge $B3$.
- **port 3** of $B3$ becomes the root port.



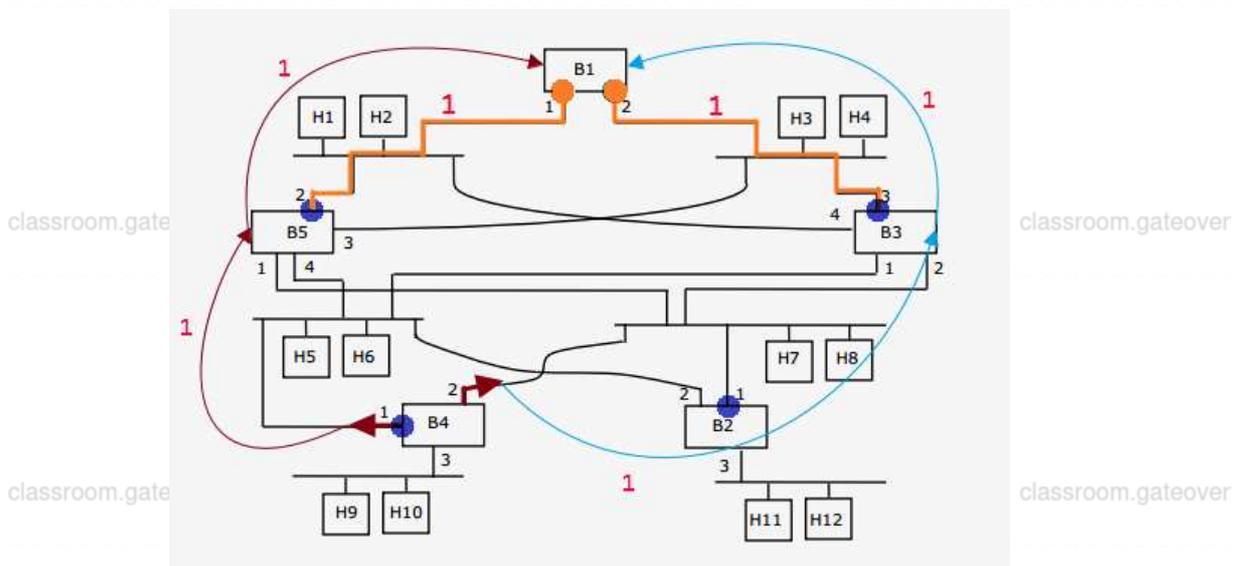
- Using the same logic we will find out the root ports for $B5$ also.



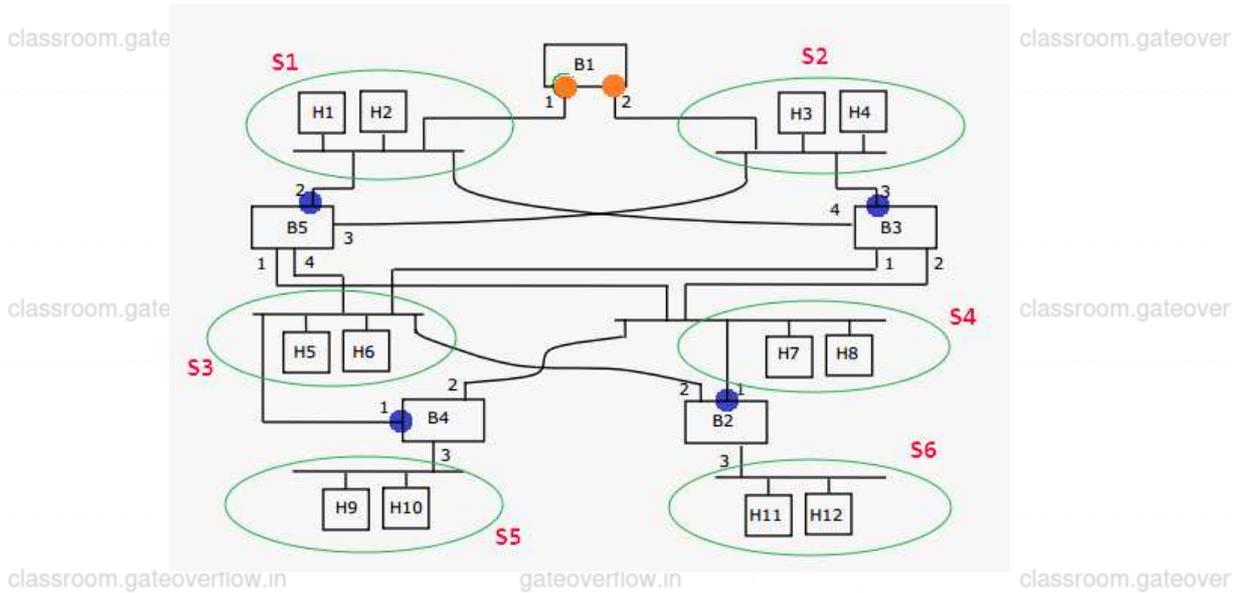
- Coming to $B4$ for root port selection.



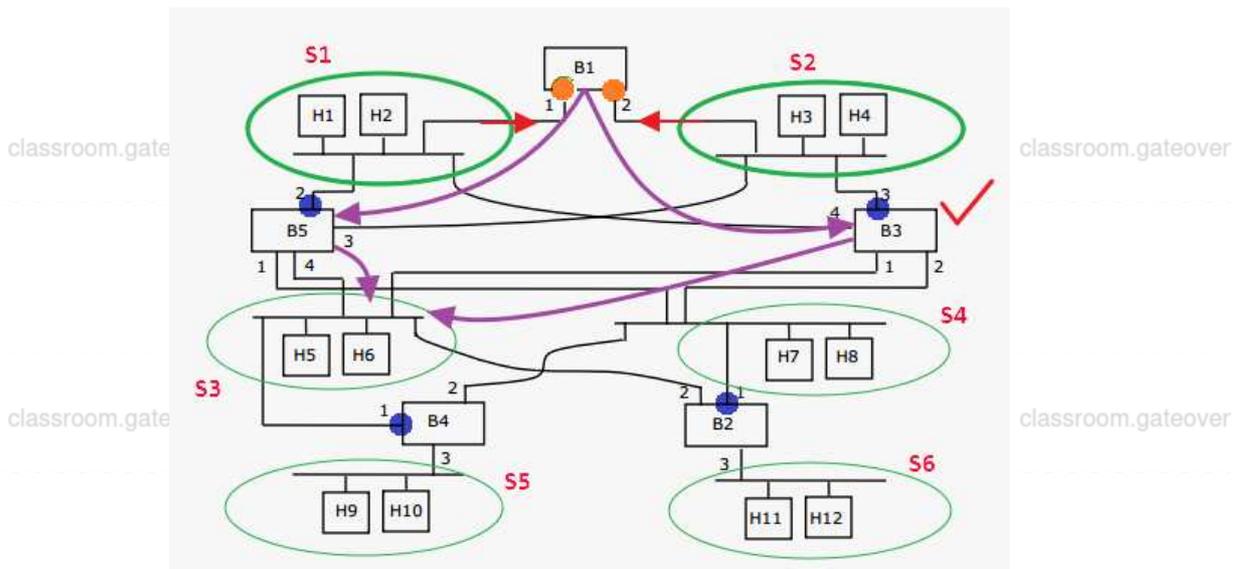
- We have again two different paths with the same cost, We will select port 1 as the root port for $B4$
- Using the same logic port 1 is selected as root port for $B2$ as well.



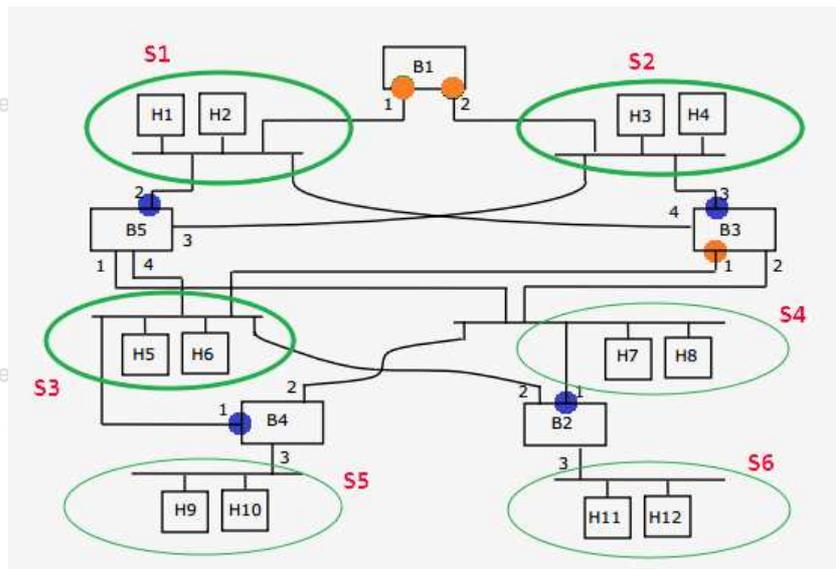
- Now we have to consider the **designated ports**
- The designated ports are the ports responsible for **forwarding traffic onto a network segment**
- We have total 6 network segments or **LAN's**. Each segment will have **one** designated ports.



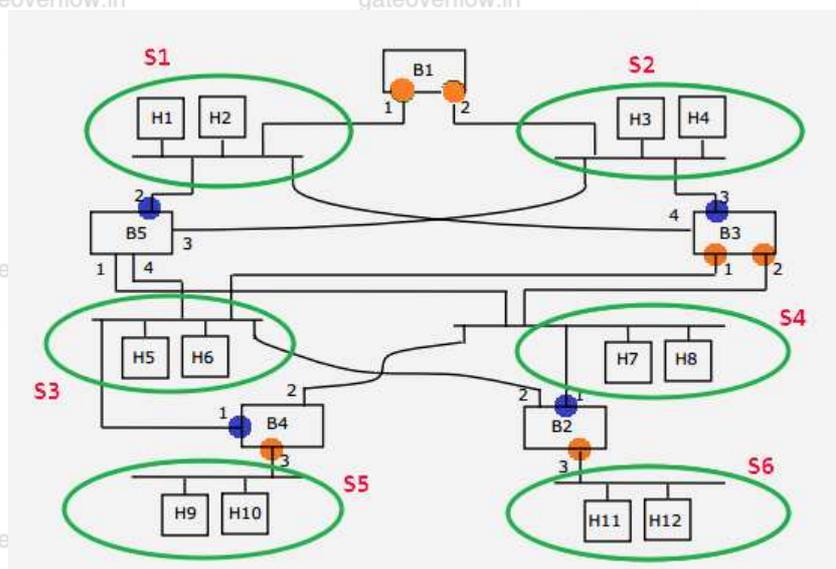
- S1 and S2 are connected to the root bridge itself via two designated ports. So no issue with segments S1 and S2 traffic.
- Let's consider other segments.
- For example S3.



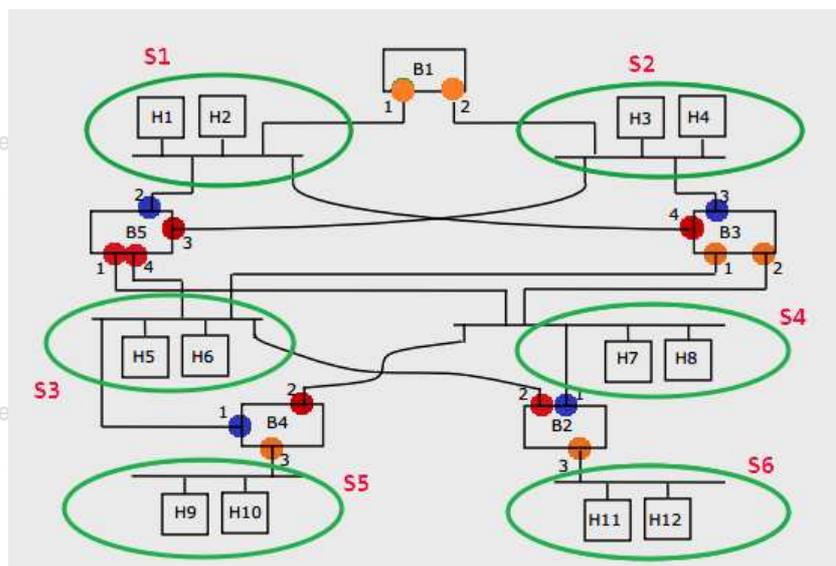
- B2, B3, B4, B5 all can forward traffic to this segment S3
- According to the question in this situation, we will consider only those bridges which are **nearer to the root bridge B1**.
- B5 and B3 are both nearer to the root bridge.
- Then we will break this tie by selecting the **lower bridge serial ID** i.e. B3 is selected and designated port is **port 1** of B3 for the segment S3



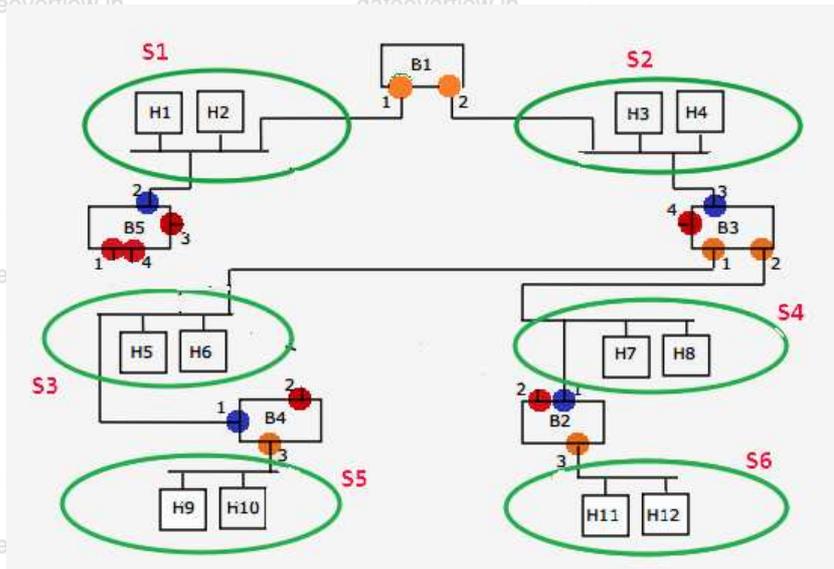
- Similarly, we can choose designated ports for $S4$, $S5$ and $S6$



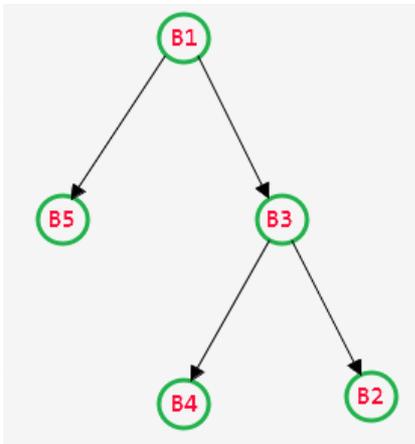
- Remaining all ports are blocked ports.



- This the final [spanning Tree](#)



- DFS traversal will give answer as **A**



PLEASE check the following two videos.[IITB lectures]

- <https://www.youtube.com/embed/JgApAnUQ1Ss>
- https://www.youtube.com/embed/s_xSIdBjagc

References

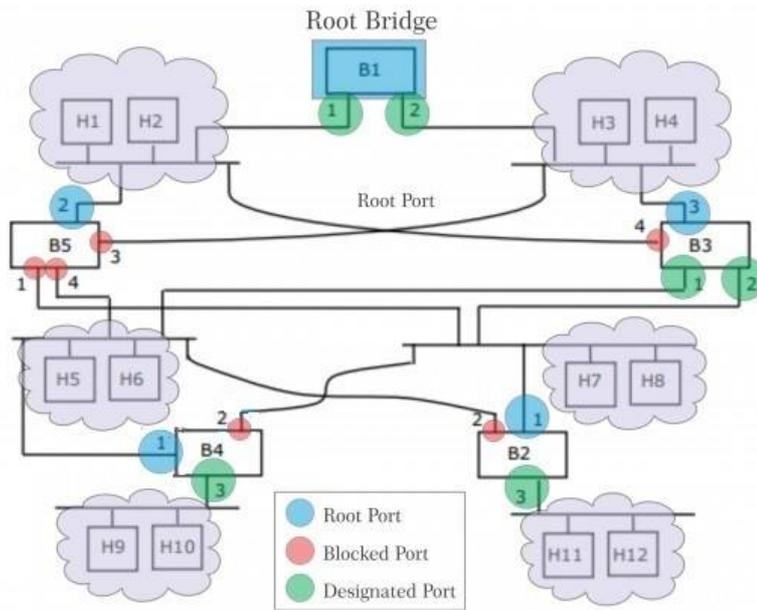


👍 290 votes

-- Debashish Deka (40.8k points)



- ✓ Option is **A** see this as we go with options, option **A** match only with this picture.



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👍 25 votes

-- Bikram (58.4k points)

2.3

Communication (3) top

2.3.1 Communication: GATE CSE 2012 | Question: 44 top

<https://gateoverflow.in/2153>



Consider a source computer (S) transmitting a file of size 10^6 bits to a destination computer (D) over a network of two routers (R_1 and R_2) and three links (L_1, L_2 , and L_3). L_1 connects S to R_1 ; L_2 connects R_1 to R_2 ; and L_3 connects R_2 to D . Let each link be of length 100 km. Assume signals travel over each link at a speed of 10^8 meters per second. Assume that the link bandwidth on each link is 1 Mbps. Let the file be broken down into 1000 packets each of size 1000 bits. Find the total sum of transmission and propagation delays in transmitting the file from S to D ?

- A. 1005 ms
- B. 1010 ms
- C. 3000 ms
- D. 3003 ms

gate2012-cse computer-networks communication normal

Answer

2.3.2 Communication: GATE IT 2007 | Question: 62 top

<https://gateoverflow.in/3506>



Let us consider a statistical time division multiplexing of packets. The number of sources is 10. In a time unit, a source transmits a packet of 1000 bits. The number of sources sending data for the first 20 time units is 6, 9, 3, 7, 2, 2, 2, 3, 4, 6, 1, 10, 7, 5, 8, 3, 6, 2, 9, 5 respectively. The output capacity of multiplexer is 5000 bits per time unit. Then the average number of backlogged of packets per time unit during the given period is

- A. 5
- B. 4.45
- C. 3.45
- D. 0

gate2007-it computer-networks communication normal

Answer

2.3.3 Communication: GATE IT 2007 | Question: 64 top

<https://gateoverflow.in/3509>



A broadcast channel has 10 nodes and total capacity of 10 Mbps. It uses polling for medium access. Once a node finishes transmission, there is a polling delay of $80 \mu s$ to poll the next node. Whenever a node is polled, it is allowed to transmit a maximum of 1000 bytes. The maximum throughput of the broadcast channel is:

- A. 1 Mbps

- B. 100/11 Mbps
- C. 10 Mbps
- D. 100 Mbps

gate2007-it computer-networks communication normal

Answer

Answers: Communication

2.3.1 Communication: GATE CSE 2012 | Question: 44

https://gateoverflow.in/2153



✓ routers are store and forward devices.

$$\text{Propagation time} = \frac{100 \text{ km}}{10^8 \text{ m/s}} = 1 \text{ milli second}$$

$$\text{Transmission time for a packet} = \frac{1000}{10^6} = 1 \text{ milli second}$$

Packets will be forwarded in a pipelined manner after the first packet reaches the receiver, in every 1 ms a new one arrives.

now Time taken by packet no 1 to reach destination is :

$$1 \text{ ms (TT at sender)} + 1 \text{ ms (PT from sender to R1)} + 1 \text{ ms (TT at R1)} + 1 \text{ ms (PT from R1 to R2)} + 1 \text{ ms (TT at R2)} + 1 \text{ ms (PT from R2 to destination)} = 6 \text{ ms}$$

So, time for packet,

$$1000 = 6 \text{ ms} + 999 \text{ ms} \\ = 1005 \text{ ms}$$

Correct Answer: A

106 votes

-- Digvijay (44.9k points)

First all data needs to be transmitted from source and after all packets transmission from source, just focus on last packet jorney, and u will get it.

$$\text{Transmission time for all packets from Source} = \frac{10^6}{1 \times 10^6} = 1 \text{ sec} = 1000 \text{ ms.}$$

(Now the last packet is our main focus, bcoz the moment last packet reaches, all previous are already reached to Destination)

$$\text{Last packet time} = 3 \times \text{propagation time of link} + 2 \times \text{transmission time of router} \quad (\text{Transmission time for source is already included in above 1000 msec}) \\ = (3 \times 1) + (2 \times 1) = 5 \text{ ms}$$

$$\text{Total time} = 1000 + 5 = 1005 \text{ ms}$$

65 votes

-- Sachin Mittal (15.8k points)

2.3.2 Communication: GATE IT 2007 | Question: 62

https://gateoverflow.in/3506



✓ Answer is B.

$$\text{Here, we can send at max 5 packets per Time unit} \frac{5000}{1000}$$

So, whatever which is not sent is backlog.

So,

$$\text{First Time Unit} \Rightarrow 6,$$

$$\text{Backlog in First time unit} \Rightarrow 6 - 5 \Rightarrow 1 \text{ This one gets added to next Time units load}$$

$$\text{Second time unit} \Rightarrow 9 + 1 \text{ (One from Previous Time Unit)}$$

Backlog in Second time Unit = $10 - 5 \Rightarrow 5$ (This one gets added to next Time Units load.)

Total Backlog this way = $1 + 5 + 3 + 5 + 2 + 0 + 0 + 0 + 0 + 1 + 0 + 5 + 7 + 7 + 10 + 8 + 9 + 6 + 10 + 10 = 89$

$$\text{Avg Backlog} = \frac{89}{20} = 4.45$$

The average number of backlogged of packets per time unit during the given period is 4.45.

👍 75 votes

-- Akash Kanase (36k points)

2.3.3 Communication: GATE IT 2007 | Question: 64 top

<https://gateoverflow.in/3509>



✓ Propagation time is not given so that's negligible here.

$$\text{efficiency} = \frac{\text{transmission time}}{(\text{transmission time} + \text{polling time})}$$

$$T_x = \frac{1000 \text{ bytes}}{10 \text{ Mbps}} = 800 \mu s.$$

Delay because of polling is = $80 \mu s$

$$\text{Efficiency of channel, } e = \frac{\text{transmission} - \text{delay}}{\text{total} - \text{delay}}$$

$$= \frac{800}{800 + 80} = \frac{10}{11}$$

$$\text{Maximum throughput is} = \frac{10}{11} \times 10 \text{ Mbps} = \frac{100}{11} \text{ Mbps}$$

Correct Answer: *B*

👍 64 votes

-- Manu Thakur (34k points)

2.4 Congestion Control (7) top

2.4.1 Congestion Control: GATE CSE 2008 | Question: 56 top

<https://gateoverflow.in/479>



In the slow start phase of the TCP congestion algorithm, the size of the congestion window:

- A. does not increase
- B. increase linearly
- C. increases quadratically
- D. increases exponentially

gate2008-cse computer-networks congestion-control normal

Answer

2.4.2 Congestion Control: GATE CSE 2012 | Question: 45 top

<https://gateoverflow.in/2156>



Consider an instance of TCP's Additive Increase Multiplicative Decrease (AIMD) algorithm where the window size at the start of the slow start phase is 2 MSS and the threshold at the start of the first transmission is 8 MSS. Assume that a timeout occurs during the fifth transmission. Find the congestion window size at the end of the tenth transmission.

- A. 8 MSS
- B. 14 MSS
- C. 7 MSS
- D. 12 MSS

gate2012-cse computer-networks congestion-control normal

Answer 

2.4.3 Congestion Control: GATE CSE 2014 Set 1 | Question: 27 [top](#) 

<https://gateoverflow.in/1794>



Let the size of congestion window of a TCP connection be 32 KB when a timeout occurs. The round trip time of the connection is 100 msec and the maximum segment size used is 2 KB. The time taken (**in msec**) by the TCP connection to get back to 32 KB congestion window is _____.

gate2014-cse-set1 computer-networks tcp congestion-control numerical-answers normal

Answer 

2.4.4 Congestion Control: GATE CSE 2015 Set 1 | Question: 29 [top](#) 

<https://gateoverflow.in/8253>



Consider a LAN with four nodes $S_1, S_2, S_3,$ and S_4 . Time is divided into fixed-size slots, and a node can begin its transmission only at the beginning of a slot. A collision is said to have occurred if more than one node transmits in the same slot. The probabilities of generation of a frame in a time slot by $S_1, S_2, S_3,$ and S_4 are 0.1, 0.2, 0.3 and 0.4 respectively. The probability of sending a frame in the first slot without any collision by any of these four stations is _____.

gate2015-cse-set1 computer-networks normal numerical-answers congestion-control

Answer 

2.4.5 Congestion Control: GATE CSE 2018 | Question: 14 [top](#) 

<https://gateoverflow.in/204088>



Consider the following statements regarding the slow start phase of the TCP congestion control algorithm. Note that *cwnd* stands for the TCP congestion window and MSS window denotes the Maximum Segments Size:

- i. The *cwnd* increases by 2 MSS on every successful acknowledgment
- ii. The *cwnd* approximately doubles on every successful acknowledgment
- iii. The *cwnd* increases by 1 MSS every round trip time
- iv. The *cwnd* approximately doubles every round trip time

Which one of the following is correct?

- A. Only (ii) and (iii) are true
- B. Only (i) and (iii) are true
- C. Only (iv) is true
- D. Only (i) and (iv) are true

gate2018-cse computer-networks tcp congestion-control normal

Answer 

2.4.6 Congestion Control: GATE CSE 2018 | Question: 55 [top](#) 

<https://gateoverflow.in/204130>



Consider a simple communication system where multiple nodes are connected by a shared broadcast medium (like Ethernet or wireless). The nodes in the system use the following carrier-sense based medium access protocol. A node that receives a packet to transmit will carrier-sense the medium for 5 units of time. If the node does not detect any other transmission, it starts transmitting its packet in the next time unit. If the node detects another transmission, it waits until this other transmission finishes, and then begins to carrier-sense for 5 time units again. Once they start to transmit, nodes do not perform any collision detection and continue transmission even if a collision occurs. All transmissions last for 20 units of time. Assume that the transmission signal travels at the speed of 10 meters per unit time in the medium.

Assume that the system has two nodes P and Q , located at a distance d meters from each other. P start transmitting a packet at time $t = 0$ after successfully completing its carrier-sense phase. Node Q has a packet to transmit at time $t = 0$ and begins to carrier-sense the medium.

The maximum distance d (in meters, rounded to the closest integer) that allows Q to successfully avoid a collision between its proposed transmission and P 's ongoing transmission is _____.

gate2018-cse computer-networks congestion-control numerical-answers

Answer 



On a TCP connection, current congestion window size is Congestion Window = 4 KB. The window size advertised by the receiver is Advertise Window = 6 KB. The last byte sent by the sender is LastByteSent = 10240 and the last byte acknowledged by the receiver is LastByteAcked = 8192. The current window size at the sender is:

- A. 2048 bytes
- B. 4096 bytes
- C. 6144 bytes
- D. 8192 bytes

gate2005-it

computer-networks

congestion-control

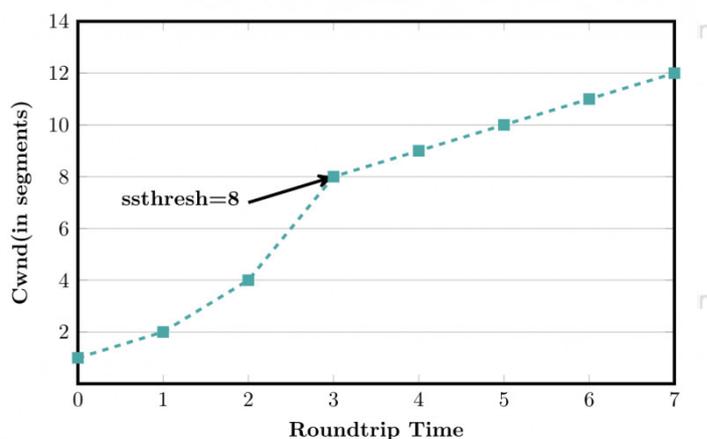
normal

Answer

Answers: Congestion Control



- ✓ Assume that ssthresh = 8.



Increase is exponential in the Slow Start Phase.

Answer is **option D**.

30 votes

-- Amar Vashishth (25.2k points)



- ✓ At:

$$t = 1, \Rightarrow 2MSS$$

$$t = 2, \Rightarrow 4MSS$$

$$t = 3, \Rightarrow 8MSS$$

$$t = 4, \Rightarrow 9MSS \text{ (after threshold additive increase)}$$

$$t = 5, \Rightarrow 10MSS \text{ (fails)}$$

Threshold will be reduced to $\frac{n}{2}$ i.e. $\frac{10}{2} = 5$.

$$t = 6, \Rightarrow 1MSS,$$

(There is an ambiguity here if the window size will be 1 MSS or 2 MSS as given in the question and due to this GATE gave marks to all. Assuming window size to be 1 MSS)

$$t = 7 \Rightarrow 2MSS$$

$$t = 8, \Rightarrow 4MSS$$

$$t = 9, \Rightarrow 5MSS$$

$$t = 10, \Rightarrow 6MSS.$$

So, at the end of 10^{th} successful transmission ,
 The the congestion window size will be $(6 + 1) = 7 MSS$.

👍 98 votes

-- Harsh181996 (3k points)

2.4.3 Congestion Control: GATE CSE 2014 Set 1 | Question: 27 top 5

<https://gateoverflow.in/1794>



✓ **Answer:** Given that at the time of **Time Out**, Congestion Window Size is $32KB$ and $RTT = 100ms$,
 When Time Out occurs, for the next round of Slow Start,

$$\text{Threshold} = \frac{\text{size of congestion window}}{2},$$

$$\text{Threshold} = 16KB$$

Suppose we have a **slow start** $\Rightarrow 2KB | 4KB | 8KB | 16KB$
 (As the threshold is reached, Additive increase starts)

$|18KB | 20KB | 22KB | 24KB | 26KB | 28KB | 30KB | 32KB$

Here | (vertical line) is representing **RTT** so the total number of vertical lines is $11 \times 100ms = 1100ms$ and so this is the answer.

👍 157 votes

-- Jay (831 points)

2.4.4 Congestion Control: GATE CSE 2015 Set 1 | Question: 29 top 5

<https://gateoverflow.in/8253>



$$\begin{aligned} P &= P(S1)P(\neg S2)P(\neg S3)P(\neg S4) \\ &+ P(\neg S1)P(S2)P(\neg S3)P(\neg S4) \\ &+ P(\neg S1)P(\neg S2)P(S3)P(\neg S4) \\ &+ P(\neg S1)P(\neg S2)P(\neg S3)P(S4) \end{aligned}$$

$$= 0.1 * 0.8 * 0.7 * 0.6 + 0.9 * 0.2 * 0.7 * 0.6 + 0.9 * 0.8 * 0.3 * 0.6 + 0.9 * 0.8 * 0.7 * 0.4$$

$$= 0.4404$$

👍 71 votes

-- Arjun Suresh (332k points)

2.4.5 Congestion Control: GATE CSE 2018 | Question: 14 top 5

<https://gateoverflow.in/204088>



✓ Each time an *ACK* is received by the sender, the congestion window is increased by 1 segment:
 $CWND = CWND + 1$.

CWND increases exponentially on every *RTT*.

Hence, correct answer is **C**.

<https://www.utdallas.edu/~venky/acn/CongestionControl.pdf>

References



👍 36 votes

-- Prashant Kumar (1k points)

2.4.6 Congestion Control: GATE CSE 2018 | Question: 55 top 5

<https://gateoverflow.in/204130>



✓ P starts transmission at $t = 0$. If P's first bit reaches Q within Q's sensing window, then Q won't transmit and there shall be no collision.

Q senses carrier till $t = 5$. At $t = 6$ it starts its transmission.

If the first bit of P reaches Q by $t = 5$, collision can be averted. Since signal speed is 10 m/time (given), we can conclude that max distance between P and Q can be 50 meters.

👍 67 votes

classroom.gateover
-- Abhishek Sarkar (281 points)

2.4.7 Congestion Control: GATE IT 2005 | Question: 73 top

<https://gateoverflow.in/3836>



✓ **Answer should be (B).**

Current Sender window = $\min(\text{Congestion Window}, \text{Advertised Window})$
= $\min(4KB, 6KB)$
= $4KB$.

👍 81 votes

-- srestha (85.2k points)

2.5

Crc Polynomial (4) top

2.5.1 Crc Polynomial: GATE CSE 2007 | Question: 68, ISRO2016-73 top

<https://gateoverflow.in/126>



The message 11001001 is to be transmitted using the CRC polynomial $x^3 + 1$ to protect it from errors. The message that should be transmitted is:

- A. 11001001000
- B. 11001001011
- C. 11001010
- D. 110010010011

gate2007-cse computer-networks error-detection crc-polynomial normal isro2016

Answer 🗨

2.5.2 Crc Polynomial: GATE CSE 2017 Set 1 | Question: 32 top

<https://gateoverflow.in/118313>



A computer network uses polynomials over $GF(2)$ for error checking with 8 bits as information bits and uses $x^3 + x + 1$ as the generator polynomial to generate the check bits. In this network, the message 01011011 is transmitted as:

- A. 01011011010
- B. 01011011011
- C. 01011011101
- D. 01011011100

gate2017-cse-set1 computer-networks crc-polynomial normal

Answer 🗨

2.5.3 Crc Polynomial: GATE CSE 2021 Set 2 | Question: 34 top

<https://gateoverflow.in/357506>



Consider the cyclic redundancy check (CRC) based error detecting scheme having the generator polynomial $X^3 + X + 1$. Suppose the message $m_4m_3m_2m_1m_0 = 11000$ is to be transmitted. Check bits $c_2c_1c_0$ are appended at the end of the message by the transmitter using the above CRC scheme. The transmitted bit string is denoted by $m_4m_3m_2m_1m_0c_2c_1c_0$. The value of the checkbit sequence $c_2c_1c_0$ is

- A. 101
- B. 110
- C. 100
- D. 111

gate2021-cse-set2 computer-networks crc-polynomial

Answer 🗨



Consider the following message $M = 1010001101$. The cyclic redundancy check (CRC) for this message using the divisor polynomial $x^5 + x^4 + x^2 + 1$ is :

- A. 01110
- B. 01011
- C. 10101
- D. 10110

gate2005-it computer-networks crc-polynomial normal

Answer

Answers: Crc Polynomial



✓ Answer - B.

Degree of generator polynomial is 3 hence 3-bits are appended before performing division

After performing division using 2^s 's complement arithmetic remainder is 011

The remainder is appended to original data bits and we get $M' = 11001001011$ from $M = 11001001$.

$$\begin{array}{r}
 1001 \overline{) 11001001000} \\
 \underline{1001} \\
 1011 \\
 \underline{1001} \\
 1000 \\
 \underline{1001} \\
 1100 \\
 \underline{1001} \\
 1010 \\
 \underline{1001} \\
 011
 \end{array}$$

Courtesy, Anurag Pandey

49 votes

-- Ankit Rokde (6.9k points)



✓ The generator polynomial has degree 3. So, we append 3 zeroes to the original message.

$$\begin{array}{r}
 1011 \overline{) 01011011000} \\
 \underline{0000} \\
 1011 \\
 \underline{1011} \\
 001100 \\
 \underline{1011} \\
 1110 \\
 \underline{1011} \\
 101
 \end{array}$$

$M' = 01011011\underline{101}$

Correct Answer: C

46 votes

-- Smriti012 (2.8k points)

2.5.3 Crc Polynomial: GATE CSE 2021 Set 2 | Question: 34 top 5

<https://gateoverflow.in/357506>



Correct Option: C

The given polynomial $x^3 + x + 1$ is written as 1011, which consists of 4 bits so, append 3 bits of 0s to the message.

$M = 11000000$

$$\begin{array}{r}
 1011 \overline{) 11000000} \\
 \underline{1011} \\
 1110 \\
 \underline{1011} \\
 1010 \\
 \underline{1011} \\
 100
 \end{array}$$

There the check bits sequence is: **100**.

1 votes

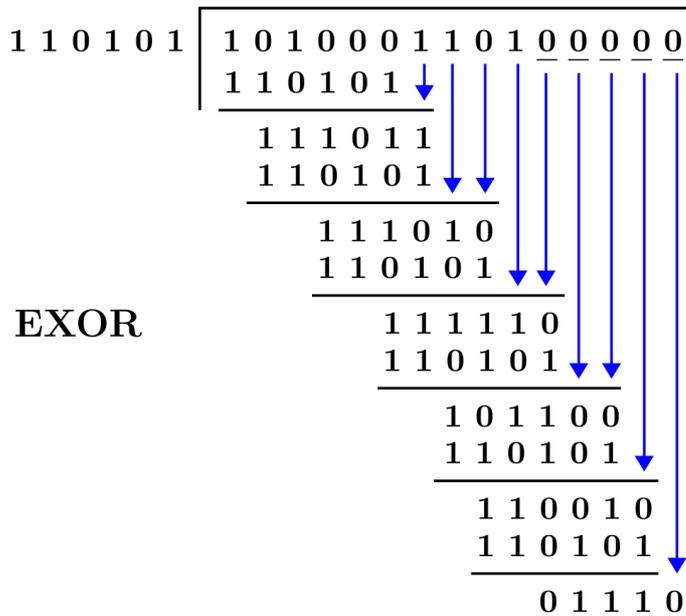
-- Cringe is my middle name... (885 points)

2.5.4 Crc Polynomial: GATE IT 2005 | Question: 78 top 5

<https://gateoverflow.in/3842>



Degree of generator polynomial is 5. Hence, 5 zeroes are appended before division.



$$M' = 1\ 0\ 1\ 0\ 0\ 0\ 1\ 1\ 0\ 1\ \boxed{0\ 1\ 1\ 1\ 0}$$

In CRC calculation, we add the remainder to the original message to get $M' = 101000110101110$.

Answer is A.

45 votes

-- kvkumar (4k points)

2.6 CsmA Cd (5) top 5

2.6.1 CsmA Cd: GATE CSE 2015 Set 3 | Question: 6 top 5 <https://gateoverflow.in/8400>

Consider a CSMA/CD network that transmits data at a rate of 100 Mbps (10^8 bits per second) over a 1 km (kilometre) cable with no repeaters. If the minimum frame size required for this network is 1250 bytes, What is the signal speed (km/sec) in the cable?

- A. 8000
- B. 10000
- C. 16000
- D. 20000

gate2015-cse-set3 computer-networks congestion-control csma-cd normal

Answer

2.6.2 CsmA Cd: GATE CSE 2016 Set 2 | Question: 53 top 5 <https://gateoverflow.in/39589>

A network has a data transmission bandwidth of 20×10^6 bits per second. It uses CSMA/CD in the MAC layer. The maximum signal propagation time from one node to another node is 40 microseconds. The minimum size of a frame in the network is _____ bytes.

gate2016-cse-set2 computer-networks csma-cd numerical-answers normal

Answer

2.6.3 CsmA Cd: GATE IT 2005 | Question: 27 top 5 <https://gateoverflow.in/3773>

Which of the following statements is TRUE about CSMA/CD:

- A. IEEE 802.11 wireless LAN runs CSMA/CD protocol
- B. Ethernet is not based on CSMA/CD protocol
- C. CSMA/CD is not suitable for a high propagation delay network like satellite network

D. There is no contention in a CSMA/CD network

gate2005-it computer-networks congestion-control csma-cd normal

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Answer

2.6.4 Csma Cd: GATE IT 2005 | Question: 71 top

https://gateoverflow.in/3834



A network with CSMA/CD protocol in the MAC layer is running at 1Gbps over a 1km cable with no repeaters. The signal speed in the cable is 2×10^8 m/sec. The minimum frame size for this network should be:

- A. 10000bits
- B. 10000bytes
- C. 5000 bits
- D. 5000bytes

gate2005-it computer-networks congestion-control csma-cd normal

Answer

2.6.5 Csma Cd: GATE IT 2008 | Question: 65 top

https://gateoverflow.in/3376



The minimum frame size required for a CSMA/CD based computer network running at 1Gbps on a 200m cable with a link speed of 2×10^8 m/sec is:

- A. 125bytes
- B. 250bytes
- C. 500bytes
- D. None of the above

gate2008-it computer-networks csma-cd normal

Answer

Answers: Csma Cd

2.6.1 Csma Cd: GATE CSE 2015 Set 3 | Question: 6 top

https://gateoverflow.in/8400



✓ For collision to be detected, the frame size should be such that the transmission time of the frame should be greater than twice the propagation delay (So, before the frame is completely sent, any possible collision will be discovered).

$$\text{So, } \frac{1250 \times 8}{10^8} \geq \frac{2 \times 1}{x}$$

$$\implies x = 2 \times 10^4 = 20000$$

Correct Answer: D

47 votes

-- Arjun Suresh (332k points)

2.6.2 Csma Cd: GATE CSE 2016 Set 2 | Question: 53 top

https://gateoverflow.in/39589



✓ Since, CSMA/CD
Transmission Delay = RTT

Hence,

$$L = B \times \text{RTT}$$

$$\implies L = B \times 2 \times T_{\text{propagation delay}}$$

$$\implies L = (20 \times 10^6) \times 2 \times 40 \times 10^{-6}$$

$$= 20 \times 2 \times 40$$

$$= 1600 \text{ bits}$$

$$= 200 \text{ bytes}$$

Hence, 200 Bytes is the answer.

43 votes

-- Shashank Chavan (2.4k points)

2.6.3 CSMA/CD: GATE IT 2005 | Question: 27

<https://gateoverflow.in/3773>



✓ Answer is C.

CSMA/CD was used in early days, 802.3 not in 802.11

There will be contention in this protocol.

Ethernet is based on CSMA/CD early in 1980s.

29 votes

-- nagalla pruthvi (675 points)

2.6.4 CSMA/CD: GATE IT 2005 | Question: 71

<https://gateoverflow.in/3834>



✓ Answer is (A)

Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely sent, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being sent to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be just t_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is $\text{bandwidth} \times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

$$\geq 2 \times 10^9 \times \frac{1000}{2 \times 10^8}$$

≥ 10000 bits

54 votes

-- Arjun Suresh (332k points)

2.6.5 CSMA/CD: GATE IT 2008 | Question: 65

<https://gateoverflow.in/3376>



✓ Minimum frame size is needed to ensure that collisions are detected properly. The minimum frame size ensures that before a frame is completely sent, it would be notified of any possible collision and hence collision detection works perfectly.

In CSMA/CD a sender won't send a packet if it senses that another sender is using it. So, assume a sender A and a receiver B. When sender sends a packet, receiver might use the cable until it is notified that a packet is being sent to it. The receiver will be notified as soon as the first bit arrives that a packet is coming and it won't send any packet after this until that packet is finished. So, in the worst case for collision, receiver will transmit a packet back to the sender just before the first bit of the packet reaches it. (If t_d is the propagation delay of the channel, this time would be just t_d). In this case, surely there will be collision. But for the sender to detect it, it should be notified of B's packet before the sending of the first packet finishes. i.e., when B's packet arrives at A (takes another t_d time), A shouldn't have finished transmission of the first packet for it to detect a collision. i.e., A should be still continuing the sending of the packet in this time interval of $2 \times t_d$. Thus,

The amount of bits that can be transmitted by A in $2 \times t_d$ time should be less than the frame size (S) (sending of the frame shouldn't finish in this time)

Amount of bits transmitted in time t is $\text{bandwidth} \times t$ and propagation delay- t_d is $\frac{\text{distance}}{\text{link speed}}$

So, $S \geq 2 \times \text{bandwidth} \times t_d$

$$\geq 2 \times 10^9 \times \frac{200}{2 \times 10^8}$$

$$\geq 2000 \text{ bits}$$

$$\geq 250 \text{ bytes}$$

Correct Answer: *B*

👍 35 votes

-- Arjun Suresh (332k points)

2.7

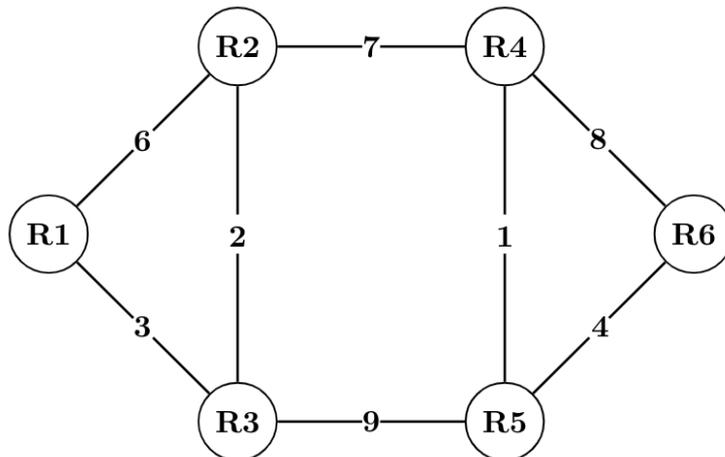
Distance Vector Routing (7) top ⬆

2.7.1 Distance Vector Routing: GATE CSE 2010 | Question: 54 top ⬆

<https://gateoverflow.in/2362>



Consider a network with 6 routers **R1** to **R6** connected with links having weights as shown in the following diagram.



All the routers use the distance vector based routing algorithm to update their routing tables. Each router starts with its routing table initialized to contain an entry for each neighbor with the weight of the respective connecting link. After all the routing tables stabilize, how many links in the network will never be used for carrying any data?

- A. 4
- B. 3
- C. 2
- D. 1

gate2010-cse computer-networks routing distance-vector-routing normal

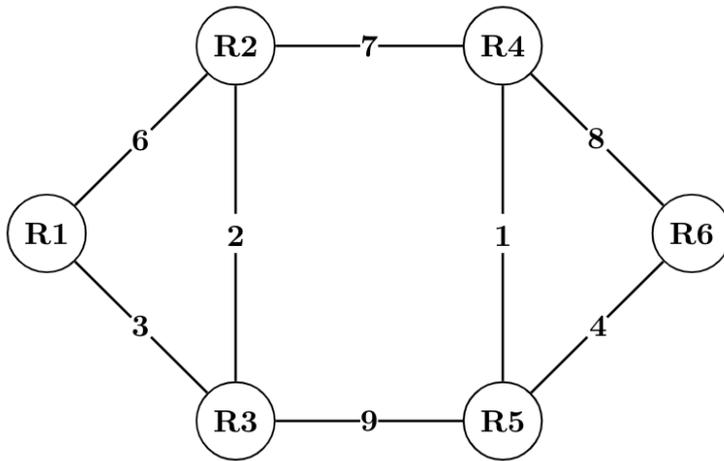
Answer ⬆

2.7.2 Distance Vector Routing: GATE CSE 2010 | Question: 55 top ⬆

<https://gateoverflow.in/43326>



Consider a network with 6 routers *R1* to *R6* connected with links having weights as shown in the following diagram.



Suppose the weights of all unused links are changed to 2 and the distance vector algorithm is used again until all routing tables stabilize. How many links will now remain unused?

- A. 0
- B. 1
- C. 2
- D. 3

gate2010-cse computer-networks routing distance-vector-routing normal

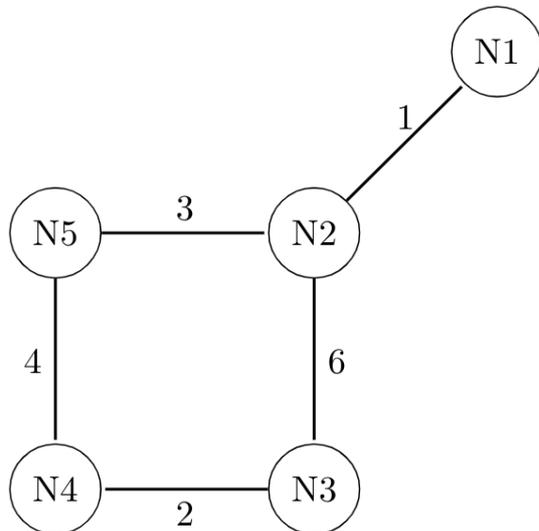
Answer

2.7.3 Distance Vector Routing: GATE CSE 2011 | Question: 52

<https://gateoverflow.in/2160>



Consider a network with five nodes, $N1$ to $N5$, as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

N1: (0, 1, 7, 8, 4)

N2: (1, 0, 6, 7, 3)

N3: (7, 6, 0, 2, 6)

N4: (8, 7, 2, 0, 4)

N5: (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes, $N1$ to $N5$, where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors

with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link $N2 - N3$ reduces to 2 (in both directions). After the next round of updates, what will be the new distance vector at node, $N3$?

- A. (3, 2, 0, 2, 5)
- B. (3, 2, 0, 2, 6)
- C. (7, 2, 0, 2, 5)
- D. (7, 2, 0, 2, 6)

gate2011-cse computer-networks routing distance-vector-routing normal

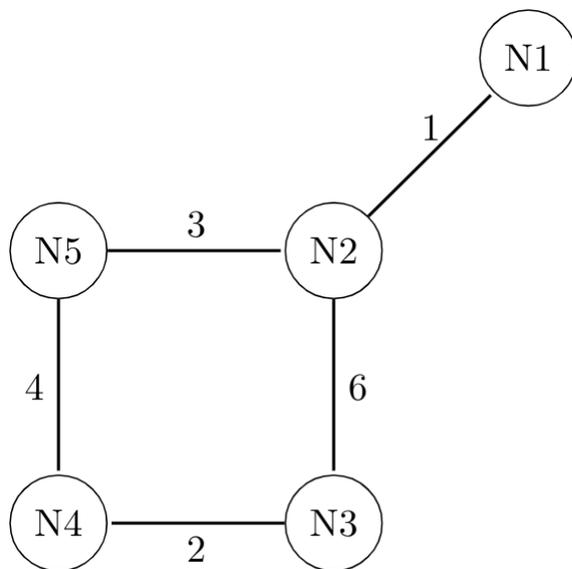
Answer

2.7.4 Distance Vector Routing: GATE CSE 2011 | Question: 53

<https://gateoverflow.in/43317>



Consider a network with five nodes, $N1$ to $N5$, as shown as below.



The network uses a Distance Vector Routing protocol. Once the routes have been stabilized, the distance vectors at different nodes are as follows.

- $N1$: (0, 1, 7, 8, 4)
- $N2$: (1, 0, 6, 7, 3)
- $N3$: (7, 6, 0, 2, 6)
- $N4$: (8, 7, 2, 0, 4)
- $N5$: (4, 3, 6, 4, 0)

Each distance vector is the distance of the best known path at that instance to nodes, $N1$ to $N5$, where the distance to itself is 0. Also, all links are symmetric and the cost is identical in both directions. In each round, all nodes exchange their distance vectors with their respective neighbors. Then all nodes update their distance vectors. In between two rounds, any change in cost of a link will cause the two incident nodes to change only that entry in their distance vectors.

The cost of link $N2 - N3$ reduces to 2 (in both directions). After the next round of updates, the link $N1 - N2$ goes down. $N2$ will reflect this change immediately in its distance vector as cost, ∞ . After the **NEXT ROUND** of update, what will be the cost to $N1$ in the distance vector of $N3$?

- A. 3
- B. 9
- C. 10
- D. ∞

gate2011-cse computer-networks routing distance-vector-routing normal

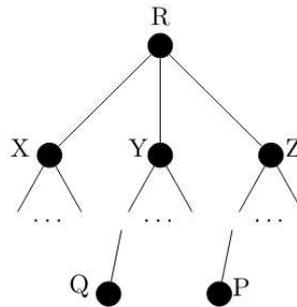
Answer



Consider a computer network using the distance vector routing algorithm in its network layer. The partial topology of the network is shown below.

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The objective is to find the shortest-cost path from the router R to routers P and Q . Assume that R does not initially know the shortest routes to P and Q . Assume that R has three neighbouring routers denoted as X , Y and Z . During one iteration, R measures its distance to its neighbours X , Y , and Z as 3, 2 and 5, respectively. Router R gets routing vectors from its neighbours that indicate that the distance to router P from routers X , Y and Z are 7, 6 and 5, respectively. The routing vector also indicates that the distance to router Q from routers X , Y and Z are 4, 6 and 8 respectively. Which of the following statement(s) is/are correct with respect to the new routing table of R , after updation during this iteration?

- A. The distance from R to P will be stored as 10
- B. The distance from R to Q will be stored as 7
- C. The next hop router for a packet from R to P is Y
- D. The next hop router for a packet from R to Q is Z

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gate2021-cse-set2

multiple-selects

computer-networks

distance-vector-routing

Answer



Count to infinity is a problem associated with:

- A. link state routing protocol.
- B. distance vector routing protocol
- C. DNS while resolving host name
- D. TCP for congestion control

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gate2005-it

computer-networks

routing

distance-vector-routing

normal

Answer

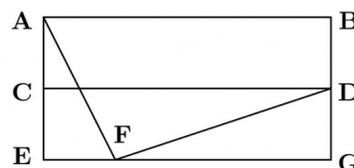


For the network given in the figure below, the routing tables of the four nodes A , E , D and G are shown. Suppose that F has estimated its delay to its neighbors, A , E , D and G as 8, 10, 12 and 6 msec respectively and updates its routing table using distance vector routing technique.

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Routing Table of A

A	0
B	40
C	14
D	17
E	21
F	9
G	24

Routing Table of D

A	20
B	8
C	30
D	0
E	14
F	7
G	22

Routing Table of E

A	24
B	27
C	7
D	20
E	0
F	11
G	22

Routing Table of G

A	21
B	24
C	22
D	19
E	22
F	10
G	0

A.

A	8
B	20
C	17
D	12
E	10
F	0
G	6

B.

A	21
B	8
C	7
D	19
E	14
F	0
G	22

C.

A	8
B	20
C	17
D	12
E	10
F	16
G	6

D.

A	8
B	8
C	7
D	12
E	10
F	0
G	6

gate2007-it computer-networks distance-vector-routing normal

Answer 

Answers: Distance Vector Routing

2.7.1 Distance Vector Routing: GATE CSE 2010 | Question: 54 [top](#)

<https://gateoverflow.in/2362>



✓ Answer (C)

Following will be distance vectors of all nodes.

Shortest Distances from R_1 to R_2, R_3, R_4, R_5 and R_6
 $R_1(5, 3, 12, 12, 16)$

Links used: $R_1 - R_3, R_3 - R_2, R_2 - R_4, R_3 - R_5, R_5 - R_6$

Shortest Distances from R_2 to R_3, R_4, R_5 and R_6
 $R_2(2, 7, 8, 12)$

Links used: $R_2 - R_3, R_2 - R_4, R_4 - R_5, R_5 - R_6$

Shortest Distances from R_3 to R_4, R_5 and R_6

$R_3(9, 9, 13)$

Links used: $R_3 - R_2, R_2 - R_4, R_3 - R_5, R_5 - R_6$

Shortest Distances from R_4 to R_5 and R_6

$R_4(1, 5)$

Links used: $R_4 - R_5, R_5 - R_6$

Shortest Distance from R_5 to R_6

$R_5(4)$

Links Used: $R_5 - R_6$

If we mark, all the used links one by one, we can see that following links are never used.

$R_1 - R_2$

$R_4 - R_6$

👍 50 votes

-- Akhil Nadh PC (16.5k points)

2.7.2 Distance Vector Routing: GATE CSE 2010 | Question: 55 [top](#)

<https://gateoverflow.in/43328>



- ✓ First we need to find which are the unused links in the graph
For that we need not make distance vector tables,
We can do this by simply looking into the graph or else DVT can also give the answer.
So, $R_1 - R_2$ and $R_4 - R_6$ will remain unused.

Now If We changed the unused links to value 2.

$R_5 - R_6$ will Now remain unused.

So, the correct answer is option **B**).

👍 41 votes

-- saif ahmed (3.2k points)

2.7.3 Distance Vector Routing: GATE CSE 2011 | Question: 52 [top](#)

<https://gateoverflow.in/2160>



- ✓ Answer is (A).
1. As soon as $N_2 - N_3$ reduces to 2, both N_2 and N_3 instantly updates their distance to N_3 and N_2 to 2 respectively. So, $N_2: (1, 0, 2, 7, 3), N_3: (7, 2, 0, 2, 6)$ becomes this.

After this starts first round of update in which each node shares its table with their respective neighbors ONLY. BUT KEEP IN MIND THAT ONLY OLD TABLES WILL BE SHARED. What I mean is tables that will be used for update at this moment contain the values as $N_1: (0, 1, 7, 8, 4), N_2: (1, 0, 2, 7, 3), N_3: (7, 2, 0, 2, 6), N_4: (8, 7, 2, 0, 4), N_5: (4, 3, 6, 4, 0)$.

SEE at this time all the entries are old EXCEPT in N_2 and N_3 where value changes to 2 instead of 6.

Question asks for N_3 . So focus on that.

N_3 receives tables from $N_2: (1, 0, 2, 7, 3)$ and $N_4: (8, 7, 2, 0, 4)$. Using THIS ONLY original $N_3: (7, 2, 0, 2, 6)$ updates to $N_3(3, 2, 0, 2, 5)$. (For updation and forming the tables for this refer FOROUZAN.)

So, answer is (A).

👍 68 votes

-- Sandeep_Uniyal (6.5k points)

2.7.4 Distance Vector Routing: GATE CSE 2011 | Question: 53 [top](#)

<https://gateoverflow.in/43317>



- ✓ First, as soon as $N_1 - N_2$ goes down, N_2 and N_1 both update that entry in their tables as infinity. So N_2 at this moment will be $N_2(\text{inf}, 0, 2, _, _)$. I have left blank coz that details are not important.

Now for N_3 to get updated in the subsequent round it will get tables from N_2 and N_4 only. But first we need to find the N_4 calculated in previous update. So in previous question N_4 received updates from N_3 and N_5 which are $N_3: (7, 6, 0, 2, 6), N_5: (4, 3, 6, 4, 0)$.

NOW THIS IS VERY IMPORTANT AS WHY N4 DID NOT GET UPDATED TABLES FROM N3. SO ANSWER IS THAT these tables were shared at the same moment and so in a particular round of update old values of all the tables are used and not the updated values.

N3 was updates AFTER IT PASSED ITS OLD table to its neighbors AS WHY WOULD N4 WAIT FOR N3 to GET UPDATED first !!! **So N4 will update its table (in prev question) to N4(8,7,2,0,4).**

See here path to N1 exists via N5 and not via N3 bcoz when table was shared by N3 it contained path to N1 as 7 and N1 via N3 sums to $7+2=9$. Now when N3 receives tables from N2(inf,0,_,_) and N4(8,7,2,0,4).

At first it will see its distance to N1 as "Inf" and NOT 3 because "inf" is the new distance with the same Next hop N2 **(If next hop is same, new entry is updated even though it is larger than previous entry for the same NEXT HOP).**

But at the same time it sees distance to N1 from N4 as 8 and so updates with the value $(N3-N4 + N4-N1) = (2+8)=10$. So N3-N1 distance in N3(10,_,0,_,_) is 10.

So, answer is (C)

Reference: <http://www.cs.princeton.edu/courses/archive/spr11/cos461/docs/lec14-distvector.pdf>

References



49 votes

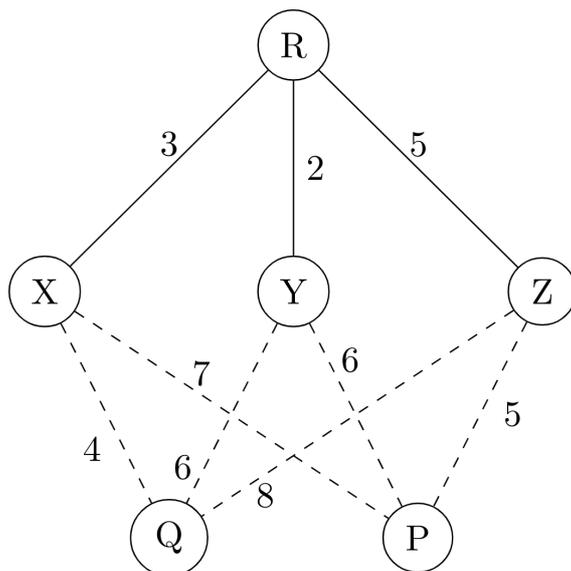
-- Sandeep_Uniyal (6.5k points)

2.7.5 Distance Vector Routing: GATE CSE 2021 Set 2 | Question: 45 top

<https://gateoverflow.in/357495>



✓



As per Distance Vector Routing Algorithm,

$$R \text{ to } P = \min \{ R - X - P, R - Y - P, R - Z - P \} = \min \{ 10, 8, 11 \} = 8 \text{ through } Y.$$

$$R \text{ to } Q = \min \{ R - X - Q, R - Y - Q, R - Z - Q \} = \min \{ 7, 8, 13 \} = 7 \text{ through } X.$$

Hence Options (B) and (C) are correct

3 votes

-- Ashwani Kumar (13k points)

2.7.6 Distance Vector Routing: GATE IT 2005 | Question: 29 top

<https://gateoverflow.in/3775>



✓

Answer is B.

Distance vector routing.

14 votes

-- nagalla pruthvi (675 points)

2.7.7 Distance Vector Routing: GATE IT 2007 | Question: 60 top

<https://gateoverflow.in/3504>



✓ Answer: (A)

Distance from F to F is 0 which eliminates option (C).

Using distance vector routing protocol, $F \rightarrow D \rightarrow B$ yields distance as 20 which eliminates options (B) and (D).

38 votes

-- Rajarshi Sarkar (27.9k points)

2.8

Error Detection (8) top

2.8.1 Error Detection: GATE CSE 1992 | Question: 01.ii top

<https://gateoverflow.in/546>



Consider a 3-bit error detection and 1-bit error correction hamming code for 4-bit data. The extra parity bits required would be _____ and the 3-bit error detection is possible because the code has a minimum distance of _____.

gate1992 computer-networks error-detection normal fill-in-the-blanks

Answer

2.8.2 Error Detection: GATE CSE 1995 | Question: 1.12 top

<https://gateoverflow.in/2599>



What is the distance of the following code 000000, 010101, 000111, 011001, 111111?

- A. 2
- B. 3
- C. 4
- D. 1

gate1995 computer-networks error-detection normal

Answer

2.8.3 Error Detection: GATE CSE 2009 | Question: 48 top

<https://gateoverflow.in/1334>



Let $G(x)$ be the generator polynomial used for CRC checking. What is the condition that should be satisfied by $G(x)$ to detect odd number of bits in error?

- A. $G(x)$ contains more than two terms
- B. $G(x)$ does not divide $1 + x^k$, for any k not exceeding the frame length
- C. $1 + x$ is a factor of $G(x)$
- D. $G(x)$ has an odd number of terms.

gate2009-cse computer-networks error-detection normal

Answer

2.8.4 Error Detection: GATE CSE 2014 Set 3 | Question: 24 top

<https://gateoverflow.in/2058>



A bit-stuffing based framing protocol uses an 8-bit delimiter pattern of 01111110. If the output bit-string after stuffing is 01111100101, then the input bit-string is:

- A. 0111110100
- B. 0111110101
- C. 0111111101
- D. 0111111111

gate2014-cse-set3 computer-networks error-detection

Answer



In a communication network, a packet of length L bits takes link L_1 with a probability of p_1 or link L_2 with a probability of p_2 . Link L_1 and L_2 have bit error probability of b_1 and b_2 respectively. The probability that the packet will be received without error via either L_1 or L_2 is

- A. $(1 - b_1)^L p_1 + (1 - b_2)^L p_2$
- B. $[1 - (b_1 + b_2)^L] p_1 p_2$
- C. $(1 - b_1)^L (1 - b_2)^L p_1 p_2$
- D. $1 - (b_1^L p_1 + b_2^L p_2)$

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gate2005-it computer-networks error-detection probability normal

Answer



An error correcting code has the following code words: 00000000, 00001111, 01010101, 10101010, 11110000 . What is the maximum number of bit errors that can be corrected?

- A. 0
- B. 1
- C. 2
- D. 3

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gate2007-it computer-networks error-detection normal

Answer



Data transmitted on a link uses the following 2D parity scheme for error detection: Each sequence of 28 bits is arranged in a 4×7 matrix (rows r_0 through r_3 , and columns d_7 through d_1) and is padded with a column d_0 and row r_4 of parity bits computed using the Even parity scheme. Each bit of column d_0 (respectively, row r_4) gives the parity of the corresponding row (respectively, column). These 40 bits are transmitted over the data link.

	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	1
r_1	1	1	0	0	1	1	1	0
r_2	0	0	0	1	0	1	0	0
r_3	0	1	1	0	1	0	1	0
r_4	1	1	0	0	0	1	1	0

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The table shows data received by a receiver and has n corrupted bits. What is the minimum possible value of n ?

- A. 1
- B. 2
- C. 3
- D. 4

gate2008-it computer-networks normal error-detection

Answer



Match the pairs in the following questions:

(A) Cyclic Redundancy Code	(p) Error Correction
(B) Serial Communication	(q) Wired-OR
(C) Open Collector	(r) Error detection
(D) Hamming Code	(s) RS-232-C

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Answer 

Answers: Error Detection

2.8.1 Error Detection: GATE CSE 1992 | Question: 01,ii top<https://gateoverflow.in/546>

- ✓ The Hamming distance between two-bit strings is the number of bits that would have to be flipped to make the strings identical.

To **detect** d errors we require a minimum Hamming distance of $d + 1$.**Correcting** d bit flips requires a minimum Hamming distance of $2 \times d + 1$, where d is number of bit in errors.**For the first blank**, each error detection we need 1 parity bit

For 3 bit error detection we need 3 parity bits. So, 3 parity bits requires here.

Also, we can calculate this way, formula is $d + p + 1 \leq 2^p$ where, d = data bits, p = parity bits, $d = 4$ bits given.According to 1st question, $d = 4$ so $4 + p + 1 \leq 2^p$ $p + 5 \leq 2^p$ now if $p = 2$ it becomes $7 \leq 4$, Not possible.If $p = 3$ it becomes $8 \leq 8$, which is possible.So, p must be 3. [Minimum value of p is 3]**The second blank** the 3-bit error detection is possible because the code has a minimum distance of ____ answer is $3 + 1 = 4$, where $d = 3$. Formula used is $d + 1$.**The answer for****2 blanks is**

[3, 4].

 31 votes

-- Bikram (58.4k points)

2.8.2 Error Detection: GATE CSE 1995 | Question: 1.12 top<https://gateoverflow.in/2599>

- ✓ Distance (also called min-distance) of a block code is the minimum number of positions in which any two distinct codes differ. Here, min-distance occurs for the codes 2 and 3 and they differ only in 2 positions. So, $d = 2$.

https://en.wikipedia.org/wiki/Block_code

Correct Answer: A

References

 35 votes

-- Arjun Suresh (332k points)

2.8.3 Error Detection: GATE CSE 2009 | Question: 48 top<https://gateoverflow.in/1334>

- ✓ Let me first explain building blocks to this problem. Before answering this, we should know the relationship between Sent codeword, Received codeword, CRC generator and error polynomial.

let's take an example:

Sent codeword = 10010 ($= x^4 + x$)Received codeword = 10110 (error at 2nd bit) ($= x^4 + x^2 + x$)Now, i can write **Sent codeword = Received codeword + error**

(10010 = 10110 + 00100, here we do modulo 2 arithmetic)

i.e $1 + 1 = 0$ without carry)

in polynomial also we can see $x^4 + x = x^4 + x^2 + x + x^2 = x^4 + 2x^2 + x = x^4 + x$

(**here multiplying with 2 means 0** because it corresponds to binary modulo 2 arithmetic **which is $1+1 = 0$ (not 2)**)

OR

We can also write,

Received codeword = Sent codeword + error (Check it using same method as above)

Sent codeword $C(x)$, Received codeword $R(x)$ and error $E(x)$.

Now we have $R(x) = C(x) + E(x)$. and let CRC polynomial be $G(x)$.

$G(x)$ always divides $C(x)$, and if there is an error then $G(x)$ should not divide $R(x)$.

Lets check -

$R(x) \bmod G(x) = (C(x) + E(x)) \bmod G(x)$ (for simplicity i am writing mod as division)

$$\frac{R(x)}{G(x)} = \frac{C(x)}{G(x)} + \frac{E(x)}{G(x)}$$

$G(x)$ always divides $C(x)$

$$\Rightarrow \frac{R(x)}{G(x)} = 0 + \frac{E(x)}{G(x)}$$

If $G(x)$ divides $E(x)$ also this would mean $G(x)$ divides $R(x)$. We know that, if $G(x)$ does not properly divide $R(x)$ then there is an error but we are never sure if there is error or not when $G(x)$ divides $R(x)$.

As we saw, $G(x)$ divides $R(x)$ or not totally depends on $G(x)$ divides $E(x)$ or not.

Whole strength of $G(x)$ lies if it does not divide any possible $E(x)$.

Lets see again $E(x)$, if there is an error in 3^{rd} and 4^{th} bit from left (LSB is 0th bit) then $E(x) = x^4 + x^3$. (it does not matter error is from toggling 1 to 0 or 0 to 1) **Check with above example.**

Now come to question. it says $G(x)$ should detect odd number of bits in error?.

If number of bits are odd then terms in $E(x)$ would be odd.

for instance if 1^{st} , 2^{nd} and 5^{th} bit got corrupted then $E(x) = x^5 + x^2 + x$.

It is clear that if any function $f(x)$ has a factor of $x - k$, then at $x=k$, $f(x)$ would be zero. I.e. $f(x) = 0$ at $x = k$.

- We want to detect odd number of bits that means received message $R(x)$ contains an odd number of inverted bits, then $E(x)$ must contain an odd number of terms with coefficients equal to 1.
- As a result, $E(1)$ must equal to 1 (**remember $1+1 = 0$, $1+1+1 = 1$.**)
- **Any Odd number of times sum of one's is 1.** $E(1)$ is not zero, this means $x + 1$ is not a factor of $E(x)$.
- Now I want $G(x)$ not to be a factor of $E(x)$, So that $G(x)$ wont divide $E(x)$ and i would happily detect odd number of bits.
- So, if we make sure that $G(1) = 0$, we can conclude that $G(x)$ does not divide any $E(x)$ corresponding to an odd number of error bits. In this case, a CRC based on $G(x)$ will detect any odd number of errors.
- As long as $1 + x$ is a factor of $G(x)$, $G(x)$ can never divide $E(x)$. Because we know $E(x)$ dont have factor of $1 + x$.

Option C.

(**Option B** might confuse you, If $G(x)$ has some factor of the form $x^k + 1$ then also $G(x)$ would detect all odd number of errors, **But in Option B**, language is changed, and that too we should not have any upper bound on k)

👍 77 votes

-- Sachin Mittal (15.8k points)

2.8.4 Error Detection: GATE CSE 2014 Set 3 | Question: 24 [top](#)

<https://gateoverflow.in/2058>



✓ 011111 *one zero emitted here* 0101

Correct Answer: B

👍 38 votes

-- abhishek1317 (267 points)

2.8.5 Error Detection: GATE IT 2005 | Question: 74 [top](#)

<https://gateoverflow.in/3837>



✓ Probability of choosing link $L_1 = p_1$

Probability for no bit error (for any single bit) = $(1 - b_1)$

Similarly for link L_2

Probability of no bit error = $(1 - b_2)$

Packet can go either through link L_1 or L_2 they are mutually exclusive events (means one event happens other won't be happening and so we can simply add their respective probabilities for the favorable case).

Probability packet will be received without any error = Probability of L_1 being chosen and no error in any of the L bits + Probability of L_2 being chosen and no error in any of the L bits

$$= (1 - b_1)^L p_1 + (1 - b_2)^L p_2.$$

Hence, answer is option **A**.

Why option **D** is not correct choice here?

Option **D** here is giving the probability of a frame being arrived with at least one bit correctly - i.e., all the bits are not errors.

👍 79 votes

-- Pooja Palod (24.1k points)

2.8.6 Error Detection: GATE IT 2007 | Question: 43 [top](#)

<https://gateoverflow.in/3478>



✓ **Answer: B**

For correction: $\left\lfloor \frac{(\text{Hamming Distance} - 1)}{2} \right\rfloor$

$= \lfloor 1.5 \rfloor = 1$ bit error.

For detection: Hamming Distance - 1 = 3 bit error.

👍 54 votes

-- Rajarshi Sarkar (27.9k points)

2.8.7 Error Detection: GATE IT 2008 | Question: 66 [top](#)

<https://gateoverflow.in/3380>



✓

	d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0
r_0	0	1	0	1	0	0	1	1
r_1	1	1	0	0	1	1	1	0
r_2	0	0	0	1	0	1	0	0
r_3	0	1	1	0	1	0	1	0
r_4	1	1	0	0	0	0	1	1

Here, we need to change minimum 3 bits, and by doing it we get correct parity column wise and row wise (Correction marked by boxed number)

C is answer

👍 38 votes

-- Prashant Singh (47.2k points)

2.8.8 Error Detection: GATE1987-2-i [top](#)

<https://gateoverflow.in/87074>



✓

(A) Cyclic Redundancy Code	(r) Redundancy checking technique (error detection)
(B) Serial Communication	(s) RS-232-C
(C) Open Collector	(q) Wired OR
(D) Hamming Code	(p) Error Correction Method

Explanation:

A. A **cyclic redundancy check** (CRC) is an error-detecting code commonly used in digital networks and storage devices to

detect accidental changes to raw data

- B. RS-232C is the physical interface that your computer uses to talk to and exchange data with your modem and other serial devices
- C. Reference <http://www.ni.com/white-paper/3544/en/>
- D. The Hamming code is an error correction method using redundant bits. By rearranging the order of bit transmission of the data units, the Hamming code can correct burst errors.

References



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13 votes

-- Lokesh Dafale (8.2k points)

2.9

Ethernet (4) top

2.9.1 Ethernet: GATE CSE 2004 | Question: 54 top

<https://gateoverflow.in/1050>



A and B are the only two stations on an Ethernet. Each has a steady queue of frames to send. Both A and B attempt to transmit a frame, collide, and A wins the first backoff race. At the end of this successful transmission by A , both A and B attempt to transmit and collide. The probability that A wins the second backoff race is:

- A. 0.5
- B. 0.625
- C. 0.75
- D. 1.0

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gate2004-cse computer-networks ethernet probability normal

Answer

2.9.2 Ethernet: GATE CSE 2013 | Question: 36 top

<https://gateoverflow.in/1547>



Determine the maximum length of the cable (in km) for transmitting data at a rate of 500 Mbps in an Ethernet LAN with frames of size 10,000 bits. Assume the signal speed in the cable to be 2,00,000 km/s.

- A. 1
- B. 2
- C. 2.5
- D. 5

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gate2013-cse computer-networks ethernet normal

Answer

2.9.3 Ethernet: GATE CSE 2016 Set 2 | Question: 24 top

<https://gateoverflow.in/39543>



In an Ethernet local area network, which one of the following statements is **TRUE**?

- A. A station stops to sense the channel once it starts transmitting a frame.
- B. The purpose of the jamming signal is to pad the frames that are smaller than the minimum frame size.
- C. A station continues to transmit the packet even after the collision is detected.
- D. The exponential back off mechanism reduces the probability of collision on retransmissions.

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gate2016-cse-set2 computer-networks ethernet normal

Answer

2.9.4 Ethernet: GATE IT 2006 | Question: 19 top

<https://gateoverflow.in/3558>



Which of the following statements is TRUE?

- A. Both Ethernet frame and IP packet include checksum fields
- B. Ethernet frame includes a checksum field and IP packet includes a CRC field

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- C. Ethernet frame includes a CRC field and IP packet includes a checksum field
- D. Both Ethernet frame and IP packet include CRC fields

Answers: Ethernet

2.9.1 Ethernet: GATE CSE 2004 | Question: 54 [top](#)

<https://gateoverflow.in/1050>



✓ [Exponential back-off algorithm](#) is in use here. Here, when a collision occurs:

- each sender sends a jam signal and waits (back-offs) $k \times 51.2\mu s$, where 51.2 is the fixed slot time and k is chosen randomly from 0 to $2^N - 1$ where N is the current transmission number and $1 \leq N \leq 10$. For $11 \leq N \leq 15$, k is chosen randomly from 0 to 1023. For $N = 16$, the sender gives up.

For this question $N = 1$ for A as this is A 's first re-transmission and $N = 2$ for B as this is its second re-transmission. So, possible values of k for A are $\{0, 1\}$ and that for B are $\{0, 1, 2, 3\}$, giving 8 possible combinations of values. Here, A wins the back-off if its k value is lower than that of B as this directly corresponds to the waiting time. This happens for the k value pairs $\{(0, 1), (0, 2), (0, 3), (1, 2), (1, 3)\}$ which is 5 out of 8. So, probability of A winning the second back-off race is $\frac{5}{8} = 0.625$.

Correct Answer: B

References



39 votes

-- Arjun Suresh (332k points)

2.9.2 Ethernet: GATE CSE 2013 | Question: 36 [top](#)

<https://gateoverflow.in/1547>



✓ transmission time \geq round trip time of 1 bit

transmission time $\geq 2 \times$ propagation time

$$\frac{10,000 \text{ bits}}{500 \text{ Mbps}} \geq 2 \times \frac{d}{2 \times 10^5 \text{ km per sec}}$$

$$2 \text{ km} \geq d$$

Option B is correct.

42 votes

-- Amar Vashishth (25.2k points)

2.9.3 Ethernet: GATE CSE 2016 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/39543>



✓ On Ethernet:

- A. This is false because station need not stop to listen to stuff!
- B. No, this is not purpose of jamming signal.
- C. No, stations sends jamming signal if collusion is detected. This is reason why (B) is false.

So, answer is (D).

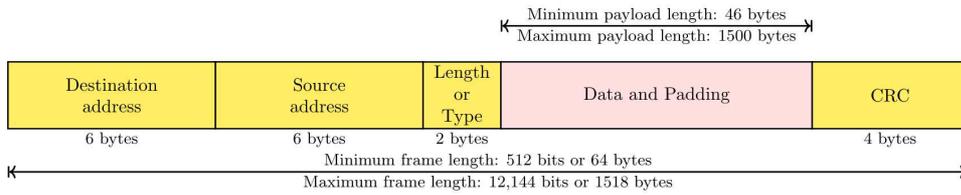
34 votes

-- Akash Kanase (36k points)



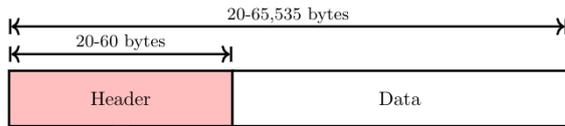
✓ The answer is (C).

Ethernet frame



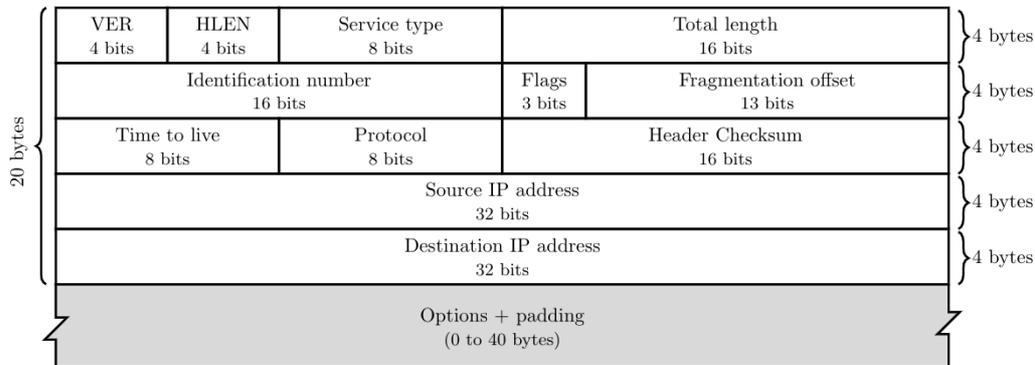
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IP packet



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Fig: IP datagram



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Fig: IP Header format

👍 24 votes

-- Prateek kumar (6.7k points)

2.10

Hamming Code (2) [top](#)

2.10.1 Hamming Code: GATE CSE 1994 | Question: 9 [top](#)



Following 7 bit single error correcting hamming coded message is received.

7	6	5	4	3	2	1	bit No.
1	0	0	0	1	1	0	X

Determine if the message is correct (assuming that at most 1 bit could be corrupted). If the message contains an error find the bit which is erroneous and gives correct message.

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gate1994 computer-networks error-detection hamming-code normal descriptive

Answer

2.10.2 Hamming Code: GATE CSE 2021 Set 1 | Question: 29 [top](#)



Assume that a 12-bit Hamming codeword consisting of 8-bit data and 4 check bits is $d_8d_7d_6d_5c_8d_4d_3d_2c_4d_1c_2c_1$, where the data bits and the check bits are given in the following tables:

Data bits								Check bits			
d_8	d_7	d_6	d_5	d_4	d_3	d_2	d_1	c_8	c_4	c_2	c_1
1	1	0	x	0	1	0	1	y	0	1	0

Which one of the following choices gives the correct values of x and y ?

- A. x is 0 and y is 0
- B. x is 0 and y is 1
- C. x is 1 and y is 0
- D. x is 1 and y is 1

gate2021-cse-set1 computer-networks hamming-code

Answer

Answers: Hamming Code

2.10.1 Hamming Code: GATE CSE 1994 | Question: 9 top

<https://gateoverflow.in/2505>



✓ Here, answer is yes. There is error in This message. Error is in bit 6.

How to calculate it? First of all reverse given input to get it in correct position from 1 to 7.

0110001

Bit-1, Bit-2 & Bit-4 are parity bits.

Calculating position of error \Rightarrow

$C_4 C_2 C_1$

1 1 0

Here, $c_4 = \text{bit}4 \oplus \text{bit}5 \oplus \text{bit}6 \oplus \text{bit}7 = 0 \oplus 0 \oplus 0 \oplus 1 = 1$
(Taking Even parity)

$c_2 = \text{bit}2 \oplus \text{bit}3 \oplus \text{bit}6 \oplus \text{bit}7 = 1 \oplus 1 \oplus 0 \oplus 1 = 1$

$c_1 = \text{bit}1 \oplus \text{bit}3 \oplus \text{bit}5 \oplus \text{bit}7 = 0 \oplus 1 \oplus 0 \oplus 1 = 0$

Reference: \Rightarrow <https://en.wikipedia.org/wiki/Hamming%287,4%29>

When you correct bit 6.

You get a message as 0110011.

If you calculate C_4, C_2, C_1 all will be 0 now!

References



21 votes

-- Akash Kanase (36k points)

2.10.2 Hamming Code: GATE CSE 2021 Set 1 | Question: 29 top

<https://gateoverflow.in/357422>



✓ First I wanna point out a mistake here, it says hamming codeword is 12-bit long, but given codeword sequence is of 13-bit due to repetition of d4 twice (I believe this is a typing error, either they should have write a 13-bit codeword, or d4 occurs only once in this codeword), also 13-bit codeword is very unlikely as it is given in this question, reason: we put check bits at $2^i \forall i \in N$,

But in the given codeword c8 is at 9th position taken from RHS)

Case 1: assume it's a 12-bit codeword and d4 is repeated twice by mistake,

12	11	10	9	8	7	6	5	4	3	2	1
d8	d7	d6	d5	c8	d4	d3	d2	c4	d1	c2	c1
1	1	0	x	y	0	1	0	0	1	1	0

(1) $c_1 + d_1 + d_2 + d_4 + d_5 + d_7$ should be of even parity

$$= 0 + 1 + 0 + 0 + x + 1 = x + 2,$$

x must be 0 for even parity.

(2) $c_2 + d_1 + d_3 + d_4 + d_6 + d_7$ should be even

$$= 1 + 1 + 1 + 0 + 0 + 1 = 4 \text{ (yes)}$$

(3) $c_4 + d_2 + d_3 + d_4 + d_8$ should be even
 $= 0 + 0 + 1 + 0 + 1 = 2$ (yes even)

(4) $c_8 + d_5 + d_6 + d_7 + d_8$ should be even
 $= y + x + 0 + 1 + 1 = y + 2$ (taking $x=0$), for even parity, **y should be 0**

Hence if code work is of 12-bit, both x and y are 0.

A is correct here

Case 2: It's a 13-bit codeword, (I don't think this will be the case, because c_8 should be at position 8), but lets try anyway

13	12	11	10	9	8	7	6	5	4	3	2	1
d8	d7	d6	d5	c8	d4	d4	d3	d2	c4	d1	c2	c1
1	1	0	x	y	0	0	1	0	0	1	1	0

(1) $c_1 + d_1 + d_2 + d_4 + c_8 + d_6 + d_8 = 0 + 1 + 0 + 0 + y + 0 + 1 = y + 2$, **y will be 0.**

(2) $c_2 + d_1 + d_3 + d_4 + d_5 + d_6 = 1 + 1 + 1 + 0 + x + 0 = x + 3$, **x will be 1**

We may conclude C is correct in this case. but i just wanna check it further for other parity bits whether they holds good or not

(3) $c_4 + d_2 + d_3 + d_4 + d_7 + d_8 = 0 + 0 + 1 + 0 + 1 + 1 = 3$ (odd parity), c_4 should be 1 for this to be true, which it isn't)

This case fails, so C is definitely not the answer.

5 votes

-- Nikhil Dhama (2.5k points)

2.11

Icmp (1) top

2.11.1 Icmp: GATE IT 2005 | Question: 26 top

<https://gateoverflow.in/3772>



Traceroute reports a possible route that is taken by packets moving from some host A to some other host B. Which of the following options represents the technique used by traceroute to identify these hosts:

- A. By progressively querying routers about the next router on the path to B using ICMP packets, starting with the first router
- B. By requiring each router to append the address to the ICMP packet as it is forwarded to B. The list of all routers en-route to B is returned by B in an ICMP reply packet
- C. By ensuring that an ICMP reply packet is returned to A by each router en-route to B, in the ascending order of their hop distance from A
- D. By locally computing the shortest path from A to B

gate2005-it computer-networks icmp application-layer-protocols normal

Answer

Answers: Icmp

2.11.1 Icmp: GATE IT 2005 | Question: 26 top

<https://gateoverflow.in/3772>



- ✓ (A) Traceroute works by sending packets with gradually increasing TTL value, starting with TTL value of 1. The first router receives the packet, decrements the TTL value and drops the packet because it then has TTL value zero. The router sends an ICMP Time Exceeded message back to the source. The next set of packets are given a TTL value of 2, so the first router forwards the packets, but the second router drops them and replies with ICMP Time Exceeded. Proceeding in this way, traceroute uses the returned ICMP Time Exceeded messages to build a list of routers that packets traverse, until the destination is reached and returns an [ICMP Echo Reply](#) message.

References



36 votes

-- Shaun Patel (6.1k points)

2.12

Ip Addressing (8) top



Which of the following assertions is FALSE about the Internet Protocol (IP)?

- A. It is possible for a computer to have multiple IP addresses
- B. IP packets from the same source to the same destination can take different routes in the network
- C. IP ensures that a packet is discarded if it is unable to reach its destination within a given number of hops
- D. The packet source cannot set the route of an outgoing packets; the route is determined only by the routing tables in the routers on the way

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gate2003-cse computer-networks ip-addressing normal

Answer



Consider three IP networks A , B and C . Host H_A in network A sends messages each containing 180 bytes of application data to a host H_C in network C . The TCP layer prefixes 20 byte header to the message.

This passes through an intermediate network B . The maximum packet size, including 20 byte IP header, in each network is:

- A: 1000 bytes
- B: 100 bytes
- C: 1000 bytes

The network A and B are connected through a 1 Mbps link, while B and C are connected by a 512 Kbps link (bps = bits per second).



Assuming that the packets are correctly delivered, how many bytes, including headers, are delivered to the IP layer at the destination for one application message, in the best case? Consider only data packets.

- A. 200
- B. 220
- C. 240
- D. 260

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gate2004-cse computer-networks ip-addressing tcp normal

Answer



Consider three IP networks A , B and C . Host H_A in network A sends messages each containing 180 bytes of application data to a host H_C in network C . The TCP layer prefixes 20 byte header to the message. This passes through an intermediate network B . The maximum packet size, including 20 byte IP header, in each network, is:

- A : 1000 bytes
- B : 100 bytes
- C : 1000 bytes

The network A and B are connected through a 1 Mbps link, while B and C are connected by a 512 Kbps link (bps = bits per second).



What is the rate at which application data is transferred to host H_C ? Ignore errors, acknowledgments, and other overheads.

- A. 325.5 Kbps
- B. 354.5 Kbps
- C. 409.6 Kbps
- D. 512.0 Kbps

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gate2004-cse computer-networks ip-addressing tcp normal

Answer

2.12.4 Ip Addressing: GATE CSE 2012 | Question: 23 top

<https://gateoverflow.in/1608>



In the IPv4 addressing format, the number of networks allowed under Class C addresses is:

- A. 2^{14}
- B. 2^7
- C. 2^{21}
- D. 2^{24}

gate2012-cse computer-networks ip-addressing easy

Answer

2.12.5 Ip Addressing: GATE CSE 2013 | Question: 37 top

<https://gateoverflow.in/1548>



In an IPv4 datagram, the M bit is 0, the value of $HLEN$ is 10, the value of total length is 400 and the fragment offset value is 300. The position of the datagram, the sequence numbers of the first and the last bytes of the payload, respectively are:

- A. Last fragment, 2400 and 2789
- B. First fragment, 2400 and 2759
- C. Last fragment, 2400 and 2759
- D. Middle fragment, 300 and 689

gate2013-cse computer-networks ip-addressing normal

Answer

2.12.6 Ip Addressing: GATE CSE 2014 Set 3 | Question: 27 top

<https://gateoverflow.in/2061>



Every host in an IPv4 network has a 1 – second resolution real-time clock with battery backup. Each host needs to generate up to 1000 unique identifiers per second. Assume that each host has a globally unique IPv4 address. Design a 50 – bit globally unique ID for this purpose. After what period (in seconds) will the identifiers generated by a host wrap around?

gate2014-cse-set3 computer-networks ip-addressing numerical-answers normal

Answer

2.12.7 Ip Addressing: GATE CSE 2017 Set 2 | Question: 20 top

<https://gateoverflow.in/118427>



The maximum number of IPv4 router addresses that can be listed in the record route (RR) option field of an IPv4 header is _____.

gate2017-cse-set2 computer-networks ip-addressing numerical-answers

Answer

2.12.8 Ip Addressing: GATE CSE 2018 | Question: 54 top

<https://gateoverflow.in/204129>



Consider an IP packet with a length of 4,500 bytes that includes a 20 – byte IPv4 header and 40 – byte TCP header. The packet is forwarded to an IPv4 router that supports a Maximum Transmission Unit (MTU) of 600 bytes. Assume that the length of the IP header in all the outgoing fragments of this packet is 20 bytes. Assume that the fragmentation offset value stored in the first fragment is 0.

The fragmentation offset value stored in the third fragment is _____.

gate2018-cse computer-networks ip-addressing numerical-answers

Answer

Answers: Ip Addressing



- ✓ In computer networking, source routing, also called path addressing, allows a sender of a packet to partially or completely specify the route of the packet takes through the network. In contrast, in non-source routing protocols, routers in the network determine the path based on the packet's destination.

http://en.wikipedia.org/wiki/Source_routing

Answer is D.

References



👍 35 votes

-- Priya_das (603 points)



- ✓ Packet A sends an IP packet of 180 bytes of data + 20 bytes of TCP header + 20 bytes of IP header to B .

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - $[80 + 20, 80 + 20, 40 + 20]$ and sends to C as the IP packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to C .

Correct Answer: D

👍 70 votes

-- Arjun Suresh (332k points)



- ✓ Packet A sends an IP packet of 180 bytes of data + 20 bytes of TCP header + 20 bytes of IP header to B .

IP layer of B now removes 20 bytes of IP header and has 200 bytes of data. So, it makes 3 IP packets - $[80 + 20, 80 + 20, 40 + 20]$ and sends to C as the IP packet size of B is 100. So, C receives 260 bytes of data which includes 60 bytes of IP headers and 20 bytes of TCP header.

For data rate, we need to consider only the slowest part of the network as data will be getting accumulated at that sender (data rate till that slowest part, we need to add time if a faster part follows a slower part).

So, here 180 bytes of application data are transferred from A to C and this causes 260 bytes to be transferred from B to C .

$$\text{Time to transfer 260 bytes from B-C} = \frac{260 \times 8}{(512 \times 1000)}$$

$$= \frac{65}{16000} = \frac{13}{3200}$$

$$\text{So, data rate} = \frac{180 \times 3200}{13} = 44.3 \text{ kbps} = 44.3 \times 8 = 354.46 \text{ kbps.}$$

Correct Answer: B

👍 67 votes

-- Arjun Suresh (332k points)



- ✓ Answer is (c)

Class	Leading Bits	Size of network number bit field	Size of rest bit field	Number of networks	Addresses per network	Total Addresses in class	Start address	End address
Class A	0	8	24	128 (2^7)	16,777,216 (2^{24})	2,147,483,648 (2^{31})	0.0.0.0	127.255.255.255
Class B	10	16	16	16,384 (2^{14})	65,536 (2^{16})	1,073,741,824 (2^{30})	128.0.0.0	191.255.255.255
Class C	110	24	8	2,097,152 (2^{21})	256 (2^8)	536,870,912 (2^{29})	192.0.0.0	223.255.255.255
Class D	1110	Not defined	Not defined	Not defined	Not defined	268,435,456 (2^{28})	224.0.0.0	239.255.255.255
Class E	1111	Not defined	Not defined	Not defined	Not defined	268,435,456 (2^{28})	240.0.0.0	255.255.255.255

We have 32 bits in the IPV4 network

Class A = 8 network bits + 24 Host bits

Class B = 16 network bits + 16 Host bits

Class C = 24 network bits + 8 host bits

Class D ([multicast](#))

Now for Class C we have 3 bits reserved for the network id.

Hence remaining bits are 21. Therefore total number of networks possible are 2^{21} .

Similarly in Class B we have 2 bits reserved.

Hence, total number of networks in Class B are 2^{14} .

And we have 1 bit reserved in Class A, therefore there are 2^7 networks.

A better reasoning for the bit reservation is given at: https://en.wikipedia.org/wiki/Classful_network

References



👍 53 votes

-- Gate Keeda (15.9k points)

2.12.5 Ip Addressing: GATE CSE 2013 | Question: 37 top ⚡

<https://gateoverflow.in/1548>



- ✓ $M = 0$ meaning no more fragments after this. Hence, its the last fragment.

IHL = internet header length = $10 \times 4 = 40B$ coz 4 is the scaling factor for this field.

Total Length = $400B$

Payload size = Total length - Header length = $400 - 40 = 360B$

fragment offset = $300 \times 8 = 2400B$ = represents how many Bytes are before this. 8 is the scaling factor here.

∴ the first byte # = 2400

Last byte # = first byte # + total bytes in payload - 1 = $2400 + 360 - 1 = 2759$

Option C is correct.

👍 76 votes

-- Amar Vashishth (25.2k points)

2.12.6 Ip Addressing: GATE CSE 2014 Set 3 | Question: 27 top ⚡

<https://gateoverflow.in/2061>



- ✓ Each host needs to generate 1000 unique identifiers per second which requires $\lceil \lg 1000 \rceil = 10$ bits.

Now, these 10 bits along with 32 bit globally unique IP address will give a globally unique 42 bit IDs which stays constant.

Since we are allowed 50 bits we can use the next 8 bits using the clock which changes every second. Thus our IDs will wrap around once in $2^8 = 256$ seconds.

👍 12 votes

-- gatecse (63.3k points)



- ✓ A record-route (RR) option is used to record the Internet routers that handle the datagram. It is listed in OPTIONS of IPv4.

According to RFC 791, there are two cases for the format of an option:

- Case 1: A single octet of option-type.
- Case 2: An option-type octet, an option-length octet, and the actual option-data octets.

In both the cases, first 16 bits of OPTIONS field is used. Therefore, out of 40 Bytes only 38 Bytes are remaining for storing IPv4 addresses. In 38 Bytes we can store 9 IPv4 addresses as each IPv4 address is of 4 Bytes.

∴ 9 should be answer.

Reference: <https://tools.ietf.org/html/rfc791>

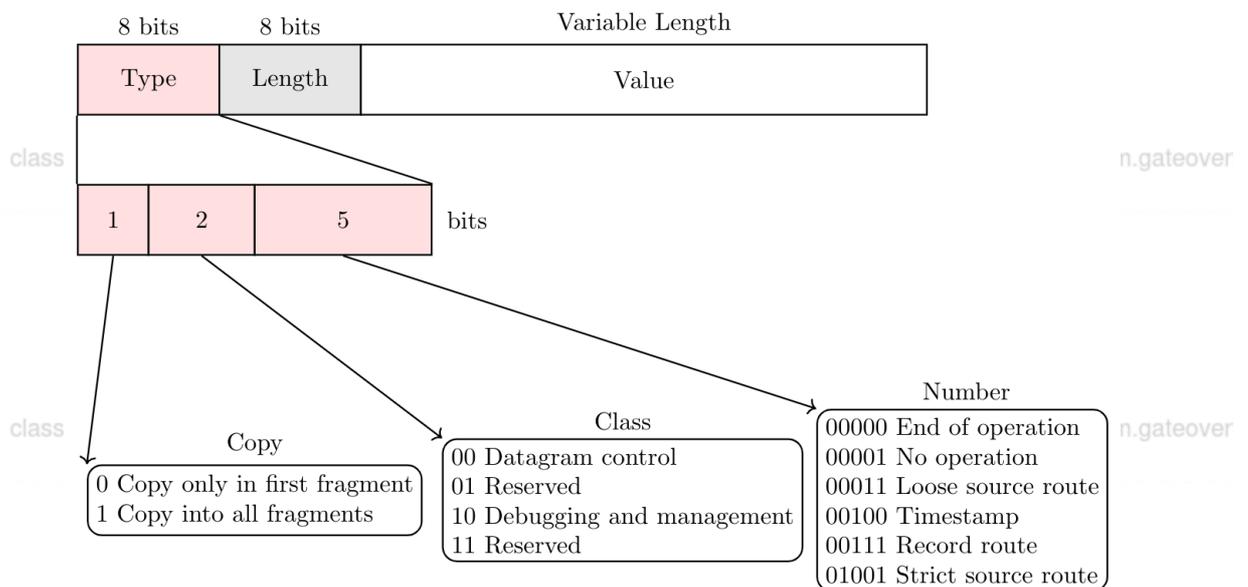


Fig: Option format

References



👍 58 votes

-- Kantikumar (3.4k points)



- ✓ Packet Length = 4500B
IP Payload = 4500 - 20 = 4480B

MTU = 600B

MTU Payload = 600B - 20B = 580B

But payload should be multiple of 8 so number nearest to 580 and multiple of 8 is 576, so MTU payload = 576B

IP Packet size = 576 + 20B = 596B

Size of Offset = $\frac{576}{8} = 72$

1st fragment offset = 0

2nd fragment offset = 72

3rd fragment offset = 144

👍 62 votes

-- Digvijay (44.9k points)

IP Packet = Data + Header

i.e 4500 bytes = 4480 (Data) + 20 (Header) bytes [Given]

Now MTU is 600 bytes.

MTU includes Data + Header

∴ Max data that can be sent is 580 bytes.

However, the total length should be a multiple of 8 (except for the last fragment), because this number will be stored in the Fragmentation offset, which specifies the number of bytes ahead of this fragment.

The nearest number to 580 which is a multiple of 8 is 576

Therefore, the fragmentation will be done in this way ⇒

Fragment#	1	2	3	4	5	6	7	8
Data(B)	576	576	576	576	576	576	576	448
Header Length(B)	20	20	20	20	20	20	20	20
Total Length(B)	596	596	596	596	596	596	596	468
Fragment Offset(B)	0	72	144	216	288	360	432	504
More Fragment	1	1	1	1	1	1	1	0

Since they have mentioned that the first fragment has an offset of 0, the third fragment has an offset value of 144.

👍 31 votes

-- Neelay Upadhyaya (1.1k points)

2.13

Ip Packet (8) top

2.13.1 Ip Packet: GATE CSE 2006 | Question: 5 top

<https://gateoverflow.in/884>



For which one of the following reasons does internet protocol(IP) use the time-to-live(TTL) field in IP datagram header?

- A. Ensure packets reach destination within that time
- B. Discard packets that reach later than that time
- C. Prevent packets from looping indefinitely
- D. Limit the time for which a packet gets queued in intermediate routers

gate2006-cse computer-networks ip-addressing ip-packet easy

Answer

2.13.2 Ip Packet: GATE CSE 2010 | Question: 15. PGEE 2018 top

<https://gateoverflow.in/2188>



One of the header fields in an IP datagram is the Time-to-Live (TTL) field. Which of the following statements best explains the need for this field?

- A. It can be used to prioritize packets.
- B. It can be used to reduce delays.
- C. It can be used to optimize throughput.
- D. It can be used to prevent packet looping.

gate2010-cse computer-networks ip-packet easy

Answer

2.13.3 Ip Packet: GATE CSE 2014 Set 3 | Question: 25 top

<https://gateoverflow.in/2059>



Host A (on TCP/IP v4 network A) sends an IP datagram D to host B (also on TCP/IP v4 network B). Assume that no error occurred during the transmission of D. When D reaches B, which of the following IP header field(s) may be different from that of the original datagram D?

- i. TTL
- ii. Checksum
- iii. Fragment Offset

A. i only

- B. i and ii only
- C. ii and iii only
- D. i, ii and iii

gate2014-cse-set3 computer-networks ip-packet normal

Answer

2.13.4 Ip Packet: GATE CSE 2014 Set 3 | Question: 28 [top](#)

<https://gateoverflow.in/2062>



An IP router with a Maximum Transmission Unit (MTU) of 1500 bytes has received an IP packet of size 4404 bytes with an IP header of length 20 bytes. The values of the relevant fields in the header of the third IP fragment generated by the router for this packet are:

- A. MF bit: 0, Datagram Length: 1444; Offset: 370
- B. MF bit: 1, Datagram Length: 1424; Offset: 185
- C. MF bit: 1, Datagram Length: 1500; Offset: 370
- D. MF bit: 0, Datagram Length: 1424; Offset: 2960

gate2014-cse-set3 computer-networks ip-packet normal

Answer

2.13.5 Ip Packet: GATE CSE 2015 Set 1 | Question: 22 [top](#)

<https://gateoverflow.in/8220>



Which of the following fields of an IP header is NOT modified by a typical IP router?

- A. Check sum
- B. Source address
- C. Time to Live (TTL)
- D. Length

gate2015-cse-set1 computer-networks ip-packet easy

Answer

2.13.6 Ip Packet: GATE CSE 2015 Set 2 | Question: 52 [top](#)

<https://gateoverflow.in/8255>



Host A sends a UDP datagram containing 8880 bytes of user data to host B over an Ethernet LAN. Ethernet frames may carry data up to 1500 bytes (i.e. MTU = 1500 bytes). Size of UDP header is 8 bytes and size of IP header is 20 bytes. There is no option field in IP header. How many total number of IP fragments will be transmitted and what will be the contents of offset field in the last fragment?

- A. 6 and 925
- B. 6 and 7400
- C. 7 and 1110
- D. 7 and 8880

gate2015-cse-set2 computer-networks ip-packet normal

Answer

2.13.7 Ip Packet: GATE CSE 2016 Set 1 | Question: 53 [top](#)

<https://gateoverflow.in/39712>



An IP datagram of size 1000 bytes arrives at a router. The router has to forward this packet on a link whose MTU (maximum transmission unit) is 100 bytes. Assume that the size of the IP header is 20 bytes.

The number of fragments that the IP datagram will be divided into for transmission is _____.

gate2016-cse-set1 computer-networks ip-packet normal numerical-answers

Answer



In the TCP/IP protocol suite, which one of the following is NOT part of the IP header?

- A. Fragment Offset
- B. Source IP address
- C. Destination IP address
- D. Destination port number

gate2004-it computer-networks ip-packet normal

Answer

Answers: Ip Packet



✓ Answer: C

The standard header that is used in *IPv4* contains key information about an Internet Protocol (IP) packet. Information includes the source and destination IP addresses of the datagram, fragmentation control parameters, and packet length. Another key element of this header is the TTL field. The TTL field consists of a single byte and is capable of holding a value from 0–255.

Because IP is connectionless, the TTL field was included in the IP header by the original designers as a mechanism to limit the life span of packets within the network. A routing loop is the most common example used to illustrate why this functionality is required. Without such a control mechanism, a routing loop could cause a packet to circle a network infinitely, depleting bandwidth and eventually destabilizing the network. As insurance against this outcome, the TTL value of an IP datagram is decremented by a value of one each time the packet is forwarded by a network device. Thus, an IP packet can never be forwarded more than 254 times, preventing the infinite packet loop problem.

https://tools.cisco.com/security/center/resources/ttl_expiry_attack.html

References



9 votes

-- Deepak Poonia (23.4k points)



✓ Answer is (D). It can be used to prevent packet looping.

31 votes

-- Sankaranarayanan P.N (8.5k points)



✓ The answer is OPTION D.

Whenever an IP packet is transmitted, the value in Time to Live (TTL) field will be decremented on every single hop. Hence, TTL is changed on every hop.

Now, since TTL changes, hence the Checksum of the packet will also change.

For the Fragmentation offset, A packet will be fragmented if the packet has a size greater than the Maximum Transmission Unit (MTU) of the network. Hence, Fragmentation offset can also be changed.

77 votes

-- saurabhkr (1k points)



✓ IP packet length is given 4404 which includes ip header of length 20
So, data is 4384.

Now, router divide this data in 3 parts
1480 1480 1424

After adding ip header in last packet size is: 1444 and since its the last packet therefore $MF = 0$

And offset is $\frac{2960}{8} = 370$

Correct Answer: A

👍 61 votes

-- annolgate (207 points)

2.13.5 Ip Packet: GATE CSE 2015 Set 1 | Question: 22 top

<https://gateoverflow.in/8220>



✓ Source Address.

👍 38 votes

-- Arjun Suresh (332k points)

2.13.6 Ip Packet: GATE CSE 2015 Set 2 | Question: 52 top

<https://gateoverflow.in/8255>



✓ Answer is C.

Number of fragments = $\left\lceil \frac{8888}{1480} \right\rceil = 7$

Offset of last fragment = $\frac{(1500 - 20) \times 6}{8} = 1110$

(scaling factor of 8 is used in offset field).

TCP or UDP header will be added to the DataUnit received from Transport Layer to Network Layer. And fragmentation happens at Network Layer. So no need to add TCP or UDP header into each fragment.

👍 108 votes

-- Vikrant Singh (11.2k points)

2.13.7 Ip Packet: GATE CSE 2016 Set 1 | Question: 53 top

<https://gateoverflow.in/39712>



✓ IP Datagram size = $1000B$

MTU = $100B$

IP header size = $20B$

So, each packet will have $20B$ header + $80B$ payload.

Therefore, $80 \times 12 = 960$

now remaining $20B$ data could be sent in next fragment.

So, total $12 + 1 = 13$ fragments.

👍 62 votes

-- Monanshi Jain (7k points)

MTU (M) is $80 + 20$ bytes

Datagram size (DS) is $980 + 20$

No. of fragments are $\frac{DS}{M} = \frac{980}{80} = 12.25$

So Answer is 13.

👍 45 votes

-- G VENKATESWARLU (461 points)

2.13.8 Ip Packet: GATE IT 2004 | Question: 86 top

<https://gateoverflow.in/3730>



✓ Answer is D: Destination Port number.

Why? Because the IP header has nothing to do with the port number.

Port numbers are used by the transport layer to ensure process to process delivery.

2.14

Lan Technologies (6) top

2.14.1 Lan Technologies: GATE CSE 2003 | Question: 83 top

<https://gateoverflow.in/966>

A 2 km long broadcast LAN has 10^7 bps bandwidth and uses CSMA/CD. The signal travels along the wire at 2×10^8 m/s. What is the minimum packet size that can be used on this network?

- A. 50 bytes
- B. 100 bytes
- C. 200 bytes
- D. None of the above

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gate2003-cse computer-networks lan-technologies normal

Answer

2.14.2 Lan Technologies: GATE CSE 2007 | Question: 65 top

<https://gateoverflow.in/1263>

There are n stations in slotted LAN. Each station attempts to transmit with a probability p in each time slot. What is the probability that **ONLY** one station transmits in a given time slot?

- A. $np(1-p)^{n-1}$
- B. $(1-p)^{n-1}$
- C. $p(1-p)^{n-1}$
- D. $1 - (1-p)^{n-1}$

tests.gatecse.in goclases.in tests.gatecse.in
gate2007-cse computer-networks lan-technologies probability normal

Answer

2.14.3 Lan Technologies: GATE CSE 2019 | Question: 49 top

<https://gateoverflow.in/302799>

Consider that 15 machines need to be connected in a LAN using 8-port Ethernet switches. Assume that these switches do not have any separate uplink ports. The minimum number of switches needed is _____

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gate2019-cse numerical-answers computer-networks lan-technologies

Answer

2.14.4 Lan Technologies: GATE IT 2004 | Question: 27 top

<https://gateoverflow.in/3668>

A host is connected to a Department network which is part of a University network. The University network, in turn, is part of the Internet. The largest network in which the Ethernet address of the host is unique is

- A. the subnet to which the host belongs
- B. the Department network
- C. the University network
- D. the Internet

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gate2004-it computer-networks lan-technologies ethernet normal

Answer

2.14.5 Lan Technologies: GATE IT 2005 | Question: 28 top

<https://gateoverflow.in/3774>

Which of the following statements is FALSE regarding a bridge?

- A. Bridge is a layer 2 device
- B. Bridge reduces collision domain
- C. Bridge is used to connect two or more LAN segments
- D. Bridge reduces broadcast domain

goclases.in

tests.gatecse.in

Answer 2.14.6 Lan Technologies: GATE IT 2006 | Question: 66 top<https://gateoverflow.in/3610>

A router has two full-duplex Ethernet interfaces each operating at 100 Mb/s. Ethernet frames are at least 84 bytes long (including the Preamble and the Inter-Packet-Gap). The maximum packet processing time at the router for wirespeed forwarding to be possible is (in microseconds)

- A. 0.01
- B. 3.36
- C. 6.72
- D. 8

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tests.gatecse.in

Answer 

Answers: Lan Technologies

2.14.1 Lan Technologies: GATE CSE 2003 | Question: 83 top<https://gateoverflow.in/966>

- ✓ In CSMA/CD, to detect a collision the transmission time (which depends on the packet size) must be greater than twice the propagation delay.

$$\text{Propagation delay here} = \frac{2km}{2 \times 10^8 m/s} = 10 \text{ microseconds}$$

$$\text{Now, transmission time for } x \text{ bytes} = \frac{x \times 8}{10^7} = 0.8x \text{ microseconds}$$

$$\text{So, } 0.8x > 2 \times 10 \implies x > 25 \text{ bytes}$$

So, None of these.

Correct Answer: *D*

 33 votes

-- Arjun Suresh (332k points)

2.14.2 Lan Technologies: GATE CSE 2007 | Question: 65 top<https://gateoverflow.in/1263>

- ✓ Probability that only one station transmits in a given slot = $\binom{n}{1} p^1 (1-p)^{n-1}$

Answer is **option A**.

p for 1 transmitting and $(1-p)$ for $n-1$ non transmitting and n ways to choose 1 from n .

 42 votes

-- Aditi Dan (4k points)

2.14.3 Lan Technologies: GATE CSE 2019 | Question: 49 top<https://gateoverflow.in/302799>

- ✓ Answer is 3.

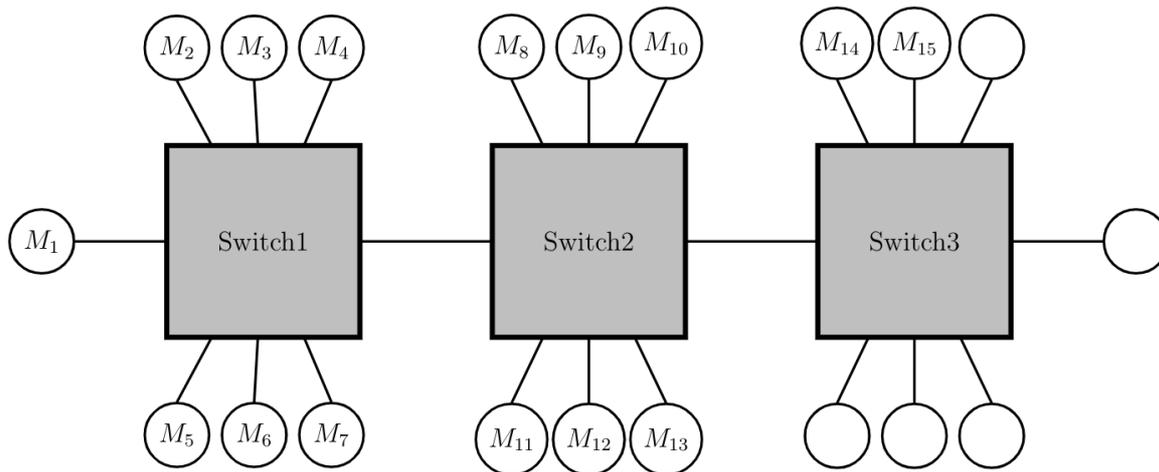
Using 3 switches we can connect maximum 20 machines together.

∴ We require at least 3 switches to connect 15 machines.

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👍 32 votes

-- Tuhin Dutta (9.2k points)

2.14.4 Lan Technologies: GATE IT 2004 | Question: 27 [top](#)

<https://gateoverflow.in/3668>



- ✓ Answer is **D**, Ethernet address is nothing but MAC Address which is present on NIC and it is unique for every network device (a single system might have multiple network cards and each can have its own MAC address).

PS: We can never say Ethernet address is unique only in a network -- because it is independent of the network a device is connected to. That is, if we move a device from one network to another, MAC address remains same. Of course we can do spoofing, but this is not relevant to the asked question.

👍 53 votes

-- Pradyumna Paralikar (297 points)

2.14.5 Lan Technologies: GATE IT 2005 | Question: 28 [top](#)

<https://gateoverflow.in/3774>



- ✓ Bridges are DataLink layer devices used to connect LANs. Bridges are collision domain separator but unable to separate Broadcast domain.

👍 21 votes

-- Digvijay (44.9k points)

2.14.6 Lan Technologies: GATE IT 2006 | Question: 66 [top](#)

<https://gateoverflow.in/3610>



- ✓ Two full-duplex Ethernet interfaces operating at 100 Mbps means the total data transfer rate to the router is 200 Mbps. (Whether full duplex or half, we just need to consider the bandwidth as that determines the speed of data arrival to the router.)

Maximum packet processing time allowed for wirespeed (no delay) forwarding = $\frac{84 \times 8}{200} \mu s = 3.36 \mu s$.

(The router operating at wirespeed means it should be fast enough to process the incoming traffic without causing a delay for transmission)

👍 10 votes

-- gatecse (63.3k points)

Here router has two incoming/outgoing hardware that is full-duplex which means we can send and receive at the same time.

Transmission time is 6.72 (How to get this Transmission time = Packet size / Bandwidth)

Transmission time is time for a packet to get out/in of wire. Also, assume even though the router has two incoming/outgoing hardware but it has a single processing unit.

Now assume that at $t = 0$ router is free. At $t = 6.72$ two packets, p_1 & p_2 arrived from two incoming/outgoing hardware. Now next slot of two packets will arrive at $6.72 + 6.72$ before that processing of these two packets must be completed so that there will not be any kind of delay. Hence we just have 6.72 maximum times to process each packet, hence for each packet, we can devote a maximum of 3.36.

Hence the answer is 3.36.

Now for further explanation, I will show when the first two packets are processed. At $t = 0$ both packets start coming out of

wire, at $t = 6.72$ both packets completely coming out of wire, and we start the processing of one of them (let's say p_1) and next packets p_3, p_4 starts coming out.

At $t = 6.72 + 3.36$ processing of p_1 done, start transmitting it through port 1.

At $t = 6.72 + 6.72$ processing of p_2 done start transmitting it through port 2.

At this time next packets p_3 & p_4 arrived, and we start processing one of them (let's say p_3), at $t=6.72+6.72+3.36$ p_1 completely transmitted., processing of p_3 done, start transmitting it through port 1 (as port 2 is busy in transmitting packet 2)

At $t = 6.72 + 6.72 + 6.72$ transmitting of p_2 done. processing of p_4 done starts transmitting it through port 2, next packets p_5 & p_6 arrived.

.
.
.
continue

👍 124 votes

-- mehul vaidya (3.8k points)

2.15

Link State Routing (1) top ⚡

2.15.1 Link State Routing: GATE CSE 2014 Set 1 | Question: 23 top ⚡

https://gateoverflow.in/1790



Consider the following three statements about link state and distance vector routing protocols, for a large network with 500 network nodes and 4000 links.

[S1]: The computational overhead in link state protocols is higher than in distance vector protocols.

[S2]: A distance vector protocol (with split horizon) avoids persistent routing loops, but not a link state protocol.

[S3]: After a topology change, a link state protocol will converge faster than a distance vector protocol.

Which one of the following is correct about $S1$, $S2$, and $S3$?

- A. $S1$, $S2$, and $S3$ are all true.
- B. $S1$, $S2$, and $S3$ are all false.
- C. $S1$ and $S2$ are true, but $S3$ is false.
- D. $S1$ and $S3$ are true, but $S2$ is false.

gate2014-cse-set1 computer-networks routing distance-vector-routing link-state-routing normal

Answer 🗃

Answers: Link State Routing

2.15.1 Link State Routing: GATE CSE 2014 Set 1 | Question: 23 top ⚡

https://gateoverflow.in/1790



✓ The computational overhead in link state protocols is higher than in distance vector protocols. Bcz LSR is based upon global knowledge whereas DVR is based upon Local info .

Persistent looping can be avoid with the help of split horizon in DVR. But there is no concept of persistent looping in LSR, in LSR only temporary loop exist and can automatically solved by system or router. $S2$ is false.

And, after a topology change, a link state protocol will converge faster than a distance vector protocol. $S3$ is true.

Answer is option **D**.

👍 53 votes

-- Paras Singh (8.9k points)

2.16

Mac Protocol (4) top ⚡

2.16.1 Mac Protocol: GATE CSE 2005 | Question: 74 top ⚡

https://gateoverflow.in/1397



Suppose the round trip propagation delay for a 10 Mbps Ethernet having 48-bit jamming signal is $46.4 \mu s$. The minimum frame size is:

- A. 94
- B. 416

- C. 464
- D. 512

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gate2005-cse computer-networks mac-protocol ethernet

Answer

2.16.2 Mac Protocol: GATE CSE 2015 Set 2 | Question: 8 top

https://gateoverflow.in/8056



A link has transmission speed of 10^6 bits/sec. It uses data packets of size 1000 bytes each. Assume that the acknowledgment has negligible transmission delay and that its propagation delay is the same as the data propagation delay. Also, assume that the processing delays at nodes are negligible. The efficiency of the stop-and-wait protocol in this setup is exactly 25%. The value of the one way propagation delay (in milliseconds) is _____.

gate2015-cse-set2 computer-networks mac-protocol stop-and-wait normal numerical-answers

Answer

2.16.3 Mac Protocol: GATE IT 2004 | Question: 85 top

https://gateoverflow.in/3729



Consider a simplified time slotted MAC protocol, where each host always has data to send and transmits with probability $p = 0.2$ in every slot. There is no backoff and one frame can be transmitted in one slot. If more than one host transmits in the same slot, then the transmissions are unsuccessful due to collision. What is the maximum number of hosts which this protocol can support if each host has to be provided a minimum throughput of 0.16 frames per time slot?

- A. 1
- B. 2
- C. 3
- D. 4

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gate2004-it computer-networks congestion-control mac-protocol normal

Answer

2.16.4 Mac Protocol: GATE IT 2005 | Question: 75 top

https://gateoverflow.in/3838



In a TDM medium access control bus LAN, each station is assigned one time slot per cycle for transmission. Assume that the length of each time slot is the time to transmit 100 bits plus the end-to-end propagation delay. Assume a propagation speed of 2×10^8 m/sec. The length of the LAN is 1 km with a bandwidth of 10 Mbps. The maximum number of stations that can be allowed in the LAN so that the throughput of each station can be $2/3$ Mbps is

- A. 3
- B. 5
- C. 10
- D. 20

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gate2005-it computer-networks mac-protocol normal

Answer

Answers: Mac Protocol

2.16.1 Mac Protocol: GATE CSE 2005 | Question: 74 top

https://gateoverflow.in/1397



✓ The sender must be able to detect a collision before completely sending a frame.

So, the minimum frame length must be such that, before the frame completely leaves the sender any collision must be detected.

Now, the worst case for collision detection is when the start of the frame is about to reach the receiver and the receiver starts sending. Collision happens and a jam signal is produced and this signal must travel to the sender.

The time for this will be the time for the start of the frame to reach near the receiver + time for the jam signal to reach the sender + transmission time for the jam signal.

(We do not need to include transmission time for the frame as as soon as the first bit of the frame arrives, the receiver will have detected it). Time for the start of the frame to reach near the receiver + Time for the jam signal to reach the sender = Round trip propagation delay = $46.4 \mu s$. So,

$$46.4 + \frac{48}{10} (48 \text{ bits at } 10 \text{ Mbps takes } 4.8 \text{ micro sec.}) = 51.2 \mu\text{s}.$$

Now, the frame length must be such that its transmission time must be more than $51.2 \mu\text{s}$.

So, minimum frame length = $51.2 \times 10^{-6} \times 10 \times 10^6 = 512 \text{ bits}$.

- <http://gatecse.in/w/images/3/32/3-MACSublayer.ppt>

A reference question from Peterson Davie:

43. Suppose the round-trip propagation delay for Ethernet is $46.4 \mu\text{s}$. This yields a minimum packet size of 512 bits (464 bits corresponding to propagation delay + 48 bits of jam signal).

- What happens to the minimum packet size if the delay time is held constant, and the signaling rate rises to 100 Mbps?
- What are the drawbacks to so large a minimum packet size?
- If compatibility were not an issue, how might the specifications be written so as to permit a smaller minimum packet size?

Another reference for requiring jam signal bits to be included for minimum frame size.

- <http://intronetworks.cs.luc.edu/current/html/ethernet.html>

Can collision be detected by the source without getting the full jam signal (by a change in current)?

Probably yes. But to be safe (from signal loss) the source waits for the entire jam signal. See below link

- <http://superuser.com/questions/264171/collisions-in-csma-cd-ethernet>

Correct Answer: D.

References



👍 108 votes

-- Arjun Suresh (332k points)

2.16.2 Mac Protocol: GATE CSE 2015 Set 2 | Question: 8 top

<https://gateoverflow.in/8056>



- ✓ In stop and wait, a frame is sent and next frame will be sent only after ACK is received.

$$\text{Efficiency} = \frac{\text{Amount of data sent}}{\text{Amount of data that could be sent}}$$

$$= \frac{\text{Amount of data sent}}{RTT \times 10^6}$$

$$= \frac{\text{Amount of data sent}}{(\text{Prop. delay for data} + \text{Prop. delay for ACK} + \text{Transmission time for data} + \text{Transmission time for ACK}) \times 10^6}$$

$$= \frac{1000 \times 8}{\left(p + p + 1000 \times \frac{8}{10^6} + 0\right) \times 10^6}$$

$$= \frac{8}{2p + 8ms} \text{ (where } p \text{ is the prop. delay in milli seconds)}$$

$$= \frac{4}{p + 4} = 0.25 \text{ (given in question)}$$

$$\text{So, } p + 4 = 16, p = 12ms.$$

41 votes

-- Arjun Suresh (332k points)

2.16.3 Mac Protocol: GATE IT 2004 | Question: 85 top

https://gateoverflow.in/3729



Let there be N such hosts. Then when one host is transmitting then others must be silent for successful transmission. So the throughput per host

$$0.16 = 0.2 \times 0.8^{N-1}$$

$$\implies 0.8 = 0.8^{N-1}$$

on comparing the exponents, since base are identical

$$N - 1 = 1, N = 2.$$

Correct Answer: B

72 votes

-- Shreyans Dhankhar (2.1k points)

2.16.4 Mac Protocol: GATE IT 2005 | Question: 75 top

https://gateoverflow.in/3838



$T_t = 10$ micro secs

$T_p = 5$ micro secs

$$\text{Efficiency of the network} = \frac{T_t}{(T_t + T_p)} = \frac{10}{15} = \frac{2}{3}.$$

Total throughput available for the entire network = Efficiency \times Bandwidth

$$= \frac{2}{3} \times 10 \text{ Mbps} = \frac{20}{3} \text{ Mbps}$$

Let, No. of stations = N (each wants a Throughput of $\frac{2}{3}$ Mbps),

$$N \times \frac{2}{3} \text{ Mbps} = \frac{20}{3} \text{ Mbps} \implies N = 10.$$

$\implies 10$ stations can be connected in the channel at max.

Correct Answer: C

77 votes

-- Ravi Ranjan (3k points)

2.17

Network Flow (5) top

2.17.1 Network Flow: GATE CSE 1992 | Question: 01, v top

https://gateoverflow.in/550



A simple and reliable data transfer can be accomplished by using the 'handshake protocol'. It accomplishes reliable data transfer because for every data item sent by the transmitter _____.

gate1992 computer-networks network-flow easy fill-in-the-blanks

Answer

2.17.2 Network Flow: GATE CSE 2017 Set 2 | Question: 35 top

https://gateoverflow.in/118537



Consider two hosts X and Y , connected by a single direct link of rate 10^6 bits/sec. The distance between the two hosts is $10,000$ km and the propagation speed along the link is 2×10^8 m/sec. Host X sends a file of $50,000$ bytes as one large message to host Y continuously. Let the transmission and propagation delays be p milliseconds and q milliseconds respectively. Then the value of p and q are

- A. $p = 50$ and $q = 100$
- B. $p = 50$ and $q = 400$
- C. $p = 100$ and $q = 50$

D. $p = 400$ and $q = 50$

gate2017-cse-set2 computer-networks network-flow

Answer 

2.17.3 Network Flow: GATE IT 2004 | Question: 80 [top](#) 

<https://gateoverflow.in/3724>



In a data link protocol, the frame delimiter flag is given by 0111. Assuming that bit stuffing is employed, the transmitter sends the data sequence 01110110 as

- A. 01101011
- B. 011010110
- C. 011101100
- D. 0110101100

gate2004-it computer-networks network-flow normal

Answer 

2.17.4 Network Flow: GATE IT 2004 | Question: 87 [top](#) 

<https://gateoverflow.in/3731>



A TCP message consisting of 2100 bytes is passed to IP for delivery across two networks. The first network can carry a maximum payload of 1200 bytes per frame and the second network can carry a maximum payload of 400 bytes per frame, excluding network overhead. Assume that IP overhead per packet is 20 bytes. What is the total IP overhead in the second network for this transmission?

- A. 40 bytes
- B. 80 bytes
- C. 120 bytes
- D. 160 bytes

gate2004-it computer-networks network-flow normal

Answer 

2.17.5 Network Flow: GATE IT 2006 | Question: 67 [top](#) 

<https://gateoverflow.in/3611>



A link of capacity 100 Mbps is carrying traffic from a number of sources. Each source generates an on-off traffic stream; when the source is on, the rate of traffic is 10 Mbps, and when the source is off, the rate of traffic is zero. The duty cycle, which is the ratio of on-time to off-time, is 1 : 2. When there is no buffer at the link, the minimum number of sources that can be multiplexed on the link so that link capacity is not wasted and no data loss occurs is S_1 . Assuming that all sources are synchronized and that the link is provided with a large buffer, the maximum number of sources that can be multiplexed so that no data loss occurs is S_2 . The values of S_1 and S_2 are, respectively,

- A. 10 and 30
- B. 12 and 25
- C. 5 and 33
- D. 15 and 22

gate2006-it computer-networks network-flow normal

Answer 

Answers: Network Flow

2.17.1 Network Flow: GATE CSE 1992 | Question: 01, [top](#) 

<https://gateoverflow.in/550>



✓ The receiver responds that it is ready to receive the data item.

Reference: http://www.sqa.org.uk/e-learning/NetInf101CD/page_28.htm

References



gateoverflow.in

gateoverflow.in

classroom.gateover

9 votes

-- Rajarshi Sarkar (27.9k points)

2.17.2 Network Flow: GATE CSE 2017 Set 2 | Question: 35 top<https://gateoverflow.in/118537>

$$\begin{aligned}
 T_t &= \frac{\text{Length}}{\text{Bandwidth}} \\
 &= \frac{50000 \times 8}{10^6} \\
 &= \frac{40}{100} = 0.4s = 400 \text{ ms} \\
 T_p &= \frac{\text{Distance}}{\text{Velocity}} \\
 &= \frac{10000 \times 10^3}{2 \times 10^8} \\
 &= \frac{1}{20} = 0.05s = 50 \text{ ms}
 \end{aligned}$$

Hence, answer (D) $p = 400, q = 50$.

30 votes

-- Arnabi Bej (5.8k points)

2.17.3 Network Flow: GATE IT 2004 | Question: 80 top<https://gateoverflow.in/3724>

✓ The answer will be option D.

The bit stuffing is done after every two '11' (as the flag is 0111) to differentiate the data part from the flag- there must not be "111" in the data so after every 11 a '0' is added. The receiver also knows this and so, it decodes every "110" as "11". Therefore, option D is the answer.

- http://web.nchu.edu.tw/~pcwang/computer_networks/data_link_layer.pdf
- https://en.wikipedia.org/wiki/High-Level_Data_Link_Control

References



44 votes

-- Gate Keeda (15.9k points)

2.17.4 Network Flow: GATE IT 2004 | Question: 87 top<https://gateoverflow.in/3731>

✓ At source : TCP passes 2100B to IP layer. IP appends 20B header and sends it to DLL and so on. (We are interested in IP overhead, So lets consider DLL header to be negligible)

A router on the way has highest layer as Network Layer, So, complete TCP segment is fragmented. And in question 1200 and 400 are given as **maximum payload without network overhead**, means we are directly given the amount of data part of IP datagram a Frame can hold. [1200 doesn't contain IP header]

Router-1: 2120B reach R_1 's network layer. It removes original IP header, fragments data part at IP and then appends IP header to all fragments and forwards. So, it divides 2100 Bytes into two fragments of size 1200 and 900. And Both fragments are sent to R_2 .

Router-2: Both fragments that reach R_2 exceed MTU at R_2 . So, both are fragmented. First packet of 1200B is fragmented into 3 packets of 400, 400 and 400 Bytes respectively and Second packet of 900B is fragmented into three fragments of 400, 400 and 100 Bytes respectively.

Original data during fragmentation should not change. Only additional IP headers are added. So totally 6 packets reach destination. And IP header is also an overhead because our main aim is to send data only.

Total IP Overhead = $6 * 20 = 120$ B

Hence, (C) is correct answer.

<http://quiz.geeksforgeeks.org/gate-gate-it-2004-question-87/>

classroom.gateover

References



64 votes

-- Manish Joshi (20.5k points)

2.17.5 Network Flow: GATE IT 2006 | Question: 67 [top](#)

<https://gateoverflow.in/3611>



✓ Since there is no buffer and constraint given is there should not be any data lost, and no wastage of capacity as well.

Since data should not be lost, we calculate for the extreme case when all sources are on (that is transmitting).

$$10 \text{ Mbps} \times n\text{-station} \leq 100 \text{ Mbps}$$

$$\Rightarrow n\text{-station} = 10$$

In the next part of the question it is given that the link is provided with large buffer and we are asked to find out the maximum number of stations.

For this we'll calculate the expected value of bandwidth usage (if more data comes we store in buffer and due to expectation, the buffer will be emptied soon or in other words buffer space will never run out):

$$E = \frac{1}{3} \times 10 + \frac{1}{3} \times 10 + \dots n\text{-station times} \leq 100 \text{ Mbps}$$

$$[\text{total time is } (1 + 2) = 3 \text{ then on time is } 1 \text{ so } \frac{1}{3} \text{ of BW}]$$

$$\Rightarrow \frac{1}{3} \times 10 \times n\text{-station} \leq 100 \text{ Mbps}$$

$$\Rightarrow n\text{-station} = 30$$

So, option (A) is answer.

49 votes

-- Vicky Bajoria (4.1k points)

2.18

Network Layering (6) [top](#)

2.18.1 Network Layering: GATE CSE 2003 | Question: 28 [top](#)

<https://gateoverflow.in/918>



Which of the following functionality *must* be implemented by a transport protocol over and above the network protocol?

- A. Recovery from packet losses
- B. Detection of duplicate packets
- C. Packet delivery in the correct order
- D. End to end connectivity

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Answer

2.18.2 Network Layering: GATE CSE 2004 | Question: 15 [top](#)

<https://gateoverflow.in/1012>



Choose the best matching between Group 1 and Group 2

Group-1	Group-2
P. Data link layer	1. Ensures reliable transport of data over a physical point-to-point link
Q. Network layer	2. Encodes/decodes data for physical transmission
R. Transport layer	3. Allows end-to-end communication between two processes
	4. Routes data from one network node to the next

- A. P-1, Q-4, R-3
- B. P-2, Q-4, R-1
- C. P-2, Q-3, R-1
- D. P-1, Q-3, R-2

gate2004-cse computer-networks network-layering normal

Answer

2.18.3 Network Layering: GATE CSE 2007 | Question: 70 top

<https://gateoverflow.in/1268>



Match the following:

- | | |
|----------|-----------------------|
| (P) SMTP | (1) Application layer |
| (Q) BGP | (2) Transport layer |
| (R) TCP | (3) Data link layer |
| (S) PPP | (4) Network layer |
| | (5) Physical layer |

- A. P - 2, Q - 1, R - 3, S - 5
- B. P - 1, Q - 4, R - 2, S - 3
- C. P - 1, Q - 4, R - 2, S - 5
- D. P - 2, Q - 4, R - 1, S - 3

gate2007-cse computer-networks network-layering network-protocols easy

Answer

2.18.4 Network Layering: GATE CSE 2013 | Question: 14 top

<https://gateoverflow.in/1436>



Assume that source S and destination D are connected through two intermediate routers labeled R. Determine how many times each packet has to visit the network layer and the data link layer during a transmission from S to D.

- A. Network layer – 4 times and Data link layer – 4 times
- B. Network layer – 4 times and Data link layer – 3 times
- C. Network layer – 4 times and Data link layer – 6 times
- D. Network layer – 2 times and Data link layer – 6 times

gate2013-cse computer-networks network-layering normal

Answer

2.18.5 Network Layering: GATE CSE 2014 Set 3 | Question: 23 top

<https://gateoverflow.in/2057>



In the following pairs of OSI protocol layer/sub-layer and its functionality, the **INCORRECT** pair is

- A. Network layer and Routing
- B. Data Link Layer and Bit synchronization
- C. Transport layer and End-to-end process communication
- D. Medium Access Control sub-layer and Channel sharing

gate2014-cse-set3 computer-networks network-layering easy

Answer



Match the following:

Field	Length in bits
P. UDP Header's Port Number	I. 48
Q. Ethernet MAC Address	II. 8
R. IPv6 Next Header	III. 32
S. TCP Header's Sequence Number	IV. 16

- A. P-III, Q-IV, R-II, S-I
 B. P-II, Q-I, R-IV, S-III
 C. P-IV, Q-I, R-II, S-III
 D. P-IV, Q-I, R-III, S-II

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network-layering

normal

Answer

Answers: Network Layering



- ✓ **Answer(D)** TCP and UDP are transport layer protocols.

Question is asking which service must be provided by transport layer so that source can successfully communicate to destination. UDP is a connection-less protocol but it's a transport layer protocol so that from here we can say that reliability is not a service that MUST be provided by transport layer protocols. with that same argument cut all those options in which such a service is mentioned which UDP doesn't provide so only (D) remain so it's the answer..

other way to answer is ' for Process to Process delivery transport layer service is MUST otherwise there is no way to deliver the data to right process'.. if reliability is in danger data can survive (Data link layer also take care about errors so we can compromise error recovery at transport layer), if there are duplicate packets , yet data can survive ,only bandwidth is wasted, if packets are delivered out of order data can survive but if data of process A is delivered to process B , data can't survive.... "to Assigning port numbers" Transport layer service is MUST...

64 votes

-- Rupendra Choudhary (11.4k points)



- ✓ Answer is A.

21 votes

-- Aditi Dan (4k points)



- ✓ **Answer is B.**

- [SMTP](#) is an application layer protocol used for e-mail transmission.
- [TCP](#) is a core transport layer protocol.
- [BGP](#) is a network layer protocol backing the core routing decisions on the Internet.
- [PPP](#) is a data link layer protocol commonly used in establishing a direct connection between two networking.

References

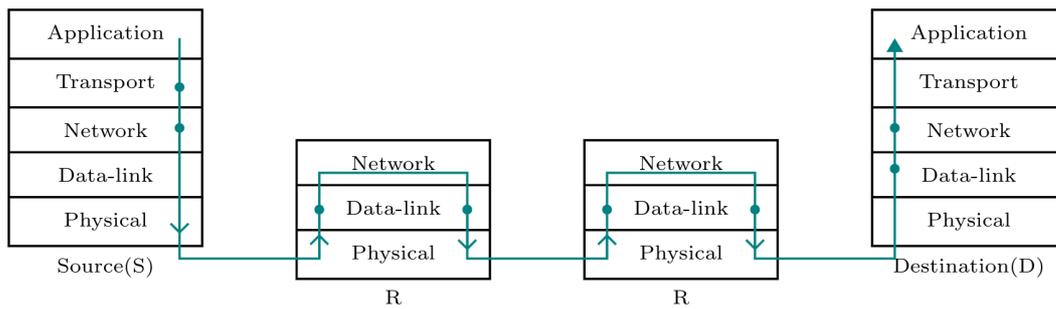


33 votes

-- naga praveen (2.8k points)



✓



C is the Answer.

👍 68 votes

-- Mithlesh Upadhyay (4.3k points)



✓

- A. One of the main functionality of Network Layer is Routing. So, option (A) is CORRECT.
 B. Bit Synchronization is always handled by Physical Layer of OSI model but not Data Link Layer. So, option (B) is INCORRECT.
 C. End – to – End Process Communication is handled by Transport Layer. So, option (C) is CORRECT.
 D. MAC sub layer have 3 types of protocols (Random, Controlled and Channelized Access).

So, option (B) is incorrect pair.

👍 33 votes

-- Çşê çâtê (1.7k points)



✓

UDP header - 16 bits

MAC address: 48 bits

IPv6 next header: 8 bits

TCP Sequence No.: 32 bits

Answer: (C) P:IV, Q:I, R:II, S:III

👍 29 votes

-- Prateek Kumar (1.1k points)



The address resolution protocol (ARP) is used for:

- A. Finding the IP address from the DNS
 B. Finding the IP address of the default gateway
 C. Finding the IP address that corresponds to a MAC address
 D. Finding the MAC address that corresponds to an IP address

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Answer



Which one of the following uses UDP as the transport protocol?

- A. HTTP

- B. Telnet
- C. DNS
- D. SMTP

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tests.gatecse.in

Answer 

2.19.3 Network Protocols: GATE CSE 2015 Set 1 | Question: 17 [top](#)

<https://gateoverflow.in/8214>



In one of the pairs of protocols given below, both the protocols can use multiple TCP connections between the same client and the server. Which one is that?

- A. HTTP, FTP
- B. HTTP, TELNET
- C. FTP, SMTP
- D. HTTP, SMTP

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gate2015-cse-set1 computer-networks network-protocols normal

Answer 

2.19.4 Network Protocols: GATE CSE 2016 Set 1 | Question: 24 [top](#)

<https://gateoverflow.in/39639>



Which one of the following protocols is **NOT** used to resolve one form of address to another one?

- A. DNS
- B. ARP
- C. DHCP
- D. RARP

gate2016-cse-set1 computer-networks network-protocols normal

goclases.in

tests.gatecse.in

Answer 

2.19.5 Network Protocols: GATE CSE 2019 | Question: 29 [top](#)

<https://gateoverflow.in/302819>



Suppose that in an IP-over-Ethernet network, a machine X wishes to find the MAC address of another machine Y in its subnet. Which one of the following techniques can be used for this?

- A. X sends an ARP request packet to the local gateway's IP address which then finds the MAC address of Y and sends to X
- B. X sends an ARP request packet to the local gateway's MAC address which then finds the MAC address of Y and sends to X
- C. X sends an ARP request packet with broadcast MAC address in its local subnet
- D. X sends an ARP request packet with broadcast IP address in its local subnet

gate2019-cse computer-networks network-protocols

Answer 

2.19.6 Network Protocols: GATE CSE 2021 Set 1 | Question: 49 [top](#)

<https://gateoverflow.in/357402>



Consider the sliding window flow-control protocol operating between a sender and a receiver over a full-duplex error-free link. Assume the following:

- The time taken for processing the data frame by the receiver is negligible.
- The time taken for processing the acknowledgement frame by the sender is negligible.
- The sender has infinite number of frames available for transmission.
- The size of the data frame is 2,000 bits and the size of the acknowledgement frame is 10 bits.
- The link data rate in each direction is 1 Mbps ($= 10^6$ bits per second).
- One way propagation delay of the link is 100 milliseconds.

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The minimum value of the sender's window size in terms of the number of frames, (rounded to the nearest integer) needed to achieve a link utilization of 50% is _____.

gate2021-cse-set1 computer-networks network-protocols sliding-window numerical-answers

Answer 

2.19.7 Network Protocols: GATE CSE 2021 Set 1 | Question: 8 [top](#) 

<https://gateoverflow.in/357444>



Consider the following two statements.

- S_1 : Destination MAC address of an ARP reply is a broadcast address.
- S_2 : Destination MAC address of an ARP request is a broadcast address.

Which one of the following choices is correct?

- A. Both S_1 and S_2 are true
- B. S_1 is true and S_2 is false
- C. S_1 is false and S_2 is true
- D. Both S_1 and S_2 are false

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computer-networks

network-protocols

Answer 

2.19.8 Network Protocols: GATE IT 2007 | Question: 69 [top](#) 

<https://gateoverflow.in/3514>



Consider the following clauses:

- i. Not inherently suitable for client authentication.
- ii. Not a state sensitive protocol.
- iii. Must be operated with more than one server.
- iv. Suitable for structured message organization.
- v. May need two ports on the server side for proper operation.

The option that has the maximum number of correct matches is [classes.in](#)

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- A. IMAP-i; FTP-ii; HTTP-iii; DNS-iv; POP3-v
- B. FTP-i; POP3-ii; SMTP-iii; HTTP-iv; IMAP-v
- C. POP3-i; SMTP-ii; DNS-iii; IMAP-iv; HTTP-v
- D. SMTP-i; HTTP-ii; IMAP-iii; DNS-iv; FTP-v

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network-protocols

normal

Answer 

2.19.9 Network Protocols: GATE IT 2008 | Question: 68 [top](#) 

<https://gateoverflow.in/3382>



Which of the following statements are TRUE?

- **S1**: TCP handles both congestion and flow control
- **S2**: UDP handles congestion but not flow control
- **S3**: Fast retransmit deals with congestion but not flow control
- **S4**: Slow start mechanism deals with both congestion and flow control

- A. S_1 , S_2 and S_3 only
- B. S_1 and S_3 only
- C. S_3 and S_4 only
- D. S_1 , S_3 and S_4 only

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network-protocols

normal

Answer 

Answers: Network Protocols

2.19.1 Network Protocols: GATE CSE 2005 | Question: 24 [top](#) 

<https://gateoverflow.in/1360>



- ✓ The address resolution protocol (**ARP**) is a protocol used by the Internet Protocol (IP) specifically IPv4, to map IP network addresses to the hardware addresses used by a data link protocol.

Show that option D is correct.

Ref: <http://www.erg.abdn.ac.uk/users/gorry/course/inet-pages/arp.html>

References



16 votes

-- Brij Mohan Gupta (1.7k points)

2.19.2 Network Protocols: GATE CSE 2007 | Question: 20 top

<https://gateoverflow.in/1218>



✓ The answer is C.

Where quick response is needed, there UDP is preferred.

33 votes

-- Gate Keeda (15.9k points)

2.19.3 Network Protocols: GATE CSE 2015 Set 1 | Question: 17 top

<https://gateoverflow.in/8214>



✓ **SMTP:** only one TCP connection.

Reference: <https://tools.ietf.org/html/rfc821>

TELNET: only one TCP connection.

Reference: <https://tools.ietf.org/html/rfc854>

HTTP: Multiple connections can be used for each resource.

Reference: <http://www.w3.org/Protocols/rfc2616/rfc2616-sec1.html#sec1>

FTP: FTP uses Telnet protocol for Control info on a TCP connection and another TCP connection for data exchange

Reference: <https://tools.ietf.org/html/rfc959> (See page 8)

So, answer is A.

References



61 votes

-- Arjun Suresh (332k points)

2.19.4 Network Protocols: GATE CSE 2016 Set 1 | Question: 24 top

<https://gateoverflow.in/39639>



- ✓
- A) DNS - host name to IP address
 - B) ARP - IP to MAC
 - D) RARP - MAC to IP

So **ANSWER** is C

34 votes

-- Abhilash Panicker (7.6k points)

2.19.5 Network Protocols: GATE CSE 2019 | Question: 29 top

<https://gateoverflow.in/302819>



✓ Steps in ARP Operation :

1. The sender (X) knows its own IP address and MAC address. X also knows the IP address of the target (Y) . It needs to find MAC address of Y

2. IP asks ARP to create an ARP request message, filling in X's IP and MAC address and Y's IP address. **The destination MAC address is set to all 0s.**
3. The message is passed to Data Link layer where it is encapsulated in a frame using MAC address of X as the source address and **physical broadcast address (all 1s)** as the destination address.
4. Every host in subnet receives the request message because we have used broadcast MAC address in the destination address. All machines except Y (we have specified Y's IP address in our ARP request message) drop the ARP request message.
5. Y replies with an ARP reply message that contains its MAC address.
6. When X receives this message, it gets to know the MAC address of Y.

Please note that, a host uses its own IP address and network mask to decide if target IP address is in its own network or not.

If it is in its network, it uses ARP to resolve the MAC address.

If target IP address is not in its network, it takes the help of default gateway to resolve MAC address using ARP.

Since in question it is clearly mentioned that X (source) and Y (destination) both are in the same subnet, we need not send ARP request message targeted at gateway and then expect it to give the MAC address of Y to X.

So the correct answer is option C.

👍 56 votes

-- NabilSayyad (761 points)

2.19.6 Network Protocols: GATE CSE 2021 Set 1 | Question: 49 [top](#)

<https://gateoverflow.in/357402>



- ✓ Let the sender window size be N .

One way propagation delay = $100\text{ ms} = 0.1\text{ s}$

$$\text{Transmission delay}_{\text{packet}} = \frac{\text{Size of data frame}}{\text{Link bit rate}} = \frac{2000}{10^6} = 0.002\text{ s}$$

$$\text{Transmission delay}_{\text{ACK}} = \frac{\text{Size of ACK frame}}{\text{Link bit rate}} = \frac{10}{10^6} = 0.00001\text{ s}$$

$$\text{Link Utilization}(\eta) = \frac{\text{Useful Data Transfer time}}{\text{Total time}}$$

$$\Rightarrow \eta = \frac{N \cdot (T_f)}{T_f + 2(T_p) + T_{ACK}}$$

$$\Rightarrow N = \left\lceil \frac{\eta \cdot (T_f + 2(T_p) + T_{ACK})}{T_f} \right\rceil = \left\lceil \frac{0.5(0.002 + 0.2 + 0.00001)}{0.002} \right\rceil = \lceil 50.5025 \rceil = 51$$

Correct Answer: 51

👍 4 votes

-- Konan-kun (191 points)

2.19.7 Network Protocols: GATE CSE 2021 Set 1 | Question: 8 [top](#)

<https://gateoverflow.in/357444>



- ✓ In ARP, source broadcasts an ARP request to all devices in local subnet.

The destination which has the matching IP address then sends an ARP response which includes the MAC address of the source and hence is a unicast message.

Option (C) S1 is false and S2 is true

👍 2 votes

-- Ashwani Kumar (13k points)

2.19.8 Network Protocols: GATE IT 2007 | Question: 69 [top](#)

<https://gateoverflow.in/3514>



- ✓ They are asking for maximum correct matches so
 - i. Should be HTTP thus we use HTTPS.
 - ii. HTTP as it does not depend on state of device or operating system.
 - iii. IMAP or DNS* Not sure but they may involve multiple servers.
 - iv. POP3 is suitable for structuring or arranging the folders.
 - v. FTP needs two ports, 20 for data and 21 for control.

Thus, **Option D**, As it's matching with HTTP-2, IMAP-3, FTP-5.

2.19.9 Network Protocols: GATE IT 2008 | Question: 68 top

<https://gateoverflow.in/3382>



- ✓ (S1) TCP handles both congestion and flow control \Rightarrow True.
It uses congestion window for congestion control & Advertisement window for flow control
 - (S2) UDP handles congestion but not flow control \Rightarrow UDP does not handle congestion but also not handle flow control.
 - (S3) Fast retransmit deals with congestion but not flow control \Rightarrow Yes.
Fast Retransmit is technique for detecting out of Order Datagram & Sending it. It is congestion control technique and has no relation with Flow control
 - (S4) Slow start mechanism deals with both congestion and flow control \Rightarrow False.
It has nothing to do with Flow control. Flow control is taken care by Advertisement window. Slow start is way Sender tries to gauge network capacity !
- Answer (B) S1 and S3 only.**

2.20 Network Switching (4) top

2.20.1 Network Switching: GATE CSE 2005 | Question: 73 top

<https://gateoverflow.in/1396>



In a packet switching network, packets are routed from source to destination along a single path having two intermediate nodes. If the message size is 24 bytes and each packet contains a header of 3 bytes, then the optimum packet size is:

- A. 4
- B. 6
- C. 7
- D. 9

gate2005-cse computer-networks network-switching normal

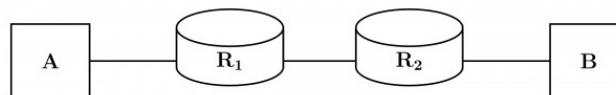
Answer

2.20.2 Network Switching: GATE CSE 2014 Set 2 | Question: 26 top

<https://gateoverflow.in/1985>



Consider the store and forward packet switched network given below. Assume that the bandwidth of each link is 10^6 bytes/sec. A user on host *A* sends a file of size 10^3 bytes to host *B* through routers *R1* and *R2* in three different ways. In the first case a single packet containing the complete file is transmitted from *A* to *B*. In the second case, the file is split into 10 equal parts, and these packets are transmitted from *A* to *B*. In the third case, the file is split into 20 equal parts and these packets are sent from *A* to *B*. Each packet contains 100 bytes of header information along with the user data. Consider only transmission time and ignore processing, queuing and propagation delays. Also assume that there are no errors during transmission. Let T_1 , T_2 and T_3 be the times taken to transmit the file in the first, second and third case respectively. Which one of the following is CORRECT?



- A. $T_1 < T_2 < T_3$
- B. $T_1 > T_2 > T_3$
- C. $T_2 = T_3, T_3 < T_1$
- D. $T_1 = T_3, T_3 > T_2$

gate2014-cse-set2 computer-networks network-switching normal

Answer

2.20.3 Network Switching: GATE CSE 2015 Set 3 | Question: 36 top

<https://gateoverflow.in/8495>



Two hosts are connected via a packet switch with 10^7 bits per second links. Each link has a propagation delay of 20 microseconds. The switch begins forwarding a packet 35 microseconds after it receives the same. If 10000 bits of data are to be transmitted between the two hosts using a packet size of 5000 bits, the time elapsed between the transmission of the first bit of data and the reception of the last bit of the data in microseconds is _____.

Answer 2.20.4 Network Switching: GATE IT 2004 | Question: 22 [top](#)<https://gateoverflow.in/3663>

Which one of the following statements is FALSE?

- A. Packet switching leads to better utilization of bandwidth resources than circuit switching
- B. Packet switching results in less variation in delay than circuit switching
- C. Packet switching requires more per-packet processing than circuit switching
- D. Packet switching can lead to reordering unlike in circuit switching

ooclasses.in

tests.gatecse.in

Answer 

Answers: Network Switching

2.20.1 Network Switching: GATE CSE 2005 | Question: 73 [top](#)<https://gateoverflow.in/1396>✓ **Correct answer should be option D.**

As we know in packet switching- dividing message into packets decrease the transmission time due to pipelined transmission.

but if there are many packets beyond some threshold then transmission time may increase. So, we can do by option checking

1. packet size = 4 = packet data + header size = 1 + 3

So no. of packets will be = $\frac{\text{message}}{\text{packet data}}$

$$= \frac{24}{1} = 24 \text{ packets.}$$

So, time to reach at receiver for 1st packet will be,

$$= 3 (\text{source} + \text{two intermediate node}) \times \text{transmission time}$$

$TT = \frac{L}{BW}$... Here, L will be changed according to option and BW will remain same ..

So time to reach at receiver for 1st packet will be = $\frac{3 \times 4}{BW} = \frac{12}{BW}$

and for remaining 23 packets will take time = $23 \times TT = \frac{23 \times 4}{BW} = \frac{92}{BW}$

$$\text{TOTAL TIME} = \frac{104}{BW}$$

2. packet size = 6 = 3 + 3 (packet data + header size) so no of packets will be 8.

Time to reach at receiver for 1st packet will be = $\frac{3 \times 6}{BW} = \frac{18}{BW}$

and for remaining 7 packet will take time = $\frac{7 \times 6}{BW} = \frac{42}{BW}$

$$\text{Total time} = \frac{60}{BW}$$

3. packet size = 7 = 4 + 3, so no of packets = $\frac{24}{4} = 6$ packets

For 1st packet time will be = $\frac{3 \times 7}{BW} = \frac{21}{BW}$

For remaining 5 packet will take time = $\frac{5 \times 7}{BW} = \frac{35}{BW}$

$$\text{Total time} = \frac{56}{BW}$$

4. packet size = 9 = 6 + 3, so no of packet will be 4.

For 1st packet time will be = $\frac{3 \times 9}{BW} = \frac{27}{BW}$

For remaining 3 packets will take time = $\frac{3 \times 9}{BW} = \frac{27}{BW}$

TOTAL time = $\frac{54}{BW}$

So, optimal packet size will be 9 byte due to less total transmission time.

Alternate method (thanks to sachin)

In that case we can do it using minimisation of a variable.

Let, 24 byte data is divided into number of packets each have x bytes of data.

Therefore, packet size = $x + 3$, and Number of packets (k) = $\frac{24}{x}$.

(it is ceil, if 24 is not multiple of x)

Total time = $3(x + 3) + (k - 1)(x + 3)$ (assumed $BW = 1$, just to avoid writing 'BW' again and again)

(ignoring propagation delay as it has nothing to do with packet size, if one wish he/she can add that too but later he will realize it will anyway become zero while differentiating.)

\Rightarrow Total time = $2x + 3k + kx + 6$ (k is equal to $24/x$)

\Rightarrow Total time = $2x + \left(\frac{3 \times 24}{x}\right) + \left(\frac{24 * x}{x}\right) + 6$

\Rightarrow Total time = $2x + \frac{72}{x} + 30$

to minimise this time, differentiation should give 0.

that gives, $2 - \frac{72}{x^2} = 0$

$\Rightarrow x = 6$.

including 3 bytes of header, packet size = 9 Bytes.

Option is D.

👍 103 votes

-- minal (13.1k points)

option D

packet size $P = p + h$ where, h is header size and

$p = \sqrt{\frac{hx}{k-1}}$ where, x is message size and k is no. of hops.

so $p = \sqrt{\frac{3 \times 24}{2}} = \sqrt{\frac{72}{2}} = \sqrt{36} = 6$

so Optimum packet size is $6 + 3 = 9$.

👍 31 votes

-- skrahul (655 points)



✓ In this question we have used the concept of pipelining.

In second and Third case, First packet will take $3 \times T_t$ time and all subsequent packets will be delivered in one T_t time.

$T_1 = 3 \times T_t = 3 \times \frac{(1000 + 100)}{B}$

$T_t = \frac{(\text{data} + \text{header})}{\text{Bandwidth}}$

data = 1000 Bytes; header = 100 Bytes

$$T_1 = \frac{3300}{B} \text{ seconds}$$

$$T_2 = 3 \times T_t' + 9 \times T_t' = 12 \times T_t'$$

$$T_t' = \frac{(\text{data} + \text{header})}{\text{Bandwidth}}$$

$$T_2 = \frac{12 \times (100 + 100)}{B} = \frac{2400}{B} \text{ seconds}$$

$$T_3 = 3 \times T_t'' + 19 \times T_t'' = 22 \times T_t''$$

$$T_t'' = \frac{(50 + 100)}{B}$$

$$T_3 = \frac{22 \times 150}{B} = \frac{3300}{B}$$

So $T_1 = T_3$ and $T_3 > T_2$;

option D

👍 92 votes

-- Vikrant Singh (11.2k points)

2.20.3 Network Switching: GATE CSE 2015 Set 3 | Question: 36 [top](#)

<https://gateoverflow.in/8495>



✓
No. of packets sent = $\frac{10000}{5000} = 2$.

Time for the first packet to reach switch = Transmission time + Propagation delay

$$= \left(\frac{5000}{10^7} \right) \times 10^6 \mu s + 20 \mu s$$

$$= 520 \mu s.$$

(Another $520 \mu s$ is required for the same packet to reach the destination from the switch and in between there is a forwarding delay of $35 \mu s$. So, first packet is received at destination at $2 \times 520 + 35 = 1075 \mu s$.)

After $520 \mu s$, the switch can start receiving the second packet and at $520 + 500 = 1020 \mu s$, second frame is completely received by the switch (we don't need to add propagation time here as packet 2 can just follow packet 1).

So, at $1055 \mu s$ from the start the switch starts sending the second packet and this will be received at destination after another $520 \mu s = 1575 \mu s$. Since we added transmission time, this ensures that the last bit of data is received at the sender.

EDIT:-

(Alternate solution)

We can think the same question in terms of last packet, argument here is: The moment last packet reaches to destination, all other packets are already reached.

Total time = Transmission time of all packets + Propagation time for first link
+ Switch Delay + Transmission time of last packet for Switch
+ propagation time for 2nd link.

$$= \left(\frac{10^4}{10^7} \text{sec} = 1 \text{ms} = 1000 \mu s \right) 1000 + 20 + 35 + 500 + 20 = 1575 \mu s.$$

👍 90 votes

-- Arjun Suresh (332k points)

2.20.4 Network Switching: GATE IT 2004 | Question: 22 [top](#)

<https://gateoverflow.in/3663>



✓
Answer is **B**.

In circuit switching, a fix bandwidth is allocated to each connection, e.g. 64 Kb/s allocated to each each phone call.

In circuit switching each connection has a dedicated circuit or channel all the way along the path and the circuit is not shared with anyone else.

Thus in circuit switching each call has its own private, guaranteed, isolated data rate from end to end. So we can say that every connection or flow is independent of others.

In the case of packet switching, all flows share the full channel capacity by statistical multiplexing.

So, the bandwidth allocated to each flow depends upon the number of concurrent flows & network traffic.

In packet switching if we know the type of link we are using, the bandwidth allocated, the packet size for any flow then we can calculate the Propagation Delay & Transmission Delays.

But, **Queueing Delay is a random variable that depends upon the number of packets arriving at the same time at any switch.**

It is the only random variable in our end to end delay expression. All other delays can be calculated precisely if we have enough information about the flows.

So, queueing adds unpredictable & variable delays in the packet switching.

There are delays like propagation delay etc. in circuit switching but they have a very small variance because of independence, privacy & bandwidth guarantees.

👍 49 votes

-- Anurag Pandey (10.5k points)

2.21

Pure Aloha (1) top ⚡

2.21.1 Pure Aloha: GATE CSE 2021 Set 2 | Question: 54 top ⚡

https://gateoverflow.in/357483



Consider a network using the pure ALOHA medium access control protocol, where each frame is of length 1,000 bits. The channel transmission rate is 1 Mbps ($= 10^6$ bits per second). The aggregate number of transmissions across all the nodes (including new frame transmissions and retransmitted frames due to collisions) is modelled as a Poisson process with a rate of 1,000 frames per second. Throughput is defined as the average number of frames successfully transmitted per second. The throughput of the network (rounded to the nearest integer) is _____

gate2021-cse-set2

computer-networks

mac-protocol

pure-aloha

numerical-answers

Answer ⚡

Answers: Pure Aloha

2.21.1 Pure Aloha: GATE CSE 2021 Set 2 | Question: 54 top ⚡

https://gateoverflow.in/357483



✓ Frame Transmission Time : $T_{fr} = L/B = 1000/10^6 = 1\text{ms}$

System generates 1000 frames in 1 second.

Now, G is defined as average no of frames generated by the system in one frame transmission time.

- 1 second \rightarrow 1000 frames
- \therefore 1ms \rightarrow 1 frame

Therefore, $G = 1$

Average number of successful transmissions, $S = G * e^{-2G} = 1 * e^{-2} = 0.13534$

Throughput is defined in question as the average number of frames successfully transmitted per second.

\therefore Throughput $= 0.13534 * 1000 = 135.34 \approx 135$.

👍 3 votes

-- sjoshis07 (169 points)

2.22

Routers Bridge Hubs Switches (1) top ⚡

2.22.1 Routers Bridge Hubs Switches: GATE CSE 2004 | Question: 16 top ⚡

https://gateoverflow.in/1013



Which of the following is NOT true with respect to a transparent bridge and a router?

- Both bridge and router selectively forward data packets
- A bridge uses IP addresses while a router uses MAC addresses
- A bridge builds up its routing table by inspecting incoming packets
- A router can connect between a LAN and a WAN

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routers-bridge-hubs-switches

normal

Answer

Answers: Routers Bridge Hubs Switches

2.22.1 Routers Bridge Hubs Switches: GATE CSE 2004 | Question: 16

<https://gateoverflow.in/1013>



- A. Both bridge and router selectively forward data packets ⇒ **True**.
Bridge can drop packets not meant for other side, so can router.
- B. A bridge uses IP addresses while a router uses MAC addresses ⇒ **False**.
A bridge operate at layer 2 (data link layer) so it uses MAC address, while router at layer 3 (network layer) so it using IP adresse
- C. A bridge builds up its routing table by inspecting incoming packets ⇒ **True**.
Self Learning Bridges
- D. A router can connect between a LAN and a WAN ⇒ **True**.
Router connecting home LAN To internet !

Correct Answer: B

42 votes

-- Akash Kanase (36k points)

2.23

Routing (9)

2.23.1 Routing: GATE CSE 2005 | Question: 26

<https://gateoverflow.in/1362>



In a network of LANs connected by bridges, packets are sent from one LAN to another through intermediate bridges. Since more than one path may exist between two LANs, packets may have to be routed through multiple bridges. Why is the *spanning tree algorithm* used for bridge-routing?

- A. For shortest path routing between LANs
- B. For avoiding loops in the routing paths
- C. For fault tolerance
- D. For minimizing collisions

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routing

normal

Answer

2.23.2 Routing: GATE CSE 2014 Set 2 | Question: 23

<https://gateoverflow.in/1981>



Which of the following is TRUE about the interior gateway routing protocols – Routing Information Protocol (*RIP*) and Open Shortest Path First (*OSPF*)

- A. RIP uses distance vector routing and OSPF uses link state routing
- B. OSPF uses distance vector routing and RIP uses link state routing
- C. Both RIP and OSPF use link state routing
- D. Both RIP and OSPF use distance vector routing

gate2014-cse-set2

computer-networks

routing

normal

Answer

2.23.3 Routing: GATE CSE 2014 Set 3 | Question: 26

<https://gateoverflow.in/2060>



An IP router implementing Classless Inter-domain Routing (CIDR) receives a packet with address 131.23.151.76. The router's routing table has the following entries:

Prefix	Outer Interface Identifier
131.16.0.0/12	3
131.28.0.0/14	5
131.19.0.0/16	2
131.22.0.0/15	1

The identifier of the output interface on which this packet will be forwarded is _____.

gate2014-cse-set3 computer-networks routing normal numerical-answers

Answer 

2.23.4 Routing: GATE CSE 2017 Set 2 | Question: 09 top

<https://gateoverflow.in/118338>



Consider the following statements about the routing protocols. Routing Information Protocol (RIP) and Open Shortest Path First (OSPF) in an IPv4 network.

- I. RIP uses distance vector routing
- II. RIP packets are sent using UDP
- III. OSPF packets are sent using TCP
- IV. OSPF operation is based on link-state routing

Which of the above statements are CORRECT?

- A. I and IV only
- B. I, II and III only
- C. I, II and IV only
- D. II, III and IV only

gate2017-cse-set2 computer-networks routing

Answer 

2.23.5 Routing: GATE CSE 2020 | Question: 15 top

<https://gateoverflow.in/333216>



Consider the following statements about the functionality of an IP based router.

- I. A router does not modify the IP packets during forwarding.
- II. It is not necessary for a router to implement any routing protocol.
- III. A router should reassemble IP fragments if the MTU of the outgoing link is larger than the size of the incoming IP packet.

Which of the above statements is/are TRUE?

- A. I and II only
- B. I only
- C. II and III only
- D. II only

gate2020-cse computer-networks routing

Answer 

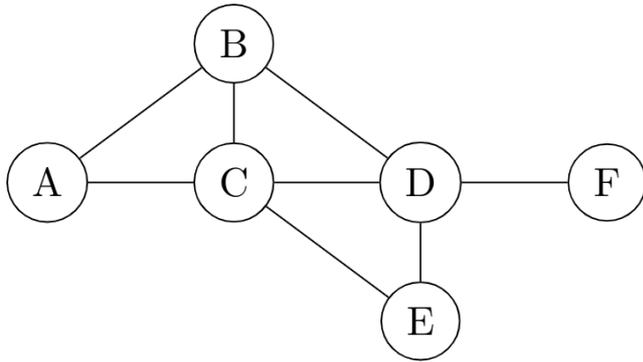
2.23.6 Routing: GATE IT 2005 | Question: 85a top

<https://gateoverflow.in/3858>



Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

- i. A node determines whether its neighbours in the graph are accessible. If so, it sets the tentative cost to each accessible neighbour as 1. Otherwise, the cost is set to ∞ .
- ii. From each accessible neighbour, it gets the costs to relay to other nodes via that neighbour (as the next hop).
- iii. Each node updates its routing table based on the information received in the previous two steps by choosing the minimum cost.



For the graph given above, possible routing tables for various nodes after they have stabilized, are shown in the following options. Identify the correct table.

A. Table for node A

A	-	-
B	B	1
C	C	1
D	B	3
E	C	3
F	C	4

B. Table for node C

A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	E	3

C. Table for node B

A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

D. Table for node D

A	B	3
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

gate2005-it computer-networks routing normal

Answer

2.23.7 Routing: GATE IT 2005 | Question: 85b [top](#)

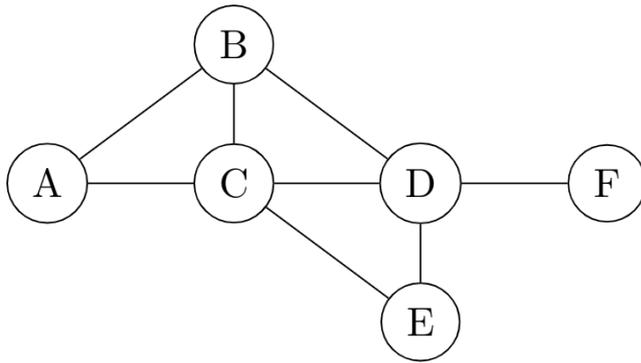
<https://gateoverflow.in/3859>



Consider a simple graph with unit edge costs. Each node in the graph represents a router. Each node maintains a routing table indicating the next hop router to be used to relay a packet to its destination and the cost of the path to the destination through that router. Initially, the routing table is empty. The routing table is synchronously updated as follows. In each updated interval, three tasks are performed.

- A node determines whether its neighbors in the graph are accessible. If so, it sets the tentative cost to each accessible neighbor as 1. Otherwise, the cost is set to ∞ .
- From each accessible neighbor, it gets the costs to relay to other nodes via that neighbor (as the next hop).
- Each node updates its routing table based on the information received in the previous two steps by choosing the minimum

cost.



Continuing from the earlier problem, suppose at some time t , when the costs have stabilized, node A goes down. The cost from node F to node A at time $(t + 100)$ is :

- A. > 100 but finite
- B. ∞
- C. 3
- D. > 3 and ≤ 100

gate2005-it computer-networks routing normal

Answer

2.23.8 Routing: GATE IT 2007 | Question: 63 top

<https://gateoverflow.in/3508>



A group of 15 routers is interconnected in a centralized complete binary tree with a router at each tree node. Router i communicates with router j by sending a message to the root of the tree. The root then sends the message back down to router j . The mean number of hops per message, assuming all possible router pairs are equally likely is

- A. 3
- B. 4.26
- C. 4.53
- D. 5.26

gate2007-it computer-networks routing binary-tree normal

Answer

2.23.9 Routing: GATE IT 2008 | Question: 67 top

<https://gateoverflow.in/3381>



Two popular routing algorithms are Distance Vector(DV) and Link State (LS) routing. Which of the following are true?

- (S1): Count to infinity is a problem only with DV and not LS routing
- (S2): In LS, the shortest path algorithm is run only at one node
- (S3): In DV, the shortest path algorithm is run only at one node
- (S4): DV requires lesser number of network messages than LS

- A. S1, S2 and S4 only
- B. S1, S3 and S4 only
- C. S2 and S3 only
- D. S1 and S4 only

gate2008-it computer-networks routing normal

Answer

Answers: Routing

2.23.1 Routing: GATE CSE 2005 | Question: 26 top

<https://gateoverflow.in/1362>



✓ The answer is (B).

Since, in a spanning tree, there is a unique path from a source to the destination, which avoids loops, since it is a tree, and contains all the nodes, since it is a spanning tree.

👍 28 votes

-- saurabhk (1k points)

2.23.2 Routing: GATE CSE 2014 Set 2 | Question: 23 top

<https://gateoverflow.in/1981>



- ✓ Both Routing Information Protocol (RIP) and Open Shortest Path First (OSPF) are Interior Gateway Protocol, i.e., they both are used within an autonomous system. RIP is an old protocol (not used anymore) based on distance vector routing. OSPF is based Link State Routing.

Correct Answer: A

👍 17 votes

-- Divya Bharti (8.8k points)

2.23.3 Routing: GATE CSE 2014 Set 3 | Question: 26 top

<https://gateoverflow.in/2060>



- ✓ Answer is Interface 1.

Given address 133.23.151.76 coming to the first field of given routing table
⇒ 131.16.0.0/12

131.0001 0111.151.76

131.0001 0000.0.0(: given mask bits = 12)

⇒ 131.16.0.0 Matched

Coming to the 2nd field of the given Routing table

⇒ 131.28.0.0/14

131.0001 0111.151.76

131.0001 0100.0.0(: given mask bits = 14)

⇒ 131.20.0.0 Not matched.

Coming to the 3rd field of the given Routing table
Error! Not a valid link. 131.19.0.0/16

131.0001 0111.151.76

131.0001 0111.0.0(: given mask bits = 16)

⇒ 131.23.0.0 Not matched

Coming to the 4th field of given Routing table

⇒ 131.22.0.0/15

131.0001 0111.151.76

131.0001 0110.0.0(: given mask bits = 15)

⇒ 131.22.0.0 Matched.

We are getting 1st and 4th entries are matched so among them we have to picked up longest mask bit, so output interface identifier is 1.

👍 45 votes

-- saurabhk (1k points)

2.23.4 Routing: GATE CSE 2017 Set 2 | Question: 09 top

<https://gateoverflow.in/118338>



- ✓ Statement 1 is **CORRECT** Bcoz RIP is one of the Oldest DVR(Distance Vector Routing) Protocols which employ the

hop count as a routing metric.

Statement 2 is **CORRECT** Bcoz RIP uses the UDP as its transport protocol with port no 520.

Statement 3 is **INCORRECT** Bcoz OSPF doesnot use a transport protocol such as UDP or TCP but encapsulates its data directly into IP Packets.

Statement 4 is **CORRECT** Bcoz OSPF is a routing protocol which uses Link State Routing(LSR) and works within a single Autonomous System.

PS:

OSPF needs to perform reliable multicasting because it needs to talk to multiple possible neighbors on the same network segment. Now, TCP does not support multicast and UDP is not reliable Therefore, OSPF implements its own transport mechanism that allows both for reliability (acknowledgements and retransmissions of lost segments) and multicasting, bypassing both TCP and UDP.

Hence, Option C is CORRECT.

👍 58 votes

-- G VENKATESWARLU (461 points)

2.23.5 Routing: GATE CSE 2020 | Question: 15 [top](#)

<https://gateoverflow.in/333216>



✓ Answer: D. II Only

Explanation

Taking the given statements one by one:

I. **(FALSE)** Router needs to fragment the incoming IP packets if the connecting line has smaller MTU (Maximum Transmission Unit) than size of incoming packets.

II. **(TRUE)** That's the case of static routing where forward paths are pre-loaded/downloaded to routers.

III. **(FALSE)** This is not possible in case of cut-through-switching where IP packet is forwarded as it arrives.

👍 7 votes

-- dhruvhacks (609 points)

2.23.6 Routing: GATE IT 2005 | Question: 85a [top](#)

<https://gateoverflow.in/3858>



✓

Table for Node A

A	-	-
B	B	1
C	C	1
D	B	2
E	C	2
F	C	3

Table for Node D

A	B	2
B	B	1
C	C	1
D	-	-
E	E	1
F	F	1

Table for Node C

A	A	1
B	B	1
C	-	-
D	D	1
E	E	1
F	D	2

Table for Node B

A	A	1
B	-	-
C	C	1
D	D	1
E	C	2
F	D	2

Correct tables are as above.

Only **option C** is matching.

👍 21 votes

-- Prashant Singh (47.2k points)

2.23.7 Routing: GATE IT 2005 | Question: 85b [top](#)

<https://gateoverflow.in/3859>



✓ We consider **A B D F** at t they are:

The distance between A and the nodes **B,D,F** respectively are:

- $t : 123$
- $t + 1 : 323$
- $t + 2 : 343$
- $t + 3 : 545$
- $t + 4 : 565$
- $t + 5 : 767$
- $t + 6 : 787$
- $t + 7 : 989$
- $t + 8 : 9109$

and this continues...

So, in every two steps, they get incremented by 2

So at $t + 99$, F is 101

At $t + 100$, F is 101

So, count to infinity problem.

So, option A.

43 votes

classroom.gateoverflow

-- Shreya Roy (3.8k points)

2.23.8 Routing: GATE IT 2007 | Question: 63 top

https://gateoverflow.in/3508



✓ OPTION is C.

Here, we have to count average hops per message.

Steps:

- 1) Message goes up from sender to root
- 2) Message comes down from root to destination

1) Average hops message goes to root -
$$\frac{(3 \times 8) + (2 \times 4) + (1 \times 2) + (0 \times 1)}{15} = 2.267$$

Here 3×8 represents 3 hops & 8 routers for Bottommost level & So on..

2) Similarly average hops when message comes down -
$$\frac{(3 \times 8) + (2 \times 4) + (1 \times 2) + (0 \times 1)}{15}$$
 {Same as above}

So, Total Hops = $2 \times 2.267 = 4.53$ (Answer)

171 votes

-- Himanshu Agarwal (12.4k points)

2.23.9 Routing: GATE IT 2008 | Question: 67 top

https://gateoverflow.in/3381



✓ S1 is true, S2 and S3 are false and S4 is true.

Link State: <https://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-112.pdf>

Distance Vector: <http://cseweb.ucsd.edu/classes/fa10/cse123/lectures/123-fa10-113.pdf>

Correct Answer: D

References



26 votes

-- Arjun Suresh (332k points)

2.24

Serial Communication (1) top

2.24.1 Serial Communication: GATE CSE 1992 | Question: 02,v top

https://gateoverflow.in/560



Start and stop bits do not contain any 'information' but are used in serial communication

- a. Error detection
- b. Error correction
- c. Synchronization
- d. Slowing down the communications

gate1992

easy

computer-networks

serial-communication

multiple-selects

Answer

2.24.1 Serial Communication: GATE CSE 1992 | Question: 02.v [top](#)<https://gateoverflow.in/560>

✓ Answer is C.

The start and stop bits are used to synchronize the serial receivers.

Reference: <http://esd.cs.ucr.edu/labs/serial/serial.html>

References



👍 9 votes

-- Rajarshi Sarkar (27.9k points)

2.25

Sliding Window (15) [top](#)2.25.1 Sliding Window: GATE CSE 2003 | Question: 84 [top](#)<https://gateoverflow.in/967>

Host A is sending data to host B over a full duplex link. A and B are using the sliding window protocol for flow control. The send and receive window sizes are 5 packets each. Data packets (sent only from A to B) are all 1000 bytes long and the transmission time for such a packet is $50 \mu s$. Acknowledgment packets (sent only from B to A) are very small and require negligible transmission time. The propagation delay over the link is $200 \mu s$. What is the maximum achievable throughput in this communication?

- A. 7.69×10^6 Bps
- B. 11.11×10^6 Bps
- C. 12.33×10^6 Bps
- D. 15.00×10^6 Bps

gate2003-cse computer-networks sliding-window normal

Answer

2.25.2 Sliding Window: GATE CSE 2005 | Question: 25 [top](#)<https://gateoverflow.in/1361>

The maximum window size for data transmission using the selective reject protocol with n -bit frame sequence numbers is:

- A. 2^n
- B. 2^{n-1}
- C. $2^n - 1$
- D. 2^{n-2}

gate2005-cse computer-networks sliding-window easy

Answer

2.25.3 Sliding Window: GATE CSE 2006 | Question: 44 [top](#)<https://gateoverflow.in/1820>

Station A uses 32 byte packets to transmit messages to Station B using a sliding window protocol. The round trip delay between A and B is 80 milliseconds and the bottleneck bandwidth on the path between A and B is 128 kbps. What is the optimal window size that A should use?

- A. 20
- B. 40
- C. 160
- D. 320

gate2006-cse computer-networks sliding-window normal

Answer 

2.25.4 Sliding Window: GATE CSE 2006 | Question: 46 [top](#) 

<https://gateoverflow.in/1922>



Station A needs to send a message consisting of 9 packets to Station B using a sliding window (window size 3) and go-back- n error control strategy. All packets are ready and immediately available for transmission. If every 5th packet that A transmits gets lost (but no acks from B ever get lost), then what is the number of packets that A will transmit for sending the message to B ?

- A. 12
- B. 14
- C. 16
- D. 18

gate2006-cse computer-networks sliding-window normal

Answer 

2.25.5 Sliding Window: GATE CSE 2007 | Question: 69 [top](#) 

<https://gateoverflow.in/1267>



The distance between two stations M and N is L kilometers. All frames are K bits long. The propagation delay per kilometer is t seconds. Let R bits/second be the channel capacity. Assuming that the processing delay is negligible, the minimum number of bits for the sequence number field in a frame for maximum utilization, when the sliding window protocol is used, is:

- A. $\lceil \log_2 \frac{2LtR+2K}{K} \rceil$
- B. $\lceil \log_2 \frac{2LtR}{K} \rceil$
- C. $\lceil \log_2 \frac{2LtR+K}{K} \rceil$
- D. $\lceil \log_2 \frac{2LtR+2K}{2K} \rceil$

gate2007-cse computer-networks sliding-window normal

Answer 

2.25.6 Sliding Window: GATE CSE 2009 | Question: 57, ISRO2016-75 [top](#) 

<https://gateoverflow.in/1340>



Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25 ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

What is the minimum number of bits (I) that will be required to represent the sequence numbers distinctly? Assume that no time gap needs to be given between transmission of two frames.

- A. $I = 2$
- B. $I = 3$
- C. $I = 4$
- D. $I = 5$

gate2009-cse computer-networks sliding-window normal isro2016

Answer 

2.25.7 Sliding Window: GATE CSE 2009 | Question: 58 [top](#) 

<https://gateoverflow.in/43470>



Frames of 1000 bits are sent over a 10^6 bps duplex link between two hosts. The propagation time is 25ms. Frames are to be transmitted into this link to maximally pack them in transit (within the link).

Let I be the minimum number of bits (I) that will be required to represent the sequence numbers distinctly assuming that no time gap needs to be given between transmission of two frames.

Suppose that the sliding window protocol is used with the sender window size of 2^I , where I is the numbers of bits as mentioned earlier and acknowledgements are always piggy backed. After sending 2^I frames, what is the minimum time the sender will have to wait before starting transmission of the next frame? (Identify the closest choice ignoring the frame processing time)

- A. 16ms
- B. 18ms
- C. 20ms
- D. 22ms

gate2009-cse computer-networks sliding-window normal

Answer 2.25.8 Sliding Window: GATE CSE 2014 Set 1 | Question: 28 top<https://gateoverflow.in/1795>

Consider a selective repeat sliding window protocol that uses a frame size of 1 KB to send data on a 1.5 Mbps link with a one-way latency of 50 msec. To achieve a link utilization of 60%, the minimum number of bits required to represent the sequence number field is _____.

gate2014-cse-set1 computer-networks sliding-window numerical-answers normal

Answer 2.25.9 Sliding Window: GATE CSE 2015 Set 3 | Question: 28 top<https://gateoverflow.in/8481>

Consider a network connecting two systems located 8000 Km apart. The bandwidth of the network is 500×10^6 bits per second. The propagation speed of the media is 4×10^6 meters per second. It needs to design a Go-Back- N sliding window protocol for this network. The average packet size is 10^7 bits. The network is to be used to its full capacity. Assume that processing delays at nodes are negligible. Then, the minimum size in bits of the sequence number field has to be _____.

gate2015-cse-set3 computer-networks sliding-window normal numerical-answers

Answer 2.25.10 Sliding Window: GATE CSE 2016 Set 2 | Question: 55 top<https://gateoverflow.in/39577>

Consider a 128×10^3 bits/second satellite communication link with one way propagation delay of 150 milliseconds. Selective retransmission (repeat) protocol is used on this link to send data with a frame size of 1 kilobyte. Neglect the transmission time of acknowledgement. The minimum number of bits required for the sequence number field to achieve 100% utilization is _____.

gate2016-cse-set2 computer-networks sliding-window normal numerical-answers

Answer 2.25.11 Sliding Window: GATE IT 2004 | Question: 81 top<https://gateoverflow.in/3725>

In a sliding window ARQ scheme, the transmitter's window size is N and the receiver's window size is M . The minimum number of distinct sequence numbers required to ensure correct operation of the ARQ scheme is

- $\min(M, N)$
- $\max(M, N)$
- $M + N$
- MN

gate2004-it computer-networks sliding-window normal

Answer 2.25.12 Sliding Window: GATE IT 2004 | Question: 83 top<https://gateoverflow.in/3727>

A 20 Kbps satellite link has a propagation delay of 400 ms. The transmitter employs the "go back n ARQ " scheme with n set to 10. Assuming that each frame is 100 byte long, what is the maximum data rate possible?

- 5 Kbps
- 10 Kbps
- 15 Kbps
- 20 Kbps

gate2004-it computer-networks sliding-window normal

Answer 



Suppose that the maximum transmit window size for a TCP connection is 12000 bytes. Each packet consists of 2000 bytes. At some point in time, the connection is in slow-start phase with a current transmit window of 4000 bytes. Subsequently, the transmitter receives two acknowledgments. Assume that no packets are lost and there are no time-outs. What is the maximum possible value of the current transmit window?

- A. 4000 bytes
- B. 8000 bytes
- C. 10000 bytes
- D. 12000 bytes

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gate2004-it computer-networks sliding-window normal

Answer



Suppose that it takes 1 unit of time to transmit a packet (of fixed size) on a communication link. The link layer uses a window flow control protocol with a window size of N packets. Each packet causes an ack or a nak to be generated by the receiver, and ack/nak transmission times are negligible. Further, the round trip time on the link is equal to N units. Consider time $i > N$. If only acks have been received till time i (no naks), then the goodput evaluated at the transmitter at time i (in packets per unit time) is

- A. $1 - \frac{N}{i}$
- B. $\frac{i}{(N+i)}$
- C. 1
- D. $1 - e^{-\left(\frac{i}{N}\right)}$

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gate2006-it computer-networks sliding-window normal

Answer



A 1 Mbps satellite link connects two ground stations. The altitude of the satellite is 36,504 km and speed of the signal is 3×10^8 m/s. What should be the packet size for a channel utilization of 25% for a satellite link using go-back-127 sliding window protocol? Assume that the acknowledgment packets are negligible in size and that there are no errors during communication.

- A. 120 bytes
- B. 60 bytes
- C. 240 bytes
- D. 90 bytes

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gate2008-it computer-networks sliding-window normal

Answer

Answers: Sliding Window



✓ We need the maximum throughput, and for that we need to send as much data as possible to fully utilize the bandwidth.

so, maximum packets that can be sent = $1 + 2a = 9$ (after calculation) for 100% efficiency.

But we have a window size of 5 only, so we can send only 5 packets at max.

$$\text{Efficiency} = \frac{5}{9}$$

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Now, $\frac{A}{Q}$, Bandwidth of the channel (BW) = $\frac{L}{T_t}$

$$= \frac{1000}{(50 \times 10^{-6})}$$

$$= 20 \times 10^6 \text{ bytes/sec.}$$

So, max. throughput achievable = Efficiency \times BW

$$= \frac{5}{9} \times 20 \times 10^6 = 11.11 \times 10^6 \text{ bytes/sec.}$$

Correct Answer: B

👍 130 votes

-- Ravi Ranjan (3k points)

I think options are given in bytes per sec instead of bits per sec.

Transmission time = 50 micro sec
 Propagation time = 200 micro sec

$$RTT = 50 + 2 \times 200 = 450 \text{ microsec}$$

(Receiver can send an ACK as soon as the first packet is received)

Total number of bits transmitted before first ACK is received,
 = $1000 \times 5 \times 8 \text{ bits} = 40000 \text{ bits}$

After first ACK is received, the same cycle of action repeats.

$$\text{So, Throughput} = \left(\frac{40000}{450} \right) \times 10^6 \text{ bits}$$

$$= 88.88 \times 10^6 \text{ bits per sec}$$

$$= 11.11 \times 10^6 \text{ bytes per sec}$$

👍 47 votes

-- Parul Agarwal (661 points)

2.25.2 Sliding Window: GATE CSE 2005 | Question: 25 top

<https://gateoverflow.in/1361>



✓ Answer is b)

In selective reject protocol, the maximum window size must be half

$$\text{the Sequence number space} = \frac{2^n}{2} = 2^{n-1}.$$

For Go-back n, the maximum window size can be $2^n - 1$.

<http://webmuseum.mi.fh-offenburg.de/index.php?view=exh&src=73> or [archive](#)

References



👍 48 votes

-- Aditi Dan (4k points)

2.25.3 Sliding Window: GATE CSE 2006 | Question: 44 top

<https://gateoverflow.in/1820>



✓ Round trip delay = 80 ms.

Quoting from Wikipedia

the round-trip delay time (RTD) or round-trip time (RTT) is the length of time it takes for a signal to be sent plus the length of time it takes for an acknowledgment of that signal to be received.

Now, in many books including standard ones, they have used RTT to mean just the 2-way propagation delay by considering the signal/packet as of the smallest possible quantity so that its transmission time is negligible. The given question is following the first definition as given by Wikipedia which is clear from the choices.

During this time the first ACK arrives and so sender can continue sending frames.

So, for maximum utilization sender should have used the full bandwidth during this time.

i.e., it should have sent $128 \text{ kbps} \times 80 \text{ ms}$ amount of data and a packet being of size 32 bytes, we get

$$\text{no. of packets} = \frac{128 \times 80}{32 \times 8} = 40.$$

Correct Answer: B

👍 55 votes

-- Arjun Suresh (332k points)

2.25.4 Sliding Window: GATE CSE 2006 | Question: 46 top

<https://gateoverflow.in/1822>



✓
 1 2 3 4 5 6 7 5 6 7 8 9 7 8 9 9

⏟
⏟
⏟

Total 16 packet Transmission

Correct Answer: C

👍 57 votes

-- riki_nitdgp_17 (143 points)

2.25.5 Sliding Window: GATE CSE 2007 | Question: 69 top

<https://gateoverflow.in/1367>



✓ **Answer: C**

We can send $\frac{\text{RTT}}{\text{Transmission Time}}$ number of packets

for maximum utilization of the channel, as in this time, we get the first ACK back and till that time, we can continue sending packets.

So, $\frac{\text{Transmission Time} + 2 \times \text{Propagation Time}}{\text{Transmission Time}}$ number of packets should be sent.

Therefore, bits required for the sequence number field:

$$\left\lceil \log_2 \left(\frac{K + 2LtR}{R} \right) \right\rceil = \left\lceil \log_2 \left(\frac{K + 2LtR}{K} \right) \right\rceil$$

Edit : here it is asked for general sliding window protocol not GBN nor SR .

In general sliding window protocol:

Sequence number bit = $\log(\text{sender window size})$

👍 65 votes

-- Rajarshi Sarkar (27.9k points)

2.25.6 Sliding Window: GATE CSE 2009 | Question: 57, ISRO2016-75 top

<https://gateoverflow.in/1340>



✓ Bandwidth won't be halved in full duplex.

<http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive>

Propagation time is given as 25 ms.

Bandwidth = 10^6 bps .

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits.

Now, since the propagation time is 25 ms, to fully pack the link we need to send at least $1000 \times 25 \times 10^{-3} = 25$ frames.

So, we need $\lceil \log_2 25 \rceil = 5$ bits.

Correct Answer: *D*

References



👍 114 votes

-- Arjun Suresh (332k points)

2.25.7 Sliding Window: GATE CSE 2009 | Question: 58 top

<https://gateoverflow.in/43470>



- ✓ Bandwidth won't be halved in full duplex. <http://superuser.com/questions/335979/does-1-gbit-s-port-in-full-duplex-mean-1-gbit-s-send-and-1-gbit-s-receive>

Propagation time is given as 25 ms.

Bandwidth = 10^6 bps.

So, to fully utilize the channel, we must send 10^6 bits into the channel in a second, which will be 1000 frames per second as each frame is 1000 bits. Now, since the propagation time is 25 ms, to fully pack the link we need to send at least $1000 \times 25 \times 10^{-3} = 25$ frames. So, we need $\lceil \log_2 25 \rceil = 5$ bits.

$I = 5$, so $2^I = 32$ frames are sent.

Now, we need to get RTT (which is the time between which a frame is sent and its ACK is received), to determine the waiting time.

Transmission time (for a frame of size 1000 bits) = $1000/10^6 = 1$ ms.

So, transmission time for 32 frames = 32 ms.

RTT = Propagation time for frame + Transmission time for frame + Propagation time for ACK + Transmission time for ACK

= 25 ms + 1 ms + 25 ms + 1 ms (ACK is piggy backed and assuming frame size for piggy backing is also 1000 bits)

= 52 ms

So, waiting time = $52 - 32 = 20$ ms. (For the 32 ms, the sender was transmitting and not waiting)

Correct Answer: *C*

References



👍 105 votes

-- Arjun Suresh (332k points)

2.25.8 Sliding Window: GATE CSE 2014 Set 1 | Question: 28 top

<https://gateoverflow.in/1795>



- ✓
$$\eta_{SR} = \frac{N}{1 + 2a}$$

$B = 1.5$ Mbps

$T_p = 50$ ms

$L = 1$ KB = 1024×8 bits

$\eta_{SR} = 60\%$

$$\therefore 0.6 = \frac{N}{1 + 2a}$$

$$\implies N = 0.6(1 + 2a)$$

$$a = \frac{T_p}{T_t} = \frac{T_p}{L} \cdot B = \frac{50 \times 10^{-3} \times 1.5 \times 10^6}{1024 \times 8} = 9.155$$

$$\therefore N = 0.6 \times (1 + 2 \times 9.155) = 11.58$$

$$w_s + w_R \leq \text{ASN}$$

$$\implies 2N \leq \text{ASN}$$

$$\implies 2 \times 11.58 \leq \text{ASN}$$

$$\implies \text{ASN} \geq \lceil 23.172 \rceil$$

$$\implies \text{ASN} \geq 24$$

\therefore Minimum number of bits required for sequence number field = $\lceil \log_2 24 \rceil = 5$.

👍 126 votes

-- Vikrant Singh (11.2k points)

A frame is 1 KB and takes $\frac{8 \times 10^3}{1.5 \times 10^6} \text{ s} = 5.33 \text{ ms}$

to reach the destination. (8 is used to convert byte to bits)

Adding the propagation delay of 50 ms, the total time will be $50 + 5.33 = 55.33 \text{ ms}$

Now, we need the ACK to reach back also, so the time between a packet is sent and an ACK is received = $55.33 + 50$ (transmission time of ACK neglected) = 105.33 ms

The channel bandwidth is 1.5 Mbps, so in 1 ms, 1.5K bits can be transferred and so in 105.33 ms, 157.995K bits can be transferred.

To, ensure 60% utilization, amount of bits to be transferred in

$$1 \text{ ms} = 157.995 \times 0.6 = 94.797 \text{ Kb} = \frac{94.797}{(8 \times 1000)} \text{ frames}$$

$$= 11.849 \text{ frames} \approx 12 \text{ frames.}$$

(we bounded up to ensure at least 60% utilization)

So, we need a minimum window size of 12.

Now, in selective repeat protocol, the window size must be less than half the sequence number space.

<https://stackoverflow.com/questions/3999065/why-is-window-size-less-than-or-equal-to-half-the-sequence-number-in-sr-protocol>

So, this means sequence number space must be larger than $2 \times 12 = 24$.

To have a sequence number space of 24, sequence bits must be at least $\log_2 24 = 5$

References



👍 44 votes

-- Arjun Suresh (332k points)



✓ Answer = 8 bits.

In order to achieve full utilization, sender has to keep on sending frames till the acknowledgement arrives for the first frame.

Time taken for acknowledgement to arrive is 2 times propagation delay + transmission time for a frame.

$$\text{One way propagation delay} = \frac{8000 \times 10^3}{(4 \times 10^6)} = 2s$$

$$\text{Time taken to transmit one frame} = \frac{10^7}{(500 \times 10^6)} = 0.02s$$

$$\text{So, RTT} = 2 \times 2 + 0.02 = 4.02s$$

$$\text{No. of frames that can be transmitted in 4.02 secs} = \frac{4.02}{0.02} = 201$$

Being Go-Back-N protocol this means $W_S = 201$ and $W_R = 1$. So, total number of sequence numbers required = $201 + 1 = 202$.

Hence, minimum number of bits required for sequence numbers till 202 is $\lceil \log_2 202 \rceil = 8$.

👍 47 votes

-- overtomanu (945 points)

2.25.10 Sliding Window: GATE CSE 2016 Set 2 | Question: 55 [top](#)

<https://gateoverflow.in/39577>



✓ **Answer is 4 bits.**

As we want 100% efficiency(μ), $w_s = 1 + 2a$

$$a = \frac{\text{propagation time}}{\text{transmission time}}$$
$$= \frac{150}{1024 \times \frac{8}{128}} = \frac{150}{64} = 2.34,$$

$$\Rightarrow w_s = 1 + 2a = 5.6875 \approx 6$$

Available seq numbers $\geq w_s + w_r$

In Selective Repeat,

$$w_s = w_r \text{ (let it be } n\text{)}$$

$$2 \times n = 2 \times 6 = 12$$

avail seq numbers ≥ 12

So, minimum seq numbers are 12.

Number of bits for that is $\lceil \log_2 12 \rceil = 4$.

👍 78 votes

-- Sreyas S (1.6k points)

2.25.11 Sliding Window: GATE IT 2004 | Question: 81 [top](#)

<https://gateoverflow.in/3725>



✓ **C) M+N**

Because $W_s + W_r \leq \text{Sequence numbers}$ (as the maximum number of unacknowledged packets at sender will be W_s and at the receiver it will be W_r , similar to the sequence numbering in Selective Repeat)

where W_s is size of sender window and W_r is receiver window size.

👍 39 votes

-- Parul Agarwal (661 points)

✓ **Answer: B**

$$\text{Transmission Time} = \frac{100 \times 8\text{bits}}{20 \text{ Kbps}} = 40 \text{ ms}$$

$$\text{Propagation Time} = 400 \text{ ms}$$

$$\text{Efficiency} = \frac{\text{Window Size} \times \text{Transmission Time}}{(\text{Transmission Time} + 2 \times \text{Propagation Time})}$$

$$= \frac{10 \times 40}{(40 + 2 \times 400)} = 0.476$$

$$\text{Maximum Data Rate} = 0.476 \times 20 \text{ Kbps} = 9.52 \text{ Kbps}$$

which is close to option B.

👍 51 votes

-- Rajarshi Sarkar (27.9k points)



✓ In slow-start phase, for each ACK, the sender increases the current transmit window by Maximum Segment Size (MSS). In the question it is given a packet consists of 2000 bytes and that can be taken as MSS. So, after two ACKs, current transmit window
 = 4000 + 2000 + 2000
 = 8000

<http://www.ece.virginia.edu/~mv/edu/ee136/Lectures/congestion-control/tcp-congestion-control.pdf> or [archive](#)

Correct Answer: B

References



👍 65 votes

-- Arjun Suresh (332k points)



✓ In [computer networks](#), **goodput** is the application level [throughput](#), i.e. the number of useful information [bits](#) delivered by the network to a certain destination per unit of time. (From wikipedia).

So, successful delivery of packet can be assured if ACK has been received for it.

So till time ' i ' we would have transmitted ' i ' packets but only $(i - N)$ can be acknowledged as minimum time for a packet to get Acknowledged is N (since RTT is N which is equal to the window size, there is no waiting time for the sender).

$$\text{So, successfully delivered packets} = (i - N)$$

$$\text{Time for transmission} = i$$

$$\text{Goodput} = \frac{\text{Successfully delivered data}}{\text{Time}}$$

$$= \frac{(i - N)}{i}$$

$$= 1 - \frac{N}{i}$$

Therefore (A)

References



2.25.15 Sliding Window: GATE IT 2008 | Question: 64 top

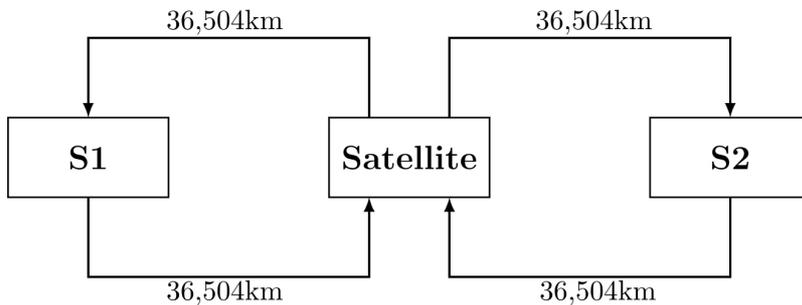
https://gateoverflow.in/3375



Distance from Station A to Satellite = 36504×10^3 m

Time to reach satellite = $\frac{36504000}{300000000} = 0.12168s$

RTT (for a bit) = $4 \times$ Time to reach satellite ($S1 \rightarrow$ Satellite, Satellite \rightarrow S2, S2 \rightarrow Satellite, Satellite \rightarrow S1)



Efficiency is the ratio of the amount of data sent to the maximum amount of data that could be sent. Let X be the packet size.

In Go-Back-N, within RTT we can sent n packets. So, useful data is n * X, where X is the packet size. Now, before we can sent another packet ACK must reach back. Time for this is transmission time for a packet (other packets are pipelined and we care only for first ACK), and RTT for a bit, (propagation times for the packet + propagation time for ACK + transmission time for ACK - neglected as per question)

Efficiency = $\frac{\text{Transmitted Data Size}}{\text{Packet Size} + \text{RTT}_{bit} \times \text{Bandwidth}}$

0.25 = $\frac{127 \times X}{X + 4 \times 0.12168 \times B}$

0.25X + 0.25 * 4 * 0.12168 * B = 127X

0.25X + 0.12168 * 10^6 = 127X

121680 = 126.75X

X = 9.6 * 10^-4 * 10^6 = 960

∴ Packet Size = 960 bits = 120 Bytes

So, option (A) is the answer.

2.26

Sockets (4) top

2.26.1 Sockets: GATE CSE 2008 | Question: 17 top

https://gateoverflow.in/415



Which of the following system calls results in the sending of SYN packets?

- A. socket
B. bind

- C. listen
- D. connect

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gate2008-cse normal computer-networks sockets

Answer 

2.26.2 Sockets: GATE CSE 2008 | Question: 59 [top](#)

<https://gateoverflow.in/482>



A client process P needs to make a TCP connection to a server process S. Consider the following situation: the server process S executes a `socket()`, a `bind()` and a `listen()` system call in that order, following which it is preempted. Subsequently, the client process P executes a `socket()` system call followed by `connect()` system call to connect to the server process S. The server process has not executed any `accept()` system call. Which one of the following events could take place?

- A. `connect()` system call returns successfully
- B. `connect()` system call blocks
- C. `connect()` system call returns an error
- D. `connect()` system call results in a core dump

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Answer 

2.26.3 Sockets: GATE CSE 2014 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/1982>



Which of the following socket API functions converts an unconnected active TCP socket into a passive socket?

- A. `connect`
- B. `bind`
- C. `listen`
- D. `accept`

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gate2014-cse-set2 computer-networks sockets easy

Answer 

2.26.4 Sockets: GATE CSE 2015 Set 2 | Question: 20 [top](#)

<https://gateoverflow.in/8108>



Identify the correct order in which a server process must invoke the function calls `accept`, `bind`, `listen`, and `recv` according to UNIX socket API.

- A. `listen`, `accept`, `bind`, `recv`
- B. `bind`, `listen`, `accept`, `recv`
- C. `bind`, `accept`, `listen`, `recv`
- D. `accept`, `listen`, `bind`, `recv`

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gate2015-cse-set2 computer-networks sockets easy

Answer 

Answers: Sockets

2.26.1 Sockets: GATE CSE 2008 | Question: 17 [top](#)

<https://gateoverflow.in/415>



✓ Answer is (D).

- **`socket()`** creates a new socket of a certain socket type, identified by an integer number, and allocates system resources to it.
- **`bind()`** is typically used on the server side, and associates a socket with a socket address structure, i.e. a specified local port number and IP address.
- **`listen()`** is used on the server side, and causes a bound TCP socket to enter listening state.
- **`connect()`** is used on the client side, and assigns a free local port number to a socket. In case of a TCP socket, it causes an attempt to establish a new TCP connection.

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When `connect()` is called by client, following three way handshake happens to establish the connection in TCP.

1. The client requests a connection by sending a SYN (synchronize) message to the server.
2. The server acknowledges this request by sending SYN-ACK back to the client.
3. The client responds with an ACK, and the connection is established.

👍 58 votes

-- minal (13.1k points)

2.26.2 Sockets: GATE CSE 2008 | Question: 59 [top](#)

<https://gateoverflow.in/482>



- ✓ First thing to note: All the sockets are by default in BLOCKING mode. What do we mean by blocking ??

Blocking mode means that when we make a system call, it blocks the caller for the time "when call() is made till the job is done OR an error returns ". We can set each socket to Non-blocking explicitly. Setting to Non-Blocking means we are telling the kernel that "If the system call cant be completed without putting process to sleep then DON'T put the process to sleep . Instead return with an ERROR immediately and continue the process" which can be checked for the completion by the caller in between the execution of other tasks.

Now coming to this question:

Suppose `connect()` is in default blocking mode then calling `connect()` sends SYN packet to the server. Since server has not executed any `accept()` call it can not acknowledge the SYN packet. `Connect()` in blocking mode keep sending SYN packets at fixed intervals(first after 6 sec, second after 24 sec typically until 75 sec latest). This is done until an error ETIMEDOUT is returned by the TCP.(in this case,else there are several other type of errors returned in case No port exists for that connection or server id not listening etc.)

Here, option (B) saying that `connect()` blocks is not entirely wrong but since we know that `accept()` call is not made by server, `connect()` WILL NOT WAIT FOREVER and SO IT CAN NOT BLOCK. It will **ultimately return** with an ERROR message.

So, option (C) is CORRECT.

Core dump thing I don't know about!

But once `connect()` returns error that socket can not be reused and must be CLOSED.

And a non-blocking `connect()` is never blocked and immediately returns with an error if connection is not successful although IT CONTINUES WITH TRYING TO CONNECT .Error here just means that it returns a message saying "I could not connect immediately BUT i am trying AND you can check it in between.

Hope it clears a bit.

👍 98 votes

-- Sandeep_Uniyal (6.5k points)

2.26.3 Sockets: GATE CSE 2014 Set 2 | Question: 24 [top](#)

<https://gateoverflow.in/1982>



- ✓ (C) is ans listen converts unconnected socket into passive connect i.e it is waiting for request from client

👍 35 votes

-- Pooja Palod (24.1k points)

2.26.4 Sockets: GATE CSE 2015 Set 2 | Question: 20 [top](#)

<https://gateoverflow.in/8108>



- ✓ Answer: (B)

Bind: Binds the socket to an address

Listen: Waits for connections to the socket

Accept: Accepts a connection to the socket

Recv: Receives data from connection

From Man page of accept:

It extracts the first connection request on the queue of pending connections for the listening socket, creates a new connected socket, and returns a new file descriptor referring to that socket. The newly created socket is not in the listening state. The original socket is unaffected by this call

👍 35 votes

-- Rajarshi Sarkar (27.9k points)

2.27

Stop And Wait (5) [top](#)



Suppose that the stop-and-wait protocol is used on a link with a bit rate of 64 kilobits per second and 20 milliseconds propagation delay. Assume that the transmission time for the acknowledgment and the processing time at nodes are negligible. Then the minimum frame size in bytes to achieve a link utilization of at least 50 % is _____.

gate2015-cse-set1 computer-networks stop-and-wait normal numerical-answers

Answer



A sender uses the Stop-and-Wait ARQ protocol for reliable transmission of frames. Frames are of size 1000 bytes and the transmission rate at the sender is 80 Kbps (1 Kbps = 1000 bits/second). Size of an acknowledgment is 100 bytes and the transmission rate at the receiver is 8 Kbps. The one-way propagation delay is 100 milliseconds.

Assuming no frame is lost, the sender throughput is _____ bytes/ second.

gate2016-cse-set1 computer-networks stop-and-wait normal numerical-answers

Answer



The values of parameters for the Stop-and-Wait ARQ protocol are as given below:

- Bit rate of the transmission channel = 1 Mbps.
- Propagation delay from sender to receiver = 0.75 ms.
- Time to process a frame = 0.25 ms.
- Number of bytes in the information frame = 1980.
- Number of bytes in the acknowledge frame = 20.
- Number of overhead bytes in the information frame = 20.

Assume there are no transmission errors. Then, the transmission efficiency (expressed in percentage) of the Stop-and-Wait ARQ protocol for the above parameters is _____ (correct to 2 decimal places).

gate2017-cse-set1 computer-networks stop-and-wait numerical-answers normal

Answer



A channel has a bit rate of 4 *kbps* and one-way propagation delay of 20 *ms*. The channel uses stop and wait protocol. The transmission time of the acknowledgment frame is negligible. To get a channel efficiency of at least 50%, the minimum frame size should be

- A. 80 bytes
- B. 80 bits
- C. 160 bytes
- D. 160 bits

gate2005-it computer-networks stop-and-wait normal

Answer



On a wireless link, the probability of packet error is 0.2. A stop-and-wait protocol is used to transfer data across the link. The channel condition is assumed to be independent of transmission to transmission. What is the average number of transmission attempts required to transfer 100 packets?

- A. 100
- B. 125
- C. 150
- D. 200



✓

$$\text{Link Utilization} = \frac{\text{Amount of data sent}}{\text{Max. amount of data that could be sent}}$$

Let x be the frame size in bits.

In stop-and-wait protocol, once a frame is sent, next frame won't be sent until ACK is received.

Time for this,

RTT = Propagation delay for frame + Transmission time for frame
+ Propagation delay for ACK + Transmission time for ACK

$$= 20 \text{ ms} + \frac{x}{64 \text{ ms}} + 20 \text{ ms} + 0 \quad (\text{as given in question})$$

$$= \left(40 + \frac{x}{64}\right) \text{ ms}.$$

Amount of data sent during RTT = x

$$\text{Max. amount of data that could be sent} = \left(40 + \frac{x}{64}\right) \times 64 = 2560 + x \text{ bits}.$$

$$\text{So, link utilization, } 0.5 = \frac{x}{(2560 + x)}$$

$$x = 2560 \text{ bits} = 320 \text{ bytes}.$$

Alternative Approach ,

Link utilization or efficiency of stop and wait protocol is ,

$$\text{efficiency} = \frac{T_x}{(T_x + 2T_p)} = \frac{1}{\left(1 + 2\left(\frac{T_p}{T_x}\right)\right)} = \frac{1}{(1 + 2a)},$$

$$\text{where, Transmission time} = T_x = \frac{\text{packet size}}{\text{bandwidth}} = \frac{L}{B}$$

$$\text{Propagation time} = T_p = \frac{\text{distance}}{\text{speed}} = \frac{d}{v}, \text{ and}$$

$$a = \frac{\text{Propagation time}}{\text{Transmission time}} = \frac{T_p}{T_x},$$

Now for 50% efficiency ,

$$\text{efficiency} = \frac{1}{(1 + 2a)}$$

$$50\% = \frac{1}{(1 + 2a)}$$

$$\frac{1}{2} = \frac{1}{(1 + 2a)}$$

$$2 = (1 + 2a)$$

$$2 - 1 = 2a$$

$$1 = 2\left(\frac{T_p}{T_x}\right)$$

$$T_x = 2 \times T_p$$

$$\frac{L}{B} = 2 \times 20 \text{ ms}$$

$$L = 2 \times 20 \text{ ms} \times B = 2 \times 20 \times 10^{-3} \times 64 \text{ k bits}$$

$$= 2 \times 20 \times 10^{-3} \times 64 \times 10^3 \text{ bits}$$

$$L = 40 \times 64 \text{ bits} = 40 \times \frac{64}{8} \text{ bytes} = 40 \times 8 \text{ bytes} = 320 \text{ bytes (answer)}$$

👍 59 votes

classroom.gateoverflow.in
-- Arjun Suresh (332k points)

2.27.2 Stop And Wait: GATE CSE 2016 Set 1 | Question: 55 top ⬆

https://gateoverflow.in/39696



✓ Answer is 2500 bytes per second.

Throughput is number of bytes we are able to send per second.

Calculate the transmission time of sender $T_{t(Send)}$, calculate one way propagation delay T_p , Calculate the transmission time of receiver $T_{t(Recv)}$

We get $T_{t(Send)}$ here as $\frac{1}{10}$ seconds,

T_p as $\frac{1}{10}$ seconds (given in question as 100 ms),

$T_{t(Recv)}$ as $\frac{1}{10}$ seconds.

So, total time taken to send a frame from sender to destination,

$$= T_{t(Send)} + 2 \times T_p + T_{t(Recv)} = \frac{4}{10} \text{ seconds}$$

So, we can send 1000 bytes (frame size) in $\frac{4}{10}$ seconds.

in 1 second, we can send 2500 bytes. So throughput is 2500 bytes per second.

👍 62 votes

-- Sreyas S (1.6k points)

Answer is 2500.

$$\text{Sender transmission time} = \frac{1000 \times 8}{(80 \times 1000)} = 0.1 \text{ sec} = 100 \text{ ms}$$

$$\text{Receiver transmission time} = \frac{100 \times 8}{(8 \times 1000)} = 0.1 \text{ sec} = 100 \text{ ms}$$

$$\text{RTT} = 2 \times 100 = 200 \text{ ms}$$

So, Total time = 400 ms

In 400 ms, we send only 1000 bytes so,

$$\text{Throughput} = \frac{1000}{(400 \times 10^{-3})} = 2500 \text{ bytes / sec}$$

👍 44 votes

-- Deepak Sharma (545 points)

2.27.3 Stop And Wait: GATE CSE 2017 Set 1 | Question: 45 top ⬆

https://gateoverflow.in/118328



✓ Efficiency is usually calculated as, $\frac{\text{InfoFrame Transmit Time}}{\text{TotalTime}}$

$$\text{Efficiency} = \frac{\text{InfoFrame Transmit Time}}{\text{InfoFrame Transmit Time} + \text{InfoFrame Process Time} + 2 \times \text{Prop Delay} + \text{AckFrame Transmit Time} + \text{AckFrame Process Time}}$$

Reference to calculate efficiency formula:

http://nptel.ac.in/courses/106106091/pdf/Lecture13_StopAndWaitAnalysis.pdf

<http://spinlab.wpi.edu/courses/ece230x/lec14-15.pdf>

From the question it is not very clear whether frame processing time is mentioned about InfoFrame or AckFrame or Combined. It is also explicitly not mentioned whether to consider Frame Processing time for ACK or not. Thus, following are the different inferences that could be made from the question -

1. As Size of InfoFrame (1980-2000 Bytes) is very large as compared to AckFrame (20 Bytes) one could assume the given processing time is for InfoFrame and processing time for AckFrame is negligible. The processing time does depend on size of frame for various parameters one of them is checksum calculation.
Check the below reference for more details -
http://rp-www.cs.usyd.edu.au/~suparek/Research/Doc/Stop-and-Wait_Simulation.pdf
2. It is also mentioned in the question that there are no transmission errors. One can also think as a hint that since frames are successfully transmitted there is no need for ACK processing at sender Side
3. Considering frame processing time given is combined both ACK+Info Frame
4. Considering frame processing time individually and which is the Ans in Official key (86.5 - 87.5)

The below answers could be due to cases 1,2,3 -
No. of Bytes in the Information frame = 1980 Bytes
(Not very clear from question whether it implies total bytes or data bytes)

No of OverHead Bytes = 20 Bytes

Assuming they have explicitly mentioned Overhead bytes -

Total Frame Size = No of Bytes in the Information frame + No of OverHead Bytes = 2000 B

$$\text{InfoTransmission Time} = \frac{\text{InfoFrame Size}}{\text{Bandwidth}}$$

$$= \frac{2000 \times 8}{1 \times 10^6} = 16 \text{ ms}$$

$$\text{AckTransmissionTime} = \frac{20 \times 8}{1 \times 10^6} = 0.16 \text{ ms}$$

$$\text{Efficiency} = \frac{16}{16 + 2 \times 0.75 + 0.25 + 0.16}$$

$$= 89.34\% \text{ (After round-off)}$$

Assuming bytes in information includes Overhead bytes -

InfoFrameTransmission Time = 15.84

Efficiency = 89.23 %

Range could be 87.5 - 89.34

Reference to the similar questions:

<https://gateoverflow.in/43981/isro-2013-41>

<https://gateoverflow.in/39696/gate-2016-1-55>

More Efficiency Concept Reference:

<http://nptel.ac.in/courses/Webcourse-contents/IIT%20Kharagpur/Computer%20networks/pdf/M3L3.pdf>

References



👍 57 votes

-- yg92 (2.3k points)

2.27.4 Stop And Wait: GATE IT 2005 | Question: 72 [top](#)

<https://gateoverflow.in/3835>



- ✓ For 50% utilization with Stop-and-wait,

$$\frac{t_t}{t_t + 2t_p} \geq \frac{1}{2},$$

where, t_t – Transmission time, t_p – propagation delay. Here, $t_t = \frac{L}{B}$, where L is the frame length in bits and B is the bitrate of the channel.

$$2t_t \geq t_t + 2t_p$$

$$t_t \geq 2t_p$$

$$\frac{L}{B} \geq 2 \times t_p$$

$$L \geq 2 \times t_p \times B$$

$$\implies L = 2 \times 20 \times 10^{-3} \times 4 \times 10^3 = 160 \text{ bits}$$

So, answer is D.

👍 32 votes

-- Pooja Palod (24.1k points)

2.27.5 Stop And Wait: GATE IT 2006 | Question: 68 [top](#)

<https://gateoverflow.in/3612>



✓ Consider that we have to send N packets and p is the error probability rate. Error rate p implies that if we are sending N packets then $N \times p$ packets will be lost and thus we have to resend those $N \times p$ packets. But the error is still there, so again while resending those $N \times p$ packets, $N \times p \times p$ will be further lost and so on. Hence, this forms a series as follows:

$$\begin{aligned} & N + N \times p + N \times p^2 + \dots \\ &= N(1 + p + p^2 + \dots) \\ &= \frac{N}{1 - p} \text{ (Sum to infinite GP series)} \end{aligned}$$

Now we are having $N = 100$ and $p = 0.2$, which implies 125 packets have to be sent on average.

Correct Answer: B

👍 46 votes

-- AAKASH SAINI (1.6k points)

2.28

Subnetting (18) [top](#)

2.28.1 Subnetting: GATE CSE 2003 | Question: 82, ISRO2009-1 [top](#)

<https://gateoverflow.in/965>



The subnet mask for a particular network is 255.255.31.0. Which of the following pairs of IP addresses could belong to this network?

- A. 172.57.88.62 and 172.56.87.23
- B. 10.35.28.2 and 10.35.29.4
- C. 191.203.31.87 and 191.234.31.88
- D. 128.8.129.43 and 128.8.161.55

gate2003-cse computer-networks subnetting normal isro2009

Answer [👍](#)

2.28.2 Subnetting: GATE CSE 2004 | Question: 55 [top](#)

<https://gateoverflow.in/1051>



The routing table of a router is shown below:

Destination	Subnet Mask	Interface
128.75.43.0	255.255.255.0	Eth0
128.75.43.0	255.255.255.128	Eth1
192.12.17.5	255.255.255.255	Eth3
Default		Eth2

On which interface will the router forward packets addressed to destinations 128.75.43.16 and 192.12.17.10 respectively?

- A. Eth1 and Eth2
- B. Eth0 and Eth2

- C. Eth0 and Eth3
- D. Eth1 and Eth3

gate2004-cse computer-networks subnetting normal

Answer

2.28.3 Subnetting: GATE CSE 2005 | Question: 27 top

<https://gateoverflow.in/1363>



An organization has a class B network and wishes to form subnets for 64 departments. The subnet mask would be:

- A. 255.255.0.0
- B. 255.255.64.0
- C. 255.255.128.0
- D. 255.255.252.0

gate2005-cse computer-networks subnetting normal

Answer

2.28.4 Subnetting: GATE CSE 2006 | Question: 45 top

<https://gateoverflow.in/1821>



Two computers C_1 and C_2 are configured as follows. C_1 has IP address 203.197.2.53 and netmask 255.255.128.0. C_2 has IP address 203.197.75.201 and netmask 255.255.192.0. Which one of the following statements is true?

- A. C_1 and C_2 both assume they are on the same network
- B. C_2 assumes C_1 is on same network, but C_1 assumes C_2 is on a different network
- C. C_1 assumes C_2 is on same network, but C_2 assumes C_1 is on a different network
- D. C_1 and C_2 both assume they are on different networks.

gate2006-cse computer-networks subnetting normal

Answer

2.28.5 Subnetting: GATE CSE 2007 | Question: 67, ISRO2016-72 top

<https://gateoverflow.in/1265>



The address of a class B host is to be split into subnets with a 6-bit subnet number. What is the maximum number of subnets and the maximum number of hosts in each subnet?

- A. 62 subnets and 262142 hosts.
- B. 64 subnets and 262142 hosts.
- C. 62 subnets and 1022 hosts.
- D. 64 subnets and 1024 hosts.

gate2007-cse computer-networks subnetting easy isro2016

Answer

2.28.6 Subnetting: GATE CSE 2008 | Question: 57 top

<https://gateoverflow.in/480>



If a class B network on the Internet has a subnet mask of 255.255.248.0, what is the maximum number of hosts per subnet?

- A. 1022
- B. 1023
- C. 2046
- D. 2047

gate2008-cse computer-networks subnetting easy

Answer



Suppose computers A and B have IP addresses 10.105.1.113 and 10.105.1.91 respectively and they both use same netmask N . Which of the values of N given below should not be used if A and B should belong to the same network?

- A. 255.255.255.0
- B. 255.255.255.128
- C. 255.255.255.192
- D. 255.255.255.224

gate2010-cse computer-networks subnetting easy

Answer



An Internet Service Provider (ISP) has the following chunk of CIDR-based IP addresses available with it: 245.248.128.0/20. The ISP wants to give half of this chunk of addresses to Organization A , and a quarter to Organization B , while retaining the remaining with itself. Which of the following is a valid allocation of addresses to A and B ?

- A. 245.248.136.0/21 and 245.248.128.0/22
- B. 245.248.128.0/21 and 245.248.128.0/22
- C. 245.248.132.0/22 and 245.248.132.0/21
- D. 245.248.136.0/24 and 245.248.132.0/21

gate2012-cse computer-networks subnetting normal isrodec2017

Answer



Consider the following routing table at an IP router:

Network No	Net Mask	Next Hop
128.96.170.0	255.255.254.0	Interface 0
128.96.168.0	255.255.254.0	Interface 1
128.96.166.0	255.255.254.0	R2
128.96.164.0	255.255.252.0	R3
0.0.0.0	Default	R4

For each IP address in Group I identify the correct choice of the next hop from Group II using the entries from the routing table above.

Group I	Group II
i) 128.96.171.92	a) Interface 0
ii) 128.96.167.151	b) Interface 1
iii) 128.96.163.151	c) R2
iv) 128.96.164.121	d) R3
	e) R4

- A. i-a, ii-c, iii-e, iv-d
- B. i-a, ii-d, iii-b, iv-e
- C. i-b, ii-c, iii-d, iv-e
- D. i-b, ii-c, iii-e, iv-d

gate2015-cse-set2 computer-networks subnetting easy

Answer



In the network 200.10.11.144/27, the *fourth* octet (in decimal) of the last IP address of the network which can be assigned

to a host is _____.

gate2015-cse-set3 computer-networks subnetting normal numerical-answers

Answer 

2.28.11 Subnetting: GATE CSE 2019 | Question: 28 [top](#)

<https://gateoverflow.in/302820>



Consider three machines M, N, and P with IP addresses 100.10.5.2, 100.10.5.5, and 100.10.5.6 respectively. The subnet mask is set to 255.255.255.252 for all the three machines. Which one of the following is true?

- A. M, N, and P all belong to the same subnet
- B. Only M and N belong to the same subnet
- C. Only N and P belong to the same subnet
- D. M, N, and P belong to three different subnets

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gate2019-cse computer-networks subnetting

Answer 

2.28.12 Subnetting: GATE CSE 2020 | Question: 38 [top](#)

<https://gateoverflow.in/333193>



An organization requires a range of IP address to assign one to each of its 1500 computers. The organization has approached an Internet Service Provider (ISP) for this task. The ISP uses CIDR and serves the requests from the available IP address space 202.61.0.0/17. The ISP wants to assign an address space to the organization which will minimize the number of routing entries in the ISP's router using route aggregation. Which of the following address spaces are potential candidates from which the ISP can allot any one of the organization?

- I. 202.61.84.0/21
- II. 202.61.104.0/21
- III. 202.61.64.0/21
- IV. 202.61.144.0/21

- A. I and II only
- B. II and III only
- C. III and IV only
- D. I and IV only

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gate2020-cse computer-networks subnetting

Answer 

2.28.13 Subnetting: GATE IT 2004 | Question: 26 [top](#)

<https://gateoverflow.in/3667>



A subnet has been assigned a subnet mask of 255.255.255.192. What is the maximum number of hosts that can belong to this subnet?

- A. 14
- B. 30
- C. 62
- D. 126

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gate2004-it computer-networks subnetting normal

Answer 

2.28.14 Subnetting: GATE IT 2005 | Question: 76 [top](#)

<https://gateoverflow.in/3839>



A company has a class C network address of 204.204.204.0. It wishes to have three subnets, one with 100 hosts and two with 50 hosts each. Which one of the following options represents a feasible set of subnet address/subnet mask pairs?

- A. 204.204.204.128/255.255.255.192
204.204.204.0/255.255.255.128
204.204.204.64/255.255.255.128
- B. 204.204.204.0/255.255.255.192
204.204.204.192/255.255.255.128

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- 204.204.204.64/255.255.255.128
- C. 204.204.204.128/255.255.255.128
204.204.204.192/255.255.255.192
204.204.204.224/255.255.255.192
- D. 204.204.204.128/255.255.255.128
204.204.204.64/255.255.255.192
204.204.204.0/255.255.255.192

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gate2005-it computer-networks subnetting normal

Answer

2.28.15 Subnetting: GATE IT 2006 | Question: 63, ISRO2015-57 [top](#)

<https://gateoverflow.in/3607>



A router uses the following routing table:

Destination	Mask	Interface
144.16.0.0	255.255.0.0	eth0
144.16.64.0	255.255.224.0	eth1
144.16.68.0	255.255.255.0	eth2
144.16.68.64	255.255.255.224	eth3

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Packet bearing a destination address 144.16.68.117 arrives at the router. On which interface will it be forwarded?

- A. eth0
B. eth1
C. eth2
D. eth3

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gate2006-it computer-networks subnetting normal isro2015

Answer

2.28.16 Subnetting: GATE IT 2006 | Question: 70 [top](#)

<https://gateoverflow.in/3614>



A subnetted Class *B* network has the following broadcast address: 144.16.95.255

Its subnet mask

- A. is necessarily 255.255.224.0
B. is necessarily 255.255.240.0
C. is necessarily 255.255.248.0
D. could be any one of 255.255.224.0, 255.255.240.0, 255.255.248.0

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gate2006-it computer-networks subnetting normal

Answer

2.28.17 Subnetting: GATE IT 2008 | Question: 84 [top](#)

<https://gateoverflow.in/3408>



Host *X* has IP address 192.168.1.97 and is connected through two routers *R1* and *R2* to another host *Y* with IP address 192.168.1.80. Router *R1* has IP addresses 192.168.1.135 and 192.168.1.110. *R2* has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Given the information above, how many distinct subnets are guaranteed to already exist in the network?

- A. 1
B. 2
C. 3
D. 6

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gate2008-it computer-networks subnetting normal

Answer



Host X has IP address 192.168.1.97 and is connected through two routers $R1$ and $R2$ to another host Y with IP address 192.168.1.80. Router $R1$ has IP addresses 192.168.1.135 and 192.168.1.110. $R2$ has IP addresses 192.168.1.67 and 192.168.1.155. The netmask used in the network is 255.255.255.224.

Which IP address should X configure its gateway as?

- A. 192.168.1.67
- B. 192.168.1.110
- C. 192.168.1.135
- D. 192.168.1.155

gate2008-it computer-networks subnetting normal

Answer [↕](#)

Answers: Subnetting



- ✓ (A) and (C) are not the answers as the second byte of IP differs and subnet mask has 255 for second byte.

Consider (B), (& for bitwise AND)

$$10.35.28.2 \& 255.255.31.0 = 10.35.28.0 (28 = 11100_2)$$

$$10.35.29.4 \& 255.255.31.0 = 10.35.29.0 (29 = 11101_2)$$

So, we get different subnet numbers

Consider (D).

$$128.8.129.43 \& 255.255.31.0 = 128.8.1.0 (129 = 1000001_2)$$

$$128.8.161.55 \& 255.255.31.0 = 128.8.1.0 (161 = 10100001_2)$$

The subnet number matches. So, (D) is the answer.

[👍](#) 113 votes

-- Arjun Suresh (332k points)



- ✓ The answer must be A.

(Using \wedge to denote bitwise AND)

For 1st packet,

$$(128.75.43.16) \wedge (255.255.255.0) = (128.75.43.0) \text{ since } \{16 \wedge 0 = 0\}, \text{ as well as}$$

$$(128.75.43.16) \wedge (255.255.255.128) = (128.75.43.0) \text{ since } \{16 \wedge 128 = 0\}.$$

Now, since both these subnet masks are producing the same Network ID, hence The one with greater number of ones will be selected, and the packet will be forwarded there. Hence packet 1 will be forwarded to Eth1.

For 2nd packet,

(192.12.17.10) when ANDed with each of the subnet masks does not match with any of the network ID, since:

$$(192.12.17.10) \wedge (255.255.255.0) = (192.12.17.0) \text{ \{Does not match with any of the network addresses\}}$$

$$(192.12.17.10) \wedge (255.255.255.128) = (192.12.17.0) \text{ \{Does not match with any of the network addresses\}}$$

$$(192.12.17.10) \wedge (255.255.255.255) = (192.12.17.10) \text{ \{Does not match with any of the network addresses\}}$$

Hence, default interface must be selected for packet 2, i.e., Interface Eth2.

[👍](#) 57 votes

-- saurabhk (1k points)



- ✓ D is correct answer.

To form subnet for 64 departments we need 6 continuous bit and the value of $11111100 = 252$.

Organization has class B network so subnet mask would be **255.255.252.0**

2.28.4 Subnetting: GATE CSE 2006 | Question: 45 top

https://gateoverflow.in/1821



Subnetmask for C1 is 255.255.128.0. So, it finds the network ID as:

$$203.197.2.53 \text{ AND } 255.255.128.0 = 203.197.0.0$$
$$203.197.75.201 \text{ AND } 255.255.128.0 = 203.197.0.0$$

Both same.

Now subnetmask for C2 is 255.255.192.0. So, the respective network IDs are:

$$203.197.2.53 \text{ AND } 255.255.192.0 = 203.197.0.0$$
$$203.197.75.201 \text{ AND } 255.255.192.0 = 203.197.64.0$$

Both not same. So, option C.

51 votes

-- Arjun Suresh (332k points)

2.28.5 Subnetting: GATE CSE 2007 | Question: 67, ISRO2016-72 top

https://gateoverflow.in/1265



In class B .. first 2 octet are reserved for NID and remaining for HID .. so first 6 bits of 3rd octet are used for subnet and remaining 10 bits for hosts ..

$$\text{Maximum number of subnets} = 2^6 - 2 = 62$$

Note that 2 is subtracted because subnet values consisting of all zeros and all ones (broadcast), reducing the number of available subnets by two in classic subnetting. In modern networks, we can have 64 as well. See here: <http://www.weird.com/~woods/classb.html>

$$\text{and no of hosts} = 2^{10} - 2 = 1022.$$

2 is subtracted for Number of hosts is also. The address with all bits as 1 is reserved as broadcast address and address with all host id bits as 0 is used as network address of subnet.

So option (C) is correct..

References



57 votes

-- minal (13.1k points)

This question is asking **maximum no of subnets and hosts/subnet...NOT how many hosts are configurable**. So, no need to Subtract 2 in either case.

Subnet bits = 6

means 2^6 or 64 subnets are possible..

and, total hosts= 2^{10} or 1024 hosts..again no need to subtract 2 since question is asking maximum no of hosts possible not how much we can configure.

So, **option d should be right** according to what they mean by maximum.

EDIT:

This is becoming a very debatable question now....firstly whatever explanation i have given is right according to question formation...people are arguing that we should subtract 2 hosts from the available, for use..i agree..but this question was about maximum possible and one option also matched..so i gone with this...

Now what to do if something like this happens again in future?

From all previous year questions over this topic it seems like we have to mind read them as what they actually mean...means for the gate questions **they are treating maximum possible hosts and available hosts all as same....**so go only according to that

else it would be very difficult to prove their thoughts wrong..

Now if asked **how many maximum subnets** we can use..**dont subtract anything**. This at least i can prove easily but mind it. **GATE still uses previous conventions of subtracting 2 subnets**..atleast this is what shown here in 2007..

If they ask **maximum hosts** or **configurable hosts**, anything. **They actually wants us to subtract 2** from the hosts and then answer. **For gate questions i think English doesnt matter..u should answer according to the past experiences and questions they have asked.**

At last, for this question **maximum subnets are 64 and hosts are 1022 is the actual answer but according to old conventions 62 and 1022**.So, go with.

Option C(closest). Choose wisely in the exam. I have explained each aspect of the question. I rest here and there should not be any more confusion regarding this!!

👍 54 votes

-- Shobhit (13.5k points)

2.28.6 Subnetting: GATE CSE 2008 | Question: 57 [top](#)

<https://gateoverflow.in/480>



✓ a number of zeros are to be counted for calculating the total number of possible hosts per subnet.

$255-248 = 7$ can be represented using 3 bits

these $3\text{bits} + 8\text{bits}$ more = 11 bits

So, possible subnets = 2^{11} out of these 2 are reserved as subnet *ID* and *DBA*

Therefore, we have maximum possible usable hosts = $2^{11} - 2 = 2046$

Correct Answer: *C*

👍 35 votes

-- Amar Vashishth (25.2k points)

2.28.7 Subnetting: GATE CSE 2010 | Question: 47 [top](#)

<https://gateoverflow.in/2349>



✓ **D** is correct answer because:

When we perform *AND* operation between *IP* address 10.105.1.113 and 255.255.255.224 result is 10.105.1.96

When we perform *AND* operation between *IP* address 10.105.1.91 and 255.255.255.224 result is 10.105.1.64

10.105.1.96 and 10.105.1.64 are different network so *D* is correct answer.

👍 37 votes

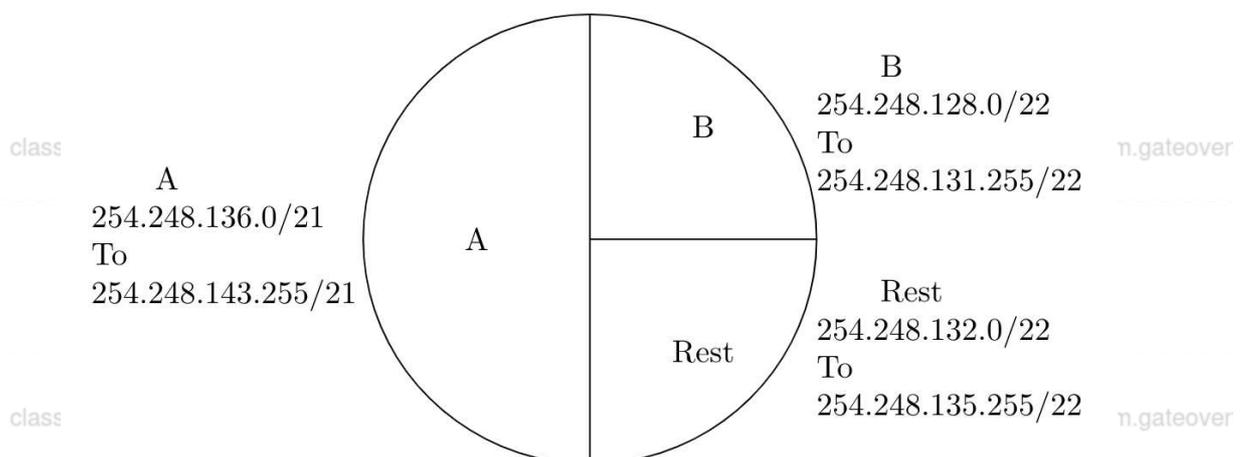
-- R.B. Tiwari (257 points)

2.28.8 Subnetting: GATE CSE 2012 | Question: 34, ISRO-DEC2017-32 [top](#)

<https://gateoverflow.in/1752>



✓



Correct option will be A

44 votes

-- Ashish Patel (297 points)



✓ Taking the 1st IP Address: 128.96.171.92

Bitwise AND between 128.96.171.92 and 255.255.254.0 we get the subnet ID as follows:

255	255	11111110	0
128	96	10101011	92
128	96	10101010	0

∴ Subnet ID = 128.96.170.0
∴ 128.96.171.92 will forward to interface 0

Taking the 2nd IP Address: 128.96.167.151

Bitwise AND between 128.96.167.151 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100111	151
128	96	10100110	0

∴ Subnet ID = 128.96.166.0
∴ 128.96.167.151 will forward to interface R2

Taking the 3rd IP Address: 128.96.163.151

Bitwise AND between 128.96.167.151 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100011	151
128	96	10100010	0

∴ Subnet ID = 128.96.162.0 (Doesn't match with any given interface)

Now, Bitwise AND between 128.96.167.151 and 255.255.252.0 we get,

255	255	11111100	0
128	96	10100011	151
128	96	10100000	0

∴ Subnet ID = 128.96.160.0 (Doesn't match with any given interface)

∴ 128.96.163.151 will forward to default interface R4

Taking the last IP Address: 128.96.164.121

Bitwise AND between 128.96.164.121 and 255.255.254.0 we get,

255	255	11111110	0
128	96	10100100	121
128	96	10100100	0

∴ Subnet ID = 128.96.164.0
∴ 128.96.167.151 will forward to interface R3

∴ Option (a) is the correct answer

16 votes

-- Pritha Majumder (487 points)



✓ Answer= 158

144 in binary = 10010000

out of this 3 bits in left are subnet bits. (27 bits are used for subnet, which means top 3 bytes and leftmost 3 bits from the last byte)

So, the 4th octet in the last IP address of the network which can be assigned to a host is 10011110. (its not 10011111 because its network broadcast address)

So, 10011110 is 158 in decimal.

👍 66 votes

-- overtomanu (945 points)

2.28.11 Subnetting: GATE CSE 2019 | Question: 28 top 5

<https://gateoverflow.in/302820>



✓ First derive the network address of those machines, then we can decide !

Finding network address for a M/C :- Perform Bitwise AND between m/c address and given subnet mask.

Subnet Mask: keep 1's in Network part + subnet part and keep 0's in Host part.

255.255.255.252 = 11111111.11111111.11111111.11111100
⇒ 24(from first 3 octets) + 6(in last octet)
= 30bits in Network+ subnet portion and last 2 bits represent the Host part.

Subnet Mask = 255.255.255.252 and M = 100.10.5.2 but keep all zero's in HOST part !

100 = 01100100	10 = 00001010	5 = 00000101	2 = 00000000
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	0

Subnet Mask = 255.255.255.252 and N = 100.10.5.5 but keep all zero's in HOST part !

100 = 01100100	10 = 00001010	5 = 00000101	5 = 00000100
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	4

Subnet Mask = 255.255.255.252 and P = 100.10.5.6 but keep all zero's in HOST part !

100 = 01100100	10 = 00001010	5 = 00000101	6 = 00000100
255 = 11111111	255 = 11111111	255 = 11111111	252 = 11111100
100	10	5	4

∴ only N and P are belong to same network (100.10.5.4/30)

👍 20 votes

-- Shaik Masthan (50.4k points)

2.28.12 Subnetting: GATE CSE 2020 | Question: 38 top 5

<https://gateoverflow.in/333193>



✓ (B) II and III only

Given IP address space: 202.61.0.0/17, 17 bits are in network ID bits(NID) and rest will be host ID bits(HID).

202.61.00000000.00000000
17 NID bits

In order to assign 1500 hosts we need minimum 11 bits

202.61.0 0000 000.00000000
17 NID bits 4 SID bits 11 HID bits

We have 4 subnet bits, eligible networks are those which belongs among possible 16 subnets.

If we expand the given Network bits we can see:

- 202.61.84.0/21 = 202.61.01010100.0

- Not possible as all Host Bits should be zero
- $202.61.104.0/21 = 202.61.01101000.0$
Possible
- $202.61.64.0/21 = 202.61.01000000.0$
Possible
- $202.61.144.0/21 = 202.61.10010000.0$
Not possible as 16^{th} bit from right (part of NID is 0 and not 1)

👍 30 votes

-- Ashwani Kumar (1.3k points)

2.28.13 Subnetting: GATE IT 2004 | Question: 26 [top](#)

<https://gateoverflow.in/3667>



- ✓ (C) is answer since you have 6 zeroes so you can make $64 - 2$ hosts

👍 25 votes

-- Shreyans Dhankhar (2.1k points)

2.28.14 Subnetting: GATE IT 2005 | Question: 76 [top](#)

<https://gateoverflow.in/3839>



- ✓ Answer is **D**.

MSB in last 8 bits helps us to get two subnets

- 10000000 → subnet1
- 00000000 → subnet2

subnet2 is divided into 2 more subnets using 7th bit

- 00000000 → subnet2(0)
- 01000000 → subnet2(1)

👍 29 votes

-- nagalla pruthvi (675 points)

2.28.15 Subnetting: GATE IT 2006 | Question: 63, ISRO2015-57 [top](#)

<https://gateoverflow.in/3614>



- ✓ Firstly start with **Longest mask**

$144.16.68.117 = 144.16.68.01110101$ AND $255.255.255.224 = 255.255.255.11100000$
 $= 144.16.68.96$ (Not matching with Destination)

Now, take $255.255.255.0$

$144.16.68.117$ AND $255.255.255.0 = 144.16.68.0$ (matched)

So, interface chosen is **eth2 OPTION (C)**.

👍 54 votes

-- Himanshu Agarwal (12.4k points)

2.28.16 Subnetting: GATE IT 2006 | Question: 70 [top](#)

<https://gateoverflow.in/3614>



- ✓ Option (D) is correct. In the broadcast address for a subnet, all the host bits are set to 1. So as long as all the bits to the right are 1, bits left to it can be taken as possible subnet.

Broadcast address for subnet is $.95.255.01011111.11111111$ (as in Class B, 16 bits each are used for network and host)

So, we can take minimum 3 bits (from left) as subnet and make rest as host bits (as they are 1).

- .224.0 11100000.00000000 (leftmost 3 bits for subnet)
- .240.0 11110000.00000000 (leftmost 4 bits for subnet)
- .248.0 11111000.00000000 (... 5 bits for subnet)

50 votes

-- Sandeep_Uniyal (6.5k points)

2.28.17 Subnetting: GATE IT 2008 | Question: 84 top

https://gateoverflow.in/3408



✓ 255.255.255.224 = 11111111.11111111.11111111.11100000

- 192.168.1.97
- 192.168.1.80
- 192.168.1.135
- 192.168.1.110
- 192.168.1.67
- 192.168.1.155

We need to do bitwise AND with subnet mask.
the last 5 bits are going to be 0 when ANDED.

No need to waste time in finding binary.
Only focus on 1st 3 bits of binary.

(From left side, 1st bit is 128,next one is 64,next one is 32..it goes like that you know.)

- 97: 0 + 64 + 32+ something so 1st 3 bits will contain 011
- 80: 0 + 64 + 0+ something so 010
- 135: 128 + 0 + 0+ something so 100
- 110: 0 + 64 + 32+ something so 011
- 67: 0 + 64 + 0+ something so 010
- 155: 128 + 0 + 0+ something so 100

So we got 011, 010, 100
3 subnets.... subnet id are...

- 192.168.1.96
- 192.168.1.64
- 192.168.1.128

Correct Answer: C

51 votes

-- Ahwan Mishra (10.2k points)

2.28.18 Subnetting: GATE IT 2008 | Question: 85 top

https://gateoverflow.in/3409



✓ X must be able to reach the gateway using the net mask.
Subnet number of host X = 192.168.1.97 & 255.255.255.224 =192.168.1.96

Now, the gateway must also have the same subnet number. Lets take IP 192.168.1.110 of R1. 192.168.1.110 & 255.255.255.224 =192.168.1.96 and hence this can be used by X.

(To quickly identify the matching mask divide the last part of mask (224 here) into powers of 2. So, 224 = 128 + 64+ 32. Now, our host X has 97 as the last part of IP = 64 + 32 + 1. So, the last part of subnet number becomes 64 +32 =96. Now, we need to consider only those IPs whose last part will contain 64 as well as 32)

http://courses.washington.edu/css432/joemcc/slides/03_cidr.ppt

Correct Answer: B

References



58 votes

-- Arjun Suresh (332k points)



While opening a *TCP* connection, the initial sequence number is to be derived using a time-of-day (ToD) clock that keeps running even when the host is down. The low order 32 bits of the counter of the ToD clock is to be used for the initial sequence numbers. The clock counter increments once per milliseconds. The maximum packet lifetime is given to be 64s.

Which one of the choices given below is closest to the minimum permissible rate at which sequence numbers used for packets of a connection can increase?

- A. 0.015/s
- B. 0.064/s
- C. 0.135/s
- D. 0.327/s

gate2009-cse computer-networks tcp difficult ambiguous

Answer



Which of the following transport layer protocols is used to support electronic mail?

- A. SMTP
- B. IP
- C. TCP
- D. UDP

gate2012-cse computer-networks tcp easy

Answer



Suppose two hosts use a *TCP* connection to transfer a large file. Which of the following statements is/are FALSE with respect to the *TCP* connection?

- I. If the sequence number of a segment is m , then the sequence number of the subsequent segment is always $m+1$.
- II. If the estimated round trip time at any given point of time is t sec, the value of the retransmission timeout is always set to greater than or equal to t sec.
- III. The size of the advertised window never changes during the course of the *TCP* connection.
- IV. The number of unacknowledged bytes at the sender is always less than or equal to the advertised window.

- A. III only
- B. I and III only
- C. I and IV only
- D. II and IV only

gate2015-cse-set1 computer-networks tcp normal

Answer



Assume that the bandwidth for a *TCP* connection is 1048560 bits/sec. Let α be the value of RTT in milliseconds (rounded off to the nearest integer) after which the *TCP* window scale option is needed. Let β be the maximum possible window size with window scale option. Then the values of α and β are

- A. 63 milliseconds, 65535×2^{14}
- B. 63 milliseconds, 65535×2^{16}
- C. 500 milliseconds, 65535×2^{14}
- D. 500 milliseconds, 65535×2^{16}

gate2015-cse-set2 computer-networks difficult tcp

Answer



Consider the following statements.

- I. TCP connections are full duplex
 - II. TCP has no option for selective acknowledgement
 - III. TCP connections are message streams
- A. Only I is correct
 - B. Only I and III are correct
 - C. Only II and III are correct
 - D. All of I, II and III are correct

gate2015-cse-set3 computer-networks tcp normal

Answer



Identify the correct sequence in which the following packets are transmitted on the network by a host when a browser requests a webpage from a remote server, assuming that the host has just been restarted.

- A. HTTP GET request, DNS query, TCP SYN
- B. DNS query, HTTP GET request, TCP SYN
- C. DNS query, TCP SYN, HTTP GET request.
- D. TCP SYN, DNS query, HTTP GET request.

gate2016-cse-set2 computer-networks normal tcp

Answer



Consider a TCP client and a TCP server running on two different machines. After completing data transfer, the TCP client calls close to terminate the connection and a FIN segment is sent to the TCP server. Server-side TCP responds by sending an ACK, which is received by the client-side TCP. As per the TCP connection state diagram (*RFC 793*), in which state does the client-side TCP connection wait for the FIN from the server-side TCP?

- A. LAST-ACK
- B. TIME-WAIT
- C. FIN-WAIT-1
- D. FIN-WAIT-2

gate2017-cse-set1 computer-networks tcp

Answer



Consider a long-lived *TCP* session with an end-to-end bandwidth of 1 Gbps (-10^9 bits-per-second). The session starts with a sequence number of 1234. The minimum time (in seconds, rounded to the closet integer) before this sequence number can be used again is _____

gate2018-cse computer-networks tcp normal numerical-answers

Answer



Consider a *TCP* connection between a client and a server with the following specifications; the round trip time is 6 ms, the size of the receiver advertised window is 50 KB, slow-start threshold at the client is 32 KB, and the maximum segment size is 2 KB. The connection is established at time $t = 0$. Assume that there are no timeouts and errors during transmission. Then the size of the congestion window (in KB) at time $t + 60$ ms after all acknowledgements are processed is _____

gate2020-cse numerical-answers computer-networks tcp

Answer 

2.29.10 Tcp: GATE CSE 2021 Set 1 | Question: 44 top

<https://gateoverflow.in/357407>



A TCP server application is programmed to listen on port number P on host S . A TCP client is connected to the TCP server over the network.

Consider that while the TCP connection was active, the server machine S crashed and rebooted. Assume that the client does not use the TCP keepalive timer. Which of the following behaviors is/are possible?

- A. If the client was waiting to receive a packet, it may wait indefinitely
- B. The TCP server application on S can listen on P after reboot
- C. If the client sends a packet after the server reboot, it will receive a RST segment
- D. If the client sends a packet after the server reboot, it will receive a FIN segment

tests.gatecse.in

goclasses.in

tests.gatecse.in

gate2021-cse-set1

multiple-selects

computer-networks

tcp

Answer 

2.29.11 Tcp: GATE CSE 2021 Set 1 | Question: 45 top

<https://gateoverflow.in/357406>



Consider two hosts P and Q connected through a router R . The maximum transfer unit (MTU) value of the link between P and R is 1500 bytes, and between R and Q is 820 bytes.

A TCP segment of size 1400 bytes was transferred from P to Q through R , with IP identification value as $0x1234$. Assume that the IP header size is 20 bytes. Further, the packet is allowed to be fragmented, i.e., Don't Fragment (DF) flag in the IP header is *not* set by P .

Which of the following statements is/are correct?

- A. Two fragments are created at R and the IP datagram size carrying the second fragment is 620 bytes.
- B. If the second fragment is lost, R will resend the fragment with the IP identification value $0x1234$.
- C. If the second fragment is lost, P is required to resend the whole TCP segment.
- D. TCP destination port can be determined by analysing *only* the second fragment.

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gate2021-cse-set1

computer-networks

tcp

Answer 

2.29.12 Tcp: GATE CSE 2021 Set 2 | Question: 7 top

<https://gateoverflow.in/357533>



Consider the three-way handshake mechanism followed during TCP connection establishment between hosts P and Q . Let X and Y be two random 32-bit starting sequence numbers chosen by P and Q respectively. Suppose P sends a TCP connection request message to Q with a TCP segment having SYN bit = 1, SEQ number = X , and ACK bit = 0. Suppose Q accepts the connection request. Which one of the following choices represents the information present in the TCP segment header that is sent by Q to P ?

- A. SYN bit = 1, SEQ number = $X + 1$, ACK bit = 0, ACK number = Y , FIN bit = 0
- B. SYN bit = 0, SEQ number = $X + 1$, ACK bit = 0, ACK number = Y , FIN bit = 1
- C. SYN bit = 1, SEQ number = Y , ACK bit = 1, ACK number = $X + 1$, FIN bit = 0
- D. SYN bit = 1, SEQ number = Y , ACK bit = 1, ACK number = X , FIN bit = 0

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gate2021-cse-set2

computer-networks

tcp

Answer 

2.29.13 Tcp: GATE IT 2004 | Question: 23 top

<https://gateoverflow.in/3664>



Which one of the following statements is FALSE?

- A. TCP guarantees a minimum communication rate
- B. TCP ensures in-order delivery
- C. TCP reacts to congestion by reducing sender window size
- D. TCP employs retransmission to compensate for packet loss

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Answer 2.29.14 Tcp: GATE IT 2004 | Question: 28 [top](#) <https://gateoverflow.in/3669>

In TCP, a unique sequence number is assigned to each

- A. byte
- B. word
- C. segment
- D. message

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Answer 2.29.15 Tcp: GATE IT 2007 | Question: 13 [top](#) <https://gateoverflow.in/3446>

Consider the following statements about the timeout value used in TCP.

- i. The timeout value is set to the RTT (Round Trip Time) measured during TCP connection establishment for the entire duration of the connection.
- ii. Appropriate RTT estimation algorithm is used to set the timeout value of a TCP connection.
- iii. Timeout value is set to twice the propagation delay from the sender to the receiver.

Which of the following choices hold?

- A. (i) is false, but (ii) and (iii) are true
- B. (i) and (iii) are false, but (ii) is true
- C. (i) and (ii) are false, but (iii) is true
- D. (i), (ii) and (iii) are false

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Answer 2.29.16 Tcp: GATE IT 2007 | Question: 14 [top](#) <https://gateoverflow.in/3447>

Consider a *TCP* connection in a state where there are no outstanding *ACK*s. The sender sends two segments back to back. The sequence numbers of the first and second segments are 230 and 290 respectively. The first segment was lost, but the second segment was received correctly by the receiver. Let X be the amount of data carried in the first segment (in bytes), and Y be the *ACK* number sent by the receiver.

The values of X and Y (in that order) are

- A. 60 and 290
- B. 230 and 291
- C. 60 and 231
- D. 60 and 230

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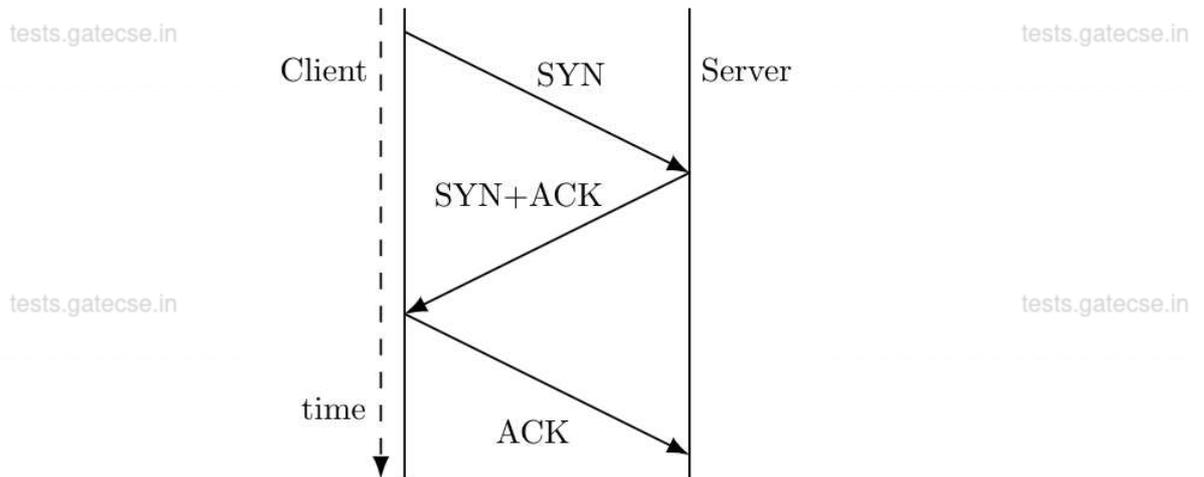
Answer 2.29.17 Tcp: GATE IT 2008 | Question: 69 [top](#) <https://gateoverflow.in/3383>

The three way handshake for TCP connection establishment is shown below.

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Which of the following statements are TRUE?

S1 : Loss of SYN + ACK from the server will not establish a connection

S2 : Loss of ACK from the client cannot establish the connection

S3 : The server moves LISTEN → SYN_RCVD → SYN_SENT → ESTABLISHED in the state machine on no packet loss

S4 : The server moves LISTEN → SYN_RCVD → ESTABLISHED in the state machine on no packet loss

- A. S2 and S3 only
- B. S1 and S4 only
- C. S1 and S3 only
- D. S2 and S4 only

gate2008-it computer-networks tcp normal

Answer

Answers: Tcp

2.29.1 Tcp: GATE CSE 2009 | Question: 47 top

<https://gateoverflow.in/1333>



✓ One of the very rare ambiguous question in GATE. It is ambiguous what the question asks for

! minimum permissible rate at which sequence numbers used for packets of a connection can increase

It is not meaningful to use "minimum" with "can increase" - should be either "maximum" with "can" or "minimum" with "should/must"

Now the second problem,

! rate at which sequence numbers used for packets of a connection

In TCP, once the Initial Sequence Number(ISN) is set, the increase in sequence number is determined by the data sent rate - for every 8 bits, it increases by 1. If the question is asking for this rate, then it is independent of the ISN and depends on the packet lifetime and number of possible sequence numbers. With 32 bits we have 2^{32} sequence numbers possible and to avoid using the same sequence number while a packet with one is still alive, we should ensure no more than 2^{32} sequence numbers in a packet lifetime which is given as $64s$. So, maximum increase possible for sequence number will be 2^{32} in $64s$ which will be $\frac{2^{32}}{64s} = 64M/s$ corresponding to a data rate of $64 \times 8 = 512Mbps$. This is not in the option.

Now the other possible meaning of the question is the rate at which the ISN of a packet can increase. This problem comes when a connection gets aborted and re-established (i.e., same IP and Port addresses at sender and receiver) very soon. In this case, receiver might get confused if it gets any sequence number which might have been used by the old connection. To, avoid this the new sequence number must be used only after all previous ones are dead. i.e., only after Maximum Life time of a packet which is $64s$. (Page 29, TCP Specification) This ensure that ISN can change only once in $64s$ giving the rate change as $1/64 = 0.015/s$ which is option A. (Even though, the ISN is changing only once, as per the question the new ISN is not old ISN +1 but old ISN + time passed in milliseconds)

Option A.

References



48 votes

-- Arjun Suresh (332k points)

2.29.2 Tcp: GATE CSE 2012 | Question: 22 top

<https://gateoverflow.in/1605>



✓ Answer is option C: TCP.

There are three primary TCP/IP protocols for E-Mail management:

- Post Office Protocol (POP)
- Simple Mail Transfer Protocol (SMTP)
- Internet Message Access Protocol (IMAP)

They all are Application Layer Protocols

Once a client connects to the E-mail Server, there may be 0(zero) or more SMTP transactions. If the client has no mail to send, then there are no SMTP transactions. Every e-mail message sent is an SMTP transfer.

SMTP is only used to send (push) messages to the server. POP and IMAP are used to receive messages as well as manage the mailbox contents(which includes tasks such as deleting, moving messages etc.).

44 votes

-- Amar Vashishth (25.2k points)

2.29.3 Tcp: GATE CSE 2015 Set 1 | Question: 19 top

<https://gateoverflow.in/8217>



✓ Option B

III. False. It is the size of the receiver's buffer that's never changed. RcvWindow is the part of the receiver's buffer that's changing all the time depending on the processing capability at the receiver's side and the network traffic.

http://web.eecs.utk.edu/~qi/teaching/ece453f06/hw/hw7_sol.htm

References



31 votes

-- GATERush (917 points)

2.29.4 Tcp: GATE CSE 2015 Set 2 | Question: 34 top

<https://gateoverflow.in/8154>



✓ In TCP when the **bandwidth delay product** increases beyond 64K receiver window scaling is needed.

The bandwidth delay product is the maximum amount of data on the network circuit at any time and is measured as $RTT * Bandwidth$. This is not the time for sending data rather just the time for sending data without acknowledgement.

So, here, we have bandwidth delay product = $(1048560 / 8) B * \alpha = 64 K$
 $\alpha = (64 K * 8) / 1048560 = 0.5 s = 500 \text{ milliseconds}$.

When window scaling happens, a 14 bit shift count is used in *TCP* header. So, the maximum possible window size gets increased from $2^{16}-1$ to $(2^{16}-1) * 2^{14}$ or from 65535 to $65535 * 2^{14}$

http://en.wikipedia.org/wiki/TCP_window_scale_option

References



87 votes

-- Arjun Suresh (332k points)

2.29.5 Tcp: GATE CSE 2015 Set 3 | Question: 22 [top](#)

<https://gateoverflow.in/8425>



- ✓ Answer is (A). Since, TCP has options for selective ACK and TCP uses byte streams that is every byte that is send using TCP is numbered.

http://repo.hackerzvoice.net/depot_madchat/ebooks/TCP-IP_Illustrated/tcp_tran.htm or [archive](#)

References



gateoverflow.in

classroom.gateover

38 votes

-- Tamojit Chatterjee (1.9k points)

2.29.6 Tcp: GATE CSE 2016 Set 2 | Question: 25 [top](#)

<https://gateoverflow.in/39572>



- ✓ Here,

C) Seems correct answer.

Say you type `www.google.com`

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gateoverflow.in

classroom.gateover

First you send DNS request to get IP address. Then you establish connection with IP of google using TCP. Finally you start talking in HTTP !

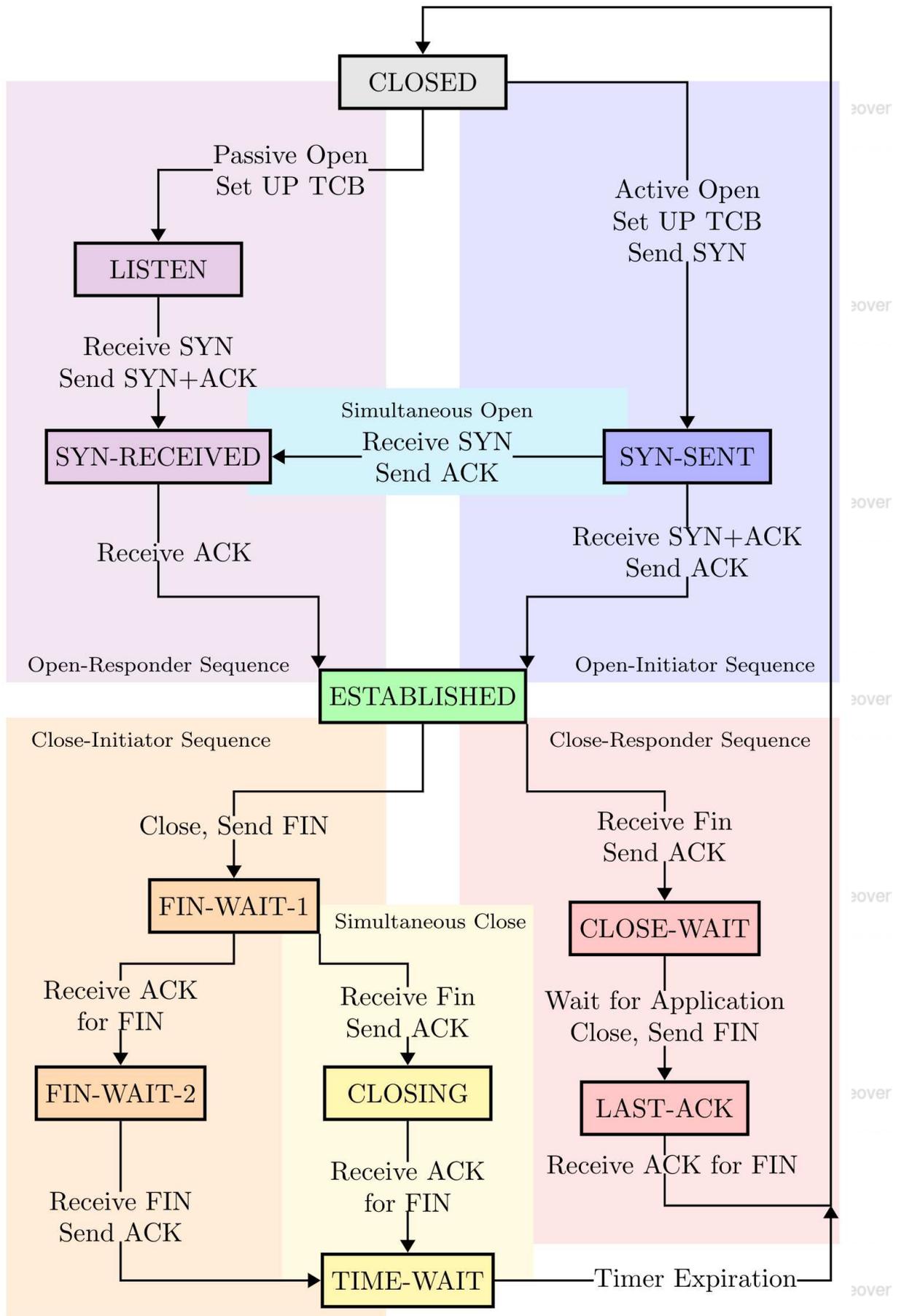
62 votes

-- Akash Kanase (36k points)

2.29.7 Tcp: GATE CSE 2017 Set 1 | Question: 14 [top](#)

<https://gateoverflow.in/118194>





Close Initiator Represents the agent which first sent the request for closing the connection when previously it was in established

state(Usually client).

Close Responder represents the agent which responds to FIN Segments(Usually the server).

Now, as we see in the diagram,

When the client sends the FIN segment to server,it moves to FIN-WAIT1 state where it waits for an Acknowledgement from the server for it's own FIN segment.

Now when the client receives ACK for its OWN FIN Segment, it moves to FIN-WAIT2. This state represents that the connection from client to server has been terminated but still the connection from server to client is open.(TCP supports full duplex connections).

Hence, answer is D.

Reference:

[1]http://tcpipguide.com/free/t_TCPOperationalOverviewandtheTCPFiniteStateMachineF-2.htm

References



39 votes

-- Ayush Upadhyaya (28 . 4k points)

2.29.8 Tcp: GATE CSE 2018 | Question: 25 top

<https://gateoverflow.in/204099>



✓ in another words qsn is asking to find Wrap-around time

$$T_{\text{minimum}} = T_{\text{wrap-around}} = \frac{2^{32} * 8}{10^9} = 34.35s$$

rounding to closest integer, we will get **34**

Note: Answer has been Modified in the Final Answer Key from GATE officials and now it is in Range from 34 to 35.

39 votes

-- NITISH JOSHI (24 . 4k points)

2.29.9 Tcp: GATE CSE 2020 | Question: 55 top

<https://gateoverflow.in/333176>



✓ In Case of AIMD :-

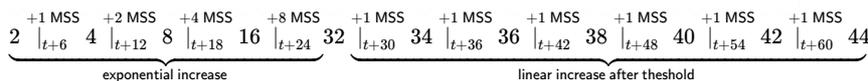
1. Start with Given MSS (Min Seq Size)
2. Increase the Window size in multiples of MSS till the threshold occurs
3. Once the threshold reached , increase the window size by 1 MSS till the timeout occurs
4. Once the timeout occurs , reduce threshold to half of current window size and again start from Given Start MSS.

$t = 0$

1 MSS = 2 KB

$W_{\text{threshold}} = 32 \text{ KB}$

| → denotes 1 RTT



∴ The size of the congestion window(in KB) at time $t + 60$ ms after all acknowledgements are processed is 44 KB

5 votes

-- Satbir Singh (21k points)

The state of congestion window changes as below

Note : As specified in question, there are no errors and timeouts

- At $t : 1 \text{ MSS}$

- At $t + 6$: 2 MSS
- At $t + 12$: 4 MSS
- At $t + 18$: 8 MSS
- At $t + 24$: 16 MSS

Now here since threshold value is reached, it is no longer in slow start phase and enters congestion avoidance phase

- At $t + 30$: 17 MSS
- At $t + 36$: 18 MSS
- At $t + 42$: 19 MSS
- At $t + 48$: 20 MSS
- At $t + 54$: 21 MSS
- At $t + 60$: 22 MSS

So at time $t + 60$, the congestion window size is 22 MSS i.e., 44 KB.

👍 14 votes

-- NabilSayyad (761 points)

2.29.10 Tcp: GATE CSE 2021 Set 1 | Question: 44 top 9

<https://gateoverflow.in/357407>



Option A is correct, because client doesn't have a keepalive timer, and the server after a reboot forgets any connection with the client existed.

As for option C and D, option D is wrong because there is no reason for a FIN segment to be sent because there is no established connection which can be closed **according to the recently rebooted server**.

As for option C, scroll down to read the paragraph from page 35*** of the documentation, which proves that it is in fact correct.

Now, for option B, during the exam i reasoned that there is a distinction between a server machine being rebooted, and a tcp application/process being restarted.

For instance, whenever your computer crashes and reboots when you were browsing on google chrome (this was the case atleast a few years ago), did your computer automatically also restart the google chrome application? Obviously not.

There are some processes which the computer automatically starts on boot, **but those are the exceptions and not the norm**.

A client or server won't simply restart its previous processes after a crash and reboot, **unless it has been configured** to do so, and nowhere in the question do i see that the server was a dedicated server running only the said tcp application.

The question asks what **behaviour** is possible on reboot. When such wording is used, it is natural to assume that it means what happens after the reboot **without any external interference**, human or otherwise. Because if we don't assume this to be true, then a whole lot of things are possible after a system restarts.

Here is some supporting text from the standard tcp documentation which you can access following this: Wikipedia → Transmission Control Protocol → RFC Documents → [STD 7](#) - Transmission Control Protocol, Protocol specification (<https://tools.ietf.org/html/std7>) → Page 32 → Half-Open Connections and Other Anomalies.

An established connection is said to be "half-open" if one of the TCPs has closed or aborted the connection at its end without the knowledge of the other, or if the two ends of the connection have become desynchronized owing to a crash that resulted in loss of memory. Such connections will automatically become reset if an attempt is made to send data in either direction. However, half-open connections are expected to be unusual, and the recovery procedure is mildly involved.

If at site A the connection no longer exists, then an attempt by the user at site B to send any data on it will result in the site B TCP receiving a reset control message. Such a message indicates to the site B TCP that something is wrong, and it is expected to abort the connection.

Assume that two user processes A and B are communicating with one another when a crash occurs causing loss of memory to A's TCP. **Depending on the operating system** supporting A's TCP, it is **likely** that some error recovery mechanism exists. **When the TCP is up again**, A is **likely** to start again from the beginning or from a recovery point. As a result, A **will probably try** to OPEN the connection again or try to SEND on the connection it believes open. In the latter case, it receives the error message "connection not open" from the local (A's) TCP. In an attempt to establish the connection, A's TCP will send a segment containing SYN. This scenario leads to the example shown in figure 10.

The highlighted words indicate that it **isn't always necessary** that the tcp process will restart after a crash, and that it is

dependent upon the operating system.

Given that we don't know what the TCP process is exactly, it **could as well be an unimportant process** on a **non well-known port**, which was used for a private connection between the client and the server, **which has no specific reason to restart** after the server reboots.

And until and unless the process restarts, it **won't start listening on its configured port number**.

***Also on Page 35 →

Reset Generation

As a general rule, reset (RST) must be sent whenever a segment arrives which apparently is not intended for the current connection. A reset must not be sent if it is not clear that this is the case.

References



👍 4 votes

-- Rishabh Gupta (511 points)

2.29.11 Top: GATE CSE 2021 Set 1 | Question: 45 top ⤴

<https://gateoverflow.in/357406>



✓ A is correct as you can follow the process of IPv4 fragmentation and you will get $620B$ fragments as described in the statement.

C is correct as fragmentation happened at the router and the sender has no way of knowing what kind of fragmentation occurred, so it will resend the whole TCP segment.

For B to be true, the original sender must retransmit the packet data in a datagram with the *same* IPv4 ID field as before, i.e. $0X1234$. Take a look at [RFC 1122](#) to see what they say about retransmitting with the same ID field (text below).

First of all, it says that retaining the ID field is optional. Secondly, it says that due to certain constraints, this is not practical, and therefore not believed to be useful (so it does not really happen in practice).

B's statement implies that the router will definitely resend a fragment with $0X1234$ ID, which can only happen if the sender resends the whole segment with the same ID number, but there is no such guarantee. Therefore B is **false**.

When sending an identical copy of an earlier datagram, a host **MAY** optionally retain the same Identification field in the copy.

Some Internet protocol experts have maintained that when a host sends an identical copy of an earlier datagram, the new copy should contain the same Identification value as the original. There are two suggested advantages: (1) if the datagrams are fragmented and some of the fragments are lost, the receiver may be able to reconstruct a complete datagram from fragments of the original and the copies; (2) a congested gateway might use the IP Identification field (and Fragment Offset) to discard duplicate datagrams from the queue.

However, the observed patterns of datagram loss in the Internet do not favor the probability of retransmitted fragments filling reassembly gaps, while other mechanisms (e.g., TCP retransmission) tend to prevent retransmission of an identical datagram [IP:9]. Therefore, **we believe that retransmitting the same Identification field is not useful**.

References



7 votes

-- Prithish C (2k points)

2.29.12 Top: GATE CSE 2021 Set 2 | Question: 7 top

https://gateoverflow.in/357533



- ✓ Host P sends the first SYN packet with SEQ number = X , SYN flag = 1 and ACK flag = 0 as it's a connection request.

Host Q will reply back with a SYN packet and acknowledging the arrival of P 's SYN packet.

Host Q will send a packet with

SYN flag = 1,

SEQ number = Y , to synchronize and establish the connection,

and

ACK flag = 1 to acknowledge the P 's SYN packet, with

ACK number = $X+1$ because ACK number denotes the sequence number of next expecting Byte.

Then P will reply back with an ACK packet to complete the three-way handshake. (not asked here)

FIN flag is used to terminate the connection, and will not be used here, **FIN flag = 0.**

Hence **C is correct.**

2 votes

-- Nikhil Dhama (2.5k points)

2.29.13 Top: GATE IT 2004 | Question: 23 top

https://gateoverflow.in/3664



- ✓ Option B: "Sequence numbers allow receivers to discard duplicate packets and properly sequence reordered packets."
- Option C: "When congestion is detected, the transmitter decreases the transmission rate by a multiplicative factor; for example, cut the congestion window in half after loss." (Additive Increase/multiplicative decrease)
- Option D: "Acknowledgments allow senders to determine when to retransmit lost packets."

So, **(A)** is answer.

http://en.wikipedia.org/wiki/Transmission_Control_Protocol#Error_detection

http://en.wikipedia.org/wiki/Additive_increase/multiplicative_decrease

References



27 votes

-- Arjun Suresh (332k points)

2.29.14 Top: GATE IT 2004 | Question: 28 top

https://gateoverflow.in/3669



- ✓ a) it should be byte

http://www.industrialnethernet.com/courses/202_2.htm

References

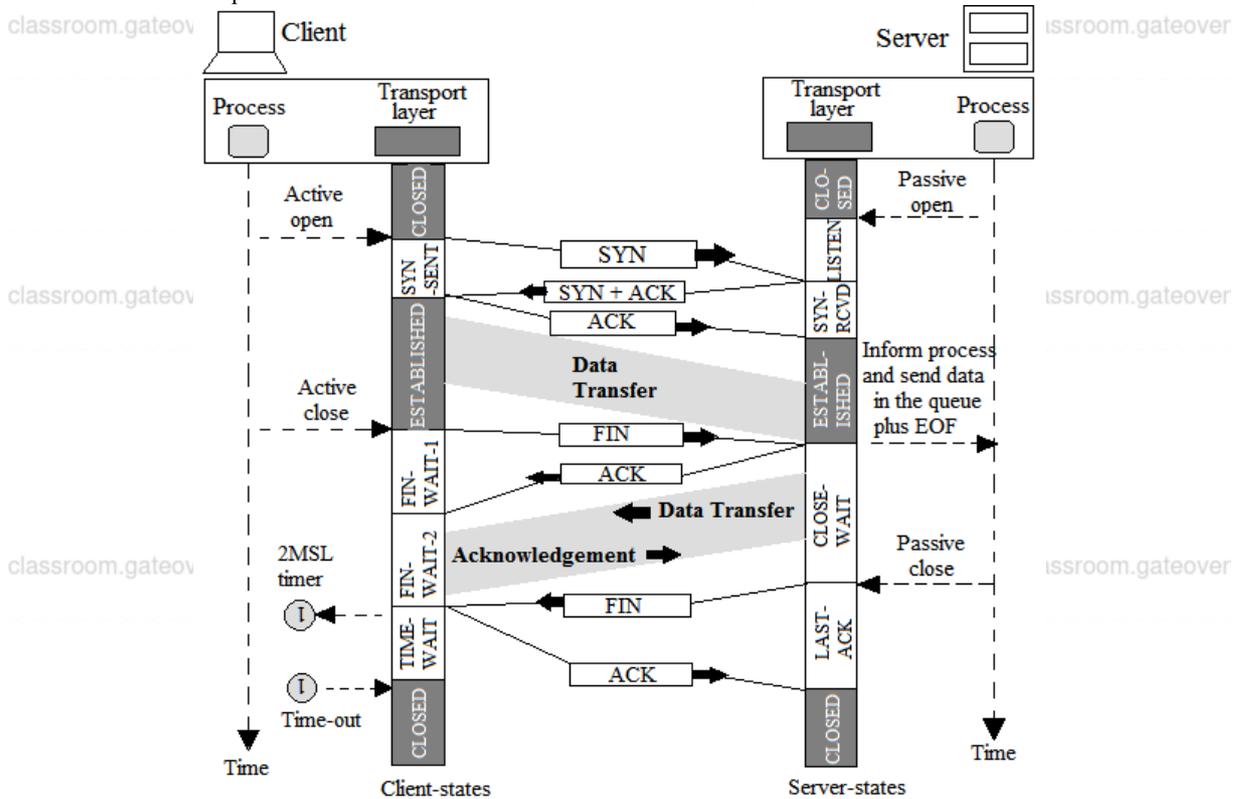


28 votes

-- Parul Agarwal (661 points)



- i. (i) TCP connection established in 3 phase between SYN send and SYN received (SYN, SYN + ACK, ACK) . After this connection establishment, data transfer takes place. Now, FIN flag is called to close the connection. FIN flag can close the connection after getting the ACK from the receiver. If ACK is not received, a timer is set which wait for the time out. So, there is no relationship between TCP connection establishment and Timeout of RTT.



- ii. This is Jacobson's algorithm (Thanks @Anirudh)

$$ERTT = p \times IRRT + (1 - p) \times NRTT$$

p is scaling factor
 IRRT initial RTT
 NRTT is new RTT
[Link here](#)

- iii. Actually timeout value is more than twice the propagation delay from sender to receiver. Because after connection establishment and data transfer complete, then only timeout occurs. So, if we start timer at the beginning of transaction, Time Out occurs after RTT completes and after final ACK comes. So, Time Out time must be more than RTT.

So, only (ii) is TRUE. Answer (B).

References



34 votes

-- srestha (85.2k points)



Answer is D.

Because it is said that the connection is TCP and the sender has sent first two segments which is clear from the text "The sequence numbers of the first and second segments are 230 and 290 respectively." That means there must be 3 Way handshaking

that has been done before the connection has been established and when sender has sent SYN packet then receiver must have ACKED him with next packet. In response to it receiver only received only 1 packet so he will come to know that 1st packet has been lost and again he will send ACK for lost packet

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 36 votes

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 -- Aditi Tiwari (879 points)



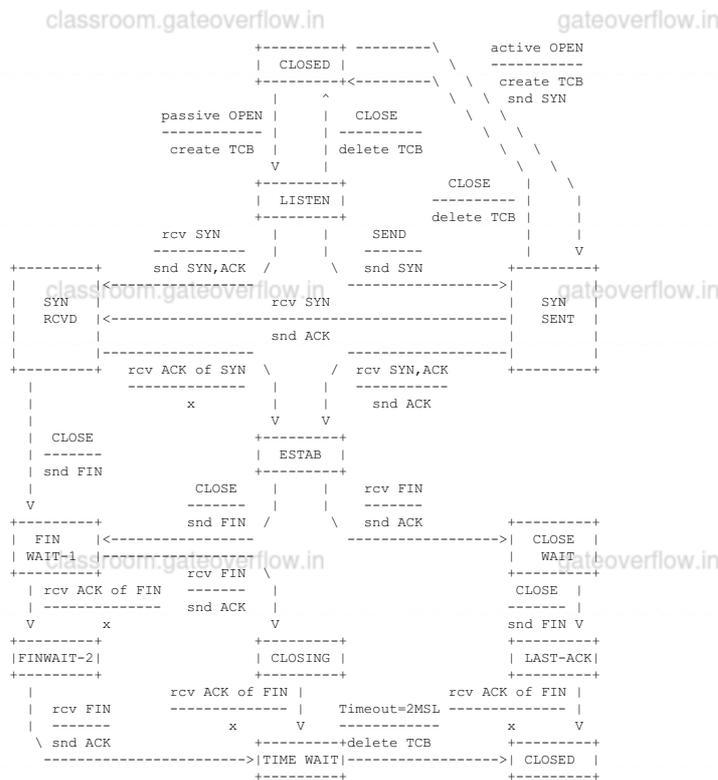
- ✓ (S1) Loss of SYN + ACK from the server will not establish a connection => True.
- (S2) Loss of ACK from the client cannot establish the connection => No this is not true. Detail reasoning: <http://stackoverflow.com/questions/16259774/what-if-a-tcp-handshake-segment-is-lost> If after ACK client immediately sends data then everything goes on without worry. (Though if along with ACK, first data packet is dropped, connection is reset)
- (S3) The server moves LISTEN → SYN_RCVD → SYN_SENT → ESTABLISHED in the state machine on no packet loss => False
- (S4) The server moves LISTEN → SYN_RCVD → ESTABLISHED in the state machine on no packet loss. => True

Answer is (B) => S1 and S4 are true.

Reference for S4 => <https://www.rfc-editor.org/rfc/rfc793.txt>

September 1981

Transmission Control Protocol
 Functional Specification



TCP Connection State Diagram
 Figure 6.

References



42 votes

-- Akash Kanase (36k points)



A computer on a 10 Mbps network is regulated by a token bucket. The token bucket is filled at a rate of 2 Mbps. It is initially filled to capacity with 16 Megabits. What is the maximum duration for which the computer can transmit at the full 10 Mbps?

- tests.gatecse.in goclasses.in tests.gatecse.in
- A. 1.6 seconds
 - B. 2 seconds
 - C. 5 seconds
 - D. 8 seconds

gate2008-cse

computer-networks

token-bucket

Answer



For a host machine that uses the token bucket algorithm for congestion control, the token bucket has a capacity of 1 megabyte and the maximum output rate is 20 megabytes per second. Tokens arrive at a rate to sustain output at a rate of 10 megabytes per second. The token bucket is currently full and the machine needs to send 12 megabytes of data. The minimum time required to transmit the data is _____ seconds.

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computer-networks

token-bucket

normal

numerical-answers

Answer

Answers: Token Bucket



- ✓ New tokens are added at the rate of r bits/sec which is 2 Mbps in the given question.

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Capacity of the token bucket (b) = 16 Mbits

Maximum possible transmission rate (M) = 10 Mbps

So, the maximum burst time = $b/(M-r) = 16/(10-2) = 2$ secondsHere is the [animation](#) for token bucket hope this will help us to understand the concept.

Correct Answer: B

References



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45 votes

-- Vikrant Singh (11.2k points)



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Initially token bucket is full.

Rate at which it is emptying is (20 – 10) MBps.

Time taken to empty token bucket of 1 MB is $\frac{1}{10}$ i.e 0.1 sec.Data send in this time is $0.1 * 20 = 2$ MB (rate at which bucket is emptying is different from rate at which data is send).Data left to send is $12 - 2 = 10$ MB.

Now bucket is empty and rate of token arriving is less than that of going out so effective data speed will be 10MBps.

Time to send remaining 10MB will be 1 sec. So total time is $1 + 0.1 = 1.1$ sec

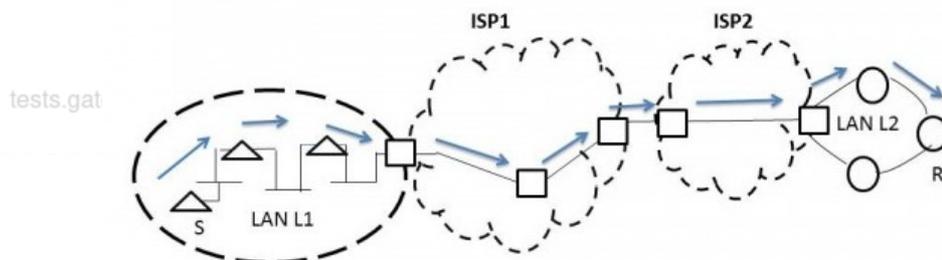
118 votes

-- Vaibhav Singh (445 points)

2.31.1 Token Ring: GATE CSE 2014 Set 2 | Question: 25 top

<https://gateoverflow.in/1983>

In the diagram shown below, $L1$ is an Ethernet LAN and $L2$ is a Token-Ring LAN. An IP packet originates from sender S and traverses to R , as shown. The links within each ISP and across the two ISPs, are all point-to-point optical links. The initial value of the TTL field is 32. The maximum possible value of the TTL field when R receives the datagram is _____.



gate2014-cse-set2 computer-networks numerical-answers lan-technologies ethernet token-ring normal

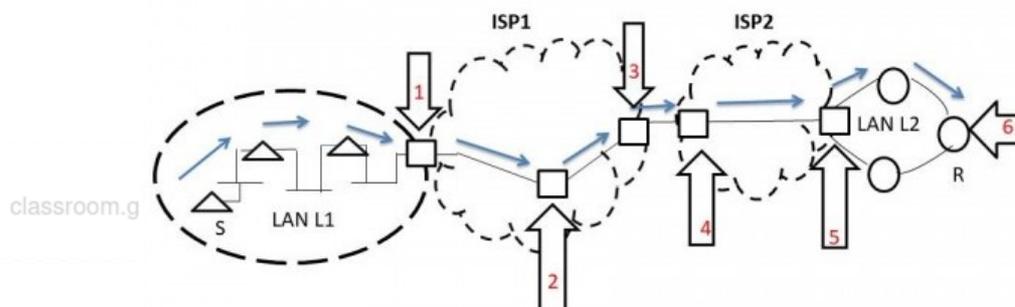
Answer

Answers: Token Ring

2.31.1 Token Ring: GATE CSE 2014 Set 2 | Question: 25 top

<https://gateoverflow.in/1983>

- ✓ Each time a packet visits network layer it decrements its TTL field. Source initializes it and others decrement it. Inside LAN it never goes to network layer, it is forwarded from data link layer itself. In routers it goes up to network layer to make a routing decision, and the router decrements it because the packet has visited the network layer, and at the receiver too, the packet has visited the network layer and network layer will do its job and decrement the TTL value.



There are 5 routers, So Network Layer will be visited 5 times and 1 time on the destination

So, TTL = 26

PS:) A receiver decrements TTL value and then checks whether it is 0 (or) not. So, 26 is the answer (not 27)

103 votes

-- Kalpish Singhal (1.6k points)

2.32.1 Udp: GATE CSE 2005 | Question: 23 top

<https://gateoverflow.in/1359>

Packets of the same session may be routed through different paths in:

- TCP, but not UDP
- TCP and UDP
- UDP, but not TCP
- Neither TCP nor UDP

gate2005-cse computer-networks tcp udp easy

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Answer 

2.32.2 Udp: GATE CSE 2013 | Question: 12 [top](#) 

<https://gateoverflow.in/1421>



The transport layer protocols used for real time multimedia, file transfer, DNS and email, respectively are

- A. TCP, UDP, UDP and TCP
- B. UDP, TCP, TCP and UDP
- C. UDP, TCP, UDP and TCP
- D. TCP, UDP, TCP and UDP

gate2013-cse computer-networks tcp udp easy

Answer 

2.32.3 Udp: GATE CSE 2017 Set 2 | Question: 18 [top](#) 

<https://gateoverflow.in/118209>



Consider socket API on a Linux machine that supports connected UDP sockets. A connected UDP socket is a UDP socket on which *connect* function has already been called. Which of the following statements is/are CORRECT?

- I. A connected UDP socket can be used to communicate with multiple peers simultaneously.
- II. A process can successfully call *connect* function again for an already connected UDP socket.

- A. I only
- B. II only
- C. Both I and II
- D. Neither I nor II

gate2017-cse-set2 computer-networks udp

Answer 

2.32.4 Udp: GATE IT 2006 | Question: 69 [top](#) 

<https://gateoverflow.in/3613>



A program on machine *X* attempts to open a *UDP* connection to port 5376 on a machine *Y*, and a *TCP* connection to port 8632 on machine *Z*. However, there are no applications listening at the corresponding ports on *Y* and *Z*. An *ICMP* Port Unreachable error will be generated by

- A. *Y* but not *Z*
- B. *Z* but not *Y*
- C. Neither *Y* nor *Z*
- D. Both *Y* and *Z*

gate2006-it computer-networks tcp udp normal

Answer 

Answers: Udp

2.32.1 Udp: GATE CSE 2005 | Question: 23 [top](#) 

<https://gateoverflow.in/1359>



- ✓ b) TCP and UDP.

Routing happens in Network layer and hence has no dependency with the the transport layer protocols TCP and UDP. The transport layer protocol- whether TCP or UDP is hidden to the router and the routing path is determined based on the the network configuration at the time and hence can change even during a session.

Reference: <http://stackoverflow.com/questions/15601389/if-tcp-is-connection-oriented-why-do-packets-follow-different-paths>

References



65 votes

-- Arjun Suresh (332k points)

2.32.2 Udp: GATE CSE 2013 | Question: 12 [top](#)

<https://gateoverflow.in/1421>



- ✓ **Real Time Multimedia:** Data packets should be delivered faster. Also it can be unreliable. Therefore UDP.
File Transfer: For example downloading a file. It should be secure and reliable. Therefore TCP.
DNS: uses both UDP and TCP for its transport. But to achieve efficiency DNS uses UDP. To start a TCP connection a minimum of three packets are required (SYN out, SYN+ACK back, ACK out). UDP uses a simple transmission model with a minimum of protocol mechanism. UDP has no handshaking dialogues.
Email: uses SMTP protocol which uses TCP protocol.
- Therefore, **C** is the answer.

43 votes

-- Pyuri sahu (1.5k points)

2.32.3 Udp: GATE CSE 2017 Set 2 | Question: 18 [top](#)

<https://gateoverflow.in/118209>



- ✓ **Calling connect Multiple Times for a UDP Socket**

A process with a connected UDP socket can call `connect` again for that socket for one of two reasons:

1. To specify a new IP address and port
2. To disconnect the socket

The first case specifying a new peer for a connected UDP socket differs from the use of `connect` with a TCP socket. `Connect` can be called only one time for a TCP socket. To disconnect a UDP socket, we call `Connect` but set the `family` member of the socket address structure to `AT_UNSPEC`.

Also, a UDP client or server can call `Connect` only if that process uses the UDP socket to communicate with **exactly one** peer.

http://www.masterraghu.com/subjects/np/introduction/unix_network_programming_v1.3/ch08lev1sec11.html

So, option **B** should be answer.

For 1st part if "NOT connected" then it'll be true <http://stackoverflow.com/questions/3329641/how-do-multiple-clients-connect-simultaneously-to-one-port-say-80-on-a-server>

References



34 votes

-- 2018 (5.5k points)

2.32.4 Udp: GATE IT 2006 | Question: 69 [top](#)

<https://gateoverflow.in/3613>



- ✓ Answer should be **(D)**,

An ICMP packet with a message type 3 (Destination Unreachable) and a message code 3 (Port Unreachable) lets you know that the machine you tried to reach is not listening on this port. When you `nmap` a machine on a port it's not listening on, it sends back an ICMP packet like this to let you know that it's not listening on that port (if the port is not firewalled. If it is, then what happens depends on the config of your firewall).

ref @ <http://www.linuxchix.org/content/courses/security/icmp>

http://www.tcpipguide.com/free/t_ICMPv4DestinationUnreachableMessages-3.htm

http://en.wikipedia.org/wiki/Internet_Control_Message_Protocol#Destination_unreachable

Port Unreachable

Unlike the Network Unreachable and Host Unreachable messages which come from routers, the **Port Unreachable** message comes from a host. The primary implication for troubleshooting is that the frame was successfully routed across the communications infrastructure, the last router ARP'd for the host, got the response, and sent the frame. Furthermore, the intended destination host was on-line and willing to accept the frame into its communications buffer. The frame was then processed by, say, TCP or, perhaps UDP, RIP, OSPF, or some other protocol. The protocol (TCP or UDP) tried to send the data up to the destination port number (TCP or UDP port) and the port process didn't exist. The protocol handler then

reports **Destination Unreachable - Port Unreachable**.

ref @ http://www.wildpackets.com/resources/compendium/tcp_ip/unreachable

- Port Unreachable - generated if the designated transport protocol (e.g., UDP) is unable to demultiplex the datagram in the transport layer of the final destination but has no protocol mechanism to inform the sender

<http://support.microsoft.com/en-us/kb/325122>

Port unreachable is a code 3 within type 3 @ <http://tools.ietf.org/html/rfc792>

<http://www.iana.org/assignments/icmp-parameters/icmp-parameters.xhtml>

<http://www.faqs.org/rfcs/rfc792.html>

References



28 votes

-- Mithlesh Upadhyay (4.3k points)

2.33

Wifi (1) top

2.33.1 Wifi: GATE CSE 2016 Set 2 | Question: 54 top

<https://gateoverflow.in/39593>



For the IEEE 802.11 MAC protocol for wireless communication, which of the following statements is/are **TRUE**?

- At least three non-overlapping channels are available for transmissions.
- The RTS-CTS mechanism is used for collision detection.
- Unicast frames are ACKed.

- All I, II, and III
- I and III only
- II and III only
- II only

gate2016-cse-set2 computer-networks wifi normal

goclasses.in

tests.gatecse.in

Answer

Answers: Wifi

2.33.1 Wifi: GATE CSE 2016 Set 2 | Question: 54 top

<https://gateoverflow.in/39593>



✓ 802.11 MAC = Wifi

- This is true, maximum 3 overlapping channels are possible in Wifi !
- This is false. Collision detection is not really possible in Wireless, because signal strength of sending & receiving signal need not be same ! So Wifi uses **collision Avoidance** instead ! In this RTS-CTS are used to announce to all nodes, that for which node wireless channel is reserved for communication. So this is collision avoidance, not detection
- This is true. Every frame in Wifi is acked, because Wifi station do not use collision detection, in Ethernet we use collision detection, in which it is possible for us to listen channel for collision & use exponential back off in case of collision detection. As in case of wifi, due to more error rate and not using collision detection strategy , we instead use ACK frame, in case of not getting ACK Host will retransmit after Random back off period

Answer is **(B)**.

Source: Kurose & Ross Top down approach to internet

Answer Keys

2.1.1	A	2.1.2	C	2.1.3	C	2.1.4	C	2.1.5	B
2.1.6	6	2.1.7	B	2.1.8	C	2.1.9	D	2.1.10	C
2.2.1	A	2.2.2	A	2.3.1	A	2.3.2	B	2.3.3	B
2.4.1	D	2.4.2	C	2.4.3	1100 : 1300	2.4.4	0.4404	2.4.5	C
2.4.6	50	2.4.7	B	2.5.1	B	2.5.2	C	2.5.3	C
2.5.4	A	2.6.1	D	2.6.2	200	2.6.3	C	2.6.4	A
2.6.5	B	2.7.1	C	2.7.2	B	2.7.3	A	2.7.4	C
2.7.5	B;C	2.7.6	B	2.7.7	A	2.8.1	3 : 4	2.8.2	A
2.8.3	C	2.8.4	B	2.8.5	A	2.8.6	B	2.8.7	C
2.8.8	N/A	2.9.1	B	2.9.2	B	2.9.3	D	2.9.4	C
2.10.1	N/A	2.10.2	A	2.11.1	A	2.12.1	D	2.12.2	D
2.12.3	B	2.12.4	C	2.12.5	C	2.12.6	256	2.12.7	9
2.12.8	144	2.13.1	C	2.13.2	D	2.13.3	D	2.13.4	A
2.13.5	B	2.13.6	C	2.13.7	13	2.13.8	D	2.14.1	D
2.14.2	A	2.14.3	3	2.14.4	D	2.14.5	D	2.14.6	B
2.15.1	D	2.16.1	D	2.16.2	12	2.16.3	B	2.16.4	C
2.17.1	N/A	2.17.2	D	2.17.3	D	2.17.4	C	2.17.5	A
2.18.1	D	2.18.2	A	2.18.3	B	2.18.4	C	2.18.5	B
2.18.6	C	2.19.1	D	2.19.2	C	2.19.3	A	2.19.4	C
2.19.5	C	2.19.6	50 : 52	2.19.7	C	2.19.8	D	2.19.9	B
2.20.1	D	2.20.2	D	2.20.3	1575	2.20.4	B	2.21.1	130 : 140
2.22.1	B	2.23.1	B	2.23.2	A	2.23.3	1	2.23.4	C
2.23.5	D	2.23.6	C	2.23.7	A	2.23.8	C	2.23.9	D
2.24.1	C	2.25.1	B	2.25.2	B	2.25.3	B	2.25.4	C
2.25.5	C	2.25.6	D	2.25.7	C	2.25.8	5	2.25.9	8
2.25.10	4	2.25.11	C	2.25.12	B	2.25.13	B	2.25.14	A
2.25.15	A	2.26.1	D	2.26.2	C	2.26.3	C	2.26.4	B
2.27.1	320	2.27.2	2500	2.27.3	86.5 : 89.5	2.27.4	D	2.27.5	B
2.28.1	D	2.28.2	A	2.28.3	D	2.28.4	C	2.28.5	C
2.28.6	C	2.28.7	D	2.28.8	A	2.28.9	A	2.28.10	158
2.28.11	C	2.28.12	B	2.28.13	C	2.28.14	D	2.28.15	C
2.28.16	D	2.28.17	C	2.28.18	B	2.29.1	A	2.29.2	C
2.29.3	B	2.29.4	C	2.29.5	A	2.29.6	C	2.29.7	D

2.29.8	34 : 35
2.29.13	A
2.30.1	B
2.32.3	B

2.29.9	44
2.29.14	A
2.30.2	1.10:1.19
2.32.4	D

2.29.10	A;B;C
2.29.15	B
2.31.1	26
2.33.1	B

2.29.11	A;C
2.29.16	D
2.32.1	B

2.29.12	C
2.29.17	B
2.32.2	C



ER-model. Relational model: Relational algebra, Tuple calculus, SQL. Integrity constraints, Normal forms. File organization, Indexing (e.g., B and B+ trees). Transactions and concurrency control.

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	2	1	2	2	2	2	2	3	2	1	2	3
2 Marks Count	3	3	3	3	2	3	3	1	2	1	2.5	3
Total Marks	8	7	8	8	6	8	8	5	6	6	7.1	8

3.1

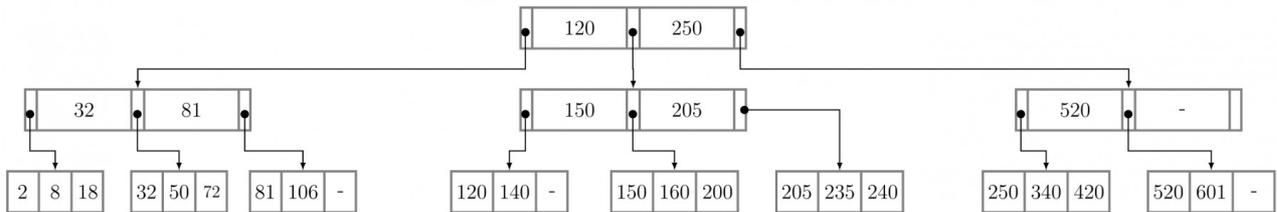
B Tree (28) top

3.1.1 B Tree: GATE CSE 1989 | Question: 12a top

<https://gateoverflow.in/91199>



The below figure shows a B^+ tree where only key values are indicated in the records. Each block can hold upto three records. A record with a key value 34 is inserted into the B^+ tree. Obtain the modified B^+ tree after insertion.



descriptive gate1989 databases b-tree

Answer

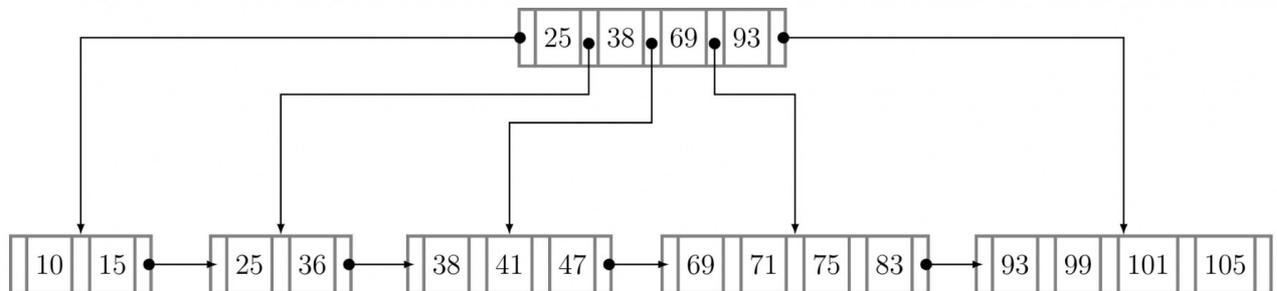
3.1.2 B Tree: GATE CSE 1994 | Question: 14a top

<https://gateoverflow.in/2510>



Consider B^+ - tree of order d shown in figure. (A B^+ - tree of order d contains between d and $2d$ keys in each node)

Draw the resulting B^+ - tree after 100 is inserted in the figure below.



gate1994 databases b-tree normal descriptive

Answer

3.1.3 B Tree: GATE CSE 1994 | Question: 14b top

<https://gateoverflow.in/360163>



For a B^+ - tree of order d with n leaf nodes, the number of nodes accessed during a search is $O(_)$.

gate1994 databases b-tree normal descriptive

Answer

3.1.4 B Tree: GATE CSE 1997 | Question: 19 top

<https://gateoverflow.in/2279>



A B^+ - tree of order d is a tree in which each internal node has between d and $2d$ key values. An internal node with M key values has $M + 1$ children. The root (if it is an internal node) has between 1 and $2d$ key values. The distance of a node from the root is the length of the path from the root to the node. All leaves are at the same distance from the root. The height of the tree is the distance of a leaf from the root.

- A. What is the total number of key values in the internal nodes of a B^+ -tree with l leaves ($l \geq 2$)?
- B. What is the maximum number of internal nodes in a B^+ - tree of order 4 with 52 leaves?
- C. What is the minimum number of leaves in a B^+ -tree of order d and height $h(h \geq 1)$?

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gate1997 databases b-tree normal descriptive

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tests.gatecse.in

Answer 

3.1.5 B Tree: GATE CSE 1999 | Question: 1.25 [top](#)

<https://gateoverflow.in/1478>



Which of the following is correct?

- A. B-trees are for storing data on disk and B^+ trees are for main memory.
- B. Range queries are faster on B^+ trees.
- C. B-trees are for primary indexes and B^+ trees are for secondary indexes.
- D. The height of a B^+ tree is independent of the number of records.

tests.gatecse.in
gate1999 databases b-tree normal

goclasses.in

tests.gatecse.in

Answer 

3.1.6 B Tree: GATE CSE 1999 | Question: 21 [top](#)

<https://gateoverflow.in/1520>



Consider a B-tree with degree m , that is, the number of children, c , of any internal node (except the root) is such that $m \leq c \leq 2m - 1$. Derive the maximum and minimum number of records in the leaf nodes for such a B-tree with height $h, h \geq 1$. (Assume that the root of a tree is at height 0).

gate1999 databases b-tree normal descriptive

Answer 

3.1.7 B Tree: GATE CSE 2000 | Question: 1.22, UGCNET-June2012-II: 11 [top](#)

<https://gateoverflow.in/646>



B^+ -trees are preferred to binary trees in databases because

- A. Disk capacities are greater than memory capacities
- B. Disk access is much slower than memory access
- C. Disk data transfer rates are much less than memory data transfer rates
- D. Disks are more reliable than memory

gate2000-cse databases b-tree normal ugcnetjune2012ii

Answer 

3.1.8 B Tree: GATE CSE 2000 | Question: 21 [top](#)

<https://gateoverflow.in/692>



(a) Suppose you are given an empty B^+ tree where each node (leaf and internal) can store up to 5 key values. Suppose values 1, 2, ..., 10 are inserted, in order, into the tree. Show the tree pictorially

- i. after 6 insertions, and
- ii. after all 10 insertions

Do NOT show intermediate stages.

(b) Suppose instead of splitting a node when it is full, we try to move a value to the left sibling. If there is no left sibling, or the left sibling is full, we split the node. Show the tree after values 1, 2, ..., 9 have been inserted. Assume, as in (a) that each node can hold up to 5 keys.

(c) In general, suppose a B^+ tree node can hold a maximum of m keys, and you insert a long sequence of keys in increasing order. Then what approximately is the average number of keys in each leaf level node.

- i. in the normal case, and
- ii. with the insertion as in (b).

Answer

3.1.9 B Tree: GATE CSE 2001 | Question: 22

https://gateoverflow.in/763



We wish to construct a B^+ tree with fan-out (the number of pointers per node) equal to 3 for the following set of key values:

80, 50, 10, 70, 30, 100, 90

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Assume that the tree is initially empty and the values are added in the order given.

- Show the tree after insertion of 10, after insertion of 30, and after insertion of 90. Intermediate trees need not be shown.
- The key values 30 and 10 are now deleted from the tree in that order show the tree after each deletion.

Answer

3.1.10 B Tree: GATE CSE 2002 | Question: 17

https://gateoverflow.in/870



- The following table refers to search items for a key in B -trees and B^+ trees.

B-tree		B ⁺ -tree	
Successful search	Unsuccessful search	Successful search	Unsuccessful search
X_1	X_2	X_3	X_4

A successful search means that the key exists in the database and unsuccessful means that it is not present in the database. Each of the entries X_1, X_2, X_3 and X_4 can have a value of either Constant or Variable. Constant means that the search time is the same, independent of the specific key value, where variable means that it is dependent on the specific key value chosen for the search.

Give the correct values for the entries X_1, X_2, X_3 and X_4 (for example $X_1 = \text{Constant}$, $X_2 = \text{Constant}$, $X_3 = \text{Constant}$, $X_4 = \text{Constant}$)

- Relation $R(A, B)$ has the following view defined on it:

```
CREATE VIEW V AS
(SELECT R1.A, R2.B
FROM R AS R1, R AS R2
WHERE R1.B=R2.A)
```

- The current contents of relation R are shown below. What are the contents of the view V ?

A	B
1	2
2	3
2	4
4	5
6	7
6	8
9	10

- The tuples (2, 11) and (11, 6) are now inserted into R . What are the *additional* tuples that are inserted in V ?

Answer

3.1.11 B Tree: GATE CSE 2002 | Question: 2.23, UGCNET-June2012-II: 26

https://gateoverflow.in/853



A B^+ - tree index is to be built on the *Name* attribute of the relation *STUDENT*. Assume that all the student names are of length 8 bytes, disk blocks are of size 512 bytes, and index pointers are of size 4 bytes. Given the scenario, what would be the best choice of the degree (i.e. number of pointers per node) of the B^+ - tree?

- A. 16
- B. 42
- C. 43
- D. 44

gate2002-cse databases b-tree normal ugcnetjune2012ii

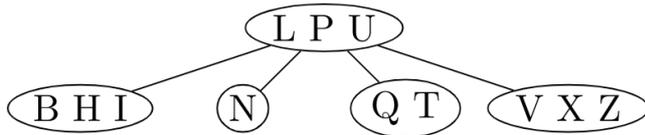
Answer

3.1.12 B Tree: GATE CSE 2003 | Question: 65 top

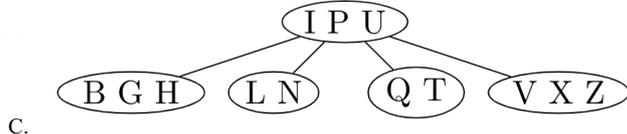
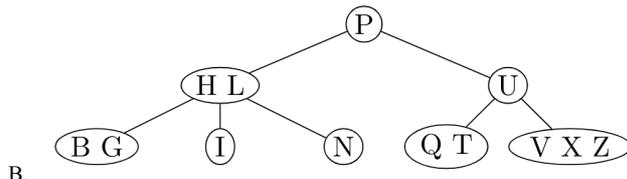
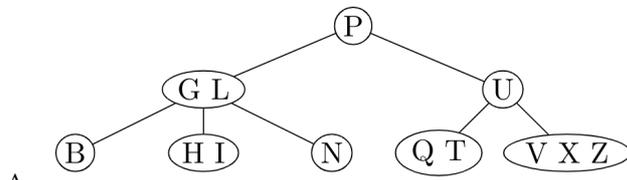
https://gateoverflow.in/952



Consider the following 2 – 3 – 4 tree (i.e., B-tree with a minimum degree of two) in which each data item is a letter. The usual alphabetical ordering of letters is used in constructing the tree.



What is the result of inserting *G* in the above tree?



D. None of the above

gate2003-cse databases b-tree normal

Answer

3.1.13 B Tree: GATE CSE 2004 | Question: 52 top

https://gateoverflow.in/1048



The order of an internal node in a *B+* tree index is the maximum number of children it can have. Suppose that a child pointer takes 6 bytes, the search field value takes 14 bytes, and the block size is 512 bytes. What is the order of the internal node?

- A. 24
- B. 25
- C. 26
- D. 27

gate2004-cse databases b-tree normal

Answer

3.1.14 B Tree: GATE CSE 2005 | Question: 28 top

https://gateoverflow.in/1364



Which of the following is a key factor for preferring *B+*-trees to binary search trees for indexing database relations?

- A. Database relations have a large number of records

- B. Database relations are sorted on the primary key
- C. B^+ -trees require less memory than binary search trees
- D. Data transfer from disks is in blocks

gate2005-cse databases b-tree normal

Answer

3.1.15 B Tree: GATE CSE 2007 | Question: 63, ISRO2016-59 top

<https://gateoverflow.in/1261>



The order of a leaf node in a B^+ - tree is the maximum number of (value, data record pointer) pairs it can hold. Given that the block size is $1K$ bytes, data record pointer is 7 bytes long, the value field is 9 bytes long and a block pointer is 6 bytes long, what is the order of the leaf node?

- A. 63
- B. 64
- C. 67
- D. 68

gate2007-cse databases b-tree normal isro2016

Answer

3.1.16 B Tree: GATE CSE 2008 | Question: 41 top

<https://gateoverflow.in/453>



A B-tree of order 4 is built from scratch by 10 successive insertions. What is the maximum number of node splitting operations that may take place?

- A. 3
- B. 4
- C. 5
- D. 6

gate2008-cse databases b-tree normal

Answer

3.1.17 B Tree: GATE CSE 2009 | Question: 44 top

<https://gateoverflow.in/1330>



The following key values are inserted into a B^+ - tree in which order of the internal nodes is 3, and that of the leaf nodes is 2, in the sequence given below. The order of internal nodes is the maximum number of tree pointers in each node, and the order of leaf nodes is the maximum number of data items that can be stored in it. The B^+ - tree is initially empty

10, 3, 6, 8, 4, 2, 1

The maximum number of times leaf nodes would get split up as a result of these insertions is

- A. 2
- B. 3
- C. 4
- D. 5

gate2009-cse databases b-tree normal

Answer

3.1.18 B Tree: GATE CSE 2010 | Question: 18 top

<https://gateoverflow.in/2191>



Consider a B^+ -tree in which the maximum number of keys in a node is 5. What is the minimum number of keys in any non-root node?

- A. 1
- B. 2
- C. 3
- D. 4

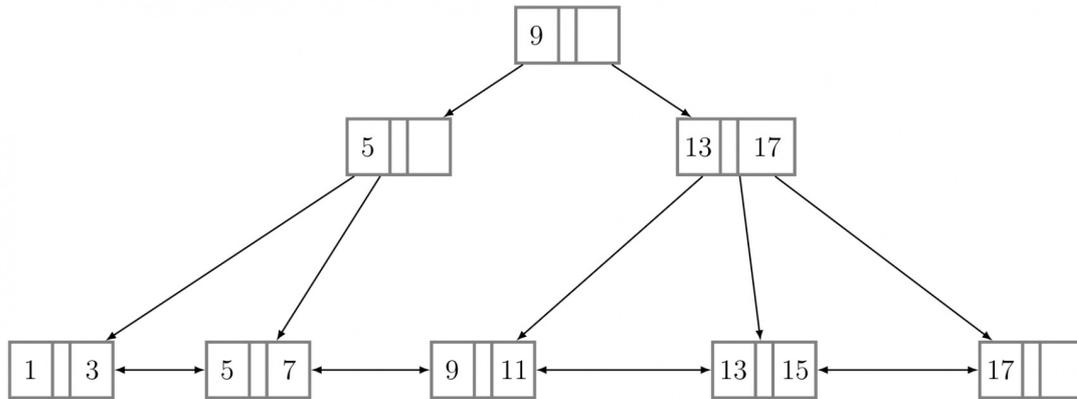
Answer 

3.1.19 B Tree: GATE CSE 2015 Set 2 | Question: 6 [top](#)

<https://gateoverflow.in/8052>



With reference to the B+ tree index of order 1 shown below, the minimum number of nodes (including the Root node) that must be fetched in order to satisfy the following query. "Get all records with a search key greater than or equal to 7 and less than 15" is _____.



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Answer 

3.1.20 B Tree: GATE CSE 2015 Set 3 | Question: 46 [top](#)

<https://gateoverflow.in/8555>



Consider a B+ tree in which the search key is 12 byte long, block size is 1024 byte, recorder pointer is 10 byte long and the block pointer is 8 byte long. The maximum number of keys that can be accommodated in each non-leaf node of the tree is _____.

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Answer 

3.1.21 B Tree: GATE CSE 2016 Set 2 | Question: 21 [top](#)

<https://gateoverflow.in/39569>



B+ Trees are considered BALANCED because.

- A. The lengths of the paths from the root to all leaf nodes are all equal.
- B. The lengths of the paths from the root to all leaf nodes differ from each other by at most 1.
- C. The number of children of any two non-leaf sibling nodes differ by at most 1.
- D. The number of records in any two leaf nodes differ by at most 1.

Answer 

3.1.22 B Tree: GATE CSE 2017 Set 2 | Question: 49 [top](#)

<https://gateoverflow.in/118561>



In a B⁺ Tree , if the search-key value is 8 bytes long , the block size is 512 bytes and the pointer size is 2 B , then the maximum order of the B⁺ Tree is _____

Answer 

3.1.23 B Tree: GATE CSE 2019 | Question: 14 [top](#)

<https://gateoverflow.in/302834>



Which one of the following statements is NOT correct about the B+ tree data structure used for creating an index of a

relational database table?

- A. B+ Tree is a height-balanced tree
- B. Non-leaf nodes have pointers to data records
- C. Key values in each node are kept in sorted order
- D. Each leaf node has a pointer to the next leaf node

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gate2019-cse databases b-tree

Answer 

3.1.24 B Tree: GATE IT 2004 | Question: 79 [top](#)

<https://gateoverflow.in/3723>



Consider a table T in a relational database with a key field K . A B -tree of order p is used as an access structure on K , where p denotes the maximum number of tree pointers in a B -tree index node. Assume that K is 10 bytes long; disk block size is 512 bytes; each data pointer P_D is 8 bytes long and each block pointer P_B is 5 bytes long. In order for each B -tree node to fit in a single disk block, the maximum value of p is

- A. 20
- B. 22
- C. 23
- D. 32

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gate2004-it databases b-tree normal

Answer 

3.1.25 B Tree: GATE IT 2005 | Question: 23, ISRO2017-67 [top](#)

<https://gateoverflow.in/3768>



A B -Tree used as an index for a large database table has four levels including the root node. If a new key is inserted in this index, then the maximum number of nodes that could be newly created in the process are

- A. 5
- B. 4
- C. 3
- D. 2

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gate2005-it databases b-tree normal isro2017

Answer 

3.1.26 B Tree: GATE IT 2006 | Question: 61 [top](#)

<https://gateoverflow.in/3605>



In a database file structure, the search key field is 9 bytes long, the block size is 512 bytes, a record pointer is 7 bytes and a block pointer is 6 bytes. The largest possible order of a non-leaf node in a $B+$ tree implementing this file structure is

- A. 23
- B. 24
- C. 34
- D. 44

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goclasses.in

tests.gatecse.in

gate2006-it databases b-tree normal

Answer 

3.1.27 B Tree: GATE IT 2007 | Question: 84 [top](#)

<https://gateoverflow.in/3536>

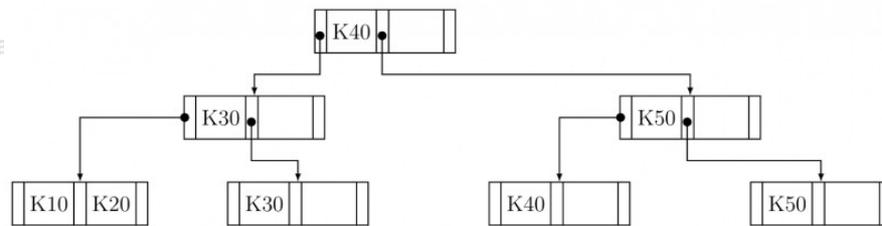


Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.

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Keys $K15$ and then $K25$ are inserted into this tree in that order. Exactly how many of the following nodes (disregarding the links) will be present in the tree after the two insertions?

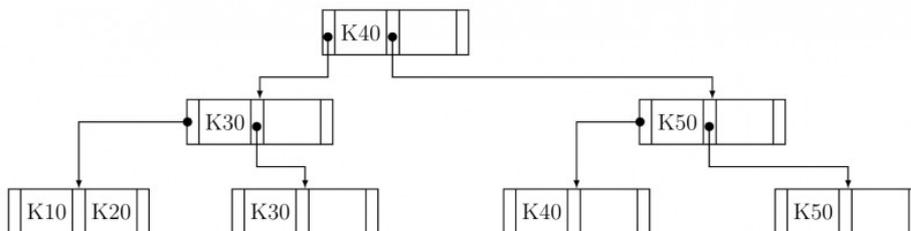


- A. 1
B. 2
C. 3
D. 4

Answer



Consider the B^+ tree in the adjoining figure, where each node has at most two keys and three links.



Keys $K15$ and then $K25$ are inserted into this tree in that order. Now the key $K50$ is deleted from the B^+ tree resulting after the two insertions made earlier. Consider the following statements about the B^+ tree resulting after this deletion.

- i. The height of the tree remains the same.



(disregarding the links) is present in the tree.

- iii. The root node remains unchanged (disregarding the links).

Which one of the following options is true?

- A. Statements (i) and (ii) are true
B. Statements (ii) and (iii) are true
C. Statements (iii) and (i) are true
D. All the statements are false

Answer

Answers: B Tree



✓ B^+ tree [Reference](#).

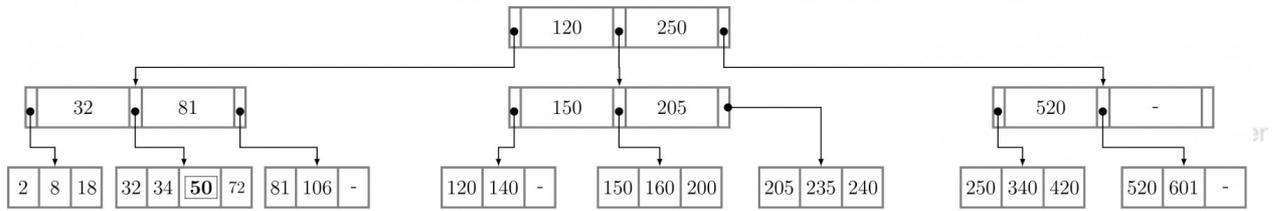
In a B^+ tree only the leaf nodes have a pointer to actual data (record pointers) whereas internal nodes points to index blocks.

In the given question we have

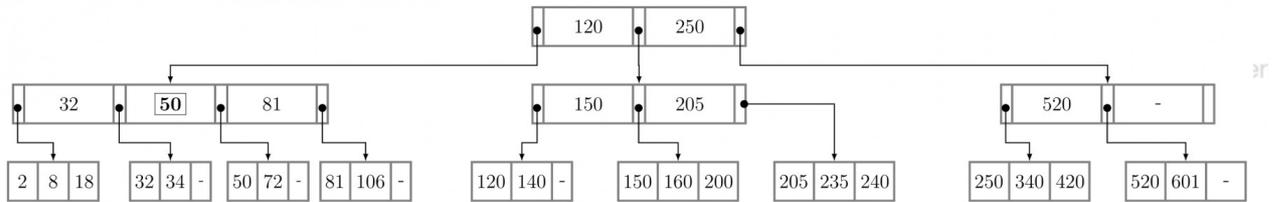
- M : Number of pointers in internal nodes = 3.

- L : Number of data items in a leaf node = 3.
- Further we can see that right biasing is used while splitting a node (same key value moving to the right, in a B^+ tree all internal key values will be present in leaf node as only the leaf node actually points to the data record)

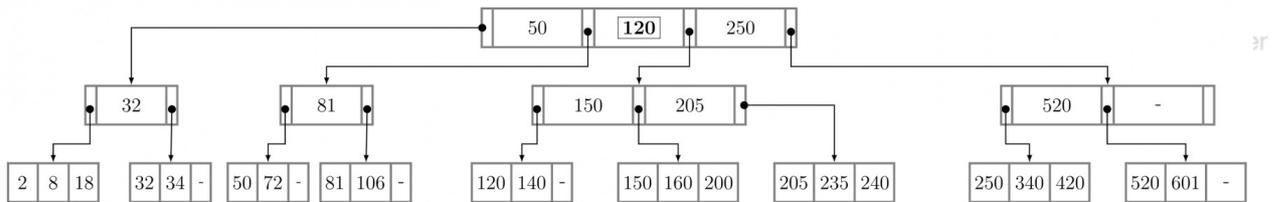
To insert 34 we'll first place it in the sorted order among the leaf nodes.



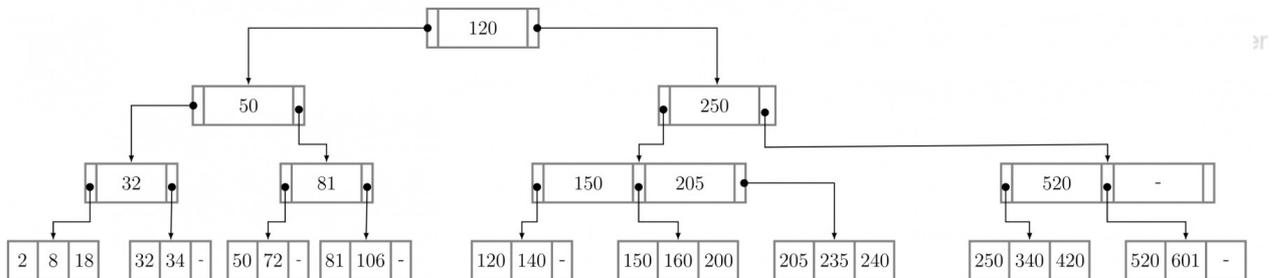
Now, we see that the block (being the leaf node the pointers here are record pointers) having 34 is overflowing and so we'll split it and move the center element to the parent block. There might be a confusion as to whether 34 or 50 should move up, but if we see the question it is following right biasing (same key value is going to the right) and so 50 must move up.



Now, we have an overflow in the internal node as the maximum capacity of an internal node is 3 block pointers but we are having 4 here. So we must again split and move 50 upwards.



Now we have an overflow in the root node and so we must again split and move 120 upwards making a new root.



Now all the B^+ tree requirements are satisfied and so the insertion algorithm terminates.

References



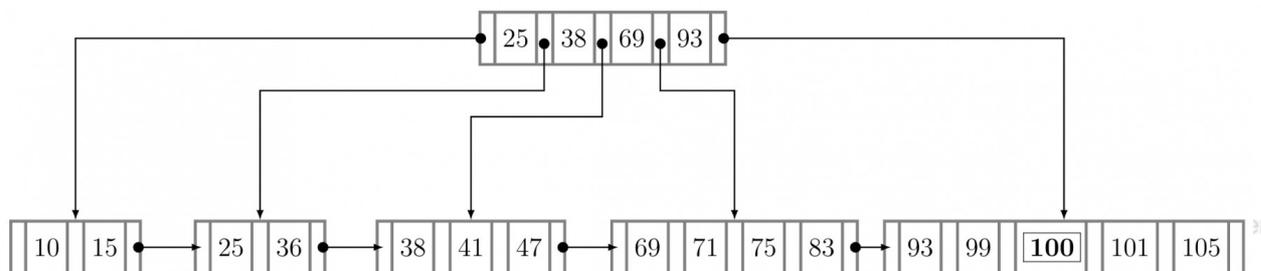
0 votes

-- Arjun Suresh (332k points)

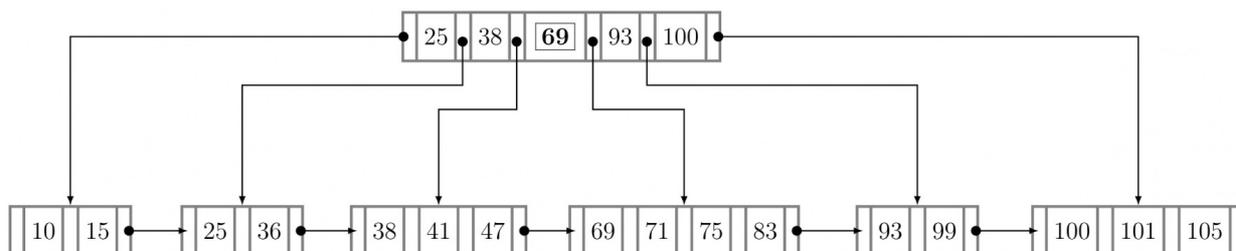


✓ For the given B^+ tree, $d = 2 \implies 2d = 4$. Also right biasing is followed as 69 is to the right of 69 in the parent node.

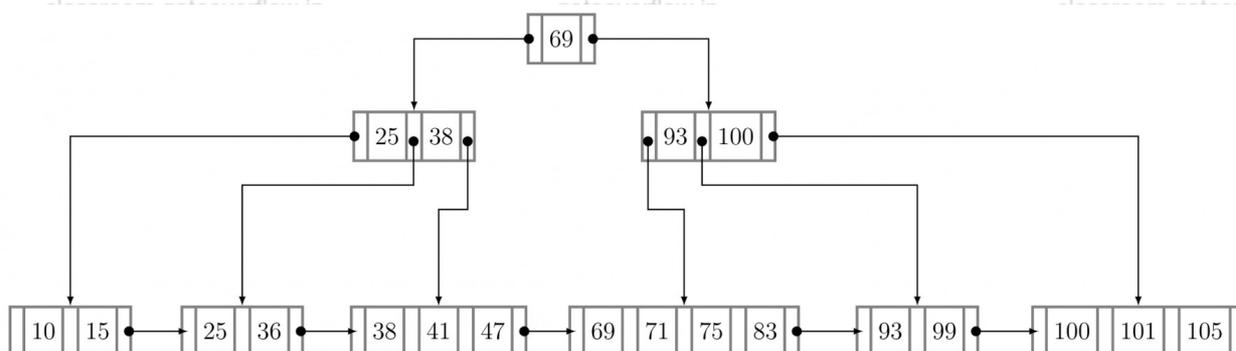
We'll insert 100 in the sorted position among the leaf nodes.



This causes an overflow and so the node will split into 2 by moving the element at position $\left\lceil \frac{2d+1}{2} \right\rceil = \left\lceil \frac{5}{2} \right\rceil = 3$, which is 100. Thus we get.



This again causes an overflow at the root node and 69 needs to be moved up forming a new root. Here, 69 is not a record pointer (only leaf nodes in B^+ tree contains record pointers) and so we need not replicate it while moving up.



Now all the property of B^+ tree is satisfied and the insertion algorithm terminates.

👍 31 votes

-- Bikram (58.4k points)



✓ For n leaves we have $n - 1$ keys in the internal node. (see 'part a' of this [question](#))

Total keys in internal nodes = $n - 1$, each node can have keys between d and $2d$.

For $n - 1$ keys there will be minimum $\left\lceil \frac{n-1}{2d} \right\rceil$ internal nodes, and maximum $\left\lceil \frac{n-1}{d} \right\rceil$ internal nodes.

To calculate Big-Omega I am taking maximum everywhere.

If every node contains $d + 1$ pointers (d keys) then height will be maximum, because number of nodes to be accommodated are fixed $\left(\left\lceil \frac{n-1}{d} \right\rceil \right)$.

If height is h then equation becomes

$$1 + (d + 1) + (d + 1)^2 + (d + 1)^3 + \dots + (d + 1)^{h-1} = \frac{n-1}{d}$$

$$\implies \frac{(d+1)^h - 1}{(d+1) - 1} = \frac{n-1}{d}$$

$$\implies (d + 1)^h = n$$

$$\implies h = \log_{(d+1)} n$$

This is the maximum height possible or says the maximum number of levels possible.

Now using h traverse we can get to the leaf node :

Answer is $O(h)$ i.e., $O(\log_{(d+1)} n) = O(\log_d n)$

References



50 votes

classroom.gateoverflow.in
-- Sachin Mittal (15.8k points)

3.1.4 B Tree: GATE CSE 1997 | Question: 19 [top](#)

<https://gateoverflow.in/2279>



✓ Let us understand specification of B^+ tree first

For a non-root node

- Minimum number of keys = $d \implies$ minimum number of children = $d + 1$
- Maximum number of keys = $2d \implies$ maximum number of children = $2d + 1$

For a root node

- Minimum number of keys = 1 so, minimum number of children = 2
- Maximum number of keys = $2d$ so, maximum number of children = $2d + 1$

Now, coming to our actual question

Part (A). For a given no of leaf node ($L \geq 2$) what will be the total no of keys in internal nodes?

Will solve this in three ways:

1. Assuming maximum nodes at each level

Height	#nodes	#keys
0	1	2d
1	$2d + 1$	$2d(2d + 1)$
\vdots	\vdots	\vdots
h	$(2d + 1)^h$	$2d[(2d + 1)^h]$

No. of leaf nodes = $(2d + 1)^h = L$

Total no. of keys in internal nodes = $2d + 2d(2d + 1) + 2d(2d + 1)^2 + \dots + 2d(2d + 1)^{h-1}$
 $= (2d + 1)^h - 1 = L - 1$

2. Assuming minimum nodes at each level

Height	#nodes	#keys
0	1	1
1	2	2d
\vdots	\vdots	\vdots
h	$2(d + 1)^{h-1}$	$2d[(d + 1)^{h-1}]$

So, no. of leaf nodes = $2(d + 1)^{h-1} = L$

Total no of keys in internal nodes = $1 + 2d + 2d(d + 1) + \dots + 2d(d + 1)^{h-2}$
 $= 2(d + 1)^{h-1} - 1 = L - 1$

3. Whenever there is an overflow in a leaf node (or whenever no of leaf node increases by one), then we move a key in the internal node (or we can say, no of internal keys increases by one).

Now, let's start with the base case. Only 2 leaf nodes (as given $L \geq 2$). So, no. of keys in root node = 1 or $L - 1$.

Once there is an overflow in a single leaf node then no of leaf nodes now would become 3 and at the same the time we will have one more key in our root node.

Part (B) Maximum number of internal nodes in a B^+ tree of order 4 with 52 leaves?

Using Bulk loading approach, here we will use minimum fill factor ($d = 4$ hence, min keys = $d = 4$ and min children/block pointer = $d + 1 = 5$)

So, we have 52 leaves so and need total 52 block pointers and one node should have minimum 5 block pointers.

So, for 52 leaves we require $\lceil 52/5 \rceil = 10$ nodes

For 11 block pointers we require $\lfloor 10/5 \rfloor = 2$ nodes
 For 2 block pointers we require 1 node "it is root node"
So, max no of internal nodes = $10 + 2 + 1 = 13$ nodes

Part (C) Minimum number of leaves in a B+ tree of order d and height $h(h \geq 1)$?

By part (A) "assuming minimum nodes at each level" case

Minimum no. of leaves = $2(d + 1)^{h-1}$

42 votes

-- saurabh rai (9k points)

3.1.5 B Tree: GATE CSE 1999 | Question: 1.25 top

<https://gateoverflow.in/1478>



A. False. Both r stored in disk

B. True. By searching leaf level linearly in B^+ tree, we can say a node is present or not in B^+ tree. But for B tree we have to traverse the whole tree

C. False. B tree and B^+ tree uses dynamic multilevel indexes <http://home.iitj.ac.in/~ramana/ch10-storage-2.pdf>

D. False. Height depends on number of record and also max no of keys in each node (order of tree)

Correct Answer: B

References



49 votes

-- srestha (85.2k points)

3.1.6 B Tree: GATE CSE 1999 | Question: 21 top

<https://gateoverflow.in/1520>



Given a B tree :

- max children at a node : $2m - 1 \implies$ max keys : $2m - 2$
- min children at a node : $m \implies$ min keys : $m - 1$

At Root node : min keys : $1 \implies$ min children : 2

Here, leaf level is at level h (because root is at level 0)

Now, we have to find

1. Minimum keys at leaf level (complete bottommost level, not just a node) -
 - **For this, we have to consider minimum everywhere.**
 - **Firstly we will count the minimum possible nodes at the leaf level.**
 - **At Root Node (level 0) :** It can have minimum 2 child (mean 2 nodes minimum for next level)
 - **At level 1 :** It has 2 nodes, each can have a minimum of m child (so, this gives $2 * m$ minimum possible nodes at next level)
 - **At level 2 :** min $2 * m^2$ Child and so on.
 - **At level $(h - 1)$:** $2 * (m)^{h-1}$ child (these are min number of leaf nodes possible)
 - **At level h (leaf level) :** $2 * (m)^{h-1}$ nodes each having minimum $(m - 1)$ keys. So, this gives the answer as $2 * (m)^{h-1} * (m - 1)$ minimum keys possible at leaf level.
2. Maximum keys at leaf level (complete bottommost level, not just a node) -
 - **For this, we have to count max everywhere.**
 - **At root (level 0) :** max child possible $2m - 1$ (nodes for next level)
 - **At level 1 :** $2m - 1$ nodes give $(2m - 1)^2$ child
 - **At level $(h - 1)$:** $(2m - 1)^h$ child (these are maximum possible nodes at leaf level)
 - **At level h (leaf level) :** $(2m - 1)^h$ nodes each having a maximum of $(2m - 2)$ keys. Giving a total of $(2m - 1)^h * (2m - 2)$ maximum keys at leaf level.

43 votes

-- Himanshu Agarwal (12.4k points)



✓ Answer is (B). The major advantage of B+ tree is in reducing the number of last level access which would be from disk in case of large data size.

<http://stackoverflow.com/questions/15485220/advantage-of-b-trees-over-bsts>

References



gateoverflow.in

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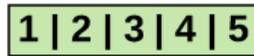
46 votes

-- Arjun Suresh (332k points)

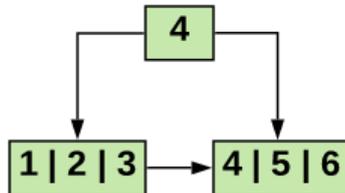


A.i)

i) Inserting 1-5 is straight forward :



then we Insert 6 :



A.ii)

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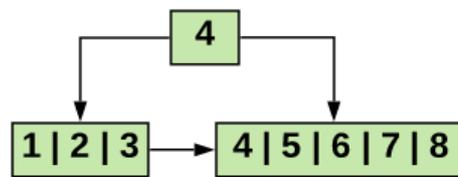
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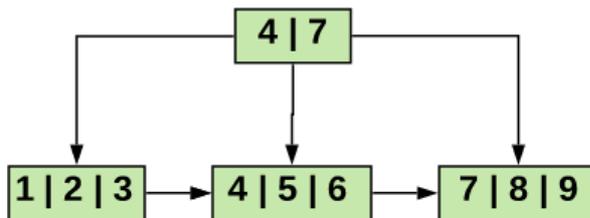
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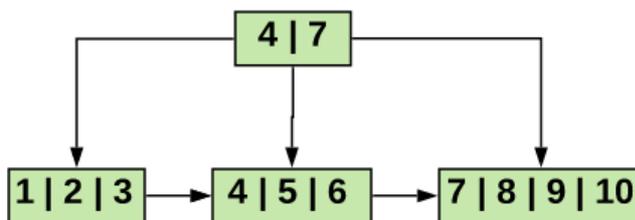
ii) After Inserting 7,8:



Insert 9 :

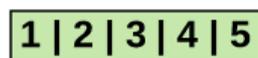


Insert 10 :



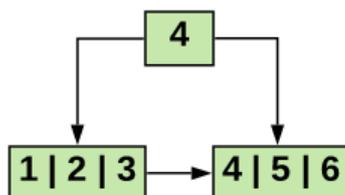
B)

B) Inserting 1-5 is same as previous

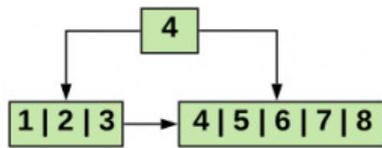


then we Insert 6 :

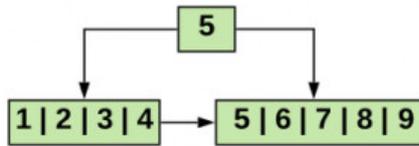
there is no left sibling we split the node.



Insert 7,8:



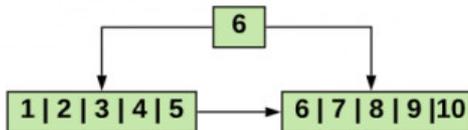
Insert 9 :



there is a left sibling
so we move a key to left
sibling.

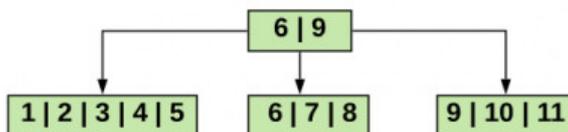
The next 2 insertions weren't asked in the question but will help you to understand part C of this question.

Insert 10 :



there is a left sibling
so we move a key to left
sibling.

Insert 11 :



left sibling is full
so, we split the node.

C. Insert a **LONG SEQUENCE** of keys in **INCREASING ORDER**

- i. In normal case: Insertion always will be done at the rightmost leaf node, and all nodes will have exact $\lfloor \frac{m+1}{2} \rfloor$ keys except this rightmost leaf (no of keys can vary from $\lfloor \frac{m+1}{2} \rfloor$ to m for rightmost leaf).

For a long sequence, we can say the average is approximately
 $\lfloor \frac{m+1}{2} \rfloor$ **(This is the answer).**

(There are two possible answers for this part, I left it on the reader to find out the second one)

Because all nodes will have $\lfloor \frac{m+1}{2} \rfloor$ keys except 1 rightmost node.

we can also find the exact average in this case:

Let there are n keys in total (inserted in increasing order),

No of leaf nodes will be exactly $\left\lceil \frac{n}{\lfloor \frac{m+1}{2} \rfloor} \right\rceil$

Average number of keys in leaf would be: $\frac{n}{\left\lceil \frac{n}{\lfloor \frac{m+1}{2} \rfloor} \right\rceil}$

- ii. With insertion as in (B): In this case, we can observe until the left sibling is full, we are shifting a key to the left leaf. As we insert more and more keys all leaf nodes are filled except the rightmost two leaves, the rightmost 2 leaves can have any number of in $\lfloor \frac{m+1}{2} \rfloor$ to m each.

For a long sequence, we can say the average is approximately $m/2$. (Same reasoning as case i)

we can find the actual average in this case as well,

Let there are n keys in total (inserted in increasing order),

Number of leaf nodes in this case will be $\lceil \frac{n}{m} \rceil$,

so average number of keys would be: $\frac{n}{\lceil \frac{n}{m} \rceil}$

4 votes

-- Nikhil Dhama (2.5k points)

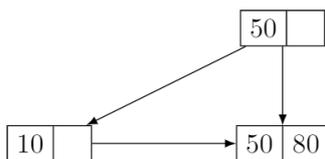


(a) B^+ tree insertion: 80, 50, 10, 70, 30, 100, 90

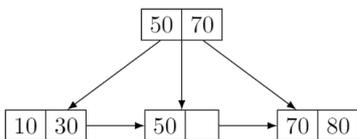
Order of $B^+ = p = 3$

- Overflow: When number of key values exceed $p - 1 = 3 - 1 = 2$

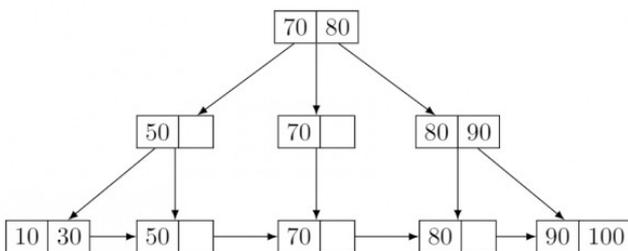
Tree after insertion of 10 :



Tree after insertion of 30 :



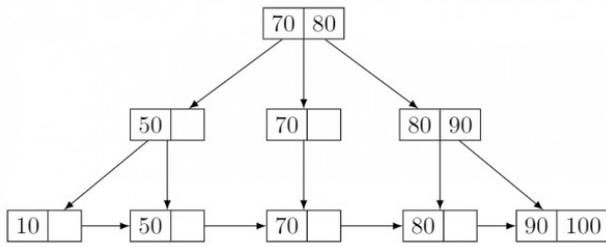
Tree after insertion of 90 :



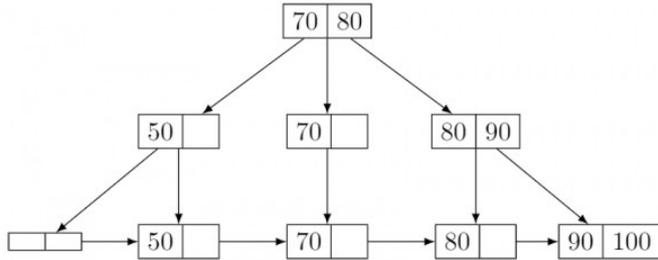
(b)

- Underflow: if leaf node contain $\lceil \frac{p}{2} \rceil - 1 = 2 - 1 = 1$ key values.

Deletion of key-value 30 :



Deletion of key-value 10 :



Here when we delete the key-value 10 then underflow happened, so we can merge this node with the right sibling.

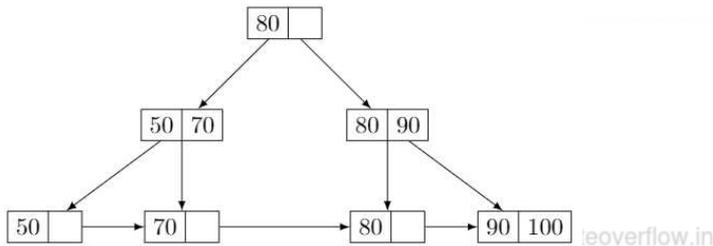
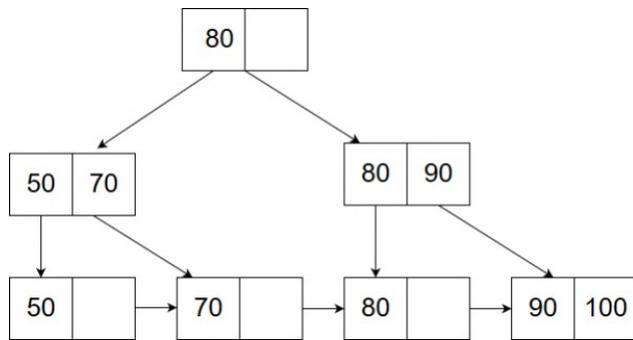
When we merge two nodes then the parent node one value needs to come down i.e. 50 here.

Now if we try to bring 50 down then that node will again suffer from underflow as it will become empty.

so we will try to merge this node it with its right sibling i.e. the node which contains 70

Again, When we merge two nodes(nodes in the 2nd level that contain 50 and 70) then one value of the parent node (i.e. node having 50, 70) needs to come down

So we will bring 70 down and merge it with 50 since bringing 70 down will not cause underflow as 80 is present in the parent node.



3 votes

-- Lakshman Patel (65.7k points)



✓ For A)

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X1 = Variable (Key can be found @ Internal nodes at various levels)

X2 = Constant

X3 = Variable, We need to just check where key is present/absent, not to access Data. (A successful search means that the key

exists in the database and unsuccessful means that it is not present in the database.) So Variable $X4 = \text{Constant}$

For Part B) i) Write down two copies of the same table for comparison side by side. Just map **B** of first to A of the second copy. Those matching tuples take **A** of first table & **B** of seconds.

Content of View A

A	B
1	3
1	4
2	5

For Part B) ii)

Additional tuples getting inserted:

A	B
11	7
11	8
2	6
1	11

30 votes

-- Akash Kanase (36k points)

3.1.11 B Tree: GATE CSE 2002 | Question: 2.23, UGCNET-June2012-II: 26

<https://gateoverflow.in/853>



✓ Answer: C

In a B^+ tree we want an entire node content to be in a disk block. A node can contain up to p pointers to child nodes and up to $p - 1$ key values for a B^+ tree of order p . Here, key size is 8 bytes and index pointer size is 4 bytes. Now a B^+ tree has different structure for internal node and leaf nodes. While internal nodes can have upto $p - 1$ key values and p child pointers, leaf node will have one sibling pointer in addition to maximum $p - 1$ keys and $p - 1$ record pointers. Since our key is Name attribute which is not assumed to be unique it must be a secondary index and hence the record pointer must be an index pointer to primary index. This will ensure size of a leaf node is same as the size of a non-leaf node. Hence for a maximum sized node we can write

$$(8 + 4)(p - 1) + 4 \leq 512 \implies 12p \leq 520 \implies p = 43.$$

<http://www.cburch.com/cs/340/reading/btree/index.html>

References



49 votes

-- Rajarshi Sarkar (27.9k points)

3.1.12 B Tree: GATE CSE 2003 | Question: 65

<https://gateoverflow.in/952>



✓ (B) is the correct answer.

Once we add G , the leaf node becomes $B G H I$, since we can have only 3 keys. the node has to split at G or H , and G or H will be added to parent node.

Since P is the parent node in options 1 and 2, its evident the 3rd element i.e. H should be selected for splitting (because after adding any key from the leftmost child node, P becomes the 3rd element in the node)

Now parent node becomes $H L P U$, select P as for splitting, and you get option B.

Hence, answer is B.

22 votes

-- ryan sequeira (3k points)



Answer: C

$$14(p - 1) + 6p \leq 512$$

$$20p - 14 \leq 512$$

$$20p \leq 526$$

Therefore, $p = 26$.

32 votes

-- Rajarshi Sarkar (27.9k points)



Answer: D

- A. Cannot compare both the trees solely on basis of this.
- B. Both trees are BST.
- C. False. High fanout in B+ ensures that it takes more memory than BST.
- D. True. Records are stored in disk blocks.

40 votes

-- Rajarshi Sarkar (27.9k points)

The answer is **option A**.

$$B_p + P(R_p + \text{Key}) \leq \text{BlockSize}$$

$$\implies 1 \times 6 + n(7 + 9) \leq 1024$$

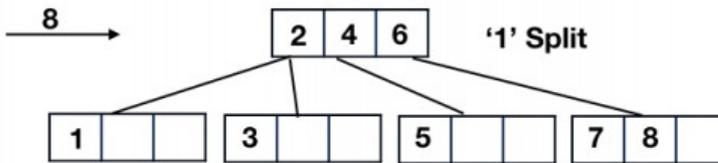
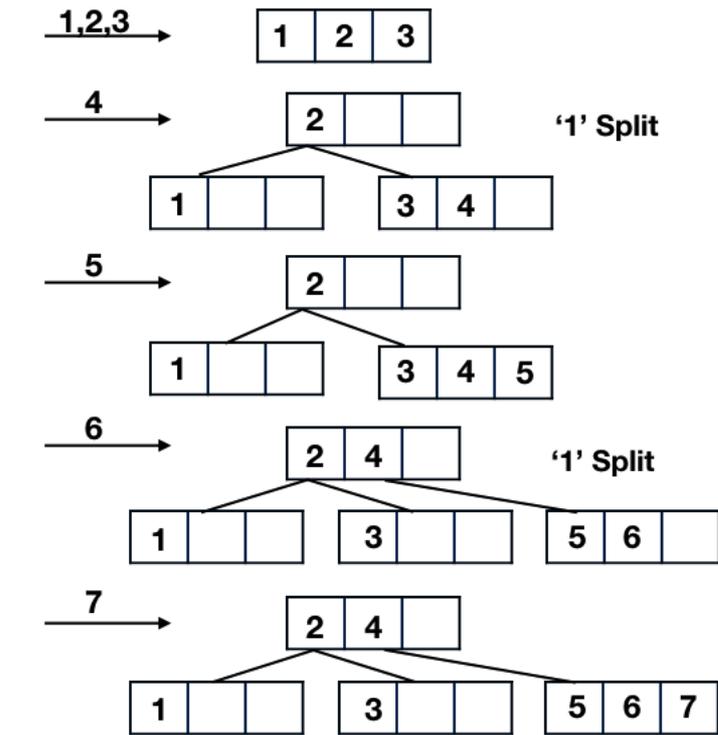
$$\implies n \leq 63.625$$

So, **63** is the answer.

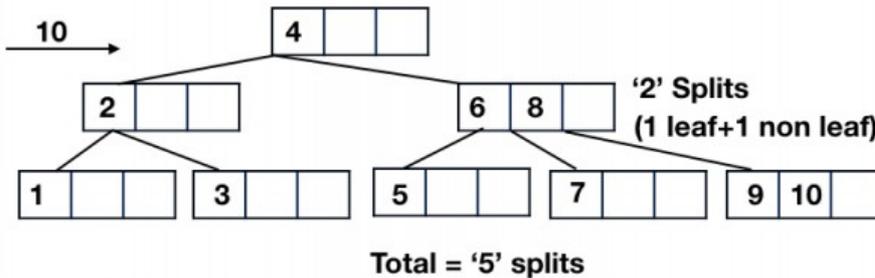
62 votes

-- Gate Keeda (15.9k points)

**Total 5 splitting** will occur during 10 successive insertionsLet's take 10 successive key values as $\{1, 2, 3, \dots, 10\}$ which can cause maximum possible splits.



9 → No. Will adjust with 7,3,5



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60 votes

-- Prateek kumar (6.7k points)

3.1.17 B Tree: GATE CSE 2009 | Question: 44 top 5

<https://gateoverflow.in/1330>



✓ In this question they have asked only to count leaf node splits.

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So, after discussing with my friends on Facebook, I found that you will get two different answers depending on which convention you follow.

Convention 1: put the middle element in the left node, if you follow this you will get 4 as answer.

Convention 2: put the middle element in the right node, if you follow this you will get 3 as answer.

4 splits:

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1. after inserting 6
2. after inserting 4
3. after inserting 2 (there will be an internal node split and a leaf node split)
4. after inserting 1

Correct Answer: C

👍 63 votes

-- Vikrant Singh (11.2k points)

3.1.18 B Tree: GATE CSE 2010 | Question: 18 top

<https://gateoverflow.in/2191>



✓ Answer: B

$$\text{Order} = 5 + 1 = 6$$

$$\text{Minimum children in a non root node} = \lceil \frac{\text{Order}}{2} \rceil = \lceil \frac{6}{2} \rceil = 3$$

$$\text{Keys} = \text{Minimum children in a non root node} - 1 = 2$$

👍 62 votes

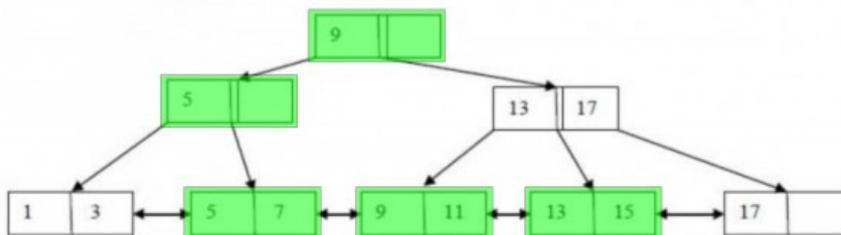
-- Rajarshi Sarkar (27.9k points)

3.1.19 B Tree: GATE CSE 2015 Set 2 | Question: 6 top

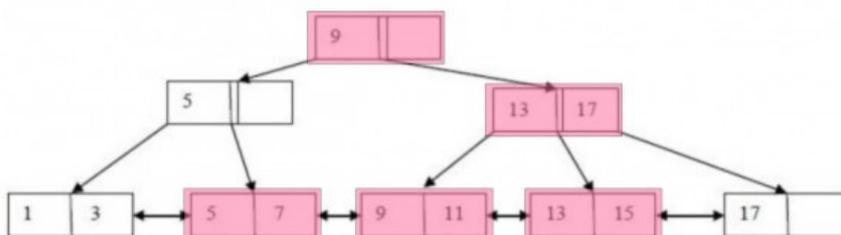
<https://gateoverflow.in/8052>



✓ whichever way you go from the root to leaves, you'll always end up counting 5 nodes.



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👍 60 votes

-- Amar Vashishth (25.2k points)

3.1.20 B Tree: GATE CSE 2015 Set 3 | Question: 46 top

<https://gateoverflow.in/8555>



✓ $(n-1)12 + n \times 8 \leq 1024$

$$n \leq 51$$

$$\text{In non leaf node number of keys} = n - 1$$

$$= 51 - 1 = 50$$

👍 63 votes

-- ppm (543 points)

✓ **Option A: In B^+ Tree all leaves are at same level.**

In both B Tree and B^+ trees, depth (length of root to leaf paths) of all leaf nodes is same. This is made sure by the insertion and deletion operations. In these trees, we do insertions in a way that if we have increase height of tree after insertion, we increase height from the root. This is different from BST where height increases from leaf nodes. Similarly, if we have to decrease height after deletion, we move the root one level down. This is also different from BST which shrinks from the bottom. The above ways of insertion and deletion make sure that depth of every leaf node is same.

👍 41 votes

-- ukn (543 points)

✓ Let order of B^+ tree is p then maximum number of child pointers = p and maximum number of keys = $p - 1$.
To accommodate all child pointers and search key, total size of these together can not exceed 512 bytes.

$$2(p) + 8(p - 1) \leq 512$$

$$\implies p \leq 52$$

Therefore, maximum order must be **52**.

👍 52 votes

-- Sachin Mittal (15.8k points)

✓ Properties of B^+ trees:
1. B^+ tree is height balance tree.
2. Key value is in sorted order.
3. Leaf node has pointer to next leaf node.
4. Non leaf node has pointer to a node (leaf or non leaf) and not pointer to data record.

Option B is not correct.

👍 26 votes

-- Digvijay (44.9k points)

✓ It is **23**.

$$(p - 1)(\text{key_ptr_size} + \text{record_ptr_size}) + p \cdot (\text{block_ptr_size}) \leq 512$$

$$\implies (p - 1)(10 + 8) + p \times 5 \leq 512$$

$$\implies 23p \leq 530$$

$$\implies p \leq 23.04$$

So, maximum value of p possible will be **23**.

👍 42 votes

-- Sandeep_Uniyal (6.5k points)

✓ Suppose all nodes are completely full means every node has $n - 1$ keys. tree has 4 levels if a new key is inserted then at every level there will be created a new node. and in worst case root node will also be broken into two parts. and we have 4 levels so, answer should be **5** because tree will be increased with one more level.

Correct Answer: **A**

👍 79 votes

-- Manu Thakur (34k points)

✓ Answer is **(C)**.

From the structure of B^+ tree we can get this equation:

$$n \times p + (n - 1) \times k \leq B \quad (\text{for non leaf node})$$

Here, n =order, p =tree/block/index pointer, B =size of block

I non leaf node no record pointer is there in B^+ tree.

$$\text{So, } n \times p + (n - 1)k \leq B$$

$$n \times 6 + (n - 1) \times 9 \leq 512$$

$$\Rightarrow n \leq 34.77$$

Largest possible value for n is 34.

👍 35 votes

-- jayendra (6.7k points)

3.1.27 B Tree: GATE IT 2007 | Question: 84 [top](#)

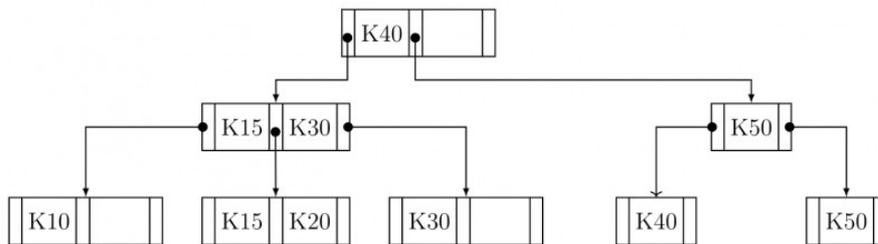
<https://gateoverflow.in/3536>



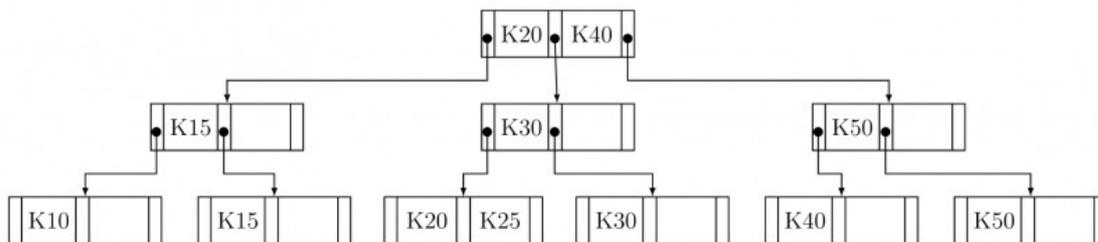
✓ Option (A) is correct.

It is a B^+ Tree.

After inserting $K15$ we get



Now, we insert $K25$, which gives -



So, we see in the final tree only $(K20, K25)$ is present. Hence, 1 (Ans).

👍 55 votes

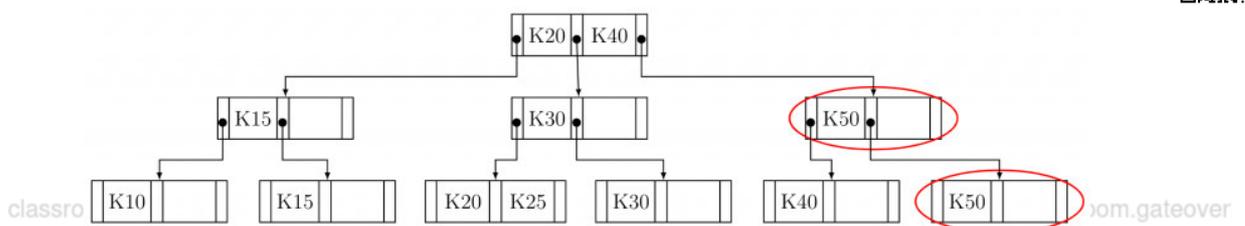
-- Himanshu Agarwal (12.4k points)

3.1.28 B Tree: GATE IT 2007 | Question: 85 [top](#)

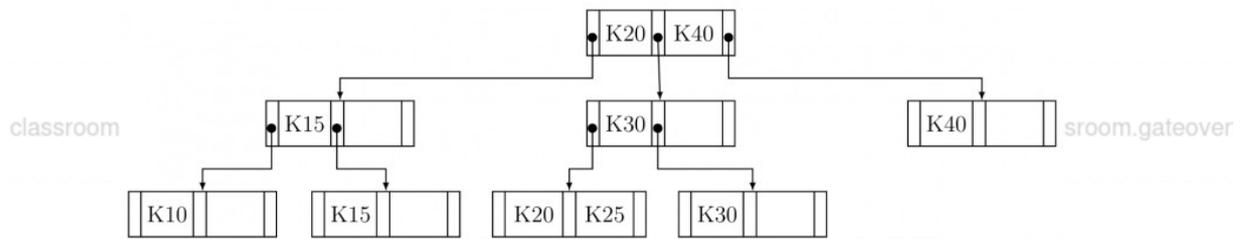
<https://gateoverflow.in/3537>



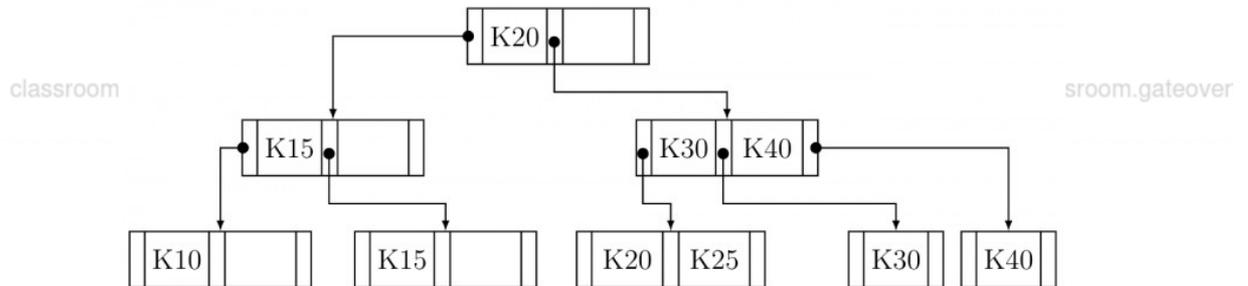
✓



Now merge 40 in upper level.



Now redistribute:



So, the answer is A.

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 39 votes -- srestha (85.2k points)

3.2 Candidate Keys (5) top

3.2.1 Candidate Keys: GATE CSE 1994 | Question: 3.7 top <https://gateoverflow.in/2493>

An instance of a relational scheme $R(A, B, C)$ has distinct values for attribute A . Can you conclude that A is a candidate key for R ? tests.gatecse.in goclasses.in tests.gatecse.in

gate1994 databases easy database-normalization candidate-keys descriptive

Answer

3.2.2 Candidate Keys: GATE CSE 2011 | Question: 12 top <https://gateoverflow.in/2114>

Consider a relational table with a single record for each registered student with the following attributes:

1. Registration_Num: Unique registration number for each registered student tests.gatecse.in
2. UID: Unique identity number, unique at the national level for each citizen
3. BankAccount_Num: Unique account number at the bank. A student can have multiple accounts or joint accounts. This attribute stores the primary account number.
4. Name: Name of the student
5. Hostel_Room: Room number of the hostel

Which of the following options is **INCORRECT**?

- A. BankAccount_Num is a candidate key
- B. Registration_Num can be a primary key goclasses.in tests.gatecse.in
- C. UID is a candidate key if all students are from the same country
- D. If S is a super key such that $S \cap \text{UID}$ is NULL then $S \cup \text{UID}$ is also a superkey

gate2011-cse databases normal candidate-keys

Answer

3.2.3 Candidate Keys: GATE CSE 2014 Set 2 | Question: 21 top <https://gateoverflow.in/1978>

The maximum number of superkeys for the relation schema $R(E, F, G, H)$ with E as the key is _____.

gate2014-cse-set2 databases numerical-answers easy candidate-keys

Answer



Given an instance of the STUDENTS relation as shown as below

StudentID	StudentName	StudentEmail	StudentAge	CPI
2345	Shankar	shankar@math	X	9.4
1287	Swati	swati@ee	19	9.5
7853	Shankar	shankar@cse	19	9.4
9876	Swati	swati@mech	18	9.3
8765	Ganesh	ganesh@civil	19	8.7

For (StudentName, StudentAge) to be a key for this instance, the value X should NOT be equal to_____.

gate2014-cse-set2

databases

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easy

candidate-keys

Answer



A *prime attribute* of a relation scheme R is an attribute that appears

- A. in all candidate keys of R
- B. in some candidate key of R
- C. in a foreign key of R
- D. only in the primary key of R

gate2014-cse-set3

databases

easy

candidate-keys

Answer

Answers: Candidate Keys



✓ No.

A	B	C
1	5	6
2	4	7
3	4	5

Suppose this is the relational instance at any point of time.

Now we can see that $A \rightarrow BC$ holds for this instance, hence $A^+ = \{A, B, C\}$. (For every unique value of A , values of B and C are distinct.

But FDs are defined on the schema and not on any instance. So, based on the state of any instance we cannot say what holds for schema (there can be other instances too for R). At the best we can say that $A \rightarrow BC$ **MAY hold** for R .

PS: If we have a single instance where $A \rightarrow BC$ is not holding, it is enough to say $A \rightarrow BC$ does not hold for the relation R .

58 votes

-- Sourav Roy (2.9k points)



✓ Answer is (A)

A relation is given (**Registration_Num, UID, BankAccount_Num, Name, Hostel_Room**).

Now, **Registration_Num** is unique for each student. So with this, we can identify each student. Hence, this can be the primary key.

UID: It's an identification number for a person in a country. (Say you're in India and your **UID** is 0243. Someone in Pakistan

may also have the same **UID** as 0243). So, if all students are from India (that is, the same country) then their **UID** will be different and then **UID** will be a Candidate key.

If **S** is a super key then **S ∪ UID** will be a Super key. e.g. **R(A, B, C, D)**, If **AB** is a superkey then **ABC, ABCD** are also superkey.

BankAccount_Num is not a candidate key, because a student can have multiple accounts or joint accounts. We can not identify each student uniquely with **BankAccount_Num**.

56 votes

-- Pranay Datta (7.8k points)

3.2.3 Candidate Keys: GATE CSE 2014 Set 2 | Question: 21 top

https://gateoverflow.in/1978



✓ Super Key is any set of attributes that uniquely determines a tuple in a relation.

Since **E** is the **only key**, **E** should be present in any super key.

Excluding **E**, there are three attributes in the relation, namely **F, G, H**. Hence, if we add **E** to any subset of those three attributes, then the resulting set is a super key. Number of subsets of **{F, G, H}** is 8. **Hence the answer is**

8. classroom.gateoverflow.in

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The following are Super Keys:

$$\left\{ \begin{array}{l} E \\ EF \\ EG \\ EH \\ EFG \\ EFH \\ EGH \\ EFGH \end{array} \right\}$$

50 votes

-- Sankaranarayanan P.N (8.5k points)

3.2.4 Candidate Keys: GATE CSE 2014 Set 2 | Question: 22 top

https://gateoverflow.in/1980



✓ Should not equal to 19.

Since if it is equal the same key will have two different values for "StudentEmail" which cannot be true by the definition of candidate/primary/super key.

43 votes

-- Aravind (2.8k points)

3.2.5 Candidate Keys: GATE CSE 2014 Set 3 | Question: 22 top

https://gateoverflow.in/2056



✓ Answer (B).

The attributes of a candidate key are called the prime attributes. Suppose **ABC** is one candidate key of a Relation **R(ABCDEFGH)**. Then the attributes **A, B** and **C** all are prime attributes. Similarly if **ABD** is also another candidate key in the same relation **R**, then **D** is also a prime attribute. And conversely, an attribute that does not occur in ANY candidate key is called a non-prime attribute.

18 votes

-- Divya Bharti (8.8k points)

3.3 Conflict Serializable (3) top

3.3.1 Conflict Serializable: GATE CSE 2017 Set 2 | Question: 44 top

https://gateoverflow.in/118640



Two transactions **T₁** and **T₂** are given as

$$T_1 : r_1(X)w_1(X)r_1(Y)w_1(Y)$$

$$T_2 : r_2(Y)w_2(Y)r_2(Z)w_2(Z)$$

where **r_i(V)** denotes a *read* operation by transaction **T_i** on a variable **V** and **w_i(V)** denotes a *write* operation by transaction **T_i** on a variable **V**. The total number of conflict serializable schedules that can be formed by **T₁** and **T₂** is _____

gate2017-cse-set2 databases transaction-and-concurrency numerical-answers conflict-serializable

Answer

3.3.2 Conflict Serializable: GATE CSE 2021 Set 1 | Question: 32

https://gateoverflow.in/357419



Let $r_i(z)$ and $w_i(z)$ denote read and write operations respectively on a data item z by a transaction T_i . Consider the following two schedules.

- $S_1 : r_1(x)r_1(y)r_2(x)r_2(y)w_2(y)w_1(x)$
- $S_2 : r_1(x)r_2(x)r_2(y)w_2(y)r_1(y)w_1(x)$

Which one of the following options is correct?

- S_1 is conflict serializable, and S_2 is not conflict serializable
- S_1 is not conflict serializable, and S_2 is conflict serializable
- Both S_1 and S_2 are conflict serializable
- Niether S_1 nor S_2 is conflict serializable

gate2021-cse-set1 databases transaction-and-concurrency conflict-serializable

Answer

3.3.3 Conflict Serializable: GATE CSE 2021 Set 2 | Question: 32

https://gateoverflow.in/357508



Let S be the following schedule of operations of three transactions T_1, T_2 and T_3 in a relational database system:

$$R_2(Y), R_1(X), R_3(Z), R_1(Y)W_1(X), R_2(Z), W_2(Y), R_3(X), W_3(Z)$$

Consider the statements P and Q below:

- $P: S$ is conflict-serializable.
- $Q: \text{If } T_3 \text{ commits before } T_1 \text{ finishes, then } S \text{ is recoverable.}$

Which one of the following choices is correct?

- Both P and Q are true
- P is true and Q is false
- P is false and Q is true
- Both P and Q are false

gate2021-cse-set2 databases transaction-and-concurrency conflict-serializable

Answer

Answers: Conflict Serializable

3.3.1 Conflict Serializable: GATE CSE 2017 Set 2 | Question: 44

https://gateoverflow.in/118640



- ✓ There is only one way to have (conflict) serializable schedule as $T1 \rightarrow T2$, because last operation of $T1$ and first operation of $T2$ conflicts each other.

Now See How many schedules are conflict serializable to $T2 \rightarrow T1$.

I am writing $T1$ —

$$R(A) \quad W(A) \quad R(B) \quad W(B)$$

If you notice, I wrote $T1$ with space in between operation.

Now See $T2$ from right, if we see $T2$ from right, then tell me first operation of $T2$ that conflicts with any operation of $T1$.

$W(C)$ and $R(C)$ do not have any conflict with any operation, but $W(B)$ has.

Pick $W(B)$ and see, at how many places it can be there.

- Case1: **W(B)** $R(A)$ $W(A)$ $R(B)$ $W(B)$
 Case2: $R(A)$ **W(B)** $W(A)$ $R(B)$ $W(B)$
 Case3: $R(A)$ $W(A)$ **W(B)** $R(B)$ $W(B)$

Pick each case and see, how many positions other operation of $T2$ can take.

Case1: **W(B)** R(A) W(A) R(B) W(B)

How many positions $W(C)$ and $R(C)$ can take ?

(note that these $W(C)$ and $R(C)$ cant come before **W(B)**)

that is $5C_1 + 5C_2 = 15$ (either both can take same space or two different spaces)

Now see, for each of these 15 positions, how many can $R(B)$ take ?

Obliviously $R(B)$ cant come before $W(B)$ therefore one position.

$15 \times 1 = 15$ total possible schedules from case 1.

Case2: R(A) **W(B)** W(A) R(B) W(B)

How many positions $W(C)$ and $R(C)$ can take ?

that is $4C_1 + 4C_2 = 10$ (either both can take same space or two different spaces)

Now see, for each of these 10 positions, how many can $R(B)$ take ?

Only 2 positions, because it has to come before **W(B)**.

$10 \times 2 = 20$ total possible schedules from case 2.

Case3: R(A) W(A) **W(B)** R(B) W(B)

How many positions $W(C)$ and $R(C)$ can take ?

that is $3C_1 + 3C_2 = 6$

Now see, for each of these 6 positions, how many can $R(B)$ take ?

Only 3 positions, because it has to come before **W(B)**.

$6 \times 3 = 18$ total possible schedules from case 3.

total schedules that are conflict serializable as $T_2 \rightarrow T_1 = 15 + 20 + 18 = 53$.

total schedules that are conflict serializable as $T_1 \rightarrow T_2 = 1$.

total schedules that are conflict serializable as either $T_2 \rightarrow T_1$ or $T_1 \rightarrow T_2 = 53 + 1 = 54$.

👍 158 votes

-- Sachin Mittal (15.8k points)

3.3.2 Conflict Serializable: GATE CSE 2021 Set 1 | Question: 32 [top](#)

<https://gateoverflow.in/357419>



✓

T ₁	T ₂
$r_1(x)$	
$r_1(y)$	
	$r_2(x)$
	$r_2(y)$
	$w_2(y)$
$w_1(x)$	

Here $r_1(y)$ and $w_2(y)$ are conflicting pairs, giving $T_1 \rightarrow T_2$ and $r_2(x)$ and $w_1(x)$ giving $T_2 \rightarrow T_1$, so the schedule is not conflict serializable.

T ₁	T ₂
r ₁ (x)	r ₂ (x)
	r ₂ (y)
	w ₂ (y)
r ₁ (y)	
w ₁ (x)	

Here $r_2(x)$ and $w_2(x)$ are conflicting pairs giving $T_2 \rightarrow T_1$, and $w_2(y)$ and $r_1(y)$ also giving $T_2 \rightarrow T_1$, therefore this schedule is conflict serializable.

Correct Option B

👍 1 votes

-- zxy123 (2.8k points)

3.3.3 Conflict Serializable: GATE CSE 2021 Set 2 | Question: 32 [top](#)

<https://gateoverflow.in/357508>



✓

T ₁	T ₂	T ₃
R(X)	R(Y)	
R(Y)		R(Z)
W(X)	R(Z)	
	W(Y)	R(X)
		W(Z)

- $T_1 \rightarrow T_2$ due to $R_1(Y)$ being before $W_2(Y)$
- $T_1 \rightarrow T_3$ due to $W_1(X)$ being before $R_3(X)$
- $T_2 \rightarrow T_3$ due to $R_2(Z)$ is being $W_3(Z)$ in the schedule.

There are no other conflicts and the discovered conflicts are not forming the cycle.

Therefore, the given schedule is Conflict Serializable.

Statement Q : If T_3 commits, before T_1 finishes, then S is recoverable.

! Schedule S is recoverable, if Tj creating the dirty read by reading the written data by Ti and Tj commits after Ti commits.

By the above definition, Q is wrong.

Option B is correct.

👍 3 votes

-- Shaik Masthan (50.4k points)

3.4

Data Independence (1) [top](#)

3.4.1 Data Independence: GATE CSE 1994 | Question: 3.11 [top](#)

<https://gateoverflow.in/2497>



State True or False with reason

Logical data independence is easier to achieve than physical data independence.

gate1994 databases normal data-independence true-false

Answer [🔗](#)

Answers: Data Independence



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 This is **False**.

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Generally, physical data independence exists in most databases and file environments where physical details are hidden from the user and applications remain unaware of these details. On the other hand, logical data independence is harder to achieve because of a much stricter requirement - it allows structural and constraint changes without affecting application programs.

👍 27 votes

-- Akash Kanase (36k points)



State whether the following statements are TRUE or FALSE:

A relation r with schema (X, Y) satisfies the function dependency $X \rightarrow Y$, The tuples $\langle 1, 2 \rangle$ and $\langle 2, 2 \rangle$ can both be in r simultaneously.

gate1987 databases database-normalization true-false

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Answer



What are the three axioms of functional dependency for the relational databases given by Armstrong.

gate1988 normal descriptive databases database-normalization

Answer



Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, x \rightarrow z\} \mid = x \rightarrow yz$$

(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and $\mid =$ means derives).

gate1988 easy descriptive databases database-normalization

Answer



Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, wy \twoheadrightarrow z\} \mid = xw \twoheadrightarrow z$$

(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and $\mid =$ means derives).

gate1988 normal descriptive databases database-normalization

Answer



Using Armstrong's axioms of functional dependency derive the following rules:

$$\{x \rightarrow y, z \subseteq y\} \mid = x \rightarrow z$$

(Note: $x \rightarrow y$ denotes y is functionally dependent on x , $z \subseteq y$ denotes z is subset of y , and $\mid =$ means derives).

gate1988 normal descriptive databases database-normalization

Answer 

3.5.6 Database Normalization: GATE CSE 1990 | Question: 2-iv [top](#) 

<https://gateoverflow.in/83977>



Match the pairs in the following questions:

(a) Secondary index	(p) Function dependency
(b) Non-procedural query language	(q) B-tree
(c) Closure of a set of attributes	(r) Domain calculus
(d) Natural join	(s) Relational algebraic operations

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gate1990

match-the-following

database-normalization

databases

Answer 

3.5.7 Database Normalization: GATE CSE 1990 | Question: 3-ii [top](#) 

<https://gateoverflow.in/84054>



Indicate which of the following statements are true:

A relational database which is in 3NF may still have undesirable data redundancy because there may exist:

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- A. Transitive functional dependencies
- B. Non-trivial functional dependencies involving prime attributes on the right-side.
- C. Non-trivial functional dependencies involving prime attributes only on the left-side.
- D. Non-trivial functional dependencies involving only prime attributes.

gate1990

normal

databases

database-normalization

multiple-selects

Answer 

3.5.8 Database Normalization: GATE CSE 1994 | Question: 3.6 [top](#) 

<https://gateoverflow.in/2492>



State True or False with reason

There is always a decomposition into Boyce-Codd normal form (BCNF) that is lossless and dependency preserving.

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gate1994

databases

database-normalization

easy

true-false

Answer 

3.5.9 Database Normalization: GATE CSE 1995 | Question: 26 [top](#) 

<https://gateoverflow.in/2665>



Consider the relation scheme $R(A, B, C)$ with the following functional dependencies:

- $A, B \rightarrow C$,
- $C \rightarrow A$

- A. Show that the scheme R is in 3NF but not in BCNF.
- B. Determine the minimal keys of relation R .

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gate1995

databases

database-normalization

normal

descriptive

Answer 

3.5.10 Database Normalization: GATE CSE 1997 | Question: 6.9 [top](#) 

<https://gateoverflow.in/2265>



For a database relation $R(a, b, c, d)$, where the domains a, b, c, d include only atomic values, only the following functional dependencies and those that can be inferred from them hold

- $a \rightarrow c$
- $b \rightarrow d$

This relation is

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- A. in first normal form but not in second normal form
- B. in second normal form but not in first normal form
- C. in third normal form
- D. none of the above

gate1997 databases database-normalization normal

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Answer 

3.5.11 Database Normalization: GATE CSE 1998 | Question: 1.34 [top](#)

<https://gateoverflow.in/1671>



Which normal form is considered adequate for normal relational database design?

- A. $2NF$
- B. $5NF$
- C. $4NF$
- D. $3NF$

gate1998 databases database-normalization easy

goclasses.in

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Answer 

3.5.12 Database Normalization: GATE CSE 1998 | Question: 26 [top](#)

<https://gateoverflow.in/1741>



Consider the following database relations containing the attributes

- Book_id
- Subject_Category_of_book
- Name_of_Author
- Nationality_of_Author

With Book_id as the primary key.

- a. What is the highest normal form satisfied by this relation?
- b. Suppose the attributes Book_title and Author_address are added to the relation, and the primary key is changed to {Name_of_Author, Book_title}, what will be the highest normal form satisfied by the relation?

gate1998 databases database-normalization normal descriptive

goclasses.in

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Answer 

3.5.13 Database Normalization: GATE CSE 1999 | Question: 1.24 [top](#)

<https://gateoverflow.in/1477>



Let $R = (A, B, C, D, E, F)$ be a relation scheme with the following dependencies $C \rightarrow F, E \rightarrow A, EC \rightarrow D, A \rightarrow B$. Which one of the following is a key for R ?

- A. CD
- B. EC
- C. AE
- D. AC

gate1999 databases database-normalization easy

goclasses.in

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Answer 

3.5.14 Database Normalization: GATE CSE 1999 | Question: 2.7, UGCNET-June2014-III: 25 [top](#)

<https://gateoverflow.in/1485>



Consider the schema $R = (S, T, U, V)$ and the dependencies $S \rightarrow T, T \rightarrow U, U \rightarrow V$ and $V \rightarrow S$. Let $R = (R1 \text{ and } R2)$ be a decomposition such that $R1 \cap R2 \neq \phi$. The decomposition is

- A. not in $2NF$
- B. in $2NF$ but not $3NF$
- C. in $3NF$ but not in $2NF$
- D. in both $2NF$ and $3NF$

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Answer 

3.5.15 Database Normalization: GATE CSE 2000 | Question: 2.24 [top](#)

<https://gateoverflow.in/671>



Given the following relation instance.

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X	Y	Z
1	4	2
1	5	3
1	6	3
3	2	2

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Which of the following functional dependencies are satisfied by the instance?

- A. $XY \rightarrow Z$ and $Z \rightarrow Y$
- B. $YZ \rightarrow X$ and $Y \rightarrow Z$
- C. $YZ \rightarrow X$ and $X \rightarrow Z$
- D. $XZ \rightarrow Y$ and $Y \rightarrow X$

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Answer 

3.5.16 Database Normalization: GATE CSE 2001 | Question: 2.23 [top](#)

<https://gateoverflow.in/741>



$R(A, B, C, D)$ is a relation. Which of the following does not have a lossless join, dependency preserving $BCNF$ decomposition?

- A. $A \rightarrow B, B \rightarrow CD$
- B. $A \rightarrow B, B \rightarrow C, C \rightarrow D$
- C. $AB \rightarrow C, C \rightarrow AD$
- D. $A \rightarrow BCD$

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Answer 

3.5.17 Database Normalization: GATE CSE 2002 | Question: 1.19 [top](#)

<https://gateoverflow.in/824>



Relation R with an associated set of functional dependencies, F , is decomposed into $BCNF$. The redundancy (arising out of functional dependencies) in the resulting set of relations is

- A. Zero
- B. More than zero but less than that of an equivalent $3NF$ decomposition
- C. Proportional to the size of F^+
- D. Indeterminate

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Answer 

3.5.18 Database Normalization: GATE CSE 2002 | Question: 16 [top](#)

<https://gateoverflow.in/869>



For relation $R=(L, M, N, O, P)$, the following dependencies hold:

$M \rightarrow O, NO \rightarrow P, P \rightarrow L$ and $L \rightarrow MN$

R is decomposed into $R_1 = (L, M, N, P)$ and $R_2 = (M, O)$.

- A. Is the above decomposition a lossless-join decomposition? Explain.
- B. Is the above decomposition dependency-preserving? If not, list all the dependencies that are not preserved.
- C. What is the highest normal form satisfied by the above decomposition?

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Answer

3.5.19 Database Normalization: GATE CSE 2002 | Question: 2.24

<https://gateoverflow.in/854>



Relation R is decomposed using a set of functional dependencies, F , and relation S is decomposed using another set of functional dependencies, G . One decomposition is definitely BCNF, the other is definitely 3NF, but it is not known which is which. To make a guaranteed identification, which one of the following tests should be used on the decompositions? (Assume that the closures of F and G are available).

- A. Dependency-preservation
- B. Lossless-join
- C. BCNF definition
- D. 3NF definition

Answer

3.5.20 Database Normalization: GATE CSE 2002 | Question: 2.25

<https://gateoverflow.in/855>



From the following instance of a relation schema $R(A, B, C)$, we can conclude that:

A	B	C
1	1	1
1	1	0
2	3	2
2	3	2

- A. A functionally determines B and B functionally determines C
- B. A functionally determines B and B does not functionally determine C
- C. B does not functionally determine C
- D. A does not functionally determine B and B does not functionally determine C

Answer

3.5.21 Database Normalization: GATE CSE 2003 | Question: 85

<https://gateoverflow.in/968>



Consider the following functional dependencies in a database.

Date_of_Birth \rightarrow Age	Age \rightarrow Eligibility
Name \rightarrow Roll_number	Roll_number \rightarrow Name
Course_number \rightarrow Course_name	Course_number \rightarrow Instructor
(Roll_number, Course_number) \rightarrow Grade	

The relation (Roll_number, Name, Date_of_birth, Age) is

- A. in second normal form but not in third normal form
- B. in third normal form but not in BCNF
- C. in BCNF
- D. in none of the above

Answer

3.5.22 Database Normalization: GATE CSE 2004 | Question: 50

<https://gateoverflow.in/1046>



The relation scheme Student Performance (name, courseNo, rollNo, grade) has the following functional dependencies:

- name, courseNo, \rightarrow grade
- rollNo, courseNo \rightarrow grade
- name \rightarrow rollNo
- rollNo \rightarrow name

The highest normal form of this relation scheme is

- A. 2NF
- B. 3NF
- C. BCNF
- D. 4NF

gate2004-cse databases database-normalization normal

Answer 

3.5.23 Database Normalization: GATE CSE 2005 | Question: 29, UGCNET-June2015-III: 9 [top](#)

<https://gateoverflow.in/1365>



Which one of the following statements about normal forms is FALSE?

- A. BCNF is stricter than 3NF
- B. Lossless, dependency-preserving decomposition into 3NF is always possible
- C. Lossless, dependency-preserving decomposition into BCNF is always possible
- D. Any relation with two attributes is in BCNF

gate2005-cse databases database-normalization easy ugcnetjune2015iii

Answer 

3.5.24 Database Normalization: GATE CSE 2005 | Question: 78 [top](#)

<https://gateoverflow.in/1401>



Consider a relation scheme $R = (A, B, C, D, E, H)$ on which the following functional dependencies hold: $\{A \rightarrow B, BC \rightarrow D, E \rightarrow C, D \rightarrow A\}$. What are the candidate keys R ?

- A. AE, BE
- B. AE, BE, DE
- C. AEH, BEH, BCH
- D. AEH, BEH, DEH

gate2005-cse databases database-normalization easy

Answer 

3.5.25 Database Normalization: GATE CSE 2006 | Question: 70 [top](#)

<https://gateoverflow.in/1848>



The following functional dependencies are given:

$AB \rightarrow CD, AF \rightarrow D, DE \rightarrow F, C \rightarrow G, F \rightarrow E, G \rightarrow A$

Which one of the following options is false?

- A. $\{CF\}^* = \{ACDEFG\}$
- B. $\{BG\}^* = \{ABCDG\}$
- C. $\{AF\}^* = \{ACDEFG\}$
- D. $\{AB\}^* = \{ABCDG\}$

gate2006-cse databases database-normalization normal

Answer 

3.5.26 Database Normalization: GATE CSE 2007 | Question: 62, UGCNET-June2014-II: 47 [top](#)

<https://gateoverflow.in/1260>



Which one of the following statements is FALSE?

- A. Any relation with two attributes is in BCNF
- B. A relation in which every key has only one attribute is in 2NF
- C. A prime attribute can be transitively dependent on a key in a 3NF relation
- D. A prime attribute can be transitively dependent on a key in a BCNF relation

gate2007-cse databases database-normalization normal ugcnetjune2014ii

Answer

3.5.27 Database Normalization: GATE CSE 2008 | Question: 69 top

<https://gateoverflow.in/492>



Consider the following relational schemes for a library database:

Book (Title, Author, Catalog_no, Publisher, Year, Price)
Collection (Title, Author, Catalog_no)

with the following functional dependencies:

- I. Title Author \rightarrow Catalog_no
- II. Catalog_no \rightarrow Title Author Publisher Year
- III. Publisher Title Year \rightarrow Price

Assume { Author, Title } is the key for both schemes. Which of the following statements is true?

- A. Both Book and Collection are in BCNF
- B. Both Book and Collection are in 3NF only
- C. Book is in 2NF and Collection in 3NF
- D. Both Book and Collection are in 2NF only

gate2008-cse databases database-normalization normal

Answer

3.5.28 Database Normalization: GATE CSE 2009 | Question: 56 top

<https://gateoverflow.in/43474>



Consider the following relational schema:

Suppliers(sid:integer, sname:string, city:string, street:string)

Parts(pid:integer, pname:string, color:string)

Catalog(sid:integer, pid:integer, cost:real)

Assume that, in the suppliers relation above, each supplier and each street within a city has unique name, and (sname, city) forms a candidate key. No other functional dependencies are implied other than those implied by primary and candidate keys. Which one of the following is TRUE about the above schema?

- A. The schema is in BCNF
- B. The schema is in 3NF but not in BCNF
- C. The schema is in 2NF but not in 3NF
- D. The schema is not in 2NF

gate2009-cse databases sql database-normalization normal

Answer

3.5.29 Database Normalization: GATE CSE 2012 | Question: 2 top

<https://gateoverflow.in/34>



Which of the following is TRUE?

- A. Every relation in 3NF is also in BCNF
- B. A relation R is in 3NF if every non-prime attribute of R is fully functionally dependent on every key of R
- C. Every relation in BCNF is also in 3NF
- D. No relation can be in both BCNF and 3NF

Answer 3.5.30 Database Normalization: GATE CSE 2013 | Question: 54 [top](#)<https://gateoverflow.in/1558>

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. $F^=$

$\{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$ is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R .

How many candidate keys does the relation R have?

- A. 3
- B. 4
- C. 5
- D. 6

Answer 3.5.31 Database Normalization: GATE CSE 2013 | Question: 55 [top](#)<https://gateoverflow.in/43290>

Relation R has eight attributes ABCDEFGH. Fields of R contain only atomic values. $F^=$ $\{CH \rightarrow G, A \rightarrow BC, B \rightarrow CFH, E \rightarrow A, F \rightarrow EG\}$ is a set of functional dependencies (FDs) so that F^+ is exactly the set of FDs that hold for R .

The relation R is

- A. in $1NF$, but not in $2NF$.
- B. in $2NF$, but not in $3NF$.
- C. in $3NF$, but not in BCNF.
- D. in BCNF.

Answer 3.5.32 Database Normalization: GATE CSE 2014 Set 1 | Question: 21 [top](#)<https://gateoverflow.in/1788>

Consider the relation scheme $R = (E, F, G, H, I, J, K, L, M, N)$ and the set of functional dependencies

$$\{\{E, F\} \rightarrow \{G\}, \{F\} \rightarrow \{I, J\}, \{E, H\} \rightarrow \{K, L\}, \{K\} \rightarrow \{M\}, \{L\} \rightarrow \{N\}\}$$

on R . What is the key for R ?

- A. $\{E, F\}$
- B. $\{E, F, H\}$
- C. $\{E, F, H, K, L\}$
- D. $\{E\}$

Answer 3.5.33 Database Normalization: GATE CSE 2014 Set 1 | Question: 30 [top](#)<https://gateoverflow.in/1797>

Given the following two statements:

S1: Every table with two single-valued attributes is in $1NF$, $2NF$, $3NF$ and BCNF.

S2: $AB \rightarrow C, D \rightarrow E, E \rightarrow C$ is a minimal cover for the set of functional dependencies $AB \rightarrow C, D \rightarrow E, AB \rightarrow E, E \rightarrow C$.

Which one of the following is **CORRECT**?

- A. S1 is TRUE and S2 is FALSE.
- B. Both S1 and S2 are TRUE.
- C. S1 is FALSE and S2 is TRUE.
- D. Both S1 and S2 are FALSE.

Answer 3.5.34 Database Normalization: GATE CSE 2015 Set 3 | Question: 20 top<https://gateoverflow.in/8420>

Consider the relation $X(P, Q, R, S, T, U)$ with the following set of functional dependencies

$$F = \{ \{P, R\} \rightarrow \{S, T\}, \{P, S, U\} \rightarrow \{Q, R\} \}$$

Which of the following is the trivial functional dependency in F^+ , where F^+ is closure to F ?

- A. $\{P, R\} \rightarrow \{S, T\}$
- B. $\{P, R\} \rightarrow \{R, T\}$
- C. $\{P, S\} \rightarrow \{S\}$
- D. $\{P, S, U\} \rightarrow \{Q\}$

Answer 3.5.35 Database Normalization: GATE CSE 2016 Set 1 | Question: 21 top<https://gateoverflow.in/39637>

Which of the following is NOT a superkey in a relational schema with attributes

V, W, X, Y, Z and primary key

VY ?

- A. $VXYZ$
- B. $VWXXZ$
- C. $VWXY$
- D. $VWXYZ$

Answer 3.5.36 Database Normalization: GATE CSE 2016 Set 1 | Question: 23 top<https://gateoverflow.in/39646>

A database of research articles in a journal uses the following schema.

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, YEAR, PRICE)

The primary key is '(VOLUME, NUMBER, STARTPAGE, ENDPAGE)

and the following functional dependencies exist in the schema.

(VOLUME, NUMBER, STARTPAGE, ENDPAGE) \rightarrow TITLE

(VOLUME, NUMBER) \rightarrow YEAR

(VOLUME, NUMBER, STARTPAGE, ENDPAGE) \rightarrow PRICE

The database is redesigned to use the following schemas

(VOLUME, NUMBER, STARTPAGE, ENDPAGE, TITLE, PRICE)(VOLUME, NUMBER, YEAR)

Which is the weakest normal form that the new database satisfies, but the old one does not?

- A. 1NF
- B. 2NF
- C. 3NF
- D. BCNF

Answer 



The following functional dependencies hold true for the relational schema $R\{V, W, X, Y, Z\}$:

$V \rightarrow W$
 $VW \rightarrow X$
 $Y \rightarrow VX$
 $Y \rightarrow Z$

Which of the following is irreducible equivalent for this set of functional dependencies?

- A. $V \rightarrow W$
 $V \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow Z$
- B. $V \rightarrow W$
 $W \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow Z$
- C. $V \rightarrow W$
 $V \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow X$
 $Y \rightarrow Z$
- D. $V \rightarrow W$
 $W \rightarrow X$
 $Y \rightarrow V$
 $Y \rightarrow X$
 $Y \rightarrow Z$

gate2017-cse-set1

databases

database-normalization

normal

Answer



Consider the following four relational schemas. For each schema, all non-trivial functional dependencies are listed. The **bolded** attributes are the respective primary keys.

Schema I: Registration(**rollno**, courses)

Field 'courses' is a set-valued attribute containing the set of courses a student has registered for.

Non-trivial functional dependency

$\text{rollno} \rightarrow \text{courses}$

Schema II: Registration (**rollno**, **courseid**, email)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid} \rightarrow \text{email}$

$\text{email} \rightarrow \text{rollno}$

Schema III: Registration (**rollno**, **courseid**, marks, grade)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid} \rightarrow \text{marks}, \text{grade}$

$\text{marks} \rightarrow \text{grade}$

Schema IV: Registration (**rollno**, **courseid**, credit)

Non-trivial functional dependencies:

$\text{rollno}, \text{courseid} \rightarrow \text{credit}$

$\text{courseid} \rightarrow \text{credit}$

Which one of the relational schemas above is in 3NF but not in BCNF?

- A. Schema I
 B. Schema II
 C. Schema III
 D. Schema IV

Answer 3.5.39 Database Normalization: GATE CSE 2019 | Question: 32 [top](#)<https://gateoverflow.in/302816>

Let the set of functional dependencies $F = \{QR \rightarrow S, R \rightarrow P, S \rightarrow Q\}$ hold on a relation schema $X = (PQRS)$. X is not in BCNF. Suppose X is decomposed into two schemas Y and Z , where $Y = (PR)$ and $Z = (QRS)$.

Consider the two statements given below.

- I. Both Y and Z are in BCNF
- II. Decomposition of X into Y and Z is dependency preserving and lossless

Which of the above statements is/are correct?

- A. Both I and II
- B. I only
- C. II only
- D. Neither I nor II

Answer 3.5.40 Database Normalization: GATE CSE 2020 | Question: 36 [top](#)<https://gateoverflow.in/333195>

Consider a relational table R that is in $3NF$, but not in BCNF. Which one of the following statements is TRUE?

- A. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a prime attribute.
- B. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a non-prime attribute and X is not a proper subset of any key.
- C. R has a nontrivial functional dependency $X \rightarrow A$, where X is not a superkey and A is a non-prime attribute and X is a proper subset of some key.
- D. A cell in R holds a set instead of an atomic value.

Answer 3.5.41 Database Normalization: GATE CSE 2021 Set 1 | Question: 33 [top](#)<https://gateoverflow.in/357418>

Consider the relation $R(P, Q, S, T, X, Y, Z, W)$ with the following functional dependencies.

$$PQ \rightarrow X; \quad P \rightarrow YX; \quad Q \rightarrow Y; \quad Y \rightarrow ZW$$

Consider the decomposition of the relation R into the constituent relations according to the following two decomposition schemes.

- $D_1 : R = [(P, QS, T); (P, T, X); (Q, Y); (Y, Z, W)]$
- $D_2 : R = [(P, Q, S); (T, X); (Q, Y); (Y, Z, W)]$

Which one of the following options is correct?

- A. D_1 is a lossless decomposition, but D_2 is a lossy decomposition
- B. D_1 is a lossy decomposition, but D_2 is a lossless decomposition
- C. Both D_1 and D_2 are lossless decompositions
- D. Both D_1 and D_2 are lossy decompositions

Answer 3.5.42 Database Normalization: GATE CSE 2021 Set 2 | Question: 40 [top](#)<https://gateoverflow.in/357500>

Suppose the following functional dependencies hold on a relation U with attributes P, Q, R, S , and T :

- $P \rightarrow QR$
- $RS \rightarrow T$

Which of the following functional dependencies can be inferred from the above functional dependencies?

- A. $PS \rightarrow T$
- B. $R \rightarrow T$
- C. $P \rightarrow R$
- D. $PS \rightarrow Q$

gate2021-cse-set2 multiple-selects databases database-normalization

Answer

3.5.43 Database Normalization: GATE IT 2004 | Question: 75 top

<https://gateoverflow.in/3719>



A relation $Empdtl$ is defined with attributes $empcode$ (unique), $name$, $street$, $city$, $state$ and $pincode$. For any $pincode$, there is only one $city$ and $state$. Also, for any given $street$, $city$ and $state$, there is just one $pincode$. In normalization terms, $Empdtl$ is a relation in

- A. $1NF$ only
- B. $2NF$ and hence also in $1NF$
- C. $3NF$ and hence also in $2NF$ and $1NF$
- D. $BCNF$ and hence also in $3NF$, $2NF$ and $1NF$

gate2004-it databases database-normalization normal

Answer

3.5.44 Database Normalization: GATE IT 2005 | Question: 22 top

<https://gateoverflow.in/3767>



A table has fields F_1, F_2, F_3, F_4, F_5 with the following functional dependencies

- $F_1 \rightarrow F_3, F_2 \rightarrow F_4, (F_1 \cdot F_2) \rightarrow F_5$

In terms of Normalization, this table is in

- A. 1 NF
- B. 2 NF
- C. 3 NF
- D. None of these

gate2005-it databases database-normalization easy

Answer

3.5.45 Database Normalization: GATE IT 2005 | Question: 70 top

<https://gateoverflow.in/3833>



In a schema with attributes A, B, C, D and E following set of functional dependencies are given

- $A \rightarrow B$
- $A \rightarrow C$
- $CD \rightarrow E$
- $B \rightarrow D$
- $E \rightarrow A$

Which of the following functional dependencies is NOT implied by the above set?

- A. $CD \rightarrow AC$
- B. $BD \rightarrow CD$
- C. $BC \rightarrow CD$
- D. $AC \rightarrow BC$

gate2005-it databases database-normalization normal

Answer



Consider a relation R with five attributes $V, W, X, Y,$ and Z . The following functional dependencies hold:

$VY \rightarrow W, WX \rightarrow Z,$ and $ZY \rightarrow V$.

Which of the following is a candidate key for R ?

- A. VXZ
- B. VXY
- C. $VWXY$
- D. $VWXYZ$

gate2006-it databases database-normalization normal

Answer



Let $R(A, B, C, D)$ be a relational schema with the following functional dependencies :

$A \rightarrow B, B \rightarrow C, C \rightarrow D$ and $D \rightarrow B$. The decomposition of R into $(A, B), (B, C), (B, D)$

- A. gives a lossless join, and is dependency preserving
- B. gives a lossless join, but is not dependency preserving
- C. does not give a lossless join, but is dependency preserving
- D. does not give a lossless join and is not dependency preserving

gate2008-it databases database-normalization normal

Answer



Let $R(A, B, C, D, E, P, G)$ be a relational schema in which the following functional dependencies are known to hold: $AB \rightarrow CD, DE \rightarrow P, C \rightarrow E, P \rightarrow C$ and $B \rightarrow G$. The relational schema R is

- A. in $BCNF$
- B. in $3NF$, but not in $BCNF$
- C. in $2NF$, but not in $3NF$
- D. not in $2NF$

gate2008-it databases database-normalization normal

Answer



Consider a schema $R(A, B, C, D)$ and functional dependencies $A \rightarrow B$ and $C \rightarrow D$. Then the decomposition of R into $R_1(A, B)$ and $R_2(C, D)$ is

- A. dependency preserving and lossless join
- B. lossless join but not dependency preserving
- C. dependency preserving but not lossless join
- D. not dependency preserving and not lossless join

gate1998 databases ugcnetjune2012iii database-normalization

Answer

Answers: Database Normalization



✓ True is answer: gateoverflow.in

$X \rightarrow Y$ says when X repeats, Y will be also repeat. Since, X is not repeated, Y may or may not repeat.

X	Y
1	2
2	2

👍 30 votes

-- Prashant Singh (47.2k points)

3.5.2 Database Normalization: GATE CSE 1988 | Question: 12i [top ⬆](#)

<https://gateoverflow.in/94398>



✓ 1. AXIOM OF REFLEXIVITY

If $Y \subseteq X$ then $X \rightarrow Y$

2. AXIOM OF AUGMENTATION

If $X \rightarrow Y$ then $XZ \rightarrow YZ$ for any Z

3. AXIOM OF TRANSITIVITY

If $X \rightarrow Y$ and $Y \rightarrow Z$ then $X \rightarrow Z$

👍 12 votes

-- Aashish (1.8k points)

3.5.3 Database Normalization: GATE CSE 1988 | Question: 12iia [top ⬆](#)

<https://gateoverflow.in/94399>



✓ $x \rightarrow z$ (Given)

$\implies xx \rightarrow zx$ (Axiom of augmentation) $\rightarrow (I)$

Also $x \rightarrow y$ (Given)

$\implies xz \rightarrow yz$ (Axiom of augmentation) $\rightarrow (II)$

Using (I) and (II) we get

$xx \rightarrow yz$ (Axiom of transitivity)

$\implies x \rightarrow yz$

👍 9 votes

-- Satbir Singh (21k points)

3.5.4 Database Normalization: GATE CSE 1988 | Question: 12iib [top ⬆](#)

<https://gateoverflow.in/94618>



✓ $x \rightarrow y$ (Given)

$\implies xw \rightarrow yw$ (using axiom of augmentation $A \rightarrow B \implies AX \rightarrow BX$)

also $yw \rightarrow z$ (Given)

$\implies xw \rightarrow z$ (using Axiom of transitivity ($A \rightarrow B$ and $B \rightarrow C$) $\implies A \rightarrow C$)

👍 5 votes

-- Satbir Singh (21k points)

3.5.5 Database Normalization: GATE CSE 1988 | Question: 12iic [top ⬆](#)

<https://gateoverflow.in/94619>



✓ $\because z \subset y$, Trivially $y \rightarrow z$. Now by transitivity, $x \rightarrow y, y \rightarrow z \implies x \rightarrow z$

👍 6 votes

-- Arkaprava Paul (1.9k points)

3.5.6 Database Normalization: GATE CSE 1990 | Question: 2-iv [top ⬆](#)

<https://gateoverflow.in/83977>



✓ Secondary index \implies B-tree

Non-procedural query language \Rightarrow Domain calculus

Closure of a set of attributes \Rightarrow Function dependency

Natural join \Rightarrow Relational algebraic operations

(a) Secondary index	(q) B-tree
(b) Non-procedural query language	(r) Domain calculus
(c) Closure of a set of attributes	(p) Function dependency
(d) Natural join	(s) Relational algebraic operations

👍 10 votes

-- Pankaj Kumar (7.8k points)

3.5.7 Database Normalization: GATE CSE 1990 | Question: 3-ii [top](#)

<https://gateoverflow.in/84054>



A. Transitive functional dependency. Therefore it is not in 3NF

B. 3NF because right side is prime attribute

C. Not in 3NF because let us suppose ABC is a candidate key (you can assume any candidate key with any no of attribute) .
now consider AB \rightarrow non-prime attribute which shows it is not in 3NF

D. involving only prime attribute so the **Right** side should definitely contain only prime attribute. therefore it is in 3NF

so B, D is the answer

Edited on 24th Nov 2020 by Gurdeep saini

👍 10 votes

-- Gurdeep (6.8k points)

3.5.8 Database Normalization: GATE CSE 1994 | Question: 3.6 [top](#)

<https://gateoverflow.in/2492>



✓ False

BCNF decomposition can always be lossless, but it may not be always possible to get a dependency preserving BCNF decomposition.

👍 38 votes

-- Sourav Roy (2.9k points)

3.5.9 Database Normalization: GATE CSE 1995 | Question: 26 [top](#)

<https://gateoverflow.in/2665>



✓ The Candidate Keys are AB and BC .

None of the given functional dependencies are partial. So, the scheme qualifies for 2NF.

There is no transitive dependency. So, the scheme qualifies for 3NF.

All determinants are not Candidate Keys. So, the scheme do not qualify for BCNF.

👍 37 votes

-- Rajarshi Sarkar (27.9k points)

3.5.10 Database Normalization: GATE CSE 1997 | Question: 6.9 [top](#)

<https://gateoverflow.in/2265>



✓ Candidate Key is ab .

Since all a,b,c,d are atomic so the relation is in 1 NF.

Checking the FDs :

$a \rightarrow c$ (Prime derives Non-Prime.)

$b \rightarrow d$ (Prime derives Non-Prime.)

Since, there are partial dependencies it is not in 2NF.

a) Answer 1NF but not 2NF

👍 36 votes

-- Sourav Roy (2.9k points)

3.5.11 Database Normalization: GATE CSE 1998 | Question: 1.34 [top](#)

<https://gateoverflow.in/1671>



✓ 3NF,

because we can always have a 3NF decomposition which is dependency preserving and lossless (not possible for any higher forms).

👍 50 votes

-- Digvijay (44.9k points)

3.5.12 Database Normalization: GATE CSE 1998 | Question: 26 [top](#)

<https://gateoverflow.in/1741>



✓ Since Book_id is the key we have,

- Book_id → Subject_Category_of_book
- Book_id → Name_of_Author
- Book_id → Nationality_of_Author

If we assume no other FD is there (this is not specified in the question), the relation is in BCNF as the LHS of every FD is primary key which is also a super key.

a. 2NF

b. New set of FDs are

- Book_id → Subject_Category_of_book
- Book_id → Name_of_Author
- Book_id → Nationality_of_Author
- Book_id → Book_title
- {Name_of_Author, Book_title} → Nationality_of_Author
- {Name_of_Author, Book_title} → Author_address
- {Name_of_Author, Book_title} → Book_id

One thing to notice here is only the primary key is being changed from Book_id to {Book_title, Name_of_Author}, but Book_id is still a key as based on convention Book_id always determines Book_title. Again if we assume no other FD, the relation is in BCNF as LHS of every FD is a super key. But it is logical to assume the FD

Name_of_Author → Author_address

(won't be valid if two authors have same address and should have been explicit in the question) and this FD is a partial FD on the candidate key {Name_of_Author, Book_title} as Name_of_Author is a part of the key and Author_address is not a key attribute. So, this violates 2NF and relation is now just in 1NF. (Debatable if we can assume FDs)

👍 49 votes

-- Arjun Suresh (332k points)

3.5.13 Database Normalization: GATE CSE 1999 | Question: 1.24 [top](#)

<https://gateoverflow.in/1477>



✓ Answer: B

EC is the key for R. Both E and C are not coming on the right hand side of any functional dependency. So, both of them must be present in any key. Now, with EC and the given FDs, we can derive all other attributes making EC a key.

👍 26 votes

-- Rajarshi Sarkar (27.9k points)

3.5.14 Database Normalization: GATE CSE 1999 | Question: 2.7, UGCNET-June2014-III: 25 [top](#)

<https://gateoverflow.in/1485>



✓ $R_1 \cap R_2 \neq \phi$. This makes the decomposition lossless join, as all the attributes are keys, $R_1 \cap R_2$ will be a key of the decomposed relations (lossless condition says the common attribute must be a key in at least one of the decomposed relation). Now, even the original relation R is in 3NF (even BCNF) as all the attributes are prime attributes (in fact each attribute is a candidate key). Hence, any decomposition will also be in 3NF (even BCNF). Option D.

PS: Decomposition in 3NF means decomposed relations are in 3NF. But when we consider any decomposed relation, we must also include any FD which are being implied by the original relational schema. For example, in a decomposed relation STU , there will be a FD $U \rightarrow S$ as well.

85 votes

-- Arjun Suresh (332k points)

3.5.15 Database Normalization: GATE CSE 2000 | Question: 2.24 [top](#)

<https://gateoverflow.in/671>



✓ (b) is answer.

If $A \rightarrow B$ then for each same value of A , B value should be same. If all the A values are distinct the FD hold irrespective of the B values.

Since all Y values are distinct FDs with Y, YX and YZ on LHS hold. So, option B is correct.

In option A, $Z \rightarrow Y$ is violated as for same Z value we have different Y values. Similarly in C, $X \rightarrow Z$ is violated and in D, $XZ \rightarrow Y$ is violated.

37 votes

-- Aravind (2.8k points)

3.5.16 Database Normalization: GATE CSE 2001 | Question: 2.23 [top](#)

<https://gateoverflow.in/741>



✓ taking up **option A** first :

We have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow B, B \rightarrow CD\}$.

Now we will try to decompose it such that the decomposition is a Lossless Join, Dependency Preserving and new relations thus formed are in BCNF.

We decomposed it to $R_1(A, B)$ and $R_2(B, C, D)$. This decomposition satisfies all three properties we mentioned prior.

taking up **option B** :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow B, B \rightarrow C, C \rightarrow D\}$.

we decomposed it as $R_1(A, B)$, $R_2(B, C)$ and $R_3(C, D)$. This decomposition too satisfies all properties as decomposition in **option A**.

taking up **option D** :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{A \rightarrow BCD\}$.

This set of FDs is equivalent to set = $\{A \rightarrow B, A \rightarrow C, A \rightarrow D\}$ on applying decomposition rule which is derived from Armstrong's Axioms.

we decomposed it as $R_1(A, B)$, $R_2(A, C)$ and $R_3(A, D)$. This decomposition also satisfies all properties as required.

taking up **option C** :

we have, $R(A, B, C, D)$ and the Functional Dependency set = $\{AB \rightarrow C, C \rightarrow AD\}$.

we decompose it as $R_1(A, B, C)$ and $R_2(C, D)$. This preserves all dependencies and the join is lossless too, but the relation R_1 is not in BCNF. In R_1 we keep ABC together otherwise preserving $\{AB \rightarrow C\}$ will fail, but doing so also causes $\{C \rightarrow A\}$ to appear in R_1 . $\{C \rightarrow A\}$ violates the condition for R_1 to be in BCNF as C is not a superkey. Condition that all relations formed after decomposition should be in BCNF is not satisfied here.

We need to identify the **INCORRECT**. Hence mark **option C**.

References



134 votes

-- Amar Vashishth (25.2k points)

(C) is the answer. Because of $AB \rightarrow C$ and $C \rightarrow A$, we cannot have A, B and C together in any BCNF relation- in relation ABC, C is not a super key and $C \rightarrow A$ exists violating BCNF condition. So, we cannot preserve $AB \rightarrow C$ dependency in any decomposition of ABCD.

For (A) we can have AB, BCD, A and B the respective keys

For (B) we can have AB, BC, CD, A, B and C the respective keys

For (D) we can have ABCD, A is key

37 votes

-- Arjun Suresh (332k points)

3.5.17 Database Normalization: GATE CSE 2002 | Question: 1.19 [top](#)

<https://gateoverflow.in/824>



✓ Answer is A.

If a relation schema is in **BCNF** then all redundancy based on functional dependency has been removed, although other types of redundancy may still exist. A relational schema R is in Boyce–Codd normal form if and only if for every one of its dependencies $X \rightarrow Y$, at least one of the following conditions hold:

- $X \rightarrow Y$ is a trivial functional dependency ($Y \subseteq X$)
- X is a super key for schema R
- http://en.wikipedia.org/wiki/Boyce%E2%80%93Codd_normal_form

References



60 votes

-- Priya_das (603 points)

3.5.18 Database Normalization: GATE CSE 2002 | Question: 16 top

<https://gateoverflow.in/869>



✓

A. Yes as $R_1 \cap R_2 = M$ and $M \rightarrow O$

B. NO

From the Dependencies obtained from R_1 and R_2 , we CANNOT infer $NO \rightarrow P$

Mistake That CAN be made: Here we CANNOT apply Pseudo Transitivity Rule using $M \rightarrow O$ & $MN \rightarrow P$ to obtain $NO \rightarrow P$ because the rule says :if $M \rightarrow O$ and $NO \rightarrow P$ then $NM \rightarrow P$ or $MN \rightarrow P$, **But here** we have $M \rightarrow O$ and $MN \rightarrow P$... SO we CANNOT apply the rule here to obtain $NO \rightarrow P$ from it.

C. BCNF

R_1 keys : P, L, MN hence BCNF

R_2 key : M hence BCNF

54 votes

-- Danish (3.4k points)

3.5.19 Database Normalization: GATE CSE 2002 | Question: 2.24 top

<https://gateoverflow.in/854>



✓

A. False. BCNF may or may not satisfy Dependency preservation, 3NF always does. But we can't make any guaranteed decision, regarding BCNF if it satisfies Dependency preservation

B. False. Both are lossless.

C. True. Using this we can always decide between BCNF & 3NF.

D. False. Every BCNF relation is also 3NF trivially.

Answer -> C (& Only C).

58 votes

-- Akash Kanase (36k points)

A. dependency preservation.

in 3NF Dependency always preserved but in BCNF it may or may not be preserved.

For a particular set of FDs it may not differentiate BCNF and 3NF.

B. Lossless join always possible in both BCNF as well as 3NF.

D. 3NF definition also unable to differentiate BCNF & 3NF bcoz every BCNF is trivially 3NF.

C. every 3NF which is not BCNF fails BCNF Definition so it may be used to differentiate which is BCNF & which is 3NF ..

25 votes

-- Digvijay (44.9k points)

3.5.20 Database Normalization: GATE CSE 2002 | Question: 2.25 top

<https://gateoverflow.in/855>



✓

Answer is C.

Generally Normalization is done on the schema itself.

From the relational instance given, we may strike out FD s that do not hold.

e.g. B does not functionally determine C (This is true).

But, we cannot say that A functionally determines B for the entire relation itself. This is because that, $A \rightarrow B$ holds for this instance, but in future there might be some tuples added to the instance that may violate $A \rightarrow B$.

So, overall on the relation we cannot conclude that $A \rightarrow B$, from the relational instance which is just a subset of an entire relation.

👍 70 votes

-- Sourav Roy (2.9k points)

3.5.21 Database Normalization: GATE CSE 2003 | Question: 85 [top](#)

<https://gateoverflow.in/1968>



✓ There are three FDs that are valid from the above set of FDs for the given relation :

1. Date_of_Birth \rightarrow Age
2. Name \rightarrow Roll_number
3. Roll_number \rightarrow Name

Candidate keys for the above are : (Date_of_Birth, Name) and (Date_of_Birth, Roll_number)

Clearly there is partial dependency here (Date_of_Birth \rightarrow Age) and Age is not a prime attribute. So, it is in 1NF only.

Option (D).

👍 58 votes

-- Danish (3.4k points)

3.5.22 Database Normalization: GATE CSE 2004 | Question: 50 [top](#)

<https://gateoverflow.in/1048>



✓ Here candidate keys are,

- name, courseNo
- rollNo, courseNo

That makes name, rollNo, and courseNo prime attributes (part of some candidate key)

Functional dependencies 3 and 4 are not partial FDs.

If a relation schema is not in 2NF, then for some FD $x \rightarrow y$, x should be a **proper subset** of some candidate key and y should be a non-prime attribute.

FDs 3 and 4 are not violating 2NF, because the RHS are prime attributes.

For a relation to be in 3NF, for every FD, $x \rightarrow y$, x should be a super key or y is a prime attribute. For FDs 3 and 4, LHS are not super keys, but RHS are prime attributes. So, they are not violating 3NF.

For a relation to be in BCNF, for every FD, $x \rightarrow y$, x should be super key. This is clearly violated for FDs 3 and 4 and so the relation scheme is not in BCNF and hence not in 4NF also.

Correct option: B.

👍 36 votes

-- rameshbabu (2.6k points)

3.5.23 Database Normalization: GATE CSE 2005 | Question: 29, UGCNET-June2015-III: 9 [top](#)

<https://gateoverflow.in/1365>



✓ Option C is the only FALSE statement.

We can always have a lossless decomposition into BCNF but not always we can have a lossless and dependency preserving decomposition. But this is always possible in the case of 3NF.

Option A is true as the requirement of BCNF required a relation schema to be in 3NF. Actually 3NF allows transitive dependency for prime attributes whereas BCNF does not.

Option D is true as shown below.

Assume the two attributes to be A and B .

Now, we can have three cases:

1. Either A or B is the candidate key but not both. i.e., $A \rightarrow B$ or $B \rightarrow A$. No other FD is possible and LHS of all FDs are superkeys and so BCNF requirement is satisfied.
2. Both A and B are candidate keys. i.e., $A \rightarrow B$ and $B \rightarrow A$. Like in above case BCNF requirement is satisfied.
3. Neither $A \rightarrow B$ nor $B \rightarrow A$ and so AB is the key. So, no other FD is possible and this case also satisfies BCNF requirement.

Thus any relation with 2 attributes is guaranteed to be in BCNF.

Ref: <https://gatecse.in/demystifying-database-normalization/>

References



0 votes

-- Arjun Suresh (332k points)

3.5.24 Database Normalization: GATE CSE 2005 | Question: 78 [top](#)

<https://gateoverflow.in/1401>



- ✓ (d) AEH, BEH, DEH

using the given functional dependencies and looking at the dependent attributes, E and H are not dependent on any. So, they must be part of any candidate key. So, only option is D. If we see the FD's, adding A, B or D to EH do form candidate keys.

34 votes

-- Aravind (2.8k points)

3.5.25 Database Normalization: GATE CSE 2006 | Question: 70 [top](#)

<https://gateoverflow.in/1148>



- ✓ $\{AF\}^* = \{AFDE\}$.

Hence, option C is wrong.

33 votes

-- Sankaranarayanan P.N (8.5k points)

3.5.26 Database Normalization: GATE CSE 2007 | Question: 62, UGCNET-June2014-II: 47 [top](#)

<https://gateoverflow.in/1260>



- ✓ Any relation with two attributes is in BCNF \Rightarrow This is true. It is trivial

A relation in which every key has only one attribute is in 2NF \Rightarrow This is true. As it is not possible to have Partial Functional Dependency !

A prime attribute can be transitively dependent on a key in a 3NF relation \Rightarrow This is true. As For 3NF to be violated we need something like Key \Rightarrow Non Key, Non Key \Rightarrow Non key. 3NF definition says that for functional dependency $x \twoheadrightarrow y$, either x should be key or y should be prime attribute. Then we can have something like Key \Rightarrow Non Key, Non key \Rightarrow Prime Attribute, resulting in Transitive FD on Prime Attribute, still in 3NF.

LHS must be always key, so No Transitive dependency is allowed.

Answer is D.

68 votes

-- Akash Kanase (36k points)

3.5.27 Database Normalization: GATE CSE 2008 | Question: 69 [top](#)

<https://gateoverflow.in/492>



- ✓ Answer: C

It is given that $\{\text{Author, Title}\}$ is the key for both schemas.

The given dependencies are :

- $\{\text{Title, Author}\} \rightarrow \text{Catalog_no}$

- $\text{Catalog_no} \rightarrow \{\text{Title, Author, Publisher, Year}\}$
- $\{\text{Publisher, Title, Year}\} \rightarrow \{\text{Price}\}$

First, let's take schema *Collection* (*Title, Author, Catalog_no*) :

- $\{\text{Title, Author}\} \rightarrow \text{Catalog_no}$

$\{\text{Title, Author}\}$ is a candidate key and hence super key also and by definition of BCNF this is in BCNF.

Now, let's see *Book* (*Title, Author, Catalog_no, Publisher, Year, Price*):

- $\{\text{Title, Author}\}^+ \rightarrow \{\text{Title, Author, Catalog_no, Publisher, Year, Price}\}$
- $\{\text{Catalog_no}\}^+ \rightarrow \{\text{Title, Author, Publisher, Year, Price, Catalog_no}\}$

So candidate keys are : $\text{Catalog_no}, \{\text{Title, Author}\}$

But in the given set of dependencies we have $\{\text{Publisher, Title, Year}\} \rightarrow \text{Price}$, which has a Transitive Dependency. **So, Book is not in 3NF but is in 2NF.**

👍 45 votes

-- worst_engineer (2.8k points)

3.5.28 Database Normalization: GATE CSE 2009 | Question: 56 top

<https://gateoverflow.in/43474>



✓ The non-trivial FDs are

1. $(sname, city) \rightarrow street$
2. $sid \rightarrow street$
3. $(sname, city) \rightarrow sid$
4. $sid \rightarrow sname$
5. $sid \rightarrow city$

For all these, LHS is a super key and hence BCNF condition is satisfied. But we have some more dependencies here:

! "each supplier and each street within a city has unique name"

This basically means each supplier in a city has unique name making $(sname, city)$ determine sid and hence making it a candidate key. Each street within a city also has a unique name and so $(street, city)$ is also a candidate key. Even then with all 3 candidate keys (for Suppliers schema), for any FD, the LHS is a super key here, and hence the relation schema (for other two relations it is straight forward) is in BCNF.

<http://db.grussell.org/section009.html>

Correct Answer: A

References



👍 62 votes

-- Arjun Suresh (332k points)

3.5.29 Database Normalization: GATE CSE 2012 | Question: 2 top

<https://gateoverflow.in/34>



✓ (C) Every relation in BCNF is also in 3NF. Straight from definition of BCNF.

👍 31 votes

-- Arjun Suresh (332k points)

3.5.30 Database Normalization: GATE CSE 2013 | Question: 54 top

<https://gateoverflow.in/1558>



✓ Here, we can see that D is not part of any $FD's$, hence D must be part of the candidate key.

Now $D^+ = \{D\}$.

Hence, we have to add A, B, C, E, F, G, H to D and check which of them are Candidate keys of size 2.

We can proceed as:

$AD^+ = \{A, B, C, D, E, F, G, H\}$

Similarly we see BD^+ , ED^+ and FD^+ also gives us all the attributes. Hence, AD, BD, ED, FD are definitely the candidate keys.

But CD^+ , GD^+ and HD^+ doesn't give all the attributes hence, CD, GD and HD are not candidate keys.

Now we need to check the candidate keys of size 3. Since AD, BD, ED, FD are all candidate keys hence we can't find candidate keys by adding elements to them as they will give us superkeys as they are already minimal. Hence, we have to proceed with CD, GD and HD .

Also, we can't add any of A, B, E, F to CD, GD, HD as they will again give us superset of AD, BD, ED, FD .

Hence, we can only add among C, G, H to CD, GD, HD .

Adding C to GD and HD we get GCD, HCD . Taking closure and we will see they are not candidate keys.

Adding H to GD we get GHD which is also not a candidate key. (no more options with 3 attributes possible)

Now we need to check for candidate keys with 4 attributes. Since, only remaining options are CGH and we have to add D only possible key of size 4 is $CGHD$ whose closure also doesn't give us all of the attributes in the relation (All possible options covered)

Hence, no of candidate keys are 4 : AD, BD, ED, FD .

Correct Answer: B

👍 32 votes

-- Indranil Maji (537 points)

3.5.31 Database Normalization: GATE CSE 2013 | Question: 55 [top](#)

<https://gateoverflow.in/43290>



✓ Here, candidate keys are AD, BD, ED and FD .

Partial dependency exists $A \rightarrow BC, B \rightarrow CFH$ and $F \rightarrow EG$ etc. In the following FDs .

For example partial dependency $A \rightarrow C$ exists in $A \rightarrow BC$ and $B \rightarrow C$ and $B \rightarrow H$ in $B \rightarrow CFH$. etc.

So, given relation is in $1NF$, but not in $2NF$.

Correct Answer: A

👍 42 votes

-- Manoj Kumar (26.7k points)

3.5.32 Database Normalization: GATE CSE 2014 Set 1 | Question: 21 [top](#)

<https://gateoverflow.in/1788>



✓ Since E, F, H cannot be derived from anything else E, F, H should be there in key.

Using Find $\{EFH\}^+$, it contains all the attributes of the relation.

Hence, it is key.

Correct Answer: B

👍 41 votes

-- Sankaranarayanan P.N (8.5k points)

3.5.33 Database Normalization: GATE CSE 2014 Set 1 | Question: 30 [top](#)

<https://gateoverflow.in/1797>



✓ (A) S1 is TRUE and S2 is FALSE.

A relation with 2 attributes is always in BCNF

The two sets of functional dependencies are not the same. We can not derive $AB \rightarrow E$ from the 1st set

👍 40 votes

-- Aravind (2.8k points)

3.5.34 Database Normalization: GATE CSE 2015 Set 3 | Question: 20 [top](#)

<https://gateoverflow.in/8420>



✓ Option C is correct because $\{P, S\} \rightarrow \{S\}$

for trivial FD, if $X \rightarrow Y$ then Y must be a subset of X and for non trivial FD $X \cap Y = \emptyset$. and here $\{S\}$ is subset of $\{P, S\}$.

PS: Trivial means something which is always there. An attribute set always determines any of the component attributes and this is always true irrespective of the relation instance. Hence, this FD becomes trivial.

👍 54 votes

-- Anoop Sonkar (4.1k points)

3.5.35 Database Normalization: GATE CSE 2016 Set 1 | Question: 21 [top](#)

<https://gateoverflow.in/39637>



- ✓ Any superset of a key is also a superkey from definition of a superkey.
So, answer is B.

! a superkey can be defined as a set of attributes of a [relation schema](#) upon which all attributes of the schema are [functionally dependent](#)

References



👍 39 votes

-- Abhilash Panicker (7.6k points)

3.5.36 Database Normalization: GATE CSE 2016 Set 1 | Question: 23 [top](#)

<https://gateoverflow.in/39646>



- ✓ The actual design is in $1NF$ coz there are partial dependencies in the given FD set so the original DB design is in $1NF$ but not $2NF$.

Now, the new design is removing all the partial dependencies so its in $2NF$

So, the weakest form that the new schema satisfies that the old one couldn't is $2NF$ answer is B .

👍 48 votes

-- Bharani Viswas (611 points)

3.5.37 Database Normalization: GATE CSE 2017 Set 1 | Question: 16 [top](#)

<https://gateoverflow.in/118296>



- ✓ In option B and option D there is a dependency $W \rightarrow X$ which is not implied by the question and hence they are definitely wrong.

Now in option C) $Y \rightarrow X$ can be removed as it can be implied as $Y \rightarrow V$ and $V \rightarrow X$.

Hence, option (A) is correct.

👍 52 votes

-- sriv_shubham (2.8k points)

3.5.38 Database Normalization: GATE CSE 2018 | Question: 42 [top](#)

<https://gateoverflow.in/204116>



- ✓ Answer is (B) .

rollno, courseid \rightarrow email

(rollno, courseid is a super key,so it comes under $3NF$ as well as $BCNF$).

email \rightarrow rollno

Here, email is not a key though but rollno comes under prime-attribute.Hence it's in $3NF$ but not $BCNF$.

👍 25 votes

-- Baljit kaur (1k points)



- ✓ Y is in BCNF because binary attribute.
 Z is not in BCNF because $S \rightarrow Q$ is in Z and S is not Super key.

Dependency Preserving:

$QR \rightarrow S$ in Z

$R \rightarrow P$ is in Y

$S \rightarrow Q$ is in Z

So it is dependency preserving.

Lossless:

$Y \cap Z = R$ which is key of Y .

Lossless it is.

Only 2nd is correct.

So Option C is the answer

👍 28 votes

-- Digvijay (44.9k points)



- ✓ In 3NF where functional dependency is of type $X \rightarrow Y$

X can be the super key or Y can be the prime attribute

Whereas in BCNF where functional dependency is of type $X \rightarrow Y$

X should be super key (BCNF is more strict compared to 3NF)

- Option (C) says it has a partial dependency (not even 2NF).
- Option (D) multiple values in a cell. i.e not atomic (not even 1NF).
- Option (B) says X is not a super key and Y is not a prime attribute. Therefore not 3NF.

Ans (A): Says X is not a super key but Y is a prime attribute. Satisfies one of the conditions of the 3NF formal definition. As X is not a Super Key it is not in BCNF.

👍 15 votes

-- Srinivas_Reddy_Kotla (775 points)



- ✓ Decomposition removes redundancy from the database. it is lossless if it's possible to reconstruct the table from the given set of decomposition tables using natural join.

Decomposition of a relation R into R_1, R_2 is a lossless-join decomposition if at least one of the following functional dependencies are in F^+ :

1. $((R_1 \cap R_2) \rightarrow (R_1 - R_2))$ is in F^+ or
2. $((R_1 \cap R_2) \rightarrow (R_2 - R_1))$ is in F^+

- Decomposition is lossless iff $R_1 \bowtie R_2 = R$

$D_1 : R = [r_1(PQST), r_2(PTX), r_3(QY), r_4(YZW)]$

$\implies r_1 \cap r_2 = (PT)^+ = PTYXZW$ which is superkey, we can combine them.

So new table is $x_1 = (PQSTX)$

In the same way; $r_3 \cap r_4 = Y^+ = YZW$

which is SK, and so we can merge them.

Thus $x_2 = (QYZW)$

Now $x_1 \cap x_2 = Q^+ = QYZW$ which is SK.

So we can get original table $(PQSTXYZW)$

So given decomposition D_1 is lossless join decomposition.

Similarly we can check for D_2

$$D_2 : R = [r_1(PQS), r_2(TX), r_3(QY), r_4(YZW)]$$

$\implies r_3 \cap r_4 = Y^+ = YZW$, is Sk we can merge them.

So new table will be $x_1 = (QYZW)$

Similarly $x_1 \cap r_1 = Q^+ = QYZW$ is also Sk, we can combine them. new table will be $x_2 = (PQSYZW)$

Now $x_2 \cap r_2$ is not superkey. no common attribute is present between them. We can try any other order of combining the relations and none of them will satisfy the lossless decomposition condition. Hence it is lossy decomposition.

\therefore decomposition D_2 is lossy decomposition.

Option A is correct.

Ref: [lossless-join-and-dependency-preserving-decomposition](#)

References



3 votes

-- Hira (14.1k points)

3.5.42 Database Normalization: GATE CSE 2021 Set 2 | Question: 40 [top](#)

<https://gateoverflow.in/357500>



✓ Option A: $(PS)^+ = P, Q, R, S, T$ so $PS \rightarrow T$ holds.

Option B: $(R)^+ = R$ so $R \rightarrow T$ doesn't hold.

Option C: $(P)^+ = P, Q, R$ so $P \rightarrow R$ holds.

Option D: $(PS)^+ = P, Q, R, S, T$ so $PS \rightarrow Q$ holds

3 votes

-- zxy123 (2.8k points)

3.5.43 Database Normalization: GATE IT 2004 | Question: 75 [top](#)

<https://gateoverflow.in/3719>



✓ It is in $2nf$ - for $2NF$ all non prime attribute should be fully functionally dependent on key. Here key is empcode and contains only one attribute hence no partial dependency. But there is transitive dependency in this (pincode \rightarrow city, state). So it is not in $3NF$.

answer: B

51 votes

-- Sankaranarayanan P.N (8.5k points)

3.5.44 Database Normalization: GATE IT 2005 | Question: 22 [top](#)

<https://gateoverflow.in/3833>



✓ Answer is A 1NF

Key is $\{F_1, F_2\}$

$F_1 \rightarrow F_3, F_2 \rightarrow F_4$ are partial dependencies (a proper subset of candidate key determining a non-key attribute) thus violating 2 NF requirement.

35 votes

-- K Rajashekar (997 points)

3.5.45 Database Normalization: GATE IT 2005 | Question: 70 [top](#)

<https://gateoverflow.in/3833>



✓ Answer is (B).

Apply membership test for all the given Functional Dependencies.

- $CD \rightarrow AC$
 $CD^+ = CDEAB$

$$2. BD \rightarrow CD \\ BD^+ = BD$$

i.e. BD cannot derive CD and hence is not implied.
Similarly do for rest two.

👍 39 votes

-- Gate Keeda (15.9k points)

3.5.46 Database Normalization: GATE IT 2006 | Question: 60 [top](#)

<https://gateoverflow.in/3604>



✓ As we can see attributes X and Y do not appear in the RHS of any FD and so they need to be part of any super/candidate key. So, candidate keys are: VXY, WXY, ZXY as these three **can determine any other** attribute where as a **proper subset** of any of them cannot determine all other attributes.

VXZ is not a super key as Y is not there where as $VWXY$ and $VWXYZ$ are super keys but since their proper subsets are also super keys they are not candidate keys.

Answer is **B**.

👍 27 votes

-- Pooja Palod (24.1k points)

3.5.47 Database Normalization: GATE IT 2008 | Question: 61 [top](#)

<https://gateoverflow.in/3371>



✓ Option A.

$(A, B)(B, C)$ – common attribute is B and due to $B \rightarrow C$, B is a key for (B, C) and hence ABC can be losslessly decomposed into (A, B) and (B, C) .

$(A, B, C)(B, D)$, common attribute is B and $B \rightarrow D$ is a FD (via $B \rightarrow C, C \rightarrow D$), and hence, B is a key for (B, D) . So, decomposition of (A, B, C, D) into $(A, B, C)(B, D)$ is lossless.

Thus the given decomposition is lossless.

The given decomposition is also dependency preserving as the dependencies $A \rightarrow B$ is present in (A, B) , $B \rightarrow C$ is present in (B, C) , $D \rightarrow B$ is present in (B, D) and $C \rightarrow D$ is indirectly present via $C \rightarrow B$ in (B, C) and $B \rightarrow D$ in (B, D) .

<http://www.sztaki.hu/~fodroczi/dbs/dep-pres-own.pdf>

References



👍 112 votes

-- Arjun Suresh (332k points)

3.5.48 Database Normalization: GATE IT 2008 | Question: 62 [top](#)

<https://gateoverflow.in/3372>



✓ Answer: D

Here AB is the candidate key and $B \rightarrow G$ is a partial dependency. So, R is not in $2NF$.

👍 41 votes

-- Rajarshi Sarkar (27.9k points)

3.5.49 Database Normalization: GATE2001-1.23, UGCNET-June2012-III: 18 [top](#)

<https://gateoverflow.in/716>



✓ Answer is **C**.

Here, no common attribute in R_1 and R_2 , therefore lossy join will be there.

and both the dependencies are preserved in composed relations so, dependency preserving.

👍 30 votes

-- jayendra (6.7k points)

A decomposition $\{R_1, R_2\}$ is a lossless-join decomposition if $R_1 \cap R_2 \rightarrow R_1$ (**R1 should be key**) or $R_1 \cap R_2 \rightarrow R_2$ (**R2 should be key**) but $(A,B) \cap (C,D) = \emptyset$ so lossy join

FD:1 $A \rightarrow B$

FD:2 $C \rightarrow D$

$R_1(A,B)$ have all attributes of FD1 and $R_2(C,D)$ have all attributes of FD2 so ,dependency preserved decomposition

Reference : - question no. 8.1 Korth <http://codex.cs.yale.edu/avi/db-book/db6/practice-exer-dir/8s.pdf>

References



👍 12 votes

-- Rishi yadav (9k points)

3.6

Er Diagram (10) top 9

3.6.1 Er Diagram: GATE CSE 2005 | Question: 75 top 9

<https://gateoverflow.in/1398>



Let E_1 and E_2 be two entities in an E/R diagram with simple-valued attributes. R_1 and R_2 are two relationships between E_1 and E_2 , where R_1 is one-to-many and R_2 is many-to-many. R_1 and R_2 do not have any attributes of their own. What is the minimum number of tables required to represent this situation in the relational model?

- A. 2
- B. 3
- C. 4
- D. 5

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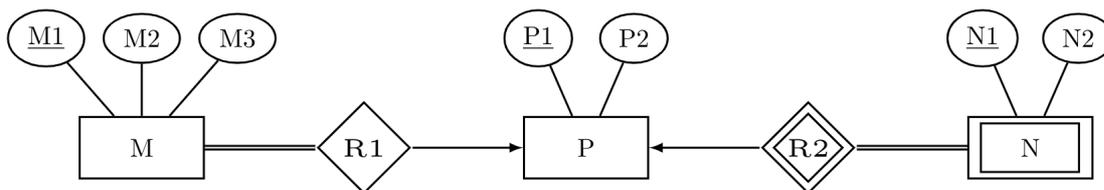
Answer 🗣️

3.6.2 Er Diagram: GATE CSE 2008 | Question: 82 top 9

<https://gateoverflow.in/390>



Consider the following ER diagram



The minimum number of tables needed to represent M, N, P, R_1, R_2 is

- A. 2
- B. 3
- C. 4
- D. 5

gate2008-cse databases er-diagram normal

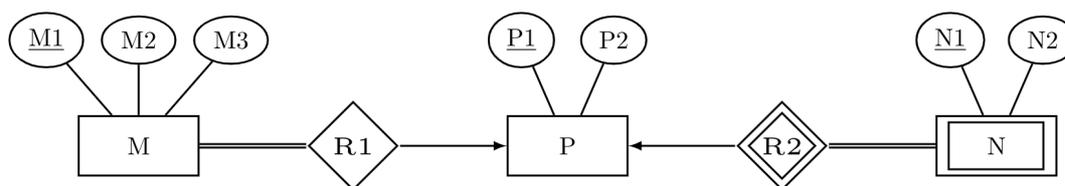
Answer 🗣️

3.6.3 Er Diagram: GATE CSE 2008 | Question: 83 top 9

<https://gateoverflow.in/87025>



Consider the following ER diagram



The minimum number of tables needed to represent $M, N, P, R1, R2$ is

Which of the following is a correct attribute set for one of the tables for the minimum number of tables needed to represent $M, N, P, R1, R2$?

- A. $M1, M2, M3, P1$
- B. $M1, P1, N1, N2$
- C. $M1, P1, N1$
- D. $M1, P1$

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goclasses.in

tests.gatecse.in

Answer

3.6.4 Er Diagram: GATE CSE 2012 | Question: 14 [top](#)

<https://gateoverflow.in/46>



Given the basic ER and relational models, which of the following is **INCORRECT**?

- A. An attribute of an entity can have more than one value
- B. An attribute of an entity can be composite
- C. In a row of a relational table, an attribute can have more than one value
- D. In a row of a relational table, an attribute can have exactly one value or a NULL value

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Answer

3.6.5 Er Diagram: GATE CSE 2015 Set 1 | Question: 41 [top](#)

<https://gateoverflow.in/8309>



Consider an Entity-Relationship (ER) model in which entity sets E_1 and E_2 are connected by an $m : n$ relationship R_{12} . E_1 and E_3 are connected by a $1 : n$ (1 on the side of E_1 and n on the side of E_3) relationship R_{13} .

E_1 has two single-valued attributes a_{11} and a_{12} of which a_{11} is the key attribute. E_2 has two single-valued attributes a_{21} and a_{22} of which a_{21} is the key attribute. E_3 has two single-valued attributes a_{31} and a_{32} of which a_{31} is the key attribute. The relationships do not have any attributes.

If a relational model is derived from the above ER model, then the minimum number of relations that would be generated if all relations are in 3NF is _____.

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Answer

3.6.6 Er Diagram: GATE CSE 2017 Set 2 | Question: 17 [top](#)

<https://gateoverflow.in/118157>



An ER model of a database consists of entity types A and B . These are connected by a relationship R which does not have its own attribute. Under which one of the following conditions, can the relational table for R be merged with that of A ?

- A. Relationship R is one-to-many and the participation of A in R is total
- B. Relationship R is one-to-many and the participation of A in R is partial
- C. Relationship R is many-to-one and the participation of A in R is total
- D. Relationship R is many-to-one and the participation of A in R is partial

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Answer



In an Entity-Relationship (ER) model, suppose R is a many-to-one relationship from entity set E_1 to entity set E_2 . Assume that E_1 and E_2 participate totally in R and that the cardinality of E_1 is greater than the cardinality of E_2 .

Which one of the following is true about R ?

- A. Every entity in E_1 is associated with exactly one entity in E_2
- B. Some entity in E_1 is associated with more than one entity in E_2
- C. Every entity in E_2 is associated with exactly one entity in E_1
- D. Every entity in E_2 is associated with at most one entity in E_1

gate2018-cse databases er-diagram normal

Answer



Which one of the following is used to represent the supporting many-one relationships of a weak entity set in an entity-relationship diagram?

- A. Diamonds with double/bold border
- B. Rectangles with double/bold border
- C. Ovals with double/bold border
- D. Ovals that contain underlined identifiers

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Answer



Consider the following entity relationship diagram (ERD), where two entities E_1 and E_2 have a relation R of cardinality 1:m.

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The attributes of E_1 are A_{11} , A_{12} and A_{13} where A_{11} is the key attribute. The attributes of E_2 are A_{21} , A_{22} and A_{23} where A_{21} is the key attribute and A_{23} is a multi-valued attribute. Relation R does not have any attribute. A relational database containing minimum number of tables with each table satisfying the requirements of the third normal form ($3NF$) is designed from the above ERD . The number of tables in the database is

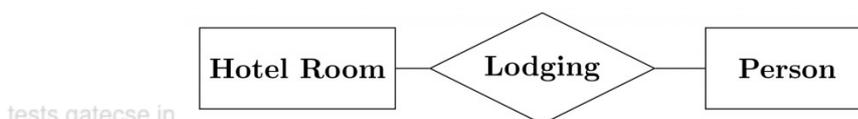
- A. 2
- B. 3
- C. 5
- D. 4

gate2004-it databases er-diagram normal

Answer



Consider the entities 'hotel room', and 'person' with a many to many relationship 'lodging' as shown below:



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If we wish to store information about the rent payment to be made by person (s) occupying different hotel rooms, then this information should appear as an attribute of

- A. Person
- B. Hotel Room
- C. Lodging
- D. None of these

gate2005-it databases er-diagram easy

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Answer 

Answers: Er Diagram

3.6.1 Er Diagram: GATE CSE 2005 | Question: 75 top 5

<https://gateoverflow.in/1398>



- ✓ We need a separate table for many-to-many relation. one-to-many relation doesn't need a separate table and can be handled using a foreign key. So, answer is **B** - 3 tables.

Reference: [MIT notes](#).

References



 42 votes

-- Arjun Suresh (332k points)

3.6.2 Er Diagram: GATE CSE 2008 | Question: 82 top 5

<https://gateoverflow.in/390>



- ✓ First strong entity types are made to tables. So, we get two tables M and P .

I assume $R1$ is $1 : 1$ or $1 : n$ as that would minimize the number of tables as asked in question.

Now participation of M in $R1$ is total (indicated by double arrow) meaning every entity of M participate in $R1$. Since $R1$ is not having an attribute, we can simple add the primary key of P to the table M and add a foreign key reference to M . This handles $R1$ and we don't need an extra table. So, M becomes $M1, M2, M3, P1$.

N here is a [weak entity](#) weakly related to P . So, we form a new table N , and includes the primary key of $P(P1)$ as foreign key reference. Now $(P1, N1)$ becomes the primary key of N .

Thus we get 3 tables.

$M : M1, M2, M3, P1$ - $M1$ primary key, $P1$ references P

$P : P1, P2$ - $P1$ primary key

$N : P1, N1, N2$ - $(P1, N1)$ primary key, $P1$ references P .

So, answers is **B**.

References



 88 votes

-- Arjun Suresh (332k points)

3.6.3 Er Diagram: GATE CSE 2008 | Question: 83 top 5

<https://gateoverflow.in/87025>



- ✓ First strong entity types are made to tables. So, we get two tables M and P .

I assume $R1$ is $1 : 1$ or $1 : n$ as that would minimize the number of tables as asked in question.

Now participation of M in $R1$ is total (indicated by double arrow) meaning every entity of M participate in $R1$. Since $R1$ is not having an attribute, we can simple add the primary key of P to the table M and add a foreign key reference to M . This handles $R1$ and we don't need an extra table. So, M becomes $\{M1, M2, M3, P1\}$.

N here is a [weak entity](#) weakly related to P . So, we form a new table N , and includes the primary key of $P(P1)$ as foreign key reference. Now $(P1, N1)$ becomes the primary key of N .

Thus we get 3 tables.

M : $M1, M2, M3, P1$ - $M1$ primary key, $P1$ references P

P : $P1, P2$ - $P1$ primary key

N : $P1, N1, N2$ - $(P1, N1)$ primary key, $P1$ references P .

So, answers is A.

References



👍 28 votes

-- Arjun Suresh (332k points)

3.6.4 Er Diagram: GATE CSE 2012 | Question: 14 [top](#) [👤](#)

<https://gateoverflow.in/46>



- ✓ (C) is incorrect as a relational table requires that, in a row, an attribute can have exactly one value or NULL value.

👍 39 votes

-- Arjun Suresh (332k points)

3.6.5 Er Diagram: GATE CSE 2015 Set 1 | Question: 41 [top](#) [👤](#)

<https://gateoverflow.in/8309>



- ✓ Answer is 4. The relations are as shown:

$\langle a_{11}, a_{12} \rangle$ for E_1

$\langle a_{21}, a_{22} \rangle$ for E_2

$\langle a_{31}, a_{32}, a_{11} \rangle$ for E_3 and $E_1 - E_3$ relationship

$\langle a_{11}, a_{21} \rangle$ for $m : n$ relationship $E_1 - E_2$

We cannot combine any relation here as it will give rise to partial functional dependency and thus violate 3NF.

Reference: [MIT notes](#)

References



👍 73 votes

-- Arjun Suresh (332k points)

3.6.6 Er Diagram: GATE CSE 2017 Set 2 | Question: 17 [top](#) [👤](#)

<https://gateoverflow.in/118157>



- ✓ The relation table for R should always be merged with the entity that has total participation and relationship should be many to one.

Answer is C.

👍 36 votes

-- Arnabi Bej (5.8k points)

3.6.7 Er Diagram: GATE CSE 2018 | Question: 11 [top](#) [👤](#)

<https://gateoverflow.in/204085>



- ✓ Since it is a **many to one relationship** from $E1$ to $E2$, therefore:

1. No entity in $E1$ can be related to more than one entity in $E2$. (hence B is incorrect)
2. An entity in $E2$ can be related to more than one entity in $E1$. (hence C and D are incorrect).

Option (A) is correct: Every entity in E1 is associated with exactly one entity in E2.

37 votes

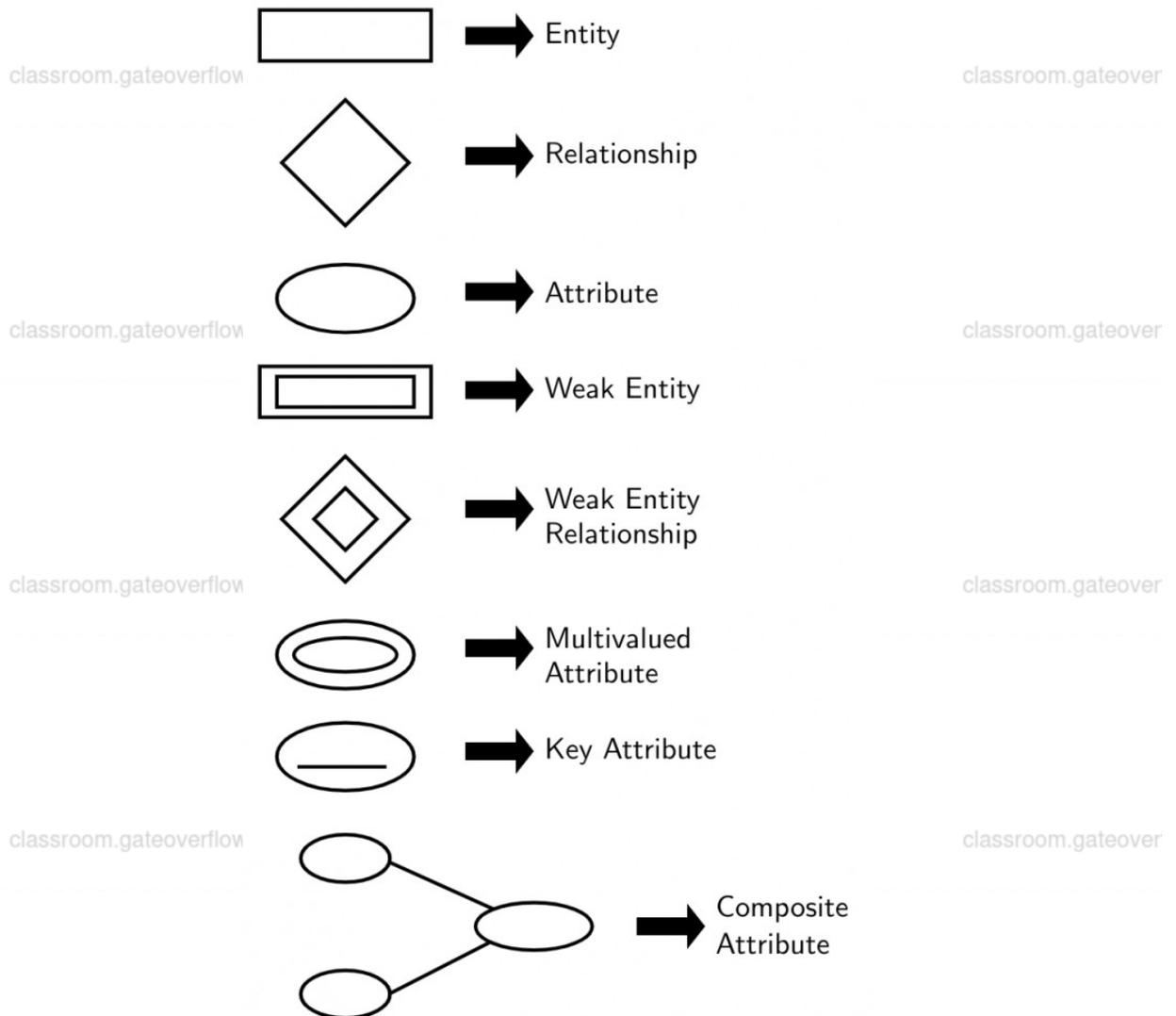
-- Aakanchha (471 points)

3.6.8 Er Diagram: GATE CSE 2020 | Question: 14 top

<https://gateoverflow.in/333217>



✓ Answer : A



Weak entity set is represented by Rectangles with double/bold border.

13 votes

-- Prashant Singh (47.2k points)

3.6.9 Er Diagram: GATE IT 2004 | Question: 73 top

<https://gateoverflow.in/3717>



✓ We need just two tables for 1NF.

T1: {A11, A12, A13}

T2: {A21, A22, A23, A11}

A23 being multi-valued, A21, A23 becomes the key for T2 as we need to repeat multiple values corresponding to the multi-valued attribute to make it 1NF. But, this causes partial FD $A21 \rightarrow A22$ and makes the table not in 2NF. In order to make the table in 2NF, we have to create a separate table for multi-valued attribute. Then we get

T1 : {A11, A12, A13} – key is A11

T2 : {A21, A22, A11} – key is A21

$T3 : \{A21, A23\}$ — key is $\{A21, A23\}$

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Here, all determinants of all FDs are keys and hence the relation is in BCNF and so 3NF also. So, we need minimum 3 tables.

Correct Answer: B

👍 98 votes

-- Arjun Suresh (332k points)

3.6.10 Er Diagram: GATE IT 2005 | Question: 21 top

https://gateoverflow.in/3766



✓ Since it is many to many, rent cannot be an attribute of room or person entities alone. If depending on number of persons sharing a room the rent for each person for the room will be different. Otherwise rent can be attribute of room. hence i go for attribute of Lodging.

Correct Answer: C

👍 47 votes

-- Sankaranarayanan P.N (8.5k points)

3.7

Indexing (11) top

3.7.1 Indexing: GATE CSE 1989 | Question: 4-xiv top

https://gateoverflow.in/8828



For secondary key processing which of the following file organizations is preferred? Give a one line justification:

- A. Indexed sequential file organization.
- B. Two-way linked list.
- C. Inverted file organization.
- D. Sequential file organization.

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gate1989 normal databases indexing descriptive

Answer

3.7.2 Indexing: GATE CSE 1990 | Question: 10b top

https://gateoverflow.in/8591



One giga bytes of data are to be organized as an indexed-sequential file with a uniform blocking factor 8. Assuming a block size of 1 Kilo bytes and a block referencing pointer size of 32 bits, find out the number of levels of indexing that would be required and the size of the index at each level. Determine also the size of the master index. The referencing capability (fanout ratio) per block of index storage may be considered to be 32.

gate1990 databases indexing descriptive

Answer

3.7.3 Indexing: GATE CSE 1993 | Question: 14 top

https://gateoverflow.in/2311



An ISAM (indexed sequential) file consists of records of size 64 bytes each, including key field of size 14 bytes. An address of a disk block takes 2 bytes. If the disk block size is 512 bytes and there are 16K records, compute the size of the data and index areas in terms of number blocks. How many levels of tree do you have for the index?

gate1993 databases indexing normal descriptive

Answer

3.7.4 Indexing: GATE CSE 1998 | Question: 1.35 top

https://gateoverflow.in/1672



There are five records in a database.

Name	Age	Occupation	Category
Rama	27	CON	A
Abdul	22	ENG	A
Jennifer	28	DOC	B
Maya	32	SER	D
Dev	24	MUS	C

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There is an index file associated with this and it contains the values 1, 3, 2, 5 and 4. Which one of the fields is the index built from?

- A. Age
- B. Name
- C. Occupation
- D. Category

gate1998 databases indexing normal

Answer

3.7.5 Indexing: GATE CSE 2008 | Question: 16, ISRO2016-60 [top](#)

<https://gateoverflow.in/414>



A clustering index is defined on the fields which are of type

- A. non-key and ordering
- B. non-key and non-ordering
- C. key and ordering
- D. key and non-ordering

gate2008-cse easy databases indexing isro2016

Answer

3.7.6 Indexing: GATE CSE 2008 | Question: 70 [top](#)

<https://gateoverflow.in/259>



Consider a file of 16384 records. Each record is 32 bytes long and its key field is of size 6 bytes. The file is ordered on a non-key field, and the file organization is unspanned. The file is stored in a file system with block size 1024 bytes, and the size of a block pointer is 10 bytes. If the secondary index is built on the key field of the file, and a multi-level index scheme is used to store the secondary index, the number of first-level and second-level blocks in the multi-level index are respectively

- A. 8 and 0
- B. 128 and 6
- C. 256 and 4
- D. 512 and 5

gate2008-cse databases indexing normal

Answer

3.7.7 Indexing: GATE CSE 2011 | Question: 39 [top](#)

<https://gateoverflow.in/2141>



Consider a relational table r with sufficient number of records, having attributes A_1, A_2, \dots, A_n and let $1 \leq p \leq n$. Two queries Q_1 and Q_2 are given below.

- $Q_1 : \pi_{A_1, \dots, A_p} (\sigma_{A_p=c} (r))$ where c is a constant
- $Q_2 : \pi_{A_1, \dots, A_p} (\sigma_{c_1 \leq A_p \leq c_2} (r))$ where c_1 and c_2 are constants.

The database can be configured to do ordered indexing on A_p or hashing on A_p . Which of the following statements is **TRUE**?

- A. Ordered indexing will always outperform hashing for both queries
- B. Hashing will always outperform ordered indexing for both queries
- C. Hashing will outperform ordered indexing on Q_1 , but not on Q_2
- D. Hashing will outperform ordered indexing on Q_2 , but not on Q_1

gate2011-cse databases indexing normal

Answer

3.7.8 Indexing: GATE CSE 2013 | Question: 15 [top](#)

<https://gateoverflow.in/1437>



An index is clustered, if

- A. it is on a set of fields that form a candidate key
- B. it is on a set of fields that include the primary key
- C. the data records of the file are organized in the same order as the data entries of the index

D. the data records of the file are organized not in the same order as the data entries of the index

gate2013-cse databases indexing normal

Answer

3.7.9 Indexing: GATE CSE 2015 Set 1 | Question: 24 top 5

https://gateoverflow.in/8222



A file is organized so that the ordering of the data records is the same as or close to the ordering of data entries in some index. Than that index is called

- A. Dense
- B. Sparse
- C. Clustered
- D. Unclustered

gate2015-cse-set1 databases indexing easy

Answer

3.7.10 Indexing: GATE CSE 2020 | Question: 54 top 5

https://gateoverflow.in/333177



Consider a database implemented using B+ tree for file indexing and installed on a disk drive with block size of 4 KB. The size of search key is 12 bytes and the size of tree/disk pointer is 8 bytes. Assume that the database has one million records. Also assume that no node of the B+ tree and no records are present initially in main memory. Consider that each record fits into one disk block. The minimum number of disk accesses required to retrieve any record in the database is _____

gate2020-cse numerical-answers databases b-tree indexing

Answer

3.7.11 Indexing: GATE CSE 2021 Set 2 | Question: 21 top 5

https://gateoverflow.in/37519



A data file consisting of 1,50,000 student-records is stored on a hard disk with block size of 4096 bytes. The data file is sorted on the primary key RollNo. The size of a record pointer for this disk is 7 bytes. Each student-record has a candidate key attribute called ANum of size 12 bytes. Suppose an index file with records consisting of two fields, ANum value and the record pointer the corresponding student record, is built and stored on the same disk. Assume that the records of data file and index file are not split across disk blocks. The number of blocks in the index file is _____

gate2021-cse-set2 numerical-answers databases indexing

Answer

Answers: Indexing

3.7.1 Indexing: GATE CSE 1989 | Question: 4-xiv top 5

https://gateoverflow.in/8228



Inverted File organization

Because of the following reasons

An index for each secondary key.

· An index entry for each distinct value of the secondary key.

It exhibits better inquiry performance

4 votes

-- Neeraj7375 (1.1k points)

3.7.2 Indexing: GATE CSE 1990 | Question: 10b top 5

https://gateoverflow.in/85691



✓ First we can understand the terms given in the question:

- Uniform blocking factor = 8

This is the no. of records which can be held in a data block.

This information is required for DENSE index which is mandatory when the index is unclustered - data records not ordered by the search key (there is an index entry for each record) as compared to fully sparse (which has an index entry for each data block). Since in the question we do not have any information about "record pointer size" we can assume that the index is sparse. (Solution considering dense index is given at end)

- Block size = 1 KB

This is the size of data block (file block containing records) as well as index block (file block containing index entries). Since file size is given as 1 giga bytes, we get no. of data blocks = $\frac{1 \text{ GB}}{1 \text{ KB}} = 1 \text{ M} = 2^{20}$

- Block referencing pointer size = 32 bits = 4 B

This is the pointer size required to point to a block.

- The referencing capability (fanout ratio) per block of index storage may be considered to be 32.

This means that an index block can refer to 32 blocks (either data or index blocks). i.e., even though we have 1024 bytes in a block, and each block pointer size is 4 bytes, it can refer to only 32 blocks. This might be due to large search key size which must be present for each index entry.

Now, coming to the solution:

No. of entries in first level index (which indexes to the data blocks) (in case of page tables in virtual memory, this will be the total no. of entries in last level page table) = no. of data blocks (assuming sparse index) = 2^{20}

No. of index blocks in level 1 = $\frac{2^{20}}{32} = 2^{15}$ as each index block can refer to 32 blocks (given fanout) which means size of level 1 index = $2^{15} \times 1 \text{ KB} = 32 \text{ MB}$

Since the fanout is 32, no. of index blocks in second level = $\frac{2^{15}}{32} = 2^{10}$.

Size of second level index = $2^{10} \times 1 \text{ KB} = 1 \text{ MB}$

No. of index blocks in third level = $\frac{2^{10}}{32} = 32$.

Size of third level index = $32 \times 1 \text{ KB} = 32 \text{ KB}$

No. of index blocks in fourth level = $\frac{32}{32} = 1$ and it occupies 1 KB. Since only 1 index block is there we do not need further level of indexing.

Searching starts in the last level (this will be level 1 page table in case of virtual memory in OS).

Master Index -- not sure exactly what this means but I assume this is the complete index whose size will be $32 \text{ MB} + 1 \text{ MB} + 32 \text{ KB} + 1 \text{ KB} = 33.033 \text{ MB}$

Now assuming dense index.

Block pointer size = 32 bits. Since, we have 8 records in a block, we need at least 3 more extra bits for a record pointer. So, we need to assume 5 bytes for a record pointer. As fanout is given in the question it is not changing when the record pointer size changes. If fanout was not given, we could have calculated it as $\frac{\text{block size}}{\text{search_key_size} + \text{record pointer size}}$

Here, we need an index entry for each record. So, we need = $\frac{1 \text{ GB}}{1 \text{ KB}} \times 8 = 8 \text{ M} = 2^{23}$ entries in first level index.

No. of index blocks in first level = $\frac{2^{23}}{32} = 2^{18}$

Size of first level index = $2^{18} \times 1 \text{ KB} = 256 \text{ MB}$

No. of index blocks in second level = $\frac{2^{18}}{32} = 2^{13}$

Size of second level index = $2^{13} \times 1 \text{ KB} = 8 \text{ MB}$

No. of index blocks in third level = $\frac{2^{13}}{32} = 2^8$

Size of third level index = $2^8 \times 1 \text{ KB} = 256 \text{ KB}$

No. of index blocks in fourth level = $\frac{2^8}{32} = 8$

Size of fourth level index = $8 \times 1 \text{ KB} = 8 \text{ KB}$

No. of index blocks in fifth level = $\lceil \frac{8}{32} \rceil = 1$

Size of fifth level index = $1 \times 1 \text{ KB} = 1 \text{ KB}$

Master Index size = $256 \text{ MB} + 8 \text{ MB} + 256 \text{ KB} + 8 \text{ KB} + 1 \text{ KB} = 264.265 \text{ MB}$

👍 34 votes

-- Arjun Suresh (332k points)



✓ Answer: 3

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Size of each index entry = $14 + 2 = 16 B$

Blocking factor of record file = $\frac{\text{Block size}}{\text{Record size}} = 512 B / 64 B = 8$

Blocking factor of index file = $\frac{\text{Block size}}{\text{Index entry size}} = 512 B / 16 B = 32$

No. of Blocks needed for data file = $\frac{\text{No. of Records}}{\text{Blocking factor of record file}} = 16 K / 8 = 2 K$

No. of first level index entries = No. of Data Blocks needed for data file = $2 K$

No. of first level index blocks = $\lceil \frac{\text{No. of first level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{2K}{32} \rceil = 64$

No. of second level index entries = No. of first level index blocks = 64

No. of second level index blocks = $\lceil \frac{\text{No. of second level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{64}{32} \rceil = 2$

No. of third level index entries = No. of second level index blocks = 2

No. of third level index blocks = $\lceil \frac{\text{No. of third level index entries}}{\text{Blocking factor of index file}} \rceil = \lceil \frac{2}{32} \rceil = 1$

👍 56 votes

-- Rajarshi Sarkar (27.9k points)



✓ Indexing will be on Occupation field because Occupation field lexicographically sorted will give the sequence 1, 3, 2, 5, 4.

Correct Answer: C

👍 71 votes

-- Digvijay (44.9k points)



✓ There are several types of ordered indexes. A **primary index** is specified on the *ordering key field* of an **ordered file** of records. Recall from **Section 17.7** that an ordering key field is used to *physically order* the file records on disk, and every record has a *unique value* for that field. If the ordering field is not a key field— that is, if numerous records in the file can have the same value for the ordering field— another type of index, called a **clustering index**, can be used. The data file is called a **clustered file** in this latter case. Notice that a file can have at most one physical ordering field, so it can have at most one primary index or one clustering index, *but not both*.

Reference -> Database Systems book BY Navathe, 6th Edition, **18.1** Types of Single- Level Ordered Indexes Page **no. 632**.

Answer should be A.

👍 33 votes

-- Akash Kanase (36k points)



✓ Content of an index will be <key, block pointer> and so will have size $6 + 10 = 16$.

In the first level, there will be an entry for each record of the file. So, total size of first-level index

= $16384 * 16$

No. of blocks in the first-level = Size of first-level index / block size

= $16384 * 16 / 1024$

= $16 * 16 = 256$

In the second-level there will be an entry for each block in the first level. So, total number of entries = 256 and total size of

second-level index

$$\begin{aligned} &= \text{No. of entries} * \text{size of an entry} \\ &= 256 * 16 \end{aligned}$$

$$\begin{aligned} \text{No. of blocks in second-level index} &= \text{Size of second-level index} / \text{block size} \\ &= 256 * 16 / 1024 \end{aligned}$$

$$= 4$$

Correct Answer: C

👍 72 votes

-- gatecse (63.3k points)

3.7.7 Indexing: GATE CSE 2011 | Question: 39 top

<https://gateoverflow.in/2141>



- ✓ (C) Hashing works well on the 'equal' queries, while ordered indexing works well better on range queries too. For example consider B+ Tree, once you have searched a key in B+ tree, you can find range of values via the block pointers pointing to another block of values on the leaf node level.

👍 64 votes

-- Prateeksha Keshari (1.7k points)

3.7.8 Indexing: GATE CSE 2013 | Question: 15 top

<https://gateoverflow.in/1437>



- ✓ Answer is C).

Index can be created using any column or combination of column which need not be unique. So, **A, B** are not the answers.

Indexed column is used to sort rows of table. Whole data record of file is sorted using index so, **C** is correct option. (Simple video explains this).



Video:



Video:

👍 29 votes

-- prashant singh (337 points)

3.7.9 Indexing: GATE CSE 2015 Set 1 | Question: 24 top

<https://gateoverflow.in/8222>



- ✓ Clustered- this is the definition of clustered indexing and for the same reason a table can have only one clustered index.

<http://www.ece.rutgers.edu/~yyzhang/spring03/notes/7-B+tree.ppt>

Correct Answer: C

References



👍 37 votes

-- Arjun Suresh (332k points)

3.7.10 Indexing: GATE CSE 2020 | Question: 54 top

<https://gateoverflow.in/333177>





Given,

1. Search Key: 12 bytes
2. Tree Pointer: 8 bytes
3. Block Size: 4096 bytes
4. Number of database records: 10^6

Since it's a B^+ tree, an internal node only has search key values and tree pointers. Let p be the order of an internal node. Hence,

$$p(8) + (p-1)(12) \leq 4096$$

which gives $p \leq 205.4$.

Therefore $p = 205$

Now,

Level	Nodes	Keys	Pointers
1	1	204	205
2	205	204×205	205^2
3	205^2	204×205^2	205^3

Level 3 alone has approximately 8.5×10^6 entries. So we can be sure that a 3-level B^+ tree is sufficient to index 10^6 records.

So to access any record (in the worst case), we need 3 block access to search for the record in the index along with 1 more access to actually access the record.

Hence, 4 accesses are required.

34 votes

-- Debasish Das (1.5k points)



ANS = 698 .

Index is being built on attribute "ANum" which is Candidate Key, but Given that file is Sorted on Primary Key "Roll No".

This indicates that The Index must a **Secondary Index**, (data records not being physically ordered as per the index making a dense record necessary) so "THERE SHOULD EXIST AN INDEX RECORD FOR **EVERY RECORD** of Original 'Student Table' ".

=> Also this Line: "Assume that Records of data file and index file are not split across disc blocks".

This indicates **UNSPANNED STRATEGY**.

With This Knowledge, let's see the Data given.

→ Record Size in Index = $12 + 7 = 19$ B ('ANum' key size + Record pointer Size), and Block Size = 4096 B

→ So number of Index records in 1 Block = $\lfloor \frac{4096}{19} \rfloor = 215$ records in 1 block (Remember again, unspanned strategy).

→ So number of blocks in the Index file = $\frac{\text{Total Number of records}}{\text{Records per block}} = \left\lceil \frac{1,50,000}{215} \right\rceil = 698$.

(Recall that this is Secondary Index)

4 votes

-- Amcodes (745 points)



Consider the following relation schema pertaining to a students database:

- Students (rollno, name, address)
- Enroll (rollno, courseno, coursename)

where the primary keys are shown underlined. The number of tuples in the student and Enroll tables are 120 and 8 respectively. What are the maximum and minimum number of tuples that can be present in (Student * Enroll), where '*' denotes natural join?

- A. 8, 8
- B. 120, 8

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- C. 960, 8
- D. 960, 120

gate2004-cse databases easy joins natural-join

Answer

3.8.2 Joins: GATE CSE 2012 | Question: 50

https://gateoverflow.in/2180



Consider the following relations A, B and C :

A		
ID	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
ID	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
ID	Phone	Area
10	2200	02
99	2100	01

How many tuples does the result of the following relational algebra expression contain? Assume that the schema of $A \cup B$ is the same as that of A .

$$(A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C$$

- A. 7
- B. 4
- C. 5
- D. 9

gate2012-cse databases joins normal

Answer

3.8.3 Joins: GATE CSE 2014 Set 2 | Question: 30

https://gateoverflow.in/1989



Consider a join (relation algebra) between relations $r(R)$ and $s(S)$ using the nested loop method. There are 3 buffers each of size equal to disk block size, out of which one buffer is reserved for intermediate results. Assuming $\text{size}(r(R)) < \text{size}(s(S))$, the join will have fewer number of disk block accesses if

- A. relation $r(R)$ is in the outer loop.
- B. relation $s(S)$ is in the outer loop.
- C. join selection factor between $r(R)$ and $s(S)$ is more than 0.5.
- D. join selection factor between $r(R)$ and $s(S)$ is less than 0.5.

gate2014-cse-set2 databases normal joins

Answer

3.8.4 Joins: GATE IT 2005 | Question: 82a

https://gateoverflow.in/3847



A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If Nested-loop join algorithm is employed to perform the join, with the most appropriate choice of table to be used in outer loop, the number of block accesses required for reading the data are

- A. 800000
- B. 40080
- C. 32020
- D. 100

gate2005-it databases normal joins

Answer



A database table T_1 has 2000 records and occupies 80 disk blocks. Another table T_2 has 400 records and occupies 20 disk blocks. These two tables have to be joined as per a specified join condition that needs to be evaluated for every pair of records from these two tables. The memory buffer space available can hold exactly one block of records for T_1 and one block of records for T_2 simultaneously at any point in time. No index is available on either table.

If, instead of Nested-loop join, Block nested-loop join is used, again with the most appropriate choice of table in the outer loop, the reduction in number of block accesses required for reading the data will be

- A. 0
- B. 30400
- C. 38400
- D. 798400

gate2005-it databases normal joins

Answer



Consider the relations $r_1(P, Q, R)$ and $r_2(R, S, T)$ with primary keys P and R respectively. The relation r_1 contains 2000 tuples and r_2 contains 2500 tuples. The maximum size of the join $r_1 \bowtie r_2$ is :

- A. 2000
- B. 2500
- C. 4500
- D. 5000

gate2006-it databases joins natural-join normal

Answer



Consider the following relation schemas :

- b-Schema = (b-name, b-city, assets)
- a-Schema = (a-num, b-name, bal)
- d-Schema = (c-name, a-number)

Let branch, account and depositor be respectively instances of the above schemas. Assume that account and depositor relations are much bigger than the branch relation.

Consider the following query:

$\Pi_{c-name} (\sigma_{b-city = "Agra" \wedge bal < 0} (\text{branch} \bowtie (\text{account} \bowtie \text{depositor})))$

Which one of the following queries is the most efficient version of the above query ?

- A. $\Pi_{c-name} (\sigma_{bal < 0} (\sigma_{b-city = "Agra"} \text{branch} \bowtie \text{account}) \bowtie \text{depositor})$
- B. $\Pi_{c-name} (\sigma_{b-city = "Agra"} \text{branch} \bowtie (\sigma_{bal < 0} \text{account} \bowtie \text{depositor}))$
- C. $\Pi_{c-name} ((\sigma_{b-city = "Agra"} \text{branch} \bowtie \sigma_{b-city = "Agra"} \wedge bal < 0 \text{account}) \bowtie \text{depositor})$
- D. $\Pi_{c-name} (\sigma_{b-city = "Agra"} \text{branch} \bowtie (\sigma_{b-city = "Agra"} \wedge bal < 0 \text{account} \bowtie \text{depositor}))$

gate2007-it databases joins relational-algebra normal

Answer

Answers: Joins



✓ Rollno in students is key, ans students table has 120 tuples, In Enroll table rollno is FK referencing to Students table. In natural join it'll return the records where the rollno value of enroll matches with the rollno of students so, in both conditions min and max records will be resulted (8, 8).
hence A is the answer.

Hint: table which has non-key, no of records of that will be resulted.

47 votes

-- Manu Thakur (34k points)



Given relations A, B and C :

A		
ID	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
ID	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
ID	Phone	Area
10	2200	02
99	2100	01

This is an example of theta join and we know: $R \bowtie_{\theta} S = \sigma_{\theta}(R \times S)$

$$\therefore (A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C = (A.Id > 40 ((A \cup B) \times C)) \cup (C.Id < 15 ((A \cup B) \times C))$$

To make the query more efficient we can perform the select operation before the cross product.

$$\therefore (A \cup B) \bowtie_{A.Id > 40 \vee C.Id < 15} C = (A.Id > 40 (A \cup B) \times C) \cup ((A \cup B) \times_{C.Id < 15} C)$$

Now calculate $A \cup B$:

ID	Name	Age
12	Arun	60
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

Please note that union is a set operation and duplicates will not be included by default.

First perform cross-product $(A.Id > 40 (A \cup B) \times C)$, i.e., Multiply each row of $A.Id > 40 (A \cup B)$ with each row of C :

ID	Name	Age	C.ID	Phone	Area
98	Rohit	20	10	2200	02
98	Rohit	20	99	2100	01
99	Rohit	11	10	2200	02
99	Rohit	11	99	2100	01

Now perform cross-product $((A \cup B) \times_{C.Id < 15} C)$, i.e., Multiply each row of $(A \cup B)$ with each row of $C.Id < 15 C$:

ID	Name	Age	C.ID	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
25	Hari	40	10	2200	02

Now take the union: $(A.Id > 40 (A \cup B) \times C) \cup ((A \cup B) \times_{C.Id < 15} C)$

We will get:

ID	Name	Age	C.ID	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
25	Hari	40	10	2200	02
98	Rohit	20	10	2200	02
98	Rohit	20	99	2100	01
99	Rohit	11	10	2200	02
99	Rohit	11	99	2100	01

which has 7 Tuples, hence answer is A.

👍 8 votes

-- Sourabh Gupta (4k points)

50. For C.ID = 10, all tuples from $A \cup B$ satisfies the join condition, hence 5 tuples (union of A and B has only 5 tuples are 2 of them are repeating for Shreya and Rohit) will be returned. Now, for C.ID = 99, A.ID = 99 and A.ID = 98 (for A.ID = 98, we need to assume $A \cup B$, has the same schema s A as told in the question) satisfies the condition A.ID>40, and hence two tuples are returned. So, number of tuples = 5 + 2 = 7.

The output will be:

Id	Name	Age	Id	Phone	Area
12	Arun	60	10	2200	02
15	Shreya	24	10	2200	02
99	Rohit	11	10	2200	02
25	Hari	40	10	2200	02
98	Rohit	20	10	2200	02
99	Rohit	11	99	2100	01
98	Rohit	20	99	2100	01

Correct Answer: A

👍 51 votes

-- Arjun Suresh (332k points)

3.8.3 Joins: GATE CSE 2014 Set 2 | Question: 30 [top](#)

<https://gateoverflow.in/1989>



✓ In joining B and B using nested loop method, with A in outer loop two factors are involved.

- No. of blocks containing all rows in A should be fetched
- No. of Rows A times no of Blocks containing all Rows of B

(in worst case all rows of B are matched with all rows of A).

In above ques, $|R| < |S|$

(i) will be less when number of rows in outer table is less since less no of rows will take less no. of blocks

(ii) if we keep R in outer loop, no. of rows in R are less and no. of blocks in S are more

If we keep S in outer loop, no of rows in S are more and no. of blocks in R are less.

In (ii) block accesses will be multiplication and will come same in both cases.

So, (i) will determine no of block accesses

So, answer is A.

👍 20 votes

-- Anurag Semwal (6.7k points)

3.8.4 Joins: GATE IT 2005 | Question: 82a [top](#)

<https://gateoverflow.in/3847>



✓ We just have to think which table would be in the outer loop. To minimize block accesses, we have to put that table outside having fewer records because for each outer record, one block access inside will be required.

Therefore, putting 2nd table outside,

- for every 400 records
 - 80 block accesses in the first table
 - = 32000
- 20 block accesses of the outer table.

So, the answer comes out to be $32000 + 20 = 32020$

Correct Answer: C.

👍 84 votes

-- Vishesh Bajpai (383 points)

Reference: http://en.wikipedia.org/wiki/Nested_loop_join

As per this reference this algorithm will involve $nr * bs + br$ block transfers

T_1 can be either R or T_2

- If R is T_1 then total number of block accesses is $2000 \times 20 + 80 = 40080$
- If R is T_2 then total number of block accesses is $400 \times 80 + 20 = 32020$

So, better is the second case (32020) Hence, I go for option C.

References



👍 42 votes

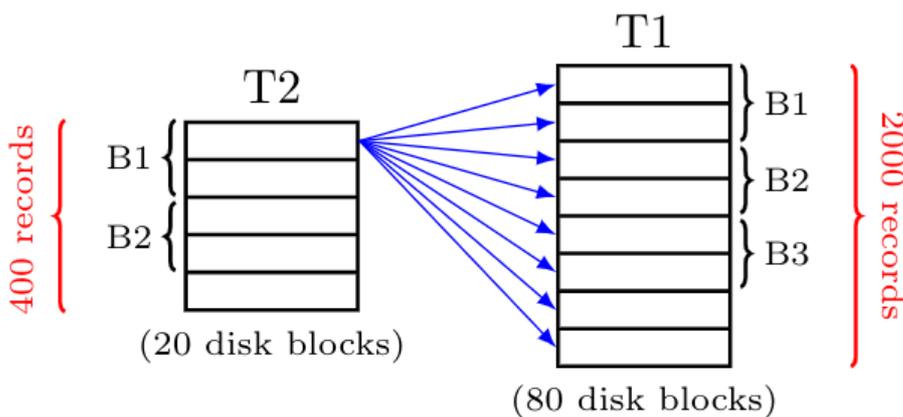
-- Sankaranarayanan P.N (8.5k points)

3.8.5 Joins: GATE IT 2005 | Question: 82b top 5

<https://gateoverflow.in/3848>



- ✓ In Nested loop join for each tuple in first table we scan through all the tuples in second table.



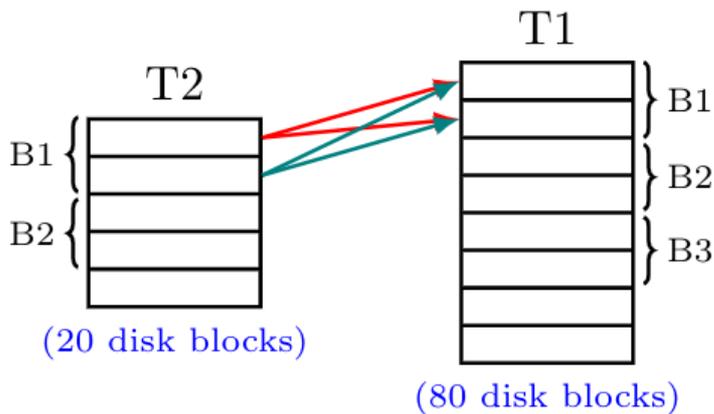
Here we will take table T_2 as the outer table in nested loop join algorithm. The number of block accesses then will be $20 + (400 \times 80) = 32020$

In block nested loop join we keep 1 block of T_1 in memory and 1 block of T_2 in memory and do join on tuples.

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For every block in T1 we need to load all blocks of T2. So number of block accesses is $80 \times 20 + 20 = 1620$

So, the difference is $32020 - 1620 = 30400$

(B) 30400

👍 65 votes

-- Omesh Pandita (1.9k points)

3.8.6 Joins: GATE IT 2006 | Question: 14 [top](#)

<https://gateoverflow.in/3553>



- ✓ The common attribute is R and it is the primary key in the second relation. So R value should be distinct (primary key implies unique) for 2500 rows. Hence when we do join, maximum possible number of tuples is 2000.

Correct option is A.

👍 36 votes

-- Sankaranarayanan P.N (8.5k points)

3.8.7 Joins: GATE IT 2007 | Question: 68 [top](#)

<https://gateoverflow.in/3513>



- ✓ It should be A. As in B we are doing a join between two massive table whereas in A we are doing join between relatively smaller table and larger one and the output that this inner table gives (which is smaller in comparison to joins that we are doing in B) is used for join with depositor table with the selection condition.

Options C and D are invalid as there is no b-city column in a-Schema.

Let's see in detail. Let there be 100 different branches. Say about 10% of accounts are below 0. Also, let there be 10,000 accounts in a branch amounting to 1,000,000 total accounts. A customer can have multiple accounts, so let there be on average 2 accounts per customer. So, this amounts to 2,000,000 total entries in depositor table. Let's assume these assumptions are true for all the branches. So, now let's evaluate options A and B.

- All the accounts in Agra branch, filter by positive balance, and then depositor details of them. So,
 - Get branch name from branch table after processing 100 records
 - Filter 10,000 accounts after processing 1,000,000 accounts belonging to Agra
 - Filter 1000 accounts after processing 10,000 accounts for positive balance
 - Get 500 depositor details after processing 2,000,000 entries for the given 1000 accounts (assuming 1 customer having 2 accounts). So, totally this amounts to 2,000,000,000 record processing.
 - So totally ≈ 2 billion records needs processing.
- All the positive balance accounts are found first, and then those in Agra are found.
 - Filter 100,000 accounts after processing 1,000,000 accounts having positive balance
 - Find the depositor details of these accounts. So, $100,000 \times 2,000,000$ records need processing and this is a much larger value than for query A. Even if we reduce the percentage of positive balance (10 we assumed) the record processing of query A will also get reduced by same rate. So, overall query A is much better than query B.

👍 59 votes

-- Shaun Patel (6.1k points)



Consider the following implications relating to functional and multivalued dependencies given below, which may or may not be correct.

- i. if $A \twoheadrightarrow B$ and $A \twoheadrightarrow C$ then $A \rightarrow BC$
- ii. if $A \rightarrow B$ and $A \rightarrow C$ then $A \twoheadrightarrow BC$
- iii. if $A \twoheadrightarrow BC$ and $A \rightarrow B$ then $A \rightarrow C$
- iv. if $A \twoheadrightarrow BC$ and $A \rightarrow B$ then $A \twoheadrightarrow C$

Exactly how many of the above implications are valid?

- A. 0
- B. 1
- C. 2
- D. 3

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multivalued-dependency-4nf

normal

Answer

Answers: Multivalued Dependency 4nf



- ✓
- a. If $A \twoheadrightarrow B$ and $A \twoheadrightarrow C$ then $A \rightarrow BC$. So FALSE
 - b. If $A \rightarrow B$ and $A \rightarrow C$ then $A \twoheadrightarrow BC$. So $A \twoheadrightarrow BC$ TRUE..
 - c. If $A \twoheadrightarrow BC$ and $A \rightarrow B$ here B is Subset of AB and $(A \cap BC)$ is phi so $A \rightarrow B$ but not $A \rightarrow C$ so FALSE (**Coalescence rule**)
 - d. If $A \rightarrow BC$ then $A \rightarrow C$ so $A \twoheadrightarrow C$ TRUE
if $A \rightarrow B$ then $A \twoheadrightarrow B$ holds but reverse not true.

Correct Answer: C

34 votes

-- Digvijay (44.9k points)



Let r be a relation instance with schema $R = (A, B, C, D)$. We define $r_1 = \pi_{A,B,C}(R)$ and $r_2 = \pi_{A,D}(r)$. Let $s = r_1 * r_2$ where $*$ denotes natural join. Given that the decomposition of r into r_1 and r_2 is lossy, which one of the following is TRUE?

- A. $s \subset r$
- B. $r \cup s = r$
- C. $r \subset s$
- D. $r * s = s$

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relational-algebra

natural-join

normal

Answer



The following functional dependencies hold for relations $R(A, B, C)$ and $S(B, D, E)$.

- $B \rightarrow A$
- $A \rightarrow C$

The relation R contains 200 tuples and the relation S contains 100 tuples. What is the maximum number of tuples possible in the natural join $R \bowtie S$?

- A. 100
- B. 200
- C. 300
- D. 2000

Answer

3.10.3 Natural Join: GATE CSE 2015 Set 2 | Question: 32

https://gateoverflow.in/8151

Consider two relations $R_1(A, B)$ with the tuples $(1, 5), (3, 7)$ and $R_2(A, C) = (1, 7), (4, 9)$. Assume that $R(A, B, C)$ is the full natural outer join of R_1 and R_2 . Consider the following tuples of the form (A, B, C) :

$a = (1, 5, null), b = (1, null, 7), c = (3, null, 9), d = (4, 7, null), e = (1, 5, 7), f = (3, 7, null), g = (4, null, 9)$.

Which one of the following statements is correct?

- A. R contains a, b, e, f, g but not c, d .
- B. R contains all a, b, c, d, e, f, g .
- C. R contains e, f, g but not a, b .
- D. R contains e but not f, g .

Answer

Answers: Natural Join

3.10.1 Natural Join: GATE CSE 2005 | Question: 30

https://gateoverflow.in/1366

✓ Answer is $C \ r \subset s$.

r			
A	B	C	D
1	2	3	3
1	5	3	4

r1		
A	B	C
1	2	3
1	5	3

r2	
A	D
1	3
1	4

s = r1 * r2			
A	B	C	D
1	2	3	3
1	2	3	4
1	5	3	4
1	5	3	4

All the rows of r are in s (marked bold). So, $r \subset s$.

And one more result $r * s = r$.

56 votes

-- Vikrant Singh (11.2k points)

3.10.2 Natural Join: GATE CSE 2010 | Question: 43

https://gateoverflow.in/2344

✓ (A) 100.

Natural join will combine tuples with same value of the common rows (if there are two common rows then both values must be equal to get into the resultant set). So by this definition we can get at the max only 100 common values.

37 votes

-- Aravind (2.8k points)

3.10.3 Natural Join: GATE CSE 2015 Set 2 | Question: 32

https://gateoverflow.in/8151

✓

$R_1(A, B) :$	A	B
	1	5
	3	7

$R_2(A, C) :$	A	C
	1	7
	4	9

Now, if we do full natural outer join:

A	B	C
1	5	7
3	7	NULL
4	NULL	9

So, option (C) is correct.

👍 37 votes

-- worst_engineer (2.8k points)

3.11

Referential Integrity (4) [top](#)

3.11.1 Referential Integrity: GATE CSE 1997 | Question: 6.10, ISRO2016-54 [top](#)

<https://gateoverflow.in/2266>



Let $R(a, b, c)$ and $S(d, e, f)$ be two relations in which d is the foreign key of S that refers to the primary key of R . Consider the following four operations R and S

- I. Insert into R
- II. Insert into S
- III. Delete from R
- IV. Delete from S

Which of the following can cause violation of the referential integrity constraint above?

- A. Both I and IV
- B. Both II and III
- C. All of these
- D. None of these

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Answer [👍](#)

3.11.2 Referential Integrity: GATE CSE 2005 | Question: 76 [top](#)

<https://gateoverflow.in/1399>



The following table has two attributes A and C where A is the primary key and C is the foreign key referencing A with on-delete cascade.

A	C
2	4
3	4
4	3
5	2
7	2
9	5
6	4

The set of all tuples that must be additionally deleted to preserve referential integrity when the tuple (2, 4) is deleted is:

- A. (3, 4) and (6, 4)
- B. (5, 2) and (7, 2)
- C. (5, 2), (7, 2) and (9, 5)
- D. (3, 4), (4, 3) and (6, 4)

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databases

referential-integrity

normal

Answer [👍](#)



Consider the following tables $T1$ and $T2$.

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$T1$		$T2$	
P	Q	R	S
2	2	2	2
3	8	8	3
7	3	3	2
5	8	9	7
6	9	5	7
8	5	7	2
9	8		

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In table $T1$ P is the primary key and Q is the foreign key referencing R in table $T2$ with on-delete cascade and on-update cascade. In table $T2$, R is the primary key and S is the foreign key referencing P in table $T1$ with on-delete set NULL and on-update cascade. In order to delete record $(3, 8)$ from the table $T1$, the number of additional records that need to be deleted from table $T1$ is

gate2017-cse-set2 databases numerical-answers referential-integrity normal

Answer



Consider the following statements $S1$ and $S2$ about the relational data model:

- $S1$: A relation scheme can have at most one foreign key.
- $S2$: A foreign key in a relation scheme R cannot be used to refer to tuples of R .

Which one of the following choices is correct?

- A. Both $S1$ and $S2$ are true
- B. $S1$ is true and $S2$ is false
- C. $S1$ is false and $S2$ is true
- D. Both $S1$ and $S2$ are false

gate2021-cse-set2 databases referential-integrity

Answer

Answers: Referential Integrity



✓

R			S		
a (PK)	b	c	d (FK referring to PK of R)	e	f
1			2		
2			1		

- Insert into R cannot cause any violation.
- Insert into S can cause violation if any value is inserted into d of S, which value is not in a of R.
- Delete from S cannot cause any violation.
- Delete from R can cause violation if any tuple is deleted, and as a result a value in 'a' gets deleted which is referenced to by 'd' in S .

Correct Answer: B

42 votes

-- Sourav Roy (2.9k points)



✓ (C)

Since deleting (2, 4), since 2 is a primary key, you have to delete its foreign key occurrence i.e (5, 2) and (7, 2)
Since we are deleting 5, and 7 we have to delete its foreign key occurrence i.e (9, 5).

There is no foreign key occurrence for 9.

43 votes

-- Aravind (2.8k points)

3.11.3 Referential Integrity: GATE CSE 2017 Set 2 | Question: 19 [top](#)

<https://gateoverflow.in/118236>



- ✓ As Q refers to R so, deleting 8 from Q won't be an issue, however S refers P. But as the relationship given is on delete set NULL, 3 will be deleted from T1 and the entry in T2 having 3 in column S will be set to NULL. So, no more deletions. Answer is 0.

74 votes

-- Prateek Kumar (1.1k points)

3.11.4 Referential Integrity: GATE CSE 2021 Set 2 | Question: 6 [top](#)

<https://gateoverflow.in/357534>



- ✓ Both S_1 and S_2 are FALSE.

In a relation scheme multiple foreign attributes can be present referring to primary keys of other relation schemes. A typical example is an EXAM_RESULTS(sid,eid,marks) scheme where sid and eid are foreign keys referring to the primary keys in STUDENT and EXAM schemes respectively.

S_2 is FALSE because a foreign key can refer to the same scheme (self-referencing foreign key). A typical example is an EMPLOYEE(eid, mid, ...) scheme where mid is the Manager ID referring to the primary key eid of the same scheme.

3 votes

-- gatecse (63.3k points)

3.12

Relational Algebra (26) [top](#)

3.12.1 Relational Algebra: GATE CSE 1992 | Question: 13b [top](#)

<https://gateoverflow.in/43581>



Suppose we have a database consisting of the following three relations:

FREQUENTS	(CUSTOMER, HOTEL)
SERVES	(HOTEL, SNACKS)
LIKES	(CUSTOMER, SNACKS)

The first indicates the hotels each customer visits, the second tells which snacks each hotel serves and last indicates which snacks are liked by each customer. Express the following query in relational algebra:

Print the hotels that serve the snack that customer Rama likes.

gate1992 databases relational-algebra normal descriptive

Answer

3.12.2 Relational Algebra: GATE CSE 1994 | Question: 13 [top](#)

<https://gateoverflow.in/2509>



Consider the following relational schema:

- COURSES (cno, cname)
- STUDENTS (rollno, sname, age, year)
- REGISTERED_FOR (cno, rollno)

The underlined attributes indicate the primary keys for the relations. The 'year' attribute for the STUDENTS relation indicates the year in which the student is currently studying (First year, Second year etc.)

- Write a relational algebra query to print the roll number of students who have registered for cno 322.
- Write a SQL query to print the age and year of the youngest student in each year.

gate1994 databases relational-algebra sql normal descriptive

Answer

3.12.3 Relational Algebra: GATE CSE 1994 | Question: 3.8 top

<https://gateoverflow.in/2494>



Give a relational algebra expression using only the minimum number of operators from $(\cup, -)$ which is equivalent to $R \cap S$.

gate1994 databases relational-algebra normal descriptive

Answer

3.12.4 Relational Algebra: GATE CSE 1995 | Question: 27 top

<https://gateoverflow.in/2666>



Consider the relation scheme.

AUTHOR	(ANAME, INSTITUTION, ACITY, AGE)
PUBLISHER	(PNAME, PCITY)
BOOK	(TITLE, ANAME, PNAME)

Express the following queries using (one or more of) SELECT, PROJECT, JOIN and DIVIDE operations.

- Get the names of all publishers.
- Get values of all attributes of all authors who have published a book for the publisher with PNAME='TECHNICAL PUBLISHERS'.
- Get the names of all authors who have published a book for any publisher located in Madras

gate1995 databases relational-algebra normal descriptive

Answer

3.12.5 Relational Algebra: GATE CSE 1996 | Question: 27 top

<https://gateoverflow.in/2779>



A library relational database system uses the following schema

- USERS (User#, User Name, Home Town)
- BOOKS (Book#, Book Title, Author Name)
- ISSUED (Book#, User#, Date)

Explain in one English sentence, what each of the following relational algebra queries is designed to determine

- $\sigma_{\text{User\#}=6} (\pi_{\text{User\#, Book Title}} ((\text{USERS} \bowtie \text{ISSUED}) \bowtie \text{BOOKS}))$
- $\pi_{\text{Author Name}} (\text{BOOKS} \bowtie \sigma_{\text{Home Town}=\text{Delhi}} (\text{USERS} \bowtie \text{ISSUED}))$

gate1996 databases relational-algebra descriptive

Answer

3.12.6 Relational Algebra: GATE CSE 1997 | Question: 76-a top

<https://gateoverflow.in/19838>



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)
- INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

What is the relational algebra expression containing one or more of $\{\sigma, \pi, \times, \rho, -\}$ which is equivalent to SQL query.

```
select eno from EMP INVOLVED where EMP.eno=INVOLVED.eno and INVOLVED.pno=3
```

gate1997 databases sql relational-algebra descriptive

Answer



Given two union compatible relations $R_1(A, B)$ and $R_2(C, D)$, what is the result of the operation $R_1 \bowtie_{A=C \wedge B=D} R_2$?

- A. $R_1 \cup R_2$
- B. $R_1 \times R_2$
- C. $R_1 - R_2$
- D. $R_1 \cap R_2$

gate1998 normal relational-algebra

Answer



Consider the following relational database schemes:

- COURSES (Cno, Name)
- PRE_REQ(Cno, Pre_Cno)
- COMPLETED (Student_no, Cno)

COURSES gives the number and name of all the available courses.

PRE_REQ gives the information about which courses are pre-requisites for a given course.

COMPLETED indicates what courses have been completed by students

Express the following using relational algebra:

List all the courses for which a student with Student_no 2310 has completed all the pre-requisites.

gate1998 databases relational-algebra normal descriptive

Answer



Consider the join of a relation R with a relation S . If R has m tuples and S has n tuples then the maximum and minimum sizes of the join respectively are

- A. $m + n$ and 0
- B. mn and 0
- C. $m + n$ and $|m - n|$
- D. mn and $m + n$

gate1999 databases relational-algebra easy isro2016

Answer



Given the relations

- employee (name, salary, dept-no), and
- department (dept-no, dept-name, address),

Which of the following queries cannot be expressed using the basic relational algebra operations ($\sigma, \pi, \times, \bowtie, \cup, \cap, -$)?

- A. Department address of every employee
- B. Employees whose name is the same as their department name
- C. The sum of all employees' salaries
- D. All employees of a given department

gate2000-cse databases relational-algebra easy isro2016

Answer



Suppose the adjacency relation of vertices in a graph is represented in a table Adj (X, Y) . Which of the following queries cannot be expressed by a relational algebra expression of constant length?

- List all vertices adjacent to a given vertex
- List all vertices which have self loops
- List all vertices which belong to cycles of less than three vertices
- List all vertices reachable from a given vertex

gate2001-cse databases relational-algebra normal

Answer



Let r and s be two relations over the relation schemes R and S respectively, and let A be an attribute in R . The relational algebra expression $\sigma_{A=a}(r \bowtie s)$ is always equal to

- $\sigma_{A=a}(r)$
- r
- $\sigma_{A=a}(r) \bowtie s$
- None of the above

gate2001-cse databases relational-algebra

Answer



A university placement center maintains a relational database of companies that interview students on campus and make job offers to those successful in the interview. The schema of the database is given below:

COMPANY(<u>cname</u> , clocation)	STUDENT(<u>srollno</u> , sname, sdegree)
INTERVIEW(<u>cname</u> , <u>srollno</u> , idate)	OFFER(<u>cname</u> , <u>srollno</u> , osalary)

The COMPANY relation gives the name and location of the company. The STUDENT relation gives the student's roll number, name and the degree program for which the student is registered in the university. The INTERVIEW relation gives the date on which a student is interviewed by a company. The OFFER relation gives the salary offered to a student who is successful in a company's interview. The key for each relation is indicated by the underlined attributes

- Write a **relational algebra** expressions (using only the operators $\bowtie, \sigma, \pi, \cup, -$) for the following queries.
 - List the *rollnumbers* and *names* of students who attended at least one interview but did not receive *any* job offer.
 - List the *rollnumbers* and *names* of students who went for interviews and received job offers from *every* company with which they interviewed.
- Write an SQL query to list, for each degree program in which more than *five* students were offered jobs, the name of the degree and the average offered salary of students in this degree program.

gate2002-cse databases normal descriptive relational-algebra sql

Answer



Consider the following SQL query

Select distinct a_1, a_2, \dots, a_n

from r_1, r_2, \dots, r_m

where P

For an arbitrary predicate P, this query is equivalent to which of the following relational algebra expressions?

- $\Pi_{a_1, a_2, \dots, a_n} \sigma_P(r_1 \times r_2 \times \dots \times r_m)$

- B. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \bowtie r_2 \bowtie \dots \bowtie r_m)$
- C. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cup r_2 \cup \dots \cup r_m)$
- D. $\Pi_{a_1, a_2, \dots, a_n} \sigma_p (r_1 \cap r_2 \cap \dots \cap r_m)$

gate2003-cse databases relational-algebra normal

Answer 

3.12.15 Relational Algebra: GATE CSE 2004 | Question: 51 [top](#)

<https://gateoverflow.in/1047>



Consider the relation Student (name, sex, marks), where the primary key is shown underlined, pertaining to students in a class that has at least one boy and one girl. What does the following relational algebra expression produce? (Note: ρ is the rename operator).

$$\pi_{name} \{ \sigma_{sex=female} (Student) \} - \pi_{name} (Student \bowtie_{(sex=female \wedge x=male \wedge marks \leq m)} \rho_{n,x,m}(Student))$$

- A. names of girl students with the highest marks
- B. names of girl students with more marks than some boy student
- C. names of girl students with marks not less than some boy student
- D. names of girl students with more marks than all the boy students

gate2004-cse databases relational-algebra normal

Answer 

3.12.16 Relational Algebra: GATE CSE 2007 | Question: 59 [top](#)

<https://gateoverflow.in/2428>



Information about a collection of students is given by the relation studInfo(studId, name, sex). The relation enroll(studId, courseId) gives which student has enrolled for (or taken) what course(s). Assume that every course is taken by at least one male and at least one female student. What does the following relational algebra expression represent?

$$\pi_{courseId} ((\pi_{studId} (\sigma_{sex="female"} (studInfo)) \times \pi_{courseId} (enroll)) - enroll)$$

- A. Courses in which all the female students are enrolled.
- B. Courses in which a proper subset of female students are enrolled.
- C. Courses in which only male students are enrolled.
- D. None of the above

gate2007-cse databases relational-algebra normal

Answer 

3.12.17 Relational Algebra: GATE CSE 2008 | Question: 68 [top](#)

<https://gateoverflow.in/491>



Let R and S be two relations with the following schema

$$R(P, Q, R1, R2, R3)$$

$$S(P, Q, S1, S2)$$

where $\{P, Q\}$ is the key for both schemas. Which of the following queries are equivalent?

- I. $\Pi_P (R \bowtie S)$
- II. $\Pi_P (R) \bowtie \Pi_P (S)$
- III. $\Pi_P (\Pi_{P,Q} (R) \cap \Pi_{P,Q} (S))$
- IV. $\Pi_P (\Pi_{P,Q} (R) - (\Pi_{P,Q} (R) - \Pi_{P,Q} (S)))$
- A. Only I and II
- B. Only I and III
- C. Only I, II and III
- D. Only I, III and IV

gate2008-cse databases relational-algebra normal

Answer

3.12.18 Relational Algebra: GATE CSE 2012 | Question: 43 top

<https://gateoverflow.in/2151>



Suppose $R_1(A, B)$ and $R_2(C, D)$ are two relation schemas. Let r_1 and r_2 be the corresponding relation instances. B is a foreign key that refers to C in R_2 . If data in r_1 and r_2 satisfy referential integrity constraints, which of the following is ALWAYS TRUE?

- A. $\prod_B(r_1) - \prod_C(r_2) = \emptyset$
- B. $\prod_C(r_2) - \prod_B(r_1) = \emptyset$
- C. $\prod_B(r_1) = \prod_C(r_2)$
- D. $\prod_B(r_1) - \prod_C(r_2) \neq \emptyset$

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gate2012-cse databases relational-algebra normal

Answer

3.12.19 Relational Algebra: GATE CSE 2014 Set 3 | Question: 21 top

<https://gateoverflow.in/2055>



What is the optimized version of the relation algebra expression $\pi_{A1}(\pi_{A2}(\sigma_{F1}(\sigma_{F2}(r))))$, where $A1, A2$ are sets of attributes in r with $A1 \subset A2$ and $F1, F2$ are Boolean expressions based on the attributes in r ?

- A. $\pi_{A1}(\sigma_{(F1 \wedge F2)}(r))$
- B. $\pi_{A1}(\sigma_{(F1 \vee F2)}(r))$
- C. $\pi_{A2}(\sigma_{(F1 \wedge F2)}(r))$
- D. $\pi_{A2}(\sigma_{(F1 \vee F2)}(r))$

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gate2014-cse-set3 databases relational-algebra easy

Answer

3.12.20 Relational Algebra: GATE CSE 2014 Set 3 | Question: 30 top

<https://gateoverflow.in/2064>



Consider the relational schema given below, where **eId** of the relation **dependent** is a foreign key referring to **empId** of the relation **employee**. Assume that every employee has at least one associated dependent in the **dependent** relation.

employee (empId, empName, empAge)

dependent (depId, eId, depName, depAge)

Consider the following relational algebra query:

$\Pi_{empId} (employee) - \Pi_{empId} (employee \bowtie_{(empId=eID) \wedge (empAge \leq depAge)} dependent)$

The above query evaluates to the set of **empIds** of employees whose age is greater than that of

- A. some dependent.
- B. all dependents.
- C. some of his/her dependents.
- D. all of his/her dependents.

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gate2014-cse-set3 databases relational-algebra normal

Answer

3.12.21 Relational Algebra: GATE CSE 2015 Set 1 | Question: 7 top

<https://gateoverflow.in/8094>



SELECT operation in SQL is equivalent to

- A. The selection operation in relational algebra
- B. The selection operation in relational algebra, except that SELECT in SQL retains duplicates
- C. The projection operation in relational algebra
- D. The projection operation in relational algebra, except that SELECT in SQL retains duplicates

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gate2015-cse-set1 databases sql relational-algebra easy

Answer

3.12.22 Relational Algebra: GATE CSE 2017 Set 1 | Question: 46

<https://gateoverflow.in/118329>



Consider a database that has the relation schema $CR(\text{StudentName}, \text{CourseName})$. An instance of the schema CR is as given below.

StudentName	CourseName
SA	CA
SA	CB
SA	CC
SB	CB
SB	CC
SC	CA
SC	CB
SC	CC
SD	CA
SD	CB
SD	CC
SD	CD
SE	CD
SE	CA
SE	CB
SF	CA
SF	CB
SF	CC

The following query is made on the database.

- $T1 \leftarrow \pi_{\text{CourseName}} (\sigma_{\text{StudentName}=SA} (CR))$
- $T2 \leftarrow CR \div T1$

The number of rows in $T2$ is _____.

gate2017-cse-set1 databases relational-algebra normal numerical-answers

Answer

3.12.23 Relational Algebra: GATE CSE 2018 | Question: 41

<https://gateoverflow.in/204115>



Consider the relations $r(A, B)$ and $s(B, C)$, where $s.B$ is a primary key and $r.B$ is a foreign key referencing $s.B$. Consider the query

$$Q : r \bowtie (\sigma_{B < 5}(s))$$

Let LOJ denote the natural left outer-join operation. Assume that r and s contain no null values.

Which of the following is NOT equivalent to Q ?

- A. $\sigma_{B < 5}(r \bowtie s)$
- B. $\sigma_{B < 5}(r \text{ LOJ } s)$
- C. $r \text{ LOJ } (\sigma_{B < 5}(s))$
- D. $\sigma_{B < 5}(r) \text{ LOJ } s$

gate2018-cse databases relational-algebra normal

Answer

3.12.24 Relational Algebra: GATE CSE 2019 | Question: 55

<https://gateoverflow.in/302793>



Consider the following relations $P(X, Y, Z)$, $Q(X, Y, T)$ and $R(Y, V)$.

Table: P

X	Y	Z
X1	Y1	Z1
X1	Y1	Z2
X2	Y2	Z2
X2	Y4	Z4

Table: Q

X	Y	T
X2	Y1	2
X1	Y2	5
X1	Y1	6
X3	Y3	1

Table: R

Y	V
Y1	V1
Y3	V2
Y2	V3
Y2	V2

How many tuples will be returned by the following relational algebra query?

$$\Pi_x(\sigma_{(P.Y=R.Y \wedge R.V=V2)}(P \times R)) - \Pi_x(\sigma_{(Q.Y=R.Y \wedge Q.T>2)}(Q \times R))$$

Answer: _____

gate2019-cse numerical-answers databases relational-algebra

Answer 

3.12.25 Relational Algebra: GATE CSE 2021 Set 1 | Question: 27 [top](#)

<https://gateoverflow.in/357424>



The following relation records the age of 500 employees of a company, where *empNo* (indicating the employee number) is the key:

$$empAge(empNo, age)$$

Consider the following relational algebra expression:

$$\Pi_{empNo}(empAge \bowtie_{(age>age1)} \rho_{empNo1,age1}(empAge))$$

What does the above expression generate?

- Employee numbers of only those employees whose age is the maximum
- Employee numbers of only those employees whose age is more than the age of exactly one other employee
- Employee numbers of all employees whose age is not the minimum
- Employee numbers of all employees whose age is the minimum

gate2021-cse-set1 databases relational-algebra

Answer 

3.12.26 Relational Algebra: GATE IT 2005 | Question: 68 [top](#)

<https://gateoverflow.in/3831>



A table 'student' with schema (roll, name, hostel, marks), and another table 'hobby' with schema (roll, hobbyname) contains records as shown below:

Table: student

Roll	Name	Hostel	Marks
1798	Manoj Rathor	7	95
2154	Soumic Banerjee	5	68
2369	Gumma Reddy	7	86
2581	Pradeep pendse	6	92
2643	Suhas Kulkarni	5	78
2711	Nitin Kadam	8	72
2872	Kiran Vora	5	92
2926	Manoj Kunkaliker	5	94
2959	Hemant Karkhanis	7	88
3125	Rajesh Doshi	5	82

Table: hobby

Roll	Hobby Name
1798	chess
1798	music
2154	music
2369	swimming
2581	cricket
2643	chess
2643	hockey
2711	volleyball
2872	football
2926	cricket
2959	photography
3125	music
3125	chess

The following SQL query is executed on the above tables:

```
select hostel
from student natural join hobby
where marks >= 75 and roll between 2000 and 3000;
```

Relations S and H with the same schema as those of these two tables respectively contain the same information as tuples. A new relation S' is obtained by the following relational algebra operation:

$$S' = \Pi_{\text{hostel}}((\sigma_{s.\text{roll}=H.\text{roll}}(\sigma_{\text{marks}>75 \text{ and } \text{roll}>2000 \text{ and } \text{roll}<3000}(S)) \times (H))$$

The difference between the number of rows output by the SQL statement and the number of tuples in S' is

- A. 6
- B. 4
- C. 2
- D. 0

gate2005-it databases sql relational-algebra normal

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Answer

Answers: Relational Algebra

3.12.1 Relational Algebra: GATE CSE 1992 | Question: 13b [top](#)

<https://gateoverflow.in/43581>



✓ OPTIMIZED ANSWER

$$\Pi_{\text{hotel}}((\sigma_{\text{customer}=\text{"Rama"}}(\text{LIKES})) \bowtie \text{SERVES})$$

👍 35 votes

-- Shubham Pandey (5k points)

3.12.2 Relational Algebra: GATE CSE 1994 | Question: 13 [top](#)

<https://gateoverflow.in/2509>



✓

- A. $\pi_{\text{rollno}}(\sigma_{\text{cno.}=322}(\text{REGISTERED_FOR}))$
- B. SELECT year, min(age) FROM STUDENTS GROUP BY year

In the second question we have to find the year and youngest student from that year. So, we have to apply MIN aggregate function on each year (group by year).

👍 31 votes

-- SAKET NANDAN (4.2k points)

3.12.3 Relational Algebra: GATE CSE 1994 | Question: 3.8 [top](#)

<https://gateoverflow.in/2494>



✓ $R - (R - S)$

There is no need to use Union operator here.

Just because they say you can use operators from $(\cup, -)$ we don't need to use both of them.

Also they are saying that **only the minimum number of operators from $(\cup, -)$** which is equivalent to $R \cap S$.

My expression is Minimal.

👍 47 votes

-- Akash Kanase (36k points)

3.12.4 Relational Algebra: GATE CSE 1995 | Question: 27 [top](#)

<https://gateoverflow.in/2666>



✓

A. $\pi_{\text{pname}}(\text{publishers})$

B. $\pi_{\text{authors}}.*(\sigma_{\text{book.pname}=\text{"TECHNICAL PUBLISHERS"}}(\text{book}) \bowtie \text{authors})$

C. $\pi_{\text{book.aname}}(\sigma_{\text{publishers.pcity}=\text{"Madras"}}(\text{publishers}) \bowtie \text{book})$

3.12.5 Relational Algebra: GATE CSE 1996 | Question: 27 top

<https://gateoverflow.in/2779>

- Select the (user# and) titles of the books issued to User# 6
- Select author names of the books issued to users whose home town is Delhi

3.12.6 Relational Algebra: GATE CSE 1997 | Question: 76-a top

<https://gateoverflow.in/19838>

$$\pi_{eno} (\sigma_{EMP.eno=INVOLVED.eno \wedge INVOLVED.pno=3} (EMP \times INVOLVED))$$

3.12.7 Relational Algebra: GATE CSE 1998 | Question: 1.33 top

<https://gateoverflow.in/1670>

This question is an example of **Theta Join**,

$$r \bowtie_{\theta} s = \sigma_{\theta}(r \times s)$$

The join here will be selecting only those tuples where $A = C$ and $B = D$, meaning it is the intersection. D option.

3.12.8 Relational Algebra: GATE CSE 1998 | Question: 27 top

<https://gateoverflow.in/1742>

T_1 will have all the available course numbers

T_2 will have all the course numbers completed by student2310

T_3 will have the combination of all the courses and the courses completed by student2310

$PRE_REQ - T_3$ (set minus operation) will return us all the entries of PRE_REQ which are not there in T_3 ,

Suppose $\langle C_1, C_5 \rangle$ is a particular tuple of $(PRE_REQ - T_3)$,

Now what does it imply? \implies It implies that C_5 is one of the prerequisite course for C_1 which has not been completed by C_5 .

Proof: If student2310 would have completed C_5 then definitely $\langle C_1, C_5 \rangle$ should have been there in T_3 (remember T_3 is the combination of all the courses and the courses completed by student2310) and in that case $(PRE_REQ - T_3)$ can not have $\langle C_1, C_5 \rangle$ as a tuple.

So, for any such $\langle C_1, C_5 \rangle$ tuple, $(\langle C_1, \text{any course id} \rangle)$ of $PRE_REQ - T_3$, C_1 should not be printed as output (Since there is some prerequisite course for C_1 which student2310 has not completed).

Now, suppose we have not got any tuple as a result of $(PRE_REQ - T_3)$ where C_2 is there under cno attribute $(\langle C_2, \text{any course id} \rangle)$, what does it imply? \implies It implies that student2310 has completed all the prerequisite courses C_2 .

Hence, in order to get the final result we need to project cno from $(PRE_REQ - T_3)$ and subtract it from T_1 .

- $T_1 \leftarrow \pi_{cno}(COURSES)$
- $T_2 \leftarrow \rho_{T_2}(\text{std2310completedcourses})(\pi_{cno}(\sigma_{\text{student_no}=2310}(COMPLETED)))$
- $T_3 \leftarrow T_1 \times T_2$
- $T_4 \leftarrow \rho_{T_4}(\text{cno, pre_cno})(PRE_REQ - T_3)$
- Result** $\leftarrow T_1 - \pi_{cno}(T_4)$

3.12.9 Relational Algebra: GATE CSE 1999 | Question: 1.18, ISRO2016-53 top

<https://gateoverflow.in/1471>

Answer is **B**.

Case 1: if there is a common attribute between R and S , and every row of r matches with the each row of s - i.e., it means, the

join attribute has the same value in all the rows of both r and s ,

Case 2: If there is no common attribute between R and S .

0 There is a common attribute between R and S and nothing matches- the join attribute in r and s have no common value.

43 votes

-- Anurag Semwal (6.7k points)

3.12.10 Relational Algebra: GATE CSE 2000 | Question: 1.23, ISRO2016-57 top

<https://gateoverflow.in/647>



✓ Possible solutions, relational algebra:

(a) Join relation using attribute dpart_no.

- $\Pi_{\text{address}}(\text{emp} \bowtie \text{depart})$ OR
- $\Pi_{\text{address}}(\sigma_{\text{emp.depart_no.}=\text{depart.depart_no.}}(\text{emp} \times \text{depart}))$

(b)

- $\Pi_{\text{name}}(\sigma_{\text{emp.depart_no.}=\text{depart.depart_no.} \wedge \text{emp.name}=\text{depart.depart_name}}(\text{emp} \times \text{depart}))$ OR
- $\Pi_{\text{name}}(\text{emp} \bowtie_{\text{emp.name}=\text{depart.depart_name}} \text{depart})$

(d) Let the given department number be x

- $\Pi_{\text{name}}(\sigma_{\text{emp.depart_no.}=\text{depart.depart_no.} \wedge \text{depart_no.}=x}(\text{emp} \times \text{depart}))$ OR
- $\Pi_{\text{name}}(\text{emp} \bowtie_{\text{depart_no.}=x} \text{depart})$

(e) We cannot generate relational algebra of aggregate functions using basic operations. We need extended operations here.

Option (c).

43 votes

-- Mithlesh Upadhyay (4.3k points)

3.12.11 Relational Algebra: GATE CSE 2001 | Question: 1.24 top

<https://gateoverflow.in/717>



✓ The answer is D.

- A. This is a simple select query.
- B. This is the simple query we need to check $X = Y$ in the where clause.
- C. Cycle < 3 . Means cycles of lengths 1 and 2. The cycle of length 1 is easy., the same as self-loop. The cycle of length 2 is also not too hard to compute. Though it'll be a bit more complex, will need to do like (X, Y) & (Y, X) both present and $X! = Y$. We can do this with a constant length (not depending on the number of tuples) RA query.
- D. This is the hardest part. Here we need to find closure of vertices. This will need a kind of loop. If the graph is like a skewed tree, our query must loop for $O(N)$ times. We can't do this with a constant length query here.

Answer: D.

51 votes

-- Akash Kanase (36k points)

3.12.12 Relational Algebra: GATE CSE 2001 | Question: 1.25 top

<https://gateoverflow.in/718>



✓ Answer is C.

C is just the better form of query, more execution friendly because requires less memory while joining. query, given in question takes more time and memory while joining.

34 votes

-- jayendra (6.7k points)

3.12.13 Relational Algebra: GATE CSE 2002 | Question: 15 top

<https://gateoverflow.in/868>



(I will write only useful attributes in relation which are required)

Ex: **INTERVIEW**

company name	student roll
A	1

B	1
C	1
A	2
B	2
A	3

OFFER

company name	student roll
A	1
B	1
C	1
A	2

So the student with rolls 1,2,3 interviewed. Student 1 did sit for all companies, got the job in all companies A,B,C. Student 2 sat for A,B, got job in A only. Student 3 sat for A, did not get.

a) Part i) :

1
2
3

minus

1
2

equals to

3

Π scrollno (Interview) - Π scrollno(Offer)

You got the required student's roll numbers but to print their names, store that in **Temp** and join with Student table.

Π scrollno,sname (Temp \bowtie Student)

a) Part ii) : Those who got interviewed (includes those who got jobs in all,some,none)

Now **interviewed - offer** = those who **did not get** jobs or got in **some**.

B	2
A	3

Now again subtract whatever you got from all students of the interview again

1
2
3

minus

2
3

equals to

1

But note that it is not an intersection. You may think... A-(A-B) so intersection.

But it is not... We are doing A-B on all tuples.

But the next subtraction is done on a particular attribute. (It became distinct since we focused on it only)

Π scrollno (Interview) - Π scrollno(Interview - Offer)

You got the required student's roll numbers but to print their names, store that in **Temp** and join with Student table.

Π scrollno,sname (Temp \bowtie Student)

b) select s.sdegree,AVG(o.osalary) from Student s,Offer o where s.srollno=o.srollno having count(distinct s.srollno)>5 group by

s.degree;

40 votes

-- Ahwan Mishra (10.2k points)

3.12.14 Relational Algebra: GATE CSE 2003 | Question: 30

https://gateoverflow.in/920



select distinct in SQL is equivalent to project and by default relation 1, relation 2 in SQL corresponds to cross-product. So, option A.

40 votes

-- Arjun Suresh (332k points)

3.12.15 Relational Algebra: GATE CSE 2004 | Question: 51

https://gateoverflow.in/1047



OPTION : (D)

The given query states the following conditions:

$$\begin{matrix} \text{Sex} & = & F \wedge \\ x & = & M \wedge \\ \text{Marks} & \leq & m \end{matrix} \rightarrow (1)$$

Let the relation be Student(Name, Sex, Marks)

Name	Sex	Marks
S1	F	30
S2	F	10
S3	M	20

Student(Name, Sex, Marks) Relation is renamed as Student(n, x, m).

Taking the cross product of the relations

No.	Name	Sex	Marks	n	x	m
1	S1	F	30	S1	F	30
2	S1	F	30	S2	F	10
3	S1	F	30	S3	M	20
4	S2	F	10	S1	F	30
5	S2	F	10	S2	F	10
6	S2	F	10	S3	M	20
7	S3	M	20	S1	F	30
8	S3	M	20	S2	M	10
9	S3	M	20	S3	M	30

Selecting the tuple (row#6 from the above table), which satisfies the condition (1) and PROJECTING $\Pi_{name} \Rightarrow$ S2

$$\Pi_{name}(\sigma_{sex=F}(\text{Student})) = \begin{matrix} S1 \\ S2 \end{matrix}$$

Hence, the query:

$$\Pi_{name}[\sigma_{sex=F}(\text{student})] - \Pi_{name} \left[\begin{matrix} \text{student} \bowtie \sigma_{x,x,m}(\text{student}) \\ sex = F \wedge \\ x = M \wedge \\ marks \leq m \end{matrix} \right]$$

$$\begin{matrix} S1 \\ S2 \end{matrix} - \begin{matrix} S2 \end{matrix} = \begin{matrix} S1 \end{matrix}$$

Let us take another relation data of Student(Name, Sex, Marks)

Name	Sex	Marks	
S1	M	100	> highest marks of M student
S2	F	50	> highest marks of F student
S3	M	40	
S4	F	30	

Taking the cross product

No.	Name	Sex	Marks	n	x	m
1	S1	M	100	S1	M	100
2	S1	M	100	S2	F	50
3	S1	M	100	S3	M	40
4	S1	M	100	S4	F	30
5	S2	F	50	S1	M	100
6	S2	F	50	S2	F	50
7	S2	F	50	S3	F	40
8	S2	F	50	S4	F	30
9	S3	M	100	S1	M	100
10	S3	M	100	S2	F	50
11	S3	M	100	S3	M	40
12	S3	M	100	S4	F	30
13	S4	F	30	S1	M	100
14	S4	F	30	S2	F	50
15	S4	F	30	S3	M	40
16	S4	F	30	S4	F	30

Consider the row numbers 5, 13, 15 from the above table,

$\begin{bmatrix} S2 \\ S4 \end{bmatrix} \implies$ Female students who scored less than equal to some Male students.

$\Pi_{name}[\sigma_{sex=F}(\text{Student})] = \begin{bmatrix} S2 \\ S4 \end{bmatrix}$

Hence, the result of the query will be:

$\begin{bmatrix} S2 \\ S4 \end{bmatrix} - \begin{bmatrix} S2 \\ S4 \end{bmatrix} = \{\}$

From the above relational data of table Student(Name, Sex, Marks)

(D) is the correct option

In short,

$\{\geq \text{All boys}\} = | \text{universal} | - | < \text{some M} |$

$\{> \text{All boys}\} = | \text{universal} | - | \leq \text{some M} |$

$\{\geq \text{some boys}\} = | \text{universal} | - | < \text{all M} |$

👍 126 votes

-- Akhil Nadh PC (16.5k points)



STUDENTINFO			ENROLL	
1	A	M	1	C1
2	A	F	2	C1
3	A	F	2	C2
			3	C2

$$\bullet \pi_{courseId}(\sigma_{sex="female"}(\text{studInfo})) \times \pi_{courseId}(\text{enroll})$$

2	C1	2	C1
2	C2	2	C2
3	C1	3	C1
3	C2	3	C2

$$\bullet (\pi_{studId}(\sigma_{sex="female"}(\text{studInfo})) \times \pi_{courseId}(\text{enroll})) - \text{enroll}$$

$$\implies 3 \ C1$$

$$\bullet \pi_{courseId}((\pi_{studId}(\sigma_{sex="female"}(\text{studInfo})) \times \pi_{courseId}(\text{enroll})) - \text{enroll})$$

$$\implies C1$$

C1 is a course id in which not all girl students enrolled.
i.e. a proper subset of girls students appeared.

Hence (B) is the correct answer.

62 votes

-- Digvijay (44.9k points)

Ans is b,

First it does a cross join between female students id and all course ids, then subtract the entries which are already present in enroll table.

Remaining are the courseids which are **NOT** done by **at least one** female student

25 votes

-- Anurag Semwal (6.7k points)

3.12.17 Relational Algebra: GATE CSE 2008 | Question: 68 [top](#)

<https://gateoverflow.in/491>



✓ (d) i, iii, iv

iv) is the expansion for natural join represented with other operators.

Why ii is not equivalent? Consider the following instances of R and S

$R : \{ \langle "1", "abc", "p1", "p2", "p3" \rangle, \langle "2", "xyz", "p1", "p2", "p3" \rangle \}$

$S : \{ \langle "1", "abc", "q1", "q2" \rangle, \langle "2", "def", "q1", "q2" \rangle \}$

Now, consider the given queries:

i. $R \bowtie S$ gives

$\{ \langle "1", "abc", "p1", "p2", "p3", "q1", "q2" \rangle \}$

Projecting P gives $\{ \langle "1" \rangle \}$

ii. $\pi_P(R) \bowtie \pi_P(S)$ gives

$\{ \langle "1" \rangle, \langle "2" \rangle \} \bowtie \{ \langle "1" \rangle, \langle "2" \rangle \}$

$= \{ \langle "1", "2" \rangle \}$

iii. $\Pi_P (\Pi_{P,Q} (R) \cap \Pi_{P,Q} (S))$ gives

$$\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} \cap \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\} = \{\langle "1", "abc" \rangle\}$$

Projecting P gives $\{\langle "1" \rangle\}$

iv. $\Pi_P (\Pi_{P,Q} (R) - (\Pi_{P,Q} (R) - \Pi_{P,Q} (S)))$ gives

$$\begin{aligned} & \{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - (\{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "1", "abc" \rangle, \langle "2", "def" \rangle\}) \\ &= \{\langle "1", "abc" \rangle, \langle "2", "xyz" \rangle\} - \{\langle "2", "xyz" \rangle\} = \{\langle "1", "abc" \rangle\} \end{aligned}$$

Projecting P gives $\{\langle "1" \rangle\}$

👍 72 votes

-- Aravind (2.8k points)

3.12.18 Relational Algebra: GATE CSE 2012 | Question: 43 [top](#)

<https://gateoverflow.in/2151>



✓ Answer is A.

Referential integrity means, all the values in foreign key should be present in primary key.

$r2(c)$ is the super set of $r1(b)$

So, {subset - superset} is always empty set.

👍 38 votes

-- Aravind (2.8k points)

3.12.19 Relational Algebra: GATE CSE 2014 Set 3 | Question: 21 [top](#)

<https://gateoverflow.in/2055>



✓ (A) $\pi_{A1}(\sigma_{F1 \wedge F2}(r))$

since A1 is subset of A2 will get only A1 attributes as it is in the outside, so we can remove project A2.

Two Selects with boolean expression can be combined into one select with And of two boolean expressions.

👍 38 votes

-- Aravind (2.8k points)

3.12.20 Relational Algebra: GATE CSE 2014 Set 3 | Question: 30 [top](#)

<https://gateoverflow.in/2064>



✓ (D) all of his/her dependents.

The inner query selects the employees whose age is less than or equal to at least one of his dependents. So, subtracting from the set of employees, gives employees whose age is greater than all of his dependents.

👍 50 votes

-- Arjun Suresh (332k points)

3.12.21 Relational Algebra: GATE CSE 2015 Set 1 | Question: 7 [top](#)

<https://gateoverflow.in/8094>



✓ Option D is correct because SELECT operation in SQL is equivalent to The projection operation in relational algebra, except that SELECT in SQL retains duplicates but projection gives only distinct.

👍 46 votes

-- Anoop Sonkar (4.1k points)

3.12.22 Relational Algebra: GATE CSE 2017 Set 1 | Question: 46 [top](#)

<https://gateoverflow.in/118329>



✓ ANS) 4

T1 WILL GIVE :-

1. CA
2. CB
3. CC

1. SA
2. SC
3. SD
4. SF

$T_2 = CR \div T_1 =$ All the tuples in CR which are matched with every tuple in T_1 :

//SB IS NOT MATCHED WITH CA, SE IS NOT MATCHED WITH CC

👍 54 votes

classroom.gateoverflow.in
-- jatin saini (4.2k points)

3.12.23 Relational Algebra: GATE CSE 2018 | Question: 41 top ↗

https://gateoverflow.in/204115



✓ Option a, b, d will restrict all record with $B < 5$ but option C will include record with $b \geq 5$ also, so false.

C is answer.

👍 31 votes

classroom.gateoverflow.in gateoverflow.in classroom.gateoverflow.in
-- Prashant Singh (47.2k points)

3.12.24 Relational Algebra: GATE CSE 2019 | Question: 55 top ↗

https://gateoverflow.in/302793



✓ $R \cdot V = V_2$, there are two tuples which have Y parameter as Y_3 and Y_2 .

$P \cdot Y = R \cdot Y$, there are no coincide with Y_3 , and there is one tuple coincide with Y_2 which have X parameter as X_2 .

$$\Pi_X(\sigma_{(P.Y=R.Y \wedge R.V=V_2)}(P \times R)) = \{X_2\}$$

$Q \cdot T > 2$, there are two tuples which have Y parameter as Y_1 and Y_2 which have X parameter as X_1

(there is no need of checking R in this query part !)

$$\Pi_X(\sigma_{(Q.Y=R.Y \wedge Q.T>2)}(Q \times R)) = \{X_1\}$$

$$\Pi_X(\sigma_{(P.Y=R.Y \wedge R.V=V_2)}(P \times R)) - \Pi_X(\sigma_{(Q.Y=R.Y \wedge Q.T>2)}(Q \times R)) = \{X_2\} - \{X_1\} = \{X_2\}$$

Number of Tuples = 1

👍 26 votes

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-- Shaik Masthan (50.4k points)

3.12.25 Relational Algebra: GATE CSE 2021 Set 1 | Question: 27 top ↗

https://gateoverflow.in/357424



✓ **Correct Answer: C**

Whenever a Database Problem intimidating like the above one(maybe it's just me) appears, it's often worth to Dissect the statements for Individual components and build up your arguments from there rather than attempting it head-on by some random example/argument only to get swayed by your hidden biases and choose the wrong answer.

Couple of Basic Ideas:

$\rho_{r1(x,y,...)}$ is the **rename operation** here, it's used to change the name of the *empAge*'s attributes *empNo*, *age* to *empNo1*, *age1* to resolve potential conflicts that can arise while referring the relations'(the table) attributes(column) when using relations that might share a common attribute name.

$\bowtie_{\langle cond \rangle}$ is a combination of σ and \times where we take the Cross Product at First between the two relations and apply the tuple select condition supplied to \bowtie by using σ . So \bowtie equals $\sigma_{\langle cond \rangle}(A \times B)$

$\Pi_{\langle attr \rangle}$ is a Column Select Operation in naive words, it's supplied with attributes that needs to be selected.

A Relation contains only **unique tuples** unlike in conventional SQL Databases.

Now,

1. First the ρ operator renames the RHS relation to *empNo1*, *age1*.
2. We take the cross product of both the relations, each tuple in A (unmodified relation *empAge*) will be combined with every tuple in B (renamed relation *empAge*).
3. We filter the tuples according to the condition $age > age1$ which implies those tuples whose age values in A that are

greater than at least one of B are selected. Since A and B are the same here only those values which aren't the minimum are selected in A are selected ($>$).

4. We find out the set of unique $empNo$ by using Projection (II) (Note: $empNo$ derived from LHS side of \bowtie the original relation A that we were talking about).

Since the $empNo$ is derived from relation A (LHS) whose age attribute is greater than the relation's minimum implies employees from A are selected whose age isn't the minimum hence, Option C is true.

Also, if $empNo1$ was chosen instead of $empNo$ then it would list all the employee numbers whose age isn't the maximum.

1 votes

-- Cringe is my middle name... (885 points)

3.12.26 Relational Algebra: GATE IT 2005 | Question: 68 [top](#)

<https://gateoverflow.in/3831>



✓ SQL query will return:

Roll	Hostel
2369	7
2581	6
2643	5
2643	5
Duplicate Row is present in Hobby table	
2872	5
2926	5
2959	7

Total 7 rows are selected.

In RA only distinct values of hostels are selected i.e. 5, 6, 7

SQL row count - RA row count = $7 - 3 = 4$

Answer is **B**.

66 votes

-- Vikrant Singh (11.2k points)

3.13

Relational Calculus (14) [top](#)

3.13.1 Relational Calculus: GATE CSE 1993 | Question: 23 [top](#)

<https://gateoverflow.in/2320>



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '*':

```
Students (rollno*, sname, saddr)
courses (cno*, cname)
enroll(rollno*, cno*, grade)
teach(tno*, tname, cao*)
```

(cno is course number, cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

Write a SQL query for retrieving roll number and name of students who got A grade in at least one course taught by teacher names Ramesh for the above relational database.

gate1993 databases sql relational-calculus normal descriptive

Answer [⌵](#)

3.13.2 Relational Calculus: GATE CSE 1993 | Question: 24 [top](#)

<https://gateoverflow.in/20351>



The following relations are used to store data about students, courses, enrollment of students in courses and teachers of courses. Attributes for primary key in each relation are marked by '*':

- students(rollno*, sname, saddr)
- courses(cno*, cname)
- enroll(rollno*, cno*, grade)

- $\text{teach}(\text{tno}^*, \text{tname}, \text{cao}^*)$

(cno is course number, cname is course name, tno is teacher number, tname is teacher name, sname is student name, etc.)

For the relational database given above, the following functional dependencies hold:

- $\text{rollno} \rightarrow \text{sname}, \text{saddr}$
- $\text{cno} \rightarrow \text{cname}$
- $\text{tno} \rightarrow \text{tname}$
- $\text{rollno}, \text{cno} \rightarrow \text{grade}$

- Is the database in 3^{rd} normal form (3NF)?
- If yes, prove that it is in 3NF. If not, normalize the relations so that they are in 3NF (without proving).

gate1993 databases sql relational-calculus normal descriptive

Answer

3.13.3 Relational Calculus: GATE CSE 1998 | Question: 2.19 top

<https://gateoverflow.in/1692>



Which of the following query transformations (i.e., replacing the l.h.s. expression by the r.h.s. expression) is incorrect? R_1 and R_2 are relations, C_1 and C_2 are selection conditions and A_1 and A_2 are attributes of R_1 .

- $\sigma_{C_1}(\sigma_{C_2}(R_1)) \rightarrow \sigma_{C_2}(\sigma_{C_1}(R_1))$
- $\sigma_{C_1}(\pi_{A_1}(R_1)) \rightarrow \pi_{A_1}(\sigma_{C_1}(R_1))$
- $\sigma_{C_1}(R_1 \cup R_2) \rightarrow \sigma_{C_1}(R_1) \cup \sigma_{C_1}(R_2)$
- $\pi_{A_1}(\sigma_{C_1}(R_1)) \rightarrow \sigma_{C_1}(\pi_{A_1}(R_1))$

gate1998 databases relational-calculus normal

Answer

3.13.4 Relational Calculus: GATE CSE 1999 | Question: 1.19 top

<https://gateoverflow.in/1472>



The relational algebra expression equivalent to the following tuple calculus expression:

$\{t \mid t \in r \wedge (t[A] = 10 \wedge t[B] = 20)\}$ is

- $\sigma_{(A=10 \vee B=20)}(r)$
- $\sigma_{(A=10)}(r) \cup \sigma_{(B=20)}(r)$
- $\sigma_{(A=10)}(r) \cap \sigma_{(B=20)}(r)$
- $\sigma_{(A=10)}(r) - \sigma_{(B=20)}(r)$

gate1999 databases relational-calculus normal

Answer

3.13.5 Relational Calculus: GATE CSE 2001 | Question: 2.24 top

<https://gateoverflow.in/742>



Which of the relational calculus expression is not safe?

- $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \neg \exists s \in R_2 (t[A] = s[A])\}$
- $\{t \mid \forall u \in R_1 (u[A] = "x" \Rightarrow \exists s \in R_2 (t[A] = s[A] \wedge s[A] = u[A]))\}$
- $\{t \mid \neg(t \in R_1)\}$
- $\{t \mid \exists u \in R_1 (t[A] = u[A]) \wedge \exists s \in R_2 (t[A] = s[A])\}$

gate2001-cse relational-calculus normal databases

Answer



With regards to the expressive power of the formal relational query languages, which of the following statements is true?

- A. Relational algebra is more powerful than relational calculus
- B. Relational algebra has the same power as relational calculus
- C. Relational algebra has the same power as safe relational calculus
- D. None of the above

gate2002-cse databases relational-calculus normal

Answer



Let $R_1(\underline{A}, B, C)$ and $R_2(\underline{D}, E)$ be two relation schema, where the primary keys are shown underlined, and let C be a foreign key in R_1 referring to R_2 . Suppose there is no violation of the above referential integrity constraint in the corresponding relation instances r_1 and r_2 . Which of the following relational algebra expressions would necessarily produce an empty relation?

- A. $\Pi_D(r_2) - \Pi_C(r_1)$
- B. $\Pi_C(r_1) - \Pi_D(r_2)$
- C. $\Pi_D(r_1 \bowtie_{C \neq D} r_2)$
- D. $\Pi_C(r_1 \bowtie_{C=D} r_2)$

gate2004-cse databases relational-calculus easy

Answer



Consider the relation **employee**(name, sex, supervisorName) with *name* as the key, *supervisorName* gives the name of the supervisor of the employee under consideration. What does the following Tuple Relational Calculus query produce?

$\{e.name \mid employee(e) \wedge (\forall x) [\neg employee(x) \vee x.supervisorName \neq e.name \vee x.sex = "male"]\}$

- A. Names of employees with a male supervisor.
- B. Names of employees with no immediate male subordinates.
- C. Names of employees with no immediate female subordinates.
- D. Names of employees with a female supervisor.

gate2007-cse databases relational-calculus normal

Answer



Which of the following tuple relational calculus expression(s) is/are equivalent to $\forall t \in r(P(t))$?

- I. $\neg \exists t \in r(P(t))$
- II. $\exists t \notin r(P(t))$
- III. $\neg \exists t \in r(\neg P(t))$
- IV. $\exists t \notin r(\neg P(t))$

- A. I only
- B. II only
- C. III only
- D. III and IV only

gate2008-cse databases relational-calculus normal

Answer



Let R and S be relational schemes such that $R = \{a, b, c\}$ and $S = \{c\}$. Now consider the following queries on the database:

1. $\pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r))$
2. $\{t \mid t \in \pi_{R-S}(r) \wedge \forall u \in s (\exists v \in r (u = v[S] \wedge t = v[R - S]))\}$
3. $\{t \mid t \in \pi_{R-S}(r) \wedge \forall v \in r (\exists u \in s (u = v[S] \wedge t = v[R - S]))\}$

4.

```
Select R.a, R.b
From R, S
Where R.c = S.c
```

Which of the above queries are equivalent?

- A. 1 and 2
- B. 1 and 3
- C. 2 and 4
- D. 3 and 4

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gate2009-cse databases relational-calculus difficult

Answer



Consider the following relational schema.

- Students(rollno: integer, sname: string)
- Courses(courseno: integer, cname: string)
- Registration(rollno: integer, courseno: integer, percent: real)

Which of the following queries are equivalent to this query in English?

“Find the distinct names of all students who score more than 90% in the course numbered 107”

- I.

```
SELECT DISTINCT S.sname FROM Students as S, Registration
as R WHERE
R.rollno=S.rollno AND R.courseno=107 AND R.percent >90
```
 - II. $\Pi_{sname}(\sigma_{courseno=107 \wedge percent > 90}(Registration \bowtie Students))$
 - III. $\{T \mid \exists S \in Students, \exists R \in Registration (S.rollno = R.rollno \wedge R.courseno = 107 \wedge R.percent > 90 \wedge T.sname = S.sname)\}$
 - IV. $\{\langle S_N \rangle \mid \exists S_R \exists R_P (\langle S_R, S_N \rangle \in Students \wedge \langle S_R, 107, R_P \rangle \in Registration \wedge R_P > 90)\}$
- A. I, II, III and IV
 - B. I, II and III only
 - C. I, II and IV only
 - D. II, III and IV only

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gate2013-cse databases sql relational-calculus normal

Answer



Which of the following relational query languages have the same expressive power?

- I. Relational algebra
 - II. Tuple relational calculus restricted to safe expressions
 - III. Domain relational calculus restricted to safe expressions
- A. II and III only
 - B. I and II only
 - C. I and III only
 - D. I, II and III

gate2006-it databases relational-algebra relational-calculus easy

Answer



Consider a selection of the form $\sigma_{A \leq 100}(r)$, where r is a relation with 1000 tuples. Assume that the attribute values for A among the tuples are uniformly distributed in the interval $[0, 500]$. Which one of the following options is the best estimate of the number of tuples returned by the given selection query ?

- A. 50
- B. 100
- C. 150
- D. 200

gate2007-it

databases

relational-calculus

probability

normal

Answer



Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

Consider the following tuple relational calculus query.

$$\{t \mid \exists E \in \text{Enrolment } t = E.\text{school-id} \wedge \{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t \wedge (\exists B \in \text{ExamResult } B.\text{erollno} = x.\text{erollno})\}$$

If a student needs to score more than 35 marks to pass an exam, what does the query return?

- A. The empty set
- B. schools with more than 35% of its students enrolled in some exam or the other
- C. schools with a pass percentage above 35% over all exams taken together
- D. schools with a pass percentage above 35% over each exam

gate2008-it

databases

relational-calculus

normal

Answer

Answers: Relational Calculus



```
select student.rollno, student.sname
From student natural join enroll on student.rollno=enroll.rollno
Where enroll.grade='A' AND enroll.cno in (select cno from teach where tname='Ramesh')
```

16 votes

-- Aravind (2.8k points)



- ✓ In table teach we have Primary Key (which is automatically a candidate key as well) as (tno, coa). We have the functional dependency $tno \rightarrow tname$ which is a partial functional dependency (a proper subset of candidate key determining a non-key attribute) which violates 2NF requirement and hence 3NF too. So the relational database is not in 3NF.

To make it in 3NF we have to break teach table into (tno*, coa*) and (tno*, tname).

9 votes

-- Taran kushwaha (1.7k points)



- ✓ D) if the selection condition is on attribute A_2 , then we cannot replace it by RHS as there will not be any attribute A_2 due to projection of A_1 only.

44 votes

-- Shaun Patel (6.1k points)

3.13.4 Relational Calculus: GATE CSE 1999 | Question: 1.19 top

<https://gateoverflow.in/1472>



✓ Answer: (C)

Tuple t should have two attributes A and B such that $t.A = 10$ and $t.B = 20$.

So, (Tuples having $A = 10$) \cap (Tuples having $B = 20$) = (Tuples having $A = 10$ and $B = 20$).

26 votes

-- Rajarshi Sarkar (27.9k points)

3.13.5 Relational Calculus: GATE CSE 2001 | Question: 2.24 top

<https://gateoverflow.in/742>



✓ Answer: C.

It returns tuples not belonging to R_1 (which is infinitely many). So, it is not safe.

Reference: http://nptel.ac.in/courses/IIT-MADRAS/Intro_to_Database_Systems_Design/pdf/3.1_Tuple_Relational_Calculus.pdf

References



37 votes

-- Rajarshi Sarkar (27.9k points)

3.13.6 Relational Calculus: GATE CSE 2002 | Question: 1.20 top

<https://gateoverflow.in/825>



✓ Answer: C

Relational algebra has the same power as safe relational calculus as:

- A query can be formulated in safe Relational Calculus if and only if it can be formulated in Relational Algebra.

30 votes

-- Rajarshi Sarkar (27.9k points)

3.13.7 Relational Calculus: GATE CSE 2004 | Question: 13 top

<https://gateoverflow.in/1010>



✓ Answer is (B).

C in R_1 is a foreign key referring to the primary key D in R_2 . So, every element of C must come from some D element.

25 votes

-- Vicky Bajoria (4.1k points)

3.13.8 Relational Calculus: GATE CSE 2007 | Question: 60 top

<https://gateoverflow.in/1258>



✓ OR (\vee) is commutative and associative, therefore i can rewrite given query as:

$\{e.name \mid employee(e) \wedge (\forall x) [\neg employee(x) \vee x.sex = "male" \vee x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [\neg (employee(x) \wedge x.sex \neq "male") \vee x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [(employee(x) \wedge x.sex \neq "male") \Rightarrow x.supervisorName \neq e.name]\}$

$\{e.name \mid employee(e) \wedge (\forall x) [(employee(x) \wedge x.sex = "female") \Rightarrow x.supervisorName \neq e.name]\}$

It is clear now they are saying something about female employees, This query does not say anything about male employees.

Therefore Option A and B are out of consideration.

This query retrieves those $e.name$ who satisfies this condition:

$$\forall x[(employee(x) \wedge x.sex = "female") \Rightarrow x.supervisorName \neq e.name]$$

Means retrieves those $e.name$, who is not a supervisor of any female employees.
i.e it retrieves name of employees with no female subordinate.
(here "immediate" is obvious, as we are checking first level supervisor.)

Hence, option C.

👍 185 votes

-- Sachin Mittal (15.8k points)

3.13.9 Relational Calculus: GATE CSE 2008 | Question: 15 top

<https://gateoverflow.in/413>



✓ Only III is correct.

The given statement means for all tuples from r , P is true. III means there does not exist a tuple in r where P is not true. Both are equivalent.

IV is not correct as it is saying that there exist a tuple, not in r for which P is not true, which is not what the given expression means.

👍 43 votes

-- Arjun Suresh (332k points)

3.13.10 Relational Calculus: GATE CSE 2009 | Question: 45 top

<https://gateoverflow.in/1331>



✓

$$1. \pi_{R-S}(r) - \pi_{R-S}(\pi_{R-S}(r) \times s - \pi_{R-S,S}(r))$$
$$= \pi_{a,b}(r) - \pi_{a,b}(\pi_{a,b}(r) \times s - \pi_R(r))$$

2. Expanding logically the statement means to select $t(a, b)$ from r such that for all tuples u in s , there is a tuple v in r , such that $u = v[S]$ and $t = v[R - S]$. This is just equivalent to (r/s)
3. Expanding logically the statement means that select $t(a, b)$ from r such that for all tuples v in r , there is a tuple u in s , such that $u = v[S]$ and $t = v[R - S]$. This is equivalent to saying to select (a, b) values from r , where the c value is in some tuple of s .
4. This selects (a, b) from all tuples from r which has an equivalent c value in s .

So, 1 and 2 are equivalent.

r		
a	b	c
Arj	TY	12
Arj	TY	14
Cell	TR	13
Tom	TW	12
Ben	TE	14

s
c
12
14

- will give $\langle Arj, TY \rangle$.
- will give $\langle Arj, TY \rangle$.
- will not return any tuple as the c value 13, is not in s .
- will give $\langle Arj, TY \rangle, \langle Arj, TY \rangle, \langle Tom, TW \rangle, \langle Ben, TE \rangle$.

<http://pages.cs.wisc.edu/~dbbook/openAccess/firstEdition/slides/pdfslides/mod311.pdf>

Correct Answer: A

References



61 votes

-- Arjun Suresh (332k points)

3.13.11 Relational Calculus: GATE CSE 2013 | Question: 35 top

https://gateoverflow.in/1546



✓ Answer: A

Four queries given in SQL, RA, TRC and DRC in four statements respectively retrieve the required information.

36 votes

-- Rajarshi Sarkar (27.9k points)

3.13.12 Relational Calculus: GATE IT 2006 | Question: 15 top

https://gateoverflow.in/3554



✓ Answer: D

All are equivalent in expressive power.

21 votes

-- Rajarshi Sarkar (27.9k points)

3.13.13 Relational Calculus: GATE IT 2007 | Question: 65 top

https://gateoverflow.in/3510



✓ $\sigma_{A \leq 100}(r)$
 r has 1000 tuples

Values for A among the tuples are uniformly distributed in the interval [0, 500]. This can be split to 5 mutually exclusive (non-overlapping) and exhaustive (no other intervals) intervals of same width of 100 ([0 - 100], [101 - 200], [201 - 300], [301 - 400], [401 - 500], 0 makes the first interval larger - this must be a typo in question) and we can assume all of them have same number of values due to Uniform distribution. So, number of tuples with A value in first interval should be in

$$\frac{\text{Total no. of tuples}}{5} = 1000/5 = 200$$

Correct Answer: D

35 votes

-- Abhinav Rana (723 points)

3.13.14 Relational Calculus: GATE IT 2008 | Question: 75 top

https://gateoverflow.in/3389



✓ $t \mid \exists E \in \text{Enrolment } t = E.\text{school-id}$

Returns school-ids from Enrolment table SUCH THAT

- $\{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t \wedge (\exists B \in \text{ExamResult } B.\text{erollno} = x.\text{erollno} \wedge B.\text{examname} = x.\text{examname} \wedge$
- **the number of student enrolments from the school for exams with marks > 35 divides**
 - $\{x \mid x \in \text{Enrolment} \wedge x.\text{school-id} = t\}$
 - **total number of student enrolments from the school**
 - $*100 > 35$
 - **percentage of student enrolments with mark > 35 is > 35**

Since to pass an exam > 35 mark is needed, this means selecting the school-ids where the pass percentage of students across all the exams taken together is > 35.

Correct Answer: C.

11 votes

-- gatecse (63.3k points)

3.14 Safe Query (I) top

3.14.1 Safe Query: GATE CSE 2017 Set 1 | Question: 41 top

https://gateoverflow.in/118324



Consider a database that has the relation schemas EMP(EmpId, EmpName, DeptId), and DEPT(DeptName, DeptId). Note that the DeptId can be permitted to be NULL in the relation EMP. Consider the following queries on the database expressed in tuple relational calculus.

- I. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \forall v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$
- II. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] \neq v[\text{DeptId}]))\}$

III. $\{t \mid \exists u \in \text{EMP}(t[\text{EmpName}] = u[\text{EmpName}] \wedge \exists v \in \text{DEPT}(t[\text{DeptId}] = v[\text{DeptId}]))\}$

Which of the above queries are safe?

- A. I and II only
- B. I and III only
- C. II and III only
- D. I, II and III

gate2017-cse-set1 databases relational-calculus safe-query normal

goclasses.in

tests.gatecse.in

Answer

Answers: Safe Query

3.14.1 Safe Query: GATE CSE 2017 Set 1 | Question: 41 top

https://gateoverflow.in/118324



✓ Answer is (D)

before \wedge operation all three expressions are the same,

i.e. return true if for each tuple t we have finite no of tuple u in employee table for which they have same employee_name.

(I) but in 2nd part, for each tuple v in department there may exist infinite no of tuple t for which they may not be equal.

i.e. true for finite no of tuples \wedge true for infinite no of tuples, over all true for finite tuple.

(ii) there may exist infinite no of tuple for which at least one tuple v belongs to department table for which they may not be equal.

i.e. true for finite no of tuples \wedge true for infinite no of tuples, over all true for finite tuple.

(iii) this one actually true for finite no of tuples, as there may exist only finite tuple which may be equal to at least one tuple v in department. bcz department table contain finite no of tuple all tuple t which are same may not be more than all tuple v in department table in case of equality operation.

i.e. true for finite \wedge true for finite tuple, over all true for finite tuple.

so all TRC query will return finite tuple which implies all are safe.

reference: <http://www.cs.sfu.ca/CourseCentral/354/zaiane/material/notes/Chapter3/node14.html>

<http://people.cs.pitt.edu/~chang/156/10calculus.html>

http://www.cs.princeton.edu/courses/archive/fall13/cos597D/notes/relational_calc.pdf

References



47 votes

-- 2018 (5.5k points)

3.15

Sql (51) top

3.15.1 Sql: GATE CSE 1988 | Question: 12iii top

https://gateoverflow.in/94625



Describe the relational algebraic expression giving the relation returned by the following SQL query.

```
Select SNAME
from S
Where SNOin
      (select SNO
       from SP
       where PNOin
            (select PNO
             from P
             Where COLOUR='BLUE'))
```

gate1988 normal descriptive databases sql

Answer

3.15.2 Sql: GATE CSE 1988 | Question: 12iv top

<https://gateoverflow.in/94626>



```
Select      SNAME
from        S
Where       SNOin
            (select  SNO
             from    SP
             where   PNOin
                    (select  PNO
                     from    P
                     where   COLOUR='BLUE' ))
```

What relations are being used in the above SQL query? Given at least two attributes of each of these relations.

gate1988 normal descriptive databases sql

Answer

3.15.3 Sql: GATE CSE 1990 | Question: 10-a top

<https://gateoverflow.in/85686>



Consider the following relational database:

- employees (eno, ename, address, basic-salary)
- projects (pno, pname, nos-of-staffs-allotted)
- working (pno, eno, pjob)

The queries regarding data in the above database are formulated below in SQL. Describe in ENGLISH sentences the two queries that have been posted:

i.

```
SELECT ename
FROM employees
WHERE eno IN
      (SELECT eno
       FROM working
       GROUP BY eno
       HAVING COUNT(*) =
        (SELECT COUNT(*)
         FROM projects))
```

ii.

```
SELECT pname
FROM projects
WHERE pno IN
      (SELECT pno
       FROM projects
       MINUS
       SELECT DISTINCT pno
        FROM working);
```

gate1990 descriptive databases sql

Answer

3.15.4 Sql: GATE CSE 1991 | Question: 12,b top

<https://gateoverflow.in/42998>



Suppose a database consist of the following relations:

```
SUPPLIER (SCODE, SNAME, CITY) .
PART (PCODE, PNAME, PDESC, CITY) .
PROJECTS (PRCODE, PRNAME, PRCITY) .
SPPR (SCODE, PCODE, PRCODE, QTY) .
```

Write algebraic solution to the following :

- Get SCODE values for suppliers who supply to both projects PR1 and PR2.
- Get PRCODE values for projects supplied by at least one supplier not in the same city.

sql gate1991 normal databases descriptive

Answer



Suppose a database consist of the following relations:

```
SUPPLIER (SCODE, SNAME, CITY) .
PART (PCODE, PNAME, PDESC, CITY) .
PROJECTS (PCODE, PRNAME, PCITY) .
SPPR (SCODE, PCODE, PRCODE, QTY) .
```

Write SQL programs corresponding to the following queries:

- Print PCODE values for parts supplied to any project in DEHLI by a supplier in DELHI.
- Print all triples <CITY, PCODE, CITY> such that a supplier in first city supplies the specified part to a project in the second city, but do not print the triples in which the two CITY values are same.

gate1991 databases sql normal descriptive

Answer



Consider the following relational database schema:

- EMP (eno name, age)
- PROJ (pno name)
- INVOLVED (eno, pno)

EMP contains information about employees. PROJ about projects and involved about which employees involved in which projects. The underlined attributes are the primary keys for the respective relations.

State in English (in not more than 15 words)

What the following relational algebra expressions are designed to determine

- $\Pi_{eno}(INVOLVED) - \Pi_{eno}((\Pi_{eno}(INVOLVED) \times \Pi_{pno}(PROJ)) - INVOLVED)$
- $\Pi_{age}(EMP) - \Pi_{age}(\sigma_{E.age < Emp.age}((\rho E(EMP) \times EMP)))$

(Note: $\rho E(EMP)$ conceptually makes a copy of EMP and names it E (ρ is called the rename operator))

gate1997 databases sql descriptive normal

Answer



Suppose we have a database consisting of the following three relations:

- FREQUENTS (student, parlor) giving the parlors each student visits.
- SERVES (parlor, ice-cream) indicating what kind of ice-creams each parlor serves.
- LIKES (student, ice-cream) indicating what ice-creams each student likes.

(Assume that each student likes at least one ice-cream and frequents at least one parlor)

Express the following in SQL:

Print the students that frequent at least one parlor that serves some ice-cream that they like.

gate1998 databases sql descriptive

Answer



Which of the following is/are correct?

- An SQL query automatically eliminates duplicates
- An SQL query will not work if there are no indexes on the relations
- SQL permits attribute names to be repeated in the same relation
- None of the above

gate1999 databases sql easy

Answer

3.15.9 Sql: GATE CSE 1999 | Question: 22-a top

<https://gateoverflow.in/1521>



Consider the set of relations

- EMP (Employee-no. Dept-no, Employee-name, Salary)
- DEPT (Dept-no. Dept-name, Location)

Write an SQL query to:

- Find all employees names who work in departments located at 'Calcutta' and whose salary is greater than Rs.50,000.
- Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000.

gate1999 databases sql easy descriptive

Answer

3.15.10 Sql: GATE CSE 1999 | Question: 22-b top

<https://gateoverflow.in/203572>



Consider the set of relations

- EMP (Employee-no. Dept-no, Employee-name, Salary)
- DEPT (Dept-no. Dept-name, Location)

Write an SQL query to:

Calculate, for each department number, the number of employees with a salary greater than Rs. 1,00,000

gate1999 databases sql descriptive easy

Answer

3.15.11 Sql: GATE CSE 2000 | Question: 2.25 top

<https://gateoverflow.in/672>



Given relations $r(w, x)$ and $s(y, z)$ the result of

```
select distinct w, x
from r, s
```

is guaranteed to be same as r , provided.

- r has no duplicates and s is non-empty
- r and s have no duplicates
- s has no duplicates and r is non-empty
- r and s have the same number of tuples

gate2000-cse databases sql

Answer

3.15.12 Sql: GATE CSE 2000 | Question: 2.26 top

<https://gateoverflow.in/673>



In SQL, relations can contain null values, and comparisons with null values are treated as unknown. Suppose all comparisons with a null value are treated as false. Which of the following pairs is not equivalent?

- $x = 5$ $not(not(x = 5))$
- $x = 5$ $x > 4$ and $x < 6$, where x is an integer
- $x \neq 5$ $not(x = 5)$
- none of the above

gate2000-cse databases sql normal

Answer

3.15.13 Sql: GATE CSE 2000 | Question: 22 [top](#)

<https://gateoverflow.in/693>



Consider a bank database with only one relation

transaction (transno, acctno, date, amount)

The amount attribute value is positive for deposits and negative for withdrawals.

- Define an SQL view TP containing the information (acctno, T1.date, T2.amount) for every pair of transaction T1, T2 and such that T1 and T2 are transaction on the same account and the date of T2 is \leq the date of T1.
- Using only the above view TP, write a query to find for each account the minimum balance it ever reached (not including the 0 balance when the account is created). Assume there is at most one transaction per day on each account and each account has at least one transaction since it was created. To simplify your query, break it up into 2 steps by defining an intermediate view V.

gate2000-cse databases sql normal descriptive

Answer

3.15.14 Sql: GATE CSE 2001 | Question: 2.25 [top](#)

<https://gateoverflow.in/743>



Consider a relation geq which represents "greater than or equal to", that is, $(x, y) \in \text{geq}$ only if $y \geq x$.

```
create table geq
(
  ib integer not null,
  ub integer not null,
  primary key ib,
  foreign key (ub) references geq on delete cascade
);
```

Which of the following is possible if tuple (x, y) is deleted?

- A tuple (z, w) with $z > y$ is deleted
- A tuple (z, w) with $z > x$ is deleted
- A tuple (z, w) with $w < x$ is deleted
- The deletion of (x, y) is prohibited

gate2001-cse databases sql normal

Answer

3.15.15 Sql: GATE CSE 2001 | Question: 21-a [top](#)

<https://gateoverflow.in/762>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Write a relational algebra using $(\Pi, \sigma, \rho, \times)$ to find the list of names which appear more than once in examinee.

gate2001-cse databases sql normal descriptive

Answer

3.15.16 Sql: GATE CSE 2001 | Question: 21-b [top](#)

<https://gateoverflow.in/203574>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Write an SQL query to list the regno of examinees who have a score greater than the average score.

gate2001-cse databases sql normal descriptive

Answer

3.15.17 Sql: GATE CSE 2001 | Question: 21-c [top](#)

<https://gateoverflow.in/203574>



Consider a relation examinee (regno, name, score), where regno is the primary key to score is a real number.

Suppose the relation appears (regno, centr_code) specifies the center where an examinee appears. Write an SQL query to list the centr_code having an examinee of score greater than 80.

gate2001-cse databases sql normal descriptive

Answer

3.15.18 Sql: GATE CSE 2003 | Question: 86 top

<https://gateoverflow.in/969>



Consider the set of relations shown below and the SQL query that follows.

Students: (Roll_number, Name, Date_of_birth)

Courses: (Course_number, Course_name, Instructor)

Grades: (Roll_number, Course_number, Grade)

```
Select distinct Name
from Students, Courses, Grades
where Students.Roll_number=Grades.Roll_number
and Courses.Instructor = 'Korth'
and Courses.Course_number = Grades.Course_number
and Grades.Grade = 'A'
```

Which of the following sets is computed by the above query?

- A. Names of students who have got an A grade in all courses taught by Korth
- B. Names of students who have got an A grade in all courses
- C. Names of students who have got an A grade in at least one of the courses taught by Korth
- D. None of the above

gate2003-cse databases sql easy

Answer

3.15.19 Sql: GATE CSE 2004 | Question: 53 top

<https://gateoverflow.in/1049>



The employee information in a company is stored in the relation

- Employee (name, sex, salary, deptName)

Consider the following SQL query

```
Select deptName
From Employee
Where sex = 'M'
Group by deptName
Having avg(salary) >
(select avg (salary) from Employee)
```

It returns the names of the department in which

- A. the average salary is more than the average salary in the company
- B. the average salary of male employees is more than the average salary of all male employees in the company
- C. the average salary of male employees is more than the average salary of employees in same the department
- D. the average salary of male employees is more than the average salary in the company

gate2004-cse databases sql normal

Answer

3.15.20 Sql: GATE CSE 2005 | Question: 77, ISRO2016-55 top

<https://gateoverflow.in/1400>



The relation **book** (title,price) contains the titles and prices of different books. Assuming that no two books have the same price, what does the following SQL query list?

```
select title
from book as B
where (select count (*)
from book as T
```

where T.price>B.price) < 5

- A. Titles of the four most expensive books
- B. Title of the fifth most inexpensive book
- C. Title of the fifth most expensive book
- D. Titles of the five most expensive books

gate2005-cse databases sql easy isro2016

Answer

3.15.21 Sql: GATE CSE 2006 | Question: 67 top

https://gateoverflow.in/1845



Consider the relation account (customer, balance) where the customer is a primary key and there are no null values. We would like to rank customers according to decreasing balance. The customer with the largest balance gets rank 1. Ties are not broke but ranks are skipped: if exactly two customers have the largest balance they each get rank 1 and rank 2 is not assigned.

Query1:

```
select A.customer, count(B.customer)
from account A, account B
where A.balance <=B.balance
group by A.customer
```

Query2:

```
select A.customer, 1+count(B.customer)
from account A, account B
where A.balance < B.balance
group by A.customer
```

Consider these statements about Query1 and Query2.

1. Query1 will produce the same row set as Query2 for some but not all databases.
2. Both Query1 and Query 2 are a correct implementation of the specification
3. Query1 is a correct implementation of the specification but Query2 is not
4. Neither Query1 nor Query2 is a correct implementation of the specification
5. Assigning rank with a pure relational query takes less time than scanning in decreasing balance order assigning ranks using ODBC.

Which two of the above statements are correct?

- A. 2 and 5
- B. 1 and 3
- C. 1 and 4
- D. 3 and 5

gate2006-cse databases sql normal

Answer

3.15.22 Sql: GATE CSE 2006 | Question: 68 top

https://gateoverflow.in/1846



Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints. Given the following four queries:

Query1:

```
select student from enrolled where student in (select student from paid)
```

Query2:

```
select student from paid where student in (select student from enrolled)
```

Query3:

```
select E.student from enrolled E, paid P where E.student = P.student
```

Query4:

```
select student from paid where exists
(select * from enrolled where enrolled.student = paid.student)
```

Which one of the following statements is correct?

- A. All queries return identical row sets for any database
- B. Query2 and Query4 return identical row sets for all databases but there exist databases for which Query1 and Query2 return different row sets
- C. There exist databases for which Query3 returns strictly fewer rows than Query2
- D. There exist databases for which Query4 will encounter an integrity violation at runtime

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gate2006-cse databases sql normal

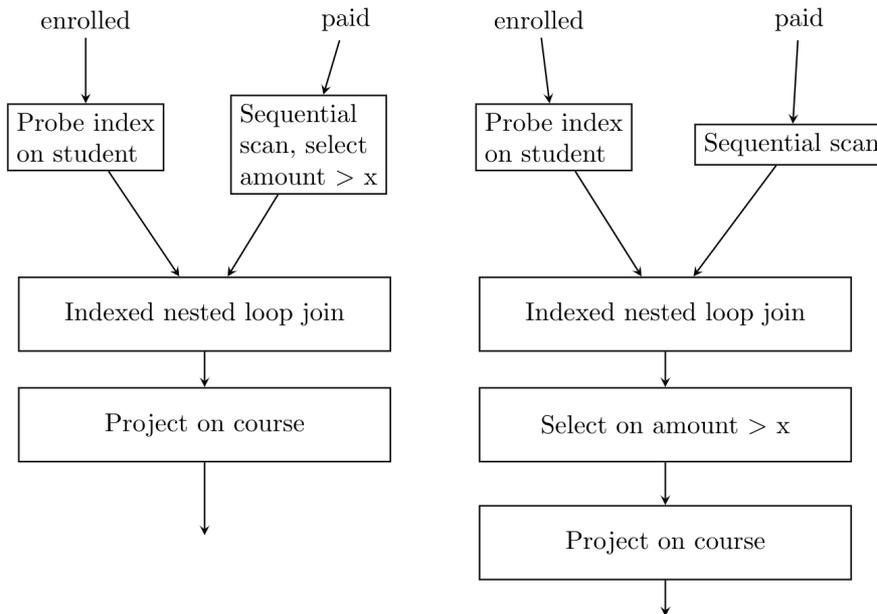
Answer

3.15.23 Sql: GATE CSE 2006 | Question: 69 [top](#)

<https://gateoverflow.in/1947>



Consider the relation enrolled (student, course) in which (student, course) is the primary key, and the relation paid (student, amount) where student is the primary key. Assume no null values and no foreign keys or integrity constraints. Assume that amounts 6000, 7000, 8000, 9000 and 10000 were each paid by 20% of the students. Consider these query plans (Plan 1 on left, Plan 2 on right) to “list all courses taken by students who have paid more than x ”



A disk seek takes $4ms$, disk data transfer bandwidth is $300 MB/s$ and checking a tuple to see if amount is greater than x takes $10\mu s$. Which of the following statements is correct?

- A. Plan 1 and Plan 2 will not output identical row sets for all databases
- B. A course may be listed more than once in the output of Plan 1 for some databases
- C. For $x = 5000$, Plan 1 executes faster than Plan 2 for all databases
- D. For $x = 9000$, Plan 1 executes slower than Plan 2 for all databases

gate2006-cse databases sql normal

Answer

3.15.24 Sql: GATE CSE 2007 | Question: 61 [top](#)

<https://gateoverflow.in/1259>



Consider the table **employee**(empId, name, department, salary) and the two queries Q_1 , Q_2 below. Assuming that department 5 has more than one employee, and we want to find the employees who get higher salary than anyone in the department 5, which one of the statements is **TRUE** for any arbitrary employee table?

```

Q1:
  Select e.empId
  From employee e
  Where not exists
    (Select * From employee s Where s.department = "5" and s.salary >= e.salary)

```

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tests.gatecse.in

```

Select e.empId
From employee e
Q2 : Where e.salary > Any
      (Select distinct salary From employee s Where s.department = "5")

```

- A. Q_1 is the correct query
- B. Q_2 is the correct query
- C. Both Q_1 and Q_2 produce the same answer
- D. Neither Q_1 nor Q_2 is the correct query

gate2007-cse databases sql normal verbal-aptitude

Answer

3.15.25 Sql: GATE CSE 2009 | Question: 55 top

<https://gateoverflow.in/1339>



Consider the following relational schema:

Suppliers(sid:integer, sname:string, city:string, street:string)

Parts(pid:integer, pname:string, color:string)

Catalog(sid:integer, pid:integer, cost:real)

Consider the following relational query on the above database:

```

SELECT S.sname
FROM Suppliers S
WHERE S.sid NOT IN (SELECT C.sid
                   FROM Catalog C
                   WHERE C.pid NOT IN (SELECT P.pid
                                       FROM Parts P
                                       WHERE P.color <> 'blue'))

```

Assume that relations corresponding to the above schema are not empty. Which one of the following is the correct interpretation of the above query?

- A. Find the names of all suppliers who have supplied a non-blue part.
- B. Find the names of all suppliers who have not supplied a non-blue part.
- C. Find the names of all suppliers who have supplied only non-blue part.
- D. Find the names of all suppliers who have not supplied only blue parts.

gate2009-cse databases sql normal

Answer

3.15.26 Sql: GATE CSE 2010 | Question: 19 top

<https://gateoverflow.in/2194>



A relational schema for a train reservation database is given below.

- passenger(pid, pname, age)
- reservation(pid, class, tid)

Passenger			Reservation		
pid	pname	Age	pid	class	tid
0	Sachine	65	0	AC	8200
1	Rahul	66	1	AC	8201
2	Sourav	67	2	SC	8201
3	Anil	69	5	AC	8203
			1	SC	8204
			3	AC	8202

What **pids** are returned by the following SQL query for the above instance of the tables?

```
SELECT pid
FROM Reservation
WHERE class='AC' AND
  EXISTS (SELECT *
          FROM Passenger
          WHERE age>65 AND
                Passenger.pid=Reservation.pid)
```

- A. 1, 0
- B. 1, 2
- C. 1, 3
- D. 1, 5

gate2010-cse databases sql normal

Answer

3.15.27 Sql: GATE CSE 2011 | Question: 32 [top](https://gateoverflow.in/2134) <https://gateoverflow.in/2134>



Consider a database table T containing two columns X and Y each of type integer. After the creation of the table, one record (X=1, Y=1) is inserted in the table.

Let MX and MY denote the respective maximum values of X and Y among all records in the table at any point in time. Using MX and MY, new records are inserted in the table 128 times with X and Y values being MX+1, 2*MY+1 respectively. It may be noted that each time after the insertion, values of MX and MY change.

What will be the output of the following SQL query after the steps mentioned above are carried out?

```
SELECT Y FROM T WHERE X=7;
```

- A. 127
- B. 255
- C. 129
- D. 257

gate2011-cse databases sql normal

Answer

3.15.28 Sql: GATE CSE 2011 | Question: 46 [top](https://gateoverflow.in/2148) <https://gateoverflow.in/2148>



Database table by name Loan_Records is given below.

Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Suresh	Ramgopal	5000.00
Mahesh	Sunderajan	7000.00

What is the output of the following SQL query?

```
SELECT count(*)
FROM (
  SELECT Borrower, Bank_Manager FROM Loan_Records) AS S
NATURAL JOIN
(SELECT Bank_Manager, Loan_Amount FROM Loan_Records) AS T
);
```

- A. 3
- B. 9
- C. 5
- D. 6

gate2011-cse databases sql normal

Answer

3.15.29 Sql: GATE CSE 2012 | Question: 15 [top](https://gateoverflow.in/47) <https://gateoverflow.in/47>



Which of the following statements are **TRUE** about an SQL query?
 P : An SQL query can contain a HAVING clause even if it does not have a GROUP BY clause

Q : An SQL query can contain a HAVING clause only if it has a GROUP BY clause
 R : All attributes used in the GROUP BY clause must appear in the SELECT clause
 S : Not all attributes used in the GROUP BY clause need to appear in the SELECT clause

- A. P and R
- B. P and S
- C. Q and R
- D. Q and S

gate2012-cse databases easy sql ambiguous

Answer

3.15.30 Sql: GATE CSE 2012 | Question: 51 top

https://gateoverflow.in/43313



Consider the following relations *A*, *B* and *C* :

A		
Id	Name	Age
12	Arun	60
15	Shreya	24
99	Rohit	11

B		
Id	Name	Age
15	Shreya	24
25	Hari	40
98	Rohit	20
99	Rohit	11

C		
Id	Phone	Area
10	2200	02
99	2100	01

How many tuples does the result of the following SQL query contain?

```
SELECT A.Id
FROM A
WHERE A.Age > ALL (SELECT B.Age
                  FROM B
                  WHERE B.Name = 'Arun')
```

- A. 4
- B. 3
- C. 0
- D. 1

gate2012-cse databases sql normal

Answer

3.15.31 Sql: GATE CSE 2014 Set 1 | Question: 22 top

https://gateoverflow.in/1789



Given the following statements:

- S1: A foreign key declaration can always be replaced by an equivalent check assertion in SQL.
- S2: Given the table $R(a, b, c)$ where a and b together form the primary key, the following is a valid table definition.

```
CREATE TABLE S (
  a INTEGER,
  d INTEGER,
  e INTEGER,
  PRIMARY KEY (d),
  FOREIGN KEY (a) references R)
```

Which one of the following statements is **CORRECT**?

- A. S1 is TRUE and S2 is FALSE
- B. Both S1 and S2 are TRUE
- C. S1 is FALSE and S2 is TRUE
- D. Both S1 and S2 are FALSE

gate2014-cse-set1 databases normal sql

Answer

3.15.32 Sql: GATE CSE 2014 Set 1 | Question: 54 top

https://gateoverflow.in/1934



Given the following schema:

employees(emp-id, first-name, last-name, hire-date, dept-id, salary)

departments(dept-id, dept-name, manager-id, location-id)

You want to display the last names and hire dates of all latest hires in their respective departments in the location ID 1700. You issue the following query:

```
SQL>SELECT last-name, hire-date
FROM employees
WHERE (dept-id, hire-date) IN
(SELECT dept-id, MAX(hire-date)
FROM employees JOIN departments USING(dept-id)
WHERE location-id =1700
GROUP BY dept-id);
```

What is the outcome?

- A. It executes but does not give the correct result
- B. It executes and gives the correct result.
- C. It generates an error because of pairwise comparison.
- D. It generates an error because of the GROUP BY clause cannot be used with table joins in a sub-query.

gate2014-cse-set1 databases sql normal

Answer

3.15.33 Sql: GATE CSE 2014 Set 2 | Question: 54 top

<https://gateoverflow.in/2021>



SQL allows duplicate tuples in relations, and correspondingly defines the multiplicity of tuples in the result of joins. Which one of the following queries always gives the same answer as the nested query shown below:

```
select * from R where a in (select S.a from S)
```

- A. select R.* from R, S where R.a=S.a
- B. select distinct R.* from R,S where R.a=S.a
- C. select R.* from R,(select distinct a from S) as S1 where R.a=S1.a
- D. select R.* from R,S where R.a=S.a and is unique R

gate2014-cse-set2 databases sql normal

Answer

3.15.34 Sql: GATE CSE 2014 Set 3 | Question: 54 top

<https://gateoverflow.in/2089>



Consider the following relational schema:

employee (empId,empName,empDept)

customer (custId,custName,salesRepId,rating)

salesRepId is a foreign key referring to **empId** of the employee relation. Assume that each employee makes a sale to at least one customer. What does the following query return?

```
SELECT empName FROM employee E
WHERE NOT EXISTS (SELECT custId
FROM customer C
WHERE C.salesRepId = E.empId
AND C.rating <> 'GOOD');
```

- A. Names of all the employees with at least one of their customers having a 'GOOD' rating.
- B. Names of all the employees with at most one of their customers having a 'GOOD' rating.
- C. Names of all the employees with none of their customers having a 'GOOD' rating.
- D. Names of all the employees with all their customers having a 'GOOD' rating.

gate2014-cse-set3 databases sql easy

Answer

3.15.35 Sql: GATE CSE 2015 Set 1 | Question: 27 top

<https://gateoverflow.in/8225>



Consider the following relation:

Student	
Roll_No	Student_Name
1	Raj
2	Rohit
3	Raj

Performance		
Roll_No	Course	Marks
1	Math	80
1	English	70
2	Math	75
3	English	80
2	Physics	65
3	Math	80

Consider the following SQL query.

```
SELECT S.Student_Name, Sum(P.Marks)
FROM Student S, Performance P
WHERE S.Roll_No= P.Roll_No
GROUP BY S.STUDENT_Name
```

The numbers of rows that will be returned by the SQL query is _____.

gate2015-cse-set1 databases sql normal numerical-answers

Answer

3.15.36 Sql: GATE CSE 2015 Set 3 | Question: 3 top

https://gateoverflow.in/8396



Consider the following relation

Cinema(*theater, address, capacity*)

Which of the following options will be needed at the end of the SQL query

```
SELECT P1.address
FROM Cinema P1
```

such that it always finds the addresses of theaters with maximum capacity?

- A. WHERE P1.capacity >= All (select P2.capacity from Cinema P2)
- B. WHERE P1.capacity >= Any (select P2.capacity from Cinema P2)
- C. WHERE P1.capacity > All (select max(P2.capacity) from Cinema P2)
- D. WHERE P1.capacity > Any (select max(P2.capacity) from Cinema P2)

gate2015-cse-set3 databases sql normal

Answer

3.15.37 Sql: GATE CSE 2016 Set 2 | Question: 52 top

https://gateoverflow.in/39604



Consider the following database table named water_schemes:

Water_schemes		
scheme_no	district_name	capacity
1	Ajmer	20
1	Bikaner	10
2	Bikaner	10
3	Bikaner	20
1	Churu	10
2	Churu	20
1	Dungargarh	10

The number of tuples returned by the following SQL query is _____.

```
with total (name, capacity) as
select district_name, sum (capacity)
from water_schemes
group by district_name
with total_avg (capacity) as
select avg (capacity)
```

```
from total
select name
from total, total_avg
where total.capacity >= total_avg.capacity
```

gate2016-cse-set2

databases

sql

normal

numerical-answers

Answer

3.15.38 Sql: GATE CSE 2017 Set 1 | Question: 23

<https://gateoverflow.in/118303>



Consider a database that has the relation schema EMP (EmpId, EmpName, and DeptName). An instance of the schema EMP and a SQL query on it are given below:

EMP		
EmpId	EmpName	DeptName
1	XYA	AA
2	XYB	AA
3	XYC	AA
4	XYD	AA
5	XYE	AB
6	XYF	AB
7	XYG	AB
8	XYH	AC
9	XYI	AC
10	XYJ	AC
11	XYK	AD
12	XYL	AD
13	XYM	AE

```
SELECT AVG (EC.Num)
FROM EC
WHERE (DeptName, Num) IN
  (SELECT DeptName, COUNT(EmpId) AS
    EC(DeptName, Num)
   FROM EMP
   GROUP BY DeptName)
```

The output of executing the SQL query is _____ .

gate2017-cse-set1

databases

sql

numerical-answers

Answer

3.15.39 Sql: GATE CSE 2017 Set 2 | Question: 46

<https://gateoverflow.in/118391>



Consider the following database table named top_scorer .

top_scorer

player	country	goals
Klose	Germany	16
Ronaldo	Brazil	15
G Muller	Germany	14
Fontaine	France	13
Pele	Brazil	12
Klinsmann	Germany	11
Kocsis	Hungary	11
Batistuta	Argentina	10
Cubillas	Peru	10
Lato	Poland	10
Lineker	England	10
T Muller	Germany	10
Rahn	Germany	10

Consider the following SQL query:

```
SELECT ta.player FROM top_scorer AS ta
WHERE ta.goals > ALL (SELECT tb.goals
FROM top_scorer AS tb
WHERE tb.country = 'Spain')
AND ta.goals > ANY (SELECT tc.goals
FROM top_scorer AS tc
WHERE tc.country='Germany')
```

The number of tuples returned by the above SQL query is _____

gate2017-cse-set2 databases sql numerical-answers

Answer

3.15.40 Sql: GATE CSE 2018 | Question: 12

<https://gateoverflow.in/204086>



Consider the following two tables and four queries in SQL.

Book (isbn, bname), Stock(isbn, copies)

Query 1:

```
SELECT B.isbn, S.copies FROM Book B INNER JOIN Stock S ON B.isbn=S.isbn;
```

Query 2:

```
SELECT B.isbn, S.copies FROM Book B LEFT OUTER JOIN Stock S ON B.isbn=S.isbn;
```

Query 3:

```
SELECT B.isbn, S.copies FROM Book B RIGHT OUTER JOIN Stock S ON B.isbn=S.isbn
```

Query 4:

```
SELECT B.isbn, S.copies FROM Book B FULL OUTER JOIN Stock S ON B.isbn=S.isbn
```

Which one of the queries above is certain to have an output that is a superset of the outputs of the other three queries?

- A. Query 1
- B. Query 2
- C. Query 3
- D. Query 4

gate2018-cse databases sql easy

Answer

3.15.41 Sql: GATE CSE 2019 | Question: 51

<https://gateoverflow.in/302797>



A relational database contains two tables Student and Performance as shown below:

Table: student

Roll_no	Student_name
1	Amit
2	Priya
3	Vinit
4	Rohan
5	Smita

Table: Performance

Roll_no	Subject_code	Marks
1	A	86
1	B	95
1	C	90
2	A	89
2	C	92
3	C	80

The primary key of the Student table is Roll_no. For the performance table, the columns Roll_no. and Subject_code together form the primary key. Consider the SQL query given below:

```
SELECT S.Student_name, sum(P.Marks)
FROM Student S, Performance P
WHERE P.Marks >84
GROUP BY S.Student_name;
```

The number of rows returned by the above SQL query is _____

gate2019-cse numerical-answers databases sql

Answer

3.15.42 Sql: GATE CSE 2020 | Question: 13 top

https://gateoverflow.in/333218



Consider a relational database containing the following schemas.

Catalogue

sno	pno	cost
S1	P1	150
S1	P2	50
S1	P3	100
S2	P4	200
S2	P5	250
S3	P1	250
S3	P2	150
S3	P5	300
S3	P4	250

Suppliers

sno	sname	location
S1	M/s Royal furniture	Delhi
S2	M/s Balaji furniture	Bangalore
S3	M/s Premium furniture	Chennai

Parts

pno	pname	part_spec
P1	Table	Wood
P2	Chair	Wood
P3	Table	Steel
P4	Almirah	Steel
P5	Almirah	Wood

The primary key of each table is indicated by underlining the constituent fields.

```
SELECT s.sno, s.sname
FROM Suppliers s, Catalogue c
WHERE s.sno=c.sno AND
cost > (SELECT AVG(cost)
FROM Catalogue
WHERE pno = 'P4'
GROUP BY pno);
```

The number of rows returned by the above SQL query is

- A. 4
- B. 5
- C. 0
- D. 2

gate2020-cse databases sql

Answer

3.15.43 Sql: GATE CSE 2021 Set 1 | Question: 23 top

https://gateoverflow.in/357428



A relation $r(A, B)$ in a relational database has 1200 tuples. The attribute A has integer values ranging from 6 to 20, and the attribute B has integer values ranging from 1 to 20. Assume that the attributes A and B are independently distributed.

The estimated number of tuples in the output of $\sigma_{(A>10) \vee (B=18)}(r)$ is _____.

gate2021-cse-set1 databases sql numerical-answers

Answer

3.15.44 Sql: GATE CSE 2021 Set 2 | Question: 31 top

https://gateoverflow.in/357509



The relation scheme given below is used to store information about the employees of a company, where `empId` is the key and `deptId` indicates the department to which the employee is assigned. Each employee is assigned to exactly one department.

`emp(empId, name, gender, salary, deptId)`

Consider the following SQL query:

```
select deptId, count(*)
from emp
where gender = 'female' and salary > (select avg(salary) from emp)
group by deptId;
```

The above query gives, for each department in the company, the number of female employees whose salary is greater than the average salary of

- A. employees in the department
- B. employees in the company
- C. female employees in the department
- D. female employees in the company

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gate2021-cse-set2 databases sql easy

Answer

3.15.45 Sql: GATE IT 2004 | Question: 74 top

https://gateoverflow.in/3718



A relational database contains two tables `student` and `department` in which `student` table has columns `roll_no`, `name` and `dept_id` and `department` table has columns `dept_id` and `dept_name`. The following insert statements were executed successfully to populate the empty tables:

```
Insert into department values (1, 'Mathematics')
Insert into department values (2, 'Physics')
Insert into student values (1, 'Navin', 1)
Insert into student values (2, 'Mukesh', 2)
Insert into student values (3, 'Gita', 1)
```

How many rows and columns will be retrieved by the following SQL statement?

```
Select * from student, department
```

- A. 0 row and 4 columns
- B. 3 rows and 4 columns
- C. 3 rows and 5 columns
- D. 6 rows and 5 columns

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gate2004-it databases sql normal

Answer

3.15.46 Sql: GATE IT 2004 | Question: 76 top

https://gateoverflow.in/3720



A table `T1` in a relational database has the following rows and columns:

Roll no.	Marks
1	10
2	20
3	30
4	NULL

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The following sequence of SQL statements was successfully executed on table `T1`.

```
Update T1 set marks = marks + 5
Select avg(marks) from T1
```

What is the output of the select statement?

- A. 18.75
- B. 20
- C. 25
- D. Null

gate2004-it databases sql normal

Answer

3.15.47 Sql: GATE IT 2004 | Question: 78 top

https://gateoverflow.in/3722



Consider two tables in a relational database with columns and rows as follows:

Roll_no	Name	Dept_id
1	ABC	1
2	DEF	1
3	GHI	2
4	JKL	3

Dept_id	Dept_name
1	A
2	B
3	C

Roll_no is the primary key of the Student table, Dept_id is the primary key of the Department table and Student.Dept_id is a foreign key from Department.Dept_id

What will happen if we try to execute the following two SQL statements?

- i. update Student set Dept_id = Null where Roll_on = 1
- ii. update Department set Dept_id = Null where Dept_id = 1

- A. Both i and ii will fail
- B. i will fail but ii will succeed
- C. i will succeed but ii will fail
- D. Both i and ii will succeed

gate2004-it databases sql normal

Answer

3.15.48 Sql: GATE IT 2005 | Question: 69 top

https://gateoverflow.in/3832



In an inventory management system implemented at a trading corporation, there are several tables designed to hold all the information. Amongst these, the following two tables hold information on which items are supplied by which suppliers, and which warehouse keeps which items along with the stock-level of these items.

Supply = (supplierid, itemcode)

Inventory = (itemcode, warehouse, stocklevel)

For a specific information required by the management, following SQL query has been written

```
Select distinct STMP.supplierid
From Supply as STMP
Where not unique (Select ITMP.supplierid
                  From Inventory, Supply as ITMP
                  Where STMP.supplierid = ITMP.supplierid
                  And ITMP.itemcode = Inventory.itemcode
                  And Inventory.warehouse = 'Nagpur');
```

For the warehouse at Nagpur, this query will find all suppliers who

- A. do not supply any item
- B. supply exactly one item
- C. supply one or more items
- D. supply two or more items

gate2005-it databases sql normal

Answer

3.15.49 Sql: GATE IT 2006 | Question: 84 top

https://gateoverflow.in/3640



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are did and

cid respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Amoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

did	Cid	day
22	101	10 / 10 / 06
22	102	10 / 10 / 06
22	103	08 / 10 / 06
22	104	07 / 10 / 06
31	102	10 / 11 / 16
31	103	06 / 11 / 16
31	104	12 / 11 / 16
64	101	05 / 09 / 06
64	102	08 / 09 / 06
74	103	08 / 09 / 06

C: Cars relation

Cid	Cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

What is the output of the following SQL query?

```

select D.dname
from Drivers D
where D.did in (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
)
    
```

- A. Karthikeyan, Boris
- B. Sachin, Salman
- C. Karthikeyan, Boris, Sachin
- D. Schumacher, Senna

gate2006-it databases sql normal

Answer

3.15.50 Sql: GATE IT 2006 | Question: 85 top

<https://gateoverflow.in/3641>



Consider a database with three relation instances shown below. The primary keys for the Drivers and Cars relation are *did* and *cid* respectively and the records are stored in ascending order of these primary keys as given in the tables. No indexing is available in the database.

D: Drivers relation

did	dname	rating	age
22	Karthikeyan	7	25
29	Salman	1	33
31	Boris	8	55
32	Arnoldt	8	25
58	Schumacher	10	35
64	Sachin	7	35
71	Senna	10	16
74	Sachin	9	35
85	Rahul	3	25
95	Ralph	3	53

R: Reserves relation

did	Cid	day
22	101	10 - 10 - 06
22	102	10 - 10 - 06
22	103	08 - 10 - 06
22	104	07 - 10 - 06
31	102	10 - 11 - 16
31	103	06 - 11 - 16
31	104	12 - 11 - 16
64	101	05 - 09 - 06
64	102	08 - 09 - 06
74	103	08 - 09 - 06

C: Cars relation

Cid	Cname	colour
101	Renault	blue
102	Renault	red
103	Ferrari	green
104	Jaguar	red

```

select D.dname
from Drivers D
where D.did in
    (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
    )

```

Let n be the number of comparisons performed when the above SQL query is optimally executed. If linear search is used to locate a tuple in a relation using primary key, then n lies in the range:

- A. 36 - 40
- B. 44 - 48
- C. 60 - 64
- D. 100 - 104

gate2006-it databases sql normal

Answer 

3.15.51 Sql: GATE IT 2008 | Question: 74 [top](#)

<https://gateoverflow.in/3388>



Consider the following relational schema:

- Student(school-id, sch-roll-no, sname, saddress)
- School(school-id, sch-name, sch-address, sch-phone)
- Enrolment(school-id, sch-roll-no, erollno, examname)
- ExamResult(erollno, examname, marks)

What does the following SQL query output?

```

SELECT sch-name, COUNT (*)
FROM School C, Enrolment E, ExamResult R
WHERE E.school-id = C.school-id

```

```

AND
E.examname = R.examname AND E.erollno = R.erollno
AND
R.marks = 100 AND S.school-id IN (SELECT school-id
                                FROM student
                                GROUP BY school-id
                                HAVING COUNT (*) > 200)
GROUP By school-id

```

- A. for each school with more than 200 students appearing in exams, the name of the school and the number of 100s scored by its students
- B. for each school with more than 200 students in it, the name of the school and the number of 100s scored by its students
- C. for each school with more than 200 students in it, the name of the school and the number of its students scoring 100 in at least one exam
- D. nothing; the query has a syntax error

gate2008-it databases sql normal

Answer

Answers: Sql

3.15.1 Sql: GATE CSE 1988 | Question: 12iii top 9

<https://gateoverflow.in/94625>



```
select PNO from P Where COLOUR='BLUE';
```

This can be written as: $\pi_{pno}(\sigma_{colour='Blue'}(P))$

Store this in T1.

$\therefore T1 \leftarrow \pi_{pno}(\sigma_{colour='Blue'}(P))$

Then

```
select SNO from SP
where PNOin (select PNO from P
            Where COLOUR='BLUE')
```

$T2 \leftarrow \pi_{sno}(\sigma_{pno=T1}(SP))$

Similary

```
Select SNAME from S
Where SNOin (select SNO from SP
            where PNOin (select PNO from P
                        Where COLOUR='BLUE'));
```

$Result \leftarrow \pi_{sname}(\sigma_{sno=T2}(S))$

4 votes

-- Sourabh Gupta (4k points)

3.15.2 Sql: GATE CSE 1988 | Question: 12iv top 9

<https://gateoverflow.in/94626>



✓ There are 3 relations here:

- S(SNAME, SNO)
- SP(SNO, PNO)
- P(PNO, COLOUR)

9 votes

-- Akash Dinkar (27.9k points)

3.15.3 Sql: GATE CSE 1990 | Question: 10-a top 9

<https://gateoverflow.in/85686>



✓

```

1.SELECT ename
FROM employees
WHERE eno IN
        (SELECT eno
         FROM working
         GROUP BY eno
         HAVING COUNT (*) =

```

```

(SELECT COUNT (*)
 FROM projects));

```

This will return : Employee name who is working for all projects.

(ii)

```
SELECT pname
FROM projects
WHERE pno IN
      (SELECT pno
       FROM projects
       MINUS
       SELECT DISTINCT pno
       FROM working);
```

This will return : Project name for which no employee is working.

33 votes

-- Prashant Singh (47.2k points)

3.15.4 Sql: GATE CSE 1991 | Question: 12,b top 3

https://gateoverflow.in/4298



PCODE values for suppliers who supply to both projects PR1 and PR2 -

$$\Pi_{\text{score}, \text{prcode}}(SPPR) \div \Pi_{\text{prcode}}(\sigma_{\text{prname}=\text{pr1} \vee \text{prname}=\text{pr2}}(PROJECTS))$$

PCODE values for projects supplied by at least one supplier not in the same city -

$$\Pi_{\text{prcode}}(\sigma_{\text{city} <> \text{prcity}}((SUPPLIER * SPPR) * PROJECTS))$$

* is natural join.

8 votes

-- Ashish verma (7.2k points)

3.15.5 Sql: GATE CSE 1991 | Question: 12-a top 3

https://gateoverflow.in/539



✓

i. Print PCODE values for parts supplied to any project in DELHI by a supplier in DELHI

```
Select SP.PCODE
From SPPR SP, Projects PR, Supplier SU
Where SP.PCODE = PR.PCODE
and SU.Scode = SP.Scode
and PR.PRcity = "DELHI"
and SU.city = "DELHI";
```

ii. Print all triples <CITY, PCODE, CITY>

```
Select SU.city, SP.Pcode, PR.PRcity
from Supplier SU, Projects PR, SPPR SP
Where SU.Scode = SP.Scode
And PR.PRcode = SP.PRcode
And SU.city <> PR.PRcity;
```

22 votes

-- Manu Thakur (34k points)

3.15.6 Sql: GATE CSE 1997 | Question: 76-b top 3

https://gateoverflow.in/203570



✓

i. $\Pi_{\text{eno}}(INVOLVED) - \Pi_{\text{eno}}((\Pi_{\text{eno}}(INVOLVED) \times \Pi_{\text{pno}}(PROJ) - INVOLVED)$

- $\Pi_{\text{eno}}(INVOLVED)$ - All employees involved in projects → (A)
- $\Pi_{\text{eno}}((\Pi_{\text{eno}}(INVOLVED) \times \Pi_{\text{pno}}(PROJ) - INVOLVED)$ - gives all employee who are not involved in at least one project. → (B)
- $A - B =$ **employee No. of employees involved on the all project. (Division Operator)**

ii. $\Pi_{\text{age}}(EMP) - \Pi_{\text{age}}(\sigma_{\text{Eage} < \text{EMP.age}}(\rho E(EMP) \times EMP))$

- $\Pi_{\text{age}}(EMP)$ - Age of all employees → (C)
- $\Pi_{\text{age}}(\sigma_{\text{Eage} < \text{EMP.age}}(\rho E(EMP) \times EMP))$ - Employees who have age less than at least one other employee → (D)
- $C - D =$ **Maximum of all ages of employees.**

14 votes

-- Prashant Singh (47.2k points)



```
SELECT DISTINCT A.student FROM
FREQUENTS A, SERVES B, LIKES C
WHERE
  A.parlor=B.parlor
  AND
  B.ice-cream=C.ice-cream
  AND
  A.student=C.student;
```

OR

```
SELECT DISTINCT A.student FROM FREQUENTS A
WHERE
  parlor IN
  (SELECT parlor FROM SERVES B
   WHERE B.ice-cream IN
    (SELECT ice-cream
     FROM LIKES C
     WHERE C.student = A.student));
```

40 votes

-- Arjun Suresh (332k points)



(D)

SQL wont remove duplicates like relational algebra projection, we have to remove it explicitly by distinct.

If there are no indexes on the relation SQL will either chose one/more on its own or simply work without any index. No index would just slow the query but it will surely work.

SQL does not permit 2 attributes to have same name in a relation.

48 votes

-- Aravind (2.8k points)



(a)

```
select Employee-name
from EMP, DEPT
where Salary>50000 and EMP.Dept-no=DEPT.Dept-no and Location="Calcutta"
```

(b)

```
select Dept-no, count(*)
from EMP where salary > 100000
group by Dept-no
```

30 votes

-- Aravind (2.8k points)



```
SELECT Dept-no, count(Employee-no) as total_employees
FROM EMP
WHERE Salary > 100000
GROUP BY Dept-no
```

4 votes

-- balraj_allam (95 points)



This question is about SQL, in SQL Relations are **MULTISET**, not SET. So, R or S can have duplicated.

Answer: A.

A. If R has duplicates, in that case, due to distinct keyword those duplicates will be eliminated in final result. So, R can not have duplicates. If S is empty RXS becomes empty, so S must be non empty. This is true.

B. Here, assume that S is empty. (No duplicates.) Then R X S will be empty. SO this is false.

C. Same argument as B.

D. Assume that R has duplicates. Then Distinct keyword will remove duplicates. So, result of query $\neq R$, so This is false.

73 votes

-- Akash Kanase (36k points)

3.15.12 Sql: GATE CSE 2000 | Question: 2.26

https://gateoverflow.in/673

Answer is option C.

Value at hand	Option A	Option B	Option C
6	× ×	× ×	✓ ✓
5	✓ ✓	✓ ✓	× ×
NULL	× ×	× ×	× ✓

68 votes

-- Amar Vashishth (25.2k points)

3.15.13 Sql: GATE CSE 2000 | Question: 22

https://gateoverflow.in/693

a.

```
Create view TP(T1.acctno, T1.date, T2.amount)
as (Select T1.acctno, T1.date, T2.amount
    from Transaction T1, Transaction T2
    where T1.acctno = T2.acctno
    and T2.date <= T1.date);
```

b.

i.

```
Create view V(acctno, date, balance)
as (select acctno, date, sum(amount)
    from TP
    group by acctno, date);
```

ii.

```
select acctno, min(balance)
from V
group by acctno;
```

7 votes

-- Sourabh Gupta (4k points)

3.15.14 Sql: GATE CSE 2001 | Question: 2.25

https://gateoverflow.in/743

Answer: C

The table can be depicted as:

ib(PK)	ub(FK)
z	w = u
u	v = x
x	y

If (x, y) is deleted then from the above table:

- $v \leq y$ (as $v = x$)
- $u < v \leq y, u! = v$ (as $v = x$ and ib is the Primary Key)
- $w < v \leq y$ (as $w = u$)
- $z < w < v \leq y, z! = w$ (as $w = u$ and ib is the Primary Key)

As, it can be seen that $w < v$ or $w < x$ (as $v = x$) so C is the answer.

34 votes

-- Rajarshi Sarkar (27.9k points)

3.15.15 Sql: GATE CSE 2001 | Question: 21-a [top](#)

<https://gateoverflow.in/762>



✓ $\pi_{\text{exm1.name}}(\sigma_{(\text{exm1.regno} \neq \text{examinee.regno}) \wedge (\text{emp1.name} = \text{emp2.name})})(\rho_{\text{exm1}}(\text{examinee}) \times \text{examinee})$

16 votes

-- Tauhin Gangwar (6.7k points)

3.15.16 Sql: GATE CSE 2001 | Question: 21-b [top](#)

<https://gateoverflow.in/203574>



✓ There are many ways to write a query, all of which will perform the same task. One way is:

classroom.gateover

```
SELECT regno
FROM examinee
WHERE score > (SELECT AVG(score)
              FROM examinee )
```

Here, the inner query is returning the average of the scores. And outer query selects those *regno* that have a score greater than this average.

11 votes

-- Rishabh Gupta (12.5k points)

3.15.17 Sql: GATE CSE 2001 | Question: 21-c [top](#)

<https://gateoverflow.in/203573>



```
SELECT DISTINCT centr_code
FROM appears
WHERE regno IN (SELECT regno
              FROM examinee
              WHERE score > 80)
```

11 votes

-- Arjun Suresh (332k points)

3.15.18 Sql: GATE CSE 2003 | Question: 86 [top](#)

<https://gateoverflow.in/969>



✓ C. Names of the students who have got an A grade in at least one of the courses taught by Korth.

31 votes

-- Arjun Suresh (332k points)

3.15.19 Sql: GATE CSE 2004 | Question: 53 [top](#)

<https://gateoverflow.in/1049>



✓ D is the answer.

The inner query is over all department and over both male and female employees while the outer query is only for male employees.

28 votes

-- Arjun Suresh (332k points)

3.15.20 Sql: GATE CSE 2005 | Question: 77, ISRO2016-55 [top](#)

<https://gateoverflow.in/1400>



✓ Answer: D

The outer query selects all titles from book table. For every selected book, the subquery returns count of those books which are more expensive than the selected book. The where clause of outer query will be true for 5 most expensive book. For example count(*) will be 0 for the most expensive book and count(*) will be 1 for second most expensive book.

78 votes

-- Rajarshi Sarkar (27.9k points)

3.15.21 Sql: GATE CSE 2006 | Question: 67 [top](#)

<https://gateoverflow.in/1845>



✓ Both Query1 and Query2 are not correct implementations because: Assume that we have a table with n customers having the same balance. In that case Query1 will give rank n to each customer. But according to the question the rank assigned should be 1. And Query2 will return an empty result set (as it will never return rank 1). So statement 4 is correct. For the same reason Query1 is wrong though it is true if we assume the relation set is empty. Statements 2 and 3 are false as 4 is TRUE. Statement 5 is false as a single scan should be faster than a join query. So, the best option should be C, though 1 is not technically correct.

A correct query to achieve the task would be:

```
select A.customer, (
  select 1+count(*)
  from account B
  where A.balance < B.balance
) from account A
```

72 votes

-- Rajarshi Sarkar (27.9k points)

3.15.22 Sql: GATE CSE 2006 | Question: 68 [top](#)

<https://gateoverflow.in/1846>



- ✓ Query1 and Query3 : output will be the same
and Query2 and Query4 : output will be same

I have run these queries on the online compiler, this what i get

```
BEGIN TRANSACTION;
-- /* Create a table called NAMES */
-- CREATE TABLE E(Id integer);
-- CREATE TABLE P(Id integer);
--
-- /* Create few records in this table */
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(1);
-- INSERT INTO E VALUES(3);
-- INSERT INTO E VALUES(3);
--
-- INSERT INTO P VALUES(1);
-- INSERT INTO P VALUES(2);
-- INSERT INTO P VALUES(3);
-- INSERT INTO P VALUES(4);
COMMIT;

/* Display all the records from the table */
-- SELECT * FROM E;
-- select "-----";
-- SELECT * FROM P;
-- select "-----";
select "Query 1:";
select E.id from E
where E.id in (select P.id from P);

select "Query 2:";
select id from P
where id in (select id from E);

select "Query 3:";

select E.id from E e, P p
where e.id = p.id;

select "Query 4:";
select id from P
where exists (select * from E where E.id = P.id);

/* output */
Query 1:
1
1
3
3
Query 2:
1
3
Query 3:
1
1
3
3
Query 4:
1
3
```

So, answer should be B.

40 votes

-- Vikrant Singh (11.2k points)

3.15.23 Sql: GATE CSE 2006 | Question: 69 [top](#)

<https://gateoverflow.in/1847>



Answer should be (C)

In all cases plan 1 is faster than plan 2 cause in plan 1 we are reducing the load by doing select amount $> x$ and then the loop
But, in case of plan 2 its in the nested loop so it need to check every time and will take more time to execute .

27 votes

-- Pranay Datta (7.8k points)



✓ Answer: A

Create a table like this:

```
create table employee(empId int(50), name varchar(50), department int(50), salary int(50));
insert into employee values (1, 'a', 4, 90);
insert into employee values (2, 'b', 5, 30);
insert into employee values (3, 'c', 5, 50);
insert into employee values (4, 'd', 5, 80);
insert into employee values (8, 'f', 7, 10);
```

Q₁ returns 1 for the above table. See here: <http://sqlfiddle.com/#!9/9acce/1>

Q₂ returns empId of those employees who get salary more than the minimum salary offered in department 5. It returns 1, 3, 4 for the above table. See here: <http://sqlfiddle.com/#!9/9acce/2>

According to the question the answer should be 1 for the above table.

PS: The question implies that the required employee must not be from department 5.

References



👍 40 votes

-- Rajarshi Sarkar (27.9k points)



✓

```
SELECT P.pid FROM Parts P WHERE P.color<>'blue'
```

Select all non blue parts

```
SELECT C.sid FROM Catalog C WHERE C.pid NOT IN
```

Selects all suppliers who have supplied a blue part

```
SELECT S.sname
FROM Suppliers S
WHERE S.sid NOT IN
```

Selects suppliers who have not supplied any blue parts.

So, **none** of the options matches.

Option C is wrong as it does not select suppliers who have not supplied any parts which the given query does.

Option A is wrong because it even selects those suppliers who have supplied blue and non-blue parts and also does not include those suppliers who have not supplied any parts.

👍 78 votes

-- Arjun Suresh (332k points)



✓ (C) 1, 3

The inner query gives passenger_id with age above 65 i.e., 1, 2, 3
The outer query chooses the class as AC, which are 1 and 3

👍 32 votes

-- Aravind (2.8k points)



✓ $X = 1, Y = 1$

$X = 2, Y = 2 \times 1 + 1 = 3$

$X = 3, Y = 2 \times 3 + 1 = 7$

$X = 4, Y = 2 \times 7 + 1 = 15$

$X = 5, Y = 2 \times 15 + 1 = 31$

$X = 6, Y = 2 \times 31 + 1 = 63$

$X = 7, Y = 2 \times 63 + 1 = 127$

Correct Answer: A

👍 41 votes

-- Arjun Suresh (332k points)

3.15.28 Sql: GATE CSE 2011 | Question: 46 [top](#)

<https://gateoverflow.in/2148>



✓ The answer is (C).

When we perform the natural join on S and T then result will be like this

Borrower	Bank_Manager	Loan_Amount
Ramesh	Sunderajan	10000.00
Ramesh	Sunderajan	7000.00
Suresh	Ramgopala	5000.00
Mahesh	Sunderajan	10000.00
Mahesh	Sunderajan	7000.00

After that count (*) will count total tuples present in this table so here it is 5.

👍 41 votes

-- neha pawar (3.3k points)

3.15.29 Sql: GATE CSE 2012 | Question: 15 [top](#)

<https://gateoverflow.in/47>



✓ GATE 2012 Answer key is (C) Q and R are true.

But correct answer should be B.

- When group by is not present, having is applied to the whole table

"A grouped table is a set of groups derived during the evaluation of a <group by clause> or a <having clause>. A group is a multiset of rows in which all values of the grouping column or columns are equal if a <group by clause> is specified, or the group is the entire table if no <group by clause> is specified. A grouped table may be considered as a collection of tables. Set functions may operate on the individual tables within the grouped table."

This shows that P is indeed correct.

Also see "having clause section"

<http://www.contrib.andrew.cmu.edu/~shadow/sql/sql1992.txt>

<http://searchsqlserver.techtarget.com/answer/ISO-ANSI-SQL-and-the-GROUP-BY-clause>

The above link says that all columns used in group by must be present in select clause as per SQL-92 standard but later standards doesn't enforce it. I tried this on MySQL and it works. It is allowed in MSSQL also- see below link.

From Microsoft (obviously applicable only to MS-SQL)

<http://msdn.microsoft.com/en-us/library/ms177673.aspx>

! Expressions in the GROUP BY clause can contain columns of the tables, derived tables or views in the FROM clause. The columns are not required to appear in the SELECT clause <select> list. Each table or view column in any nonaggregate expression in the <select> list must be included in the GROUP BY list:

So, as per standard it is not allowed, but in most current DBMS it is allowed. And there is no reason why this shouldn't be allowed. So, ideally 'S' is more correct than 'R' or both are debatable and marks should have been given to all. [classroom.gateoverflow](https://www.classroom.gateoverflow.in)



56 votes

-- Arjun Suresh (332k points)

3.15.30 Sql: GATE CSE 2012 | Question: 51 [top](#)

<https://gateoverflow.in/43313>



✓ <cond> ALL evaluates to TRUE if inner query returns no tuples. So, Number of tuples returned will be number of tuples in $A = 3$.

Reference: <http://dcx.sap.com/1200/en/dbusage/all-test-quantified-subquery.html>

Correct Answer: B

References



48 votes

-- Arjun Suresh (332k points)

3.15.31 Sql: GATE CSE 2014 Set 1 | Question: 22 [top](#)

<https://gateoverflow.in/1789>



✓ (D)Both are false

S1: Foreign key constraint means a lot of constraints it has to be a primary key(which intrun has few constraints)

Alternate reason: Using a check condition we can have the same effect as Foreign key while adding elements to the child table. But when we delete an element from the parent table the referential integrity constraint is no longer valid. So, a check constraint cannot replace a foreign key. So, we cannot replace it with a single check.

S2: if a and b forms a primary key in R, a alone cannot form a foreign key. i.e. $R(a,b,c)$ and $S(a,d,e)$ a of S references to a of R but a of R is not candidate key but a prime attribute since a,b combine a key.

Foreign key definition: it should be a candidate key in some other table(in our case it is only a prime attribute).

92 votes

-- Aravind (2.8k points)

3.15.32 Sql: GATE CSE 2014 Set 1 | Question: 54 [top](#)

<https://gateoverflow.in/1934>



✓

```
SELECT dept-id, MAX(hire-date)
FROM employees JOIN departments USING(dept-id)
WHERE location-id =1700
GROUP BY dept-id
```

This inner query will give the max hire date of each department whose location_id =1700

and outer query will give the last name and hire-date of all those employees who joined on max hire date. answer should come to (B) no errors.

And we can use group by and where together, who said we can not :(

Example: create table departments(dept_id number, dept_name varchar2(25), location_id number);
Query: select d1.dept_name,max(d1.location_id)

from departments d1, departments d2
 where d1.dept_name = d2.dept_name
 and d1.dept_name='AA'
 group by d1.dept_name;
 will give output.

40 votes

-- Manu Thakur (34k points)

3.15.33 Sql: GATE CSE 2014 Set 2 | Question: 54 top

https://gateoverflow.in/2021



✓ C)

Consider the following instances of R and S

R		
A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

S		
A	X	Z
1	2	3
3	5	7
7	6	5
7	6	5

Now output of given query

```
select * from R where a in (select S.a from S)
```

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

For Option,

A) since multiplicity of tuples is disturbed

```
select R.* from R, S where R.a=S.a
```

∴ Output will be

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9
7	8	9
7	8	9

B)

```
select distinct R.* from R,S where R.a=S.a
```

∴ only Distinct R will be chosen in the end so, output will be

A	B	C
1	2	3
7	8	9

C) ANSWER

```
select R.* from R, (select distinct a from S) as S1 where R.a=S1.a
```

Multiplicity of tuples is maintained. ∴ Multiplicity of duplicate tuples will be distributed when there is a match between R.a and S.a and for that match S.a's value is repeated.

So, Output will be

A	B	C
1	2	3
1	2	3
7	8	9
7	8	9

👍 76 votes

-- Kalpish Singhal (1.6k points)

3.15.34 Sql: GATE CSE 2014 Set 3 | Question: 54 top

<https://gateoverflow.in/2089>



✓

```
SELECT empNAME
FROM employee (E)
WHERE NOT EXISTS
```

if any customer is there
who gave bad rating then
do not choose this EMPLOYEE

if something exist in this then

For an employee

```
( SELECT custId
FROM CUSTOMER C
WHERE C.saleRepId = E.empId
AND C.rating <> 'GOOD' )
```

all customer who did not give good rating

So, an employee whose *ALL* customers gives him GOOD rating is chosen;

All such employees are chosen.

Answer = option D

👍 50 votes

-- Amar Vashishth (25.2k points)

3.15.35 Sql: GATE CSE 2015 Set 1 | Question: 27 top

<https://gateoverflow.in/8225>



✓

For answering there is no need to execute the query, we can directly answer this as 2

How?

! Group by Student_Names

It means all name that are same should be kept in one row.

There are 3 names. But in that there is a duplicate with Raj being repeated \implies Raj produces one row and Rohit produces one row \implies Total 2 rows.

For better understanding, I'll just analyze the whole query

1st statement which is executed from the query is From Clause : **From Student S, Performance P**

\implies cross product of those two tables will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
1	Raj	1	Maths	80
1	Raj	1	English	70
1	Raj	2	Maths	75
1	Raj	3	English	80
1	Raj	2	Physics	65
1	Raj	3	Maths	80
2	Rohit	1	Maths	80
2	Rohit	1	English	70
2	Rohit	2	Maths	75
2	Rohit	3	English	80
2	Rohit	2	Physics	65
2	Rohit	3	Maths	80
3	Raj	1	Maths	80
3	Raj	1	English	70
3	Raj	2	Maths	75
3	Raj	1	English	80
3	Raj	2	Physics	65
3	Raj	3	Maths	80

2nd statement which is executed from the query is Where Clause : **Where S.Roll_no = P.Roll_no**

⇒ delete those rows which does not satisfy the WHERE condition. Then the result will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
1	Raj	1	Maths	80
1	Raj	1	English	70
2	Rohit	2	Maths	75
2	Rohit	2	Physics	65
3	Raj	3	English	80
1	Raj	3	Maths	80

3rd statement which is executed from the query is Group by Clause : **Group by S.Student_Name**

⇒ Merge those rows which are having same name, then result will be

S.RollNo	S.Student_name	P.Roll_no	P.Course	P.marks
{1, 1, 3, 3}	Raj	{1, 1, 3, 3}	{Maths, English}	{80, 70, 80, 80}
2	Rohit	2	{Maths, Physics}	{75, 65}

Note that, this can't be used as final result as it violates 1NF (multiple values in each tuple for S.Roll_no, P.Roll_no, P.Course and P.marks)

4th statement which is executed from the query is Select Clause : **Select S.Student_Name, SUM(P.marks)**

⇒ Delete un-necessary columns and calculate the aggregate functions, then result will be

S.Student_name	P.marks
Raj	310
Rohit	140

👍 70 votes

-- naresh1845 (1.1k points)



✓ A is the answer

- B - Returns the addresses of all theaters.
- C - Returns null set. max() returns a single value and there won't be any value > max.
- D - Returns null set. Same reason as C. All and ANY works the same here as max returns a single value.

63 votes

-- Arjun Suresh (332k points)

3.15.37 Sql: GATE CSE 2016 Set 2 | Question: 52 top

<https://gateoverflow.in/39604>



- ✓ 1st query will return the following:

Table Name : Total (**name, capacity**)

name	capacity
Ajmer	20
Bikaner	40
Churu	30
Dungargarh	10

2nd Query will return, **Total_avg (capacity)** 25

Since $\text{sum of capacity} = 100/4 = 25$

3rd query will be final and it's tuples will be considered as output, where name of district and its total capacity should be more than or equal to 25

name
Bikaner
Churu

Hence, **2 tuples** returned.

75 votes

-- Shashank Chavan (2.4k points)

3.15.38 Sql: GATE CSE 2017 Set 1 | Question: 23 top

<https://gateoverflow.in/118303>



- ✓ The inner query will return

DeptName	Num
AA	4
AB	3
AC	3
AD	2
AE	1

Now $\text{AVG}(\text{EC.Num})$ will find the average of Num values in the above-returned query, which is $(4 + 3 + 3 + 2 + 1) \div 5 = 2.6$

So according to me, the answer should be 2.6.

43 votes

-- sriv_shubham (2.8k points)

3.15.39 Sql: GATE CSE 2017 Set 2 | Question: 46 top

<https://gateoverflow.in/118391>



- ✓ ALL (EMPTY SET) always returns TRUE. So first where condition is always satisfied.

Second where condition will return all those rows who have more goals than ANY German player. Since, minimum goals by a German is 10, all the rows which are greater than 10 Goals will be returned.

I.e. first 7 rows in the table.

Hence, answer: **7**.

48 votes

-- tvkkk (1.1k points)

3.15.40 Sql: GATE CSE 2018 | Question: 12

https://gateoverflow.in/204086



Answer is D.

Since the full-outer join is nothing but a combination of inner-join and the remaining tuples of both the tables that couldn't satisfy the common attributes' equality condition, and merging them with "null" values.

20 votes

-- Baljit kaur (1k points)

3.15.41 Sql: GATE CSE 2019 | Question: 51

https://gateoverflow.in/302797



Group by Student_name \implies number of distinct values of Student_name

in the instance of the relation all rows have distinct name then it should results 5 tuples !

27 votes

-- Shaik Masthan (50.4k points)

3.15.42 Sql: GATE CSE 2020 | Question: 13

https://gateoverflow.in/333218



The given query is a nested subquery but not co-related subquery (inner query is independent of the outer and so can be executed independently)

```
SELECT AVG (cost) FROM Catalogue WHERE pno= 'P4' GROUP BY pno
```

sno	pno	cost
S1	P1	150
S1	P2	50
S1	P3	100
S2	P4	200
S2	P5	250
S3	P1	250
S3	P2	150
S3	P5	300
S3	P4	250

First, we will select the tuples with pno = 'P4' and then group by pno (so just one group) and then find the average cost.

sno	pno	cost
S2	P4	200
S3	P4	250

So average cost = $\frac{200+250}{2} = 225$

\therefore the inner query will return 225

Now the given SQL query would become

```
SELECT s.sno,s.sname FROM Supplier s , Catalogue c WHERE s.sno=c.sno AND cost > 225
```

So here we need to do cross product of supplier table s and Catalogue table c and from the cross product we will select those rows where s.sno = c.sno AND cost > 225

Since it is given that cost > 225 so we do not need to consider rows from the Catalogue table having cost \leq 225 while doing cross product. Hence from the Catalogue table only the row numbers 5, 6, 8, 9 need to be taken while doing the cross product.

After doing cross product we'll get,

s.sno	s.name	s.location	c.sno	c.pno	c.cost
S1	M/s Royal furniture	Delhi	S2	P5	250
S1	M/s Royal furniture	Delhi	S3	P1	250
S1	M/s Royal furniture	Delhi	S3	P5	300
S1	M/s Royal furniture	Delhi	S3	P4	250
S2	M/s Balaji furniture	Bangalore	S2	P5	250
S2	M/s Balaji furniture	Bangalore	S3	P1	250
S2	M/s Balaji furniture	Bangalore	S3	P5	300
S2	M/s Balaji furniture	Bangalore	S3	P4	250
S3	M/s Premium furniture	Chennai	S2	P5	250
S3	M/s Premium furniture	Chennai	S3	P1	250
S3	M/s Premium furniture	Chennai	S3	P5	300
S3	M/s Premium furniture	Chennai	S3	P4	250

Now after doing cross product only 4 tuples will be selected from the table due to the condition $s.sno = c.sno$

s.sno	s.name	s.location	c.sno	c.pno	c.cost
S2	M/s Balaji furniture	Bangalore	S2	P5	250
S3	M/s Premium furniture	Chennai	S3	P1	250
S3	M/s Premium furniture	Chennai	S3	P5	300
S3	M/s Premium furniture	Chennai	S3	P4	250

∴ Option A. 4 is the correct answer

👍 17 votes

-- Satbir Singh (21k points)

3.15.43 Sql: GATE CSE 2021 Set 1 | Question: 23 top

<https://gateoverflow.in/357428>



✓

- $P(A > 10) = \frac{10}{15} = \frac{2}{3}$
- $P(B = 18) = \frac{1}{20}$
- $P(A > 10 \wedge B = 18) = \frac{2}{3} \times \frac{1}{20} = \frac{1}{30}$

$$P(A > 10 \vee B = 18) = P(A > 10) + P(B = 18) - P(A > 10 \wedge B = 18)$$

$$= \frac{2}{3} + \frac{1}{20} - \frac{1}{30} = \frac{40+3-2}{60} = \frac{41}{60}$$

$$\text{Estimated number of tuples} = \frac{41}{60} \times 1200 = 820$$

The above answer is TRUE for SQL SELECT but not for Relational Algebra as by theory relational algebra operates on a set which means all the elements must be distinct. Since we have 15 distinct possible values for A and 20 distinct possible values for B , in strict relational algebra we'll get

$$\text{Estimated number of tuples} = \frac{41}{60} \times (15 \times 20) = 205.$$

Official Answer: 205 OR 820.

👍 9 votes

-- zxy123 (2.8k points)

3.15.44 Sql: GATE CSE 2021 Set 2 | Question: 31 top

<https://gateoverflow.in/357509>



✓

It's a nested query but not Co-related query.

Evaluate the innermost query first.

```
select avg(salary)
from emp
```

It is given that emp represent employees of a company.

So, Option B is the correct answer.

👍 2 votes

-- Shaik Masthan (50.4k points)



- ✓ Since, there is no specific joining condition specified, it will retrieve Cartesian product of the table

Number of rows = product of number of rows in each relation = $3 \times 2 = 6$

Number of columns = sum of number of columns = $3 + 2 = 5$

Answer: D.

👍 52 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ Update on null gives null. Now, avg function ignores null values. So, here avg will be $(15 + 25 + 35)/3 = 25$.

<http://msdn.microsoft.com/en-us/library/ms177677.aspx>

Correct Answer: C

References



👍 44 votes

-- Arjun Suresh (332k points)



- ✓ Answer is C

Here in (i) when we update in STUDENT table Dept_id = NULL it is fine as a foreign key can be NULL.

But in (ii) if we set in DEPARTMENT table dept id = NULL it is not possible as PRIMARY KEY cannot be NULL.

Instead of update to NULL, if we try DELETE, then also it is not allowed as we have foreign key reference to it from STUDENT table with Dept_id = 1. DELETE ON CASCADE clause is a way to avoid this issue which will delete all referenced entries from the child table too but unless told we cannot assume this as this cause is not universally applicable.

👍 40 votes

-- neha pawar (3.3k points)



- ✓ Answer is D) supply two or more items
The whole query returns the distinct list of suppliers who supply two or more items.

👍 32 votes

-- Bran Stark (339 points)



- ✓ For color = "Red", did = {22, 22, 31, 31, 64}

For color = "Green", did = {22, 31, 74}

Intersection of Red and Green will give did = {22, 31} which is Karthikeyan and Boris

Answer: A

👍 34 votes

-- Vikrant Singh (11.2k points)



```

select D.dname
from Drivers D
where D.did in (
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'red'
    intersect
    select R.did
    from Cars C, Reserves R
    where R.cid = C.cid and C.colour = 'green'
)

```

```

select R.did from Cars C, Reserves R where R.cid = C.cid and C.colour = 'red'

```

So, first, get 2 red cars by scanning 4 tuples of the cars relation. Now, for each of the two 'red' cars, we scan all the 10 tuples of the 'Reserves' relation and thus we get $2 \times 10 + 4 = 24$ comparisons. But this is not optimal. We can check in the reverse order for each tuple of the 'Reserves' relation because 'cid' is a primary key (hence unique) of 'Cars' relation.

Supposing our earlier selection is $\langle 102, 104 \rangle$ then this requires $3 + 7 \times 2 = 17$ comparisons. due to if $(R.cid == 102 || R.cid == 104)$

If the order was $\langle 104, 102 \rangle$, then $2 + 8 \times 2 = 18$ comparisons. due to if $(R.cid == 104 || R.cid == 102)$

Thus, totally 21 to 22 comparisons and gives $\langle 22, 31, 64 \rangle$ as did.

Similarly for the 'green' car we get $4 + 10 = 14$ comparisons. due to if $(R.cid == 103)$ and gives $\langle 22, 31, 74 \rangle$ as did.

Intersect requires $1 + 2 + 3 = 6$ comparisons in the best case and $3 + 2 + 3 = 8$ in the worst case and this gives $\langle 22, 31 \rangle$.

Finally, we have to locate the did 22 and did 31 from the driver table and did is the primary key. As told in the question, we use linear search and for 22, we hit on the first try, and for 31 we hit on the third try. So, $1 + 3 = 4$ comparisons.

Thus total no. of comparisons = $(21 \text{ to } 22) + 14 + (6 \text{ to } 8) + 4 = 45 \text{ to } 48$.

Correct Answer: B.

63 votes

-- Arjun Suresh (332k points)



D:

If Select clause consist aggregate and non - aggregate columns. All non aggregate columns in the Select clause must appear in Group By clause. But in this query Group by clause consists school-id instead of school-name

<http://weblogs.sqlteam.com/jeffs/archive/2007/07/20/but-why-must-that-column-be-contained-in-an-aggregate.aspx>

References



63 votes

-- erravi90 (131 points)



In a database system, unique timestamps are assigned to each transaction using Lamport's logical clock. Let $TS(T_1)$ and $TS(T_2)$ be the timestamps of transactions T_1 and T_2 respectively. Besides, T_1 holds a lock on the resource R, and T_2 has requested a conflicting lock on the same resource R. The following algorithm is used to prevent deadlocks in the database system assuming that a killed transaction is restarted with the same timestamp.

if $TS(T_2) < TS(T_1)$ then

T_1 is killed

else T_2 waits.

Assume any transaction that is not killed terminates eventually. Which of the following is TRUE about the database system that uses the above algorithm to prevent deadlocks?

- A. The database system is both deadlock-free and starvation-free.
- B. The database system is deadlock-free, but not starvation-free.
- C. The database system is starvation-free, but not deadlock-free.
- D. The database system is neither deadlock-free nor starvation-free.

gate2017-cse-set1 databases timestamp-ordering deadlock normal

Answer

Answers: Timestamp Ordering

3.16.1 Timestamp Ordering: GATE CSE 2017 Set 1 | Question: 42 top

<https://gateoverflow.in/118325>



In a database system, **unique** timestamps are assigned to each transaction using Lamport's logical clock

Since Unique Timestamps are assigned, so there is no question of two transaction having same timestamp.

Moreover, there is nothing mentioned about the size of the counter by which it can be determined that whether there will be case of timestamp wrap around or not.

So, there will be no timestamp wrap around.

In Lamport's logical clock Timestamps are assigned in increasing order of enumeration.

So, $T_i < T_j$ if Transaction T_i came into system before T_j .

The above scheme given is nothing but " **Wound-Wait** " Scheme in which younger transaction is killed by older transaction that came into system before this younger transaction came.[1][2]

So, this is a part of Basic Time-Stamp Ordering in Concurrency Control.

And Basic Time Stamp ordering protocol is deadlock free and **not starvation free, in general.**

Here in this question according to given condition, the database system is both deadlock free and starvation free as well , as it is Wound wait scheme and in case of wound wait it **avoid starvation**, because in Wound Wait scheme **we restart a transaction that has been aborted, with it's same original Timestamp** . If it restart with a new Timestamp then there is a possibility of Starvation (as larger TimeStamp transaction is aborted here and new Transaction which is coming next have always greater TimeStamp than previous one). But that is Not the case here.

Reference:

[1] <http://www.cs.colostate.edu/~cs551/CourseNotes/Deadlock/WaitWoundDie.html>

[2] <http://stackoverflow.com/questions/32794142/what-is-the-difference-between-wait-die-and-wound-wait>

Hence, answer is (A).

PS: The **Wound-wait scheme means** :

- The **newer transactions** are **killed** when an **older transaction** make a **request** for a **lock** being **held** by the **newer transactions** .
- Here the algorithm says $TS(T_2) < TS(T_1)$ means T_2 is **older** transaction (as TS of T_2 is less than TS of T_1 ..means **T_2 come first then T_1 come and TS is assign in increasing order**), so **newer one is T_1** and also question says **T_1 holds a lock on the resource R , and T_2 has requested a conflicting lock on the same resource R .**
- So T_1 is killed as per Wound-wait scheme .

Reference :

<http://www.mathcs.emory.edu/~cheung/Courses/554/Syllabus/8-recv+serial/deadlock-compare.html>

timestamps are assigned to each transaction using Lamport's logical clock.

This line means timestamps are assigns in increasing order .

We can divide the answer into 3 parts:

Part 1: Is it Wound wait scheme?

Yes, given algorithm:

If $TS(T_2) < TS(T_1)$, then

T_1 is killed

else, T_2 waits.

comes under wound wait scheme..as here old transaction is always survive and older transaction wounds newer transaction when both want to apply lock on same resource ..

Part 2 : Wound Wait avoid Starvation

Yes, How?

as newer one is die and restart with same timestamp and older one is survive always so after execute older transaction that newer one can definitely execute and new transactions which are coming can die and restart again (previous newer became older that time).

Part 3 : Does Starvation freedom implies Deadlock freedom?

Yes, here no starvation means also No deadlock possibility.

In one line - wound wait -> no starvation -> no deadlock -> option A.

EDIT

Another way to think about Deadlock and starvation

Deadlock is prevented because we are **violating NO-Preemption** Condition for the deadlock to happen.

How starvation free? Here Bounded waiting for transactions is ensured.HOW?

Consider "n" transactions T_1, T_2, \dots, T_n having their timestamps order as $TS(T_1) < TS(T_2) < \dots < TS(T_n)$ (Timestamps are unique)

Consider for $k, 1 < k \leq n$ a transaction T_k , this transaction T_k can be atmost preempted by Transaction sets T_1, T_2, \dots, T_{k-1} and it is also given "**Any transaction that is not killed eventually terminates**". Means Eventually a time would come when, all transactions T_j having $TS(T_j) < TS(T_k)$ will terminate and T_k would get chance without preemption. And this J would lie in range $1 \leq j \leq k - 1$. **Bounded waiting ensured.**

References



👍 111 votes

-- Ayush Upadhyaya (28.4k points)

3.17

Transaction And Concurrency (28) top ⚡

3.17.1 Transaction And Concurrency: GATE CSE 1999 | Question: 2.6 top ⚡

https://gateoverflow.in/1484



For the schedule given below, which of the following is correct:

- 1 Read A
- 2 Read B
- 3 Write A
- 4 Read A
- 5 Write A
- 6 Write B
- 7 Read B
- 8 Write B

- A. This schedule is serializable and can occur in a scheme using 2PL protocol
- B. This schedule is serializable but cannot occur in a scheme using 2PL protocol
- C. This schedule is not serializable but can occur in a scheme using 2PL protocol
- D. This schedule is not serializable and cannot occur in a scheme using 2PL protocol

gate1999 databases transaction-and-concurrency normal

Answer

3.17.2 Transaction And Concurrency: GATE CSE 2003 | Question: 29, ISRO2009-73 [top](#)

<https://gateoverflow.in/919>



Which of the following scenarios may lead to an irrecoverable error in a database system?

- A. A transaction writes a data item after it is read by an uncommitted transaction
- B. A transaction reads a data item after it is read by an uncommitted transaction
- C. A transaction reads a data item after it is written by a committed transaction
- D. A transaction reads a data item after it is written by an uncommitted transaction

gate2003-cse databases transaction-and-concurrency easy isro2009

Answer

3.17.3 Transaction And Concurrency: GATE CSE 2003 | Question: 87 [top](#)

<https://gateoverflow.in/970>



Consider three data items D_1 , D_2 , and D_3 , and the following execution schedule of transactions T_1 , T_2 , and T_3 . In the diagram, $R(D)$ and $W(D)$ denote the actions reading and writing the data item D respectively.

T1	T2	T3
	R(D3); R(D2); W(D2);	
R(D1); W(D1);		R(D2); R(D3);
		W(D2); W(D3);
R(D2); W(D2);	R(D1);	
	W(D1);	

Which of the following statements is correct?

- A. The schedule is serializable as $T_2; T_3; T_1$
 B. The schedule is serializable as $T_2; T_1; T_3$
 C. The schedule is serializable as $T_3; T_2; T_1$
 D. The schedule is not serializable

gate2003-cse databases transaction-and-concurrency normal

Answer

3.17.4 Transaction And Concurrency: GATE CSE 2006 | Question: 20, ISRO2015-17 [top](#)

<https://gateoverflow.in/981>



Consider the following log sequence of two transactions on a bank account, with initial balance 12000, that transfer 2000 to a mortgage payment and then apply a 5% interest.

1. T1 start
2. T1 B old = 12000 new = 10000
3. T1 M old = 0 new = 2000
4. T1 commit
5. T2 start
6. T2 B old = 10000 new = 10500
7. T2 commit

Suppose the database system crashes just before log record 7 is written. When the system is restarted, which one statement is true of the recovery procedure?

- A. We must redo log record 6 to set B to 10500
 B. We must undo log record 6 to set B to 10000 and then redo log records 2 and 3
 C. We need not redo log records 2 and 3 because transaction T1 has committed
 D. We can apply redo and undo operations in arbitrary order because they are idempotent

gate2006-cse databases transaction-and-concurrency normal isro2015

Answer

3.17.5 Transaction And Concurrency: GATE CSE 2007 | Question: 64 [top](#)

<https://gateoverflow.in/1262>



Consider the following schedules involving two transactions. Which one of the following statements is **TRUE**?

- $S_1 : r_1(X); r_1(Y); r_2(X); r_2(Y); w_2(Y); w_1(X)$
- $S_2 : r_1(X); r_2(X); r_2(Y); w_2(Y); r_1(Y); w_1(X)$

- A. Both S_1 and S_2 are conflict serializable.
 B. S_1 is conflict serializable and S_2 is not conflict serializable.
 C. S_1 is not conflict serializable and S_2 is conflict serializable.
 D. Both S_1 and S_2 are not conflict serializable.

gate2007-cse databases transaction-and-concurrency normal

Answer

3.17.6 Transaction And Concurrency: GATE CSE 2009 | Question: 43 [top](#)

<https://gateoverflow.in/1329>



Consider two transactions T_1 and T_2 , and four schedules S_1, S_2, S_3, S_4 , of T_1 and T_2 as given below:

$T_1 : R_1[x]W_1[x]W_1[y]$

$T_2 : R_2[x]R_2[y]W_2[y]$

$S_1 : R_1[x]R_2[x]R_2[y]W_1[x]W_1[y]W_2[y]$

$S_2 : R_1[x]R_2[x]R_2[y]W_1[x]W_2[y]W_1[y]$

$S_3 : R_1[x]W_1[x]R_2[x]W_1[y]R_2[y]W_2[y]$

$S_4 : R_2[x]R_2[y]R_1[x]W_1[x]W_1[y]W_2[y]$

Which of the above schedules are conflict-serializable?

- A. S_1 and S_2
- B. S_2 and S_3
- C. S_3 only
- D. S_4 only

gate2009-cse databases transaction-and-concurrency normal

Answer

3.17.7 Transaction And Concurrency: GATE CSE 2010 | Question: 20

<https://gateoverflow.in/2196>



Which of the following concurrency control protocols ensure both conflict serializability and freedom from deadlock?

- I. 2-phase locking
 - II. Time-stamp ordering
- A. I only
 - B. II only
 - C. Both I and II
 - D. Neither I nor II

gate2010-cse databases transaction-and-concurrency normal

Answer

3.17.8 Transaction And Concurrency: GATE CSE 2010 | Question: 42

<https://gateoverflow.in/2343>



Consider the following schedule for transactions T_1 , T_2 and T_3 :

T1	T2	T3
Read(X)		
	Read(Y)	
		Read(Y)
	Write(Y)	
Write(X)		
		Write(X)
	Read(X)	
	Write(X)	

Which one of the schedules below is the correct serialization of the above?

- A. $T_1 \rightarrow T_3 \rightarrow T_2$
- B. $T_2 \rightarrow T_1 \rightarrow T_3$
- C. $T_2 \rightarrow T_3 \rightarrow T_1$
- D. $T_3 \rightarrow T_1 \rightarrow T_2$

gate2010-cse databases transaction-and-concurrency normal

Answer

3.17.9 Transaction And Concurrency: GATE CSE 2012 | Question: 27

<https://gateoverflow.in/1612>



Consider the following transactions with data items P and Q initialized to zero:

T_1	read (P); read (Q); if P = 0 then Q := Q + 1; write (Q)
T_2	read (Q); read (P); if Q = 0 then P := P + 1; write (P)

Any non-serial interleaving of **T1** and **T2** for concurrent execution leads to

- A. a serializable schedule
- B. a schedule that is not conflict serializable
- C. a conflict serializable schedule
- D. a schedule for which a precedence graph cannot be drawn

gate2012-cse databases transaction-and-concurrency normal

Answer

3.17.10 Transaction And Concurrency: GATE CSE 2014 Set 1 | Question: 29

<https://gateoverflow.in/1796>



Consider the following four schedules due to three transactions (indicated by the subscript) using *read* and *write* on a data item x , denoted by $r(x)$ and $w(x)$ respectively. Which one of them is conflict serializable?

- A. $r_1(x); r_2(x); w_1(x); r_3(x); w_2(x);$
- B. $r_2(x); r_1(x); w_2(x); r_3(x); w_1(x);$
- C. $r_3(x); r_2(x); r_1(x); w_2(x); w_1(x);$
- D. $r_2(x); w_2(x); r_3(x); r_1(x); w_1(x);$

gate2014-cse-set1 databases transaction-and-concurrency normal

Answer

3.17.11 Transaction And Concurrency: GATE CSE 2014 Set 2 | Question: 29

<https://gateoverflow.in/1988>



Consider the following schedule **S** of transactions T_1, T_2, T_3, T_4 :

T1	T2	T3	T4
	Reads(X)		
		Writes(X)	
		Commit	
Writes(X)			
Commit			
	Writes(Y)		
	Reads(Z)		
	Commit		
			Reads(X)
			Reads(Y)
			Commit

Which one of the following statements is CORRECT?

- A. S is conflict-serializable but not recoverable
- B. S is not conflict-serializable but is recoverable
- C. S is both conflict-serializable and recoverable
- D. S is neither conflict-serializable nor is it recoverable

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Answer

3.17.12 Transaction And Concurrency: GATE CSE 2014 Set 3 | Question: 29 [top](#)

<https://gateoverflow.in/2063>



Consider the transactions $T1$, $T2$, and $T3$ and the schedules $S1$ and $S2$ given below.

- $T1 : r1(X); r1(Z); w1(X); w1(Z)$
- $T2 : r2(Y); r2(Z); w2(Z)$
- $T3 : r3(Y); r3(X); w3(Y)$
- $S1 : r1(X); r3(Y); r3(X); r2(Y); r2(Z); w3(Y); w2(Z); r1(Z); w1(X); w1(Z)$
- $S2 : r1(X); r3(Y); r2(Y); r3(X); r1(Z); r2(Z); w3(Y); w1(X); w2(Z); w1(Z)$

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Which one of the following statements about the schedules is TRUE?

- A. Only $S1$ is conflict-serializable.
- B. Only $S2$ is conflict-serializable.
- C. Both $S1$ and $S2$ are conflict-serializable.
- D. Neither $S1$ nor $S2$ is conflict-serializable.

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Answer

3.17.13 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 1 [top](#)

<https://gateoverflow.in/8047>



Consider the following transaction involving two bank accounts x and y .

```
read(x); x:=x-50; write(x); read(y); y:=y+50; write(y)
```

The constraint that the sum of the accounts x and y should remain constant is that of

- A. Atomicity
- B. Consistency
- C. Isolation
- D. Durability

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Answer

3.17.14 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 46 [top](#)

<https://gateoverflow.in/8246>



Consider a simple checkpointing protocol and the following set of operations in the log.

(start, T4); (write, T4, y, 2, 3); (start, T1); (commit, T4); (write, T1, z, 5, 7);

(checkpoint);

(start, T2); (write, T2, x, 1, 9); (commit, T2); (start, T3); (write, T3, z, 7, 2);

If a crash happens now and the system tries to recover using both undo and redo operations, what are the contents of the undo list and the redo list?

- A. Undo: T3, T1; Redo: T2
- B. Undo: T3, T1; Redo: T2, T4
- C. Undo: none; Redo: T2, T4, T3, T1
- D. Undo: T3, T1, T4; Redo: T2

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Answer

3.17.15 Transaction And Concurrency: GATE CSE 2015 Set 3 | Question: 29

<https://gateoverflow.in/8482>



Consider the partial Schedule S involving two transactions $T1$ and $T2$. Only the *read* and the *write* operations have been shown. The *read* operation on data item P is denoted by $read(P)$ and *write* operation on data item P is denoted by $write(P)$.

Time Instance	Transaction ID	
	T1	T2
1	read(A)	
2	write(A)	
3		read(C)
4		write(C)
5		read(B)
6		write(B)
7		read(A)
8		commit
9	read(B)	

Suppose that the transaction $T1$ fails immediately after time instance 9. Which of the following statements is correct?

- A. $T2$ must be aborted and then both $T1$ and $T2$ must be re-started to ensure transaction atomicity
- B. Schedule S is non-recoverable and cannot ensure transaction atomicity
- C. Only $T2$ must be aborted and then re-started to ensure transaction atomicity
- D. Schedule S is recoverable and can ensure transaction atomicity and nothing else needs to be done

gate2015-cse-set3

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normal

Answer

3.17.16 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 22

<https://gateoverflow.in/39644>



Which one of the following is NOT a part of the ACID properties of database transactions?

- A. Atomicity
- B. Consistency
- C. Isolation
- D. Deadlock-freedom

gate2016-cse-set1

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easy

Answer

3.17.17 Transaction And Concurrency: GATE CSE 2016 Set 1 | Question: 51

<https://gateoverflow.in/39703>



Consider the following two phase locking protocol. Suppose a transaction T accesses (for read or write operations), a certain set of objects $\{O_1, \dots, O_k\}$. This is done in the following manner:

- Step 1. T acquires exclusive locks to O_1, \dots, O_k in increasing order of their addresses.
- Step 2. The required operations are performed.
- Step 3. All locks are released

This protocol will

- A. guarantee serializability and deadlock-freedom
- B. guarantee neither serializability nor deadlock-freedom
- C. guarantee serializability but not deadlock-freedom
- D. guarantee deadlock-freedom but not serializability.

gate2016-cse-set1

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normal

Answer



Suppose a database schedule S involves transactions T_1, \dots, T_n . Construct the precedence graph of S with vertices representing the transactions and edges representing the conflicts. If S is serializable, which one of the following orderings of the vertices of the precedence graph is guaranteed to yield a serial schedule?

- A. Topological order
- B. Depth-first order
- C. Breadth-first order
- D. Ascending order of the transaction indices

gate2016-cse-set2

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transaction-and-concurrency

normal

Answer



Consider the following database schedule with two transactions T_1 and T_2 .

$$S = r_2(X); r_1(X); r_2(Y); w_1(X); r_1(Y); w_2(X); a_1; a_2$$

Where $r_i(Z)$ denotes a read operation by transaction T_i on a variable Z , $w_i(Z)$ denotes a write operation by T_i on a variable Z and a_i denotes an abort by transaction T_i .

Which one of the following statements about the above schedule is **TRUE**?

- A. S is non-recoverable.
- B. S is recoverable, but has a cascading abort.
- C. S does not have a cascading abort.
- D. S is strict.

gate2016-cse-set2

databases

transaction-and-concurrency

normal

Answer



Consider the following two statements about database transaction schedules:

- I. Strict two-phase locking protocol generates conflict serializable schedules that are also recoverable.
- II. Timestamp-ordering concurrency control protocol with Thomas' Write Rule can generate view serializable schedules that are not conflict serializable

Which of the above statements is/are TRUE?

- A. I only
- B. II only
- C. Both I and II
- D. Neither I nor II

gate2019-cse

databases

transaction-and-concurrency

Answer



Consider a schedule of transactions T_1 and T_2 :

T_1	RA			RC		WD		WB	Commit	
T_2		RB	WB		RD		WC			Commit

Here, RX stands for "Read(X)" and WX stands for "Write(X)". Which one of the following schedules is conflict equivalent to the above schedule?

- A.

T_1				RA	RC	WD	WB		Commit	
T_2	RB	WB	RD					WC		Commit
- B.

T_1	RA	RC	WD	WB					Commit	
T_2					RB	WB	RD	WC		Commit

C.	T_1	RA	RC	WD				WB	Commit	
	T_2				RB	WB	RD		WC	Commit
D.	T_1					RA	RC	WD	WB	Commit
	T_2	RB	WB	RD	WC					Commit

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gate2020-cse databases transaction-and-concurrency

Answer

3.17.22 Transaction And Concurrency: GATE CSE 2021 Set 1 | Question: 13 top

https://gateoverflow.in/357439



Suppose a database system crashes again while recovering from a previous crash. Assume checkpointing is not done by the database either during the transactions or during recovery.

Which of the following statements is/are correct?

- A. The same undo and redo list will be used while recovering again
- B. The system cannot recover any further
- C. All the transactions that are already undone and redone will not be recovered again
- D. The database will become inconsistent

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gate2021-cse-set1 multiple-selects databases transaction-and-concurrency

Answer

3.17.23 Transaction And Concurrency: GATE IT 2004 | Question: 21 top

https://gateoverflow.in/3662



Which level of locking provides the highest degree of concurrency in a relational database ?

- A. Page
- B. Table
- C. Row
- D. Page, table and row level locking allow the same degree of concurrency

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gate2004-it databases normal transaction-and-concurrency

Answer

3.17.24 Transaction And Concurrency: GATE IT 2004 | Question: 77 top

https://gateoverflow.in/3721



Consider the following schedule S of transactions T_1 and T_2 :

T1	T2
Read(A)	
$A = A - 10$	
	Read(A)
	$Temp = 0.2 * A$
	Write(A)
	Read(B)
Write(A)	
Read(B)	
$B = B + 10$	
Write(B)	
	$B = B + Temp$
	Write(B)

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Which of the following is TRUE about the schedule S ?

- A. S is serializable only as T_1, T_2
- B. S is serializable only as T_2, T_1
- C. S is serializable both as T_1, T_2 and T_2, T_1

D. S is not serializable either as $T1, T2$ or as $T2, T1$

gate2004-it databases transaction-and-concurrency normal

Answer

3.17.25 Transaction And Concurrency: GATE IT 2005 | Question: 24 top

https://gateoverflow.in/3769



Amongst the ACID properties of a transaction, the 'Durability' property requires that the changes made to the database by a successful transaction persist

- A. Except in case of an Operating System crash
- B. Except in case of a Disk crash
- C. Except in case of a power failure
- D. Always, even if there is a failure of any kind

gate2005-it databases transaction-and-concurrency easy

Answer

3.17.26 Transaction And Concurrency: GATE IT 2005 | Question: 67 top

https://gateoverflow.in/3830



A company maintains records of sales made by its salespersons and pays them commission based on each individual's total sales made in a year. This data is maintained in a table with following schema:

salesinfo = (salespersonid, totalsales, commission)

In a certain year, due to better business results, the company decides to further reward its salespersons by enhancing the commission paid to them as per the following formula:

- If $\text{commission} \leq 50000$, enhance it by 2%
- If $50000 < \text{commission} \leq 100000$, enhance it by 4%
- If $\text{commission} > 100000$, enhance it by 6%

The IT staff has written three different SQL scripts to calculate enhancement for each slab, each of these scripts is to run as a separate transaction as follows:

```
T1
Update salesinfo
Set commission = commission * 1.02
Where commission <= 50000;

T2
Update salesinfo
Set commission = commission * 1.04
Where commission > 50000 and commission is <= 100000;

T3
Update salesinfo
Set commission = commission * 1.06
Where commission > 100000;
```

Which of the following options of running these transactions will update the commission of all salespersons correctly

- A. Execute T1 followed by T2 followed by T3
- B. Execute T2, followed by T3; T1 running concurrently throughout
- C. Execute T3 followed by T2; T1 running concurrently throughout
- D. Execute T3 followed by T2 followed by T1

gate2005-it databases transaction-and-concurrency normal

Answer

3.17.27 Transaction And Concurrency: GATE IT 2007 | Question: 66 top

https://gateoverflow.in/3511



Consider the following two transactions: $T1$ and $T2$.

```
T1 :      read (A);      T2 :      read (B);
        read (B);      read (A);
        If A = 0 then B ← B + 1;  If B ≠ 0 then A ← A - 1;
        write (B);      write (A);
```

Which of the following schemes, using shared and exclusive locks, satisfy the requirements for strict two phase locking for the above transactions?

- A.
- | | |
|---|--|
| <p><i>S1</i> :</p> <p>lock S(A);</p> <p>read (A);</p> <p>lock S(B);</p> <p>read (B);</p> <p>If $A = 0$</p> <p>then $B \leftarrow B + 1$;</p> <p>write (B);</p> <p>commit;</p> <p>unlock (A);</p> <p>unlock (B);</p> | <p><i>S2</i> :</p> <p>lock S(B);</p> <p>read (B);</p> <p>lock S(A);</p> <p>read (A);</p> <p>If $B \neq 0$</p> <p>then $A \leftarrow A - 1$;</p> <p>write (A);</p> <p>commit;</p> <p>unlock (B);</p> <p>unlock (A);</p> |
|---|--|
-
- B.
- | | |
|---|--|
| <p><i>S1</i> :</p> <p>lock X(A);</p> <p>read (A);</p> <p>lock X(B);</p> <p>read (B);</p> <p>If $A = 0$</p> <p>then $B \leftarrow B + 1$;</p> <p>write (B);</p> <p>unlock (A);</p> <p>commit;</p> <p>unlock (B);</p> | <p><i>S2</i> :</p> <p>lock X(B);</p> <p>read (B);</p> <p>lock X(A);</p> <p>read (A);</p> <p>If $B \neq 0$</p> <p>then $A \leftarrow A - 1$;</p> <p>write (A);</p> <p>unlock (A);</p> <p>commit;</p> <p>unlock (A);</p> |
|---|--|
-
- C.
- | | |
|---|--|
| <p><i>S1</i> :</p> <p>lock S(A);</p> <p>read (A);</p> <p>lock X(B);</p> <p>read (B);</p> <p>If $A = 0$</p> <p>then $B \leftarrow B + 1$;</p> <p>write (B);</p> <p>unlock (A);</p> <p>commit;</p> <p>unlock (B);</p> | <p><i>S2</i> :</p> <p>lock S(B);</p> <p>read (B);</p> <p>lock X(A);</p> <p>read (A);</p> <p>If $B \neq 0$</p> <p>then $A \leftarrow A - 1$;</p> <p>write (A);</p> <p>unlock (B);</p> <p>commit;</p> <p>unlock (A);</p> |
|---|--|
-
- D.
- | | |
|---|--|
| <p><i>S1</i> :</p> <p>lock S(A);</p> <p>read (A);</p> <p>lock X(B);</p> <p>read (B);</p> <p>If $A = 0$</p> <p>then $B \leftarrow B + 1$;</p> <p>write (B);</p> <p>unlock (A);</p> <p>unlock (B);</p> <p>commit;</p> | <p><i>S2</i> :</p> <p>lock S(B);</p> <p>read (B);</p> <p>lock X(A);</p> <p>read (A);</p> <p>If $B \neq 0$</p> <p>then $A \leftarrow A - 1$;</p> <p>write (A);</p> <p>unlock (A);</p> <p>unlock (A);</p> <p>commit;</p> |
|---|--|

gate2007-it databases transaction-and-concurrency normal

Answer 



Consider the following three schedules of transactions T1, T2 and T3. [Notation: In the following NYO represents the action Y (R for read, W for write) performed by transaction N on object O.]

(S1)	2RA	2WA	3RC	2WB	3WA	3WC	1RA	1RB	1WA	1WB
(S2)	3RC	2RA	2WA	2WB	3WA	1RA	1RB	1WA	1WB	3WC
(S3)	2RA	3RC	3WA	2WA	2WB	3WC	1RA	1RB	1WA	1WB

Which of the following statements is TRUE?

- A. S1, S2 and S3 are all conflict equivalent to each other
- B. No two of S1, S2 and S3 are conflict equivalent to each other
- C. S2 is conflict equivalent to S3, but not to S1
- D. S1 is conflict equivalent to S2, but not to S3

gate2008-it databases transaction-and-concurrency normal

Answer

Answers: Transaction And Concurrency

3.17.1 Transaction And Concurrency: GATE CSE 1999 | Question: 2.6 top

<https://gateoverflow.in/1484>



If we draw the precedence graph we get a loop, and hence the schedule is not conflict serializable.

There is no blind write too so, there is no chance that view serializability can occur.

Now 2pl ensures CS.

Since possibility of CS is ruled out at the onset, so schedule cannot occur in 2PL.

Ans d)

42 votes

-- Sourav Roy (2.9k points)

3.17.2 Transaction And Concurrency: GATE CSE 2003 | Question: 29, ISRO2009-73 top

<https://gateoverflow.in/919>



✓

- A. Here if transaction writing data commits, then transaction which read the data might get phantom tuple/ Unrepeatable error. Though there is no irrecoverable error possible even in this option.
- B. This is non issue. Both transaction reading data.
- C. This is non issue.
- D. This is dirty read. In case if transaction reading uncommitted data commits, irrecoverable error occurs of uncommitted transaction fails. So (D) is answer

42 votes

-- Akash Kanase (36k points)

3.17.3 Transaction And Concurrency: GATE CSE 2003 | Question: 87 top

<https://gateoverflow.in/970>



✓

There is a cycle in precedence graph so schedule is not conflict serialisable.

Check View Serializability:

Checking View Serializability is NPC problem so proving by contradiction..

1. Initial Read

T_2 read D_2 value from initial database and T_1 modify D_2 so T_2 should execute before T_1 .
i.e., $T_2 \rightarrow T_1$

2. Final write.

final write of D_1 in given schedule done by T_2 and T_1 modify D_1 i.e. $W(D_1)$.
that means T_2 should execute after T_1 .
i.e., $T_1 \rightarrow T_2$

So, schedule not even View Serializable.

Not Serializable.

Correct Answer: D

39 votes

-- Digvijay (44.9k points)

3.17.4 Transaction And Concurrency: GATE CSE 2006 | Question: 20, ISRO2015-17

https://gateoverflow.in/981



Answer should be B. Here we are not using checkpoints so, redo log records 2 and 3 and undo log record 6. Consider the following steps taken from the book 'Navathe':

PROCEDURE RIU_M

1. Use two lists of transactions maintained by the system: the committed transactions since the last checkpoint and the active transactions
2. Undo all the *write_item* operations of the *active* (uncommitted) transaction, using the UNDO procedure. The operations should be undone in the reverse order in which they were written into the log.
3. Redo all the *write_item* operations of the *committed* transactions from the log, in the order in which they were written into the log.

105 votes

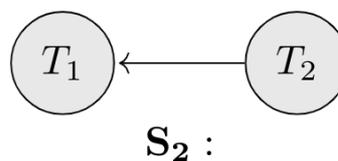
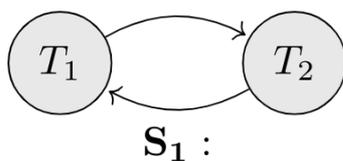
-- Pooja Palod (24.1k points)

3.17.5 Transaction And Concurrency: GATE CSE 2007 | Question: 64

https://gateoverflow.in/1262



- For S_1 : it is **not conflict serializable**
- For S_2 : it is **conflict serializable**



Answer is option C.

28 votes

-- Amar Vashishth (25.2k points)

3.17.6 Transaction And Concurrency: GATE CSE 2009 | Question: 43

https://gateoverflow.in/1329



- The answer is B.
- S_1 has a cycle from $T_1 \rightarrow T_2$ and $T_2 \rightarrow T_1$.
- S_2 -- It is uni-directional and has only $T_2 \rightarrow T_1$.
- S_3 -- It is uni-directional and has only $T_1 \rightarrow T_2$.
- S_4 -- same as S_1 .

A schedule is conflict serializable if there is no cycle in the directed graph made by the schedules.

In the schedules we check for RW, WR, WW conflicts between the schedules and only these conflicts contribute in the edges of the graph.

26 votes

-- Gate Keeda (15.9k points)

3.17.7 Transaction And Concurrency: GATE CSE 2010 | Question: 20

https://gateoverflow.in/2196



- In basic two phase locking there is a chance for deadlock
- Conservative 2pl is deadlock free

I go with B.

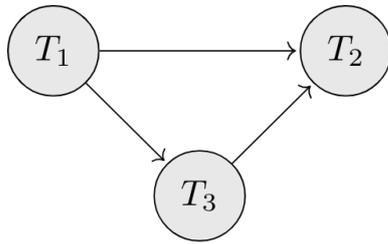
49 votes

-- Sankaranarayanan P.N (8.5k points)



✓ Answer is option A.

create precedence graph and apply [Topological sort](#) on it to obtain
 $T_1 \rightarrow T_3 \rightarrow T_2$



References



👍 42 votes

-- Amar Vashishth (25.2k points)



✓ Answer is (B). Explanation: $T_1 : r(P), r(Q), w(Q)$ $T_2 : r(Q), r(P), w(P)$ now, consider any non serial schedule for example, $S : r_1(P), r_2(Q), r_1(Q), r_2(P), w_1(Q), w_2(P)$ now, draw a precedence graph for this schedule. here there is a conflict from $T_1 \rightarrow T_2$ and there is a conflict from $T_2 \rightarrow T_1$ therefore, the graph will contain a cycle. so we can say that the schedule is not conflict serializable.

👍 68 votes

-- jayendra (6.7k points)



✓ (D) make precedence graph for all the options, for option (D) only graph will be acyclic, hence (D) is CSS.

👍 22 votes

-- Manu Thakur (34k points)



✓ Answer: S is both conflict serializable and recoverable.

Recoverable? Look if there are any dirty reads? Since there are no dirty read, it simply implies schedule is recoverable(if there were dirty read, then we would have taken into consideration the order in which transactions commit)

Conflict serializable? Draw the precedence graph(make edges if there is a conflict instruction among T_i and T_j . But for the given schedule, no cycle exists in precedence graph, thus it's conflict serializable.

Hope this helps.

👍 50 votes

-- Ramandeep Singh (131 points)

Even though [@Ramandeep Singh](#) has answered this question, I'd like to add some additional points because in the comments and discussion on this question, many students are having incorrect arguments which they think are correct.

The Mistake that most students are doing (in the comments to this question) is that they are Not making correct Precedence Graph because they are not making conflict edges in the Precedence graph "from a committed transaction to a newly started transaction"....which is completely wrong because if you do so then How will you make Precedence Graph for Serial Schedule??

Following all the definitions and concepts are directly (without modification) picked mostly from **Navathe** and some from the following link : <http://www.ict.griffith.edu.au/~rwt/uoe/1.1.ccc.html>

Refer Navathe if you still have some doubt.

Transactions : gateoverflow.in gateoverflow.in classroom.gateover

A *transaction* is effectively a sequence of read and write operations on atomic database items. A transaction may be incomplete because the (database) system crashes, or because it is *aborted* by either the system or the user (or application). Complete transactions are *committed*. **Transactions must terminate by either aborting or committing.**

Complete Schedule :

A schedule S of n transactions T_1, T_2, \dots, T_n is said to be a complete schedule if the following conditions hold:

1. The operations in S are exactly those operations in T_1, T_2, \dots, T_n , **including a commit or abort operation as the last operation for each transaction in the schedule.** gateoverflow.in classroom.gateover
2. For any pair of operations from the same transaction T_i , their relative order of appearance in S is the same as their order of appearance in T_i . (i.e Operation order in/of every transaction must preserve.)
3. For any two conflicting operations, one of the two must occur before the other in the schedule.

Condition 1 simply states that all operations in the transactions must appear in the complete schedule. Since every transaction has either committed or aborted, **a complete schedule will not contain any active transactions at the end of the schedule.**

In general, it is difficult to encounter complete schedules in a transaction processing system because new transactions are continually being submitted to the system. Hence, it is useful to define the concept of the committed projection $C(S)$ of a schedule S .

Committed Projection of a schedule :

Committed Projection $C(S)$ of a schedule S includes only the operations in S that belong to **committed transactions**—that is, transactions T_i whose commit operation C_i is in S .

Given a schedule S , the committed projection $C(S)$ is the subset of S consisting of operations ($r_1(X), w_2(Y)$, etc) that are part of transactions that have committed (that is, $r_1(X)$ would be part of $C(S)$ only if transaction 1's commit, c_1 , were also part of S). This is sometimes useful in analyzing schedules when transactions are continuously being added.

A committed projection $C(S)$ of a schedule S includes the operations in S only from the committed transactions. Let's take an example :

Transactions:

- $T_1 : r_1(X); w_1(X); r_1(Y); w_1(Y); c_1;$
- $T_2 : r_2(Y); w_2(Y); a_2;$
- $T_3 : r_3(X); w_3(X);$
- $S_1 : r_1(X); r_2(Y); w_1(X); w_2(Y); r_1(Y); a_2; w_1(Y); c_1; r_3(X); w_3(X);$

Then $C(S_1) = ??$

Well, $C(S_1)$ will be the same as T_1 because T_3 has No Commit/Abort operation as the last operation of the transaction and T_2 is Not committed. So, by the definition of Committed Transaction, $C(S_1) = T_1$.

Now, as according to Navathe,

We can theoretically define a schedule S to be serializable if **its committed projection $C(S)$ is equivalent to some serial schedule, since only committed transactions are guaranteed by the DBMS.**

And It applies to both Conflict and View Serializability.

A schedule is serialisable if the effect of its committed projection (the restriction to its committed transactions) on any consistent database is identical to that of some serial schedule of its committed transactions.

(Conflict) Serialisability theorem :

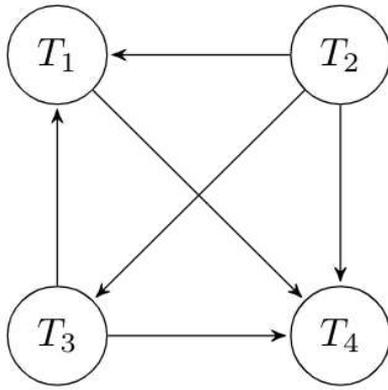
Given a schedule S , define the serialisation graph(Precedence Graph) $SG(S)$ to have the committed transactions of S as its **nodes**, and a directed edge from T_1 to T_2 if T_1 and T_2 contain conflicting operations O_1 and O_2 such that O_1 precedes O_2 in S . Then S is serialisable if and only if $SG(S)$ is acyclic.

<http://www.ict.griffith.edu.au/~rwt/uoe/1.1.ccc.html>

Now, coming to the given question :

The given schedule is Complete Schedule as all the transactions in the schedule are committed(or aborted). Moreover, the given schedule is Committed Projection of itself as well because all the Transactions are committed. Now, as the above definition of Conflict serializability suggests, we make Precedence graph for this schedule and in the precedence graph, the Nodes will be the Transactions participating in the committed projection of the schedule(which is same as the given schedule) ..

The precedence graph will be as following :



From the precedence graph we can see that Only One serial schedule is conflict equivalent to the given schedule which is $T_2, T_3, T_1, T_4, \dots$. No other schedule is conflict equivalent to the given schedule.

Only One serial schedule is conflict equivalent to the given schedule which is $T_2, T_3, T_1, T_4, \dots$. This makes sense because T_2 is reading the initial value of data item X (directly from the database) But if we run either of T_3 or T_1 before T_2 then they will write the data item X and T_2 will have to read the modified value of X . Hence, Only one Serial Schedule can be equivalent to the given schedule and that is T_2, T_3, T_1, T_4 .

The Mistake that most students are doing (in the comments to this question) is that they are Not making correct Precedence Graph because they are not making conflict edges from a committed transaction to a new started transaction....which is completely wrong because if you do so then How will you make Precedence Graph for Serial Schedule??

Serial Schedule (Definition as it is given in Navathe) : Formally, a schedule S is serial if, for every transaction T participating in the schedule, all the operations of T are executed consecutively in the schedule; otherwise, the schedule is called nonserial. Therefore, in a serial schedule, only one transaction at a time is active—the commit (or abort) of the active transaction initiates execution of the next transaction. No interleaving occurs in a serial schedule.

$S = R_1(X) W_1(X) C1 R_2(X) W_2(X) C2 R_3(X) W_3(X) C3$

If you make precedence graph for this schedule, then you must get a acyclic precedence graph But those students who are not putting conflict edges in the precedence graph "from a committed transaction to a newly started transaction" then you won't get any edges in this graph and the graph will be empty graph, which you know is not correct.

Consider this schedule :

T_1	T_2	T_3
	Write(X)	
Writes(Z)		
Writes(X)		
Commit		
	Writes(Y)	
	Reads(Y)	
		Writes(Z)
		Writes(M)
		Commit
	Reads(M)	
	Commit	

Try to find whether this schedule is Conflict Serializable Or Not??

If you do it correctly, It is Not conflict serializable because there is Cycle in the precedence graph of this schedule. But If you don't put conflict edges in the precedence graph "from a committed transaction (T_1) to a newly started transaction (T_3)" then you won't get edge $T_1 \rightarrow T_3$ in the precedence graph and hence, you will incorrectly get the answer as Conflict serializable.

References



classroom.gateoverflow.in

gateoverflow.in

classroom.gateover

45 votes

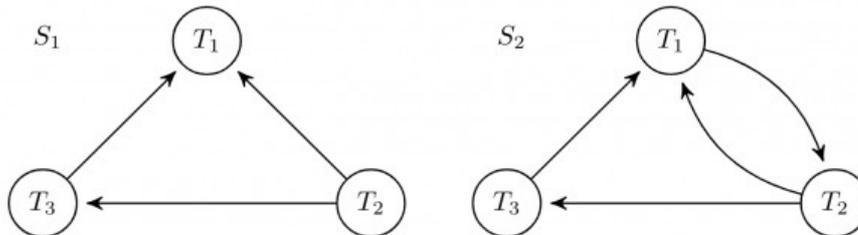
-- Deepak Poonia (23.4k points)

3.17.12 Transaction And Concurrency: GATE CSE 2014 Set 3 | Question: 29 [top](#)

<https://gateoverflow.in/2063>



✓



classroom.gateover

S_1 has no cycle hence, **Conflict-Serializable**

S_2 has cycle hence **NOT Conflict-Serializable**

Answer is option A.

37 votes

-- Amar Vashishth (25.2k points)

3.17.13 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 1 [top](#)

<https://gateoverflow.in/8047>



✓

B. Consistency

In the given transaction Atomicity guarantees that the said constraint is satisfied. But this constraint is not part of Atomicity property. It is just that Atomicity implies Consistency here.

23 votes

-- Arjun Suresh (332k points)

3.17.14 Transaction And Concurrency: GATE CSE 2015 Set 2 | Question: 46 [top](#)

<https://gateoverflow.in/8246>



✓

T1	T2	T3	T4
			start
			w(y, 2, 3)
start			
			commit
w(z, 5, 7)			
checkpoint	checkpoint	checkpoint	checkpoint
	start		
	w(x, 1, 9)		
	commit		
		start	
		w(z, 7, 2)	
crash	crash	crash	crash

Now from the table we can find that $T1$ and $T3$ has uncommitted write operation, so they must be undone. Even though $T2$ has committed after writing, but it is after checkpoint. So, it needs to be redone.

Answer is A.

71 votes

-- worst_engineer (2.8k points)



✓ The correct option is B.

Why A is not correct because it says abort transaction T2 and then redo all the operations .

But is there a guarantee that it will succeed this time ??(no maybe again T1 will fail).

Now as to why b is correct because as the other answer points out it is by definition an irrecoverable schedule now even if we start to undo the actions on by one(after t1 fails) in order to ensure transaction atomicity. Still we cannot undo a committed transaction. Hence, this schedule is unrecoverable by definition and also not atomic since it leaves the data base in an inconsistent state.

👍 66 votes

-- Tamojit Chatterjee (1.9k points)



- ✓ A - Atomicity
- C - Consistency
- I - Isolation
- D - Durability.

Answer (D)

👍 33 votes

-- Abhilash Panicker (7.6k points)



✓ Two Phase Locking protocol is conflict serializable. So this is a modified version of the basic 2PL protocol, So serializability should be guaranteed.. and we can get a serializable scheduling by ordering based on Lock points(same as in basic 2PL).

Now in Step 1, exclusive locks are acquired to O_1, O_2, O_3, \dots in increasing order of addresses..since it is mentioned as exclusive lock, only one transaction can lock the object..

Due to acquiring of locks based on ordering of addresses.. and locks aren't released until the transaction completes its operation.. we can prevent the circular wait condition, and hence making it deadlock free.

So, the answer should be (A) guarantees serializability and deadlock freedom

👍 78 votes

-- Abhilash Panicker (7.6k points)



✓ Topological Order.

👍 24 votes

-- Sharathkumar Anbu (595 points)



✓ Answer is C

T1	T2
R(x)	R(x)
W(x)	R(y)
R(y)	W(x)
a1	a2

- (A): This is not possible, because we have no dirty read ! No dirty read \implies Recoverable
- (B): This is not possible, because of no Dirty read ! No dirty read \implies No cascading aborts !
- (D): This is not true, because we can see clearly in image that after $W_1(X)$ before T_1 commit or aborts T_2 does $W_2(x)$!
- C is only option remaining !

👍 62 votes

-- Akash Kanase (36k points)

3.17.20 Transaction And Concurrency: GATE CSE 2019 | Question: 11 [top](#)

<https://gateoverflow.in/302837>



1. Strict 2PL allows only schedules whose precedence graph is acyclic i.e. schedule is Conflict Serial. In 2PL, transactions do not release exclusive locks until the transaction has committed or aborted i.e. schedule is recoverable.
2. Time stamp ordering schedule with Thomas write rule generate View serial schedule with BLIND WRITE. Because of BLIND WRITE it won't be Conflict Serial.

So, Option C - both are true

👍 41 votes

-- Digvijay (44.9k points)

3.17.21 Transaction And Concurrency: GATE CSE 2020 | Question: 37 [top](#)

<https://gateoverflow.in/333194>



If you draw the dependency graph, you'll notice that there is a cycle. Hence **Option (D)** and **Option (B)** are straightaway **False**.

Now in **Option (C)**, there is a swapping operation of conflicting operations $W_1(D)$ and $R_2(D)$. Hence it's **False** as well.

Hence, **Option(A)** is the answer

👍 8 votes

-- Debasish Das (1.5k points)

3.17.22 Transaction And Concurrency: GATE CSE 2021 Set 1 | Question: 13 [top](#)

<https://gateoverflow.in/357439>



Answer: A

Ideation/Source of the content: Navathe 6th Edition, 22.1: Recovery Concepts

Explanation:

Support for option A and against option C: Since check-pointing is not used we have to depend on the system logs. Let's suppose we have three transactions A, B and C. Also assume that transaction A and C commits before failure and B was started but the system crashed before it can commit. So, in the first recovery process database will redo A and C as per the system logs. Now consider that while redoing A successfully commits, the system crashed for the second time before the B can commit. So, while recovering for the second time the same system logs will be used. However, it should be noted that the system logs will also have entry to redo transaction A since it was committed after the first failure. However, the undo/redo operations are idempotent (they are the same no matter how many time they are executed).

Against option B: If the system crashes again same logic as above can be used for recovery.

Against option D: Inconsistency refers to situations (generally) when the value of a shared variable varies in two or more transactions, but that doesn't seem to happen here as no uncommitted transaction's data is being read/written during the entire recovery process.

Conclusion: So, the only option of selecting the same list for undo/redo seems to be correct.

👍 1 votes

-- Abhishek Dutta (145 points)

3.17.23 Transaction And Concurrency: GATE IT 2004 | Question: 21 [top](#)

<https://gateoverflow.in/3662>



Row level locking provides more concurrency, because different transactions can access different rows in a table / page at same time,

Correct Answer: C

👍 41 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ There is a cycle in the precedence graph - so the given schedule is not Conflict Serializable.

If a schedule is view serializable but not conflict serializable it MUST have one or more blind writes. Here, there is no blind writes. So, the given schedule is not even view serializable.

Option D is the Answer.

👍 51 votes

-- Sandeep_Uniyal (6.5k points)



- ✓ Answer **d**. Irrespective of any failure the successful result of transaction should persist.

Suppose we book ticket 2 months in advance in irctc and transaction success.

Then when we are going to board the train on that time they tells because of system/disk/power crash they dont have your seat information and you are not allowed in the seat.

it is a serious problem. hence result should persist irrespective of all crashes.

👍 89 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ **Correct Answer : D**

$T3$ followed by $T2$ followed by $T1$ will be correct execution sequence:

other cases some people will get two times increment

eg. if we have $T1$ followed by $T2$

if initial commision is 49500

then he is belonging to < 50000

hence, $49500 * 1.02 = 50490$

now, he is eligible in second category

then, $50490 * 1.04 = 52509.6$

so, he wil get increment two times. but he is eligible for only one slab of commision.

👍 91 votes

-- Sankaranarayanan P.N (8.5k points)



- ✓ **Answer is (C).**

Many of you would point a DEADLOCK and I won't deny But see Question just asks for requirement to follow Strict 2PL. Requirement are

1. **Exclusive locks should be released after the commit.**
2. **No Locking can be done after the first Unlock and vice versa.**

In 2PL deadlock may occur BUT it may be that it doesn't occur at all.

Consider that in option (C) if both execute in serial order without concurrency. Then that is perfectly valid and YES it follows Strict 2PL.

👍 50 votes

-- Sandeep_Uniyal (6.5k points)



- ✓ Two schedules are conflict equivalent if we can derive one schedule by swapping the non-conflicting operations of the other schedule.

S1

<i>T1</i>	<i>T2</i>	<i>T3</i>
	<i>R(A)</i>	
	<i>W(A)</i>	
		<i>R(C)</i>
	<i>W(B)</i>	
		<i>W(A)</i>
		<i>W(C)</i>
<i>R(A)</i>		
<i>R(B)</i>		
<i>W(A)</i>		
<i>W(B)</i>		

Here, we can swap *R(C)* and *W(B)* since they are non-conflicting pair (since they are operating on different data items)

After swapping the schedule will become $T2 \rightarrow T3 \rightarrow T1$

<i>T1</i>	<i>T2</i>	<i>T3</i>
	<i>R(A)</i>	
	<i>W(A)</i>	
	<i>W(B)</i>	
		<i>R(C)</i>
		<i>W(A)</i>
		<i>W(C)</i>
<i>R(A)</i>		
<i>R(B)</i>		
<i>W(A)</i>		
<i>W(B)</i>		

S2

<i>T1</i>	<i>T2</i>	<i>T3</i>
		<i>R(C)</i>
	<i>R(A)</i>	
	<i>W(A)</i>	
	<i>W(B)</i>	
		<i>W(A)</i>
<i>R(A)</i>		
<i>R(B)</i>		
<i>W(A)</i>		
<i>W(B)</i>		
		<i>W(C)</i>

Here, we can swap and write *R(C)* after performing *T2* operations:- *R(A)*, *W(A)* and *W(B)* since each of them form non-conflicting pair with *R(C)* (since they are operating on different data items)

Also, we can swap *W(C)* and can execute it before all the *T1* operations as each of the *t1* operations are forming non-conflicting pair with *W(C)* (since they are operating on different data items)

After swapping the schedule will become $T2 \rightarrow T3 \rightarrow T1$

$T1$	$T2$	$T3$
	$R(A)$	
	$W(A)$	
	$W(B)$	
		$R(C)$
		$W(A)$
		$W(C)$
$R(A)$		
$R(B)$		
$W(A)$		
$W(B)$		

S3

$T1$	$T2$	$T3$
	$R(A)$	
		$R(C)$
		$W(A)$
	$W(A)$	
	$W(B)$	
		$W(C)$
$R(A)$		
$R(B)$		
$W(A)$		
$W(B)$		

Here, we can't swap the operations and make it as $T2 \rightarrow T3 \rightarrow T1$ because of the conflicting pairs $W(A)$ and $W(A)$

\therefore Option D. $S1$ is conflict equivalent to $S2$, but not to $S3$ is the correct answer.

👍 17 votes

-- Satbir Singh (21k points)

Answer Keys

3.1.1	N/A	3.1.2	N/A	3.1.3	N/A	3.1.4	N/A	3.1.5	B
3.1.6	N/A	3.1.7	B	3.1.8	N/A	3.1.9	N/A	3.1.10	N/A
3.1.11	C	3.1.12	B	3.1.13	C	3.1.14	D	3.1.15	A
3.1.16	C	3.1.17	C	3.1.18	B	3.1.19	5	3.1.20	50
3.1.21	A	3.1.22	52	3.1.23	B	3.1.24	C	3.1.25	A
3.1.26	C	3.1.27	A	3.1.28	A	3.2.1	N/A	3.2.2	A
3.2.3	8	3.2.4	19	3.2.5	B	3.3.1	54	3.3.2	B
3.3.3	B	3.4.1	False	3.5.1	True	3.5.2	N/A	3.5.3	N/A
3.5.4	N/A	3.5.5	N/A	3.5.6	N/A	3.5.7	B;D	3.5.8	False
3.5.9	N/A	3.5.10	A	3.5.11	D	3.5.12	N/A	3.5.13	B
3.5.14	D	3.5.15	B	3.5.16	C	3.5.17	A	3.5.18	N/A
3.5.19	C	3.5.20	C	3.5.21	D	3.5.22	B	3.5.23	C

3.5.24	D	3.5.25	C	3.5.26	D	3.5.27	C	3.5.28	A
3.5.29	C	3.5.30	B	3.5.31	A	3.5.32	B	3.5.33	A
3.5.34	C	3.5.35	B	3.5.36	B	3.5.37	A	3.5.38	B
3.5.39	C	3.5.40	A	3.5.41	A	3.5.42	A;C;D	3.5.43	B
3.5.44	A	3.5.45	B	3.5.46	B	3.5.47	A	3.5.48	D
3.5.49	A	3.6.1	B	3.6.2	B	3.6.3	A	3.6.4	C
3.6.5	4	3.6.6	C	3.6.7	A	3.6.8	A	3.6.9	B
3.6.10	C	3.7.1	N/A	3.7.2	N/A	3.7.3	3	3.7.4	C
3.7.5	A	3.7.6	C	3.7.7	C	3.7.8	C	3.7.9	C
3.7.10	4	3.7.11	698 : 698	3.8.1	A	3.8.2	A	3.8.3	A
3.8.4	C	3.8.5	B	3.8.6	A	3.8.7	A	3.9.1	C
3.10.1	C	3.10.2	A	3.10.3	C	3.11.1	B	3.11.2	C
3.11.3	0.00	3.11.4	D	3.12.1	N/A	3.12.2	N/A	3.12.3	N/A
3.12.4	N/A	3.12.5	N/A	3.12.6	N/A	3.12.7	D	3.12.8	N/A
3.12.9	B	3.12.10	C	3.12.11	D	3.12.12	C	3.12.13	N/A
3.12.14	A	3.12.15	D	3.12.16	B	3.12.17	D	3.12.18	A
3.12.19	A	3.12.20	D	3.12.21	D	3.12.22	4	3.12.23	C
3.12.24	1	3.12.25	C	3.12.26	B	3.13.1	N/A	3.13.2	N/A
3.13.3	D	3.13.4	C	3.13.5	C	3.13.6	C	3.13.7	B
3.13.8	C	3.13.9	C	3.13.10	A	3.13.11	A	3.13.12	D
3.13.13	D	3.13.14	C	3.14.1	D	3.15.1	N/A	3.15.2	N/A
3.15.3	N/A	3.15.4	N/A	3.15.5	N/A	3.15.6	N/A	3.15.7	N/A
3.15.8	D	3.15.9	N/A	3.15.10	N/A	3.15.11	A	3.15.12	C
3.15.13	N/A	3.15.14	C	3.15.15	N/A	3.15.16	N/A	3.15.17	N/A
3.15.18	C	3.15.19	D	3.15.20	D	3.15.21	C	3.15.22	B
3.15.23	C	3.15.24	A	3.15.25	X	3.15.26	C	3.15.27	A
3.15.28	C	3.15.29	C	3.15.30	B	3.15.31	D	3.15.32	B
3.15.33	C	3.15.34	D	3.15.35	2	3.15.36	A	3.15.37	2
3.15.38	2.6	3.15.39	7	3.15.40	D	3.15.41	5	3.15.42	A
3.15.43	819 : 820 ; 205 : 205	3.15.44	B	3.15.45	D	3.15.46	C	3.15.47	C
3.15.48	D	3.15.49	A	3.15.50	B	3.15.51	D	3.16.1	A
3.17.1	D	3.17.2	D	3.17.3	D	3.17.4	B	3.17.5	C
3.17.6	B	3.17.7	B	3.17.8	A	3.17.9	B	3.17.10	D
3.17.11	C	3.17.12	A	3.17.13	B	3.17.14	A	3.17.15	B
3.17.16	D	3.17.17	A	3.17.18	A	3.17.19	C	3.17.20	C
3.17.21	A	3.17.22	A	3.17.23	C	3.17.24	X	3.17.25	D

3.17.26

D

3.17.27

C

3.17.28

D



Boolean algebra. Combinational and sequential circuits. Minimization. Number representations and computer arithmetic (fixed and floating point)

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	2	3	2	4	2	3	2	3	3	2	2.6	4
2 Marks Count	2	2	1	2	2	0	4	2	0	0	1.6	4
Total Marks	6	7	4	8	6	3	10	7	3	3	6	10

4.1

Adder (10) [top](#)4.1.1 Adder: GATE CSE 1988 | Question: 4ii [top](#)
<https://gateoverflow.in/94360>


Using binary full adders and other logic gates (if necessary), design an adder for adding 4-bit number (including sign) in 2's complement notation.

gate1988 digital-logic descriptive adder

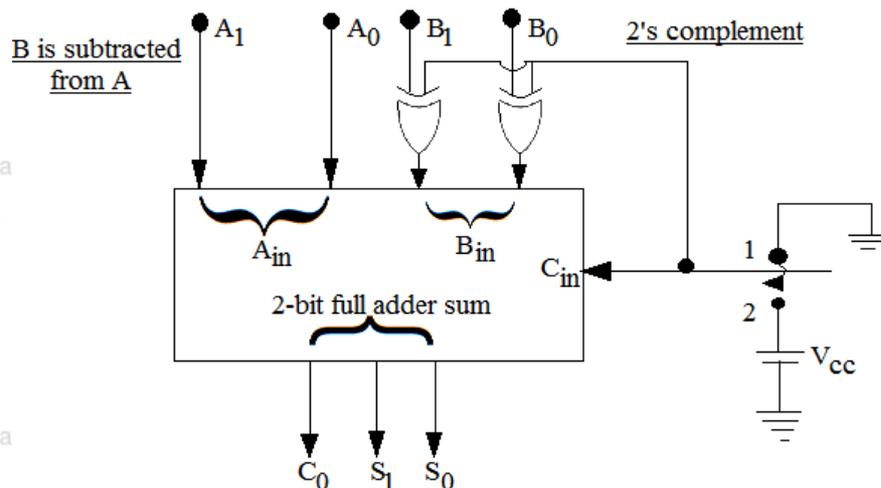
[goclasses.in](#)
[tests.gatecse.in](#)

Answer [🔒](#)

4.1.2 Adder: GATE CSE 1990 | Question: 1-i [top](#)
<https://gateoverflow.in/83829>


Fill in the blanks:

In the two bit full-adder/subtractor unit shown in below figure, when the switch is in position 2 _____ using _____ arithmetic.



gate1990 digital-logic adder fill-in-the-blanks

Answer [🔒](#)

4.1.3 Adder: GATE CSE 1993 | Question: 9 [top](#)
<https://gateoverflow.in/2306>


Assume that only half adders are available in your laboratory. Show that any binary function can be implemented using half adders only.

gate1993 digital-logic combinational-circuits adder descriptive

Answer [🔒](#)

4.1.4 Adder: GATE CSE 1997 | Question: 2.5 [top](#)
<https://gateoverflow.in/2231>


An N -bit carry lookahead adder, where N is a multiple of 4, employs ICs 74181 (4 bit ALU) and 74182 (4 bit carry lookahead generator).

The minimum addition time using the best architecture for this adder is

- A. proportional to N
- B. proportional to $\log N$
- C. a constant
- D. None of the above

gate1997 digital-logic normal adder

Answer

4.1.5 Adder: GATE CSE 1999 | Question: 2.16 [top](#) <https://gateoverflow.in/1494>



The number of full and half-adders required to add 16-bit numbers is

- A. 8 half-adders, 8 full-adders
- B. 1 half-adder, 15 full-adders
- C. 16 half-adders, 0 full-adders
- D. 4 half-adders, 12 full-adders

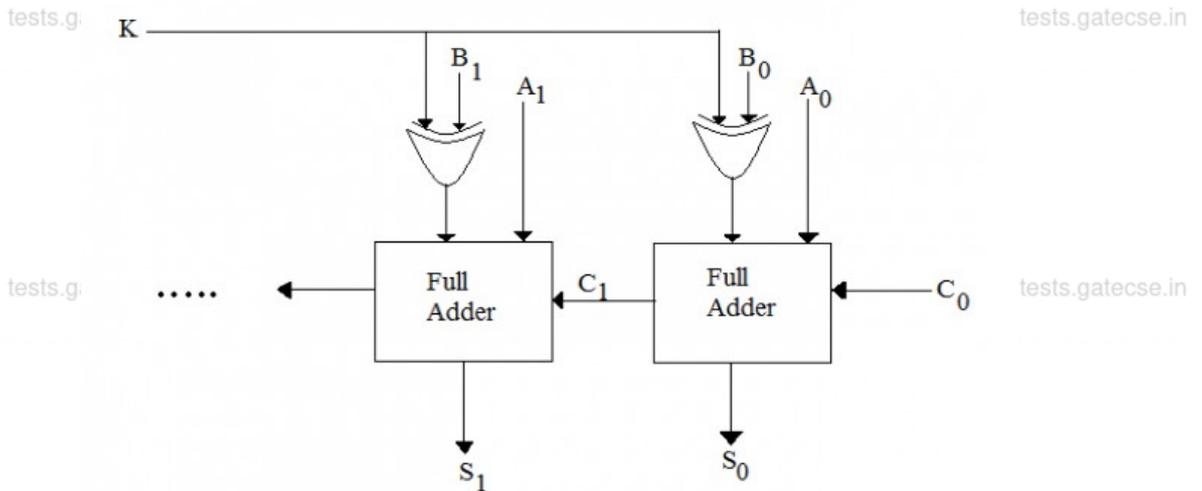
gate1999 digital-logic normal adder

Answer

4.1.6 Adder: GATE CSE 2003 | Question: 46 [top](#) <https://gateoverflow.in/937>



Consider the ALU shown below.



If the operands are in 2^s complement representation, which of the following operations can be performed by suitably setting the control lines K and C_0 only (+ and - denote addition and subtraction respectively)?

- A. $A + B$, and $A - B$, but not $A + 1$
- B. $A + B$, and $A + 1$, but not $A - B$
- C. $A + B$, but not $A - B$ or $A + 1$
- D. $A + B$, and $A - B$, and $A + 1$

gate2003-cse digital-logic normal adder

Answer

4.1.7 Adder: GATE CSE 2004 | Question: 62 [top](#) <https://gateoverflow.in/1057>



A 4-bit carry look ahead adder, which adds two 4-bit numbers, is designed using AND, OR, NOT, NAND, NOR gates only. Assuming that all the inputs are available in both complemented and uncomplemented forms and the delay of each gate is one time

unit, what is the overall propagation delay of the adder? Assume that the carry network has been implemented using two-level AND-OR logic.

- A. 4 time units
- B. 6 time units
- C. 10 time units
- D. 12 time units

gate2004-cse digital-logic normal adder

Answer

4.1.8 Adder: GATE CSE 2015 Set 2 | Question: 48 top

https://gateoverflow.in/8250



A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit-ripple-carry binary adder is implemented by using four full adders. The total propagation time of this 4-bit binary adder in microseconds is _____.

gate2015-cse-set2 digital-logic adder normal numerical-answers

Answer

4.1.9 Adder: GATE CSE 2016 Set 1 | Question: 33 top

https://gateoverflow.in/39688



Consider a carry look ahead adder for adding two n-bit integers, built using gates of fan-in at most two. The time to perform addition using this adder is

- A. $\Theta(1)$
- B. $\Theta(\log(n))$
- C. $\Theta(\sqrt{n})$
- D. $\Theta(n)$

gate2016-cse-set1 digital-logic adder normal

Answer

4.1.10 Adder: GATE CSE 2016 Set 2 | Question: 07 top

https://gateoverflow.in/39573



Consider an eight-bit ripple-carry adder for computing the sum of A and B , where A and B are integers represented in 2's complement form. If the decimal value of A is one, the decimal value of B that leads to the longest latency for the sum to stabilize is _____.

gate2016-cse-set2 digital-logic adder normal numerical-answers

Answer

Answers: Adder

4.1.1 Adder: GATE CSE 1988 | Question: 4ii top

https://gateoverflow.in/94360

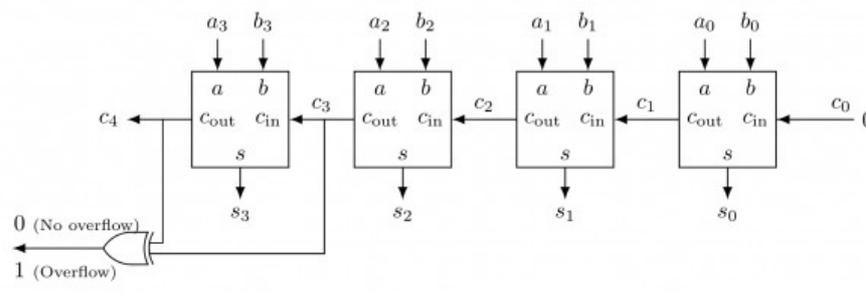


✓ Overflow condition in 2's complement number system:-

1. $c_3 = 1, c_4 = 1 \implies$ No overflow
2. $c_3 = 0, c_4 = 0 \implies$ No overflow
3. $c_3 = 1, c_4 = 0 \implies$ Overflow ($a_3 = b_3 = 0$)
4. $c_3 = 0, c_4 = 1 \implies$ Overflow ($a_3 = b_3 = 1$)

We can conclude that the overflow condition for 2's complement number system is:

$$c_3 \oplus c_4 = 1(\text{OR}) a_3 \cdot \bar{b}_3 \cdot s_3 + a_3 \cdot b_3 \cdot \bar{s}_3 = 1$$



Here, we used 4 – bit binary full adder and Ex-OR gate.

The Ex-OR gate is used to check the overflow condition.

👍 10 votes

-- Lakshman Patel (65.7k points)

4.1.2 Adder: GATE CSE 1990 | Question: 1-i [top](#)

<https://gateoverflow.in/83829>



✓ When the switch is at position 2, it is connected to V_{cc} thus, the value of control input $M = 1$ which is fed to XOR gates as well. So

- $B_1 \oplus 1 = \overline{B_1}$ and
- $B_0 \oplus 1 = \overline{B_0}$

And the basic hardware is of adder only.

Now C_{in} is connected to V_{cc} as well. Hence, $C_{in} = 1$.

Net operation can be denoted as : $S_0 = A_0 + \overline{B_0} + 1$ and similarly for S_1 as well.

This is nothing but an expression of subtraction using 2's complement. (Had it been $A_0 + \overline{B_0}$, it would have been addition of 1's complement merely, but for subtraction we need to have 2's complement of other operand which is B here)

Hence, the correct answer should be : subtraction, 2's complement

👍 34 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

4.1.3 Adder: GATE CSE 1993 | Question: 9 [top](#)

<https://gateoverflow.in/2306>



✓ Half Adder gives two outputs:

- $S = A \oplus B$
- $C = A \cdot B$

We can perform any operation using Half adder if we can implement basic gates using half adder.

- AND operation $C = A \cdot B$
- Not operation = $S(\text{with } A \text{ and } 1) = A \oplus 1 = A' \cdot 1 + A \cdot 1' = A'$
- OR operation = $((A \oplus 1) \cdot (B \oplus 1)) \oplus 1 = (A' \cdot B')' = A + B$

👍 26 votes

-- Praveen Saini (41.9k points)

4.1.4 Adder: GATE CSE 1997 | Question: 2.5 [top](#)

<https://gateoverflow.in/2231>



✓ For $N = 64 \text{ bits}$.

Suppose you want to build a 64 bit adder then you need 16 4-bit ALU and 16 4-bit carry generator, at this point there will be 16 carries that will ripple through these 16 ALU modules, to speed up the adder we need to get rid of these 16 rippling carries, now we can again use 4 4-bit carry generator to generate these 16 carries, now we have only 4 carries to ripple through, again we can use the same trick to minimize the rippling of these 4 carries, we can use an additional 4-bit carry generator which will generate these carry and we are done :) there will be no more propagation of carry among the ALU modules.

So, we have used 3 level of 4-bit carry generator, and the time taken to add 64 bits will be proportional to 3 which is $\log_4 64$.

So, in general to add N – bits it takes $\log_4 N$ time.

Correct Answer: [B](#)

44 votes

[classroom.gateoverflow.in](#)
-- Vikrant Singh (11.2k points)

4.1.5 Adder: GATE CSE 1999 | Question: 2.16 [top 5](#)

<https://gateoverflow.in/1494>



✓ Answer is B.

For LSB addition we do not need a full adder.

For addition of subsequent bits we need full adders since carry from previous addition has to be fed into the addition operation.

55 votes

-- Ankit Rokde (6.9k points)

4.1.6 Adder: GATE CSE 2003 | Question: 46 [top 5](#)

<https://gateoverflow.in/937>



✓ Correct Option: A

There are two control line one is K and another is C_0 .

- When $K = 1$, $C_0 = 1$ we can perform $A - B$
- When $K = 0$, $C_0 = 0$ we can perform $A + B$

But without manipulating $B(B_0, B_1, \dots)$ we cannot perform $A+1$. But here we have only two control lines which is K, C_0 . Therefore the answer is A.

Note:

For A+B : $C_0 = 0$, $K = 0$, and $0 \oplus x = x$

	A_3	A_2	A_1	A_0						
+	B_3	B_2	B_1	B_0						
	S_3	S_2	S_1	S_0						
						C_3	C_2	C_1	$C_0=0$	
						A_3	A_2	A_1	A_0	
						+	B_3	B_2	B_1	B_0
						S_3	S_2	S_1	S_0	
<i>Sum Output:</i>						C_4	C_3	C_2	C_1	
<i>Carry Output:</i>										

For A-B : $C_0 = 1$, $K = 1$, and $1 \oplus x = \bar{x}$

given that numbers are in 2's complement representations, So $A - B = A + 2$'s complement of B

How to get 2's complement of B ?

2's complement of B = 1's complement of B + 1

So, by keeping $K=1$, we get 1's complement of B and By keeping $C_0 = 1$, we are adding 1 to 1's complement of B.

41 votes

-- Riya Roy(Arayana) (5.3k points)

4.1.7 Adder: GATE CSE 2004 | Question: 62 [top 5](#)

<https://gateoverflow.in/1057>



✓ It would take 6 time units.

We know that:

$$G_i = A_i B_i,$$

$$P_i = A_i \oplus B_i \text{ and}$$

$$S_i = P_i \oplus C_i$$

Also

$$C_1 = G_0 + P_0 C_0$$

$$C_2 = G_1 + P_1 G_0 + P_1 P_0 C_0$$

$$C_3 = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_0$$

$$C_4 = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0 + P_3P_2P_1P_0C_0$$

XOR can be implemented in 2 levels; level-1 ANDs and Level-2 OR. Hence it would take 2 time units to calculate P_i and S_i

The 4-bit addition will be calculated in 3 stages

1. **(2 time units)** In 2 time units we can compute G_i and P_i in parallel. 2 time units for P_i since its an XOR operation and 1 time unit for G_i since its an AND operation.

2. **(2 time units)** Once G_i and P_i are available, we can calculate the carries, C_i , in 2 time units.

Level-1 we compute all the conjunctions (AND). Example $P_3G_2, P_3P_2G_1, P_3P_2P_1G_0$ and $P_3P_2P_1P_0C_0$ which are required for C_4 .

Level-2 we get the carries by computing the disjunction (OR).

3. **(2 time units)** Finally we compute the Sum in 2 time units, as its an XOR operation.

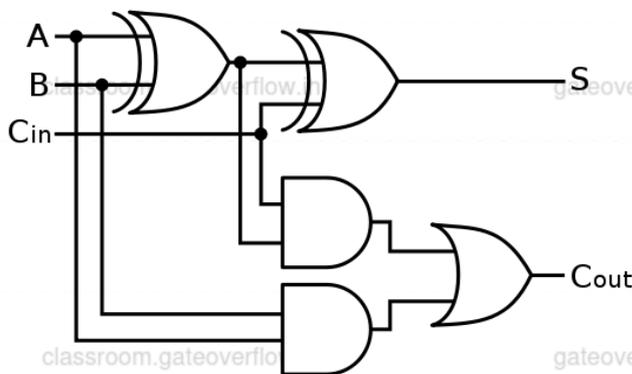
Hence, the total is $2 + 2 + 2 = 6$ time units.

👍 133 votes

-- ryan sequeira (3k points)

4.1.8 Adder: GATE CSE 2015 Set 2 | Question: 48 top 5

<https://gateoverflow.in/8250>



S_1 should wait for C_1 to be ready. Delay for generating C is 1 EXOR + 1 AND + 1 OR = $2.4 + 1.2 + 1.2 = 4.8 \mu s$

Delay for sum is XOR + XOR = $2.4 + 2.4 = 4.8 \mu s$

But for the second adder, there the first EXOR can be done even before waiting for the previous output. So, we can get the sum in Another $2.4 \mu s$ and carry in another $2.4 \mu s$. In this way, 4-bit sum can be obtained after

$$4.8 \mu s + 3 * 2.4 \mu s = 12 \mu s.$$

But the question says we use ripple-carry adder. So, each adder must wait for the full output from the previous adder. This would make the total delay = $4 * 4.8 = 19.2 \mu s$ and this is the key given by GATE, so obviously they meant this.

👍 116 votes

-- Arjun Suresh (332k points)

4.1.9 Adder: GATE CSE 2016 Set 1 | Question: 33 top 5

<https://gateoverflow.in/39688>



✓ Look ahead carry generator gives output in constant time if fan in = number of inputs.

Example, it will take $O(1)$ to calculate $c_4 = g_3 + p_3g_2 + p_3p_2g_1 + p_3p_2p_1g_0 + p_3p_2p_1p_0c_0$, if OR gate with 5 inputs is present.

If we have 8 inputs, and OR gate with 2 inputs, to build an OR gate with 8 inputs, we will need 4 gates in level-1, 2 in level-2 and 1 in level-3. Hence, 3 gate delays, for each level.

Similarly an n-input gate constructed with 2-input gates, total delay will be $O(\log n)$.

Hence, **answer is option B.**

👍 103 votes

-- ryan sequeira (3k points)



✓ Answer is -1.

In case of -1 we get bit sequence 11111111 adding this we get a carry upto carry flag, so largest time to ripple!

👍 57 votes

-- viv696 (1.7k points)

4.2

Array Multiplier (2) [top](#)4.2.1 Array Multiplier: GATE CSE 1999 | Question: 1.21 [top](#)<https://gateoverflow.in/1474>

The maximum gate delay for any output to appear in an array multiplier for multiplying two n bit numbers is

- A. $O(n^2)$
- B. $O(n)$
- C. $O(\log n)$
- D. $O(1)$

gate1999 digital-logic normal array-multiplier

Answer [👍](#)

4.2.2 Array Multiplier: GATE CSE 2003 | Question: 11 [top](#)<https://gateoverflow.in/902>

Consider an array multiplier for multiplying two n bit numbers. If each gate in the circuit has a unit delay, the total delay of the multiplier is

- A. $\Theta(1)$
- B. $\Theta(\log n)$
- C. $\Theta(n)$
- D. $\Theta(n^2)$

gate2003-cse digital-logic normal array-multiplier

Answer [👍](#)

Answers: Array Multiplier

4.2.1 Array Multiplier: GATE CSE 1999 | Question: 1.21 [top](#)<https://gateoverflow.in/1474>

✓ In an $N \times M$ array multiplier we have $N \times M$ AND gates and $(M - 1), N - bit$ adders are used.

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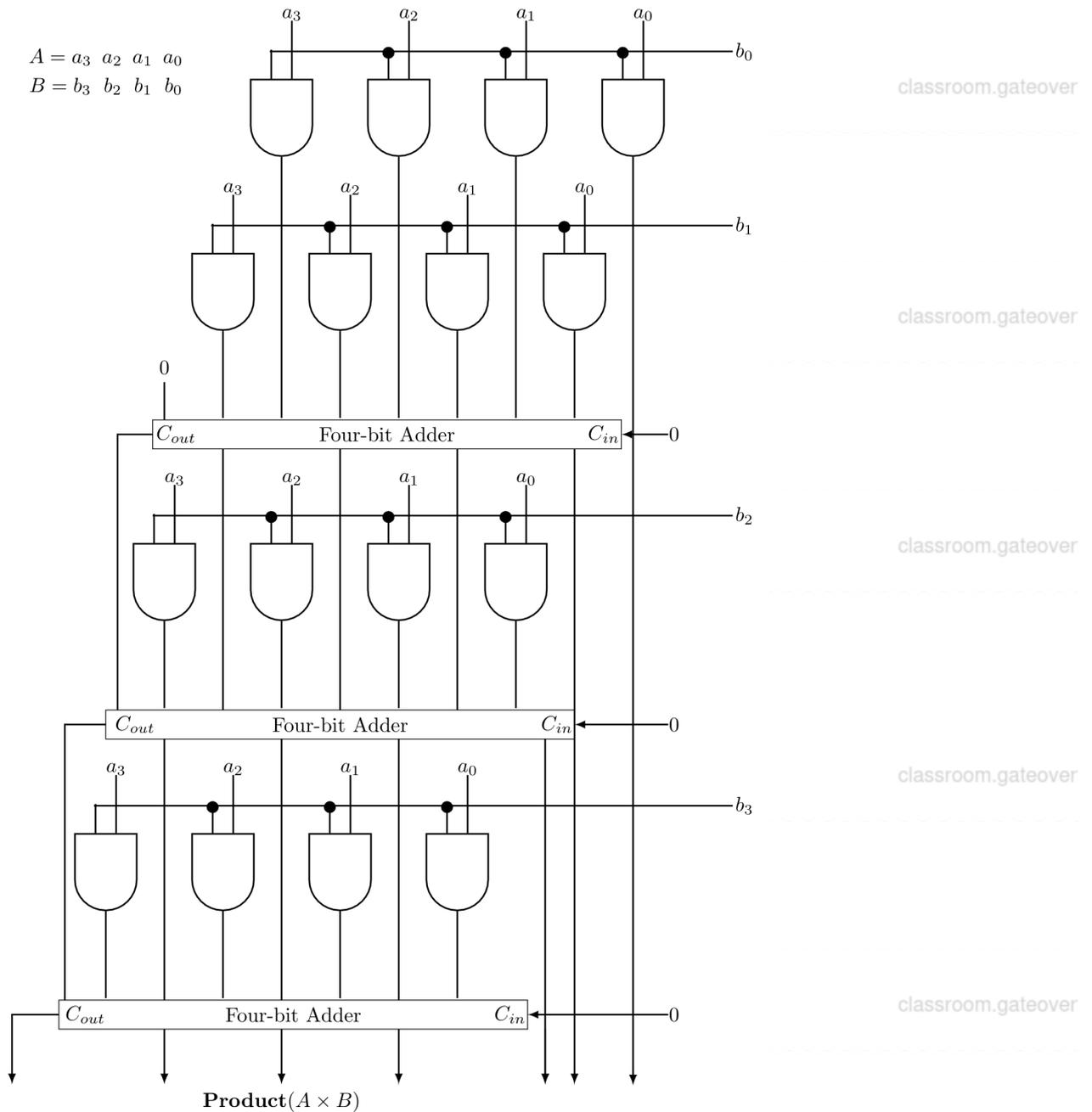
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Total delay in $N \times M$ ($N \geq M$) array multiplier due to AND gate in partial products at all level is just 1 unit AND gate delay as the operation is done parallel wise at each step. Now delays at level 1 to $(M - 1) = (M - 1) \times$ delay due to 1 unit of $N - bit$ adder. Therefore the maximum gate delay is $O(M)$ but here $M = N \therefore O(N)$.

http://www.dauniv.ac.in/downloads/CArch_PPTs/CompArchCh03L06ArrayMult.pdf or [archive](#)

Refer this article page 16.

Correct Answer: B

References



23 votes

-- Riya Roy(Arayana) (5.3k points)



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				A3	A2	A1	A0	Inputs
			×	B3	B2	B1	B0	
			C	B0 × A3	B0 × A2	B0 × A1	B0 × A0	Internal Signals
	+			B1 × A3	B1 × A2	B1 × A1	B1 × A0	
		C	Sum	Sum	Sum	Sum		
	+			B2 × A3	B2 × A2	B2 × A1	B2 × A0	
		C	Sum	Sum	Sum	Sum		
	+			B3 × A3	B3 × A2	B3 × A1	B3 × A0	Outputs
		C	Sum	Sum	Sum	Sum		
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	

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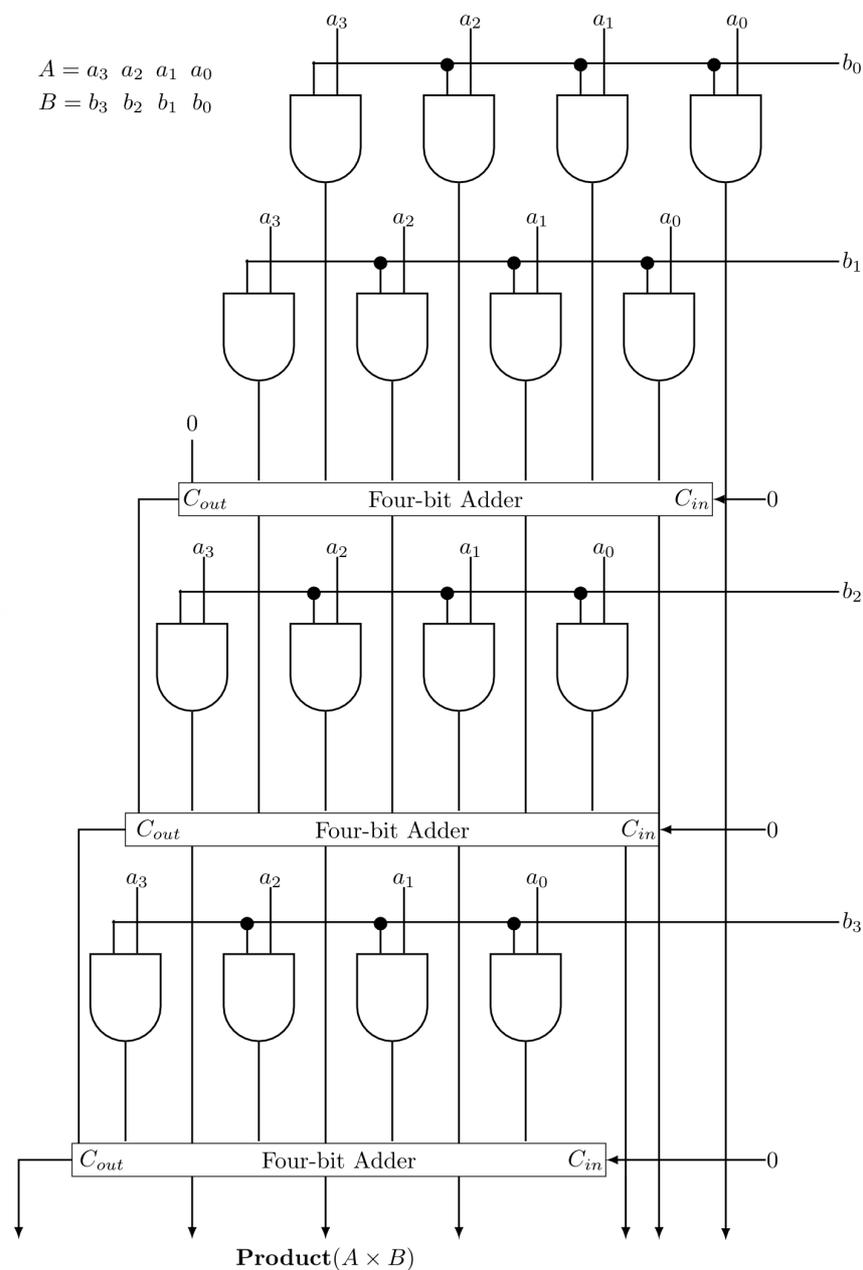
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Now to MULTIPLY these two Numbers:

1. 4 AND GATES REQUIRED B_0 MULTIPLY WITH $A_3 \ A_2 \ A_1 \ A_0$.
2. 4 AND GATES REQUIRED B_1 MULTIPLY WITH $A_3 \ A_2 \ A_1 \ A_0$.
3. 4 BIT ADDER
4. 4 AND GATES REQUIRED B_2 MULTIPLY WITH $A_3 \ A_2 \ A_1 \ A_0$.
5. 4 BIT ADDER
6. 4 AND GATES REQUIRED B_3 MULTIPLY WITH $A_3 \ A_2 \ A_1 \ A_0$.
7. 4 BIT ADDER

For 4 bits, Total Delay = $3 + 4 = 7$

For n bits, Total Delay = $n - 1 + n = 2n - 1$

So, Total Delay = $\Theta(n)$.

Correct Answer: C

👍 52 votes

-- Vidhi Sethi (8.3k points)



Consider numbers represented in 4-bit Gray code. Let $h_3h_2h_1h_0$ be the Gray code representation of a number n and let $g_3g_2g_1g_0$ be the Gray code of $(n + 1) \pmod{16}$ value of the number. Which one of the following functions is correct?

- A. $g_0(h_3h_2h_1h_0) = \sum(1, 2, 3, 6, 10, 13, 14, 15)$
 B. $g_1(h_3h_2h_1h_0) = \sum(4, 9, 10, 11, 12, 13, 14, 15)$
 C. $g_2(h_3h_2h_1h_0) = \sum(2, 4, 5, 6, 7, 12, 13, 15)$
 D. $g_3(h_3h_2h_1h_0) = \sum(0, 1, 6, 7, 10, 11, 12, 13)$

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gate2006-cse digital-logic number-representation binary-codes normal

Answer



Consider the binary code that consists of only four valid codewords as given below:

00000, 01011, 10101, 11110

Let the minimum Hamming distance of the code p and the maximum number of erroneous bits that can be corrected by the code be q . Then the values of p and q are

- A. $p = 3$ and $q = 1$
 B. $p = 3$ and $q = 2$
 C. $p = 4$ and $q = 1$
 D. $p = 4$ and $q = 2$

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gate2017-cse-set2 digital-logic binary-codes

Answer

Answers: Binary Codes



✓ The answer is C.

Decimal n	Binary n	H(x) = Gray(n)	G(x) = Gray[(n + 1) mod 16]
0	0000	0000(00)	0001
1	0001	0001(01)	0011
2	0010	0011(03)	0010
3	0011	0010(02)	0110
4	0100	0110(06)	0111
5	0101	0111(07)	0101
6	0110	0101(05)	0100
7	0111	0100(04)	1100
8	1000	1100(12)	1101
9	1001	1101(13)	1111
10	1010	1111(15)	1110
11	1011	1110(14)	1010
12	1100	1010(10)	1011
13	1101	1011(11)	1001
14	1110	1001(09)	1000
15	1111	1000(08)	0000

We need to map min terms of $g_3g_2g_1g_0$ with respect to $h_3h_2h_1h_0$.

Hence as highlighted g_2 matches with option C.

Edit :

We have to map $h(x)$ with $g(x)$. Mod 16 is used in $g(x)$ only because since we have 4 bits, the maximum possible no that can be represented is 15, so after 15 we shouldn't get 16 and go back to 0. that's why.

Now, mapping is simple. We just have to map such that $h(x) \rightarrow g(x + 1)$

This means if h represents gray code of 0 then g will represent the gray code of 1

If h represents the gray code of 1 then g will represent 2 and so on.

For the last number $h(15) \bmod 16$ actually comes into the picture which will make it represent as $g(0)$

So, drawing the table as mentioned above.

Now, write g as a function of f . Simply how we do minimization. See the minterms.

Be careful only in one thing here.

An example for 2 gray code representations is 0011 meaning 3 in decimal. So, if we select this row as a minterm (just an example) then we have selected 3 and not 2, means row numbers are not representing minterms. Rest everything is fine!

👍 66 votes

-- ryan sequeira (3k points)

4.3.2 Binary Codes: GATE CSE 2017 Set 2 | Question: 34 top

<https://gateoverflow.in/118376>



✓ 00000(**code1**), 01011(**code2**), 10101(**code3**), 11110 (**code4**)

Hamming distance = min of all hamming distances.

Which is 3 b/w (**code1**) and (**code2**) so,

$$p = 3$$

Now to correct d bit error we need hamming distance = $2d + 1$

So, $2d + 1 = 3$ will gives $d = 1$.

A is answer.

👍 41 votes

-- Prashant Singh (47.2k points)

4.4

Boolean Algebra (31) top

4.4.1 Boolean Algebra: GATE CSE 1987 | Question: 1-II top

<https://gateoverflow.in/80032>



The total number of Boolean functions which can be realised with four variables is:

- A. 4
- B. 17
- C. 256
- D. 65, 536

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gate1987 digital-logic boolean-algebra functions combinatory

Answer 🗨

4.4.2 Boolean Algebra: GATE CSE 1987 | Question: 12-a top

<https://gateoverflow.in/82556>



The Boolean expression $A \oplus B \oplus A$ is equivalent to

- A. $AB + \overline{A} \overline{B}$
- B. $\overline{A} B + A \overline{B}$
- C. B
- D. \overline{A}

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Answer 🗨

4.4.3 Boolean Algebra: GATE CSE 1988 | Question: 2-iii top

<https://gateoverflow.in/91679>



Let $*$ be defined as a Boolean operation given as $x * y = \overline{x} \overline{y} + xy$ and let $C = A * B$. If $C = 1$ then prove that $A = B$.

gate1988 digital-logic descriptive boolean-algebra

Answer 🗨

4.4.4 Boolean Algebra: GATE CSE 1989 | Question: 4-x top

<https://gateoverflow.in/88166>



A switching function is said to be neutral if the number of input combinations for which its value is 1 is equal to the number of

input combinations for which its value is 0. Compute the number of neutral switching functions of n variables (for a given n).

gate1989 descriptive digital-logic boolean-algebra

Answer 

4.4.5 Boolean Algebra: GATE CSE 1989 | Question: 5-a [top ⁵](#)

<https://gateoverflow.in/88230>



Find values of Boolean variables A, B, C which satisfy the following equations:

- $A + B = 1$
- $AC = BC$
- $A + C = 1$
- $AB = 0$

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Answer 

4.4.6 Boolean Algebra: GATE CSE 1992 | Question: 02-1 [top ⁵](#)

<https://gateoverflow.in/555>



The operation which is commutative but not associative is:

- A. AND
- B. OR
- C. EX-OR
- D. NAND

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gate1992 easy digital-logic boolean-algebra multiple-selects

Answer 

4.4.7 Boolean Algebra: GATE CSE 1994 | Question: 4 [top ⁵](#)

<https://gateoverflow.in/2500>



A. Let $*$ be a Boolean operation defined as $A * B = AB + \overline{A} \overline{B}$. If $C = A * B$ then evaluate and fill in the blanks:

- i. $A * A = \underline{\hspace{2cm}}$
- ii. $C * A = \underline{\hspace{2cm}}$

B. Solve the following boolean equations for the values of A, B and C :

$$AB + \overline{A}C = 1$$
$$AC + B = 0$$

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gate1994 digital-logic normal boolean-algebra descriptive

Answer 

4.4.8 Boolean Algebra: GATE CSE 1995 | Question: 2.5 [top ⁵](#)

<https://gateoverflow.in/2617>



What values of A, B, C and D satisfy the following simultaneous Boolean equations?

$$\overline{A} + AB = 0, AB = AC, AB + \overline{A}C + CD = \overline{C}D$$

- A. $A = 1, B = 0, C = 0, D = 1$
- B. $A = 1, B = 1, C = 0, D = 0$
- C. $A = 1, B = 0, C = 1, D = 1$
- D. $A = 1, B = 0, C = 0, D = 0$

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Answer 

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Let $*$ be defined as $x * y = \bar{x} + y$. Let $z = x * y$. Value of $z * x$ is

- A. $\bar{x} + y$
- B. x
- C. 0
- D. 1

gate1997 digital-logic normal boolean-algebra

Answer



What happens when a bit-string is XORed with itself n -times as shown:

$$[B \oplus (B \oplus (B \oplus (B \dots n \text{ times})))]$$

- A. complements when n is even
- B. complements when n is odd
- C. divides by 2^n always
- D. remains unchanged when n is even

gate1998 digital-logic normal boolean-algebra

Answer



Which of the following operations is commutative but not associative?

- A. AND
- B. OR
- C. NAND
- D. EXOR

gate1998 digital-logic easy boolean-algebra

Answer



Which of the following expressions is not equivalent to \bar{x} ?

- A. $x \text{ NAND } x$
- B. $x \text{ NOR } x$
- C. $x \text{ NAND } 1$
- D. $x \text{ NOR } 1$

gate1999 digital-logic easy boolean-algebra

Answer



The simultaneous equations on the Boolean variables x, y, z and w ,

- $x + y + z = 1$
- $xy = 0$
- $xz + w = 1$
- $xy + \bar{z}\bar{w} = 0$

have the following solution for x, y, z and w , respectively:

- A. 0 1 0 0

- B. 1 1 0 1
- C. 1 0 1 1
- D. 1 0 0 0

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Answer

4.4.14 Boolean Algebra: GATE CSE 2002 | Question: 2-3 top

https://gateoverflow.in/833



Let $f(A, B) = A' + B$. Simplified expression for function $f(f(x + y, y), z)$ is

- A. $x' + z$
- B. xyz
- C. $xy' + z$
- D. None of the above

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Answer

4.4.15 Boolean Algebra: GATE CSE 2004 | Question: 17 top

https://gateoverflow.in/1014



A Boolean function $x'y' + xy + x'y$ is equivalent to

- A. $x' + y'$
- B. $x + y$
- C. $x + y'$
- D. $x' + y$

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gate2004-cse digital-logic easy boolean-algebra

Answer

4.4.16 Boolean Algebra: GATE CSE 2007 | Question: 32 top

https://gateoverflow.in/1230



Let $f(w, x, y, z) = \sum(0, 4, 5, 7, 8, 9, 13, 15)$. Which of the following expressions are NOT equivalent to f ?

P: $x'y'z' + w'xy' + wy'z + xz$

Q: $w'y'z' + wx'y' + xz$

R: $w'y'z' + wx'y' + xyz + xy'z$

S: $x'y'z' + wx'y' + w'y$

- A. P only
- B. Q and S
- C. R and S
- D. S only

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Answer

4.4.17 Boolean Algebra: GATE CSE 2007 | Question: 33 top

https://gateoverflow.in/1231



Define the connective $*$ for the Boolean variables X and Y as:

$$X * Y = XY + X'Y'$$

Let $Z = X * Y$. Consider the following expressions P , Q and R .

$$P: X = Y * Z, Q: Y = X * Z, R: X * Y * Z = 1$$

Which of the following is **TRUE**?

- A. Only P and Q are valid.

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- B. Only Q and R are valid.
- C. Only P and R are valid.
- D. All P, Q, R are valid.

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Answer

4.4.18 Boolean Algebra: GATE CSE 2008 | Question: 26

https://gateoverflow.in/424



If P, Q, R are Boolean variables, then

$(P + \bar{Q})(P \cdot \bar{Q} + P \cdot R)(\bar{P} \cdot \bar{R} + \bar{Q})$ simplifies to

- A. $P \cdot \bar{Q}$
- B. $P \cdot \bar{R}$
- C. $P \cdot \bar{Q} + R$
- D. $P \cdot \bar{R} + Q$

gate2008-cse easy digital-logic boolean-algebra

Answer

4.4.19 Boolean Algebra: GATE CSE 2012 | Question: 6

https://gateoverflow.in/38



The truth table represents the Boolean function

X	Y	(X,Y)
0	0	0
0	1	0
1	0	1
1	1	1

- A. X
- B. $X + Y$
- C. $X \oplus Y$
- D. Y

gate2012-cse digital-logic easy boolean-algebra

Answer

4.4.20 Boolean Algebra: GATE CSE 2013 | Question: 21

https://gateoverflow.in/1532



Which one of the following expressions does **NOT** represent exclusive NOR of x and y ?

- A. $xy + x'y'$
- B. $x \oplus y'$
- C. $x' \oplus y$
- D. $x' \oplus y'$

gate2013-cse digital-logic easy boolean-algebra

Answer

4.4.21 Boolean Algebra: GATE CSE 2014 Set 3 | Question: 55

https://gateoverflow.in/2090



Let \oplus denote the exclusive OR (XOR) operation. Let '1' and '0' denote the binary constants. Consider the following Boolean expression for F over two variables P and Q :

$$F(P, Q) = ((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$$

The equivalent expression for F is

- A. $P + Q$

- B. $\overline{P+Q}$
- C. $\overline{P\oplus Q}$
- D. $\overline{P\oplus Q}$

gate2014-cse-set3 digital-logic normal boolean-algebra

Answer 

4.4.22 Boolean Algebra: GATE CSE 2015 Set 1 | Question: 39 [top](#)

<https://gateoverflow.in/8294>



Consider the operations

$$f(X, Y, Z) = X'YZ + XY' + Y'Z' \text{ and } g(X, Y, Z) = X'YZ + X'YZ' + XY$$

Which one of the following is correct?

- A. Both $\{f\}$ and $\{g\}$ are functionally complete
- B. Only $\{f\}$ is functionally complete
- C. Only $\{g\}$ is functionally complete
- D. Neither $\{f\}$ nor $\{g\}$ is functionally complete

gate2015-cse-set1 boolean-algebra difficult

Answer 

4.4.23 Boolean Algebra: GATE CSE 2015 Set 2 | Question: 37 [top](#)

<https://gateoverflow.in/8162>



The number of min-terms after minimizing the following Boolean expression is _____.

$$[D'+AB'+A'C+AC'D+A'C'D]'$$

gate2015-cse-set2 digital-logic boolean-algebra normal numerical-answers

Answer 

4.4.24 Boolean Algebra: GATE CSE 2016 Set 1 | Question: 06 [top](#)

<https://gateoverflow.in/39629>



Consider the Boolean operator # with the following properties :

$x\#0=x$, $x\#1=\bar{x}$, $x\#x=0$ and $x\#\bar{x}=1$. Then $x\#y$ is equivalent to

- A. $x\bar{y} + \bar{x}y$
- B. $x\bar{y} + \bar{x}\bar{y}$
- C. $xy + x\bar{y}$
- D. $xy + \bar{x}\bar{y}$

gate2016-cse-set1 digital-logic boolean-algebra easy

Answer 

4.4.25 Boolean Algebra: GATE CSE 2016 Set 2 | Question: 08 [top](#)

<https://gateoverflow.in/39540>



Let, $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 0$ where x_1, x_2, x_3, x_4 are Boolean variables, and \oplus is the XOR operator.

Which one of the following must always be TRUE?

- A. $x_1x_2x_3x_4 = 0$
- B. $x_1x_3 + x_2 = 0$
- C. $\bar{x}_1 \oplus \bar{x}_3 = \bar{x}_2 \oplus \bar{x}_4$
- D. $x_1 + x_2 + x_3 + x_4 = 0$

gate2016-cse-set2 digital-logic boolean-algebra normal

Answer 



If w, x, y, z are Boolean variables, then which one of the following is INCORRECT?

- A. $wx + w(x + y) + x(x + y) = x + wy$
- B. $w\bar{x}(y + \bar{z}) + \bar{w}x = \bar{w} + x + \bar{y}z$
- C. $(w\bar{x}(y + x\bar{z}) + \bar{w}\bar{x})y = x\bar{y}$
- D. $(w + y)(wxy + wyz) = wxy + wyz$

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normal

Answer



Let \oplus and \odot denote the Exclusive OR and Exclusive NOR operations, respectively. Which one of the following is NOT CORRECT?

- A. $\overline{P \oplus Q} = P \odot Q$
- B. $\overline{\overline{P \oplus Q}} = P \odot Q$
- C. $\overline{P \oplus Q} = P \oplus Q$
- D. $P \oplus \overline{P \oplus Q} = (P \odot \overline{P \odot Q})$

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Answer



Which one of the following is NOT a valid identity?

- A. $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
- B. $(x + y) \oplus z = x \oplus (y + z)$
- C. $x \oplus y = x + y$, if $xy = 0$
- D. $x \oplus y = (xy + x'y)'$

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digital-logic

boolean-algebra

Answer



Consider the following Boolean expression.

$$F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$$

Which of the following Boolean expressions is/are equivalent to \bar{F} (complement of F)?

- A. $(\bar{X} + \bar{Y} + \bar{Z})(X + \bar{Y})(Y + \bar{Z})$
- B. $X\bar{Y} + \bar{Z}$
- C. $(X + \bar{Z})(\bar{Y} + \bar{Z})$
- D. $X\bar{Y} + Y\bar{Z} + X\bar{Y}\bar{Z}$

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gate2021-cse-set1

multiple-selects

digital-logic

boolean-algebra

Answer



The function $A\bar{B}C + \bar{A}BC + AB\bar{C} + \bar{A}\bar{B}C + A\bar{B}\bar{C}$ is equivalent to

- A. $A\bar{C} + AB + \bar{A}C$
- B. $A\bar{B} + A\bar{C} + \bar{A}C$

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- C. $\bar{A}B + A\bar{C} + A\bar{B}$
 D. $\bar{A}B + AC + A\bar{B}$

gate2004-it digital-logic boolean-algebra easy

Answer

4.4.31 Boolean Algebra: GATE IT 2005 | Question: 7

https://gateoverflow.in/3752



Which of the following expressions is equivalent to $(A \oplus B) \oplus C$

- A. $(A + B + C)(\bar{A} + \bar{B} + \bar{C})$
 B. $(A + B + C)(\bar{A} + \bar{B} + C)$
 C. $ABC + \bar{A}(B \oplus C) + \bar{B}(A \oplus C)$
 D. None of these

gate2005-it digital-logic normal boolean-algebra

Answer

Answers: Boolean Algebra

4.4.1 Boolean Algebra: GATE CSE 1987 | Question: 1-II

https://gateoverflow.in/80032



✓ A **Boolean function** of 4 variables is a function from a set of $2^4 = 16$ elements (all combinations of 4 variables) to a set of $2(\{0, 1\})$ elements. So, number of such functions will be $2^{16} = 65,536$

Correct Answer: D

References



26 votes

-- Prashant Singh (47.2k points)

4.4.2 Boolean Algebra: GATE CSE 1987 | Question: 12-a

https://gateoverflow.in/82556



✓ Option (C)

$$A \oplus A = 0 \text{ and } 0 \oplus A = A$$

$$A \oplus B \oplus A = (A \oplus A) \oplus B = 0 \oplus B = B$$

25 votes

-- Prajwal Bhat (7.6k points)

4.4.3 Boolean Algebra: GATE CSE 1988 | Question: 2-iii

https://gateoverflow.in/91679



✓ $C = A * B$

$$\Rightarrow C = \bar{A} \bar{B} + AB$$

$$\Rightarrow C = \overline{A \text{ XOR } B}$$

$$\Rightarrow C = A \text{ XNOR } B$$

Truth table is:

A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

When $C = 1$, observing the truth table we can say $A = B$.

👍 16 votes

-- Arnab Bhadra (3.7k points)

4.4.4 Boolean Algebra: GATE CSE 1989 | Question: 4-x [top ⤴](#)

<https://gateoverflow.in/88166>



For an 'n' variable function, total number of possible minterms(input combinations) will be 2^n . Half of them will be one i.e., 2^{n-1} .

Thus total number of neutral functions possible = Choosing any 2^{n-1} combinations to be 1 out of 2^n combination. i.e. $\binom{2^n}{2^{n-1}}$.

👍 17 votes

-- Jeeten (95 points)

4.4.5 Boolean Algebra: GATE CSE 1989 | Question: 5-a [top ⤴](#)

<https://gateoverflow.in/88230>



✓ From $A + B = 1$ and $AB = 0$ we get either of A, B is 1 and another is 0

Now, $AC = BC$, here C has to be 0 (because A, B has different values)

$$C = 0$$

$$\text{Now, } A + C = 1$$

$$\text{So, } A = 1 \text{ and } AB = 0 \text{ so, } B = 0$$

So, we get:

$$A = 1, B = 0, C = 0$$

These are the values.

👍 21 votes

-- Aboveallplayer (12.5k points)

4.4.6 Boolean Algebra: GATE CSE 1992 | Question: 02-i [top ⤴](#)

<https://gateoverflow.in/555>



✓ The answer is D.

Remark:

1. Every logic gate follows Commutative law.
2. AND, OR, Ex-OR, EX-NOR follows Associative law also. NAND, NOR doesn't follow Associative law.

👍 31 votes

-- Ankit Rokde (6.9k points)

4.4.7 Boolean Algebra: GATE CSE 1994 | Question: 4 [top ⤴](#)

<https://gateoverflow.in/2500>



✓

A.

i. $A * A = AA + A'A' = A + A' = 1$

ii. $C * A = (A * B) * A = (AB + A'B') * A = (AB + A'B')A + (AB + A'B')'A'$
 $= (AB + A'B')A + (A'B + AB')A' = AB + 0 + A'B + 0 = B.$

B. $AB + A'C = 1, AC + B = 0$

$\implies AC + B = 0$, means both $B = 0$ and $AC = 0$

$$\implies AB + A'C = 1$$

$$\implies A'C = 1 \quad [\because B = 0, AB = 0]$$

So, $C = 1$ and $A = 0$

$A = 0, B = 0$ and $C = 1$

👍 27 votes

-- Praveen Saini (41.9k points)

4.4.8 Boolean Algebra: GATE CSE 1995 | Question: 2.5 top b

<https://gateoverflow.in/2617>



✓ $A' + AB = 0 \implies A' + B = 0$

$\therefore A' = 0$ and $B = 0$

$A = 1$

$$AB = AC \implies B = C \implies C = 0$$

$$AB + AC' + CD = C'D$$

$$\implies 0 + 1 + 0 = D$$

$$\implies D = 1$$

Correct Answer: A

👍 16 votes

-- Sutanay Bhattacharjee (3.1k points)

4.4.9 Boolean Algebra: GATE CSE 1997 | Question: 2-1 top b

<https://gateoverflow.in/2227>



✓ Answer is option B.

$$z * x = (x * y) * x$$

$$= (\bar{x} + y) * x$$

$$= \bar{x} + y + x$$

$$x. \bar{y} + x = x$$

👍 29 votes

-- Arjun Suresh (332k points)

4.4.10 Boolean Algebra: GATE CSE 1998 | Question: 1.13 top b

<https://gateoverflow.in/1680>



✓ It should be (D).

Let number of \oplus be two (even case):

$$B \oplus B \oplus B = B \oplus 0 = B \text{ (remains unchanged)}$$

Let number of \oplus be three (odd case):

$$B \oplus B \oplus B \oplus B = B \oplus B \oplus 0 = B \oplus B = 0 \text{ (gives 0)}$$

👍 37 votes

-- Rajarshi Sarkar (27.9k points)

4.4.11 Boolean Algebra: GATE CSE 1998 | Question: 2.8 top b

<https://gateoverflow.in/1680>



✓ We all know AND, OR are both associative and commutative. we don't know about EXOR and NAND

We can consume some time and prove it by truth table..and come up with the results that EXOR is also associative and commutative so the only left out is NAND its commutative but not associative

Correct Answer: C

👍 17 votes

-- Bhagirathi Nayak (11.7k points)

4.4.12 Boolean Algebra: GATE CSE 1999 | Question: 1.7 top

<https://gateoverflow.in/1460>



✓

- A. $\overline{xx} = \bar{x}$
- B. $\overline{x+x} = \bar{x}, \bar{x} = \bar{x}$
- C. $\overline{x.1} = \bar{x} + 0 = \bar{x}$
- D. $\overline{x+1} = \bar{x}.0 = 0$

Here, $x \text{ NOR } 1$ will not be equal to \bar{x} .

Hence, option (D) $x \text{ NOR } 1$.

👍 11 votes

-- Leen Sharma (28.7k points)

4.4.13 Boolean Algebra: GATE CSE 2000 | Question: 2.10 top

<https://gateoverflow.in/657>



✓

Take each option one by one and try to put the values of x, y, z and w in question:

1.

- $0 + 1 + 0 = 1$
- $0.1 = 0$
- $0.0 + 0 = 0$ (went wrong) So, this is not the right option

2.

- $1 + 1 + 0 = 1$
- $1.1 = 1$ (went wrong) not right

3.

- $1 + 0 + 1 = 1$
- $1.0 = 0$
- $1.1 + 1 = 1$
- $1.0 + 1.0 = 0$ This is the right option

Correct Answer: C

👍 31 votes

-- shekhar chauhan (32.8k points)

4.4.14 Boolean Algebra: GATE CSE 2002 | Question: 2-3 top

<https://gateoverflow.in/833>



✓

$$\begin{aligned} f(f(x+y, y), z) &= f((x+y)' + y), z) \\ &= ((x+y)' + y)' + z \\ &= (x+y).y' + z (\because (a+b)' = a'.b') \\ &= xy' + z \end{aligned}$$

Correct Answer: C

👍 30 votes

-- Arjun Suresh (332k points)

4.4.15 Boolean Algebra: GATE CSE 2004 | Question: 17 top

<https://gateoverflow.in/1014>



✓

Answer is **option D**.

$$\begin{aligned} x'y' + x'y &= x'(y+y') = x' \\ x' + xy &= x' + y \end{aligned}$$



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	wx	00	01	11	10
yz	00	1	1		1
	01		1	1	1
	11		1	1	
	10				

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K-map

So, minimized expression will be

$xz + w'y'z' + wx'y'$ which is Q. From the K-map, we can also get P and R. So, only S is NOT equivalent to f .

http://www.eecs.berkeley.edu/~newton/Classes/CS150sp98/lectures/week4_2/sld011.htm

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Alternatively,

Go with Minterm representation of each option, (Note that order of W, X, Y, Z should be preserved.)

Here, x means do not care (x takes value either 0 or 1)

$$\begin{aligned}
 P &: X'Y'Z' + W'XY' + WY'Z + XZ \\
 &= xX'Y'Z' + W'XY'x + WxY'Z + xXxZ \\
 &= x000 + 010x + 1x01 + x1x1 \\
 &= 0000 + 1000 + 0100 + 0101 + 1001 + 1101 + 0101 + 0111 + 1101 + 1111 \\
 &= 0 + 8 + 4 + 5 + 9 + 13 + 5 + 7 + 13 + 15 \\
 &= \sum m(0, 4, 5, 7, 8, 9, 13, 15)
 \end{aligned}$$

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$$\begin{aligned}
 Q &: W'Y'Z' + WX'Y' + XZ \\
 &= W'xY'Z' + WX'Y'x + xXxZ \\
 &= 0x00 + 100x + x1x1 \\
 &= 0000 + 0100 + 1000 + 1001 + 0101 + 0111 + 1101 + 1111 \\
 &= 0 + 4 + 8 + 9 + 5 + 7 + 13 + 15 \\
 &= \sum m(0, 4, 5, 7, 8, 9, 13, 15)
 \end{aligned}$$

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$$\begin{aligned}
 R &: W'Y'Z' + WX'Y' + XYZ + XY'Z \\
 &= W'xY'Z' + WX'Y'x + xXYZ + xXY'Z \\
 &= 0x00 + 100x + x111 + x101 \\
 &= 0000 + 0100 + 1000 + 1001 + 0111 + 1111 + 0101 + 1101 \\
 &= 0 + 4 + 8 + 9 + 7 + 15 + 5 + 13 \\
 &= \sum m(0, 4, 5, 7, 8, 9, 13, 15)
 \end{aligned}$$

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$$\begin{aligned}
 S &: X'Y'Z' + WX'Y' + W'Y \\
 &= xX'Y'Z' + WX'Y'x + W'xYx \\
 &= x000 + 100x + 0x1x \\
 &= 0000 + 1000 + 1000 + 1001 + 0010 + 0011 + 0110 + 0111 \\
 &= 0 + 8 + 8 + 9 + 2 + 3 + 6 + 7 \\
 &= \sum m(0, 2, 3, 6, 7, 8, 9)
 \end{aligned}$$

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Correct Answer: D

References

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42 votes

-- Arjun Suresh (332k points)

4.4.17 Boolean Algebra: GATE CSE 2007 | Question: 33 top

<https://gateoverflow.in/1231>

✓ P:

$$\begin{aligned}
Y * Z &= Y * (X * Y) \\
&= Y * (XY + X'Y') \\
&= Y(XY + X'Y') + Y'(XY + X'Y') \\
&= XY + Y'((X' + Y')(X + Y)) \\
&= XY + Y'(X'Y + XY') \\
&= XY + XY' \\
&= X(Y + Y') \\
&= X
\end{aligned}$$

So, P is valid.

Q:

$$\begin{aligned}
X * Z &= X * (X * Y) \\
&= X * (XY + X'Y') \\
&= X(XY + X'Y') + X'(XY + X'Y') \\
&= XY + X'((X' + Y')(X + Y)) \\
&= XY + X'(X'Y + XY') \\
&= XY + X'Y \\
&= Y(X + X') \\
&= Y
\end{aligned}$$

So, Q is also valid.

R:

$$\begin{aligned}
X * Y * Z &= (X * Y) * (X * Y) \\
&= (XY + X'Y') * (XY + X'Y') \\
&= (XY + X'Y')(XY + X'Y') + (XY + X'Y')'(XY + X'Y') \\
&= (XY + X'Y') + (XY + X'Y')' (\because AA = A) \\
&= 1 (\because A + A' = 1)
\end{aligned}$$

So, R is also valid.

Hence, D choice.

42 votes

-- Arjun Suresh (332k points)

4.4.18 Boolean Algebra: GATE CSE 2008 | Question: 26 top

<https://gateoverflow.in/424>✓ Ans is (A) $P\bar{Q}$

$$\begin{aligned}
&(P + \bar{Q})(P\bar{Q} + PR)(\bar{P}\bar{R} + \bar{Q}) \\
&= (PP\bar{Q} + PPR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q}) \\
&= (P\bar{Q} + PR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q}) \\
&= P\bar{Q} + P\bar{Q}R \\
&= P\bar{Q}
\end{aligned}$$

41 votes

-- Keith Kr (4.5k points)

4.4.19 Boolean Algebra: GATE CSE 2012 | Question: 6 top

https://gateoverflow.in/38



✓ Whenever X is true (X, Y) is true and whenever X is false (X, Y) is false, so the answer is (A) X .

39 votes

-- Omesh Pandita (1.9k points)

4.4.20 Boolean Algebra: GATE CSE 2013 | Question: 21 top

https://gateoverflow.in/1532



✓ A : means both are either true OR both are false. then it will be true = ExNOR

B & C : whenever any one of the literal is complemented then ExOR can be turned to ExNOR and complement sign on the literal can be removed. So these two also represents ExNOR operation of x and y .

Answer is option D. It is the ExOR operation b/w the two.

29 votes

-- Amar Vashishth (25.2k points)

4.4.21 Boolean Algebra: GATE CSE 2014 Set 3 | Question: 55 top

https://gateoverflow.in/2090



✓ XOR is associative and commutative. Also, $A \oplus A = 0$ and $A \oplus 1 = \bar{A}$ and $A \oplus 0 = A$. So
 $((1 \oplus P) \oplus (P \oplus Q)) \oplus ((P \oplus Q) \oplus (Q \oplus 0))$
 $\implies (1 \oplus P) \oplus ((P \oplus Q) \oplus (P \oplus Q)) \oplus (Q \oplus 0)$
 $\implies (1 \oplus 0) \oplus (P \oplus Q)$
 $\implies 1 \oplus (P \oplus Q)$
 $\implies (P \oplus Q)$

Correct Answer: D

40 votes

-- Arjun Suresh (332k points)

4.4.22 Boolean Algebra: GATE CSE 2015 Set 1 | Question: 39 top

https://gateoverflow.in/8294



✓ g is preserving 0 as when all inputs are zero, output is always 0 and so g cannot be functionally complete.

f is not preserving 0.

f is not preserving 1. (when all inputs are 1, output is 0).

f is not linear as in XY' only one (odd) input ($X = 1, Y = Z = 0$) needs to be 1 and in $X'YZ$ two inputs (even) ($X = 0, Y = Z = 1$) need to be 1.

f is not monotone as changing Y from 0 to 1, can take f from 1 to 0.

f is not self dual as $f(X, Y, Z) \neq \neg f(\neg X, \neg Y, \neg Z)$

So, f satisfies all 5 conditions required for functional completeness.

Hence, B is the answer.

<http://cs.ucsb.edu/~victor/ta/cs40/posts-criterion.pdf>

References



93 votes

-- Arjun Suresh (332k points)

4.4.23 Boolean Algebra: GATE CSE 2015 Set 2 | Question: 37 top

https://gateoverflow.in/8162



✓ $F = [D' + AB' + A'C + AC'D + A'C'D]'$

$F' = D' + AB' + A'C + AC'D + A'C'D$

Now we have F' , so fill 0's (maxterms) in K-map for each term

As for **D'**

CD \ AB	00	01	11	10
00	0			0
01	0			0
11	0			0
10	0			0

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Similarly for AB' , $A'C$, $AC'D$ and $A'C'D$. We will get

CD \ AB	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	0	0		0
10	0	0	0	0

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We get one place for minterm and that is **ABCD**

👍 62 votes

-- Praveen Saini (41.9k points)

4.4.24 Boolean Algebra: GATE CSE 2016 Set 1 | Question: 06 [top](#)

<https://gateoverflow.in/39529>



✓ These are properties of XOR function.. so answer is A) $x\bar{y} + \bar{x}y$

👍 35 votes

-- Abhilash Panicker (7.6k points)

4.4.25 Boolean Algebra: GATE CSE 2016 Set 2 | Question: 08 [top](#)

<https://gateoverflow.in/39540>



✓ Let $x_1 = 1$ $x_2 = 1$ $x_3 = 1$ and $x_4 = 1$

such that $x_1 \oplus x_2 \oplus x_3 \oplus x_4 = 1 \oplus 1 \oplus 1 \oplus 1 = 0$

- A. $x_1 x_2 x_3 x_4 = 1.1.1.1 = 1$, False
- B. $x_1 x_3 + x_2 = 1.1 + 1 = 1$, False
- C. is always True.
- D. $x_1 + x_2 + x_3 + x_4 = 1 + 1 + 1 + 1 = 1$, False

Correct Answer: C

👍 61 votes

-- Praveen Saini (41.9k points)

4.4.26 Boolean Algebra: GATE CSE 2017 Set 2 | Question: 27 [top](#)

<https://gateoverflow.in/118494>



✓ Let us try to simplify (minimize) the expression given in each option

Option - A: $wx + w(x + y) + x(x + y) = x + wy$

$wx + wx + wy + x$

$$wx + wy + x$$

$$x(1 + w) + wy$$

$$x + wy$$

Option - B: $w\bar{x}(y + \bar{z}) + \bar{w}x = \bar{w} + x + \bar{y}z$

$$\overline{w\bar{x} + (y + \bar{z})} + \bar{w}x$$

$$\bar{w} + x + \bar{y}z + \bar{w}x$$

$$\bar{w} + \bar{w}x + x + \bar{y}z$$

$$\bar{w} + x + \bar{y}z$$

Option - D: $(w + y)(wxy + wyz) = wxy + wyz$

$$wxy + wyz + wxy + wyz$$

$$wxy + wyz$$

Option A, B, D are matching fine.

Hence, **Option - C** is the answer

👍 29 votes

-- Arunav Khare (3.9k points)

4.4.27 Boolean Algebra: GATE CSE 2018 | Question: 4 top

<https://gateoverflow.in/204078>



✓ Consider *Option(D)*. LHS can be simplified as,

$$(P \oplus \bar{P}) \oplus Q = 1 \oplus Q = \bar{Q}$$

Similarly, for RHS

$$(P \odot \bar{P}) \odot \bar{Q} = 0 \odot \bar{Q} = Q$$

$LHS \neq RHS$ therefore, **Option (D)** is the correct answer.

Other options can be simplified as follows.

1. $\overline{P \oplus Q} = \overline{PQ + \bar{P}\bar{Q}} = (\overline{PQ}) (\overline{\bar{P}\bar{Q}}) = (\bar{P} + Q) (P + \bar{Q}) = PQ + \bar{P}\bar{Q} = P \odot Q$
2. $\bar{P} \oplus Q = (\bar{P})\bar{Q} + (\bar{P})Q = PQ + \bar{P}\bar{Q} = P \odot Q$
3. $\bar{P} \oplus \bar{Q} = (\bar{P})(\bar{Q}) + (\bar{P})(Q) = \bar{P}\bar{Q} + P\bar{Q} = P \oplus Q$

👍 18 votes

-- Prateek Dwivedi (3.5k points)

4.4.28 Boolean Algebra: GATE CSE 2019 | Question: 6 top

<https://gateoverflow.in/302842>



- ✓ XOR is associative so $(x \oplus y) \oplus z = x \oplus (y \oplus z)$
- 2. For 2 input, XOR and $XNOR$ are complement to each other i.e. $x \oplus y = (xy + x'y)'$
- 3. $x \oplus y = x + y$ if $xy = 0$

Only false statement is option B.

👍 26 votes

-- Digvijay (44.9k points)

4.4.29 Boolean Algebra: GATE CSE 2021 Set 1 | Question: 42 top

<https://gateoverflow.in/357409>



✓ $F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$

Taking complement of above expression;

$$\bar{F} = \overline{(X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)}$$

Applying De-Morgan's law;

$$\bar{F} = \overline{(X + Y + Z)} + \overline{(\bar{X} + Y)} + \overline{(\bar{Y} + Z)}$$

$$\bar{F} = (\bar{X} \cdot \bar{Y} \cdot \bar{Z}) + \bar{X} \cdot \bar{Y} + \bar{Y} \cdot \bar{Z}$$

$$\left[\because \bar{\bar{X}} = X, \text{ Using double negation law} \right]$$

$$\therefore \bar{F} = (\bar{X} \cdot \bar{Y} \cdot \bar{Z}) + (X \cdot \bar{Y}) + (Y \cdot \bar{Z}) \rightarrow \text{Option (D)}$$

Taking \bar{Y} as common we get;

$$\bar{F} = \bar{Y} [(\bar{X}\bar{Z}) + X] + Y\bar{Z}$$

$\because A + BC = (A + B)(A + C)$ Applying distributive law here]

$$\bar{F} = \bar{Y} [(X + \bar{X})(X + \bar{Z})] + Y\bar{Z}$$

$$\bar{F} = \bar{Y} [X + \bar{Z}] + Y\bar{Z}$$

$$\bar{F} = X\bar{Y} + \bar{Y}\bar{Z} + Y\bar{Z}$$

Taking \bar{Z} as common

$$\bar{F} = X\bar{Y} + \bar{Z}(Y + \bar{Y})$$

$\because (Y + \bar{Y}) = 1$ using complement law

$$\therefore \bar{F} = X\bar{Y} + \bar{Z} \rightarrow \text{Option (B)}$$

Applying distributive law here we get;

$$\bar{F} = (X + \bar{Z})(\bar{Y} + \bar{Z}) \rightarrow \text{Option (C)}$$

So, correct options are B, C, D.

Option A is false and can be proved as follows:

Take $X = 0, Y = 1, Z = 0$

Now, $F = 0$, since $(\bar{Y} + Z)$ term will be zero. So, \bar{F} must be 1.

But option A gives 0 as the term $X + \bar{Y}$ evaluates to 0. So, option A is not equal to \bar{F} .

[Properties of Boolean Algebra](#)

References



1 votes

-- Hira (14.1k points)

4.4.30 Boolean Algebra: GATE IT 2004 | Question: 44 [top](#)

<https://gateoverflow.in/3687>



✓

AB \ C	00	01	11	10
0			1	1
1	1	1		1

So, the equivalent expression will be $\bar{A}C + A\bar{C} + A\bar{B}$

(B) option

36 votes

-- Arjun Suresh (332k points)

4.4.31 Boolean Algebra: GATE IT 2005 | Question: 7

<https://gateoverflow.in/3752>



✓ Correct answer is C

$$(A \oplus B) \oplus C$$

$$\text{At } C = 0, (A \oplus B) \oplus C = (A \oplus B) \text{ ---(I) [as } 0 \oplus x = 0 \cdot x' + 0 \cdot x = x \text{]}$$

$$\text{At } C = 0, ABC + A'(B \oplus C) + B'(A \oplus C)$$

$$= 0 + A'(B \oplus 0) + B'(A \oplus 0) = A'B + AB' = A \oplus B \text{ ----(II)}$$

$$\text{At } C = 1, (A \oplus B) \oplus C = (A \odot B) \text{ --- (III) [as } 1 \oplus x = 1 \cdot x' + 1 \cdot x = x' \text{]}$$

$$\text{At } C = 1, ABC + A'(B \oplus C) + B'(A \oplus C)$$

$$= AB + A'(B \oplus 1) + B'(A \oplus 1) = AB + A'B' = (A \odot B) \text{ --(IV)}$$

from eq (I), (II), (III) and (IV) it is clear

$$(A \oplus B) \oplus C = ABC + A'(B \oplus C) + B'(A \oplus C)$$

39 votes

-- Praveen Saini (41.9k points)

4.5

Booths Algorithm (6)

4.5.1 Booths Algorithm: GATE CSE 1990 | Question: 8b

<https://gateoverflow.in/85671>



State the Booth's algorithm for multiplication of two numbers. Draw a block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers.

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Answer

4.5.2 Booths Algorithm: GATE CSE 1996 | Question: 1.23

<https://gateoverflow.in/2727>



Booth's algorithm for integer multiplication gives worst performance when the multiplier pattern is

- A. 101010...1010
- B. 100000...0001
- C. 111111...1111
- D. 011111...1110

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Answer

4.5.3 Booths Algorithm: GATE CSE 1999 | Question: 1.20

<https://gateoverflow.in/1473>



Booth's coding in 8 bits for the decimal number -57 is:

- A. 0 - 100 + 1000
- B. 0 - 100 + 100 - 1
- C. 0 - 1 + 100 - 10 + 1
- D. 00 - 10 + 100 - 1

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Answer



Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as

- A. 0-100100-1
- B. 11000111
- C. 0-1001000
- D. 0100-1001

gate2005-it digital-logic booths-algorithm normal

Answer



When multiplicand Y is multiplied by multiplier $X = x_{n-1}x_{n-2} \dots x_0$ using bit-pair recoding in Booth's algorithm, partial products are generated according to the following table.

Row	x_{i+1}	x_i	x_{i-1}	Partial Product
1	0	0	0	0
2	0	0	1	Y
3	0	1	0	Y
4	0	1	1	$2Y$
5	1	0	0	?
6	1	0	1	$-Y$
7	1	1	0	$-Y$
8	1	1	1	?

The partial products for rows 5 and 8 are

- A. $2Y$ and Y
- B. $-2Y$ and $2Y$
- C. $-2Y$ and 0
- D. 0 and Y

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Answer



The two numbers given below are multiplied using the Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for the multiplication of the above two numbers?

- A. 6
- B. 8
- C. 10
- D. 12

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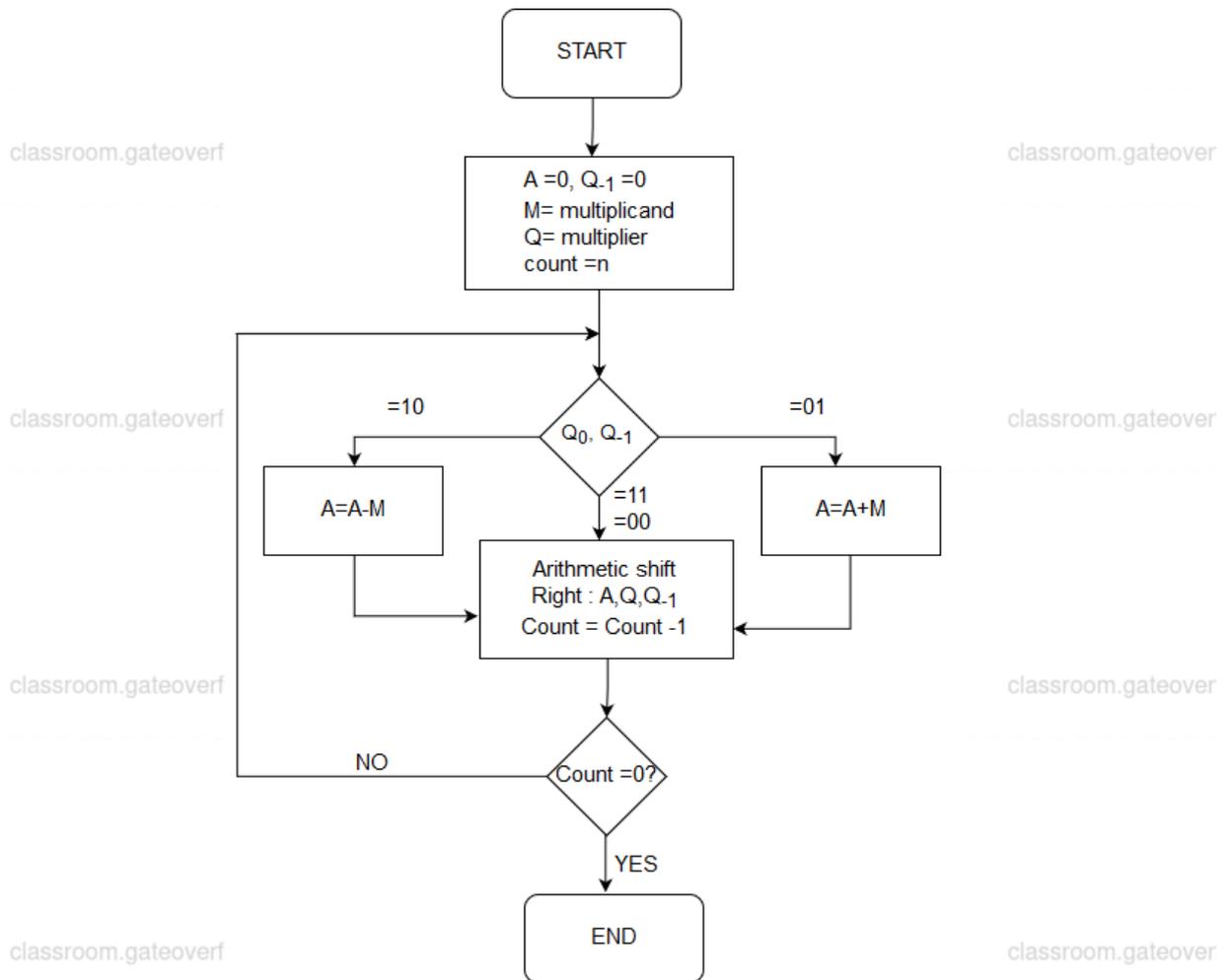
Answer

Answers: Booths Algorithm



- ✓ [Booth's multiplication algorithm](#) is a multiplication algorithm that multiplies two signed binary numbers in two's complement notation.

The block diagram for the implementation of the Booth's algorithm for determining the product of two 8-bit signed numbers is as shown below.



The Multiplier and Multiplicand are placed in the Q and M registers, respectively. There is also a 1-bit register placed logically to the right of the least significant bit (Q_0) of the Q register and designated Q_{-1} .

The results of the multiplication will appear in the A and Q registers. A and Q_{-1} are initialized to 0. The control logic scans the bits of the multiplier one at a time. Now, as each bit is examined, the bit to its right is also examined. If the two bits are the same (11 or 00), then all of the bits of the A , Q , and Q_{-1} registers are shifted to the right 1 bit. If the two bits differ, then the multiplicand is added to or subtracted from the A register, depending on whether the two bits are 01 or 10. Following, the addition or subtraction, the right shift occurs.

In either case, the right shift is such that the leftmost bit of A , namely A_{n-1} , not only is shifted into A_{n-2} , but also remains in A_{n-1} . This is required to preserve the sign of the number in A and Q . It is known as an arithmetic shift, because it preserves the sign bit.

References



6 votes

-- Satbir Singh (21k points)

4.5.2 Booths Algorithm: GATE CSE 1996 | Question: 1.23 top 9

<https://gateoverflow.in/2727>



✓ Answer: A

The worst case of an implementation using Booth's algorithm is when pairs of 01s or 10s occur very frequently in the multiplier.

30 votes

-- Rajarshi Sarkar (27.9k points)



✓ Convert 57 to Binary & Get 2's complement. It is "11000111" & Attach one extra 0 to right of it

110001110

To calculate booth code subtract right digit from left digit in every consecutive 2 digits.

So, 11 → 0, 10 → +1. Finally, 10 → +1

So, answer is (B).

There is another way to solve this question.

0 – 100 + 100 – 1 → If you check binary weighted sum of this code you will get –57. This is trick to quick check. Booth code is always equivalent to it's original value if checked as weighted code. If you check it before doing above procedure & if only one of option maps, you don't need to do above procedure, just mark the answer.

Here, $(-1) \times 64 + (+1) \times 8 + (-1) \times 1 = -57$.

👍 37 votes

-- Akash Kanase (36k points)



✓ 2's complement of –57 is (11000111)

Booth multiplier :

1	1	0	0	0	1	1	1	
1	0	0	0	1	1	1	0	(put 0 in 1st and shift multiplier left by 1 bit)
0	-1	0	0	1	0	0	-1	

Use this encoded scheme: 00 → 0, 01 → +1, 10 → –1, 11 → 0

Correct Answer: A.

👍 21 votes

-- Prashant Singh (47.2k points)



✓ We can have 1 bit or 2 bit Booth codes. This question is about 2 bit Booth codes. In Booth's algorithm, we get partial products by multiplying specific codes with the multiplicand. These partial products are used to get the actual product. We initially calculate 2 bit booth code of the multiplier in this question. Then each bit of the code is multiplied with the multiplicand to get the partial product as shown in the last column of the given table. Here, the multiplicand is Y. So, notice that each row of partial product column is multiplied with Y.

Now, the question is how to get these codes i.e., how to represent a multiplier with a 2 bit booth code. For that we need to look at the pair of 3 bits as shown in the table below. To get code C_i , look for 3 bits as shown.

x_{i+1}	x_i	x_{i-1}	Boothcode(C_i)
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	2
1	0	0	–2
1	0	1	–1
1	1	0	–1
1	1	1	0

Now, multiply i^{th} code to get partial product. Therefore, Option C is correct.

👍 6 votes

-- Monanshi Jain (7k points)



Answer is **B**.

Append **0** the end of multiplier : 0111 0111 1011 1101 **0**

Now, Paired bits from right end as 00-(**0**), 01-(**+1**), 10-(**-1**) and 11-(**0**)

note:- pairs are overlapped.

Count **+1=4** (additions required)

Count **-1=4** (subtractions required)

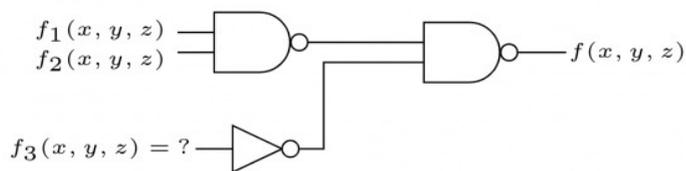
So, total **8** pair hence addition/subtraction required = 8.

👍 27 votes

-- Rajarshi Sarkar (27.9k points)



Consider the following logic circuit whose inputs are functions f_1, f_2, f_3 and output is f



Given that

- $f_1(x, y, z) = \Sigma(0, 1, 3, 5)$
- $f_2(x, y, z) = \Sigma(6, 7)$, and
- $f(x, y, z) = \Sigma(1, 4, 5)$.

f_3 is

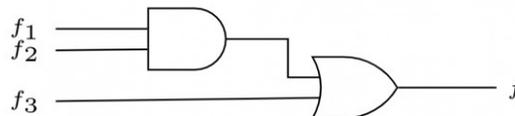
- $\Sigma(1, 4, 5)$
- $\Sigma(6, 7)$
- $\Sigma(0, 1, 3, 5)$
- None of the above

gate2002-cse digital-logic normal canonical-normal-form circuit-output

Answer



Given f_1, f_3 and f in canonical sum of products form (in decimal) for the circuit



$$f_1 = \Sigma m(4, 5, 6, 7, 8)$$

$$f_3 = \Sigma m(1, 6, 15)$$

$$f = \Sigma m(1, 6, 8, 15)$$

then f_2 is

- $\Sigma m(4, 6)$
- $\Sigma m(4, 8)$
- $\Sigma m(6, 8)$

D. $\Sigma m(4, 6, 8)$

gate2008-cse digital-logic canonical-normal-form easy

Answer 

4.6.3 Canonical Normal Form: GATE CSE 2010 | Question: 6 [top](#)

<https://gateoverflow.in/2177>



The minterm expansion of $f(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$ is

- A. $m_2 + m_4 + m_6 + m_7$
- B. $m_0 + m_1 + m_3 + m_5$
- C. $m_0 + m_1 + m_6 + m_7$
- D. $m_2 + m_3 + m_4 + m_5$

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gate2010-cse digital-logic canonical-normal-form normal

Answer 

4.6.4 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 43 [top](#)

<https://gateoverflow.in/8503>



The total number of prime implicants of the function $f(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 10)$ is _____

gate2015-cse-set3 digital-logic canonical-normal-form normal numerical-answers goclasses.in

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Answer 

4.6.5 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 44 [top](#)

<https://gateoverflow.in/8504>



Given the function $F = P' + QR$, where F is a function in three Boolean variables P, Q and R and $P' = \neg P$, consider the following statements.

(S1) $F = \Sigma(4, 5, 6)$

(S2) $F = \Sigma(0, 1, 2, 3, 7)$

(S3) $F = \Pi(4, 5, 6)$

(S4) $F = \Pi(0, 1, 2, 3, 7)$

Which of the following is true?

- A. (S1)-False, (S2)-True, (S3)-True, (S4)-False
- B. (S1)-True, (S2)-False, (S3)-False, (S4)-True
- C. (S1)-False, (S2)-False, (S3)-True, (S4)-True
- D. (S1)-True, (S2)-True, (S3)-False, (S4)-False

gate2015-cse-set3 digital-logic canonical-normal-form normal

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Answer 

4.6.6 Canonical Normal Form: GATE CSE 2019 | Question: 50 [top](#)

<https://gateoverflow.in/302798>



What is the minimum number of 2-input NOR gates required to implement a 4 -variable function expressed in sum-of-minterms form as $f = \Sigma(0, 2, 5, 7, 8, 10, 13, 15)$? Assume that all the inputs and their complements are available. Answer:

gate2019-cse numerical-answers digital-logic canonical-normal-form

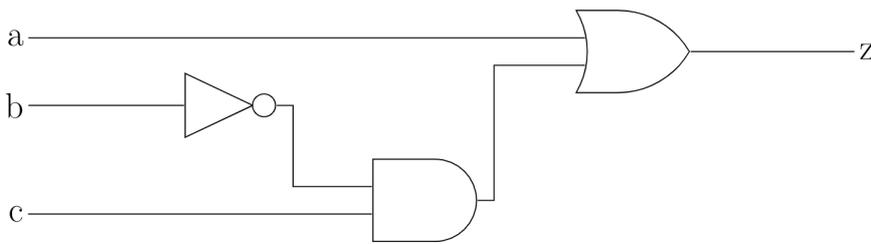
Answer 

4.6.7 Canonical Normal Form: GATE CSE 2020 | Question: 28 [top](#)

<https://gateoverflow.in/332203>



Consider the Boolean function $z(a, b, c)$.



Which one of the following minterm lists represents the circuit given above?

- A. $z = \sum(0, 1, 3, 7)$
- B. $z = \sum(1, 4, 5, 6, 7)$
- C. $z = \sum(2, 4, 5, 6, 7)$
- D. $z = \sum(2, 3, 5)$

gate2020-cse digital-logic canonical-normal-form

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Answer

Answers: Canonical Normal Form

4.6.1 Canonical Normal Form: GATE CSE 2002 | Question: 2-1 [top](#)

<https://gateoverflow.in/831>



✓ $f = ((f_1 f_2)' f_3)' = f_1 f_2 + f_3$

In minimum sum of products form, AND of two expressions will contain the common terms. Since f_1 and f_2 don't have any common term, $f_1 f_2$ is 0 and hence $f = f_3 = \sum(1, 4, 5)$.

Correct Answer: A

81 votes

-- Arjun Suresh (332k points)

4.6.2 Canonical Normal Form: GATE CSE 2008 | Question: 8 [top](#)

<https://gateoverflow.in/406>



✓ Answer is C.

With AND gates we will choose intersection of min-terms.

With OR gates we will take union of min-terms.

45 votes

-- Ankit Rokde (6.9k points)

4.6.3 Canonical Normal Form: GATE CSE 2010 | Question: 6 [top](#)

<https://gateoverflow.in/2177>



✓
$$\begin{aligned} PQ + QR' + PR' &= PQR + PQR' + PQR' + P'QR' + PQR' + PQ'R' \\ &= PQR + PQR' + P'QR' + PQ'R' (111 + 110 + 010 + 100) \\ &= m_7 + m_6 + m_2 + m_4 \end{aligned}$$

Option A.

Alternatively,
Using K-map

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QR	00	01	11	10
P				
0				1
1	1		1	1

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34 votes

-- Arjun Suresh (332k points)

4.6.4 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 43 [top](#)

<https://gateoverflow.in/8503>



✓

yz	00	01	11	10
wx				
00	*1	0	0	1
01	1	*1	0	*1
11	0	0	0	0
10	0	0	0	*1

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As you can see that there is one 4-set and two 2-set that are covering the star marked 1's (i.e. the ones that are not covered by any other combinations).

So, the answer is 3.

53 votes

-- Tamojit Chatterjee (1.9k points)

4.6.5 Canonical Normal Form: GATE CSE 2015 Set 3 | Question: 44 [top](#)

<https://gateoverflow.in/8504>



✓ $F = P' + QR$, draw the Kmap for this

We can find the minterm $\sum(0, 1, 2, 3, 7)$ and maxterm $\Pi(4, 5, 6)$

So, option A is correct: (S1)-False, (S2)-True, (S3)-True, (S4)-False

33 votes

-- Anoop Sonkar (4.1k points)

$$F = P' + QR$$

for SOP we have :

$$F = P.1.1 + 1.QR' = P'(Q + Q')(R + R') + (P + P')QR$$

$$P'QR + P'QR' + P'Q'R + P'Q'R' + PQR + P'QR$$

$$P'QR + P'QR' + P'Q'R + P'Q'R' + PQR$$

$F = \sum(0, 1, 2, 3, 7)$ (considering barred terms as 0 and unbarred as 1 and converting them to binary and then to decimal).

now for POS we have :

$$F = P' + QR = (P' + Q)(P' + R) = (P' + Q + 0)(P' + R + 0)$$

$$(P' + Q + R \cdot R')(P' + R + Q \cdot Q')$$

$$(P' + Q + R)(P' + Q + R)(P' + Q + R')(P' + Q' + R)$$

$$(P' + Q + R)(P' + Q + R')(P' + Q' + R)$$

$F = \prod(4, 5, 6)$ (considering barred terms as 1 and unbarred as 0 and converting them to binary and then to decimal).

<http://mcs.uwsuper.edu/sb/461/PDF/sop.html>

References



15 votes

-- Tamojit Chatterjee (1.9k points)

4.6.6 Canonical Normal Form: GATE CSE 2019 | Question: 50 top 5

<https://gateoverflow.in/302798>



✓

CD \ AB	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	1	1	0
10	1	0	0	1

$$f = (B' + D) \cdot (B + D')$$

It is mentioned that both Complimentary as well as Uncomplimentary forms are available.

$$B' \text{ NOR } D = (B' + D)'$$

$$B \text{ NOR } D' = (B + D)'$$

$$(B' \text{ NOR } D) \text{ NOR } (B \text{ NOR } D')$$

$$= ((B' + D)' + (B + D)')$$

$$= ((B' + D)'' \cdot (B + D)'')$$

$$= ((B' + D) \cdot (B + D))$$

$$= f$$

Thus, 3 NOR Gates are required.

32 votes

-- Balaji Jegan (3.5k points)

4.6.7 Canonical Normal Form: GATE CSE 2020 | Question: 28 top 5

<https://gateoverflow.in/333203>



✓

From given circuit $z = a + b'c$

K-Map for the above expression is:

bc \ a	00	01	11	10
0	0	1	0	0
1	1	1	1	1

Minterms are $\sum(1, 4, 5, 6, 7)$

Hence, option (B) is correct

7 votes

4.7

Carry Generator (2) top

4.7.1 Carry Generator: GATE CSE 2006 | Question: 36 top

<https://gateoverflow.in/1294>



Given two three bit numbers $a_2a_1a_0$ and $b_2b_1b_0$ and c the carry in, the function that represents the carry generate function when these two numbers are added is:

- A. $a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2a_0b_1b_0 + a_1b_2b_1 + a_1a_0b_2b_0 + a_0b_2b_1b_0$
- B. $a_2b_2 + a_2b_1b_0 + a_2a_1b_1b_0 + a_1a_0b_2b_1 + a_1a_0b_2 + a_1a_0b_2b_0 + a_2a_0b_1b_0$
- C. $a_2 + b_2 + (a_2 \oplus b_2)(a_1 + b_1 + (a_1 \oplus b_1) + (a_0 + b_0))$
- D. $a_2b_2 + \overline{a_2}a_1b_1 + \overline{a_2}a_1a_0b_0 + \overline{a_2}a_0\overline{b_1}b_0 + a_1\overline{b_2}b_1 + \overline{a_1}a_0\overline{b_2}b_0 + a_0\overline{b_2}b_1b_0$

gate2006-cse digital-logic normal carry-generator

Answer

4.7.2 Carry Generator: GATE CSE 2007 | Question: 35 top

<https://gateoverflow.in/1233>



In a look-ahead carry generator, the carry generate function G_i and the carry propagate function P_i for inputs A_i and B_i are given by:

$$P_i = A_i \oplus B_i \text{ and } G_i = A_i B_i$$

The expressions for the sum bit S_i and the carry bit C_{i+1} of the look ahead carry adder are given by:

$$S_i = P_i \oplus C_i \text{ and } C_{i+1} = G_i + P_i C_i, \text{ where } C_0 \text{ is the input carry.}$$

Consider a two-level logic implementation of the look-ahead carry generator. Assume that all P_i and G_i are available for the carry generator circuit and that the AND and OR gates can have any number of inputs. The number of AND gates and OR gates needed to implement the look-ahead carry generator for a 4-bit adder with S_3, S_2, S_1, S_0 and C_4 as its outputs are respectively:

- A. 6, 3
- B. 10, 4
- C. 6, 4
- D. 10, 5

gate2007-cse digital-logic normal carry-generator adder

Answer

Answers: Carry Generator

4.7.1 Carry Generator: GATE CSE 2006 | Question: 36 top

<https://gateoverflow.in/1294>



✓ $c_1 = a_0 b_0$

$$c_2 = a_1 b_1 + a_1 c_1 + b_1 c_1$$

$$c_3 = a_2 b_2 + a_2 c_2 + b_2 c_2 \\ = a_2 b_2 + a_2 a_1 b_1 + a_2 a_1 c_1 + a_2 b_1 c_1 + b_2 a_1 b_1 + b_2 a_1 c_1 + b_2 b_1 c_1$$

$$= a_2b_2 + a_2a_1b_1 + a_2a_1a_0b_0 + a_2b_1a_0b_0 + b_2a_1b_1 + b_2a_1a_0b_0 + b_2b_1a_0b_0$$

Option is A.

Considering the carry in function c , $c_1 = a_0b_0 + a_0c + b_0c$, but c is missing in all options and hence ignored.

👍 65 votes

-- Arjun Suresh (332k points)

4.7.2 Carry Generator: GATE CSE 2007 | Question: 35 [top](#)

<https://gateoverflow.in/1233>



✓ $C1 = G0 + C0.P0$

$$C2 = G1 + G0.P1 + C0.P0.P1$$

$$C3 = G2 + G1.P2 + G0.P1.P2 + C0.P0.P1.P2$$

$C4 = G3 + G2.P3 + G1.P2.P3 + G0.P1.P2.P3 + C0.P0.P1.P2.P3$ // read this as carry is generated in 3rd stage OR carry is generated in 2nd stage AND propagated to 3rd stage OR carry is generated in 1st stage AND carry is propagated through 2nd AND 3rd stage OR carry is generated in 0th stage AND propagated through 1st 2nd AND 3rd stage OR initial carry is propagated through 0th, 1st, 2nd AND 3rd stage.

4 OR gates are required for $C1, C2, C3, C4$

- 1 AND gate for $C1$
- 2 AND gate for $C2$
- 3 AND gate for $C3$
- 4 AND gate for $C4$
- AND = 10
- OR = 4

Correct Answer: B.

👍 60 votes

-- Vikrant Singh (11.2k points)

4.8

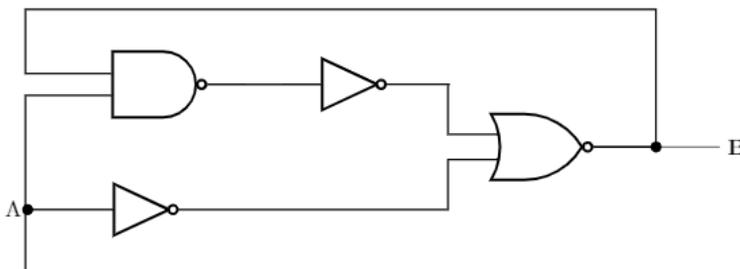
Circuit Output (38) [top](#)

4.8.1 Circuit Output: GATE CSE 1989 | Question: 4-ix [top](#)

<https://gateoverflow.in/88164>



Explain the behaviour of the following logic circuit with level input A and output B .



gate1989 descriptive digital-logic circuit-output

Answer

4.8.2 Circuit Output: GATE CSE 1990 | Question: 3-i [top](#)

<https://gateoverflow.in/84051>



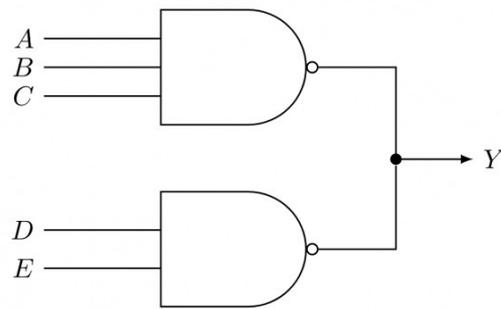
Choose the correct alternatives (More than one may be correct).

Two NAND gates having open collector outputs are tied together as shown in below figure.

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The logic function Y , implemented by the circuit is,

- A. $Y = \overline{ABC} + \overline{DE}$
- B. $Y = \overline{ABC} + DE$
- C. $Y = \overline{ABC} \cdot \overline{DE}$
- D. $Y = \overline{ABC} \cdot DE$

gate1990 normal digital-logic circuit-output

Answer

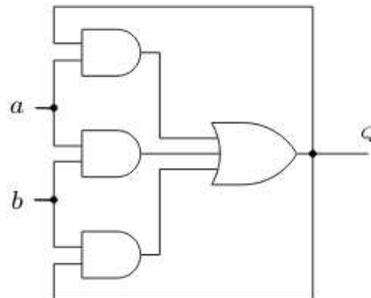
4.8.3 Circuit Output: GATE CSE 1991 | Question: 5-a [top](#)

<https://gateoverflow.in/531>



Analyse the circuit in Fig below and complete the following table

a	b	Q_n
0	0	
0	1	
1	0	
1	1	



gate1991 digital-logic normal circuit-output sequential-circuit descriptive

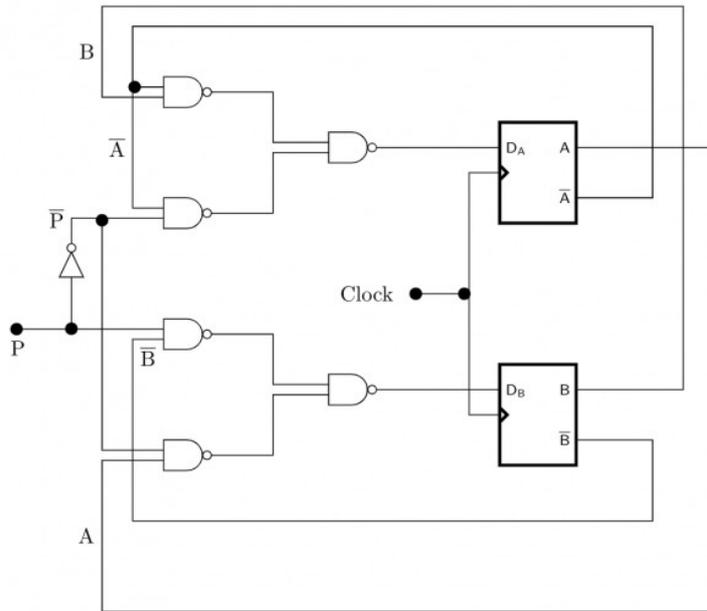
Answer

4.8.4 Circuit Output: GATE CSE 1993 | Question: 19 [top](#)

<https://gateoverflow.in/2316>



A control algorithm is implemented by the NAND – gate circuitry given in figure below, where A and B are state variable implemented by D flip-flops, and P is control input. Develop the state transition table for this controller.



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gate1993 digital-logic sequential-circuit flip-flop circuit-output normal descriptive

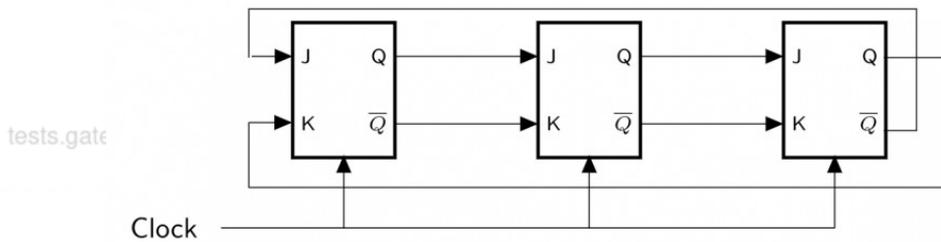
Answer

4.8.5 Circuit Output: GATE CSE 1993 | Question: 6-3 top 3

https://gateoverflow.in/17237



For the initial state of 000, the function performed by the arrangement of the J-K flip-flops in figure is:



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- A. Shift Register
- B. Mod- 3 Counter
- C. Mod- 6 Counter
- D. Mod- 2 Counter
- E. None of the above

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gate1993 digital-logic sequential-circuit flip-flop digital-counter circuit-output multiple-selects

Answer

4.8.6 Circuit Output: GATE CSE 1993 | Question: 6.1 top 3

https://gateoverflow.in/2288

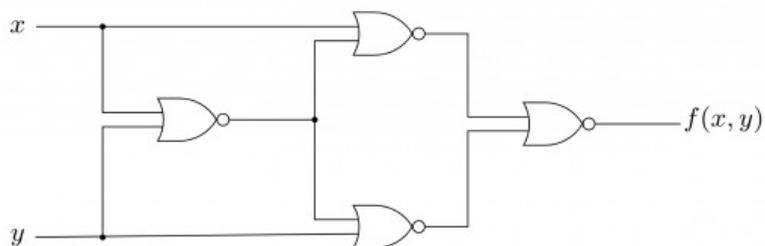


Identify the logic function performed by the circuit shown in figure.

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- A. exclusive OR
- B. exclusive NOR
- C. NAND
- D. NOR
- E. None of the above

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gate1993 digital-logic combinational-circuits circuit-output normal

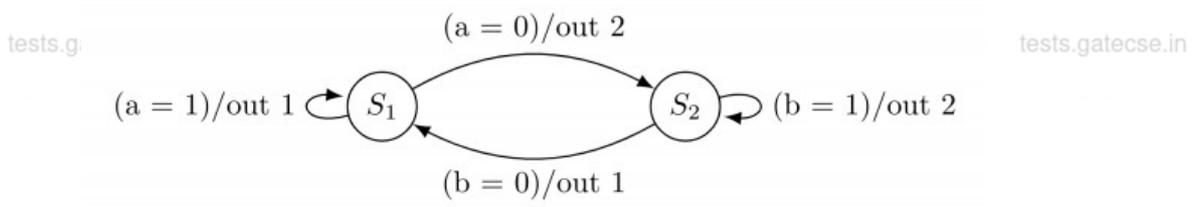
Answer

4.8.7 Circuit Output: GATE CSE 1993 | Question: 6.2 top

<https://gateoverflow.in/17235>



If the state machine described in figure should have a stable state, the restriction on the inputs is given by



- A. $a \cdot b = 1$
- B. $a + b = 1$
- C. $\overline{a} + \overline{b} = 0$
- D. $\overline{a \cdot b} = 1$
- E. $\overline{a + b} = 1$

gate1993 digital-logic normal circuit-output sequential-circuit

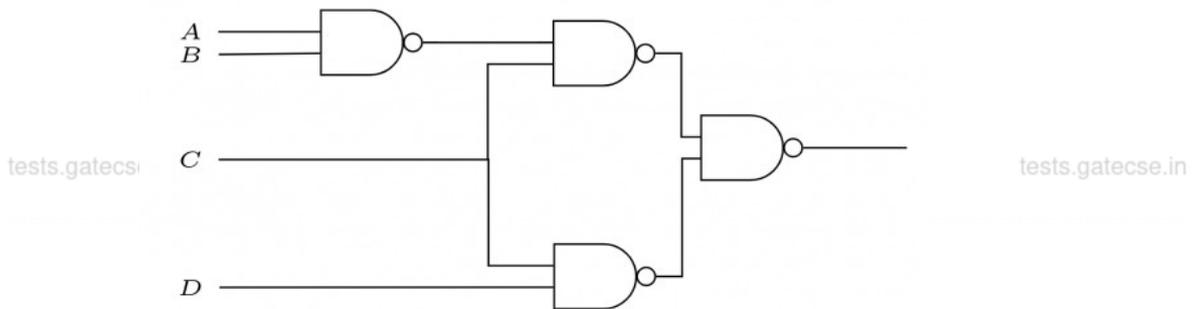
Answer

4.8.8 Circuit Output: GATE CSE 1994 | Question: 1.8 top

<https://gateoverflow.in/2445>



The logic expression for the output of the circuit shown in figure below is:



- A. $\overline{AC} + \overline{BC} + CD$
- B. $\overline{AC} + \overline{BC} + CD$
- C. $ABC + \overline{C} \overline{D}$
- D. $\overline{A} \overline{B} + \overline{B} \overline{C} + CD$

gate1994 digital-logic circuit-output normal

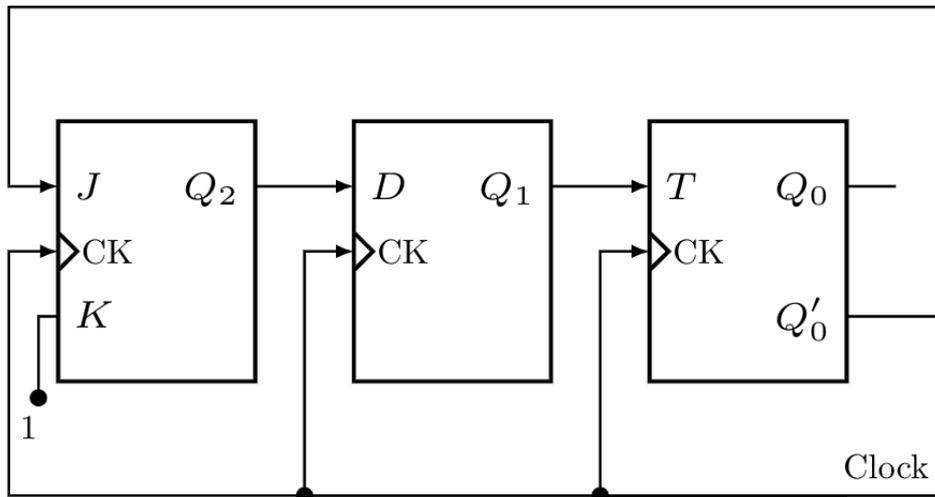
Answer

4.8.9 Circuit Output: GATE CSE 1994 | Question: 11 top

<https://gateoverflow.in/2507>



Find the contents of the flip-flop Q_2, Q_1 and Q_0 in the circuit of figure, after giving four clock pulses to the clock terminal. Assume $Q_2 Q_1 Q_0 = 000$ initially.



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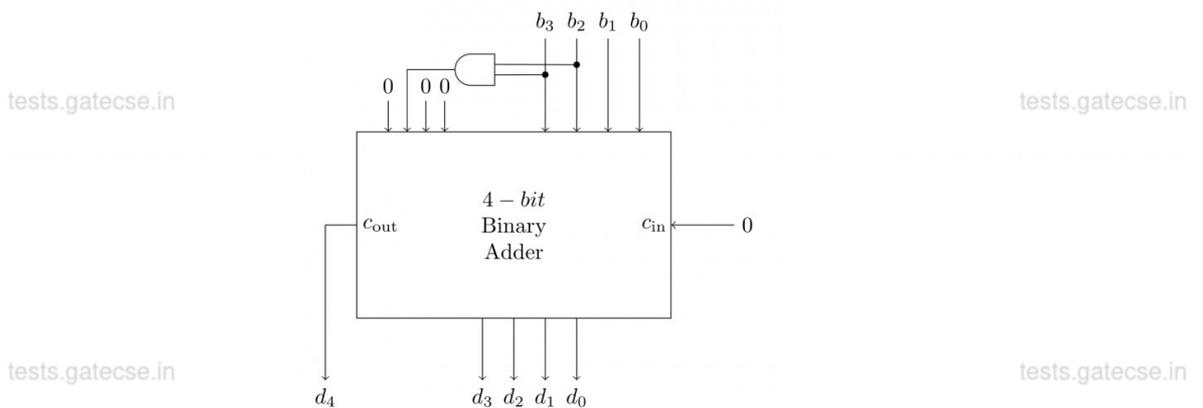
gate1994 digital-logic sequential-circuit digital-counter circuit-output normal descriptive

Answer

4.8.10 Circuit Output: GATE CSE 1996 | Question: 2.21 <https://gateoverflow.in/2750>



Consider the circuit in below figure which has a four bit binary number $b_3b_2b_1b_0$ as input and a five bit binary number, $d_4d_3d_2d_1d_0$ as output.



- A. Binary to Hex conversion
- B. Binary to BCD conversion
- C. Binary to Gray code conversion
- D. Binary to *radix* - 12 conversion

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gate1996 digital-logic circuit-output normal

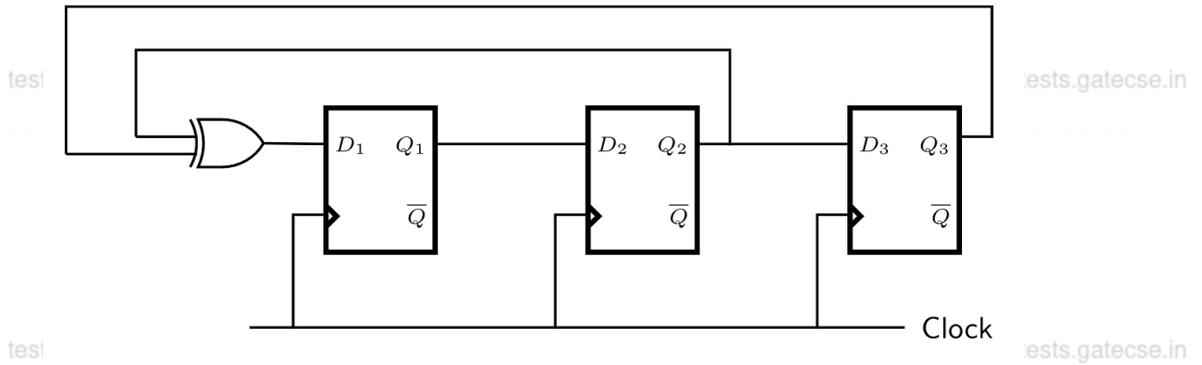
Answer

4.8.11 Circuit Output: GATE CSE 1996 | Question: 24-a <https://gateoverflow.in/2776>



Consider the synchronous sequential circuit in the below figure

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Draw a state diagram, which is implemented by the circuit. Use the following names for the states corresponding to the values of flip-flops as given below.

Q1	Q2	Q3	State
0	0	0	S ₀
0	0	1	S ₁
-	-	-	-
-	-	-	-
-	-	-	-
1	1	1	S ₇

gate1996 digital-logic circuit-output normal descriptive

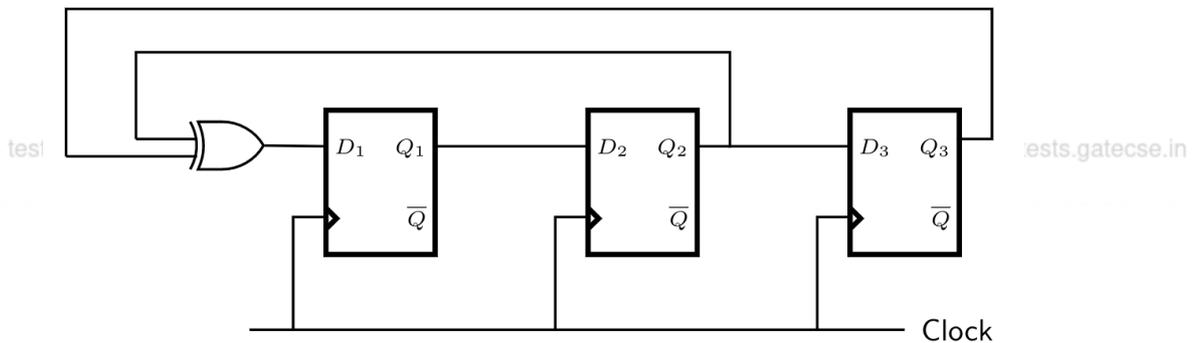
Answer

4.8.12 Circuit Output: GATE CSE 1996 | Question: 24-b

<https://gateoverflow.in/203691>



Consider the synchronous sequential circuit in the below figure



Given that the initial state of the circuit is S₄, identify the set of states, which are not reachable.

gate1996 normal digital-logic circuit-output descriptive

Answer

4.8.13 Circuit Output: GATE CSE 1997 | Question: 5.5

<https://gateoverflow.in/2256>

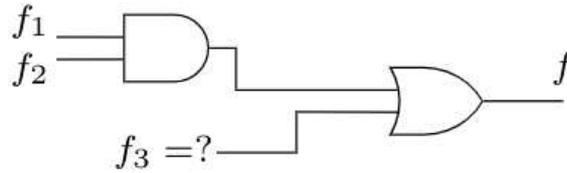


Consider a logic circuit shown in figure below. The functions f_1 , f_2 and f (in canonical sum of products form in decimal notation) are:

$$f_1(w, x, y, z) = \sum 8, 9, 10$$

$$f_2(w, x, y, z) = \sum 7, 8, 12, 13, 14, 15$$

$$f(w, x, y, z) = \sum 8, 9$$



The function f_3 is

- A. $\sum 9, 10$
- B. $\sum 9$
- C. $\sum 1, 8, 9$
- D. $\sum 8, 10, 15$

gate1997 digital-logic circuit-output normal

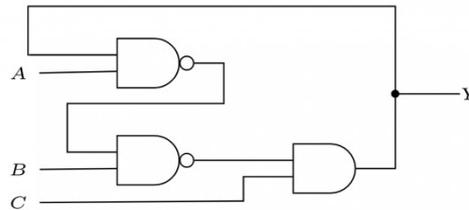
Answer

4.8.14 Circuit Output: GATE CSE 1999 | Question: 2.8 [top](#)

<https://gateoverflow.in/1486>



Consider the circuit shown below. In a certain steady state, the line Y is at '1'. What are the possible values of A , B and C in this state?



- A. $A = 0, B = 0, C = 1$
- B. $A = 0, B = 1, C = 1$
- C. $A = 1, B = 0, C = 1$
- D. $A = 1, B = 1, C = 1$

gate1999 digital-logic circuit-output normal

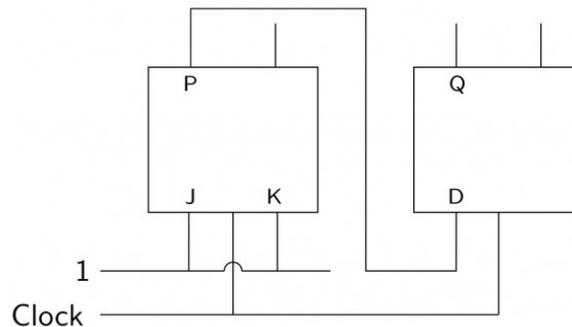
Answer

4.8.15 Circuit Output: GATE CSE 2000 | Question: 2.12 [top](#)

<https://gateoverflow.in/659>



The following arrangement of master-slave flip flops



has the initial state of P, Q as 0, 1 (respectively). After three clock cycles the output state P, Q is (respectively),

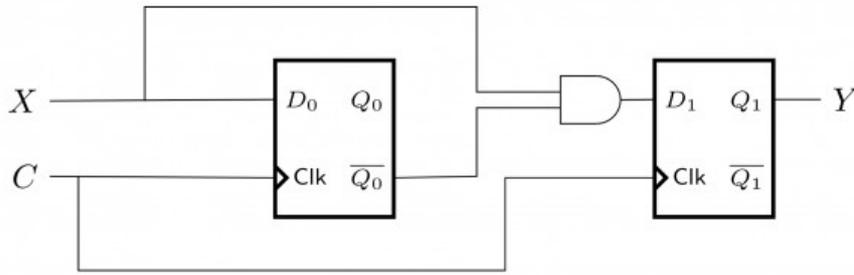
- A. 1, 0
- B. 1, 1

- C. 0,0
- D. 0,1

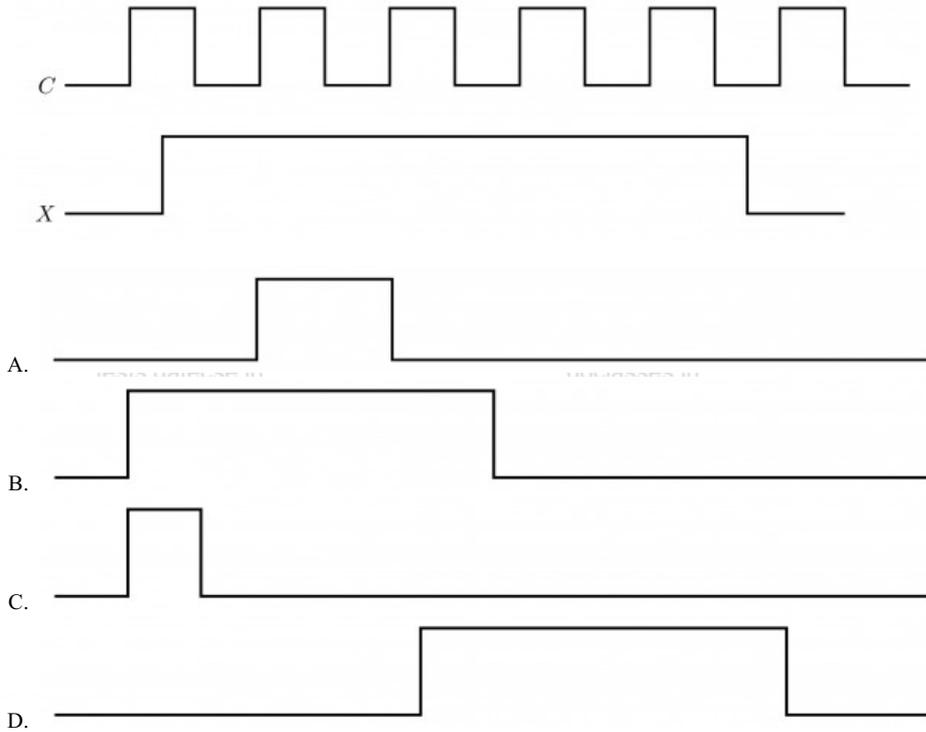
Answer

4.8.16 Circuit Output: GATE CSE 2001 | Question: 2.8

Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D Flip-flops are positive edged triggered and have set up times 20 nanosecond and hold times 0.



Consider the following timing diagrams of X and C. The clock period of $C \geq 40$ nanosecond. Which one is the correct plot of Y?

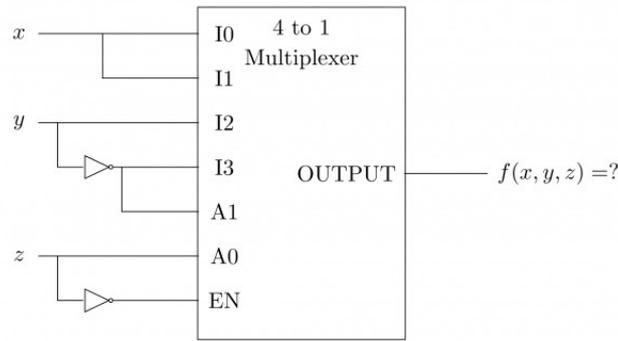


Answer

4.8.17 Circuit Output: GATE CSE 2002 | Question: 2.2

Consider the following multiplexer where I_0, I_1, I_2, I_3 are four data input lines selected by two address line combinations $A1A0 = 00, 01, 10, 11$ respectively and f is the output of the multiplexor. EN is the Enable input.

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The function $f(x, y, z)$ implemented by the above circuit is

- A. xyz'
- B. $xy + z$
- C. $x + y$
- D. None of the above

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gate2002-cse digital-logic circuit-output normal

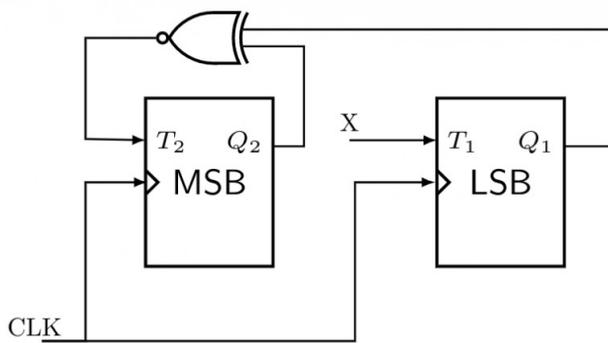
Answer

4.8.18 Circuit Output: GATE CSE 2004 | Question: 61

<https://gateoverflow.in/1056>



Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence $0 - 2 - 3 - 1 = 0$, as shown below.



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To complete the circuit, the input X should be

- A. Q_2^c
- B. $Q_2 + Q_1$
- C. $(Q_1 + Q_2)^c$
- D. $Q_1 \oplus Q_2$

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gate2004-cse digital-logic circuit-output normal

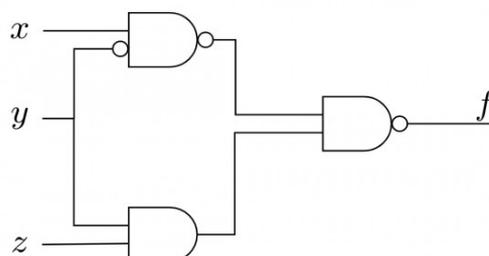
Answer

4.8.19 Circuit Output: GATE CSE 2005 | Question: 15

<https://gateoverflow.in/1351>



Consider the following circuit.



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Which one of the following is TRUE?

- A. f is independent of x
- B. f is independent of y
- C. f is independent of z
- D. None of x, y, z is redundant

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gate2005-cse digital-logic circuit-output normal

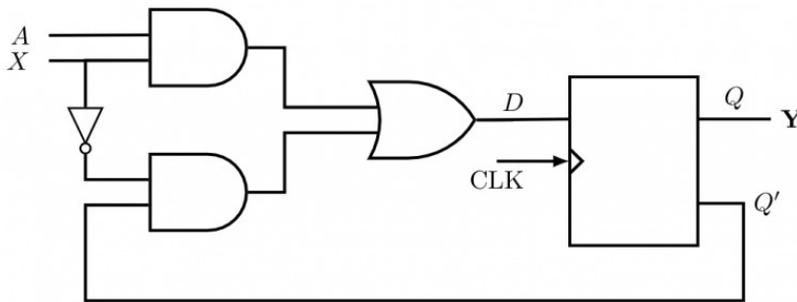
Answer

4.8.20 Circuit Output: GATE CSE 2005 | Question: 62 top

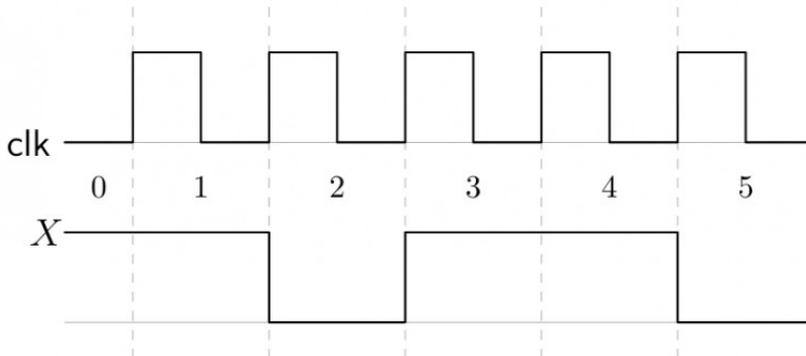
<https://gateoverflow.in/264>



Consider the following circuit involving a positive edge triggered D FF.



Consider the following timing diagram. Let A_i represents the logic level on the line a in the i -th clock period.



Let A' represent the complement of A . The correct output sequence on Y over the clock periods 1 through 5 is:

- A. $A_0 A_1 A'_1 A_3 A_4$
- B. $A_0 A_1 A'_2 A_3 A_4$
- C. $A_1 A_2 A'_2 A_3 A_4$
- D. $A_1 A'_2 A_3 A_4 A'_5$

gate2005-cse digital-logic circuit-output normal

Answer

4.8.21 Circuit Output: GATE CSE 2005 | Question: 64 top

<https://gateoverflow.in/1387>

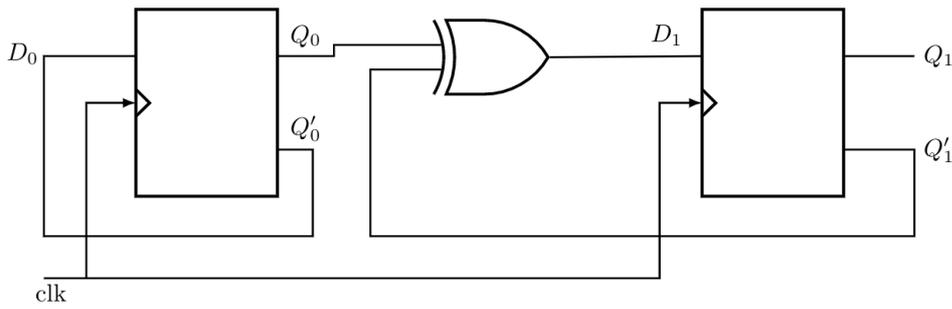


Consider the following circuit:

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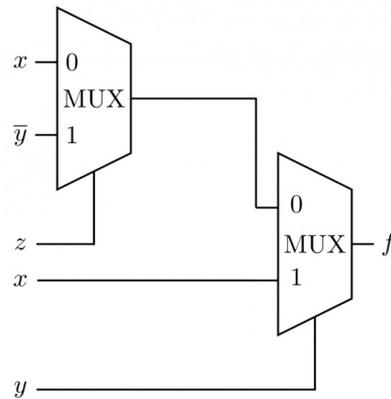
The flip-flops are positive edge triggered D FFs. Each state is designated as a two-bit string Q_0Q_1 . Let the initial state be 00. The state transition sequence is

- A. $00 \rightarrow 11 \rightarrow 01$
- B. $00 \rightarrow 11$
- C. $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$
- D. $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$

gate2005-cse digital-logic circuit-output
 Answer

4.8.22 Circuit Output: GATE CSE 2006 | Question: 35

<https://gateoverflow.in/1292>



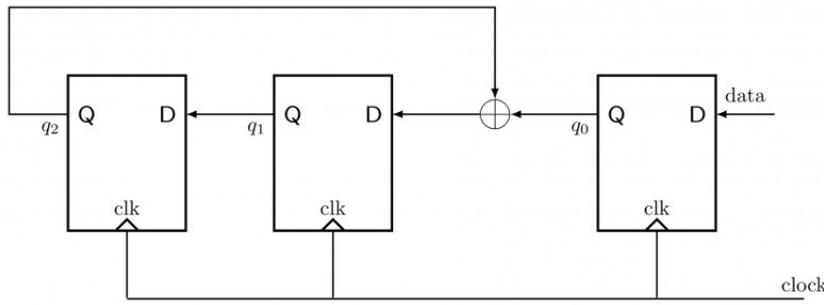
Consider the circuit above. Which one of the following options correctly represents $f(x, y, z)$

- A. $x\bar{z} + xy + \bar{y}z$
- B. $x\bar{z} + xy + \bar{y}\bar{z}$
- C. $xz + xy + \bar{y}\bar{z}$
- D. $xz + x\bar{y} + \bar{y}z$

gate2006-cse digital-logic circuit-output normal
 Answer



Consider the circuit in the diagram. The \oplus operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared).



The following data: 100110000 is supplied to the “data” terminal in nine clock cycles. After that the values of $q_2 q_1 q_0$ are:

- A. 000
- B. 001
- C. 010
- D. 101

gate2006-cse digital-logic circuit-output easy

Answer [↗](#)



You are given a free running clock with a duty cycle of 50% and a digital waveform f which changes only at the negative edge of the clock. Which one of the following circuits (using clocked D flip-flops) will delay the phase of f by 180° ?

- A.
- B.
- C.
- D.

gate2006-cse digital-logic normal circuit-output

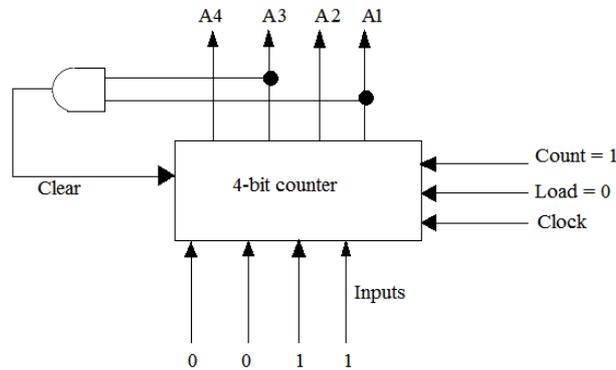
Answer [↗](#)



The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”):

Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No Change
0	↑	1	X	Load Input
0	↑	0	1	Count Next

The counter is connected as follows:



Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence:

- A. 0, 3, 4
- B. 0, 3, 4, 5
- C. 0, 1, 2, 3, 4
- D. 0, 1, 2, 3, 4, 5

gate2007-cse digital-logic circuit-output normal

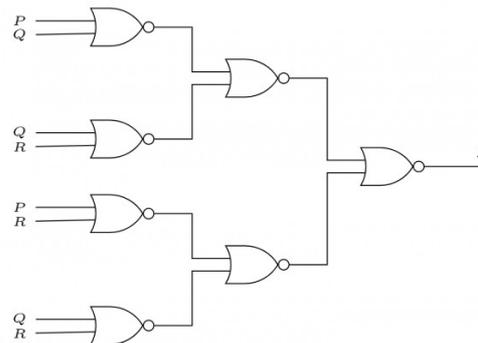
Answer

4.8.26 Circuit Output: GATE CSE 2010 | Question: 31

<https://gateoverflow.in/2205>



What is the boolean expression for the output f of the combinational logic circuit of NOR gates given below?



- A. $\overline{Q + R}$
- B. $\overline{P + Q}$
- C. $\overline{P + R}$
- D. $\overline{P + Q + R}$

gate2010-cse digital-logic circuit-output normal

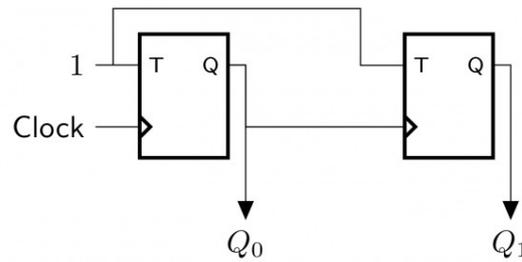
Answer

4.8.27 Circuit Output: GATE CSE 2010 | Question: 32

<https://gateoverflow.in/2205>



In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00. What are the next four values of Q_1Q_0 ?



- A. 11, 10, 01, 00
- B. 10, 11, 01, 00
- C. 10, 00, 01, 11
- D. 11, 10, 00, 01

gate2010-cse digital-logic circuit-output normal

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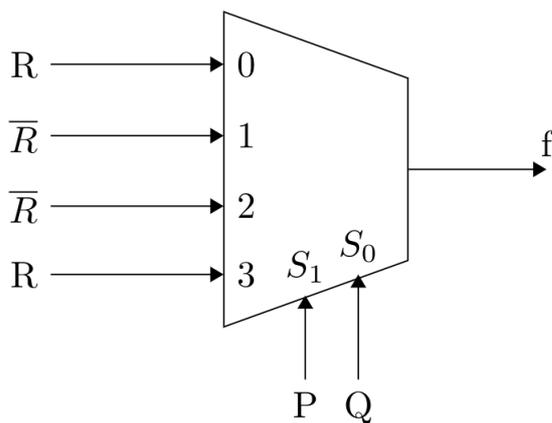
Answer

4.8.28 Circuit Output: GATE CSE 2010 | Question: 9 [top](#)

<https://gateoverflow.in/2182>



The Boolean expression of the output f of the multiplexer shown below is



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- A. $\overline{P \oplus Q \oplus R}$
- B. $P \oplus Q \oplus R$
- C. $P + Q + R$
- D. $\overline{P + Q + R}$

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gate2010-cse digital-logic circuit-output easy

Answer

4.8.29 Circuit Output: GATE CSE 2011 | Question: 50 [top](#)

<https://gateoverflow.in/2157>



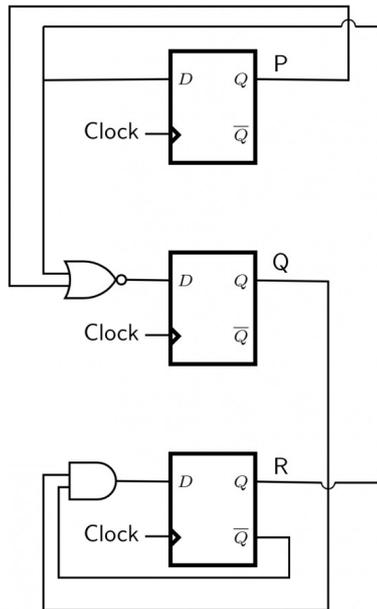
Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.

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If at some instance prior to the occurrence of the clock edge, P , Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

- A. 000
- B. 001
- C. 010
- D. 011

gate2011-cse digital-logic circuit-output flip-flop normal

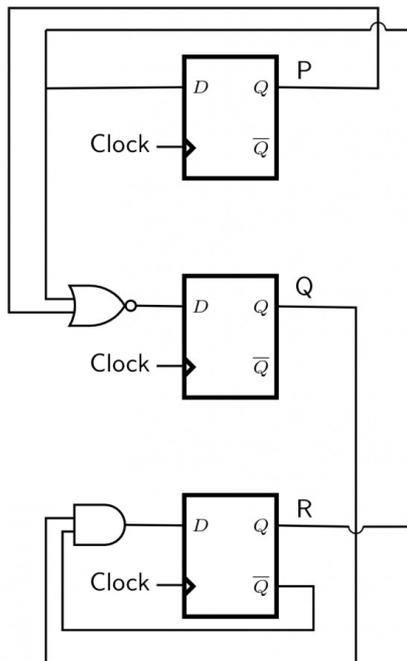
Answer

4.8.30 Circuit Output: GATE CSE 2011 | Question: 51 [top](#)

<https://gateoverflow.in/43318>



Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration.



If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

- A. 3

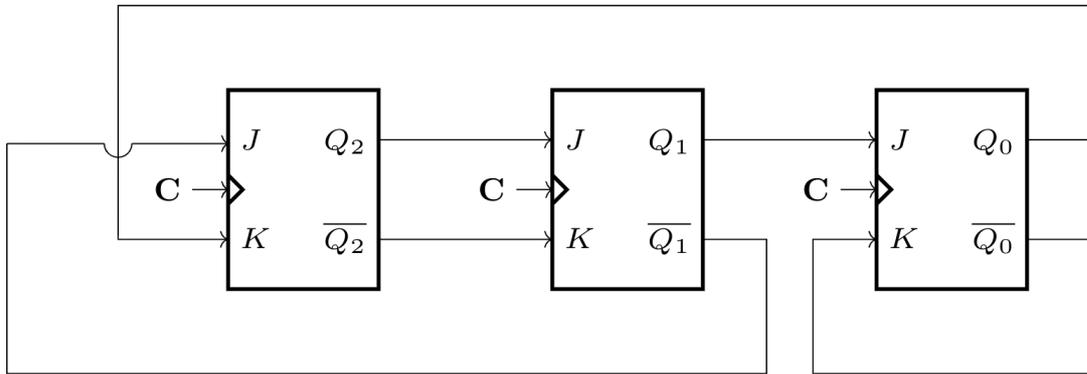
- B. 4
- C. 5
- D. 6

gate2011-cse digital-logic circuit-output normal

Answer

4.8.31 Circuit Output: GATE CSE 2014 Set 3 | Question: 45

https://gateoverflow.in/2079



The above sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is

- A. 001, 010, 011
- B. 111, 110, 101
- C. 100, 110, 111
- D. 100, 011, 001

gate2014-cse-set3 digital-logic circuit-output normal

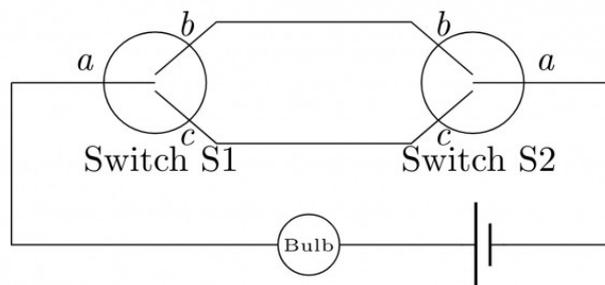
Answer

4.8.32 Circuit Output: GATE IT 2005 | Question: 10

https://gateoverflow.in/3755



A two-way switch has three terminals a, b and c . In ON position (logic value 1), a is connected to b , and in OFF position, a is connected to c . Two of these two-way switches S_1 and S_2 are connected to a bulb as shown below.



Which of the following expressions, if true, will always result in the lighting of the bulb ?

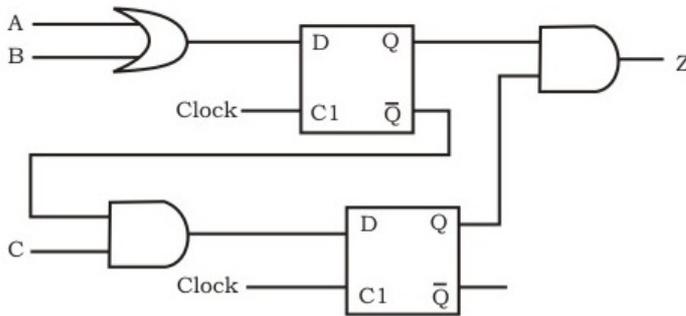
- A. $S_1.S_2$
- B. $S_1 + S_2$
- C. $S_1 \oplus S_2$
- D. $S_1 \oplus \overline{S_2}$

gate2005-it digital-logic circuit-output normal

Answer



Which of the following input sequences will always generate a 1 at the output z at the end of the third cycle?



- A.

A	B	C
0	0	0
1	0	1
1	1	1
- B.

A	B	C
1	0	1
1	1	0
1	1	1
- C.

A	B	C
0	1	1
1	0	1
1	1	1
- D.

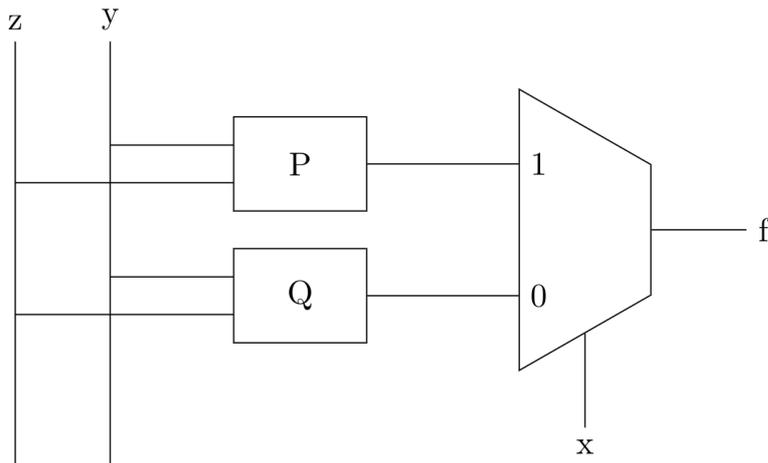
A	B	C
0	0	1
1	1	0
1	1	1

gate2005-it | digital-logic | circuit-output | normal

Answer



The majority function is a Boolean function $f(x, y, z)$ that takes the value 1 whenever a majority of the variables x, y, z are 1. In the circuit diagram for the majority function shown below, the logic gates for the boxes labeled P and Q are, respectively,



- A. XOR, AND
- B. XOR, XOR
- C. OR, OR
- D. OR, AND

gate2006-it digital-logic circuit-output normal

Answer

4.8.35 Circuit Output: GATE IT 2007 | Question: 38

<https://gateoverflow.in/3471>



The following expression was to be realized using 2-input AND and OR gates. However, during the fabrication all 2-input AND gates were mistakenly substituted by 2-input NAND gates. $(a \cdot b) \cdot c + (a' \cdot c) \cdot d + (b \cdot c) \cdot d + a \cdot d$

What is the function finally realized ?

- A. 1
- B. $a' + b' + c' + d'$
- C. $a' + b + c' + d'$
- D. $a' + b' + c + d'$

gate2007-it digital-logic circuit-output normal

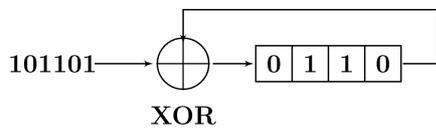
Answer

4.8.36 Circuit Output: GATE IT 2007 | Question: 40

<https://gateoverflow.in/3473>



What is the final value stored in the linear feedback shift register if the input is 101101?



- A. 0110
- B. 1011
- C. 1101
- D. 1111

gate2007-it digital-logic circuit-output normal

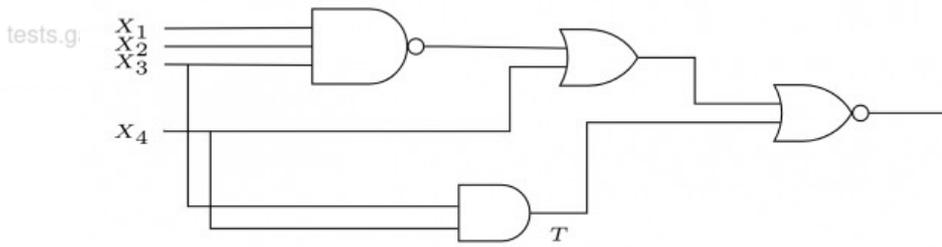
Answer

4.8.37 Circuit Output: GATE IT 2007 | Question: 45

<https://gateoverflow.in/3480>



The line T in the following figure is permanently connected to the ground.



Which of the following inputs ($X_1X_2X_3X_4$) will detect the fault?

- A. 0000
- B. 0111
- C. 1111
- D. None of these

gate2007-it digital-logic circuit-output normal

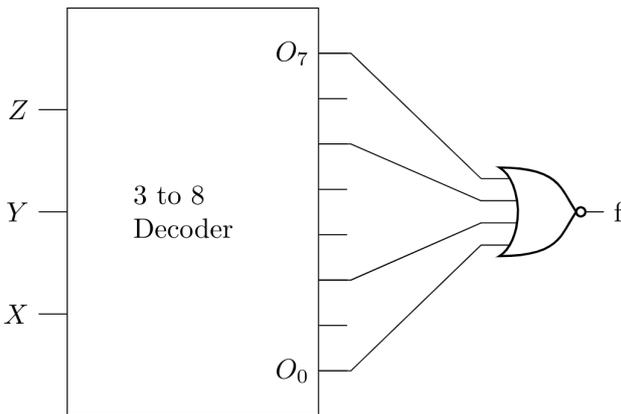
Answer

4.8.38 Circuit Output: GATE IT 2008 | Question: 9

<https://gateoverflow.in/3269>



What Boolean function does the circuit below realize?



- A. $xz + \bar{x}\bar{z}$
- B. $x\bar{z} + \bar{x}z$
- C. $\bar{x}\bar{y} + yz$
- D. $xy + \bar{y}\bar{z}$

gate2008-it digital-logic circuit-output normal

Answer

Answers: Circuit Output

4.8.1 Circuit Output: GATE CSE 1989 | Question: 4-ix

<https://gateoverflow.in/88164>



✓ This is a **sequential circuit** (whose output depends not only on the present value of its input signals but on the sequence of past inputs) not a **combinational** one (whose output depends only on the present inputs), therefore solving using just input variable does not yields correct output.

First we need to simplify the circuit.

The two NOT gates at the input end of the NOR gate can be combined with the gate to get: $(A' + B) = AB$

Now, since we have two variables we will have 4 combinations 00 01 10 11.

On analyzing each we will see that for every combination where

- $A = 0$ we have the stable output of 0
- $A = 1$ we will have a RACE condition

4.8.2 Circuit Output: GATE CSE 1990 | Question: 3-i

https://gateoverflow.in/84051



From [wikipedia \(third paragraph\)](#),

By tying the output of several open collectors together, the common line becomes a "wired AND" (positive-true logic) or "wired OR" (negative-true logic) gate. A "wired AND" behaves like the boolean AND of the two (or more) gates in that it will be logic 1 whenever (all) are in the high impedance state, and 0 otherwise. A "wired OR" behaves like the Boolean OR for negative-true logic, where the output is LOW if any of its inputs are low.

So, after tying the open-collector NAND Gates, the common line becomes a **wired AND**.

$$\text{So, } Y = (\overline{ABC}) \cdot (\overline{DE})$$

By D' Morgan's law, $Y = \overline{ABC + DE}$

Hence,

Correct Answer: Option (B)

References



4.8.3 Circuit Output: GATE CSE 1991 | Question: 5-a

https://gateoverflow.in/531



The output of the circuit given as : $Q = aQ_{n-1} + ab + bQ_{n-1}$

Hence, $Q_n = Q_{n-1}(a + b) + ab$

$$00 \implies Q_{n-1}(0 + 0) + 0.0 = Q_{n-1}(0) + 0 = 0 + 0 = 0$$

$$01 \implies Q_{n-1}(0 + 1) + 0.1 = Q_{n-1}(1) + 0 = Q_{n-1} + 0 = Q_{n-1}$$

$$10 \implies Q_{n-1}(1 + 0) + 1.0 = Q_{n-1}(1) + 0 = Q_{n-1} + 0 = Q_{n-1}$$

$$11 \implies Q_{n-1}(1 + 1) + 1.1 = Q_{n-1}(1) + 1 = Q_{n-1} + 1 = 1$$

a	b	Q_n
0	0	0
0	1	Q_{n-1}
1	0	Q_{n-1}
1	1	1

4.8.4 Circuit Output: GATE CSE 1993 | Question: 19

https://gateoverflow.in/2316



$A(t + 1) = D_a = A'B + A'P'$

$B(t + 1) = D_b = PB' + P'A$

Present State		Input	Next State	
A	B	P	A(t+1)	B(t+1)
0	0	0	1	0
0	0	1	0	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	0

Note: Recheck the table by putting the values of A , B and P in equations of $A(t+1)$ and $B(t+1)$.

👍 24 votes

-- Praveen Saini (41.9k points)

4.8.5 Circuit Output: GATE CSE 1993 | Question: 6-3 top 5

<https://gateoverflow.in/17237>



- ✓ Circuit behaves as shift register and mod 6 counter

Clock Cycle	Output
1	100
2	110
3	111
4	011
5	001
6	000

This is Johnson counter which is an application of Shift Register. And Johnson counter is mod 2N counter.

👍 50 votes

-- Pooja Palod (24.1k points)

4.8.6 Circuit Output: GATE CSE 1993 | Question: 6.1 top 5

<https://gateoverflow.in/2288>



- ✓ $(x + x'y').(y + x'y') = (x + y')(x' + y) = xy + x'y' = \text{Exclusive-NOR}$

👍 16 votes

-- Praveen Saini (41.9k points)

4.8.7 Circuit Output: GATE CSE 1993 | Question: 6.2 top 5

<https://gateoverflow.in/17235>



- ✓ If $a = 0$ state changes from S_1 to S_2 and if $b = 0$ state changes from S_2 to S_1 .

So, $a = 0, b = 0$ is surely not a stable state as then the states will be oscillating. So, the condition for stability is that both a and b should not be 0 together which is given by $a + b = 1$ or $\overline{ab} = 0$.

Options A and C are equivalent and both ensures stable states albeit by enforcing stricter than required conditions.

Correct Answer: Option B.

👍 13 votes

-- Arjun Suresh (332k points)

4.8.8 Circuit Output: GATE CSE 1994 | Question: 1.8 top 5

<https://gateoverflow.in/2445>



- ✓ $((AB)C)'(CD) = ((AB)C) + CD = (A' + B')C + CD = A'C + B'C + CD$

👍 39 votes

-- Arjun Suresh (332k points)

4.8.9 Circuit Output: GATE CSE 1994 | Question: 11 top 5

<https://gateoverflow.in/2507>



- ✓ Initial $Q_2 = 0, Q_1 = 0, Q_0 = 0$

Clock 1 :

- $Q_2 = 1$ [$J = (\text{old } Q_0)' = 1, K = 1, \text{New } Q_2 = \text{Complement of old } Q_2 = 1$]
- $Q_1 = 0$ [$D = \text{old } Q_2 = 0, \text{new } Q_1 = D = 0$]
- $Q_0 = 0$ [$T = \text{old } Q_1 = 0, \text{New } Q_0 = \text{old } Q_0 = 0$]

Clock 2 :

- $Q_2 = 0$ [$J = (\text{old } Q_0)' = 1, K = 1, \text{New } Q_2 = \text{Complement of old } Q_2 = 0$]
- $Q_1 = 1$ [$D = \text{old } Q_2 = 1, \text{new } Q_1 = D = 1$]
- $Q_0 = 0$ [$T = \text{old } Q_1 = 0, \text{New } Q_0 = \text{old } Q_0 = 0$]

Clock 3 :

- $Q_2 = 1$ [$J = (\text{old } Q_0)' = 1, K = 1, \text{New } Q_2 = \text{Complement of old } Q_2 = 1$]
- $Q_1 = 0$ [$D = \text{old } Q_2 = 0, \text{New } Q_1 = D = 0$]
- $Q_0 = 1$ [$T = \text{old } Q_1 = 1, \text{New } Q_0 = \text{complement of old } Q_0 = 1$]

Clock 4 :

- $Q_2 = 0$ [$J = (\text{old } Q_0)' = 0, K = 1, \text{new } Q_2 = \text{Reset} = 0$]
- $Q_1 = 1$ [$D = \text{old } Q_2 = 1, \text{new } Q_1 = D = 1$]
- $Q_0 = 1$ [$T = \text{old } Q_1 = 1, \text{new } Q_0 = \text{old } Q_0 = 1$]

After 4 clock pulses $Q_2Q_1Q_0$ is 011

Note : for JK flipflops, $Q_{(t+1)} = JQ' + K'Q$, for D flipflops, $Q_{(t+1)} = D$, and for T flipflops $Q_{(t+1)} = T \oplus Q$ Where $Q_{(t+1)}$ represent new value of Q .

👍 31 votes

-- Praveen Saini (41.9k points)

4.8.10 Circuit Output: GATE CSE 1996 | Question: 2.21 [top](#)

<https://gateoverflow.in/2750>



- ✓ Whenever, $b_2 = b_3 = 1$, then only 0100 i.e., 4 is added to the given binary number. Let's write all possibilities for b .

b_3	b_2	b_1	b_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Note that the last 4 combinations (1100, 1101, 1110, 1111) leads to b_3 and b_2 as 1. So, in these combinations only 0100 will be added.

1100 is 12
 1101 is 13
 1110 is 14
 1111 is 15
 in binary unsigned number system.

1100 + 0100 = 10000 .
 1101 + 0100 = 10001 and so on.
 This is conversion to radix 12.

Correct Answer: D

21 votes

-- Monanishi Jain (7k points)

4.8.11 Circuit Output: GATE CSE 1996 | Question: 24-a top

https://gateoverflow.in/2776



State Diagram :

$S_7 \rightarrow S_3 \rightarrow S_1 \rightarrow S_4 \rightarrow S_2 \rightarrow S_5 \rightarrow S_6 \rightarrow S_7$

b. Given the initial state S_4 , S_0 state will not be reachable. If the system enters S_0 state then $Q_0=Q_1=Q_2=0$ and after that it will stay in S_0 state indefinitely and can't go to any other state.

18 votes

-- shreya ghosh (2.8k points)

4.8.12 Circuit Output: GATE CSE 1996 | Question: 24-b top

https://gateoverflow.in/203691

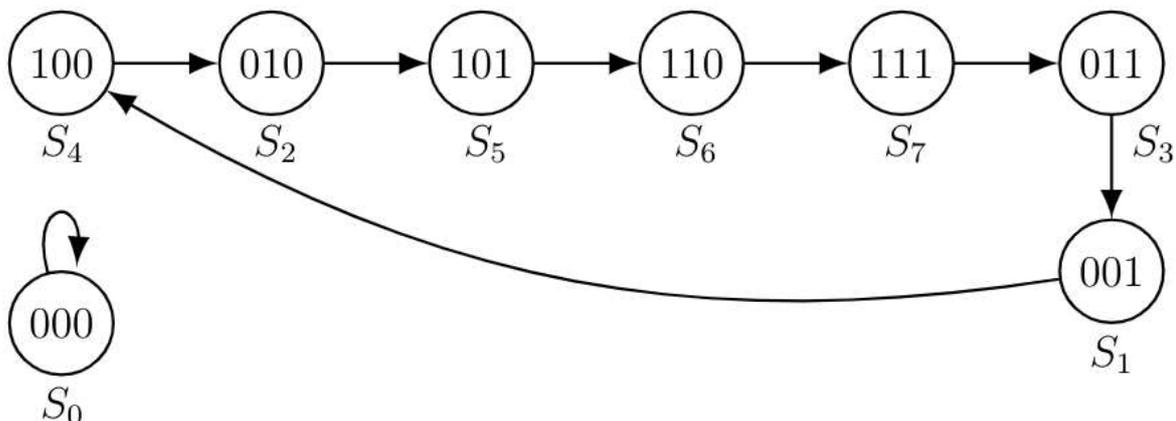


✓

- $Q_{3N} = D_3 \Rightarrow Q_{3N} = Q_2$
- $Q_{2N} = D_2 \Rightarrow Q_{2N} = Q_1$
- $Q_{1N} = D_1 \Rightarrow Q_{1N} = Q_3 \oplus Q_2$

Q_1	Q_2	Q_3	Q_{1N}	Q_{2N}	Q_{3N}
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	1

Given that the initial state = $S_4 = 100$.



Unreachable state is S_0

So, set of states which are not reachable = $\{S_0\}$

9 votes

classroom.gateoverflow.in
-- Pinaki Dash (1.5k points)

4.8.13 Circuit Output: GATE CSE 1997 | Question: 5.5 top 5

<https://gateoverflow.in/2256>



✓ $f = (f_1 \wedge f_2) \vee f_3$

Since f_1 and f_2 are in canonical sum of products form, $f_1 \wedge f_2$ will only contain their common terms- that is $f_1 \wedge f_2 = \Sigma 8$

Now, $\Sigma 8 \vee f_3 = \Sigma 8, 9$

So, $f_3 = \Sigma 9$

Correct Answer: B

31 votes

-- Arjun Suresh (332k points)

4.8.14 Circuit Output: GATE CSE 1999 | Question: 2.8 top 5

<https://gateoverflow.in/1486>



✓ The figure is not clear- I assume there is a NOT gate just before taking Y making the final AND gate a NAND gate.

We have a steady state- meaning output is not changing. Y is 1 and remains 1 in the next state(s). So, we can write

$$Y = ((\overline{AY}). B). C$$

$$1 = \overline{A}. B + \overline{C}$$

So, $C = 0$ or $\overline{A}. B = 1$

So, option B is TRUE.

19 votes

-- Arjun Suresh (332k points)

4.8.15 Circuit Output: GATE CSE 2000 | Question: 2.12 top 5

<https://gateoverflow.in/659>



✓ Here, clocks are applied to both flip flops simultaneously. Outputs for 3 cycles will proceed as follows:

- When 11 is applied to JK flip flop it toggles the value of P. So, output at P will be 1.
- Input to D flip flop will be 0 (initial value of P). So, output at Q will be 0.

JK flip flop it toggles the value of P. So, output at P will be 0.

- Input to D flip flop will be 1 (current value of P) . So, output at Q will be 1.

- JK flip flop it toggles the value of P. So, output at P will be 1.
- Input to D flip flop will be 0 (initial value of P) so output at Q will be 0.

So, answer is A.

56 votes

-- Pooja Palod (24.1k points)

4.8.16 Circuit Output: GATE CSE 2001 | Question: 2.8 top 5

<https://gateoverflow.in/726>



✓ Answer is (a).

Given clock is + edge triggered.

See the first positive edge. X is 0, and hence, the output is 0. Q_0 is 0 and Q'_0 is 1.

Second + edge, X is 1 and Q'_0 is also 1. So, output is 1. (When second positive edge of the clock arrives, Q'_0 would surely be 1 because the setup time of flip-flop is given as 20 ns and the clock period is ≥ 40 ns)

Third + edge, X is 1 and Q'_0 is 0, So, output is 0. (Q'_0 becomes 0 before the third positive edge, but output Y would not change)

as the flip-flop is positive edge triggered)

Now, output never changes back to 1 as Q_0' is always 0 and when Q_0' finally becomes 1, X is 0.

Set up time and hold times are given just to ensure that edge triggering works properly.

👍 50 votes

-- Arjun Suresh (332k points)

4.8.17 Circuit Output: GATE CSE 2002 | Question: 2.2 [top](#)

<https://gateoverflow.in/832>



- ✓ As x is connected to $I0$ & $I1$, y connected to $I2$, y' connected to $I3$ & $A1$, z connected to $A0$ and z' connected to ENABLE (EN),

$$f = (\overline{A1} \cdot \overline{A0} \cdot I0 + \overline{A1} \cdot A0 \cdot I1 + A1 \cdot \overline{A0} \cdot I2 + A1 \cdot A0 \cdot I3) \cdot EN$$

$$\begin{aligned} \implies f &= (xyz' + xyz + y'z'y + zy')z' \\ &= (xyz' + xyz + zy')z' = xyz' \end{aligned}$$

Correct Answer: A

👍 58 votes

-- Digvijay (44.9k points)

4.8.18 Circuit Output: GATE CSE 2004 | Question: 61 [top](#)

<https://gateoverflow.in/1056>



- ✓ Sequence is 0 – 2 – 3 – 1 – 0

From the given sequence, we have state table as

Q_2	Q_1	Q_2^+	Q_1^+
0	0	1	0
0	1	0	0
1	0	1	1
1	1	0	1

Now we have present state and next state, use excitation table of T flip-flop

Q_2	Q_1	Q_2^+	Q_1^+	T_2	T_1
0	0	1	0	1	0
0	1	0	0	0	1
1	0	1	1	0	1
1	1	0	1	1	0

From state table, $T_2 = Q_2 \odot Q_1$, and $T_1 = Q_2 \oplus Q_1$

$$X = T_1 = Q_2 \oplus Q_1$$

Correct Answer: D

👍 85 votes

-- Praveen Saini (41.9k points)

4.8.19 Circuit Output: GATE CSE 2005 | Question: 15 [top](#)

<https://gateoverflow.in/1351>



- ✓ The expression will be

$$f = [(x \cdot y)'] \cdot (y \cdot z)]' = [(x' + y) \cdot (y \cdot z)]' = [x' \cdot y \cdot z + y \cdot z]' = [(x' + 1) \cdot (y \cdot z)]' = [1 \cdot (y \cdot z)]' = [y \cdot z]' = y' + z'$$

The final expression only contains y and z ,

Therefore, answer will be (a) f is Independent of x

28 votes

-- jec.himanshu (189 points)

4.8.20 Circuit Output: GATE CSE 2005 | Question: 62 top

https://gateoverflow.in/264



✓

- $D = AX + X'Q'$
- $Y = D$

A_i represent the logic level on the line A at the i^{th} clock period. If we see the timing diagram carefully, we can see that during the rising edge, the output Y is determined by the X value just before that rising edge. i.e., during the rising edge say for clk2, X value that determines the output is 1 and not 0 (because it takes some propagation delay for the 0 to reach the flip flop). Similarly, the A output that determines the output for clk i , is A_{i-1} .

- For clk1, X is 1, so, $D = A = A_0$
- For clk2, X is 1, so $D = A = A_1$
- For clk3, X is 0, so $D = Q'_2 = A'_1$
- For clk4, X is 1, so $D = A = A_3$
- For clk5, X is 1, so $D = A = A_4$

So, answer is A choice.

69 votes

-- Arjun Suresh (332k points)

4.8.21 Circuit Output: GATE CSE 2005 | Question: 64 top

https://gateoverflow.in/1387



✓

Clearly, Q_0 alternates in every clk cycle as Q'_0 is fed as input and it is **D** flipflop. Q_1 becomes 1 if its prev value and current Q_0 differs (EXOR).

So, the sequence of transitions will be : 00 → 11 → 01 → 10 → 00 , (**D**) choice.

34 votes

-- Arjun Suresh (332k points)

4.8.22 Circuit Output: GATE CSE 2006 | Question: 35 top

https://gateoverflow.in/1292



✓

Result of MUX (first one), is, say $f_1 = x\bar{z} + \bar{y}z$
 Result of MUX(second one), $f = f_1\bar{y} + xy$

$$\begin{aligned}
 &= (x\bar{z} + \bar{y}z)\bar{y} + xy \\
 &= x\bar{y}\bar{z} + \bar{y}z + xy \\
 &= x(\bar{y}\bar{z} + y) + \bar{y}z \\
 &= x(\bar{y} + y)(\bar{z} + y) + \bar{y}z \\
 &= xz' + xy + y'z.
 \end{aligned}$$

Option A.

Note:

1. $f = I_0\bar{S} + I_1S$, for 2 : 1 MUX, where I_0 and I_1 are inputs, S is the select line
2. Distributive property, $A + BC = (A + B)(A + C)$
3. $A + \bar{A} = 1$

52 votes

-- Praveen Saini (41.9k points)

4.8.23 Circuit Output: GATE CSE 2006 | Question: 37 top

https://gateoverflow.in/1295



✓

Data	Q ₀	Q ₁	Q ₂
1	1	$Q_{0_{start}} \text{ XOR } Q_{2_{start}} = 0 \text{ XOR } 0 = 0$	$Q_{1_{start}} = 0$
0	0	$1 \text{ XOR } 0 = 1$	0
0	0	$0 \text{ XOR } 0 = 0$	1
1	1	$0 \text{ XOR } 1 = 1$	0
1	1	$1 \text{ XOR } 0 = 1$	1
0	0	$1 \text{ XOR } 1 = 0$	1
0	0	$0 \text{ XOR } 1 = 1$	0
0	0	$0 \text{ XOR } 0 = 0$	1
0	0	$0 \text{ XOR } 1 = 1$	0

So, option C.

40 votes

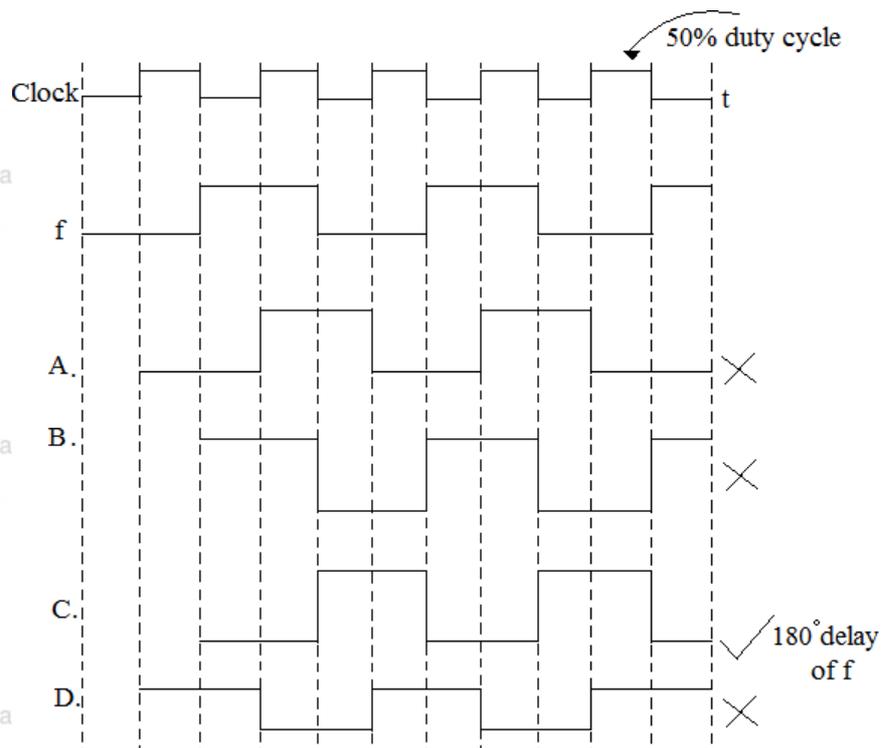
-- Arjun Suresh (332k points)

4.8.24 Circuit Output: GATE CSE 2006 | Question: 8 top 5

<https://gateoverflow.in/887>



Ans- C.



42 votes

-- Aaditya Pundir (361 points)

B and D are inverting f and hence cannot be the answer. gateoverflow.in

In A, the output is activated by CLK on the final D flip flop. So, the output will have the same phase as f.

In C, the output is activated by CLK', and since CLK is having 50% duty cycle, this should mean the output will now have a

phase difference of 180 degrees.

11 votes

-- Arjun Suresh (332k points)



Whenever $A_4A_3A_2A_1 = 0101$, clear line will be enabled as A_3 and A_1 are set.

Given table says that whenever clear control signal is set, it clears to 0000, before the current clock cycle completes.

So, 5 is cleared to 0 in the same clock cycle and counter sequence is 0, 1, 2, 3, 4

Hence, option C .

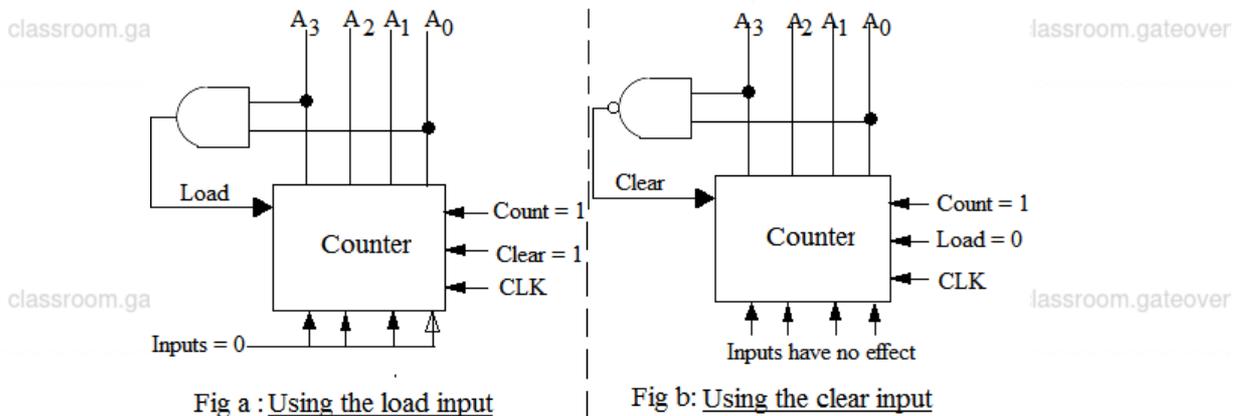
40 votes

-- pramod (2.8k points)

(C) is the correct answer!

Remark :

1. If $clear = 1$, counter will be reset to 0000 without any delay, and counter doesn't count 5 .
2. If $load = 1$, counter will be loaded with the input 0011, but note that counter counts 5 in this case unlike clear input.
3. Counter counts from 0 to 4.
4. Clear and Load are **direct inputs**, it means they can be applied to the counter without using any pulse.



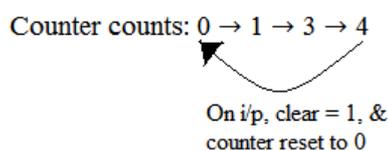
Two ways to achieve a BCD counter with parallel load

When the output reaches the count of 1001, both A_0 and A_3 become 1, making the output of the AND gate equal to 1. This condition activates the Load input; therefore, on the next clock edge the register does not count, but is loaded from its four inputs . Since all four inputs are connected to logic 0, an all-0's value is loaded into the register following the count of 1001. Thus, the circuit goes through the count from 0000 through 1001 and back to 0000, as is required in a BCD counter.

In Fig (b), the NAND gate detects the count of 1010, but as soon as this count occurs, the register is cleared. The count 1010 has no chance of staying on for any appreciable time, because the register goes immediately to 0

1. If $clear = 1$, then clear the counter.
2. If $clear = 0, load = 0, count = 1$, counter counts.
3. $load = 1$, loads the input to the counter.

If $load = 1$, then counter will be loaded with $i/p = 0011$ to the given counter, $count = 1, load = 0, clock = \uparrow$



Note: If o/p of AND gate is led to load, then counter will be loaded with 0011.

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-- Manu Thakur (34k points)

29 votes

4.8.26 Circuit Output: GATE CSE 2010 | Question: 31 top 5

https://gateoverflow.in/2205



✓ Level 1:

$$\overline{(P+Q)}\overline{(Q+R)}\overline{(P+R)}\overline{(Q+R)}$$

Level 2:

$$\overline{(P+Q)} + \overline{(Q+R)} = (P+Q)(Q+R) = PQ + PR + Q + QR$$

$$\overline{(P+R)}\overline{(Q+R)} = (P+R)(Q+R) = PQ + R + QR + PR$$

Level 3:

$$PR + QR + PQ + Q + R = Q + R \therefore \text{Answer: Option A}$$

24 votes

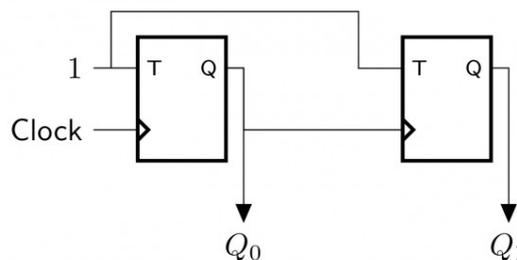
-- Sona Praneeth Akula (3.4k points)

4.8.27 Circuit Output: GATE CSE 2010 | Question: 32 top 5

https://gateoverflow.in/2206



✓ Option A.



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2nd flip-flop will be active only when 1st flip flop produces output 1. For clocks 2 and 4 old output is retained by Flip-Flop 2.

	T_0	Q_0	T_1	Q_1		Q_1	Q_0
		0		0		1	1
T	Q_{n+1}	1	1	1	1	1	1
0	Q_n	1	0	1	1	1	0
1	$\overline{Q_n}$	1	1	1	0	0	1
		1	0	1	0	0	0

For rows 2 and 4, Clk for T_1 is 0 and hence old o/p is retained

47 votes

-- Akhil Nadh PC (16.5k points)

4.8.28 Circuit Output: GATE CSE 2010 | Question: 9 top 5

https://gateoverflow.in/2182



$$\begin{aligned} f &= S'_0 S'_1 R + S'_0 S_1 R' + S_0 S'_1 R' + S_0 S_1 R \\ &= Q' P' R + Q' P R' + Q P' R' + Q P R \\ &= Q' (P \oplus R) + Q (P \oplus R)' \\ &= Q \oplus P \oplus R = P \oplus Q \oplus R \end{aligned}$$

Doing truth value substitution,

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P	Q	R	f	$P \oplus Q \oplus R$
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Correct Answer: B

32 votes

-- Arjun Suresh (332k points)

4.8.29 Circuit Output: GATE CSE 2011 | Question: 50 [top](#)

<https://gateoverflow.in/2157>



✓ Answer - D

As in D-flip-flop, next output is $Q^+ = D$

- $P_{i+1} = R_i$
- $Q_{i+1} = (P_i + R_i)'$
- $R_{i+1} = R_i' Q_i$

CLOCK	Inputs			Outputs		
	$D_1 = R$	$D_2 = (P + R)$	$D_3 = Q \bar{R}$	P	Q	R
1	0	1	0	0	1	0
2	0	1	1	0	1	1
3	1	0	0	1	0	0
4	0	0	0	0	0	0
5	0	1	0	0	1	0

So, total number of distinct outputs = 4.

28 votes

-- Ankit Rokde (6.9k points)

4.8.30 Circuit Output: GATE CSE 2011 | Question: 51 [top](#)

<https://gateoverflow.in/43318>



✓ Characteristic equation of D FF is, $Q(t+1) = D$

So, $P^+ = R$, $Q^+ = \overline{P + R}$, and $R^+ = Q \cdot R'$

Sequence of states will be as:

Clock Pulse	PQR
Initially	000
1	010
2	011
3	100
4	000

4 is the number of distinct states.

Correct Answer: B

27 votes

-- Praveen Saini (41.9k points)

4.8.31 Circuit Output: GATE CSE 2014 Set 3 | Question: 45 top

https://gateoverflow.in/2079



✓

Initial State			Input						Next State		
Q2	Q1	Q0	J2	K2	J1	K1	J0	K0	Q2'	Q1'	Q0'
0	0	0	1	0	0	1	0	1	1	0	0
1	0	0	1	0	1	0	0	1	1	1	0
1	1	0	0	0	1	0	1	1	1	1	1

Option C

39 votes

-- Gate_15_isHere (459 points)

4.8.32 Circuit Output: GATE IT 2005 | Question: 10 top

https://gateoverflow.in/3755



✓

If we look carefully, bulb will be ON when both switches S1 and S2 are in the same state, either off or on.

S1	S2	Bulb
0	0	On
0	1	Off
1	0	Off
1	1	On

This is Ex-NOR operation, hence (C) is the correct option.

53 votes

-- Manu Thakur (34k points)

4.8.33 Circuit Output: GATE IT 2005 | Question: 43 top

https://gateoverflow.in/3804



	A	B	C	Q1	Q2	Z	Comment
After 1 st Cycle	X	X	X	X	X	X	
After 2 nd Cycle	0	0	X	0	X	X	Q1 is 0 making A and B 0
After 3 rd Cycle	X	X	1	1	1	1	Z is 1 making Q1 and Q2 1, Either A or B is 1. Q1' of previous cycle is 1.

The filling is done in reverse order. Here, none of the options match. So, something wrong somewhere.

41 votes

-- Arjun Suresh (332k points)

4.8.34 Circuit Output: GATE IT 2006 | Question: 36 top

https://gateoverflow.in/3575



✓

Given expression:

$$xP + \bar{x}Q = f$$

$$\text{Or, } x(y \text{ op}_1 z) + \bar{x}(y \text{ op}_2 z) = f \rightarrow (1)$$

X	Y	Z	Output(f)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

x\yz	00	01	11	10
0	1	...
1	...	1	1	1

$$\begin{aligned}
 f &\implies xz + xy + yz \\
 &\implies xz + xy + (x + \bar{x})yz \\
 &\implies xz + xy + xyz + \bar{x}yz \\
 &\implies x(z + y + yz) + \bar{x}yz \\
 &\implies x[z + y(1 + z)] + \bar{x}(y \bullet z) \\
 &\implies x(z + y) + \bar{x}(y \bullet z) \quad \rightarrow (2)
 \end{aligned}$$

Comparing (1) and (2) we get,

$$OP_1 = +(OR)$$

$$OP_2 = \bullet(AND)$$

Correct Answer: D

👍 63 votes

-- Subhankar Das (357 points)

4.8.35 Circuit Output: GATE IT 2007 | Question: 38 [top](#)

<https://gateoverflow.in/3471>



✓ The final answer will come as:

$$\begin{aligned}
 &a' + c' + d' + a'c + ab + bc \\
 &= a'(c + 1) + c' + d' + ab + bc \\
 &= a' + c' + d' + ab + bc \\
 &= (a' + a)(a' + b) + (c' + c)(c' + b) + d' \\
 &= a' + b + c' + b + d' \\
 &= a' + b + c' + d'
 \end{aligned}$$

Option is C.

👍 29 votes

-- Manali (2.1k points)

4.8.36 Circuit Output: GATE IT 2007 | Question: 40 [top](#)

<https://gateoverflow.in/3473>



✓ Answer: (A)

The four bit register contains: 1011, 1101, 0110, 1011, 1101, **0110** after each shift.

👍 29 votes

-- Rajarshi Sarkar (27.9k points)



- ✓ To detect the fault, we should get an unexpected output. The final gate here is a NOR gate which produces output 0 if either of its inputs is 1 and else 1. i.e., the output will be 0 for inputs (0, 1), (1, 0) and (1, 1) and output will be 1 for (0, 0).

By grounding T is at 0. So, we can ignore the inputs (1, 0) and (0, 0) to the final NOR gate as they won't be detecting faults. Now, expected (1, 1) input will become (1, 0) due to grounding of T but produces same output 0 as for (1, 1). Hence this also cannot detect the defect. So, to detect the defect, the input to the final gate must be (0, 1) which is expected to produce a 0 but will produce a 1 due to grounding of T .

Now, for (0, 1) input for the final gate, we must have,

$$X_3 = X_4 = 1$$

But if $X_4 = 1$, the OR gate makes 1 output and we won't get (0, 1) input for the final gate. This means, no input sequence can detect the fault of the circuit.

Alternatively, we can write equation for the circuit as

$$(((x_1 \cdot x_2 \cdot x_3)' + x_4) + x_3 \cdot x_4)' = ((x_1 \cdot x_2 \cdot x_3)' + x_4)' \cdot (x_3 \cdot x_4)' = x_1 \cdot x_2 \cdot x_3 \cdot x_4' \cdot (x_3 + x_4) = x_1 \cdot x_2 \cdot x_3 \cdot x_4'$$

For the faulty circuit output will be

$$((x_1 \cdot x_2 \cdot x_3)' + x_4)' = x_1 \cdot x_2 \cdot x_3 \cdot x_4'$$

So, there is no effect of T being grounded here. Answer is D option.

👍 69 votes

-- Arjun Suresh (332k points)



- ✓ Answer: B

$$F = \overline{(\bar{x}\bar{z} + xz)} = x\bar{z} + \bar{x}z$$

👍 35 votes

-- Rajarshi Sarkar (27.9k points)

4.9

Conjunctive Normal Form (1) [top](#)

Which of the following is TRUE about formulae in Conjunctive Normal Form?

- For any formula, there is a truth assignment for which at least half the clauses evaluate to true.
- For any formula, there is a truth assignment for which all the clauses evaluate to true.
- There is a formula such that for each truth assignment, at most one-fourth of the clauses evaluate to true.
- None of the above.

gate2007-cse digital-logic normal conjunctive-normal-form

Answer 🗃

Answers: Conjunctive Normal Form



- ✓ Answer is **option A**.

To Prove: For any formula, there is a truth assignment for which at least half the clauses evaluate to true

Proof:

Consider an arbitrary truth assignment. For each of its clause i , introduce a random variable.

$$X_i = \begin{cases} 1 & \text{if clause } i \text{ is satisfied;} \\ 0 & \text{otherwise.} \end{cases}$$

Then, $X = \sum_i X_i$ is the number of satisfied clauses.

Given any clause c , it is unsatisfied only if all of its k constituent literals evaluates to false; as they are joined by OR operator coz the formula is in CNF.

Now, because each literal within a clause has a $\frac{1}{2}$ chance of evaluating to true independently of any of the truth value of any of the other literals, the probability that they are all false is $(\frac{1}{2})^k = \frac{1}{2^k}$.

Thus, the probability that c is satisfied(true) is $1 - \frac{1}{2^k}$

$$\text{So, } E(X_i) = 1 \times \left(1 - \frac{1}{2^k}\right) = 1 - \frac{1}{2^k}$$

This means that $E(X_i) \geq \frac{1}{2}$

(try putting arbitrary valid values of k to see that)

Summation on both sides to get $E(X)$,

Therefore, we have $E(X) = \sum_i E(X_i) \geq \frac{m}{2}$; where m is the number of clauses.

$E(X)$ represents expected number of satisfied(to true) clauses.

So, there must exist an assignment that satisfies(to true) at least half of the clauses.

👍 52 votes

-- Amar Vashishth (25.2k points)

4.10

Decoder (2) top ⚡

4.10.1 Decoder: GATE CSE 2007 | Question: 8, ISRO2011-31 top ⚡

https://gateoverflow.in/1206



How many 3-to-8 line decoders with an enable input are needed to construct a 6-to-64 line decoder without using any other logic gates?

- A. 7
- B. 8
- C. 9
- D. 10

gate2007-cse digital-logic normal isro2011 decoder

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Answer 🗳️

4.10.2 Decoder: GATE CSE 2020 | Question: 20 top ⚡

https://gateoverflow.in/333211



If there are m input lines and n output lines for a decoder that is used to uniquely address a byte addressable 1 KB RAM, then the minimum value of $m + n$ is _____.

gate2020-cse numerical-answers digital-logic decoder

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tests.gatecse.in

Answer 🗳️

Answers: Decoder

4.10.1 Decoder: GATE CSE 2007 | Question: 8, ISRO2011-31 top ⚡

https://gateoverflow.in/1206



✓ Answer is C:

To get 6 : 64 we need 64 o/p

We have 3 : 8 decode with 8 o/p. So, we need $64/8 = 8$ decoders.

Now, to select any of this 8 decoder we need one more decoder.

Total = $8 + 1 = 9$ decoders

👍 45 votes

-- jayendra (6.7k points)

4.10.2 Decoder: GATE CSE 2020 | Question: 20 top ⚡

https://gateoverflow.in/333211



✓ Given that we need to address every byte of a 1 KB RAM. Therefore 1K addresses are needed.

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By using decoder, output lines should be $n = 1\text{ K} = 1024$. This means we should have number of input lines, $m = \log_2 1024 = 10$.

Thus, $m + n = 10 + 1024 = 1034$.

👍 12 votes

-- Shaik Masthan (50.4k points)

4.11

Digital Circuits (7) top

4.11.1 Digital Circuits: GATE CSE 1992 | Question: 02-ii top

https://gateoverflow.in/556



All digital circuits can be realized using only

- A. Ex-OR gates
- B. Multiplexers
- C. Half adders
- D. OR gates

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gate1992

normal

digital-logic

digital-circuits

multiple-selects

Answer

4.11.2 Digital Circuits: GATE CSE 1996 | Question: 5 top

https://gateoverflow.in/2757



A logic network has two data inputs A and B , and two control inputs C_0 and C_1 . It implements the function F according to the following table.

C_1	C_0	F
0	0	$A + B$
0	1	$A + B$
1	0	$A \oplus B$

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Implement the circuit using one 4 to 1 Multiplexer, one 2-input Exclusive OR gate, one 2-input AND gate, one 2-input OR gate and one Inverter.

gate1996

digital-logic

normal

digital-circuits

descriptive

Answer

4.11.3 Digital Circuits: GATE CSE 2002 | Question: 7 top

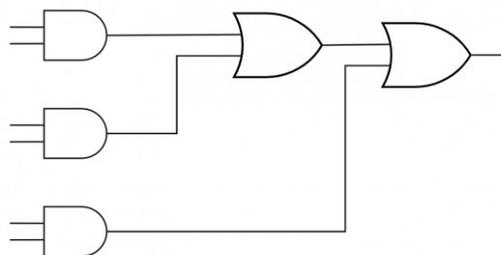
https://gateoverflow.in/860



- A. Express the function $f(x, y, z) = xy' + yz'$ with only one complement operation and one or more AND/OR operations. Draw the logic circuit implementing the expression obtained, using a single NOT gate and one or more AND/OR gates.
- B. Transform the following logic circuit (without expressing its switching function) into an equivalent logic circuit that employs only 6 NAND gates each with 2-inputs.

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gate2002-cse

digital-logic

normal

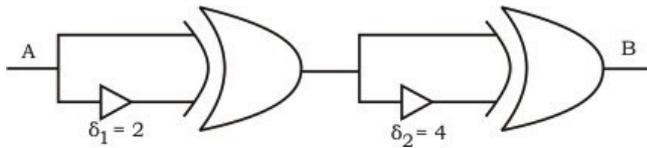
descriptive

digital-circuits

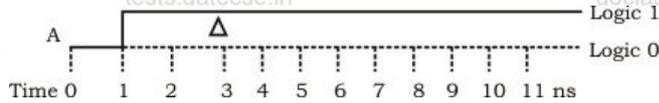
Answer



Consider the following circuit composed of XOR gates and non-inverting buffers.



The non-inverting buffers have delays $\delta_1 = 2ns$ and $\delta_2 = 4ns$ as shown in the figure. Both XOR gates and all wires have zero delays. Assume that all gate inputs, outputs, and wires are stable at logic level 0 at time 0. If the following waveform is applied at input A , how many transition(s) (change of logic levels) occur(s) at B during the interval from 0 to 10 ns?



- A. 1
- B. 2
- C. 3
- D. 4

gate2003-cse digital-logic digital-circuits

Answer



Which one of the following circuits is **NOT** equivalent to a 2-input *XNOR* (exclusive *NOR*) gate?

- A.
- B.
- C.
- D.

gate2011-cse digital-logic normal digital-circuits

Answer



In the following truth table, $V = 1$ if and only if the input is valid.

Inputs				Outputs		
D_0	D_1	D_2	D_3	X_0	X_1	V
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	1	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

What function does the truth table represent?

- A. Priority encoder
- B. Decoder
- C. Multiplexer
- D. Demultiplexer

gate2013-cse digital-logic normal digital-circuits

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Answer

4.11.7 Digital Circuits: GATE CSE 2014 Set 3 | Question: 8 [top](#) 

Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

```
f(x, a, b, y)
{
  if(x is 1) y = a;
  else y = b;
}
```

Which one of the following digital logic blocks is the most suitable for implementing this function?

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- A. Full adder
- B. Priority encoder
- C. Multiplexor
- D. Flip-flop

gate2014-cse-set3 digital-logic easy digital-circuits

Answer

Answers: Digital Circuits

4.11.1 Digital Circuits: GATE CSE 1992 | Question: 02-ii [top](#) 

✓ Answer: B, C [gateoverflow.in](#)

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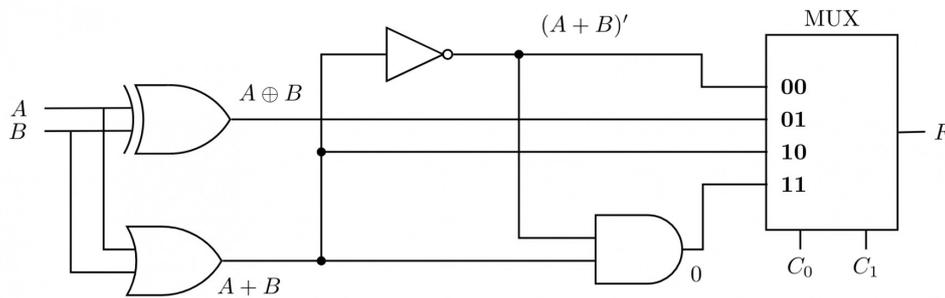
NOR gate, NAND gate, Multiplexers and Half adders can also be used to realise all digital circuits.

👍 19 votes

-- Rajarshi Sarkar (27.9k points)

4.11.2 Digital Circuits: GATE CSE 1996 | Question: 5 [top](#) 

✓



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This is the implementation asked in question

- $C_0 = 0, C_1 = 0$ line 00 will be selected and F will give $(A + B)'$
- $C_0 = 0, C_1 = 1$ line 01 will be selected and F will give $(A \oplus B)$
- $C_0 = 1, C_1 = 0$ line 10 will be selected and F will give $(A + B)$
- $C_0 = 1, C_1 = 1$ line 11 will be selected and F will give $(A + B)' \cdot (A + B) = 0$

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👍 26 votes

-- Praveen Saini (41.9k points)



✓ $f(x, y, z) = xy' + yz' = xy'z' + xy'z + x'yz' + xyz'$
 $f(x, y, z) = \sum_m(2, 4, 5, 6)$

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	yz	00	01	11	10
x	0	0	0	0	1
1	1	1	0	1	

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K-map
gateoverflow.in

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By pairing of 1's, we get two pairs (2, 6), (4, 5) resulting in same expression $F = xy' + yz'$

But by pairing of 0's, we get two pairs (0, 1), (2, 7), we get $F' = yz + x'y'$

Take complement, $F = \overline{(yz) \cdot (x + y)}$

so we can implement the function with 1 NOT, 1 OR and 2 AND gates.

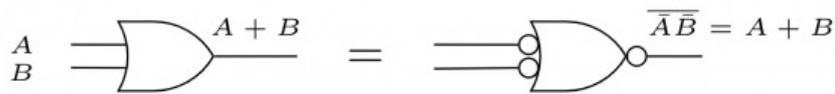
For the second part, we need to implement given circuit using NANDs only.

so best way is to replace OR with Invert NAND, $A + B = \overline{\overline{A}\overline{B}}$

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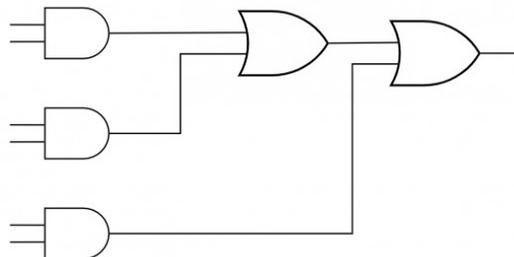
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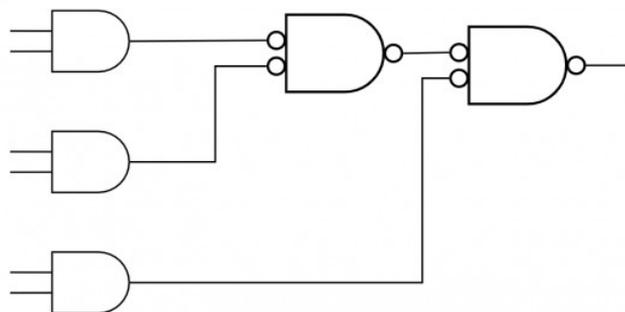
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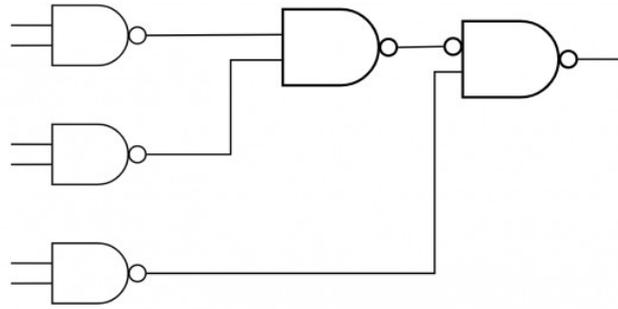
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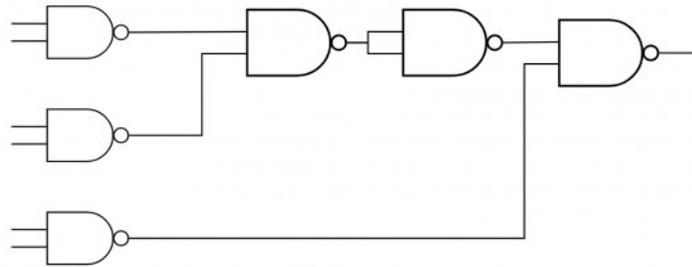
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44 votes

-- Praveen Saini (41.9k points)

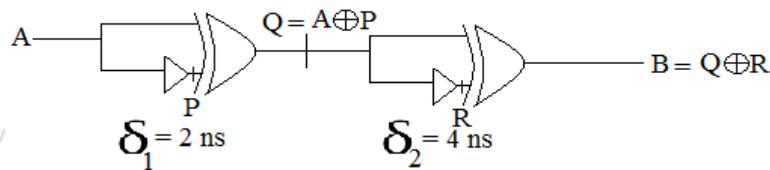
4.11.4 Digital Circuits: GATE CSE 2003 | Question: 47 [top](#)

<https://gateoverflow.in/29098>



✓

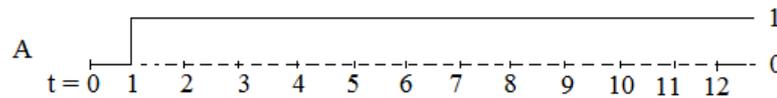
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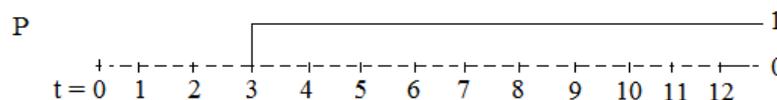
Let us plot the logic states at the various points of interests in this circuit.

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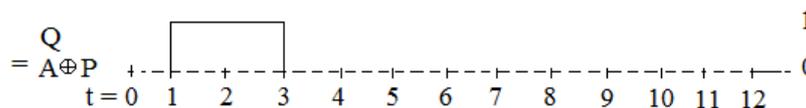
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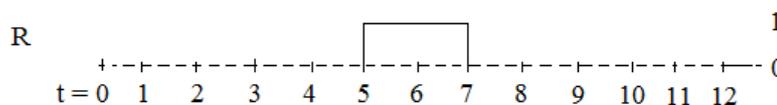
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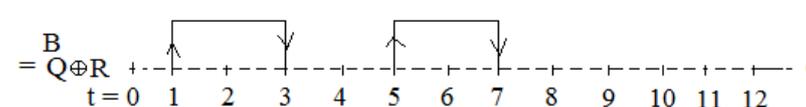
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Explanation :

Note that,  is not an inverter but a buffer used for introducing delay.

∴ Output at 'P' and 'R' will be obtained at 2 ns and 4 ns respectively after the change in their inputs.

Hence, waveforms of 'P' and 'R' are shifted by 2 ns and 4 ns as compared to their inputs.

Also, note that 'Q' and 'B' are plotted using their corresponding input waveforms.

Finally, we can see that there are 4 changes in logic levels in the waveforms of 'B'.

Answer is : Option D

👍 108 votes

-- tvkkk (1.1k points)

4.11.5 Digital Circuits: GATE CSE 2011 | Question: 13 top

<https://gateoverflow.in/2115>



✓

- A. $(AB' + A'B)' = A \odot B$
- B. $(A'(B')' + (A')'B')' = (A \oplus B)' = A \odot B$
- C. $A'B' + (A')'B = A \odot B$
- D. $((AB')'.(A + B'))' = (AB') + (A + B')' = AB' + A'B = A \oplus B$

So, Answer is (D)

👍 26 votes

-- srestha (85.2k points)

4.11.6 Digital Circuits: GATE CSE 2013 | Question: 5 top

<https://gateoverflow.in/1414>



✓

Answer is A.

For 2^n inputs we are having n outputs. Here $n=2$.

http://en.wikipedia.org/wiki/Priority_encoder

References



👍 27 votes

-- Sona Praneeth Akula (3.4k points)

4.11.7 Digital Circuits: GATE CSE 2014 Set 3 | Question: 8 top

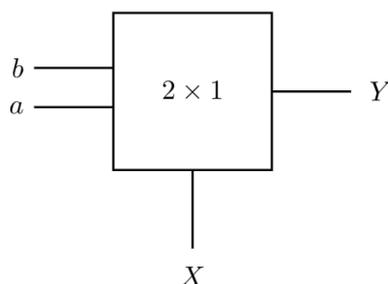
<https://gateoverflow.in/2042>



✓

If $X = 1$ $Y = a$;
else $(X = 0)$ $Y = b$;

Input : (a, b, X) Output : Y



$$Y = \bar{X}b + Xa.$$

4.12

Digital Counter (10) top

4.12.1 Digital Counter: GATE CSE 1987 | Question: 10c top

https://gateoverflow.in/82452



Give a minimal DFA that performs as a $\text{mod } -3$, 1's counter, i.e. outputs a 1 each time the number of 1's in the input sequence is a multiple of 3.

gate1987 digital-logic digital-counter descriptive

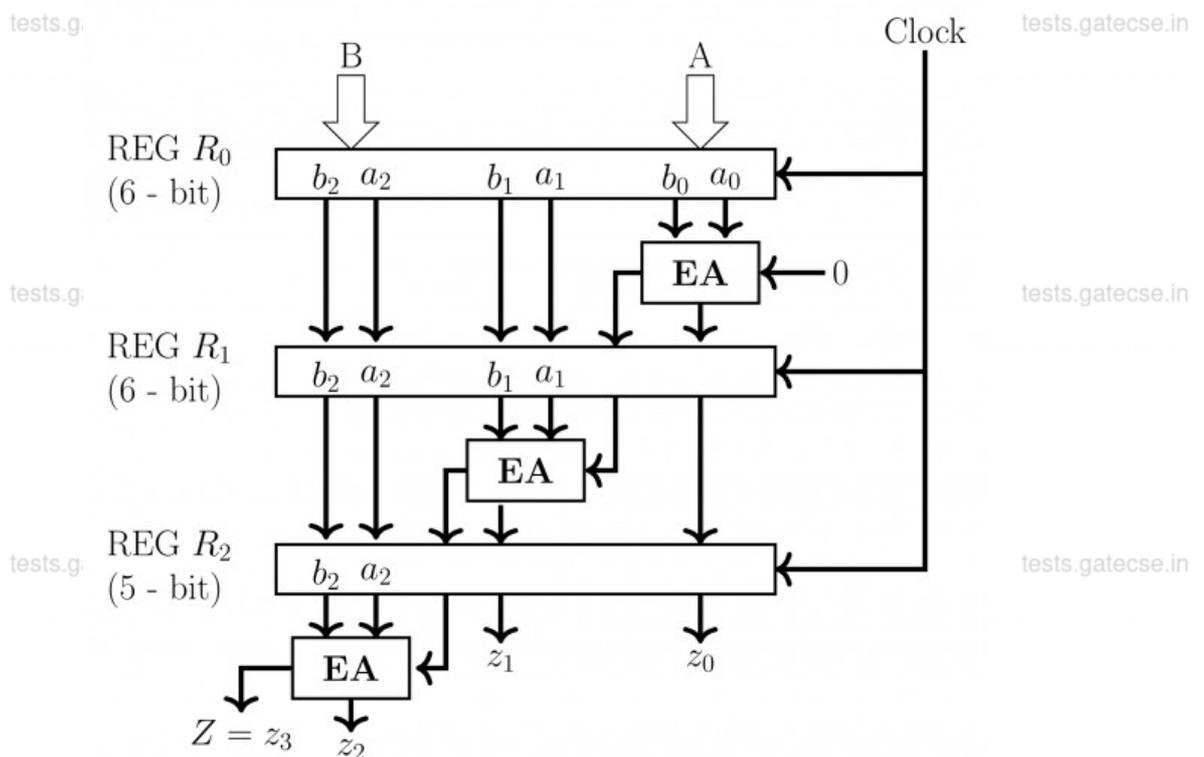
Answer

4.12.2 Digital Counter: GATE CSE 2002 | Question: 8 top

https://gateoverflow.in/861



Consider the following circuit. $A = a_2a_1a_0$ and $B = b_2b_1b_0$ are three bit binary numbers input to the circuit. The output is $Z = z_3z_2z_1z_0$. R_0 , R_1 and R_2 are registers with loading clock shown. The registers are loaded with their input data with the falling edge of a clock pulse (signal CLOCK shown) and appears as shown. The bits of input number A, B and the full adders are as shown in the circuit. Assume Clock period is greater than the settling time of all circuits.



a. For 8 clock pulses on the CLOCK terminal and the inputs A, B as shown, obtain the output Z (sequence of 4-bit values of Z). Assume initial contents of R_0, R_1 and R_2 as all zeros.

A	110	011	111	101	000	000	000	000
B	101	101	011	110	000	000	000	000
Clock No	1	2	3	4	5	6	7	8

b. What does the circuit implement?

gate2002-cse digital-logic normal descriptive digital-counter

Answer



The minimum number of D flip-flops needed to design a mod-258 counter is

- A. 9
- B. 8
- C. 512
- D. 258

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gate2011-cse digital-logic normal digital-counter

Answer



Let $k = 2^n$. A circuit is built by giving the output of an n -bit binary counter as input to an n -to- 2^n bit decoder. This circuit is equivalent to a

- A. k -bit binary up counter.
- B. k -bit binary down counter.
- C. k -bit ring counter.
- D. k -bit Johnson counter.

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gate2014-cse-set2 digital-logic normal digital-counter

Answer



Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

- A. 0, 1, 3, 7, 15, 14, 12, 8, 0
- B. 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
- C. 0, 2, 4, 6, 8, 10, 12, 14, 0
- D. 0, 8, 12, 14, 15, 7, 3, 1, 0

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gate2015-cse-set1 digital-logic digital-counter easy

Answer



The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0, 0, 1, 1, 2, 2, 3, 3, 0, 0, ...) is _____.

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gate2015-cse-set2 digital-logic digital-counter normal numerical-answers

Answer



We want to design a synchronous counter that counts the sequence 0 – 1 – 0 – 2 – 0 – 3 and then repeats. The minimum number of J-K flip-flops required to implement this counter is _____

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gate2016-cse-set1 digital-logic digital-counter flip-flop normal numerical-answers

Answer



The next state table of a 2-bit saturating up-counter is given below.

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Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expressions for T_1 and T_0 are

- A. $T_1 = Q_1 Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
 B. $T_1 = \bar{Q}_1 Q_0, T_0 = \bar{Q}_1 + \bar{Q}_0$
 C. $T_1 = Q_1 + Q_0, T_0 = \bar{Q}_1 \bar{Q}_0$
 D. $T_1 = Q_1 Q_0, T_0 = Q_1 + Q_0$

gate2017-cse-set2 digital-logic digital-counter

Answer

4.12.9 Digital Counter: GATE IT 2005 | Question: 11

https://gateoverflow.in/3756



How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

- A. 134
 B. 133
 C. 124
 D. 123

gate2005-it digital-logic digital-counter normal

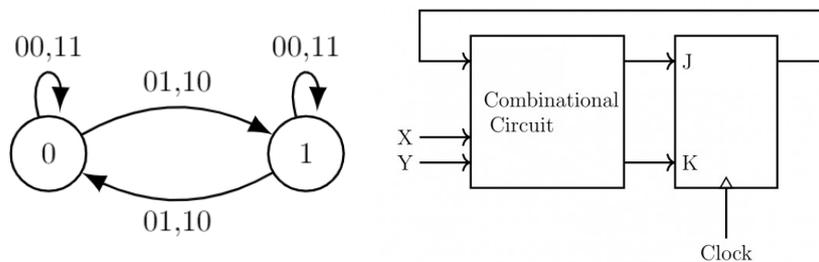
Answer

4.12.10 Digital Counter: GATE IT 2008 | Question: 37

https://gateoverflow.in/3747



Consider the following state diagram and its realization by a JK flip flop



The combinational circuit generates J and K in terms of x, y and Q. The Boolean expressions for J and K are :

- A. $\overline{x \oplus y}$ and $\overline{x \oplus y}$
 B. $x \oplus y$ and $x \oplus y$
 C. $x \oplus y$ and $\overline{x \oplus y}$
 D. $x \oplus y$ and $x \oplus y$

gate2008-it digital-logic boolean-algebra normal digital-counter

Answer

Answers: Digital Counter

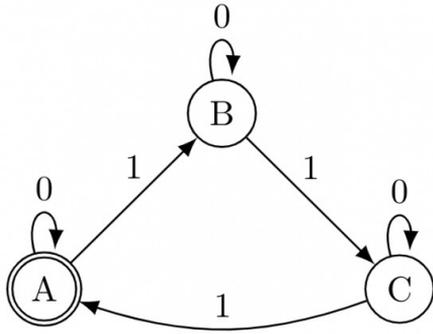
4.12.1 Digital Counter: GATE CSE 1987 | Question: 10c

https://gateoverflow.in/82452

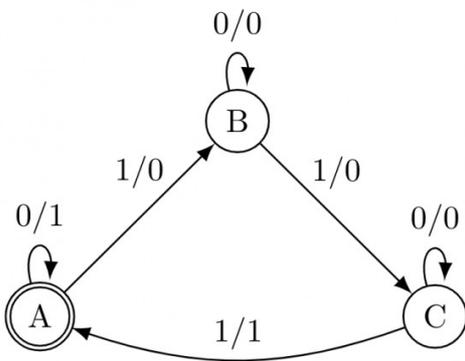


- ✓ Since it is given that the minimal DFA outputs 1 \implies we have to make a minimal DFA and then convert it into mealy/moore machine by associating output with each input or state.

the minimal DFA will be as shown below :-



I am associating output with each input i.e. creating a mealy machine. It will print 1 each time the number of 1's in the input sequence is a multiple of 3.



7 votes

-- Satbir Singh (21k points)

4.12.2 Digital Counter: GATE CSE 2002 | Question: 8

<https://gateoverflow.in/861>



(A)

	output Z
Clock-1	0000
Clock-2	0000
Clock-3	1011
Clock-4	1000
Clock-5	1010
Clock-6	1011
Clock-7	0000
Clock-8	0000

(B) The circuit is a 3 – bit ripple binary adder.

9 votes

-- Himanshu Agarwal (12.4k points)

4.12.3 Digital Counter: GATE CSE 2011 | Question: 15

<https://gateoverflow.in/2117>



Mod 258 counter has 258 states. We need to find no. of bits to represent 257 at max. $2^n \geq 258 \implies n \geq 9$.

Answer is A.

28 votes

-- Sona Praneeth Akula (3.4k points)



- ✓ Binary counter of n bits can count up to 2^n numbers. When this output from counter is fed as input (n bit) to decoder one out of 2^n output lines will be activated. So, this arrangement of counter and decoder is behaving as 2^n or k – bit ring counter.

Correct Answer: C

👍 36 votes

-- Pooja Palod (24.1k points)



- ✓ Johnson Counter is a **switch-tail ring counter** in which a **circular shift register** with the complemented output of the last flip-flop connected to the input of the first flip-flop.

(D) is the correct answer!

👍 25 votes

-- Manu Thakur (34k points)



- ✓ First, lets design a counter for 0, 1, 2, 3. It is a MOD - 4 counter. Hence, number of Flip Flops required will be two. Count sequence will be:

00 → 01 → 10 → 11

Count sequence mentioned in question is:

00 → 00 → 01 → 01 → 10 → 10 → 11 → 11

Now, two flip flops won't suffice. Since we are confronted with repeated sequence, we may add another bit to the above sequence:

000 → 100 → 001 → 101 → 010 → 110 → 011 → 111

Now each and every count is unique, occurring only once. Meanwhile, our machine has been extended to a MOD - 8 counter. Hence, three Flip Flops suffice.

Just neglect the MSB flip flop output and take the o/p of other two only. So, we have :

0, 0, 1, 1, 2, 2, 3, 3, . . .

So, correct answer: 3.

👍 151 votes

-- Mithlesh Upadhyay (4.3k points)



- ✓ We need four JK flipflops.

0 → 1 → 0 → 2 → 0 → 3

0000 → 0001 → 0100 → 0010 → 1000 → 0011

There are 6 states and 3 of them correspond to same states.

To differentiate between 0, 1, 2, 3 we need 2 bits.

To differentiate between 3 0's we need another 2 bits.

So, total 4 – bits → 4FFs

Edit:

whether using extra combinational logic for output is allowed in a counter?

Page No. 10/11 <http://textofvideo.nptel.iitm.ac.in/117105080/lec23.pdf> or [archive](#)

Now, if you see the counters, now a counter we can define in this way the counter is a degenerate finite state machine, where the **state is the only** output. So, there is **no other primary output** from this machine, so the counter is defined like that.

ALSO

Page No. 3 <http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf> or [archive](#)

Counter you know what counter it is, that's what we want we count the output of counter what is the particular count what is the current count that is the output of a count so no external output. **The counter is a case of a state machine in which there are no external inputs, no external outputs.**

Page No. 10 <http://textofvideo.nptel.iitm.ac.in/117106086/lec24.pdf> or [archive](#)

always do that let us say 1 0 0 you want count twice you can put 1 0 0 to 1 0 0 but then when you draw the Karnaugh Map you don't know which 1 0 0 you are talking about so instead of doing that you can have an external input defined when x is equal to 0 it remains there so you can put x is equal to 0 and for all of those x is equal to 1. So from S_0 to S_1 it will remain, both 0 and 1 it will take here, from here it will take here only if x is equal to 1 and if x is equal to 0 it will remain here so external input can be used more elegantly for that design.

At 35:30 www.youtube.com/watch?v=MiuMYEn3dpg

Here In Counter, we cannot use external variable, that purpose will be served by FF's only We have four distinct states 0, 1, 2, 3 so, 2FF for them for 3 0's to distinguish we need 2 more FF's <http://www.youtube.com/watch?v=MiuMYEn3dpg>

4FF required.

References



118 votes

-- Abhilash Panicker (7.6k points)

4.12.8 Digital Counter: GATE CSE 2017 Set 2 | Question: 42 [top](#)

<https://gateoverflow.in/11857>



✓ Answer is B)

Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_2
0	0	0	1	0	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	0	0

By using above excitation table,

$$T_1 = Q_1'Q_0,$$

$$T_2 = (Q_1Q_0)' = Q_1' + Q_0'$$

23 votes

-- jatin sainsi (4.2k points)

4.12.9 Digital Counter: GATE IT 2005 | Question: 11 [top](#)

<https://gateoverflow.in/3756>



✓ D.123 Pulses.

As in a 2^8 Counter, the range would be from 0 – 255. Hence to go from 10101100(172) to 00100111(39), the counter has to go initially from 172 to 255 and then from 0 to 39.

Hence to go from 172 to 255, $255 - 172 = 83$ Clock pulses would be required. then from 255 to 0, again 1 clock pulse would be required. Then, from 0 to 39, 39 clock pulses would be required. Hence in total $83 + 1 + 39 = 123$ Clock pulses would be

required.

73 votes

-- Afaque Ahmad (727 points)

4.12.10 Digital Counter: GATE IT 2008 | Question: 37

https://gateoverflow.in/3347



From state diagram:

Q	X	Y	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	1	X
0	1	0	1	1	X
0	1	1	0	0	X
1	0	0	1	X	0
1	0	1	0	X	1
1	1	0	0	X	1
1	1	1	1	X	0

Excitation table of JK

Q	Q_{n+1}	J	K
0	0	0	d
0	1	1	d
1	0	d	1
1	1	d	0

XY	00	01	11	10
Q				
0		1		1
1	X	X	X	X

$J = X'Y + XY' = X \oplus Y$

XY	00	01	11	10
Q				
0	X	X	X	X
1		1		1

$K = X'Y + XY' = X \oplus Y$

Option D.

71 votes

-- Riya Roy(Arayana) (5.3k points)

4.13

Dual Function (1)

4.13.1 Dual Function: GATE CSE 2014 Set 2 | Question: 6

https://gateoverflow.in/1958



The dual of a Boolean function $F(x_1, x_2, \dots, x_n, +, \cdot, ')$, written as F^D is the same expression as that of F with $+$ and \cdot swapped. F is said to be self-dual if $F = F^D$. The number of self-dual functions with n Boolean variables is

- A. 2^n
- B. 2^{n-1}
- C. 2^{2^n}
- D. $2^{2^{n-1}}$

gate2014-cse-set2 digital-logic normal dual-function

Answer

Answers: Dual Function



- ✓ A function is self dual if it is equal to its dual (A dual function is obtained by interchanging . and +).

For self-dual functions,

1. Number of min terms equals number of max terms
2. Function should not contain two complementary minterms - whose sum equals $2^n - 1$, where n is the number of variables.

	A	B	C
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

So, here (0, 7)(1, 6)(2, 5)(3, 4) are complementary terms so in self-dual we can select any one of them but not both.

Totally $2 \times 2 \times 2 \times 2 = 2^4$ possibility because say from (0, 7) we can pick anyone in minterm but not both.

For example, let $f = \sum(0, 6, 2, 3)$

NOTE: here I have taken only one of the complementary term for min term from the sets.

So, remaining numbers will go to MAXTERMS

For above example, $2^4 = 16$ self dual functions are possible

So, if we have N variables, total Minterms possible is 2^n

Then half of them we selected so 2^{n-1} .

Now we have 2 choices for every pair for being selected.

So total such choices = $\underbrace{2 \times 2 \times 2 \times 2 \dots 2}_{2^{n-1} \text{ times}}$

$\therefore 2^{2^{n-1}}$ (option D)

👍 64 votes

-- Kalpish Singhal (1.6k points)

4.14

Fixed Point Representation (2) top

4.14.1 Fixed Point Representation: GATE CSE 2017 Set 1 | Question: 7 top

<https://gateoverflow.in/118287>

The n -bit fixed-point representation of an unsigned real number X uses f bits for the fraction part. Let $i = n - f$. The range of decimal values for X in this representation is

- 2^{-f} to 2^i
- 2^{-f} to $(2^i - 2^{-f})$
- 0 to 2^i
- 0 to $(2^i - 2^{-f})$

gate2017-cse-set1

digital-logic

number-representation

fixed-point-representation

Answer

4.14.2 Fixed Point Representation: GATE CSE 2018 | Question: 33 top

<https://gateoverflow.in/204107>

Consider the unsigned 8-bit fixed point binary number representation, below,

$$b_7 b_6 b_5 b_4 b_3 \cdot b_2 b_1 b_0$$

where the position of the primary point is between b_3 and b_2 . Assume b_7 is the most significant bit. Some of the decimal numbers

listed below **cannot** be represented **exactly** in the above representation:

- i. 31.500
- ii. 0.875
- iii. 12.100
- iv. 3.001

Which one of the following statements is true?

- A. None of *i*, *ii*, *iii*, *iv* can be exactly represented
- B. Only *ii* cannot be exactly represented
- C. Only *iii* and *iv* cannot be exactly represented
- D. Only *i* and *ii* cannot be exactly represented

gate2018-cse digital-logic number-representation fixed-point-representation normal

Answer

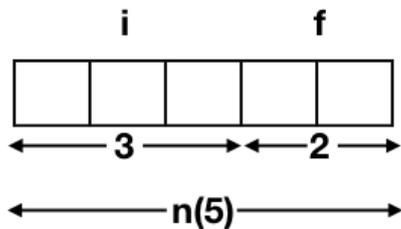
Answers: Fixed Point Representation

4.14.1 Fixed Point Representation: GATE CSE 2017 Set 1 | Question: 7

<https://gateoverflow.in/118287>

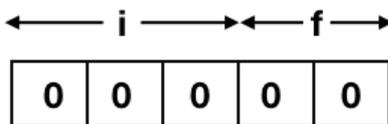


Unsigned real number x .



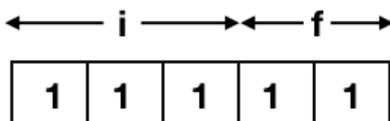
Let $n = 5, f = 2, i = 5 - 2 = 3$.

1. Minimum value of x :



Value on decimal = 0.

2. Maximum value of x :



Value on decimal = $2^3 - 2^{-2} = 8 - 0.25 = 7.75$ (Or $2^2 + 2^1 + 2^0 + 2^{-1} + 2^{-2} = 7.75$)

So (D) is the answer.

92 votes

-- 2018 (5.5k points)

4.14.2 Fixed Point Representation: GATE CSE 2018 | Question: 33

<https://gateoverflow.in/204107>



✓ 31.500 can be represented as 11111.100 in the above mentioned fixed form representation

0.875 can be represented as 00000.111.

We can't represent 3 and 4.

Hence, C is the correct answer.

4.15

Flip Flop (6) top

4.15.1 Flip Flop: GATE CSE 2001 | Question: 11 top

<https://gateoverflow.in/752>

A sequential circuit takes an input stream of $0's$ and $1's$ and produces an output stream of $0's$ and $1's$. Initially it replicates the input on its output until two consecutive $0's$ are encountered on the input. From then onward, it produces an output stream, which is the bit-wise complement of input stream until it encounters two consecutive $1's$, whereupon the process repeats. An example input and output stream is shown below.

The input stream:	101100		01001011		011
The desired output:	101100		10110100		011

J-K master-slave flip-flops are to be used to design the circuit.

- Give the state transition diagram
- Give the minimized sum-of-product expression for J and K inputs of one of its state flip-flops

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gate2001-cse digital-logic normal descriptive flip-flop

Answer

4.15.2 Flip Flop: GATE CSE 2004 | Question: 18, ISRO2007-31 top

<https://gateoverflow.in/1015>

In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

- $Q = 0, Q' = 1$
- $Q = 1, Q' = 0$
- $Q = 1, Q' = 1$
- Indeterminate states

gate2004-cse digital-logic easy isro2007 flip-flop

Answer

4.15.3 Flip Flop: GATE CSE 2015 Set 1 | Question: 37 top

<https://gateoverflow.in/8287>

A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip-flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip-flops are connected to a free-running common clock? Assume that $J = K = 1$ is the toggle mode and $J = K = 0$ is the state holding mode of the JK flip-flops. Both the flip-flops have non-zero propagation delays.

- 0110110...
- 0100100...
- 011101110...
- 011001100...

gate2015-cse-set1 digital-logic flip-flop normal

Answer

4.15.4 Flip Flop: GATE CSE 2017 Set 1 | Question: 33 top

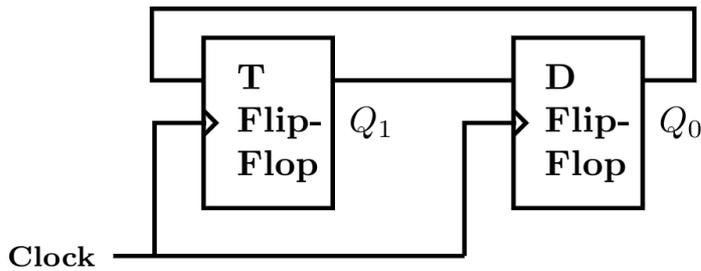
<https://gateoverflow.in/118315>

Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T flip-flop is connected to the input of the D flip-flop.

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Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs

- A. Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively.
- B. Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively.
- C. Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively.
- D. Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively.

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gate2017-cse-set1 digital-logic flip-flop normal

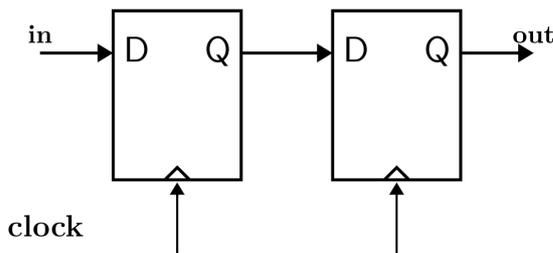
Answer

4.15.5 Flip Flop: GATE CSE 2018 | Question: 22

https://gateoverflow.in/204096



Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops.



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The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is ____

gate2018-cse digital-logic flip-flop numerical-answers normal

Answer

4.15.6 Flip Flop: GATE IT 2007 | Question: 7

https://gateoverflow.in/3440



Which of the following input sequences for a cross-coupled $R - S$ flip-flop realized with two $NAND$ gates may lead to an oscillation?

- A. 11, 00
- B. 01, 10
- C. 10, 01
- D. 00, 11

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gate2007-it digital-logic normal flip-flop

Answer

Answers: Flip Flop

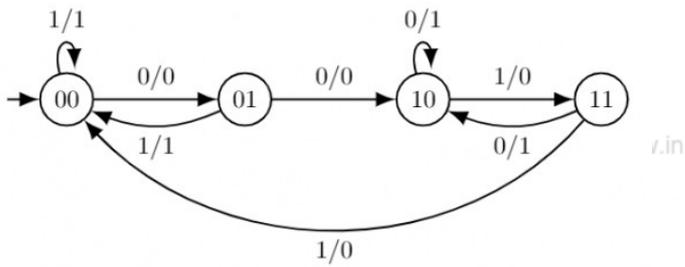
4.15.1 Flip Flop: GATE CSE 2001 | Question: 11

https://gateoverflow.in/752



✓ We can design a Mealy Machine as per the requirement given in the question.

From which we will get state table, and we can design sequential circuit using any Flip-flop from the state table (with the help of excitation table) :gateoverflow.in gateoverflow.in classroom.gateoverl



As we get 4 states (renaming state component to binary states), we need two FFs to implement it.

Let A and B be present states, x be the input and y be the output.

Present State	Input	Next State	Output	FF inputs		FF inputs	
AB	X	$A'B'$	Y	J_A	K_A	J_B	K_B
00	0	01	0	0	X	1	X
00	1	00	1	0	X	0	X
01	0	10	0	1	X	X	1
01	1	00	1	0	X	X	1
10	0	10	1	X	0	0	X
10	1	11	0	X	0	1	X
11	0	10	1	X	0	X	1
11	1	00	0	X	1	X	1

Q_t	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

BX	00	01	11	10
0				1
1	X	X	X	X

$$J_A = BX'$$

BX	00	01	11	10
0	X	X	X	X
1			1	

$$K_A = BX$$

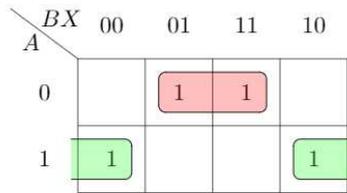
BX	00	01	11	10
0	1		X	X
1		1	X	X

$$J_B = A'X' + AX$$

$$J_B = A \odot X$$

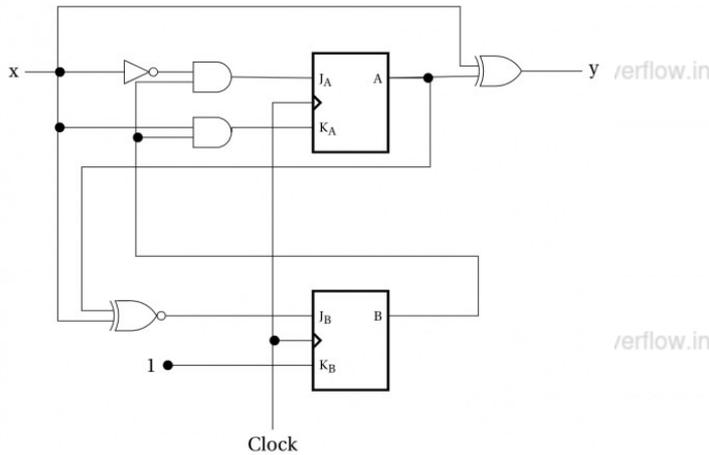
BX	00	01	11	10
0	X	X	1	1
1	X	X	1	1

$$K_B = 1$$



$$Y = A'X + AX'$$

$$Y = A \oplus X$$



29 votes

-- Praveen Saini (41.9k points)

4.15.2 Flip Flop: GATE CSE 2004 | Question: 18, ISRO2007-31

<https://gateoverflow.in/1015>



✓ Answer should be C. The reasoning is as follows:

When both R and S are set as 0, we will get both Q and Q' as 1 (these must be ideally mutually complementary). This output will be permanent and is not dependent on any sequence of events but just the input values (so no race condition). But after this state if we enter both R and S as 1, the output will be indeterminate depending on which NAND gate processes first (either Q or Q' will become 0 but we can't determine which (race condition) and it will lead to an indeterminate state.

PS: $R = 0, S = 0$ in an SR latch made by cross coupling 2 NAND gates will lead to a forbidden state. Forbidden state means, this state is invalid and must not be entered. This is different from an indeterminate state which means a state where we are not sure of the output. Again this is different from a toggling state where the output changes continuously.

57 votes

-- Prateek Arora (285 points)

4.15.3 Flip Flop: GATE CSE 2015 Set 1 | Question: 37

<https://gateoverflow.in/8287>



✓

Q_{prev}	D	Q(JK)	Explanation
-	1	0	Now, the D output is 1, meaning J and K = 1; for next cycle
0	0	1	J = K = 1(D output from prev state), so output toggles from 0 to 1
1	1	1	J = K = 0, so output remains 1
1	1	0	J = K = 0, so output remains 1
0	0	1	J = K = 1, so output toggles from 0 to 1
1	1	1	J = K = 0, so output remains 1

D flipflop output will be same as its input and JK flipflop output toggles when 1 is given to both J and K inputs.
i.e., $Q = D_{prev}(Q_{prev}') + (D_{prev}')Q_{prev}$

Correct Answer: A

35 votes

-- Arjun Suresh (332k points)



- ✓ Since it is synchronous so, after every clock cycle **T will toggle if input is 1** and will be in **Hold State if input is 0**. **D** flip-flop's output always follows input

- After 1 clock cycles : $Q1=0$ (Toggle) $Q0=1$
- After 2 clock cycles : $Q1=1$ (Toggle) $Q0=0$
- After 3 clock cycles: $Q1=1$ (Hold) $Q0=1$
- After 4 clock cycles: $Q1=0$ (Toggle) $Q0=1$

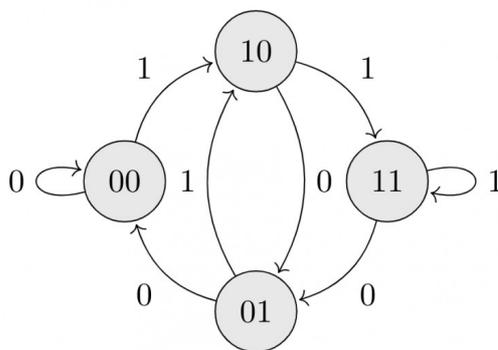
Hence, option **(B)** is correct.

👍 31 votes

-- sriv_shubham (2.8k points)



- ✓ Answer Is 2.



Here **00 on input 0** and **11 on input 1** have transition back to itself. So, answer is 2.

👍 55 votes

-- Suraj Sajeer (311 points)



- ✓ For a cross-coupled $R - S$ flip flop with two NAND gates 11 is no change and 00 is forbidden. 00 is forbidden (not allowed but not indeterminate) because in this state both Q and Q' equals 1. Moreover, in this state if inputs are changed to 11, next state is indeterminate (meaning we cannot determine the output)- Q can be 0 and Q' can be 1 or $Q = 1$ and $Q' = 0$. There is also a chance that outputs can oscillate here when the following happens:

1. Inputs are set to 11
2. When both inputs of NAND gates are 1 output is 0
3. Suppose NAND gate 1 becomes 0 first.
4. This 0 goes as input to NAND gate 2.
5. By this time NAND gate 2 produces its own output as 0.
6. Now, this 0 goes as input to NAND gate 1 which makes its output 1.
7. The 0 input to NAND gate 2 (from step 4) now makes its output 1.
8. Whole cycle can repeat and output toggles between 1 and 0.

This is just a possibility and that is why question says "may oscillate."

The input sequence 00,11 (Option D) may oscillate.

[https://en.wikipedia.org/wiki/Flip-flop_\(electronics\)#SR_NAND_latch](https://en.wikipedia.org/wiki/Flip-flop_(electronics)#SR_NAND_latch)

References



4.16

Floating Point Representation (9) top

4.16.1 Floating Point Representation: GATE CSE 1987 | Question: 1-vii top

<https://gateoverflow.in/80201>



The exponent of a floating-point number is represented in excess-N code so that:

- A. The dynamic range is large.
- B. The precision is high.
- C. The smallest number is represented by all zeros.
- D. Overflow is avoided.

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gate1987 digital-logic number-representation floating-point-representation

Answer

4.16.2 Floating Point Representation: GATE CSE 1989 | Question: 1-vi top

<https://gateoverflow.in/87053>



Consider an excess -50 representation for floating point numbers with 4 BCD digit mantissa and 2 BCD digit exponent in normalised form. The minimum and maximum positive numbers that can be represented are _____ and _____ respectively.

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descriptive gate1989 digital-logic number-representation floating-point-representation

Answer

4.16.3 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-a top

<https://gateoverflow.in/83830>



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16, The range of the exponent is _____

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gate1990 digital-logic number-representation floating-point-representation fill-in-the-blanks

Answer

4.16.4 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-b top

<https://gateoverflow.in/203832>



A 32-bit floating-point number is represented by a 7-bit signed exponent, and a 24-bit fractional mantissa. The base of the scale factor is 16, The range of the exponent is _____, if the scale factor is represented in excess-64 format.

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tests.gatecse.in

gate1990 digital-logic number-representation floating-point-representation fill-in-the-blanks

Answer

4.16.5 Floating Point Representation: GATE CSE 1997 | Question: 72 top

<https://gateoverflow.in/19702>



Following floating point number format is given

f is a fraction represented by a 6-bit mantissa (includes sign bit) in sign magnitude form, e is a 4-bit exponent (includes sign bit) in sign magnitude form and $n = (f, e) = f \cdot 2^e$ is a floating point number. Let $A = 54.75$ in decimal and $B = 9.75$ in decimal

- a. Represent A and B as floating point numbers in the above format.
- b. Show the steps involved in floating point addition of A and B .
- c. What is the percentage error (up to one position beyond decimal point) in the addition operation in (b)?

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goclasses.in

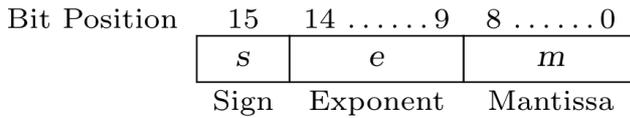
tests.gatecse.in

gate1997 digital-logic floating-point-representation normal descriptive

Answer



The following is a scheme for floating point number representation using 16 bits.



Let $s, e,$ and m be the numbers represented in binary in the sign, exponent, and mantissa fields respectively. Then the floating point number represented is:

$$\begin{cases} (-1)^s (1 + m \times 2^{-9}) 2^{e-31}, & \text{if the exponent } \neq 111111 \\ 0, & \text{otherwise} \end{cases}$$

What is the maximum difference between two successive real numbers representable in this system?

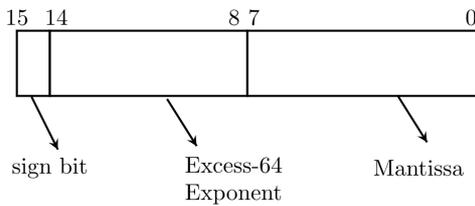
- A. 2^{-40}
- B. 2^{-9}
- C. 2^{22}
- D. 2^{31}

gate2003-cse digital-logic number-representation floating-point-representation normal

Answer [↗](#)



Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The decimal number 0.239×2^{13} has the following hexadecimal representation (without normalization and rounding off):

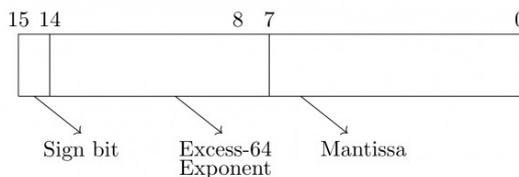
- A. 0D 24
- B. 0D 4D
- C. 4D 0D
- D. 4D 3D

gate2005-cse digital-logic number-representation floating-point-representation normal

Answer [↗](#)



Consider the following floating-point format.



Mantissa is a pure fraction in sign-magnitude form.

The normalized representation for the above format is specified as follows. The mantissa has an implicit 1 preceding the binary (radix) point. Assume that only 0's are padded in while shifting a field.

The normalized representation of the above number (0.239×2^{13}) is:

- A. 0A 20
- B. 11 34
- C. 49 D0
- D. 4A E8

gate2005-cse digital-logic number-representation floating-point-representation normal

Answer

4.16.9 Floating Point Representation: GATE CSE 2020 | Question: 29

<https://gateoverflow.in/333202>



Consider three registers $R1$, $R2$, and $R3$ that store numbers in IEEE-754 single precision floating point format. Assume that $R1$ and $R2$ contain the values (in hexadecimal notation) $0x42200000$ and $0xC1200000$, respectively.

If $R3 = \frac{R1}{R2}$, what is the value stored in $R3$?

- A. $0x40800000$
- B. $0xC0800000$
- C. $0x83400000$
- D. $0xC8500000$

gate2020-cse floating-point-representation digital-logic

Answer

Answers: Floating Point Representation

4.16.1 Floating Point Representation: GATE CSE 1987 | Question: 1-vii

<https://gateoverflow.in/80201>



✓ Answer : C) The smallest number is represented by all zeros.

In computer system, a floating-point number is represented as S E M, i.e. using Sign bit, Exponent bits and Mantissa bits.

The exponent can be a positive as well as a negative number. So to represent negative number we can use 1's complement or 2's complement. Better choice would be 2's complement.

If we use 2's complement system to represent exponent, then problem will arise while comparing 2 floating point numbers. For example, if exponent of the 2 numbers are negative then for comparing we will have to convert them into positive number.

So, to avoid this extra work, excess-N code is used so that all exponent can be represented in positive numbers, starting with 0.

28 votes

-- Kantikumar (3.4k points)

4.16.2 Floating Point Representation: GATE CSE 1989 | Question: 1-vi

<https://gateoverflow.in/87053>



✓ In binary we have normalized number of the form $(-1)^S \times 1.M \times 2^{E - \text{Bias}}$ where,

- S : sign bit
- M : Mantissa
- E : Exponent

Similarly for Binary Coded Decimal (BCD) numbers the normalized number representation will be $(-1)^S \times 1.M \times 10^{E - \text{Bias}}$

Here bias is given to be excess - 50 meaning that we need to subtract 50 from the base exponent field to get the actual exponent.

So, maximum mantissa value with 4 BCD digits = 9999

Maximum base exponent value with 2 BCD digits = 99

So, maximum actual exponent value possible with 2 BCD digits = 99 - Bias

$$= 99 - 50$$

$$= 49$$

So, the magnitude of the largest positive number = 9.9999×10^{49}

Similarly,

To get a minimum positive number, we have to set mantissa = 0 and exponent field = 0

So, doing that we get exponent = $0 - 50 = -50$

So, magnitude of minimum positive number = 1.0000×10^{50}

Therefore, maximum positive number = 9.9999×10^{49}

Minimum positive number = 1.0000×10^{-50}

👍 8 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

4.16.3 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-a [top](#)

<https://gateoverflow.in/83830>



- PS: It is an old question and IEEE format was not there then. Currently we use IEEE format if anything is unspecified.

As given exponent bits are 7 bits.

So, minimum it could be all 7 bit are 0's and maximum it could all 1's.

Assuming 2's complement representation minimum value = $-2^6 = -64$ and maximum value = $2^6 - 1 = 63$.

👍 18 votes

-- minal (13.1k points)

4.16.4 Floating Point Representation: GATE CSE 1990 | Question: 1-iv-b [top](#)

<https://gateoverflow.in/203832>



Minimum number = 0, maximum number = 127,

Given excess 64 so, bias number is 64,

Range will be $0 - 64 = -64$ to $(127 - 64 = 63)63$.

Here, in question given that base is 16, so the actual value represented will be $(-1)^s (0.M) \times 16^{E-\text{bias}}$.

👍 10 votes

-- minal (13.1k points)

4.16.5 Floating Point Representation: GATE CSE 1997 | Question: 72 [top](#)

<https://gateoverflow.in/19702>



PART A

$$A = 54.75 = 110110.11_2$$

Coming to the floating point representation we need to know whether to use "implied 1" in normalized representation or not. This is a 1997 question and IEEE-754 was not there and hence we cannot assume implied one.

$$\text{So, } A = 110110.11 = 0.11011011 \times 2^6$$

Thus mantissa = 11011011 and exponent = 110. We use sign magnitude representation for both mantissa and exponent, mantissa bits are 6 including sign and exponent bits are 4 including sign. So, we get

mantissa = 011011 and exponent = 0110 which means $A = (011011, 0110)$

$$B = 9.75 = 1001.11_2$$

$$= 0.100111 \times 2^4$$

So, mantissa bits = 010011 (truncated to 6 bits) and exponent bits = 0100.

$$\Rightarrow B = (010011, 0100)$$

PART B

To add two floating point numbers we must first make their exponents same and then add the mantissas. To make the exponents same we must make the smaller one equal to the larger (we cannot do the other way around as we can only shift the mantissa bits to right but not the left).

Here, $A = (011011, 0110)$ and $B = (010011, 0100)$.

Since, exponent of A is larger we change B to $B = (000100, 0110)$.

Now, adding the mantissa parts of A and B (MSB is sign bit and not added as in 2 's complement representation) we get $11011 + 00100 = 11111$. Thus we get $A + B = (011111, 0110)$.

PART C

Precise Result of $A + B = 54.75 + 9.75 = 64.5$

Result got in Part (b) = $0.10010 \times 2^7 = 1001000_2 = 72_{10}$.

So, error = $72 - 64.5 = 7.5$

$$\text{Percentage Error} = \frac{\text{Error}}{\text{Original Value}} \times 100 = \frac{7.5}{64.5} \times 100 = 11.63\%$$

👍 7 votes

-- Arjun Suresh (332k points)

4.16.6 Floating Point Representation: GATE CSE 2003 | Question: 43 top

<https://gateoverflow.in/934>



- ✓ The maximum difference between two successive real numbers will occur at extremes. This is because numbers are represented up to mantissa bits and as the exponent grows larger, the difference gets multiplied by a larger value. (The minimum difference happens for the least positive exponent value).

Biasing will be done by adding 31 as given in the question. So, actual value of exponent will be represented value -31 . Also, we can not have exponent field as all 1's as given in question (usually taken for representing infinity, NAN etc). So, largest value that can be stored is $111110 = 62$.

Largest number will be $1.111111111 \times 2^{62-31} = (2 - 2^{-9}) \times 2^{31}$

Second largest number will be $1.111111110 \times 2^{62-31} = (2 - 2^{-8}) 2^{31}$

So, difference between these two numbers

$$= (2 - 2^{-9}) \times 2^{31} - (2 - 2^{-8}) \times 2^{31} = 2^{31} [(2 - 2^{-9}) - (2 - 2^{-8})] = 2^{31} [2^{-8} - 2^{-9}] = 2^{31} \times 2^{-9} = 2^{22}$$

Correct Answer: C.

👍 69 votes

-- Ashish Gupta (759 points)

4.16.7 Floating Point Representation: GATE CSE 2005 | Question: 85-a top

<https://gateoverflow.in/1407>



- ✓ Answer is **option D** in both questions.

$$0.239 = (0.00111101)_2$$

(a) Stored exponent = actual + biasing

$$13 + 64 = 77$$

$$(77)_{10} = (1001101)_2$$

$$\text{Answer is: } \underbrace{0}_{\text{sign}} \underbrace{1001101}_{\text{exponent}} \underbrace{00111101}_{\text{mantissa}} = 0x \text{ 4D 3D}$$

(b) For normalized representation

$$0.00111101 * 2^{13} = 1.11101 * 2^{10}$$

$$\text{Stored exponent} = 10 + 64 = 74$$

$$(74)_{10} = (1001010)_2$$

$$\text{Answer: } \underbrace{0}_{\text{sign}} \underbrace{1001010}_{\text{exponent}} \underbrace{11101000}_{\text{mantissa}} = 0x \text{ 4A E8}$$

👍 47 votes

-- Pooja Palod (24.1k points)

4.16.8 Floating Point Representation: GATE CSE 2005 | Question: 85-b top

<https://gateoverflow.in/82139>



- ✓ For finding normalised representation we need to find unnormalised one first. So, we have:

0.239×2^{13} as the number. So, we find the binary equivalent of 0.239 till 8 digits as capacity of mantissa field is 8 bits.

We follow the following procedure:

- $0.239 \times 2 = 0.478$
- $0.478 \times 2 = 0.956$
- $0.956 \times 2 = 1.912$
- $0.912 \times 2 = 1.824$
- $0.824 \times 2 = 1.648$
- $0.648 \times 2 = 1.296$
- $0.296 \times 2 = 0.512$
- $0.512 \times 2 = 1.024$

We stop here as we have performed 8 iterations and hence, 8 digits of mantissa of unnormalised number is obtained. Now we have:

Mantissa of given number = 0011 1101

So, the number can be written as: 0.00111101×2^{13}

Now we need to align the mantissa towards left to get normalised number. And in the question it is mentioned that during alignment process 0's will be padded in the right side as a result of mantissa alignment to left.

So, to get normalised number, we align to left 3 times, to get new mantissa = 11101000

Exponent will also decrease by 3 hence, new exponent = 10

So, normalised number = 1.11101000×2^{10}

Actual exponent = 10

Given excess 64 is used which means bias value = 64

So, exponent field value = $10 + 64 = 74$

And of course sign bit = 0 being a positive number.

Thus the final representation of number
 = 0 1001010 11101000
 = 0100 1010 1110 1000
 = $(4AE8)_{16}$

Hence, (D) should be the correct answer.

👍 32 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

4.16.9 Floating Point Representation: GATE CSE 2020 | Question: 29

<https://gateoverflow.in/333202>



$$R_3 = \frac{R_1}{R_2} = \frac{42200000}{C1200000} = \frac{0.100\ 0010\ 0:010}{1.100\ 0001\ 0:010} = \frac{+132\ 010}{-130\ 010} = -(2 + 127)000 = 110000001000 = C08$$

Here, last 20 zeroes are not written in numerator and denominator

For IEEE single precision format,
 S(Sign Bit) = 1 bit
 E(Exponent) = 8 bits
 M(Mantissa) = 23 bits

- (1) Sign bit will be -ve because division of +ve and -ve will result in a -ve number
- (2) Exponent will be $(132 - 130 = 2)$ and biased exponent will be $2 + 127 = 129$
- (3) Normalized Mantissa will be $\frac{1.010}{1.010} = 1.000$

For more elaboration, please refer: [General Floating-Point Division](#)

References



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23 votes

-- Vijay Verma (195 points)

$$R1 = 0x42200000 = 0100\ 0010\ 0010\ 0000\ 0000\ 0000\ 0000\ 0000$$

As per IEEE -754 single precision format,

S=0 ==> +ve number

$$\text{Exponent} = (10000100)_2 = 128+4 = 132$$

$$\text{true exponent} = 132-127 = 5$$

$$\text{Mantissa} = (010\ 000000000)_2$$

$$\text{value} = (-1)^0 \cdot (1.010000000000\dots) \cdot 2^5 = (101000.000000\dots)_2 = 40$$

$$R2 = 0xC1200000 = 1100\ 0001\ 0010\ 0000\ 0000\ 0000\ 0000\ 0000$$

As per IEEE -754 single precision format,

S=1 ==> -ve number

$$\text{Exponent} = (10000010)_2 = 128+2 = 130$$

$$\text{true exponent} = 130-127 = 3$$

$$\text{Mantissa} = (010\ 000000000)_2$$

$$\text{value} = (-1)^1 \cdot (1.010000000000\dots) \cdot 2^3 = (1010.000000\dots)_2 = -10$$

$$R3 = \frac{40}{-10} = -4$$

represent -4 in IEEE-754 single precision format

S=1

$$\text{Value} = (100.0000) \cdot 2^0 = (1.00000000\dots) \cdot 2^2$$

$$\text{true exponent} = 2 ==> \text{exponent} = 2+127=129 = (10000001)_2$$

Mantissa = 000000..0

-4 in IEEE format : 1100 0000 1000 0000 0000 0000 0000 0000

in Hexa decimal format : 0xC0800000

option B is correct

33 votes

-- Shaik Masthan (50.4k points)



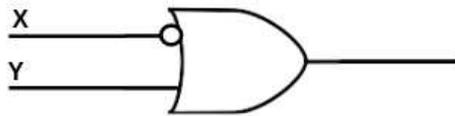
Show that $\{\text{NOR}\}$ is a functionally complete set of Boolean operations.

gate1989 descriptive digital-logic functional-completeness

Answer



The implication gate, shown below has two inputs (x and y); the output is 1 except when $x = 1$ and $y = 0$, realize $f = \bar{x}y + x\bar{y}$ using only four implication gates.



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Show that the implication gate is functionally complete.

gate1998 digital-logic functional-completeness descriptive

Answer



Which of the following sets of component(s) is/are sufficient to implement any arbitrary Boolean function?

- XOR gates, NOT gates
- 2 to 1 multiplexers
- AND gates, XOR gates
- Three-input gates that output $(A \cdot B) + C$ for the inputs A, B and C .

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gate1999 digital-logic normal functional-completeness multiple-selects

Answer



A set of Boolean connectives is functionally complete if all Boolean functions can be synthesized using those. Which of the following sets of connectives is NOT functionally complete?

- EX-NOR
- implication, negation
- OR, negation
- NAND

gate2008-it digital-logic easy functional-completeness

Answer

Answers: Functional Completeness



- ✓ The functionally complete set is by which you can perform all operations. So, if any logical set is able to implement the operation $\{\text{And}, \text{NOT}\}$ or $\{\text{OR}, \text{NOT}\}$; it is known as functionally complete.

Now come to NOR gate.

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- $A(\text{NOR})B = (A + B)'$

- $A(\text{NOR})A = (A + A)' = (A)'$, so we can perform the NOT operation .
- $(A + B)' \text{ NOR } (A + B)' = ((A + B)' + (A + B)')' = ((A + B)')' = (A + B)$, so OR operation is also performed successfully .

So, NOR is functionally complete.

👍 16 votes

-- Amit Pal (3k points)

4.17.2 Functional Completeness: GATE CSE 1998 | Question: 5 [top](#)

<https://gateoverflow.in/1696>



- ✓ Implication gate is $A \rightarrow B$ which becomes $A + B$

So, let $f(A, B) = A' + B$

$f(A, 0) = A'$ (we get complement)

$f(f(A, 0), B) = f(A', B) = A + B$ (we get OR gate)

Thus it is functionally complete.

Let $F(X, Y) = X' + Y$

$F(Y, X) = Y' + X$

$F(F(Y' + X), 0) = X'Y$

$F(F(X, Y), X'Y) = XY' + XY'$ Therefore, the above function is implemented with 4 implication gates.

👍 16 votes

-- Riya Roy(Arayana) (5.3k points)

4.17.3 Functional Completeness: GATE CSE 1999 | Question: 2.9 [top](#)

<https://gateoverflow.in/1487>



- ✓ 1. XOR and NOT gates can only make XOR and XNOR which are not functionally complete- $a \oplus \bar{a} = 1, a \oplus a = 0$.
- 2. 2-1 multiplexer is functionally complete provided we have external 1 and 0 available. For NOT gate, use x as select line and use 0 and 1 as inputs. For AND gate, use y and 0 as inputs and x as select. With {AND, NOT} any other gate can be made.
- 3. XOR can be used to make a NOT gate ($a \oplus 1 = \bar{a}$) and {AND, NOT} is functionally complete. Again this requires external 1.
- 4. We have $AB + C$. Using $C = 0$, we get an AND gate. Using $B = 1$ we get an OR gate. But we cannot derive a NOT gate here.

So, options B and C are true provided external 1 and 0 are available.

👍 49 votes

-- Arjun Suresh (332k points)

4.17.4 Functional Completeness: GATE IT 2008 | Question: 1 [top](#)

<https://gateoverflow.in/3222>



- ✓ EX-NOR is not functionally complete.

NOR and NAND are functionally complete logic gates, OR , AND, NOT any logic gate can be implemented using them.

And (Implication, Negation) is also functionally complete

First complement q to get q' then

$p \rightarrow q' = p' + q'$

Now complement the result to get AND gate

$(p' + q')' \Rightarrow pq$

👍 43 votes

-- Manu Thakur (34k points)

4.18

Ieee Representation (7) [top](#)

4.18.1 Ieee Representation: GATE CSE 2008 | Question: 4 [top](#)

<https://gateoverflow.in/402>



In the IEEE floating point representation the hexadecimal value 0x00000000 corresponds to

- A. The normalized value 2^{-127}
- B. The normalized value 2^{-126}
- C. The normalized value $+0$
- D. The special value $+0$

gate2008-cse digital-logic floating-point-representation ieee-representation easy

Answer

4.18.2 IEEE Representation: GATE CSE 2012 | Question: 7 [top](#) <https://gateoverflow.in/39>



The decimal value 0.5 in IEEE single precision floating point representation has

- A. fraction bits of 000 . . . 000 and exponent value of 0
- B. fraction bits of 000 . . . 000 and exponent value of -1
- C. fraction bits of 100 . . . 000 and exponent value of 0
- D. no exact representation

gate2012-cse digital-logic normal number-representation ieee-representation

Answer

4.18.3 IEEE Representation: GATE CSE 2014 Set 2 | Question: 45 [top](#) <https://gateoverflow.in/2011>



The value of a float type variable is represented using the single-precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponent and 23 bits for the mantissa. A float type variable X is assigned the decimal value of -14.25 . The representation of X in hexadecimal notation is

- A. C1640000H
- B. 416C0000H
- C. 41640000H
- D. C16C0000H

gate2014-cse-set2 digital-logic number-representation normal ieee-representation

Answer

4.18.4 IEEE Representation: GATE CSE 2017 Set 2 | Question: 12 [top](#) <https://gateoverflow.in/118434>



Given the following binary number in 32-bit (single precision) IEEE-754 format :

00111110011011010000000000000000

The decimal value closest to this floating-point number is :

- A. $1.45 * 10^1$
- B. $1.45 * 10^{-1}$
- C. $2.27 * 10^{-1}$
- D. $2.27 * 10^1$

gate2017-cse-set2 digital-logic number-representation floating-point-representation ieee-representation

Answer

4.18.5 IEEE Representation: GATE CSE 2021 Set 1 | Question: 24 [top](#) <https://gateoverflow.in/357427>



Consider the following representation of a number in IEEE 754 single-precision floating point format with a bias of 127.

$S : 1 \quad E : 10000001 \quad F : 111100000000000000000000$

Here S , E and F denote the sign, exponent, and fraction components of the floating point representation.

The decimal value corresponding to the above representation (rounded to 2 decimal places) is _____.

gate2021-cse-set1 digital-logic number-representation ieee-representation numerical-answers

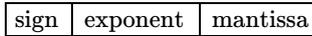
Answer

4.18.6 Ieee Representation: GATE CSE 2021 Set 2 | Question: 4

https://gateoverflow.in/357536



The format of the single-precision floating point representation of a real number as per the IEEE 754 standard is as follows:



Which one of the following choices is correct with respect to the *smallest* normalized positive number represented using the standard?

- A. exponent = 00000000 and mantissa = 000000000000000000000000
- B. exponent = 00000000 and mantissa = 000000000000000000000001
- C. exponent = 00000001 and mantissa = 000000000000000000000000
- D. exponent = 00000001 and mantissa = 000000000000000000000001

gate2021-cse-set2 digital-logic number-representation ieee-representation

Answer

4.18.7 Ieee Representation: GATE IT 2008 | Question: 7

https://gateoverflow.in/3267



The following bit pattern represents a floating point number in IEEE 754 single precision format

1 10000011 101000000000000000000000

The value of the number in decimal form is

- A. -10
- B. -13
- C. -26
- D. None of the above

gate2008-it digital-logic number-representation floating-point-representation ieee-representation normal

Answer

Answers: Ieee Representation

4.18.1 Ieee Representation: GATE CSE 2008 | Question: 4

https://gateoverflow.in/402



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S	BE	M	Value
0 / 1	All 0's	All 0's	0
0	All 1's	All 0's	$+\infty$
1	All 1's	All 0's	$-\infty$
0 / 1	All 1's	Non-zero	NaN

The answer is option D.

Reference: <http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



48 votes

-- Amar Vashishth (25.2k points)

4.18.2 Ieee Representation: GATE CSE 2012 | Question: 7

https://gateoverflow.in/39



- (B) is the answer. IEEE 754 representation uses normalized representation when the exponent bits are all non zeroes and hence an implicit '1' is used before the decimal point. So, if mantissa is:

0000..0

Ut would be treated as:

1.000..0

and hence, the exponent need to be -1 for us to get 0.1 which is the binary representation of 0.5.

More into IEEE floating point representation:
<http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



36 votes

-- gatecse (63.3k points)

4.18.3 IEEE Representation: GATE CSE 2014 Set 2 | Question: 45 top 5

<https://gateoverflow.in/2011>



✓ IEEE-754 representation for float (single-precision) type is as follows

0	1-8	9-31
Sign	Exponent	Mantissa

Thus, the exponent field is of 8 bits and mantissa is of 23 bits (precision is actually of 24 bits due to an implied 1 mandated in normalized representation; IEEE 754 also allows denormalized numbers which are close to 0 but this is not applicable to the given question).

The exponent field also requires sign to represent fractions. IEEE 754 does this by giving a bias -- 127 for single-precision which means we simply subtract 127 from the represented value to get the actual value. Thus, 0 becomes -127 and 255 (maximum value representable using 8 bits becomes 128.

Now, coming to the given question we need to represent -14.25 which equals -1110.01 in binary.

Converting to normalized form (only one 1 to the left of .) we get

$$-1110.01 = -1.11001 \times 2^3$$

Since we omit the implied 1 in IEEE-754 representation we get

- Mantissa bits = 11001
- Exponent bits = 11 + 0111111 = 10000010 (Adding bias 127)
- Sign bit = 1 (since number is negative)

This will be 1 10000010 110010000000000000000000

Grouping in 4 bits to convert to Hexadecimal we get

$$1100\ 0001\ 0110\ 0100\ 0000\ 0000\ 0000\ 0000$$

$$= C1640000H$$

Option A.

More Reference: <http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



11 votes

-- Arjun Suresh (332k points)



- ✓ In 32 bit (single precision) IEEE-754 format, binary number is represented as $S(1 \text{ bit}) E(8 \text{ bit}) M(23 \text{ bits})$ with implicit normalization and exponent is represented with Excess-127 code.
- Here, Sign bit = 0 \Rightarrow Number is positive.
- Exponent bits = 01111100 = 124 $\Rightarrow E = 124 - 127 = -3$ (Excess-127)
- Mantissa bits = 11011010000000000000000 \Rightarrow Number = 1.1101101 (Implicit normalization).
- \therefore Number = $1.1101101 * 2^{-3} = 0.0011101101 = 0.227 = 2.27 * 10^{-1}$
- \therefore Answer should be C.

👍 38 votes

-- Kantikumar (3.4k points)



- ✓ -7.75 is correct answer.
- Here, Sign bit = 1 \rightarrow Number is negative.
- Exponent bits = 10000001 = 129₁₀ $\rightarrow E = 129 - 127 = 2$ as IEEE-754 single precision format uses 127 as the exponent bias.
- Mantissa bits = 11110000000000000000000
- Number = $-1.111100 \dots 00 \times 2^2 = -111.11$
- \therefore Number = $(-7.75)_{10}$.

Reference: <https://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



👍 4 votes

-- Himanshu (929 points)



- ✓ In IEEE 754 representation all 1s in exponent field is reserved for special numbers
- + (when sign bit is positive) and - (when sign bit is negative) infinities when all mantissa bits are zeroes.
 - SNAN (Signaling Not A Number): when leading mantissa bit is 0 and at least one other mantissa bit is non-zero
 - NAN (Quiet NAN): when leading mantissa bit is 1

More read on QNAN vs SNAN: <https://stackoverflow.com/questions/18118408/what-is-the-difference-between-quiet-nan-and-signaling-nan>

Also, all 0s for exponent field is reserved for denormalized numbers (small numbers between 0 and ± 1 which cannot be represented using normalized numbers). That is, a normalized IEEE 754 represented number (both single and double precision) must have at least one bit set in the exponent field and for the smallest exponent this will be the right most bit. Now, to make it the smallest **positive** normalized number in single-precision format, we can have all mantissa bits 0 which will give the numerical value as $1.000 \dots 0 \times 2^{1-127} = 2^{-126}$. (Here, 1 before "." is implied in IEEE 754 representation for every normalized numbers and 127 is the exponent bias used to have negative exponents without an explicit sign bit)

Reference: <https://steve.hollasch.net/cgindex/coding/ieeefloat.html>

References



2 votes

gatecse (63.3k points)

4.18.7 IEEE Representation: GATE IT 2008 | Question: 7

https://gateoverflow.in/3267



✓ Sign bit is 1 \implies number is negative

Exponent bits- 1000011

Exponent is added with 127 bias in IEEE single precision format. So, actual exponent = $1000011 - 127 = 131 - 127 = 4$

Mantissa bits- 1010000000000000000000

In IEEE format, an implied 1 is before mantissa, and hence the actual number is:

$$-1.101 \times 2^4$$

$$= -(11010)_2 = -26$$

<http://steve.hollasch.net/cgindex/coding/ieeefloat.html>

Correct Answer: C

References



44 votes

Arjun Suresh (332k points)

4.19

K Map (19)

4.19.1 K Map: GATE CSE 1987 | Question: 16-a

https://gateoverflow.in/82698

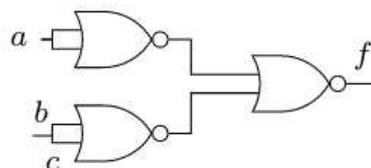


A Boolean function f is to be realized only by NOR gates. Its K -map is given below:

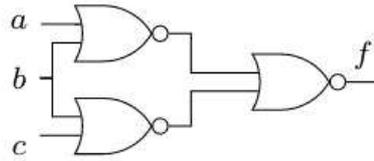
	ab	00	01	11	10
c	0	0	0	1	1
	1	0	1	1	1

The realization is

A.



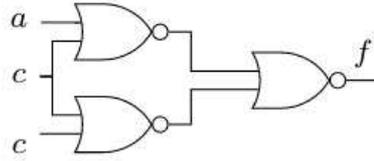
B.



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C.

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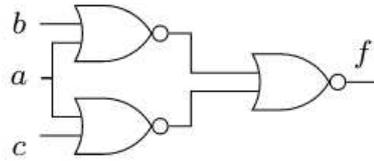
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D.

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gate1987 digital-logic k-map

Answer

4.19.2 K Map: GATE CSE 1988 | Question: 3a-b top

https://gateoverflow.in/94358



		<i>BC</i>			
		00	01	11	10
<i>A</i>	0	1		1	1
	1		1	1	

		<i>B</i>	
		0	1
<i>A</i>	0	\bar{C}	1
	1	C	C

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The Karnaugh map of a function of (A, B, C) is shown on the left hand side of the above figure.

The reduced form of the same map is shown on the right hand side, in which the variable C is entered in the map itself. Discuss,

- The methodology by which the reduced map has been derived and
- the rules (or steps) by which the boolean function can be derived from the entries in the reduced map.

gate1988 descriptive digital-logic k-map

Answer

4.19.3 K Map: GATE CSE 1992 | Question: 01-i top

https://gateoverflow.in/545



The Boolean function in sum of products form where K-map is given below (figure) is _____

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		C	
		0	1
B	0	1	0
	1	\bar{A}	A

tests.gatecse.in

gate1992 digital-logic k-map normal fill-in-the-blanks

Answer

4.19.4 K Map: GATE CSE 1995 | Question: 15-a top

https://gateoverflow.in/2651



Implement a circuit having the following output expression using an inverter and a nand gate

$$Z = \bar{A} + \bar{B} + C$$

gate1995 digital-logic k-map normal descriptive

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Answer

4.19.5 K Map: GATE CSE 1995 | Question: 15-b top

https://gateoverflow.in/20387



What is the equivalent minimal Boolean expression (in sum of products form) for the Karnaugh map given below?

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		AB			
		00	01	11	10
CD	00	1			1
	01		1	1	
	11		1	1	
	10	1			1

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gate1995 digital-logic boolean-algebra k-map normal descriptive

Answer

4.19.6 K Map: GATE CSE 1996 | Question: 2.24 top

https://gateoverflow.in/2753



What is the equivalent Boolean expression in product-of-sums form for the Karnaugh map given in Fig

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goclasses.in

tests.gatecse.in

		AB			
		00	01	11	10
CD	00		1	1	
	01	1			1
	11	1			1
	10		1	1	

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A. $B\bar{D} + \bar{B}D$

B. $(B + \bar{C} + D)(\bar{B} + C + \bar{D})$

C. $(B + D)(\bar{B} + \bar{D})$

D. $(B + \bar{D})(\bar{B} + D)$

gate1996 digital-logic k-map easy

Answer

4.19.7 K Map: GATE CSE 1998 | Question: 2.7 top

https://gateoverflow.in/1679



The function represented by the Karnaugh map given below is

	BC	00	01	10	11
A	0	1	0	0	1
	1	1	0	0	1

A. $A \cdot B$

B. $AB + BC + CA$

C. $B \oplus C$

D. $A \cdot BC$

gate1998 digital-logic k-map normal

Answer

4.19.8 K Map: GATE CSE 1999 | Question: 1.8 top

https://gateoverflow.in/1461



Which of the following functions implements the Karnaugh map shown below?

	CD	00	01	11	10
AB	00	0	0	1	0
	01	X	X	1	X
	11	0	1	1	0
	10	0	1	1	0

A. $\bar{A}B + CD$

B. $D(C + A)$

C. $AD + \bar{A}B$

D. $(C + D)(\bar{C} + D) + (A + B)$

gate1999 digital-logic k-map easy

Answer

4.19.9 K Map: GATE CSE 2000 | Question: 2.11 top

https://gateoverflow.in/658



Which functions does NOT implement the Karnaugh map given below?

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	wz	00	01	11	10
xy	00	0	X	0	0
	01	0	X	1	1
	11	1	1	1	1
	10	0	X	0	0

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tests.gatecse.in

goclasses.in

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- A. $(w + x)y$
- B. $xy + yw$
- C. $(w + x)(\bar{w} + y)(\bar{x} + y)$
- D. None of the above

gate2000-cse digital-logic k-map normal

Answer 

4.19.10 K Map: GATE CSE 2001 | Question: 1.11 [top](#)

<https://gateoverflow.in/704>



Given the following karnaugh map, which one of the following represents the minimal Sum-Of-Products of the map?

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	wx	00	01	11	10
yz	00	0	X	0	X
	01	X	1	X	1
	11	0	X	1	0
	10	0	1	X	0

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- A. $XY + Y'Z$
- B. $WX'Y' + XY + XZ$
- C. $W'X + Y'Z + XY$
- D. $XZ + Y$

gate2001-cse k-map digital-logic normal

Answer 

4.19.11 K Map: GATE CSE 2002 | Question: 1.12 [top](#)

<https://gateoverflow.in/816>



Minimum sum of product expression for $f(w, x, y, z)$ shown in Karnaugh-map below

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tests.gatecse.in

		wx			
		00	01	11	10
yz	00	0	1	1	0
	01	X	0	0	1
	11	X	0	0	1
	10	0	1	1	X

- A. $xz + y'z$
- B. $xz' + zx'$
- C. $x'y + zx'$
- D. None of the above

gate2002-cse digital-logic k-map normal

goclasses.in

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Answer 

4.19.12 K Map: GATE CSE 2003 | Question: 45 top

<https://gateoverflow.in/936>



The literal count of a Boolean expression is the sum of the number of times each literal appears in the expression. For example, the literal count of $(xy + xz')$ is 4. What are the minimum possible literal counts of the product-of-sum and sum-of-product representations respectively of the function given by the following Karnaugh map? Here, X denotes "don't care"

		zw			
		00	01	11	10
xy	00	X	1	0	1
	01	0	1	X	0
	11	1	X	X	0
	10	X	0	0	X

- A. (11, 9)
- B. (9, 13)
- C. (9, 10)
- D. (11, 11)

gate2003-cse digital-logic k-map normal

goclasses.in

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Answer 

4.19.13 K Map: GATE CSE 2008 | Question: 5 top

<https://gateoverflow.in/403>



In the Karnaugh map shown below, X denotes a don't care term. What is the minimal form of the function represented by the Karnaugh map?

	ab	00	01	11	10
cd	00	1	1		1
	01	X			
	11	X			
	10	1	1		X

- A. $\bar{b}. \bar{d} + \bar{a}. \bar{d}$
- B. $\bar{a}. \bar{b} + \bar{b}. \bar{d} + \bar{a}. b. \bar{d}$
- C. $\bar{b}. \bar{d} + \bar{a}. b. \bar{d}$
- D. $\bar{a}. \bar{b} + \bar{b}. \bar{d} + \bar{a}. \bar{d}$

gate2008-cse digital-logic k-map easy

Answer

4.19.14 K Map: GATE CSE 2012 | Question: 30 [top](#)

<https://gateoverflow.in/1615>



What is the minimal form of the Karnaugh map shown below? Assume that X denotes a don't care term

	ab	00	01	11	10
cd	00	1	X	X	1
	01	X			1
	11				
	10	1			X

- A. $\bar{b}\bar{d}$
- B. $\bar{b}\bar{d} + \bar{b}\bar{c}$
- C. $\bar{b}\bar{d} + \bar{a}\bar{b}\bar{c}d$
- D. $\bar{b}\bar{d} + \bar{b}\bar{c} + \bar{c}\bar{d}$

gate2012-cse digital-logic k-map easy

Answer

4.19.15 K Map: GATE CSE 2017 Set 1 | Question: 21 [top](#)

<https://gateoverflow.in/118301>



Consider the Karnaugh map given below, where X represents "don't care" and blank represents 0.

	ba	00	01	11	10
dc	00		X	X	
	01	1			X
	11	1			1
	10		X	X	

Assume for all inputs (a, b, c, d) , the respective complements $(\bar{a}, \bar{b}, \bar{c}, \bar{d})$ are also available. The above logic is implemented using 2-input NOR gates only. The minimum number of gates required is _____.

gate2017-cse-set1 digital-logic k-map numerical-answers normal

Answer

4.19.16 K Map: GATE CSE 2019 | Question: 30

<https://gateoverflow.in/302818>



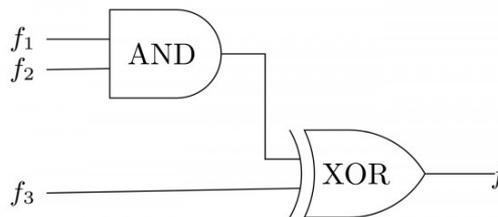
Consider three 4-variable functions f_1, f_2 , and f_3 , which are expressed in sum-of-minterms as

$$f_1 = \Sigma(0, 2, 5, 8, 14),$$

$$f_2 = \Sigma(2, 3, 6, 8, 14, 15),$$

$$f_3 = \Sigma(2, 7, 11, 14)$$

For the following circuit with one AND gate and one XOR gate the output function f can be expressed as:



- A. $\Sigma(7, 8, 11)$
- B. $\Sigma(2, 7, 8, 11, 14)$
- C. $\Sigma(2, 14)$
- D. $\Sigma(0, 2, 3, 5, 6, 7, 8, 11, 14, 15)$

gate2019-cse digital-logic k-map digital-circuits

Answer

4.19.17 K Map: GATE IT 2006 | Question: 35

<https://gateoverflow.in/3574>



The boolean function for a combinational circuit with four inputs is represented by the following Karnaugh map.

	PQ	00	01	11	10
RS	00	1	0	0	1
	01	0	0	1	1
	11	1	1	1	0
	10	1	0	0	1

Which of the product terms given below is an essential prime implicant of the function?

- A. QRS
- B. PQS
- C. PQ'S'
- D. Q'S'

gate2006-it digital-logic k-map normal

Answer

4.19.18 K Map: GATE IT 2007 | Question: 78 top

<https://gateoverflow.in/3530>



Consider the following expression

$$a\bar{d} + \bar{a}\bar{c} + \bar{b}\bar{c}d$$

Which of the following Karnaugh Maps correctly represents the expression?

A.

cd \ ab	00	01	11	10
00	X	X		
01	X	X		
11	X	X		X
10	X			X

B.

cd \ ab	00	01	11	10
00	X	X		
01	X			
11	X	X		X
10	X	X		X

C.

cd \ ab	00	01	11	10
00	X	X		
01	X	X		X
11	X	X		X
10	X			X

D.

cd \ ab	00	01	11	10
00	X	X		
01	X	X		X
11	X	X		X
10	X		X	X

gate2007-it digital-logic k-map normal

Answer

4.19.19 K Map: GATE IT 2007 | Question: 79 top

https://gateoverflow.in/3531



Consider the following expression

$$a\bar{d} + \bar{a}\bar{c} + b\bar{c}d$$

Which of the following expressions does not correspond to the Karnaugh Map obtained for the given expression?

- A. $\bar{c}\bar{d} + a\bar{d} + ab\bar{c} + \bar{a}\bar{c}d$
- B. $\bar{a}\bar{c} + \bar{c}\bar{d} + a\bar{d} + ab\bar{c}d$
- C. $\bar{a}\bar{c} + a\bar{d} + ab\bar{c} + \bar{c}d$
- D. $\bar{b}\bar{c}\bar{d} + a\bar{c}\bar{d} + \bar{a}\bar{c} + ab\bar{c}$

gate2007-it digital-logic k-map normal

Answer

Answers: K Map

4.19.1 K Map: GATE CSE 1987 | Question: 16-a top

https://gateoverflow.in/82698



Two Max Terms are:

$(a + b)(a + c)$ so, "a" is common here only possibility is option D.

K-map will give min terms = $a[41's \text{ circle}] + bc[21's \text{ box}]$

Option D circuit will give = $(a + b)(a + c) = a + bc$

D will be answer.

20 votes

-- papesh (18k points)

4.19.2 K Map: GATE CSE 1988 | Question: 3a-b top

https://gateoverflow.in/94358



✓

		BC			
		00	01	11	10
0	A	1		1	1
1			1	1	

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We can get the truth table as

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

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Now, to reduce the K-map to a Variable Entrant Map we can write the function F in terms of C . i.e., wherever F is becoming 1 dependent on C (i.e. when C complements F must become 0), we replace 1 with C or \bar{C} based on whichever is giving output 1. So, we can rewrite the truth table as

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A	B	F
0	0	\bar{C}
0	1	1
1	0	C
1	1	C

In the above truth table $F = 1$ for second row, because when $A = 0, B = 1, F = 1$ for both C and \bar{C} making F independent of C . Now, if we draw the K -map for the above truth table we get the reduced Variant Entrant map given.

👍 10 votes

-- Arjun Suresh (332k points)

4.19.3 K Map: GATE CSE 1992 | Question: 01-i [top](#) [👍](#)

<https://gateoverflow.in/545>



✓

Answer - $ABC + B'C' + A'C'$

Expand this K map of 2 variables (4 cells) to K map of three variable (8 cells)

Entries which are non zero are: $A'B'C', AB'C', A'BC'$ and ABC

Minimize SOP expression using that K map.

👍 22 votes

-- Ankit Rokde (6.9k points)

4.19.4 K Map: GATE CSE 1995 | Question: 15-a [top](#) [👍](#)

<https://gateoverflow.in/2651>



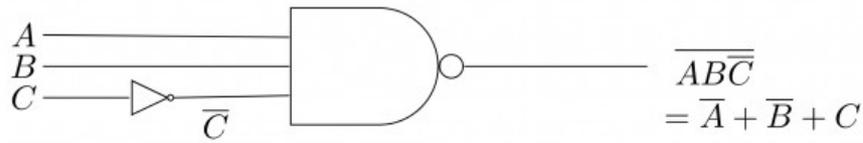
✓

The circuit can be implemented as follows:

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16 votes

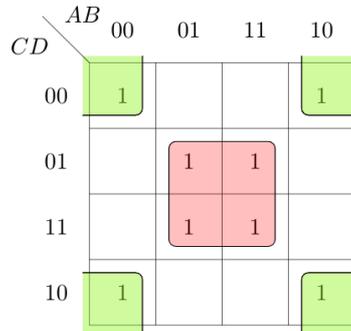
-- Leen Sharma (28.7k points)

4.19.5 K Map: GATE CSE 1995 | Question: 15-b top

https://gateoverflow.in/203837



✓



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SUM OF PRODUCT is equal to XNOR GATE

$$SOP = BD + \overline{B}\overline{D} = \overline{B \oplus D} = B \odot D$$

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10 votes

-- Lakshman Patel (65.7k points)

4.19.6 K Map: GATE CSE 1996 | Question: 2.24 top

https://gateoverflow.in/2753



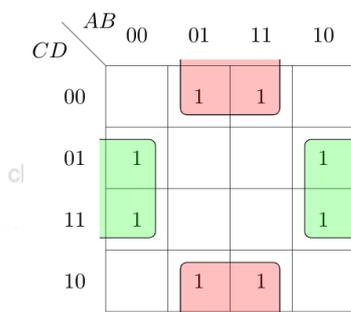
✓

Following two K-Maps are equivalent and represent the same boolean function.

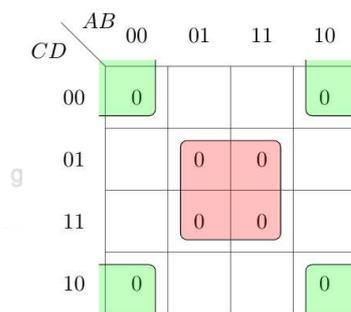
While the first K-Map gives us the boolean expression in Sum-of-Product form, and the second K-Map gives us the same boolean function in Product-of-Sum form:

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(i)



(ii)

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(C) is correct option!

PS: If SOP is asked answer will be (A).

11 votes

-- Manu Thakur (34k points)



✓ The given K-map is not standard as after "01" we have "10" and two variables are changing for consecutive column. This means it is not safe to merge adjacent 1s. By converting the K-map to standard form we get

		BC			
		00	01	11	10
A	0	1	0	1	0
	1	1	0	1	0

which gives

$$BC + \bar{B}\bar{C} = B \text{ XNOR } C = B \odot C$$

This can be represented as negation of XOR = $\overline{B \oplus C}$

Option C is correct.

👍 24 votes

-- shekhar chauhan (32.8k points)



		CD			
		00	01	11	10
AB	00	0	0	1	0
	01	X	X	1	X
	11	0	1	1	0
	10	0	1	1	0

$$CD + AD = D(C + A)$$

Correct Answer: B

👍 11 votes

-- Rameez Raza (1.8k points)



✓ **Answer is D.**

See we can simplify each equation given in the option and get that all of them gives $xy + wy$. But let think in another way.

1st option is written in POS form, as we can check we get the same if we consider the following implicants.

		wz			
		00	01	11	10
xy	00	0	X	0	0
	01	0	X	1	1
	11	1	1	1	1
	10	0	X	0	0

which is $(w + x)y$

for the second one

wz	00	01	11	10
xy				
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

Which gives $wy + xy$

wz	00	01	11	10
xy				
00	0	X	0	0
01	0	X	1	1
11	1	1	1	1
10	0	X	0	0

now for 3rd one, we can verify like this

which is $(w + x)(\bar{w} + y)(\bar{x} + y)$

So as we can verify each equation in a given K-Map, **so the answer is option D**

14 votes

akshat sinha (609 points)

4.19.10 K Map: GATE CSE 2001 | Question: 1.11

<https://gateoverflow.in/704>



✓

wx	00	01	11	10
yz				
00	0	X	0	X
01	X	1	X	1
11	0	X	1	0
10	0	1	X	0

Answer: A

22 votes

Priya Sukumaran (141 points)

4.19.11 K Map: GATE CSE 2002 | Question: 1.12

<https://gateoverflow.in/816>



✓

		wx			
		00	01	11	10
yz	00	0	1	1	0
	01	X	0	0	1
	11	X	0	0	1
	10	0	1	1	X

Two quads are getting formed xz and $z\bar{x}$

Ans is Option B

15 votes

-- GATE_2016 (469 points)

4.19.12 K Map: GATE CSE 2003 | Question: 45 top

<https://gateoverflow.in/936>



We will be getting two different groupings..

Grouping 1 : (9, 8)

		zw			
		00	01	11	10
xy	00	X	1	0	1
	01	0	1	X	0
	11	1	X	X	0
	10	X	0	0	X

cl

$$\text{SOP : } 2 + 3 + 3 = 8$$

		zw			
		00	01	11	10
xy	00	X	1	0	1
	01	0	1	X	0
	11	1	X	X	0
	10	X	0	0	X

ga

$$\text{POS : } 2 + 2 + 2 + 3 = 9$$

GROUPING 2 : (9, 10)

		zw			
		00	01	11	10
xy	00	X	1	0	1
	01	0	1	X	0
	11	1	X	X	0
	10	X	0	0	X

cl

		zw			
		00	01	11	10
xy	00	X	1	0	1
	01	0	1	X	0
	11	1	X	X	0
	10	X	0	0	X

gateo

$$\text{POS : } 2 + 2 + 2 + 3 = 9$$

$$\begin{aligned} \text{SOP} &: 2 + 2 + 3 \\ &+ 3 = 10 \end{aligned}$$

Both the grouping are correct representation of the function $f(wxyz)$

PS: Some wrong beliefs about don't cares

1. "once you have assumed a don't care as '1' u can't use the same don't care for grouping zeros and vice versa"
2. "if don't care has been used in POS than can't be used in SOP"

Both these statements are wrong. Don't care simply means just don't care -- say we use don't care $d3$ for grouping 1 in SOP we can use $d3$ for grouping 0 in POS. (The literals in SOP and POS may not be the same)

K-Map grouping is not unique. And the question says about minimal literals. So, the **best answer would be (9,8)** Since there is no option in GATE we can go with (9, 10) (the question setter might have missed Grouping 1)

77 votes

-- Akhil Nadh PC (16.5k points)

4.19.13 K Map: GATE CSE 2008 | Question: 5 [top](#)

<https://gateoverflow.in/403>



✓ 2 quads are getting formed:

ab \ cd	00	01	11	10
00	1	1		1
01	X			
11	X			
10	1	1		X

Value for first one is $a'd'$ and value for 2^{nd} one is $b'd'$.

Answer is Option A.

26 votes

-- GATE_2016 (469 points)

4.19.14 K Map: GATE CSE 2012 | Question: 30 [top](#)

<https://gateoverflow.in/1615>



✓

ab \ cd	00	01	11	10
00	1	X	X	1
01	X			1
11				
10	1			X

2 quads are getting formed.

Value for First one is $b'd'$ and value for 2^{nd} one is $b'c'$. So, **answer is option B.**

31 votes

-- GATE_2016 (469 points)

4.19.15 K Map: GATE CSE 2017 Set 1 | Question: 21 [top](#)

<https://gateoverflow.in/118301>



✓ From K-map simplification we get the min-term as CA' . So We can simplyfy it for NOR gate expression

I.e. $C \text{ NOR } A = (C' + A)' = CA'$

Now complemented inputs are also given to us so, for 2 input NOR gate **we need only 1 NOR gate.**

1 is correct answer .

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👍 51 votes

-- Aboveallplayer (12.5k points)

4.19.16 K Map: GATE CSE 2019 | Question: 30 top 5

<https://gateoverflow.in/302818>



✓ Perform $f_1 \cdot f_2$ first, then with the result perform XOR with f_3 .

$f_1 \cdot f_2$ means just take common minterms in f_1 and f_2 (WHY? due to AND gate present, the minterm should be present in both functions.)

$$f_1 \cdot f_2 = \Sigma(0, 2, 5, 8, 14) \cdot \Sigma(2, 3, 6, 8, 14, 15) = \Sigma(2, 8, 14)$$

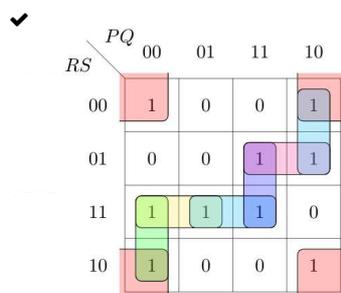
$$\Sigma(2, 8, 14) \oplus \Sigma(2, 7, 11, 14) = \Sigma(7, 8, 11)$$

👍 34 votes

-- Shaik Masthan (50.4k points)

4.19.17 K Map: GATE IT 2006 | Question: 35 top 5

<https://gateoverflow.in/3574>



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Only the top leftmost and bottom rightmost 1s have no alternate groupings. So, they form the essential prime implicants.

Answer is D. $Q'S'$

👍 22 votes

-- Ankit Kumar (265 points)

4.19.18 K Map: GATE IT 2007 | Question: 78 top 5

<https://gateoverflow.in/3530>



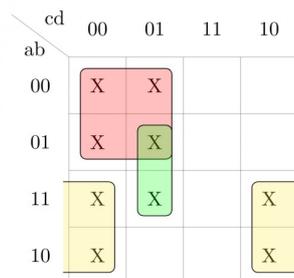
$$\begin{aligned} a\bar{d} + \bar{a}c + b\bar{c}d &= \overset{m_8}{a\bar{b}\bar{c}\bar{d}} + \overset{m_{10}}{a\bar{b}c\bar{d}} + \overset{m_{12}}{ab\bar{c}\bar{d}} + \overset{m_{14}}{abc\bar{d}} \\ &+ \overset{m_0}{\bar{a}\bar{b}\bar{c}\bar{d}} + \overset{m_4}{\bar{a}b\bar{c}\bar{d}} + \overset{m_5}{\bar{a}b\bar{c}d} + \overset{m_1}{\bar{a}b\bar{c}\bar{d}} \\ &+ \overset{m_5}{\bar{a}b\bar{c}d} + \overset{m_{13}}{ab\bar{c}\bar{d}} \end{aligned}$$

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When we minimize a K-map, we can assume either 0 or 1 for don't cares. But here they have asked for the expression

represented by the K-map. So we can consider X as 1 and not as a don't care. Also the given expression is equivalent to the above K-map but not the minimal one. Minimal expression will be $\bar{a}\bar{c} + b\bar{c} + a\bar{d}$.

Hence, Option A.

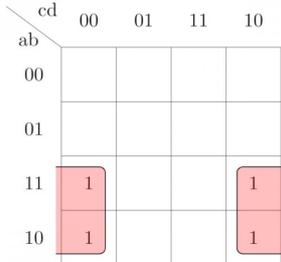
👍 10 votes

-- Arjun Suresh (332k points)



✓ ad' [fill minterm in K-map in front for a and d'] [gateoverflow.in](#)

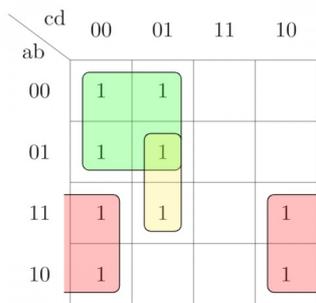
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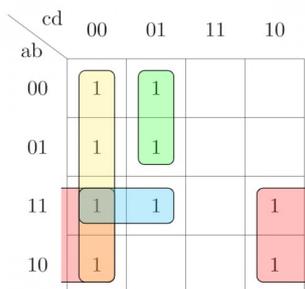
Similarly, fill all minterms for $ad' + a'c' + bc'd$, resulting K-map will be:



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Option (a) $c'd' + ad' + abc' + a'c'd$



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is equivalent to given expression

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Option (b) $a'c' + c'd' + ad' + abc'd$

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[gateoverflow.in](#)

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cd \ ab	00	01	11	10
00	1	1		
01	1	1		
11	1	1		1
10	1			1

is equivalent to given expression.

Option (c) $a'c' + ad' + abc' + c'd$

cd \ ab	00	01	11	10
00	1	1		
01	1	1		
11	1	1		1
10	1	1		1

is not equivalent to given expression.

Option (d) $b'c'd' + acd' + a'c' + abc'$

cd \ ab	00	01	11	10
00	1	1		
01	1	1		
11	1	1		1
10	1			1

is equivalent to given expression.

So, answer is C.

👍 29 votes

-- Praveen Saini (41.9k points)

4.20

Little Endian Big Endian (1) [top](#)

4.20.1 Little Endian Big Endian: GATE CSE 2021 Set 2 | Question: 44 [top](#)

<https://gateoverflow.in/357496>



If the numerical value of a 2-byte unsigned integer on a little endian computer is 255 more than that on a big endian computer, which of the following choices represent(s) the unsigned integer on a little endian computer?

A. 0x6665

- B. 0x0001
- C. 0x4243
- D. 0x0100

gate2021-cse-set2 multiple-selects digital-logic number-representation little-endian-big-endian

Answer

Answers: Little Endian Big Endian

4.20.1 Little Endian Big Endian: GATE CSE 2021 Set 2 | Question: 44

https://gateoverflow.in/357496



✓ This question is poorly framed and has interpretation ambiguity. Refer to the discussion on this question in the below link :

<https://cs.stackexchange.com/questions/135713/representation-of-unsigned-integer-on-a-little-endian-big-endian-computer>

All kinds of “interpretations” are available in that discussion.

The following is my interpretation of the question :

It is asking “which of the following choices represent(s) the unsigned integer **on a little-endian computer?**”

Take Option “0x6665” :

It is saying that 0x6665 is the representation of an integer on a little-endian computer, so, it means that the original number must have been 0x6566.

So, for the original number 0x6566 :

- On little endian(LE) : 0x6665
- On Big endian(BE) : 0x6566

Clearly, $LE = 255 + BE$

Similarly, for 0x0100.

Take 0x0100 :

It is saying that 0x0100 is the representation of an integer on a little-endian computer, so, it means that the original number must have been 0x0001.

So, for the number 0x0001 :

- On little endian(LE) : 0x0100
- On Big endian(BE) : 0x0001

Clearly, $LE = 255 + BE$

Similarly for 0x4243 and 0x0001, They do not satisfy “ $LE = 255 + BE$ ” , So, answer is option A,D.

Refer to Slide 26 in the below article :

Nice Reference: <https://www.cs.utexas.edu/~byoung/cs429/slides2-bits-bytes.pdf>

Representing Integers:

```
int A = 15213;
int B = -15213;
long int C = 15213;
```

$$15213_{10} = 0011101101101101_2 = 3B6D_{16}$$

	Linux (little endian)	Alpha (little endian)	Sun (big endian)
A	6D 3B 00 00	6D 3B 00 00	00 00 3B 6D
B	93 C4 FF FF	93 C4 FF FF	FF FF C4 93
C	6D 3B 00 00 00 00 00 00	6D 3B 00 00 00 00 00 00	00 00 00 00 00 00 3B 6D

Byte Ordering Examples:

1. Big Endian: Most significant byte has lowest (first) address.
2. Little Endian: Least significant byte has lowest address.

Example:

- Int variable x has 4-byte representation 0x01234567.

- Address gives by $\&x$ is $0x100$.

Big Endian:

Address:			0x100	0x101	0x102	0x103		
Value:			01	23	45	67		

Little Endian:

Address:			0x100	0x101	0x102	0x103		
Value:			67	45	23	01		

Note that different people are having different interpretations of this question. I have asked this question on cs.StackExchange, and you can read the discussion in the below link :

<https://cs.stackexchange.com/questions/135713/representation-of-unsigned-integer-on-a-little-endian-big-endian-computer>

References



12 votes

-- Deepak Poonia (23.4k points)

4.21

Memory Interfacing (3) top

4.21.1 Memory Interfacing: GATE CSE 1995 | Question: 2.2 top

<https://gateoverflow.in/2614>



The capacity of a memory unit is defined by the number of words multiplied by the number of bits/word. How many separate address and data lines are needed for a memory of $4K \times 16$?

- 10 address, 16 data lines
- 11 address, 8 data lines
- 12 address, 16 data lines
- 12 address, 12 data lines

gate1995

digital-logic

memory-interfacing

normal

Answer

4.21.2 Memory Interfacing: GATE CSE 2010 | Question: 7 top

<https://gateoverflow.in/2178>



The main memory unit with a capacity of 4 megabytes is built using $1M \times 1$ -bit DRAM chips. Each DRAM chip has $1K$ rows of cells with $1K$ cells in each row. The time taken for a single refresh operation is 100 nanoseconds. The time required to perform one refresh operation on all the cells in the memory unit is

- 100 nanoseconds
- 100×2^{10} nanoseconds
- 100×2^{20} nanoseconds
- 3200×2^{20} nanoseconds

gate2010-cse

digital-logic

memory-interfacing

normal

Answer

4.21.3 Memory Interfacing: GATE IT 2005 | Question: 9 top

<https://gateoverflow.in/3754>



A dynamic RAM has a memory cycle time of 64 nsec. It has to be refreshed 100 times per msec and each refresh takes 100 nsec . What percentage of the memory cycle time is used for refreshing?

- 10
- 6.4
- 1
- 0.64

Answers: Memory Interfacing

4.21.1 Memory Interfacing: GATE CSE 1995 | Question: 2.2 [top](#)<https://gateoverflow.in/2614>

- ✓ ROM memory size = $2^m \times n$

m = no. of address lines n = no. of data lines

Given, $4K \times 16$

$$= 2^2 \times 2^{10} \times 16$$

$$= 2^{12} \times 16$$

Address lines = 12

Data lines = 16

Correct Answer: C

 36 votes

-- Sanket_ (3.1k points)

4.21.2 Memory Interfacing: GATE CSE 2010 | Question: 7 [top](#)<https://gateoverflow.in/2178>

- ✓ There are $4 \times 8 = 32$ DRAM chips to get 4MB from $1M \times 1$ -bit chips. Now, all chips can be refreshed in parallel so do all cells in a row. So, the total time for refresh will be number of rows times the refresh time

$$= 1K \times 100$$

$$= 100 \times 2^{10} \text{ nanoseconds}$$

Reference: <http://www.downloads.reactivemicro.com/Public/Electronics/DRAM/DRAM%20Refresh.pdf>

Correct Answer: B

References



 60 votes

-- Arjun Suresh (332k points)

4.21.3 Memory Interfacing: GATE IT 2005 | Question: 9 [top](#)<https://gateoverflow.in/3754>

- ✓ Ans : (C) 1

In 1 ms refresh 100 times

$$\text{In } 64 \text{ ns} - \text{refresh } \frac{100}{10^{-3}} \times 64 \times 10^{-9} \text{ times}$$

$$= 10^5 \times 10^{-9} \times 64 = 64 \times 10^{-4} \text{ times}$$

In 1 memory cycle, refresh 64×10^{-4} times

1 refresh takes 100 ns

$$64 \times 10^{-4} \text{ refreshes take } 100 \times 10^{-9} \times 64 \times 10^{-4}$$

$$= 64 \times 10^{-11} \text{ s}$$

$$\therefore \% \text{ refreshing time} = \frac{\text{refreshing time in cycle}}{\text{total time}} \times 100$$

$$= \frac{64 \times 10^{-11}}{64 \times 10^{-9}} \times 100$$

$$= \frac{1}{10^2} \times 100 = 1\%$$

65 votes

-- Afaque Ahmad (727 points)

4.22

Min No Gates (4) top

4.22.1 Min No Gates: GATE CSE 2000 | Question: 9 top

<https://gateoverflow.in/680>



Design a logic circuit to convert a single digit BCD number to the number modulo six as follows (Do not detect illegal input):

- Write the truth table for all bits. Label the input bits I_1, I_2, \dots with I_1 as the least significant bit. Label the output bits R_1, R_2, \dots with R_1 as the least significant bit. Use 1 to signify truth.
- Draw one circuit for each output bit using, *altogether*, two two-input AND gates, one two-input OR gate and two NOT gates.

gate2000-cse digital-logic min-no-gates descriptive

Answer

4.22.2 Min No Gates: GATE CSE 2004 | Question: 58 top

<https://gateoverflow.in/1053>



A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5 , and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

- 2
- 3
- 4
- 5

gate2004-cse digital-logic normal min-no-gates

Answer

4.22.3 Min No Gates: GATE CSE 2009 | Question: 6 top

<https://gateoverflow.in/1298>



What is the minimum number of gates required to implement the Boolean function $(AB+C)$ if we have to use only 2-input NOR gates?

- 2
- 3
- 4
- 5

gate2009-cse digital-logic min-no-gates normal

Answer

4.22.4 Min No Gates: GATE IT 2004 | Question: 8 top

<https://gateoverflow.in/3649>



What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

- 2
- 4
- 5
- 6

gate2004-it digital-logic min-no-gates normal

Answer

Answers: Min No Gates



✓

I_4	I_3	I_2	I_1		R_3	R_2	R_1
0	0	0	0	0	0	0	0
0	0	0	1	1	0	0	1
0	0	1	0	2	0	1	0
0	0	1	1	3	0	1	1
0	1	0	0	4	1	0	0
0	1	0	1	5	1	0	1
0	1	1	0	6	0	0	0
0	1	1	1	7	0	0	1
1	0	0	0	8	0	1	0
1	0	0	1	9	0	1	1

- $R_1 = I_1$
- $R_2 = I_2 \bar{I}_3 + I_4$
- $R_3 = I_3 \bar{I}_2$

This requires 2 NOT gates, 2 two-input AND gates and 1 two-input OR gate.

👍 14 votes

-- Savir husen khan (305 points)

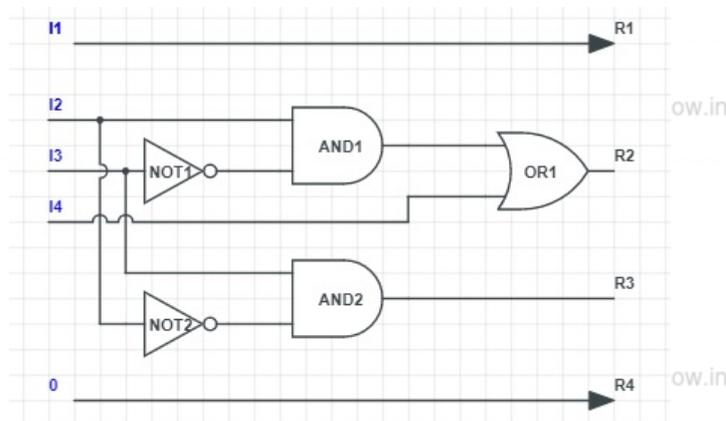
After using Don't care (10,11,12,13,14,15) and after K-Map simplification you will get

$R_1 = I_1$

$R_2 = I_2 \bar{I}_3 + I_4$

$R_3 = I_3 \bar{I}_2$

$R_4 = 0$



Here, 2 input AND Gate used=2

2 input OR Gate used=1

NOT Gate used=2

👍 11 votes

-- Krishn Kumar Gupta (1.1k points)



✓

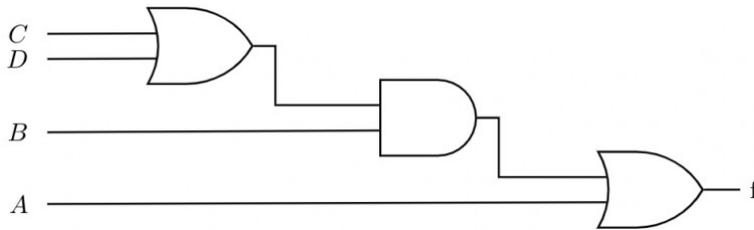
Answer should be (B). As according to question, truth table will be like:

A	B	C	D	f
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	don't care
1	0	1	1	don't care
1	1	0	0	don't care
1	1	0	1	don't care
1	1	1	0	don't care
1	1	1	1	don't care

Using this truth table we get 3 sub cube which are combined with following minterms $A(8, 9, 10, 11, 12, 13, 14, 15)$, $BD(5, 13, 7, 15)$ and $BC(6, 7, 14, 15)$

So, $f = A + BD + BC = A + B(C + D)$

So, minimum gate required 2 OR gate and 1 AND gate = 3 minimum gates.



CD \ AB	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	-	-	-	-
10	1	1	-	-

42 votes

-- minal (13.1k points)

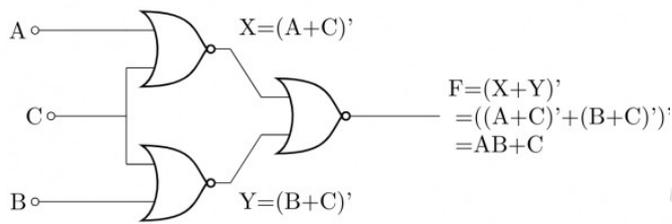
4.22.3 Min No Gates: GATE CSE 2009 | Question: 6 top

<https://gateoverflow.in/1298>



Given boolean function is

$$\begin{aligned}
 f &= AB + C \\
 &= (A + C) \cdot (B + C) \\
 &= ((A + C)' + (B + C)')'
 \end{aligned}$$



Therefore, 3 NOR gates required .

Correct Answer: B

77 votes

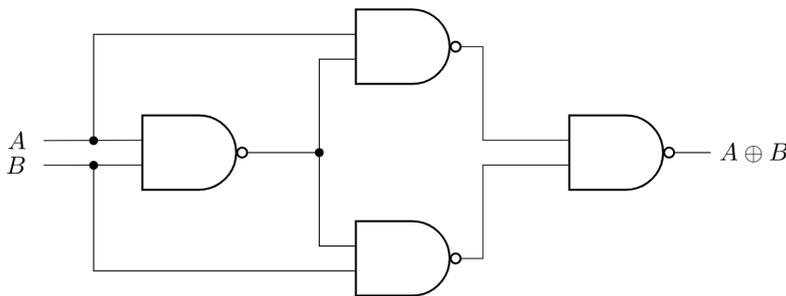
-- Mithlesh Upadhyay (4.3k points)

4.22.4 Min No Gates: GATE IT 2004 | Question: 8

<https://gateoverflow.in/3649>



Correct Option B 4.



A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

20 votes

-- Manu Madhavan (827 points)

4.23

Min Product Of Sums (2)

4.23.1 Min Product Of Sums: GATE CSE 1990 | Question: 5-a

<https://gateoverflow.in/85396>



Find the minimum product of sums of the following expression

$$f = ABC + \bar{A} \bar{B} \bar{C}$$

gate1990 digital-logic boolean-algebra min-product-of-sums canonical-normal-form descriptive

Answer

4.23.2 Min Product Of Sums: GATE CSE 2017 Set 2 | Question: 28

<https://gateoverflow.in/118370>



Given $f(w, x, y, z) = \sum_m(0, 1, 2, 3, 7, 8, 10) + \sum_d(5, 6, 11, 15)$; where d represents the 'don't-care' condition in Karnaugh maps. Which of the following is a minimum product-of-sums (POS) form of $f(w, x, y, z)$?

- A. $f = (\bar{w} + \bar{z})(\bar{x} + z)$
- B. $f = (\bar{w} + z)(x + z)$
- C. $f = (w + z)(\bar{x} + z)$
- D. $f = (w + \bar{z})(\bar{x} + z)$

gate2017-cse-set2 digital-logic min-product-of-sums

Answer

Answers: Min Product Of Sums



✓ Minimal POS

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BC	00	01	11	10
A				
0		0 0		0
1	0 0			0

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$$f = (\bar{A} + B)(A + \bar{C})(\bar{B} + C)$$

👍 26 votes

-- Lokesh Dafale (8.2k points)



✓ A. $(\bar{x} + z)(\bar{z} + \bar{w})$

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WX	00	01	11	10
YZ				
00	1	0 0		1
01	1	d	0 0	
11	1	1	d d	
10	1	d 0		1

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👍 34 votes

-- Joker (1.6k points)



Three switching functions f_1 , f_2 and f_3 are expressed below as sum of minterms.

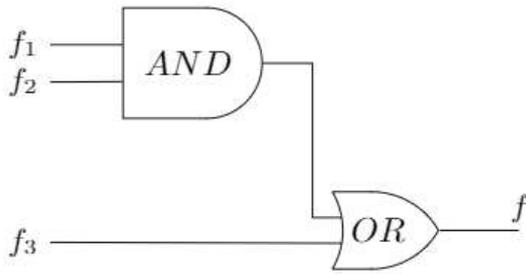
- $f_1(w, x, y, z) = \sum 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \sum 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \sum 2, 4, 5, 8$

Express the function f realised by the circuit shown in the below figure as the sum of minterms (in decimal notation).

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gate1988 descriptive digital-logic easy circuit-output min-sum-of-products-form

Answer

4.24.2 Min Sum Of Products Form: GATE CSE 1991 | Question: 5-b [top](https://gateoverflow.in/26437) <https://gateoverflow.in/26437>

Find the minimum sum of products form of the logic function $f(A, B, C, D) = \Sigma_m(0, 2, 8, 10, 15) + \Sigma_d(3, 11, 12, 14)$ where m and d represent minterm and don't care term respectively.

gate1991 digital-logic boolean-algebra min-sum-of-products-form descriptive

Answer

4.24.3 Min Sum Of Products Form: GATE CSE 1997 | Question: 71 [top](https://gateoverflow.in/19701) <https://gateoverflow.in/19701>

Let $f = (\bar{w} + y)(\bar{x} + y)(w + \bar{x} + z)(\bar{w} + z)(\bar{x} + z)$

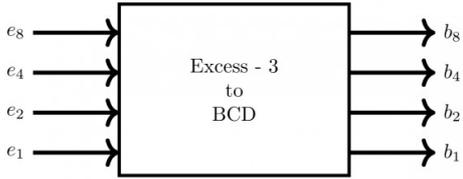
- A. Express f as the minimal sum of products. Write only the answer.
- B. If the output line is stuck at 0, for how many input combinations will the value of f be correct?

gate1997 digital-logic min-sum-of-products-form numerical-answers

Answer

4.24.4 Min Sum Of Products Form: GATE CSE 2001 | Question: 10 [top](https://gateoverflow.in/751) <https://gateoverflow.in/751>

- a. Is the 3-variable function $f = \Sigma(0, 1, 2, 4)$ its self-dual? Justify your answer.
- b. Give a minimal product-of-sum form of the b output of the following excess-3 to BCD converter.



gate2001-cse digital-logic normal descriptive min-sum-of-products-form

Answer

4.24.5 Min Sum Of Products Form: GATE CSE 2005 | Question: 18 [top](https://gateoverflow.in/1354) <https://gateoverflow.in/1354>

The switching expression corresponding to $f(A, B, C, D) = \Sigma(1, 4, 5, 9, 11, 12)$ is:

- A. $BC'D' + A'C'D + AB'D$
- B. $ABC' + ACD + B'C'D$
- C. $ACD' + A'BC' + AC'D'$
- D. $A'BD + ACD' + BCD'$

Answer

4.24.6 Min Sum Of Products Form: GATE CSE 2007 | Question: 9

https://gateoverflow.in/1207



Consider the following Boolean function of four variables:

$$f(w, x, y, z) = \Sigma(1, 3, 4, 6, 9, 11, 12, 14)$$

The function is

- A. independent of one variables.
- B. independent of two variables.
- C. independent of three variables.
- D. dependent on all variables

Answer

4.24.7 Min Sum Of Products Form: GATE CSE 2011 | Question: 14

https://gateoverflow.in/2116



The simplified SOP (Sum of Product) from the Boolean expression

$$(P + \bar{Q} + \bar{R}). (P + \bar{Q} + R). (P + Q + \bar{R})$$

is

- A. $(\bar{P}. Q + \bar{R})$
- B. $(P + \bar{Q}. \bar{R})$
- C. $(\bar{P}. Q + R)$
- D. $(P. Q + R)$

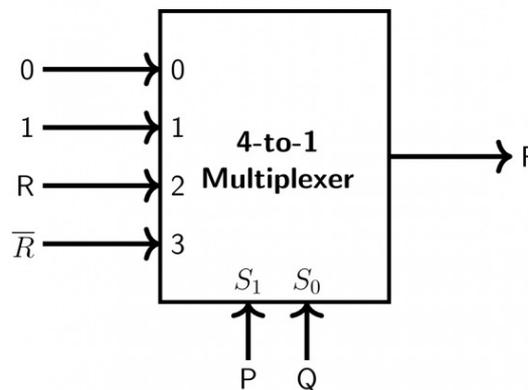
Answer

4.24.8 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 45

https://gateoverflow.in/1923



Consider the 4-to-1 multiplexer with two select lines S_1 and S_0 given below



The minimal sum-of-products form of the Boolean expression for the output F of the multiplexer is

- A. $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
- B. $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
- C. $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$

D. $PQ\bar{R}$

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gate2014-cse-set1 digital-logic normal multiplexer min-sum-of-products-form

Answer 

4.24.9 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 7 [top](#)

<https://gateoverflow.in/1764>



Consider the following Boolean expression for F :

$$F(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$$

The minimal sum-of-products form of F is

- A. $PQ + QR + QS$
- B. $P + Q + R + S$
- C. $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- D. $\bar{P}R + \bar{R}PS + P$

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gate2014-cse-set1 digital-logic normal min-sum-of-products-form

Answer 

4.24.10 Min Sum Of Products Form: GATE CSE 2014 Set 3 | Question: 7 [top](#)

<https://gateoverflow.in/2041>



Consider the following minterm expression for F :

$$F(P, Q, R, S) = \sum 0, 2, 5, 7, 8, 10, 13, 15$$

The minterms 2, 7, 8 and 13 are 'do not care' terms. The minimal sum-of-products form for F is

- A. $Q\bar{S} + \bar{Q}S$
- B. $\bar{Q}\bar{S} + QS$
- C. $\bar{Q}\bar{R}\bar{S} + \bar{Q}R\bar{S} + Q\bar{R}S + QRS$
- D. $\bar{P}\bar{Q}\bar{S} + \bar{P}QS + PQS + P\bar{Q}\bar{S}$

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gate2014-cse-set3 digital-logic min-sum-of-products-form normal

Answer 

4.24.11 Min Sum Of Products Form: GATE CSE 2018 | Question: 49 [top](#)

<https://gateoverflow.in/204124>



Consider the minterm list form of a Boolean function F given below.

$$F(P, Q, R, S) = \sum m(0, 2, 5, 7, 9, 11) + d(3, 8, 10, 12, 14)$$

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Here, m denotes a minterm and d denotes a don't care term. The number of essential prime implicants of the function F is ____

gate2018-cse digital-logic min-sum-of-products-form numerical-answers

Answer 

4.24.12 Min Sum Of Products Form: GATE CSE 2021 Set 2 | Question: 52 [top](#)

<https://gateoverflow.in/357485>



Consider a Boolean function $f(w, x, y, z)$ such that

$$\begin{aligned} f(w, 0, 0, z) &= 1 \\ f(1, x, 1, z) &= x + z \\ f(w, 1, y, z) &= wz + y \end{aligned}$$

The number of literals in the minimal sum-of-products expression of f is _____

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Answer

4.24.13 Min Sum Of Products Form: GATE IT 2008 | Question: 8 top

https://gateoverflow.in/3268



Consider the following Boolean function of four variables

$$f(A, B, C, D) = \Sigma(2, 3, 6, 7, 8, 9, 10, 11, 12, 13)$$

The function is

- A. independent of one variable
- B. independent of two variables
- C. independent of three variable
- D. dependent on all the variables

Answer

Answers: Min Sum Of Products Form

4.24.1 Min Sum Of Products Form: GATE CSE 1988 | Question: 2-v top

https://gateoverflow.in/91685



Final output = $\Sigma 0, 1, 2, 4, 5, 8$

- $f_1(w, x, y, z) = \Sigma 0, 1, 2, 3, 5, 12$
- $f_2(w, x, y, z) = \Sigma 0, 1, 2, 10, 13, 14, 15$
- $f_3(w, x, y, z) = \Sigma 2, 4, 5, 8$

f_1 AND f_2 will give the common minterms - $f_{12} = \Sigma 0, 1, 2$.

Now f_{12} OR $f_3 = \Sigma 0, 1, 2, 4, 5, 8$.

16 votes

-- kunal chaltrotra (13.6k points)

4.24.2 Min Sum Of Products Form: GATE CSE 1991 | Question: 5-b top

https://gateoverflow.in/26437



✓

	CD	00	01	11	10
AB					
00		1		X	1
01					
11		X		1	X
10		1		X	1

The minimum SOP form of the logic function is given as : $f(A, B, C, D) = B'D' + AC$.

18 votes

-- Kalpna Bhargav (2.5k points)

4.24.3 Min Sum Of Products Form: GATE CSE 1997 | Question: 71 top

https://gateoverflow.in/19701





WX \ YZ	00	01	11	10
00	1	0	0	0
01	1	0	0	0
11	1	1	1	1
10	1	0	0	0

Answer of question A: $w'x' + yz$

Answer of question B:

Stuck at 0, means output is fixed at 0 (No matter what the input is). We got 0 for 9 input combinations (Check K-Map). So, answer is **9**.

👍 28 votes

-- Akash Kanase (36k points)



There are two conditions for a function being self dual.

1. it should be a neutral function. (no. of minterms = no. of max terms)
2. no two mutually exclusive terms should be there like (0 – 7 are mutually exclusive 1 – 6, 2 – 5, 3 – 4) from these pairs only one should be there.

Clearly, there are 4 minterms, so number of minterms = no. of maxterms.
And second condition is also satisfied. So, it is a self dual function .

(b) Excess-3 to BCD

Truth Table

Inputs				Outputs			
W	X	Y	Z	A	B	C	D
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1

MAPS:

	YZ	00	01	11	10
WX					
00		X	X		X
01					
11		1	X	X	X
10				1	

Map for A
 $A = WX + WYZ$

	YZ	00	01	11	10
WX					
00		X	X		X
01				1	
11			X	X	X
10		1	1		1

Map for B
 $B = X'Y' + XYZ + X'Z'$

	YZ	00	01	11	10
WX					
00		X	X		X
01			1		1
11		X		X	X
10			1		1

Map for C
 $C = Y'Z + ZY' = Y \oplus Z$

	YZ	00	01	11	10
WX					
00		X	X		X
01		1			1
11		1	X	X	X
10		1			1

Map for D
 $D = Z'$

26 votes

-- Ravi Singh (11.8k points)

4.24.5 Min Sum Of Products Form: GATE CSE 2005 | Question: 18 [top](#)

<https://gateoverflow.in/1354>



✓ Answer is: [A]

	CD	00	01	11	10
AB					
00			1		
01		1	1		
11		1			
10			1	1	

15 votes

-- Desert_Warrior (6k points)

4.24.6 Min Sum Of Products Form: GATE CSE 2007 | Question: 9 [top](#)

<https://gateoverflow.in/1207>



✓ The K-map would be

wx \ yz	00	01	11	10
00		1	1	
01	1			1
11	1			1
10		1	1	

So, the minimized expression would be

$$x'z + xz' = x \oplus z.$$

Option B.

21 votes

-- Arjun Suresh (332k points)

4.24.7 Min Sum Of Products Form: GATE CSE 2011 | Question: 14

<https://gateoverflow.in/2116>



✓

P \ QR	00	01	11	10
0	1	0	0	0
1	1	1	1	1

K-map

Answer is B

26 votes

-- Sona Praneeth Akula (3.4k points)

4.24.8 Min Sum Of Products Form: GATE CSE 2014 Set 1 | Question: 45

<https://gateoverflow.in/1923>



✓

S_0 and S_1 are used to select the input given to be given as output.

S_0	S_1	Output
0	0	0
0	1	1
1	0	R
1	1	R'

So, output becomes 1 for $S_0' S_1 + S_0 S_1' R + S_0 S_1 R'$

$$= P'Q + PQ'R + PQR'$$

$$= P'Q + PQR' + PQ'R$$

$$= Q(P' + PR') + PQ'R$$

$$= Q(P' + R') + PQ'R (\because A + A'B = A + B)$$

$$= P'Q + QR' + PQ'R$$

Option (A)

31 votes

-- Arjun Suresh (332k points)



RS \ PQ	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	1	1	1	1
10	0	0	0	0

Minimal SOP = $PQ + QR + QS$

Hence, **option A** is correct.

32 votes

-- Amar Vashishth (25.2k points)



While putting the terms to K-map the 3rd and 4th columns are swapped so, do 3rd and 4th rows. So, term 2 is going to (0, 3) column instead of (0, 2), 8 is going to (3, 0) instead of (2, 0) etc.

RS \ PQ	00	01	11	10
00	1			X
01		1	X	
11		X	1	
10	X			1

Solving this k-map gives **B** as the answer.

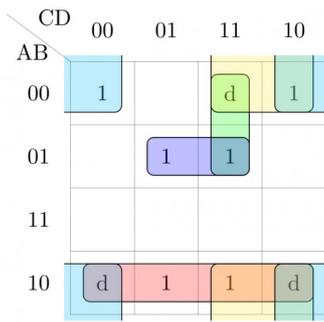
Reference: <http://www.cs.uiuc.edu/class/sp08/cs231/lectures/04-Kmap.pdf>

References



22 votes

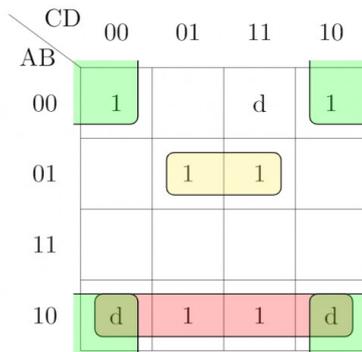
-- Srinath Jayachandran (2.9k points)



Implicant: Any product term p in SOP form such that $p \implies f$ is an implicant of f . So, we have 9 implicants for F here one corresponding to each 1 or d in the K-map.

Prime Implicant: A minimal implicant is called a prime implicant (no extra literals than required). So, we have 5 prime implicants for $F - \{\bar{A}BD, \bar{B}\bar{D}, A\bar{B}, \bar{A}CD, \bar{B}C\}$. (for each 1 or d in $K - map$ try to combine with near by 1s and do not care conditions)

Essential Prime Implicant: A prime implicant which cannot be replaced by any other for getting the output. i.e., essential prime implicants cover the output that no other combination of other prime implicants can. In K-map, this means an essential prime implicant must cover a 1 (**we do not consider don't care as essential**) which is not covered by any other prime implicant. Here, we have 3 essential prime implicants corresponding to 3 selections shown in the below $K - map$.



So, 3 Essential Prime Implicants.

References



41 votes

-- Digvijay (44.9k points)



✓

yz	00	01	11	10
wx				
00	1	1	0	0
01	0	0	1	1
11	0	1	1	1
10	1	1	1	0

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We can see 3 squares, so number of literals = $3 \times 2 = 6$.

classroom.gateover

👍 8 votes

-- zxy123 (2.8k points)

4.24.13 Min Sum Of Products Form: GATE IT 2008 | Question: 8 top

<https://gateoverflow.in/3268>



✓

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	CD	00	01	11	10
AB					
00				1	1
01				1	1
11		1	1		
10		1	1	1	1

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$$\begin{aligned}
 (2, 3, 6, 7) & : \bar{A}C \\
 (2, 3, 10, 11) & : \bar{B}C \\
 (8, 9, 12, 13) & : A\bar{C} \\
 \hline
 y & = \bar{A}C + \bar{B}C + A\bar{C}
 \end{aligned}$$

Option A.

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👍 21 votes

-- Aditi Tiwari (879 points)

4.25

Multiplexer (13) top

4.25.1 Multiplexer: GATE CSE 1987 | Question: 1-IV top

<https://gateoverflow.in/80193>



The output F of the below multiplexer circuit can be represented by

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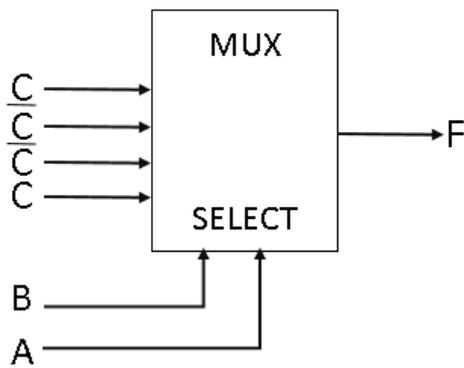
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- A. $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$
- B. $A \oplus B \oplus C$
- C. $A \oplus B$
- D. $\bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C}$

gate1987 digital-logic combinational-circuits multiplexer circuit-output

Answer

4.25.2 Multiplexer: GATE CSE 1990 | Question: 5-b

<https://gateoverflow.in/85398>



Show with the help of a block diagram how the Boolean function :

$$f = AB + BC + CA$$

can be realised using only a 4 : 1 multiplexer.

gate1990 descriptive digital-logic combinational-circuits multiplexer

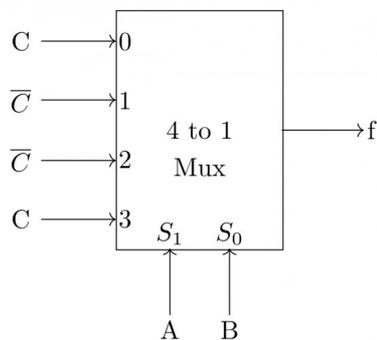
Answer

4.25.3 Multiplexer: GATE CSE 1996 | Question: 2.22

<https://gateoverflow.in/2751>



Consider the circuit in figure. f implements



- A. $\bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC$
- B. $A + B + C$
- C. $A \oplus B \oplus C$
- D. $AB + BC + CA$

gate1996 digital-logic circuit-output easy multiplexer

Answer

4.25.4 Multiplexer: GATE CSE 1998 | Question: 1.14

<https://gateoverflow.in/1651>



A multiplexer with a 4-bit data select input is a

- A. 4 : 1 multiplexer
- B. 2 : 1 multiplexer
- C. 16 : 1 multiplexer
- D. 8 : 1 multiplexer

gate1998 digital-logic multiplexer easy

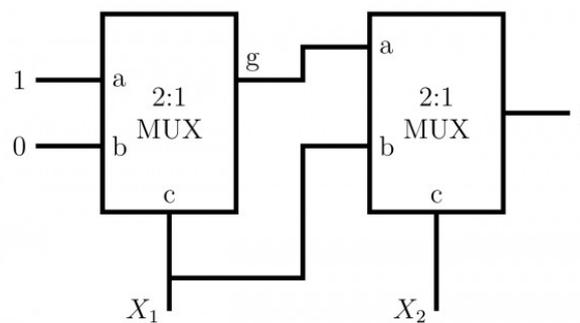
Answer

4.25.5 Multiplexer: GATE CSE 2001 | Question: 2.11

<https://gateoverflow.in/729>



Consider the circuit shown below. The output of a 2 : 1 MUX is given by the function $(ac' + bc)$.



Which of the following is true?

- A. $f = X_1' + X_2$
- B. $f = X_1'X_2 + X_1X_2'$
- C. $f = X_1X_2 + X_1'X_2'$
- D. $f = X_1 + X_2'$

gate2001-cse digital-logic normal multiplexer

Answer

4.25.6 Multiplexer: GATE CSE 2004 | Question: 60

<https://gateoverflow.in/1055>



Consider a multiplexer with X and Y as data inputs and Z as the control input. $Z = 0$ selects input X , and $Z = 1$ selects input Y . What are the connections required to realize the 2-variable Boolean function $f = T + R$, without using any additional hardware?

- A. R to X, 1 to Y, T to Z
- B. T to X, R to Y, T to Z
- C. T to X, R to Y, 0 to Z
- D. R to X, 0 to Y, T to Z

gate2004-cse digital-logic normal multiplexer

Answer

4.25.7 Multiplexer: GATE CSE 2007 | Question: 34

<https://gateoverflow.in/1232>



Suppose only one multiplexer and one inverter are allowed to be used to implement any Boolean function of n variables. What is the minimum size of the multiplexer needed?

- A. 2^n line to 1 line
- B. 2^{n+1} line to 1 line

C. 2^{n-1} line to 1line

D. 2^{n-2} line to 1line

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gate2007-cse digital-logic normal multiplexer

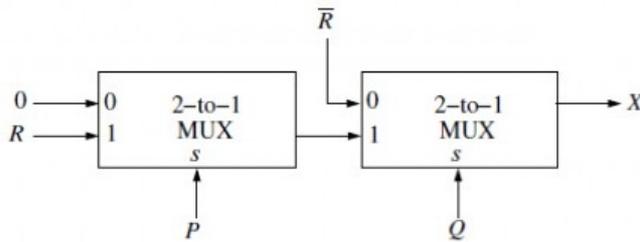
Answer

4.25.8 Multiplexer: GATE CSE 2016 Set 1 | Question: 30

https://gateoverflow.in/39722



Consider the two cascade 2 to 1 multiplexers as shown in the figure .



The minimal sum of products form of the output X is

- A. $\overline{P} \overline{Q} + PQR$
- B. $\overline{P} \overline{Q} + QR$
- C. $PQ + \overline{P} \overline{Q} R$
- D. $\overline{Q} \overline{R} + PQR$

gate2016-cse-set1 digital-logic multiplexer normal

Answer

4.25.9 Multiplexer: GATE CSE 2020 | Question: 19

https://gateoverflow.in/333212



A multiplexer is placed between a group of 32 registers and an accumulator to regulate data movement such that at any given point in time the content of only one register will move to the accumulator. The number of select lines needed for the multiplexer is _____.

gate2020-cse numerical-answers digital-logic multiplexer

Answer

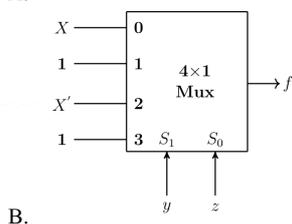
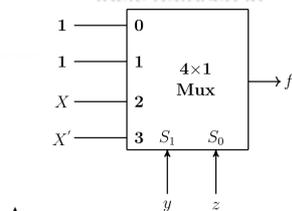
4.25.10 Multiplexer: GATE CSE 2021 Set 2 | Question: 5

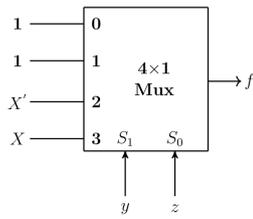
https://gateoverflow.in/357535



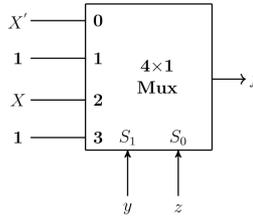
Which one of the following circuits implements the Boolean function given below?

$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6, \text{ where } m_i \text{ is the } i^{\text{th}} \text{ minterm.}$$





C.



D.

gate2021-cse-set2 digital-logic combinational-circuits multiplexer

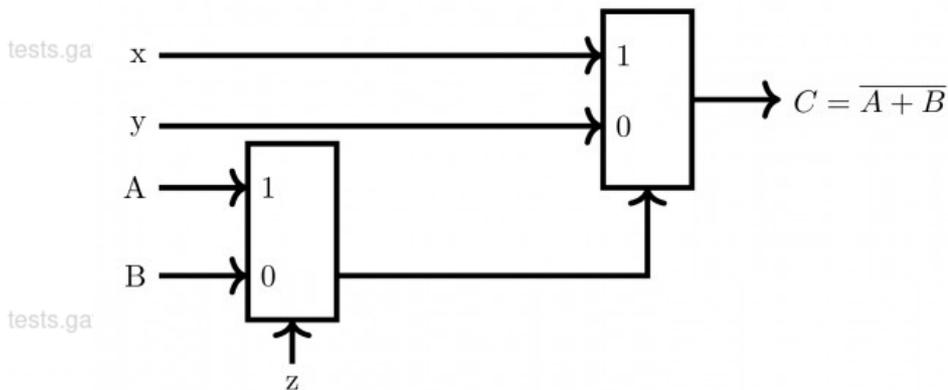
Answer

4.25.11 Multiplexer: GATE IT 2005 | Question: 48

<https://gateoverflow.in/3809>



The circuit shown below implements a 2-input NOR gate using two 2 – 4 MUX (control signal 1 selects the upper input). What are the values of signals x, y and z ?



- A. 1, 0, B
- B. 1, 0, A
- C. 0, 1, B
- D. 0, 1, A

gate2005-it digital-logic normal multiplexer

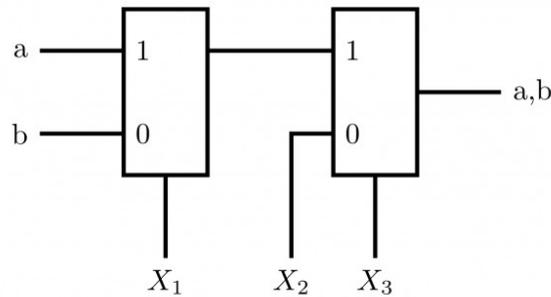
Answer

4.25.12 Multiplexer: GATE IT 2007 | Question: 8

<https://gateoverflow.in/3441>



The following circuit implements a two-input AND gate using two 2 – 1 multiplexers.



What are the values of X_1, X_2, X_3 ?

- A. $X_1 = b, X_2 = 0, X_3 = a$
- B. $X_1 = b, X_2 = 1, X_3 = b$
- C. $X_1 = a, X_2 = b, X_3 = 1$
- D. $X_1 = a, X_2 = 0, X_3 = b$

gate2007-it digital-logic normal multiplexer

Answer

4.25.13 Multiplexer: GATE1992-04-b [top](#)

<https://gateoverflow.in/17407>



A priority encoder accepts three input signals (A, B and C) and produces a two-bit output (X_1, X_0) corresponding to the highest priority active input signal. Assume A has the highest priority followed by B and C has the lowest priority. If none of the inputs are active the output should be 00 , design the priority encoder using $4 : 1$ multiplexers as the main components.

gate1992 digital-logic combinational-circuits multiplexer descriptive

Answer

Answers: Multiplexer

4.25.1 Multiplexer: GATE CSE 1987 | Question: 1-IV [top](#)

<https://gateoverflow.in/80193>



✓ Answer is B)

$$\begin{aligned} & A'B'C + AB'C' + A'BC' + ABC \\ &= (A + B')(A' + B)C + A'BC' + AB'C' \\ &= A \oplus B \oplus C \end{aligned}$$

18 votes

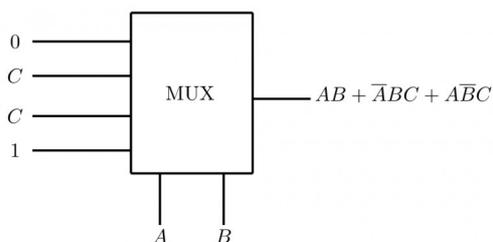
-- srestha (85.2k points)

4.25.2 Multiplexer: GATE CSE 1990 | Question: 5-b [top](#)

<https://gateoverflow.in/85398>



✓ $AB + BC + CA = AB + A'BC + AB'C$



18 votes

-- kirti singh (2.6k points)



✓

- $0 - C$ will be selected for $A = 0, B = 0$.
- $1 - \bar{C}$ will be selected for $A = 0, B = 1$.
- $2 - \bar{C}$ will be selected for $A = 1, B = 0$.
- $3 - C$ will be selected for $A = 1, B = 1$.

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$$\text{So, } f = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$

$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$

$$= \bar{A}(B \oplus C) + A(B \odot C)$$

$$= \bar{A}(B \oplus C) + A(\overline{B \oplus C})$$

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$$= A \oplus B \oplus C$$

Correct Answer: C

👍 25 votes

-- Arjun Suresh (332k points)



✓

for n bit data select input

$$2^n : 1$$

for 4 it is 16 : 1

Correct Answer: C

👍 27 votes

-- Bhagirathi Nayak (11.7k points)



✓

$$g = X_1'$$

$$\text{So, } f = ac' + bc$$

$$= X_1'X_2' + X_1X_2$$

So, (C).ssroom.gateoverflow.in

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👍 30 votes

-- Arjun Suresh (332k points)



✓

Answer is **option A**.

$$Z'X + ZY$$

Put $Z = T, X = R, Y = 1$ in $Z'X + ZY$

$$= T'R + 1 * T$$

$$= (T + T')(T + R)$$

$$= T + R$$

👍 27 votes

-- Digvijay (44.9k points)



✓

$$2^{n-1} \text{ to } 1$$

We will map $(n - 1)$ variables to select lines and 1 variable to input line

44 votes

-- Anurag Semwal (6.7k points)

4.25.8 Multiplexer: GATE CSE 2016 Set 1 | Question: 30

https://gateoverflow.in/39722



For 2 : 1 MUX, output $Y = S'I_0 + SI_1$

So, output of MUX1, $f_1 = P'0 + PR = PR$

Output of MUX2, $f_2 = Q'R' + Qf_1 = Q'R' + PQR$

which is option D

43 votes

-- Monanshi Jain (7k points)

4.25.9 Multiplexer: GATE CSE 2020 | Question: 19

https://gateoverflow.in/333212



If there are 'm' select lines for a multiplexor, then it may have up to 2^m input lines.

Given that there are 32 input lines. So, there must be $\lceil \log_2 n \rceil = \lceil \log_2 32 \rceil = 5$ select lines.

12 votes

-- Shaik Masthan (50.4k points)

4.25.10 Multiplexer: GATE CSE 2021 Set 2 | Question: 5

https://gateoverflow.in/357535



- $f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6$
- $S_1 = y, S_0 = z$

Draw a small table as following and mark the min-terms in f.

	I_0	I_1	I_2	I_3
\bar{x}	0	1	2	3
x	4	5	6	7

$I_0 = (\bar{x} + x) = 1$ (both rows are marked)

$I_1 = (\bar{x} + x) = 1$ (both rows are marked)

$I_2 = x$ (only row corresponding to x is marked)

$I_3 = \bar{x}$ (only row corresponding to \bar{x} is marked)

A is correct.

2 votes

-- Nikhil Dhama (2.5k points)

4.25.11 Multiplexer: GATE IT 2005 | Question: 48

https://gateoverflow.in/3809



$f = Az + B\bar{z}$ (As A will be selected when z is high).

So, next function will become $g = xf + y\bar{f}$

$= x(Az + B\bar{z}) + y(\overline{Az + B\bar{z}})$

Putting $x = 0, y = 1, z = A$, we get $g = \overline{AA + B\bar{A}} = \overline{A + B}$ ($\because A + B\bar{A} = A + B$) and answer will become D

38 votes

-- John Carter (1.4k points)

4.25.12 Multiplexer: GATE IT 2007 | Question: 8

https://gateoverflow.in/3441



Answer: A

$F = (bX'_1 + aX_1)X_3 + X_2X'_3$

Put $X_1 = b, X_2 = 0, X_3 = a$ to get $F = ab$.

👍 26 votes

-- Rajarshi Sarkar (27.9k points)

4.25.13 Multiplexer: GATE1992-04-b [top](#)

<https://gateoverflow.in/17407>



✓ MSB – Most Significant Bit
LSB – Least Significant Bit

TRUTH TABLE

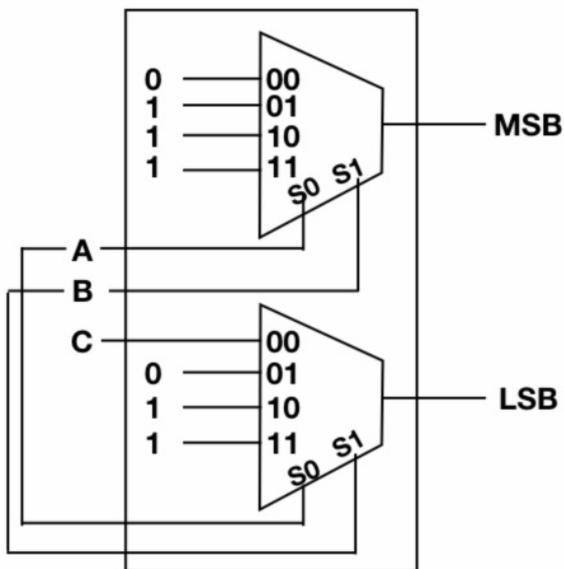
Inputs : A, B, C

Outputs : MSB, LSB

A	B	C	MSB	LSB
0	0	0	0	0
0	0	1	0	1
0	1	X	1	0
1	X	X	1	1

$$\text{MSB} = A + B$$

$$\text{LSB} = A + \overline{B}C$$



It can be implemented using two 4×1 Multiplexers.

👍 34 votes

-- Anurag Pandey (10.5k points)

4.26

Number Representation (51) [top](#)

4.26.1 Number Representation: GATE CSE 1988 | Question: 2-vi [top](#)

<https://gateoverflow.in/91687>



Define the value of r in the following: $\sqrt{(41)_r} = (7)_{10}$

gate1988 digital-logic normal number-representation descriptive

Answer

4.26.2 Number Representation: GATE CSE 1990 | Question: 1-viii [top](#)

<https://gateoverflow.in/87055>



The condition for overflow in the addition of two 2^l 's complement numbers in terms of the carry generated by the two most significant bits is _____.

gate1990 digital-logic number-representation fill-in-the-blanks

Answer 

4.26.3 Number Representation: GATE CSE 1991 | Question: 01-iii [top](#) 

<https://gateoverflow.in/503>



Consider the number given by the decimal expression:

$$16^3 * 9 + 16^2 * 7 + 16 * 5 + 3$$

The number of 1's in the unsigned binary representation of the number is _____

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gate1991 digital-logic number-representation normal numerical-answers

Answer 

4.26.4 Number Representation: GATE CSE 1991 | Question: 01-v [top](#) 

<https://gateoverflow.in/503>



When two 4-bit numbers $A = a_3a_2a_1a_0$ and $B = b_3b_2b_1b_0$ are multiplied, the bit c_1 of the product C is given by _____

gate1991 digital-logic normal number-representation fill-in-the-blanks

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Answer 

4.26.5 Number Representation: GATE CSE 1992 | Question: 4-a [top](#) 

<https://gateoverflow.in/583>



Consider addition in two's complement arithmetic. A carry from the most significant bit does not always correspond to an overflow. Explain what is the condition for overflow in two's complement arithmetic.

gate1992 digital-logic normal number-representation descriptive

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Answer 

4.26.6 Number Representation: GATE CSE 1993 | Question: 6.5 [top](#) 

<https://gateoverflow.in/2286>



Convert the following numbers in the given bases into their equivalents in the desired bases:

A. $(110.101)_2 = (x)_{10}$

B. $(1118)_{10} = (y)_H$

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gate1993 digital-logic number-representation normal descriptive

Answer 

4.26.7 Number Representation: GATE CSE 1994 | Question: 2.7 [top](#) 

<https://gateoverflow.in/2474>



Consider n -bit (including sign bit) 2's complement representation of integer numbers. The range of integer values, N , that can be represented is $_____ \leq N \leq _____$.

gate1994 digital-logic number-representation easy fill-in-the-blanks

Answer 

4.26.8 Number Representation: GATE CSE 1995 | Question: 18 [top](#) 

<https://gateoverflow.in/2655>



The following is an incomplete Pascal function to convert a given decimal integer (in the range -8 to $+7$) into a binary integer in 2's complement representation. Determine the expressions A , B , C that complete program.

```
function TWOSCOMPS (N:integer):integer;
var
  REM, EXPONENT:integer;
  BINARY :integer;
begin
  if (N>=-8) and (N<=+7) then
  begin
    if N<0 then
      N:=-A;
    BINARY:=0;
    EXPONENT:=1;
    while N<>0 do
```

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```

begin
    REM:=N mod 2;
    BINARY:=BINARY + B*EXPONENT;
    EXPONENT:=EXPONENT*10;
    N:=C
end
TWOSCOMP:=BINARY
end
end;
```

gate1995 digital-logic number-representation normal descriptive

Answer

4.26.9 Number Representation: GATE CSE 1995 | Question: 2.12, ISRO2015-9 top

https://gateoverflow.in/2624



The number of 1's in the binary representation of $(3 * 4096 + 15 * 256 + 5 * 16 + 3)$ are:

- A. 8
- B. 9
- C. 10
- D. 12

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gate1995 digital-logic number-representation normal isro2015

Answer

4.26.10 Number Representation: GATE CSE 1996 | Question: 1.25 top

https://gateoverflow.in/2729



Consider the following floating-point number representation.

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31	24	23	0
Exponent		Mantissa	

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The exponent is in 2's complement representation and the mantissa is in the sign-magnitude representation. The range of the magnitude of the normalized numbers in this representation is

- A. 0 to 1
- B. 0.5 to 1
- C. 2^{-23} to 0.5
- D. 0.5 to $(1 - 2^{-23})$

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gate1996 digital-logic number-representation normal

Answer

4.26.11 Number Representation: GATE CSE 1997 | Question: 5.4 top

https://gateoverflow.in/2255



Given $\sqrt{(224)_r} = (13)_r$.

The value of the radix r is:

- A. 10
- B. 8
- C. 5
- D. 6

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gate1997 digital-logic number-representation normal

Answer

4.26.12 Number Representation: GATE CSE 1998 | Question: 1.17 top

https://gateoverflow.in/1654



The octal representation of an integer is $(342)_8$. If this were to be treated as an eight-bit integer in an 8085 based computer, its decimal equivalent is

- A. 226
- B. -98
- C. 76

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D. -30

gate1998 digital-logic number-representation normal 8085

Answer

4.26.13 Number Representation: GATE CSE 1998 | Question: 2.20 [top](#)

<https://gateoverflow.in/1693>



Suppose the domain set of an attribute consists of signed four digit numbers. What is the percentage of reduction in storage space of this attribute if it is stored as an integer rather than in character form?

- A. 80%
- B. 20%
- C. 60%
- D. 40%

gate1998 digital-logic number-representation normal

Answer

4.26.14 Number Representation: GATE CSE 1999 | Question: 2.17 [top](#)

<https://gateoverflow.in/1495>



Zero has two representations in

- A. Sign-magnitude
- B. $2's$ complement
- C. $1's$ complement
- D. None of the above

gate1999 digital-logic number-representation easy multiple-selects

Answer

4.26.15 Number Representation: GATE CSE 2000 | Question: 1.6 [top](#)

<https://gateoverflow.in/629>



The number 43 in $2's$ complement representation is

- A. 01010101
- B. 11010101
- C. 00101011
- D. 10101011

gate2000-cse digital-logic number-representation easy

Answer

4.26.16 Number Representation: GATE CSE 2000 | Question: 2.14 [top](#)

<https://gateoverflow.in/661>



Consider the values of $A = 2.0 \times 10^{30}$, $B = -2.0 \times 10^{30}$, $C = 1.0$, and the sequence

$X := A + B$	$Y := A + C$
$X := X + C$	$Y := Y + B$

executed on a computer where floating point numbers are represented with 32 bits. The values for X and Y will be

- A. $X = 1.0, Y = 1.0$
- B. $X = 1.0, Y = 0.0$
- C. $X = 0.0, Y = 1.0$
- D. $X = 0.0, Y = 0.0$

gate2000-cse digital-logic number-representation normal

Answer

4.26.17 Number Representation: GATE CSE 2001 | Question: 2.10 [top](#)

<https://gateoverflow.in/728>



The 2^i 's complement representation of $(-539)_{10}$ in hexadecimal is

- A. *ABE*
- B. *DBC*
- C. *DE5*
- D. *9E7*

gate2001-cse digital-logic number-representation easy

Answer

4.26.18 Number Representation: GATE CSE 2002 | Question: 1.14 [top](#)

<https://gateoverflow.in/818>



The decimal value 0.25

- A. is equivalent to the binary value 0.1
- B. is equivalent to the binary value 0.01
- C. is equivalent to the binary value 0.00111
- D. cannot be represented precisely in binary

gate2002-cse digital-logic number-representation easy

Answer

4.26.19 Number Representation: GATE CSE 2002 | Question: 1.15 [top](#)

<https://gateoverflow.in/819>



The 2^i 's complement representation of the decimal value -15 is

- A. 1111
- B. 11111
- C. 111111
- D. 10001

gate2002-cse digital-logic number-representation easy

Answer

4.26.20 Number Representation: GATE CSE 2002 | Question: 1.16 [top](#)

<https://gateoverflow.in/821>



Sign extension is a step in

- A. floating point multiplication
- B. signed 16 bit integer addition
- C. arithmetic left shift
- D. converting a signed integer from one size to another

gate2002-cse digital-logic easy number-representation

Answer

4.26.21 Number Representation: GATE CSE 2002 | Question: 1.21 [top](#)

<https://gateoverflow.in/826>



In 2^i 's complement addition, overflow

- A. is flagged whenever there is carry from sign bit addition
- B. cannot occur when a positive value is added to a negative value
- C. is flagged when the carries from sign bit and previous bit match
- D. None of the above

gate2002-cse digital-logic number-representation normal

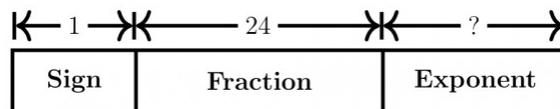
Answer



Consider the following 32-bit floating-point representation scheme as shown in the format below. A value is specified by 3 fields, a one bit sign field (with 0 for positive and 1 for negative values), a 24 bit fraction field (with the binary point is at the left end of the fraction bits), and a 7 bit exponent field (in excess-64 signed integer representation, with 16 is the base of exponentiation). The sign bit is the most significant bit.

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- A. It is required to represent the decimal value -7.5 as a normalized floating point number in the given format. Derive the values of the various fields. Express your final answer in the hexadecimal.
- B. What is the largest value that can be represented using this format? Express your answer as the nearest power of 10.

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gate2002-cse digital-logic number-representation normal descriptive

Answer



Assuming all numbers are in 2^s complement representation, which of the following numbers is divisible by 1111011?

- A. 11100111
- B. 11100100
- C. 11010111
- D. 11011011

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gate2003-cse digital-logic number-representation normal

Answer



If 73_x (in base- x number system) is equal to 54_y (in base- y -number system), the possible values of x and y are

- A. 8, 16
- B. 10, 12
- C. 9, 13
- D. 8, 11

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gate2004-cse digital-logic number-representation easy

Answer



What is the result of evaluating the following two expressions using three-digit floating point arithmetic with rounding?

$(113. + -111.) + 7.51$

$113. + (-111. + 7.51)$

- A. 9.51 and 10.0 respectively
- B. 10.0 and 9.51 respectively
- C. 9.51 and 9.51 respectively
- D. 10.0 and 10.0 respectively

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gate2004-cse digital-logic number-representation normal

Answer



Let $A = 11111010$ and $B = 00001010$ be two 8-bit 2's complement numbers. Their product in 2's complement is

- A. 11000100
- B. 10011100
- C. 10100101
- D. 11010101

gate2004-cse digital-logic number-representation easy

Answer



The range of integers that can be represented by an n bit 2's complement number system is:

- A. -2^{n-1} to $(2^{n-1} - 1)$
- B. $-(2^{n-1} - 1)$ to $(2^{n-1} - 1)$
- C. -2^{n-1} to 2^{n-1}
- D. $-(2^{n-1} + 1)$ to $(2^{n-1} - 1)$

gate2005-cse digital-logic number-representation easy isro2009 isro2015

Answer



The hexadecimal representation of $(657)_8$ is:

- A. 1AF
- B. D78
- C. D71
- D. 32F

gate2005-cse digital-logic number-representation easy

Answer



We consider the addition of two 2's complement numbers $b_{n-1}b_{n-2}\dots b_0$ and $a_{n-1}a_{n-2}\dots a_0$. A binary adder for adding unsigned binary numbers is used to add the two numbers. The sum is denoted by $c_{n-1}c_{n-2}\dots c_0$ and the carry-out by c_{out} . Which one of the following options correctly identifies the overflow condition?

- A. $c_{out} \oplus (a_{n-1} \oplus b_{n-1})$
- B. $a_{n-1}b_{n-1}c_{n-1} + a_{n-1}b_{n-1}c_{n-1}$
- C. $c_{out} \oplus c_{n-1}$
- D. $a_{n-1} \oplus b_{n-1} \oplus c_{n-1}$

gate2006-cse digital-logic number-representation normal

Answer



Let r denote number system radix. The only value(s) of r that satisfy the equation $\sqrt{121_r} = 11_r$, is/are

- A. decimal 10
- B. decimal 11
- C. decimal 10 and 11
- D. any value > 2

Answer

4.26.31 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57 [top](https://gateoverflow.in/1297) <https://gateoverflow.in/1297>



$(1217)_8$ is equivalent to

- A. $(1217)_{16}$
- B. $(028F)_{16}$
- C. $(2297)_{10}$
- D. $(0B17)_{16}$

Answer

4.26.32 Number Representation: GATE CSE 2010 | Question: 8 [top](https://gateoverflow.in/2179) <https://gateoverflow.in/2179>



P is a 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. The 2's complement representation of $8 \times P$ is

- A. $(C3D8)_{16}$
- B. $(187B)_{16}$
- C. $(F878)_{16}$
- D. $(987B)_{16}$

Answer

4.26.33 Number Representation: GATE CSE 2013 | Question: 4 [top](https://gateoverflow.in/1413) <https://gateoverflow.in/1413>



The smallest integer that can be represented by an 8-bit number in 2's complement form is

- A. -256
- B. -128
- C. -127
- D. 0

Answer

4.26.34 Number Representation: GATE CSE 2014 Set 1 | Question: 8 [top](https://gateoverflow.in/1766) <https://gateoverflow.in/1766>



The base (or radix) of the number system such that the following equation holds is _____.

$$\frac{312}{20} = 13.1$$

Answer

4.26.35 Number Representation: GATE CSE 2014 Set 2 | Question: 8 [top](https://gateoverflow.in/1871) <https://gateoverflow.in/1871>



Consider the equation $(123)_5 = (x8)_y$ with x and y as unknown. The number of possible solutions is _____.

Answer

4.26.36 Number Representation: GATE CSE 2015 Set 3 | Question: 35 [top](https://gateoverflow.in/8494) <https://gateoverflow.in/8494>



Consider the equation $(43)_x = (y3)_8$ where x and y are unknown. The number of possible solutions is _____

gate2015-cse-set3 digital-logic number-representation normal numerical-answers

Answer 

4.26.37 Number Representation: GATE CSE 2016 Set 1 | Question: 07 [top](#) 

<https://gateoverflow.in/39549>



The 16-bit 2's complement representation of an integer is 1111 1111 1111 0101; its decimal representation is _____

gate2016-cse-set1 digital-logic number-representation normal numerical-answers

Answer 

4.26.38 Number Representation: GATE CSE 2016 Set 2 | Question: 09 [top](#) 

<https://gateoverflow.in/39546>



Let X be the number of distinct 16-bit integers in 2's complement representation. Let Y be the number of distinct 16-bit integers in sign magnitude representation. Then $X - Y$ is _____.

gate2016-cse-set2 digital-logic number-representation normal numerical-answers

Answer 

4.26.39 Number Representation: GATE CSE 2017 Set 1 | Question: 9 [top](#) 

<https://gateoverflow.in/118289>



When two 8-bit numbers $A_7 \dots A_0$ and $B_7 \dots B_0$ in 2's complement representation (with A_0 and B_0 as the least significant bits) are added using a **ripple-carry adder**, the sum bits obtained are $S_7 \dots S_0$ and the carry bits are $C_7 \dots C_0$. An overflow is said to have occurred if

- A. the carry bit C_7 is 1
- B. all the carry bits (C_7, \dots, C_0) are 1
- C. $(A_7 \cdot B_7 \cdot \bar{S}_7 + \bar{A}_7 \cdot \bar{B}_7 \cdot S_7)$ is 1
- D. $(A_0 \cdot B_0 \cdot \bar{S}_0 + \bar{A}_0 \cdot \bar{B}_0 \cdot S_0)$ is 1

gate2017-cse-set1 digital-logic number-representation

Answer 

4.26.40 Number Representation: GATE CSE 2017 Set 2 | Question: 1 [top](#) 

<https://gateoverflow.in/118337>



The representation of the value of a 16-bit unsigned integer X in hexadecimal number system is $BCA9$. The representation of the value of X in octal number system is

- A. 571244
- B. 736251
- C. 571247
- D. 136251

gate2017-cse-set2 digital-logic number-representation

Answer 

4.26.41 Number Representation: GATE CSE 2019 | Question: 22 [top](#) 

<https://gateoverflow.in/302826>



Two numbers are chosen independently and uniformly at random from the set $\{1, 2, \dots, 13\}$.

The probability (rounded off to 3 decimal places) that their 4-bit (unsigned) binary representations have the same most significant bit is _____.

gate2019-cse numerical-answers digital-logic number-representation probability

Answer 



In 16-bit 2's complement representation, the decimal number -28 is:

- A. 1111 1111 0001 1100
- B. 0000 0000 1110 0100
- C. 1111 1111 1110 0100
- D. 1000 0000 1110 0100

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gate2019-cse digital-logic number-representation

Answer



Consider $Z = X - Y$ where X, Y and Z are all in sign-magnitude form. X and Y are each represented in n bits. To avoid overflow, the representation of Z would require a minimum of:

- A. n bits
- B. $n - 1$ bits
- C. $n + 1$ bits
- D. $n + 2$ bits

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gate2019-cse digital-logic number-representation

Answer



Let the representation of a number in base 3 be 210. What is the hexadecimal representation of the number?

- A. 15
- B. 21
- C. D2
- D. 528

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gate2021-cse-set1 digital-logic number-representation normal

Answer



If x and y are two decimal digits and $(0.1101)_2 = (0.8xy5)_{10}$, the decimal value of $x + y$ is _____

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gate2021-cse-set2 numerical-answers digital-logic number-representation

Answer



Using a 4-bit 2's complement arithmetic, which of the following additions will result in an overflow?

- i. $1100 + 1100$
- ii. $0011 + 0111$
- iii. $1111 + 0111$

- A. i only
- B. ii only
- C. iii only
- D. i and iii only

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gate2004-it digital-logic number-representation normal

Answer



The number $(123456)_8$ is equivalent to

- A. $(A72E)_{16}$ and $(22130232)_4$
- B. $(A72E)_{16}$ and $(22131122)_4$
- C. $(A73E)_{16}$ and $(22130232)_4$
- D. $(A62E)_{16}$ and $(22120232)_4$

gate2004-it digital-logic number-representation normal

Answer



$(34.4)_8 \times (23.4)_8$ evaluates to

- A. $(1053.6)_8$
- B. $(1053.2)_8$
- C. $(1024.2)_8$
- D. None of these

gate2005-it digital-logic number-representation normal

Answer



The addition of 4 – bit, two's complement, binary numbers 1101 and 0100 results in

- A. 0001 and an overflow
- B. 1001 and no overflow
- C. 0001 and no overflow
- D. 1001 and an overflow

gate2006-it digital-logic number-representation normal isro2009

Answer



$(C012.25)_H - (10111001110.101)_B =$

- A. $(135103.412)_o$
- B. $(564411.412)_o$
- C. $(564411.205)_o$
- D. $(135103.205)_o$

gate2007-it digital-logic number-representation normal

Answer



A processor that has the carry, overflow and sign flag bits as part of its program status word (PSW) performs addition of the following two 2's complement numbers 01001101 and 11101001. After the execution of this addition operation, the status of the carry, overflow and sign flags, respectively will be:

- A. 1, 1, 0
- B. 1, 0, 0
- C. 0, 1, 0
- D. 1, 0, 1

gate2008-it digital-logic number-representation normal

4.26.1 Number Representation: GATE CSE 1988 | Question: 2-vi [top](#)

<https://gateoverflow.in/91687>



✓ $\sqrt{41_r} = 7_{10}$

Squaring both sides we get

$41_r = 49_{10}$

$\implies 4r + 1 = 10 \times 4 + 9$

$\implies 4r = 48$

$\implies r = 12.$

23 votes

-- kunal chalotra (13.6k points)

4.26.2 Number Representation: GATE CSE 1990 | Question: 1-viii [top](#)

<https://gateoverflow.in/87058>



✓ The condition for overflow in the addition of two 2's complement numbers in terms of the carry generated by the two most significant bits is when carry on MSB but not From MSB, or Carry from MSB but not on MSB. i.e.,

$$C_{out} \oplus C_{n-1} = 1.$$

i.e. For overflow to happen during addition of two numbers in 2's complement form

! They must have same sign and result is of opposite sign Overflow occurs if 1. (+A) + (+B) = -C 2. (-A) + (-B) = +C

PS: Overflow is useful for signed numbers and useless for unsigned numbers

21 votes

-- Prashant Singh (47.2k points)

4.26.3 Number Representation: GATE CSE 1991 | Question: 01-iii [top](#)

<https://gateoverflow.in/500>



✓ The hex representation of given no. is $(9753)_{16}$

Its binary representation is $(1001011101010011)_2$

The no. of 1's is 9.

38 votes

-- Keith Kr (4.5k points)

4.26.4 Number Representation: GATE CSE 1991 | Question: 01-v [top](#)

<https://gateoverflow.in/503>



✓

		a_3	a_2	a_1	a_0		
	\times	b_3	b_2	b_1	b_0		
		a_3b_0	a_2b_0	a_1b_0	a_0b_0		
		a_3b_1	a_2b_1	a_1b_1	a_0b_1	-	
		a_3b_2	a_2b_2	a_1b_2	a_0b_2	-	-
		a_3b_3	a_2b_3	a_1b_3	a_0b_3	-	-
c_7	c_6	c_5	c_4	c_3	c_2	c_1	c_0

$c_1 = b_1a_0 \oplus a_1b_0$

55 votes

-- Pooja Palod (24.1k points)



✓ XOR of C_{in} with C_{out} of the MSB position.

👍 17 votes

-- Amar Vashishth (25.2k points)



✓
A. $1 * 2^2 + 1 * 2^1 + 0 * 2^0 + 1 * 2^{-1} + 0 * 2^{-2} + 1 * 2^{-3} = 6.625$
B. $1118 \bmod 16 = 14$, quotient = 69

$69 \bmod 16 = 5$, quotient = 4
 $4 \bmod 16 = 4$.

Writing the mods in the reverse order (in hex) gives $(45E)_H$.

Both can be done using a calculator also.

👍 21 votes

-- Arjun Suresh (332k points)



✓ $-2^{n-1} \leq N \leq 2^{n-1} - 1$

Example : Let us have 3 bit binary numbers (unsigned)

$000 (0_{10})$ to $111 (7_{10})$ total of $8(2^3)$ numbers.

But when we have one sign bit then we have half the number of negatives -4 to -1 , 0 and 1 to 3 .

bit pattern: 100 101 110 111 000 001 010 011

1's comp: -3 -2 -1 0 0 1 2 3

2's comp.: -4 -3 -2 -1 0 1 2 3

👍 26 votes

-- Praveen Saini (41.9k points)



✓ $A = 16 + N$, (for $N = -1$, $A = 15$ which is the largest value, for $N = -8$, $A = 8$)

$B = \text{REM}$

$C = N/2$

👍 7 votes

-- Shaun Patel (6.1k points)



✓ I suggest the following approach, here we can clearly see that numbers are getting multiplied by powers of 16. So this is nothing but Hexadecimal number in disguise.

$(3 \times 4096 + 15 \times 256 + 5 \times 16 + 3) = (3F53)_{16} = (00111111010011)_2$ which has total $2 + 4 + 2 + 2 = 10$ 1's

Correct Answer: C.

👍 77 votes

-- Akash Kanase (36k points)



✓ Here, we are asked "magnitude" - so we just need to consider the mantissa bits.

Also, we are told "normalized representation"- so most significant bit of mantissa is always 1 (this is different from IEEE 754 normalized representation where this 1 is omitted in representation, but here it seems to be added on the right of decimal point as

seen from options).

So, the maximum value of mantissa will be 23 1's where a decimal point is assumed before first 1. So, this value will be $1 - 2^{-23}$

Due to the 1 in normalized representation, the smallest positive number will be 1 followed by 23 0's which will be $2^{-1} = 0.5$.

So ans d.

References



46 votes

-- Pooja Palod (24.1k points)

4.26.11 Number Representation: GATE CSE 1997 | Question: 5.4 top

<https://gateoverflow.in/2255>



✓ $\sqrt{(224)_r} = (13)_r$

Converting r base to decimal

$$\sqrt{2 \times r^2 + 2 \times r + 4} = 1 \times r + 3$$

Take square on both sides

$$2r^2 + 2r + 4 = r^2 + 6r + 9$$

$$\implies r^2 - 4r - 5 = 0$$

$$\implies r^2 - 5r + r - 5 = 0$$

$$\implies (r - 5)(r + 1) = 0$$

r being a base, it can not be -1 .

So, $C. r = 5$ is correct answer

26 votes

-- Praveen Saini (41.9k points)

4.26.12 Number Representation: GATE CSE 1998 | Question: 1.17 top

<https://gateoverflow.in/1654>



✓ $(342)_8 = (011100010)_2 = (11100010)_2$.

If we treat this as an 8 bit integer, the first bit becomes sign bit and since it is "1", number is negative. 8085 uses 2's complement representation for integers and hence the decimal equivalent will be $-(00011110)_2 = -30$.

Correct Answer: D

39 votes

-- Arjun Suresh (332k points)

4.26.13 Number Representation: GATE CSE 1998 | Question: 2.20 top

<https://gateoverflow.in/1693>



✓ I assume byte addressable memory- nothing smaller than a byte can be used.

We have four digits. So, to represent signed 4 digit numbers we need 5 bytes- 4 for four digits and 1 for the sign (like -7354). So, required memory = 5 bytes

Now, if we use integer, the largest number needed to represent is 9999 and this requires 2 bytes of memory for signed representation (one byte can represent only 256 unique integers).

So, memory savings while using integer is $\frac{(5-2)}{5} = \frac{3}{5} = 60\%$

Correct Answer: C

50 votes

-- Arjun Suresh (332k points)

4.26.14 Number Representation: GATE CSE 1999 | Question: 2.17 [top 5](#)

<https://gateoverflow.in/1495>



A and C.

Sign Magnitude

- $+0 = 0000$
- $-0 = 1000$

1's complement

- $+0 = 0000$
- $-0 = 1111$

26 votes

-- neelansh (151 points)

4.26.15 Number Representation: GATE CSE 2000 | Question: 1.6 [top 5](#)

<https://gateoverflow.in/629>



$2's$ complement representation is not same as $2's$ complement of a number. In $2's$ complement representation positive integers are represented in its normal binary form while negative numbers are represented in its $2's$ complement form. So, (c) is correct here.

http://www.ele.uri.edu/courses/ele447/proj_pages/divid/twos.html or [archive](#)

References



58 votes

-- Arjun Suresh (332k points)

4.26.16 Number Representation: GATE CSE 2000 | Question: 2.14 [top 5](#)

<https://gateoverflow.in/861>



Given 32 bits representation. So, the maximum precision can be 32 bits (In 32-bit IEEE representation, maximum precision is 24 bits but we take the best case here). This means approximately 10 digits.

$$A = 2.0 \times 10^{30}, C = 1.0$$

So, $A + C$ should make the 31st digit to 1, which is surely outside the precision level of A (it is 31st digit and not 31st bit). So, this addition will just return the value of A which will be assigned to Y .

So, $Y + B$ will return 0.0 while $X + C$ will return 1.0.

B choice.

Sample program if anyone wants to try:

```
#include<stdio.h>
int main()
{
    float a = 2.0e30;
    float b = -2.0e30;
    float c = 1.0;
    float y = a+c;
    printf("a = %0.25f y = %0.25f\n",a, y);
    y = y + b;
    float x = a + b;
    printf("x = %0.25f\n",x);
    x = x + c;
    printf("x = %0.25f\n",x);
}
```

32 votes

-- Arjun Suresh (332k points)

4.26.17 Number Representation: GATE CSE 2001 | Question: 2.10 [top 5](#)

<https://gateoverflow.in/728>



✓ $539 = 512 + 16 + 8 + 2 + 1 = 2^9 + 2^4 + 2^3 + 2^1 + 2^0$
 $= (1000011011)_2$

Now all answers have 12 bits, so we add two 0's at beginning $= (001000011011)_2$

To convert to 2's complement invert all bits till the rightmost 1, which will be $(110111100101)_2$

$= (110111100101)_2$

$= (DE5)_{16}$

Correct Answer: C

👍 40 votes

-- Arjun Suresh (332k points)

4.26.18 Number Representation: GATE CSE 2002 | Question: 1.14 [top ⤴](#)

<https://gateoverflow.in/818>



✓ **First Multiplication Iteration**

Multiply 0.25 by 2

$0.25 * 2 = 0.50$ (Product) Fractional part = 0.50 Carry = 0 (**MSB**)

Second Multiplication Iteration

Multiply 0.50 by 2

$0.50 * 2 = 1.00$ (Product) Fractional part = 1.00 Carry = 1 (**LSB**)

The fractional part in the 2nd iteration becomes zero and hence we stop the multiplication iteration.

Carry from the 1st multiplication iteration becomes **MSB** and carry from 2nd iteration becomes **LSB**.

So the result is 0.01

Correct Answer: B.

👍 23 votes

-- shekhar chauhan (32.8k points)

4.26.19 Number Representation: GATE CSE 2002 | Question: 1.15 [top ⤴](#)

<https://gateoverflow.in/819>



✓ D) is the correct ans. In 2's complement representation, positive numbers are represented in simple binary form and negative numbers are represented in its 2's complement form. So, for -15, we have to complement its binary value - 01111 and add a 1 to it, which gives 10001. Option D.

👍 29 votes

-- Ujjwal Saini (283 points)

4.26.20 Number Representation: GATE CSE 2002 | Question: 1.16 [top ⤴](#)

<https://gateoverflow.in/821>



✓ (D) is the answer. Sign extension (filling the upper bits using the sign bit) is needed while increasing the number of bits for representing a number. For positive numbers, 0 is extended and for negative numbers 1 is extended.

👍 28 votes

-- gatecse (63.3k points)

4.26.21 Number Representation: GATE CSE 2002 | Question: 1.21 [top ⤴](#)

<https://gateoverflow.in/826>



✓ (B) is the answer. When a positive value and negative value are added overflow never happens.

<http://sandbox.mc.edu/~bennet/cs110/tc/orules.html>

References



👍 40 votes

-- Arjun Suresh (332k points)



- ✓ Here, mantissa is represented in normalized representation and exponent in excess-64 (subtract 64 to get actual value).

a. We have to represent $-(7.5)_{10} = -(111.1)_2$.

Now we are using base 16 for exponent. So, mantissa will be .01111 and this makes exponent as 1 (4 bit positions and no hiding first 1 as in IEEE 754 as this is not mentioned in question) which in excess-64 will be $64 + 1 = 65$. Number being negative sign bit is 1. So, we get

$$(1 \underbrace{01111000 \dots 0}_{19 \text{ zeroes}} 1000001)_2 = (\text{BC}000041)_{16}$$

b. Largest value will be with largest possible mantissa, largest possible exponent and positive sign bit. So, this will be all 1's except sign bit which will be

$$0.\underbrace{111 \dots 1}_{24 \text{ ones}} \times 16^{127-64} = (1 - 2^{-24}) \times 16^{63} = (1 - 2^{-24}) \times 16^{63}$$

(Again we did not add implicit 1 as in IEEE 754)

$$2^x = 10^y \implies y = \log 2^x = x \log 2$$

$$\text{So, } (1 - 2^{-24}) \times 16^{63} = (1 - 10^{-24 \log 2}) \times 10^{63 \log 16} \approx (1 - 10^{-7}) \times 10^{76} = 10^{76}$$

Not directly relevant here, but a useful read: <https://jeapostrophe.github.io/courses/2015/fall/305/notes/dist/reading/help-floating-point.pdf>

References



34 votes

-- Arjun Suresh (332k points)



- ✓ MSB of 2's complement number has a weight of $-2^{(n-1)}$

(Trick: (from reversing sign extension) just skip all leading 1's from MSB except but 1, and then calculate the value as normal signed binary rep.)

so by calculating, we get the given number is -5 in decimal. and options are

- A. -25
- B. -28
- C. -41
- D. -37

Therefore it is clear that -25 is divisible by -5 . so we can say that (A) is correct 😊

28 votes

-- Nitin Sharma (2.2k points)



- ✓ Answer is D.

$$x \times 7 + 3 = 5 \times y + 4 \implies 7x = 5y + 1$$

Only option satisfying this is D.

25 votes

-- Aditi Dan (4k points)



- ✓ $(113. + -111.) = 1.13 \times 10^2 + -1.11 \times 10^2 = 0.02 \times 10^2 = 2.0 \times 10^0$

$$2.0 \times 10^0 + 7.51 \times 10^0 = 9.51 \times 10^0$$

$$(-111. + 7.51) = -1.11 \times 10^2 + 7.51 \times 10^0 = -1.11 \times 10^2 + 0.08 \times 10^2 = -1.03 \times 10^2$$

$$113. + -1.03 \times 10^2 = 1.13 \times 10^2 + -1.03 \times 10^2 = 0.1 \times 10^2 = 10.0$$

Reference: <https://www.doc.ic.ac.uk/~eedwards/compsys/float/>

Correct Answer: A

References



73 votes

-- Arjun Suresh (332k points)

4.26.26 Number Representation: GATE CSE 2004 | Question: 66 top

<https://gateoverflow.in/1060>



- ✓ $A = 1111 \quad 1010 = -6$
- $B = 0000 \quad 1010 = 10$
- $A \times B = -60 = 1100 \quad 0100$

Correct Answer: A

30 votes

-- Digvijay (44.9k points)

4.26.27 Number Representation: GATE CSE 2005 | Question: 16, ISRO2009-18, ISRO2015-2 top

<https://gateoverflow.in/1352>



- ✓ Total number of distinct numbers that can be represented using n bits = 2^n .

In case of unsigned numbers these corresponds to numbers from 0 to $2^n - 1$.

In case of signed numbers in 1's complement or sign magnitude representation, these corresponds to numbers from $-(2^{n-1} - 1)$ to $2^{n-1} - 1$ with 2 separate representations for 0.

In case of signed numbers in 2's complement representation, these corresponds to numbers from -2^{n-1} to $2^{n-1} - 1$ with a single representation for 0.

4 votes

-- Arjun Suresh (332k points)

4.26.28 Number Representation: GATE CSE 2005 | Question: 17 top

<https://gateoverflow.in/1353>



- ✓ $(657)_8 = (\underbrace{110}_6 \underbrace{101}_5 \underbrace{111}_7)_2 = (\underbrace{1}_1 \underbrace{1010}_A \underbrace{1111}_F)_2 = (1AF)_{16}$

Correct Answer: A.

17 votes

-- Arjun Suresh (332k points)

4.26.29 Number Representation: GATE CSE 2006 | Question: 39 top

<https://gateoverflow.in/1815>



- ✓ Number representation in 2's complement representation:

- Positive numbers as they are
- Negative numbers in 2's complement form.

So, the [overflow conditions](#) are

1. When we add two positive numbers (sign bit 0) and we get a sign bit 1
2. When we add two negative numbers (sign bit 1) and we get sign bit 0
3. [Overflow is relevant only for signed numbers](#) and carry is used for unsigned numbers
4. [When the carryout bit and the carryin to the most significant bit differs](#)

PS: When we add one positive and one negative number we won't get a carry. Also points 1 and 2 are leading to point 4.

Now the question is a bit tricky. It is **actually asking the condition of overflow of signed numbers when we use an adder which is meant to work for unsigned numbers.**

So, if we see the options, B is the correct one here as the first part takes care of case 2 (negative numbers) and the second part takes care of case 1 (positive numbers) - point 4. We can see counterexamples for other options:

A - Let $n = 4$ and we do $0111 + 0111 = 1110$. This overflows as in 2^n 's complement representation we can store only up to 7. But the overflow condition in A returns false as $c_{out} = 0$.

C - This works for the above example. But fails for $1001 + 0001 = 1010$ where there is no actual overflow ($-7 + 1 = -6$), but the given condition gives an overflow as $c_{out} = 0$ and $c_{n-1} = 1$.

D - This works for both the above examples, but fails for $1111 + 1111 = 1110$ ($-1 + -1 = -2$) where there is no actual overflow but the given condition says so.

Reference: http://www.mhhe.com/engcs/electrical/hamacher/5e/graphics/ch02_025-102.pdf

Thanks, @Dilpreet for the link and correction.

References



61 votes

-- Digvijay (44.9k points)

4.26.30 Number Representation: GATE CSE 2008 | Question: 6 top

<https://gateoverflow.in/404>



✓ $\sqrt{(121)_r} = 11_r$

$$\sqrt{(1 \times r^0) + (2 \times r^1) + (1 \times r^2)} = (1 \times r^0) + (1 \times r^1)$$

$$\sqrt{(1+r)^2} = 1+r$$

$$1+r = 1+r$$

So any integer r satisfies this but r must be greater than 2 as we have 2 in 121 and radix must be greater than any of the digits. **(D) is the most appropriate answer**

43 votes

-- Keith Kr (4.5k points)

4.26.31 Number Representation: GATE CSE 2009 | Question: 5, ISRO2017-57 top

<https://gateoverflow.in/1297>



✓ Answer: (b)

Here are two different ways of solving this problem.

Short Method

Given number is in base 8 thus each digit can be represented in three binary bits to get overall binary equivalent.

$$(1217)_8 = (001\ 010\ 001\ 111)_2$$

I have written the equivalent in group of three bits for easy understanding of the conversion. We can rearrange them in group of four to get equivalent hexadecimal number (in similar manner).

$$(001010001111)_2 = (0010\ 1000\ 1111)_2 = (28F)_{16}$$

Long Method

In a nut shell the long method follow the following conversion

$$OCT \rightarrow DEC \rightarrow HEX$$

This procedure is good in a sense that the given option also have a decimal equivalent, and thereby might save some time (no in this case, unfortunately).

Here is the the decimal equivalent

$$(1217)_8 = (1 * 8^3 + 2 * 8^2 + 1 * 8^1 + 7 * 8^0)_{10} = (655)_{10}$$

And we see that decimal equivalent is not in option therefore we proceed for hexadecimal conversion using [division method](#).

$$(655)_{10} = (28F)_{16}$$

Which we can find in given options.

HTH

References



24 votes

-- Prateek Dwivedi (3.5k points)

4.26.32 Number Representation: GATE CSE 2010 | Question: 8 [top](#)

<https://gateoverflow.in/2179>



- ✓ Multiplication can be directly carried in 2's complement form. $F87B = 1111\ 1000\ 0111\ 1011$ can be left shifted 3 times to give $8P = 1100\ 0011\ 1101\ 1000 = C3D8$.

Or, we can do as follows:

MSB in $(F87B)$ is 1. So, P is a negative number. So, $P = -1 * 2$'s complement of $(F87B) = -1 * (0785) = -1 * (0000\ 0111\ 1000\ 0101)$

$8 * P = -1 * (0011\ 1100\ 0010\ 1000)$ (P in binary left shifted 3 times)

In 2's complement representation, this equals, $1100\ 0011\ 1101\ 1000 = C3D8$

Correct Answer: A

68 votes

-- Arjun Suresh (332k points)

4.26.33 Number Representation: GATE CSE 2013 | Question: 4 [top](#)

<https://gateoverflow.in/1413>



- ✓ Range of 2's complement no $= > (-2^{n-1})$ to $+(2^{n-1} - 1)$

Here $n =$ No of bits $= 8$.

So minimum no $= -2^7 = (B) -128$

33 votes

-- Akash Kanase (36k points)

4.26.34 Number Representation: GATE CSE 2014 Set 1 | Question: 8 [top](#)

<https://gateoverflow.in/1766>



- ✓ Let 'x' be the base or radix of the number system.

The equation is: $\frac{3x^2 + 1x^1 + 2x^0}{2x^1 + 0x^0} = 1x^1 + 3x^0 + 1x^{-1}$

$$\Rightarrow \frac{3x^2 + x + 2}{2x} = x + 3 + 1/x$$

$$\Rightarrow \frac{3x^2 + x + 2}{2x} = \frac{x^2 + 3x + 1}{x}$$

$$\Rightarrow 3x^2 + x + 2 = 2x^2 + 6x + 2$$

$$\Rightarrow x^2 - 5x = 0$$

$$\Rightarrow x(x - 5) = 0$$

$$\Rightarrow x = 0 \text{ or } x = 5$$

As base or radix of a number system cannot be zero, **here $x = 5$** .

41 votes

-- vinodmits (363 points)



✓ Converting both sides to decimal,

$$25 + 10 + 3 = x * y + 8$$

$$\text{So, } xy = 30$$

Possible pairs are (1, 30), (2, 15), (3, 10) as the minimum base should be greater than 8.

👍 42 votes

-- Tejas Jaiswal (559 points)



✓

$$(43)_x = (y3)_8$$

Since a number in base k can only have digits from 0 to $(k - 1)$, we can conclude that: $x \geq 5$ and $y \leq 7$

Now, the original equation, when converted to decimal base gives:

$$4x^1 + 3x^0 = y(8^1) + 3(8^0)$$

$$4x + 3 = 8y + 3$$

$$x = 2y$$

So, we have the following constraints:

$$x \geq 5, y \leq 7, x = 2y, y \text{ are integers}$$

The set of values of (x, y) that satisfy these constraints are:

$$\underline{(x, y)}$$

$$(6, 3)$$

$$(8, 4)$$

$$(10, 5)$$

$$(12, 6)$$

$$(14, 7)$$

I am counting 5 pairs of values.

👍 52 votes

-- Praveen Saini (41.9k points)



✓ 1111 1111 1111 0101

2's complement of

$$1111 \ 1111 \ 1111 \ 0101 =$$

$$0000 \ 0000 \ 0000 \ 1011 =$$

$$+11$$

2's complement of

$$-11 =$$

$$+11, \text{ in } 2's \text{ complement representation}$$

2's complement of

$$+11 =$$

$$-11, \text{ in } 2's \text{ complement representation}$$

So

$$-11 \text{ it should be}$$

34 votes

-- Praveen Saini (41.9k points)

4.26.38 Number Representation: GATE CSE 2016 Set 2 | Question: 09 top

https://gateoverflow.in/39546



✓ **2's Complement Representation**

The range of n -bit 2's Complement Numbers is $-(2^{n-1})$ to $+(2^{n-1} - 1)$

For example, if $n = 2$, then $-2, -1, 0, 1$ belong to the range (which are distinct)

In general 2^n distinct integers are possible with n -bit 2's Complement Number $\rightarrow X$

Sign Magnitude Representation

The range of n -bit Sign Magnitude numbers is $-(2^{n-1} - 1)$ to $+(2^{n-1} - 1)$

For example, if $n = 2$, then $-1, -0, +0, +1$ belong to the range in which $-0 = +0$ and both represent zero.

In general $2^n - 1$ distinct integers are possible with n -bit Sign magnitude representation $\rightarrow Y$

$X - Y = 2^n - (2^n - 1) = 1.$

37 votes

-- Uzumaki Naruto (1.6k points)

4.26.39 Number Representation: GATE CSE 2017 Set 1 | Question: 9 top

https://gateoverflow.in/118289



✓ **Answer is (C)**

Overflow is said to occur in the following cases

C7	C6	Overflow
0	0	NO
0	1	YES
1	0	YES
1	1	NO

The 3rd condition occurs in the following case A7B7S7, now the question arises how?

C7	C6
A7	1
B7	1
S7	0

NOW, A7 = 1 AND B7 = 1 S7 = 0 is only possible when C6 = 0 otherwise S7 would become 1.

C7 has to be 1 (1 + 1 + 0 generates carry)

ON similar basis we can prove that C7 = 0 and C6 = 1 is produced by A7' B7' S7. Hence, either of the two conditions cause overflow. Hence(C).

Why not A? when C7 = 1 and C6 = 1 this doesn't indicate overflow (4th row in the table)

Why not B? if all carry bits are 1 then, C7 = 1 and C6 = 1 (This also generates 4th row)

Why not D? These combinations are C0 and C1, the lower carries do not indicate overflow

36 votes

-- (points)

4.26.40 Number Representation: GATE CSE 2017 Set 2 | Question: 1 top

https://gateoverflow.in/118337



✓ **Given: (BCA9)₁₆**

1011 1100 1010 1001

For octal number system: grouping of three- three bits from right to left

1 011 110 010 101 001

1 3 6 2 5 1

Answer: option D) (1 3 6 2 5 1)₈

👍 22 votes

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-- Smriti012 (2.8k points)

4.26.41 Number Representation: GATE CSE 2019 | Question: 22 top

<https://gateoverflow.in/302826>



✓ These are two groups:

1. MSB with 1
2. MSB with 0

$$n_{MSB0} = 7, n_{MSB1} = 6, n_{total} = 13$$

Choose randomly and INDEPENDENTLY two elements out of 13 elements such that MSB is same.

$$P = \frac{n_{MSB1} * n_{MSB1} + n_{MSB0} * n_{MSB0}}{n_{total} * n_{total}}$$

$$P = \frac{7*7 + 6*6}{13*13} = \frac{85}{169} = 0.5029$$

👍 39 votes

-- Digvijay (44.9k points)

4.26.42 Number Representation: GATE CSE 2019 | Question: 4 top

<https://gateoverflow.in/302844>



✓ $(+28)_{10} = (0000\ 0000\ 00011100)_2$
-28 is nothing but 2s complement of +28.

So, 2s complement of $(0000\ 0000\ 0001\ 1100)_2$ is $(1111\ 1111\ 1110\ 0100)_2$

$(-28)_{10} = (1111\ 1111\ 1110\ 0100)_2$. **Answer is (C).**

👍 28 votes

-- Digvijay (44.9k points)

4.26.43 Number Representation: GATE CSE 2019 | Question: 8 top

<https://gateoverflow.in/302840>



✓ Let X and Y represents 31 and -31 respectively in binary sign magnitude form. X and Y will take 6 bits as range of sign magnitude form is $-(2^{(n-1)} - 1)$ to $2^{(n-1)} - 1$; where n is the number of bits.

Now in question $Z = X - Y$,

$$Z = 31 - (-31) = 62$$

To represent 62 in sign magnitude form we need 7 (6 + 1) bits.

Hence, $n + 1$ bits needed.

Answer is C.

👍 36 votes

-- DIVYANSHU SAXENA (421 points)

4.26.44 Number Representation: GATE CSE 2021 Set 1 | Question: 6 top

<https://gateoverflow.in/357446>



✓ Firstly convert base 3 into a decimal number system(Base 10):

$$(21)_3 = (x)_{10} \implies 0 * 3^0 + 1 * 3^1 + 2 * 3^2 = (21)_{10}$$

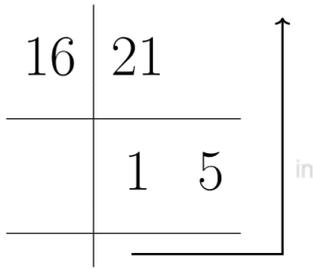
Now convert $(21)_{10}$ into a hexadecimal system. dividing by 16 that is:

$$(21)_{10} = (z)_{16}$$

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$\therefore z = (15)_{16}$

Option A is correct.

👍 1 votes

-- Hira (14.1k points)

4.26.45 Number Representation: GATE CSE 2021 Set 2 | Question: 18 top ⬆

<https://gateoverflow.in/357522>



✓ **Answer: 3**

This conversion is just

$$\frac{1}{2} + \frac{1}{4} + \frac{1}{16} = \frac{8+4+1}{16} = \frac{13}{16} = 0.8125$$

On comparison we get $x = 1$ and $y = 2$. Hence, $x + y = 3$.

👍 3 votes

-- witness_07 (145 points)

Answer = 3

- A. $(0.1)_2 = (0.5)_{10}$
- B. $(0.01)_2 = (0.25)_{10}$
- C. $(0.001)_2 = (0.125)_{10}$
- D. $(0.0001)_2 = (0.0625)_{10}$

$A + B + D \implies (0.1101)_2 = 0.8125$

👍 7 votes

-- JATIN MITTAL (2.1k points)

4.26.46 Number Representation: GATE IT 2004 | Question: 42 top ⬆

<https://gateoverflow.in/3685>



✓ Only (ii) is the answer.

In 2's complement arithmetic, overflow happens only when

1. Sign bit of two input numbers is 0, and the result has sign bit 1
2. Sign bit of two input numbers is 1, and the result has sign bit 0.

Overflow is important only for signed arithmetic while carry is important only for unsigned arithmetic.

A carry happens when there is a carry to (or borrow from) the most significant bit. Here, (i) and (iii) cause a carry but only (ii) causes overflow.

http://teaching.idallen.com/dat2343/10f/notes/040_overflow.txt

References



👍 39 votes

-- Arjun Suresh (332k points)



$$\checkmark \quad (123456)_8 = (001\ 010\ 011\ 100\ 101\ 110)_2 = (\underbrace{00}_{A}\ \underbrace{1010}_7\ \underbrace{0111}_2\ \underbrace{0010}_{E}\ \underbrace{1110}_E)_2 = (A72E)_{16}$$

$$= (00\ 10\ 10\ 01\ 11\ 00\ 10\ 11\ 10)_2 = (22130232)_4$$

So, option (A).

👍 28 votes

-- Arjun Suresh (332k points)



✓ Simply convert $(34.4)_8$ and $(23.4)_8$ to decimal.

$(34.4)_8 = 28.5$ in decimal and $(23.4)_8 = 19.5$ in decimal.

$$28.5 \times 19.5 = 555.75$$

Now convert 555.75 back to octal which is $(1053.6)_8$

$$\begin{aligned} \overleftarrow{(34.4)}_8 \text{ to decimal} \\ &= 3 \times 8^1 + 4 \times 8^0 + 4 \times 8^{-1} \\ &= 24 + 4 + 0.5 \\ &= (28.5)_{10} \end{aligned}$$

$$\begin{aligned} \overleftarrow{(23.4)}_8 \text{ to decimal} \\ &= 2 \times 8^1 + 3 \times 8^0 + 4 \times 8^{-1} \\ &= 16 + 3 + 0.5 \\ &= (19.5)_{10} \end{aligned}$$

$$(28.5)_{10} \times (19.5)_{10} = (555.75)_{10}$$

Now,

$$(555.75)_{10} = (?)_8$$

To convert the integer part

8	555
8	69 3
8	8 5
8	1 0
8	0 1 ↑

We get 1053.

To convert the decimal, keep multiplying by 8 till decimal part becomes 0.

$$0.75 \times 8 \rightarrow \underbrace{6}_{\text{keep the integral part}} . \underbrace{00}_{\text{0 decimal part}}$$

$$\therefore (555.75)_{10} = (1053.6)_8$$

Correct Answer: A

👍 44 votes

-- Afaque Ahmad (727 points)

✓ Answer: **C**.

The addition results in 0001 and no overflow with 1 as carry bit.

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In 2's complement addition Overflow happens only when:

- Sign bit of two input numbers is 0, and the result has sign bit 1.
- Sign bit of two input numbers is 1, and the result has sign bit 0.

👍 51 votes

-- Rajarshi Sarkar (27.9k points)

✓ $(C012.25)_H - (10111001110.101)_B$

$$= 1100\ 0000\ 0001\ 0010.\ 0010\ 0101$$

$$- 0000\ 0101\ 1100\ 1110.\ 1010\ 0000$$

$$= 1011\ 1010\ 0100\ 0011.\ 1000\ 0101$$

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$$= 1\ 011\ 101\ 001\ 000\ 011.\ 100\ 001\ 010$$

$$= (135103.412)_o$$

Binary subtraction is like decimal subtraction: $0 - 0 = 0, 1 - 1 = 0, 1 - 0 = 1, 0 - 1 = 1$ with 1 borrow.Correct Answer: **A**

👍 41 votes

-- Arjun Suresh (332k points)

✓ Answer: **B**

01001101

+11101001

100110110

Carry = 1

Overflow = 0 (In 2's complement addition Overflow happens only when: Sign bit of two input numbers is 0, and the result has sign bit 1 OR Sign bit of two input numbers is 1, and the result has sign bit 0.)

Sign bit = 0.

👍 39 votes

-- Rajarshi Sarkar (27.9k points)



State whether the following statements are TRUE or FALSE with reason:

RAM is a combinational circuit and PLA is a sequential circuit.

gate1990 true-false digital-logic ram pla

anlclassse in

taste naterse in

Answer

Answers: Pla



Both the statements are false.

1. RAM is not a combinational circuit. For **RAM**, the input is the memory location selector and the operation (read or write) and another byte (which can be input for write operation, or output for read operation), and the output is either a success indicator (for write operation) or the byte at the selected location (for read operation). It does depend on past inputs, or rather, on the past write operations at the selected byte. This is a **Sequential logic circuit**.
2. PLA is a combinational circuit as ROM & PAL. PLA is a programmable logic device with a programmable AND array and a programmable OR array. A PLA with n inputs has fewer than $2n$ AND gates (otherwise there would be no advantage over a ROM implementation of the same size). A PLA only needs to have enough AND gates to decode as many unique terms as there are in the functions it will implement.

👍 11 votes

-- vamsi2376 (2.8k points)

4.28

Prime Implicants (2) [top](#)4.28.1 Prime Implicants: GATE CSE 1997 | Question: 5.1 [top](#)

<https://gateoverflow.in/2252>



Let $f(x, y, z) = x + \bar{y}x + xz$ be a switching function. Which one of the following is valid?

- $\bar{y}x$ is a prime implicant of f
- xz is a minterm of f
- xz is an implicant of f
- y is a prime implicant of f

gate1997 digital-logic normal prime-implicants

goclasses.in

tests.gatecse.in

Answer [👍](#)

4.28.2 Prime Implicants: GATE CSE 2004 | Question: 59 [top](#)

<https://gateoverflow.in/1054>



Which are the essential prime implicants of the following Boolean function?

$$f(a, b, c) = a'c + ac' + b'c$$

- $a'c$ and ac'
- $a'c$ and $b'c$
- $a'c$ only.
- ac' and bc'

gate2004-cse digital-logic normal prime-implicants

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Answer [👍](#)

Answers: Prime Implicants

4.28.1 Prime Implicants: GATE CSE 1997 | Question: 5.1 [top](#)

<https://gateoverflow.in/2252>



✓ In sum of terms, any term is an implicant because it implies the function. So, xz is an implicant and hence **C** is the answer. Still, lets see the other options.

If no minimization is possible for an implicant (by removing any variable) it becomes a prime implicant.

If a prime implicant is present in any possible expression for a function, it is called an essential prime implicant. (For example in K-map we might be able to choose among several prime implicants but for essential prime implicants there won't be a choice).

xy	00	01	11	10
z				
0	1	1		1
1	1	1	1	1

So, $f = x' + y'x + xz$

$= y' + x' + z$ (could be also derived using algebraic rules as in <http://www.ee.surrey.ac.uk/Projects/Labview/boolalgebra/>)

So, the prime implicants are x' , y' and z . Being single variable ones and with no common variables, all must be essential also.

Now, a choice is false, as y' is a prime implicant and hence, $y'x$ is just an implicant but not prime.

b choice - xz is not a minterm. A minterm must include all variables. So, xyz is a minterm so, is $xy'z$, but not xz .

d choice - y' is a prime implicant not y .

References



33 votes

-- Arjun Suresh (332k points)

4.28.2 Prime Implicants: GATE CSE 2004 | Question: 59

<https://gateoverflow.in/1054>



✓ $f(a, b, c) = a'c + ac' + b'c$

We can write these product of sum terms into canonical product of sum form.

$f(a, b, c) = \underbrace{a'b'c}_{001} + \underbrace{a'bc}_{011} + \underbrace{ab'c'}_{100} + \underbrace{abc'}_{110} + \underbrace{ab'c}_{101} + \underbrace{a'b'c}_{001}$

$f(a, b, c) = \sum(1, 3, 4, 5, 6)$

Now, we can draw the k-map for these minterms.

bc	00	01	11	10
a				
0	0	1	1	0
1	1	1	0	1

- Prime implicant of f is an implicant that is minimal - that is, the removal of any literal from product term results in a non-implicant for f .
- Essential prime implicant is an prime implicant that cover an output of the function that no combination of other prime implicants is able to cover.

Prime implicants are: $a'c, b'c, ab', ac'$

Essential prime implicants are: $a'c, ac'$ (green color).

References:

- http://dispert.international-university.eu/Digital_Design_Website_English/digital_2/dig002_5.html
- <http://web.cecs.pdx.edu/~mcnames/ECE171/Lectures/Lecture10.html>

References



14 votes

-- Lakshman Patel (65.7k points)

4.29

Rom (4) top

4.29.1 Rom: GATE CSE 1993 | Question: 6.6 top

<https://gateoverflow.in/2285>



A ROM is used to store the Truth table for binary multiple units that will multiply two 4-bit numbers. The size of the ROM (number of words \times number of bits) that is required to accommodate the Truth table is M words \times N bits. Write the values of M and N .

gate1993 digital-logic normal rom descriptive

Answer

4.29.2 Rom: GATE CSE 1996 | Question: 1.21 top

<https://gateoverflow.in/2725>



A ROM is used to store the table for multiplication of two 8-bit unsigned integers. The size of ROM required is

- A. 256×16
- B. $64K \times 8$
- C. $4K \times 16$
- D. $64K \times 16$

gate1996 digital-logic normal rom

Answer

4.29.3 Rom: GATE CSE 2012 | Question: 19 top

<https://gateoverflow.in/51>



The amount of ROM needed to implement a 4-bit multiplier is

- A. 64 bits
- B. 128 bits
- C. 1 Kbits
- D. 2 Kbits

gate2012-cse digital-logic normal rom

Answer

4.29.4 Rom: GATE IT 2004 | Question: 10 top

<https://gateoverflow.in/3651>



What is the minimum size of ROM required to store the complete truth table of an 8-bit \times 8-bit multiplier?

- A. $32K \times 16$ bits
- B. $64K \times 16$ bits
- C. $16K \times 32$ bits
- D. $64K \times 32$ bits

gate2004-it digital-logic normal rom

Answer

Answers: Rom

4.29.1 Rom: GATE CSE 1993 | Question: 6.6 top

<https://gateoverflow.in/2285>



✓ A is 4 bit binary no $A4A3A2A1$

B is 4 bit binary no $B4B3B2B1$

M is result of multiplication $M8M7M6M5M4M3M2M1$ [check biggest no $1111 \times 1111 = 11100001$]

A4	A3	A2	A1	B4	B3	B2	B1	M8	M7	M6	M5	M4	M3	M2	M1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
.
.
1	1	1	1	1	1	1	0	1	1	0	1	0	0	1	0
1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1

4 bits of A and 4 bits of B mean input will consist of 8 bits and need address 00000000 to $11111111 = 2^8$ address

The output will be of 8 bits

So memory will be of $2^8 \times 8$

$M = 256, N = 8$

👍 22 votes

-- Praveen Saini (41.9k points)

4.29.2 Rom: GATE CSE 1996 | Question: 1.21 [top](#)

<https://gateoverflow.in/2725>



- ✓ When we multiply two 8 bit numbers result can go up to 16 bits. So, we need 16 bits for each of the multiplication result. Number of results possible = $2^8 \times 2^8 = 2^{16} = 64 K$ as we need to store all possible results of multiplying two 8 bit numbers. So, $64 K \times 16$ is the answer.

Correct Answer: D

👍 74 votes

-- Arjun Suresh (332k points)

4.29.3 Rom: GATE CSE 2012 | Question: 19 [top](#)

<https://gateoverflow.in/51>



- ✓ A ROM cannot be written. So, to implement a 4-bit multiplier we must store all the possible combinations of $2^4 \times 2^4$ inputs and their corresponding 8 output bits giving a total of $2^4 \times 2^4 \times 8$ bits = 2048 bits. So, **(D)** is the answer.

PS: We are not storing the input bits explicitly -- those are considered in order while accessing the output 8 bits. In this way, by storing all the possible outputs in order we can avoid storing the input combinations.

👍 55 votes

-- Arjun Suresh (332k points)

4.29.4 Rom: GATE IT 2004 | Question: 10 [top](#)

<https://gateoverflow.in/3651>



- ✓ Answer - B.

Multiplying 2 8 bit digits will give result in maximum 16 bits

Total number of multiplications possible = $2^8 \times 2^8$

Hence, space required = $64K \times 16$ bits

👍 25 votes

-- Ankit Rokde (6.9k points)

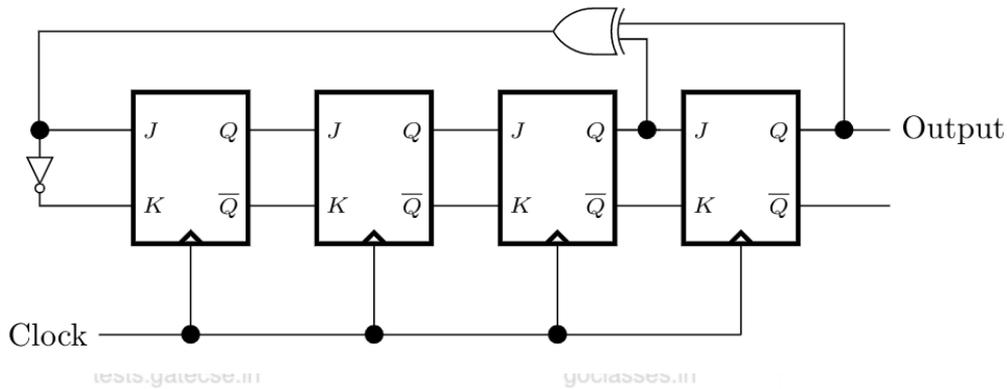
4.30

Sequential Circuit (6) [top](#)

4.30.1 Sequential Circuit: GATE CSE 1987 | Question: 1-III [top](#)

<https://gateoverflow.in/80034>





The above circuit produces the output sequence:

- A. 1111 1111 0000 0000
- B. 1111 0000 1111 0000
- C. 1111 0001 0011 0101
- D. 1010 1010 1010 1010

gate1987 digital-logic sequential-circuit flip-flop digital-counter

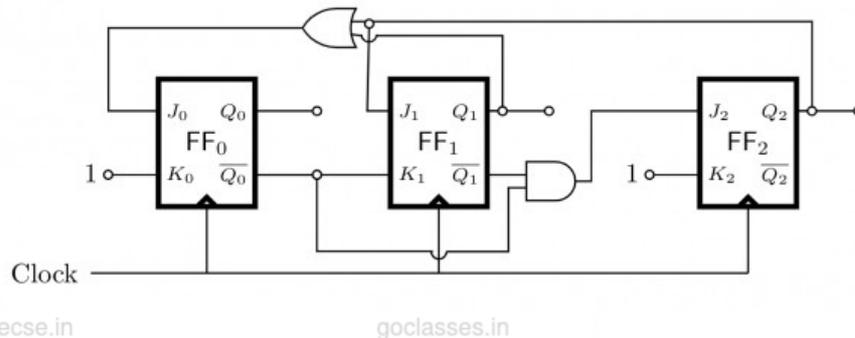
Answer

4.30.2 Sequential Circuit: GATE CSE 1990 | Question: 5-c

<https://gateoverflow.in/85400>



For the synchronous counter shown in Fig.3, write the truth table of $Q_0, Q_1,$ and Q_2 after each pulse, starting from $Q_0 = Q_1 = Q_2 = 0$ and determine the counting sequence and also the modulus of the counter.



gate1990 descriptive digital-logic sequential-circuit flip-flop digital-counter

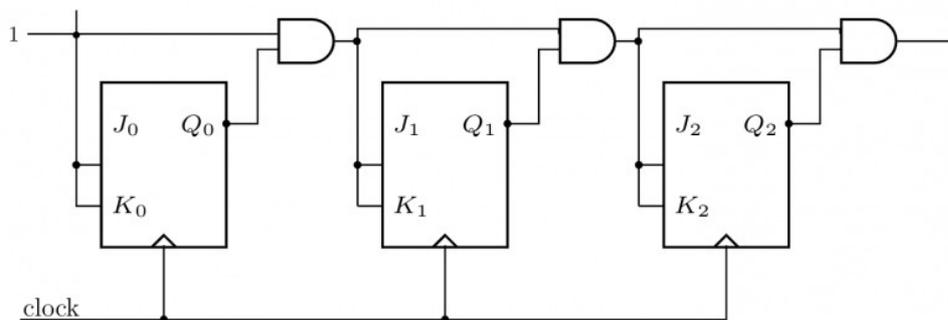
Answer

4.30.3 Sequential Circuit: GATE CSE 1991 | Question: 5-c

<https://gateoverflow.in/26442>



Find the maximum clock frequency at which the counter in the figure below can be operated. Assume that the propagation delay through each flip flop and each AND gate is 10 ns. Also, assume that the setup time for the JK inputs of the flip flops is negligible.



Answer

4.30.4 Sequential Circuit: GATE CSE 1994 | Question: 2-1

https://gateoverflow.in/2468



The number of flip-flops required to construct a binary modulo N counter is _____

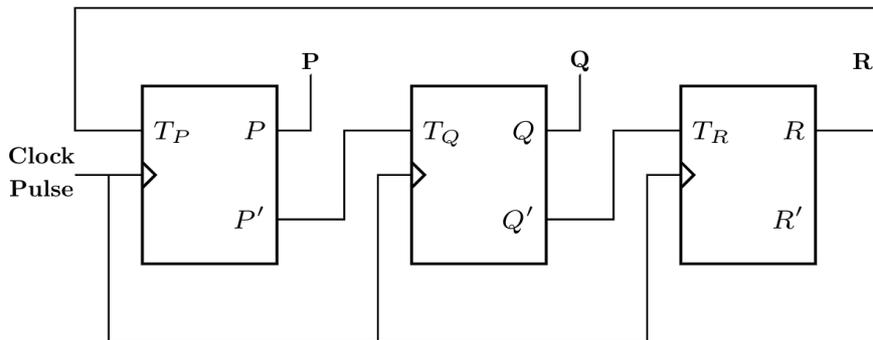
Answer

4.30.5 Sequential Circuit: GATE CSE 2021 Set 1 | Question: 28

https://gateoverflow.in/357423



Consider a 3-bit counter, designed using T flip-flops, as shown below:



Assuming the initial state of the counter given by PQR as 000, what are the next three states?

- A. 011, 101, 000
- B. 001, 010, 111
- C. 011, 101, 111
- D. 001, 010, 000

Answer

4.30.6 Sequential Circuit: GATE1992-04-c

https://gateoverflow.in/17408



Design a 3-bit counter using D-flip flops such that not more than one flip-flop changes state between any two consecutive states.

Answer

Answers: Sequential Circuit

4.30.1 Sequential Circuit: GATE CSE 1987 | Question: 1-III

https://gateoverflow.in/80034



Let us suppose the initial output of all the JK flip flops is 1

So we can draw the below table to get the output Q_3

Index	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
					Q_2	\bar{Q}_2	Q_1	\bar{Q}_1	Q_0	\bar{Q}_0	$Q_3 \oplus Q_2$	J'_0
0	1	1	1	1	1	0	1	0	1	0	0	1
1	1	1	1	0	1	0	1	0	0	1	0	1
2	1	1	0	0	1	0	0	1	0	1	0	1
3	1	0	0	0	0	1	0	1	0	1	1	0
4	0	0	0	1	0	1	0	1	1	0	0	1
5	0	0	1	0	0	1	1	0	0	1	0	1
6	0	1	0	0	1	0	0	1	0	1	1	0
7	1	0	0	1	0	1	0	1	1	0	1	0
8	0	0	1	1	0	1	1	0	1	0	0	1
9	0	1	1	0	1	0	1	0	0	1	1	0
10	1	1	0	1	1	0	0	1	1	0	0	1
11	1	0	1	0	0	1	1	0	0	1	1	0
12	0	1	0	1	1	0	0	1	1	0	1	0
13	1	0	1	1	0	1	1	0	1	0	1	0
14	0	1	1	1	1	0	1	0	1	0	1	0
	1	1	1	1								

From the above table Q_3 that is output is 1111 0001 0011 0101

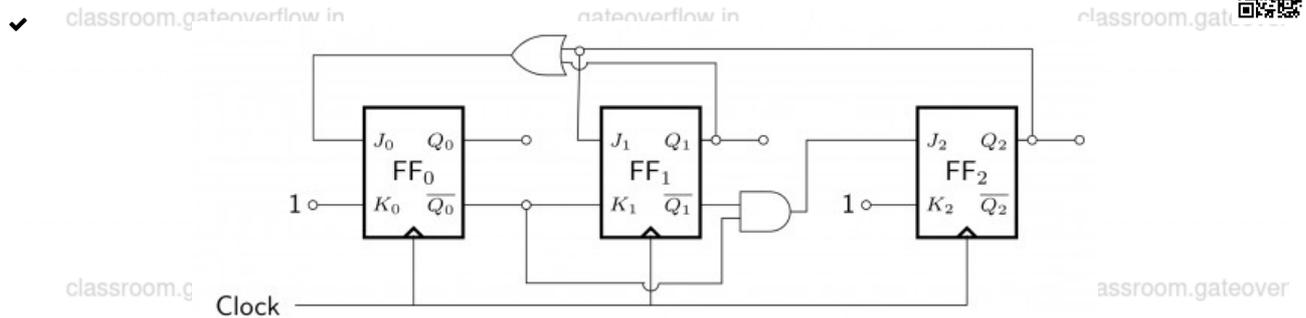
So the answer should be C.

3 votes

-- Digvijaysingh Gautam (6.3k points)

4.30.2 Sequential Circuit: GATE CSE 1990 | Question: 5-c

<https://gateoverflow.in/85400>

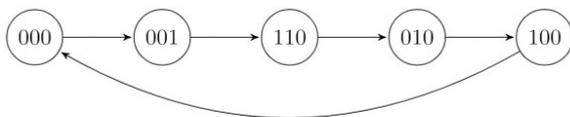


Q_0	Q_1	Q_2	Q_{0N}	Q_{1N}	Q_{2N}
0	0	0	0	0	1
0	0	1	1	1	0
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	0	1	0
1	1	0	0	1	0
1	1	1	0	1	0

$$Q_{0N} = Q_0 \implies J_0 = Q_1 + Q_2, K_0 = 1$$

$$Q_{1N} = Q_1 \implies J_1 = Q_2, K_1 = \bar{Q}_0$$

$$Q_{2N} = Q_2 \implies J_2 = Q_1, K_2 = 1$$



0-1-6-2-4-0

So, MOD 5 counter.

25 votes

-- Akash Dinkar (27.9k points)

4.30.3 Sequential Circuit: GATE CSE 1991 | Question: 5-c top 5

<https://gateoverflow.in/26442>



✓ In a JK flip flop the output toggles when both J and K inputs are 1. So, we must ensure that with each clock the output from the previous stage reaches the current stage.

Setup time is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly

It is given that setup time is negligible - means as soon as data is stable, the next clock can be given.

- Time to get output from FF once input (and clock) is given = $10ns$. (Propagation Delay)
- Time for inputs to reach $FF_1 = 0$. (Zero AND gate)
- Time for inputs to reach $FF_2 = 10$. (One AND gate)
- Time for inputs to reach $FF_3 = 20$. (Two AND gates)

So, minimum time period needed for clock is $10 + \max(0, 10, 20) = 10 + 20 = 30ns$ which would mean a maximum clock frequency of $1/30GHz = 33.33MHz$

88 votes

-- Arjun Suresh (332k points)

4.30.4 Sequential Circuit: GATE CSE 1994 | Question: 2-1 top 5

<https://gateoverflow.in/2468>



✓ Let say we have to design a mod-8 counter i.e 000 to 111. So we need 3 bits to represent i.e 3 FF.

For mod $N : 2^x = N$

$$\implies x = \lceil \log_2 N \rceil$$

27 votes

-- Praveen Saini (41.9k points)

4.30.5 Sequential Circuit: GATE CSE 2021 Set 1 | Question: 28 top 5

<https://gateoverflow.in/35743>



✓ From the given 3 state counter made from T flipflops, the next input sequence are as follows:

- $T_P = R$
- $T_Q = \overline{P}$
- $T_R = \overline{Q}$

Initial State			Current input			Next State		
P	Q	R	T_P	T_Q	T_R	P^+	Q^+	R^+
0	0	0	0	1	1	0	1	1
0	1	1	1	1	0	1	0	1
1	0	1	1	0	1	0	0	0

In T flip flop for low input(0), the next state is Q_n (current state) and for high input(1), it toggles/complements the present state ($\overline{Q_n}$)

011, 101, 000

Option A is correct.

4 votes

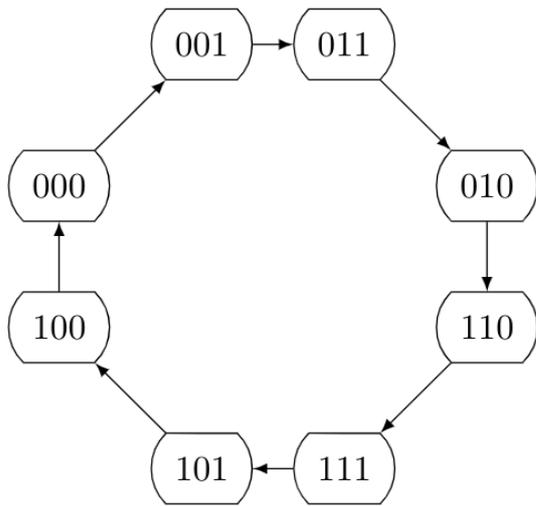
-- Hira (14.1k points)

4.30.6 Sequential Circuit: GATE1992-04-c top 5

<https://gateoverflow.in/17408>



✓ State diagram will be as (remember concept of GRAY code)



State table and 3-bit synchronous counter with D FFs, will be as

Present State	Next State	FF Inputs
ABC	$\bar{A}\bar{B}\bar{C}$	$D_A D_B D_C$
001	011	011
000	001	001
010	110	110
011	010	010
100	000	000
101	100	100
110	111	111

$A \backslash BC$	00	01	11	10
0	0	0	0	1
1	0	1	1	1

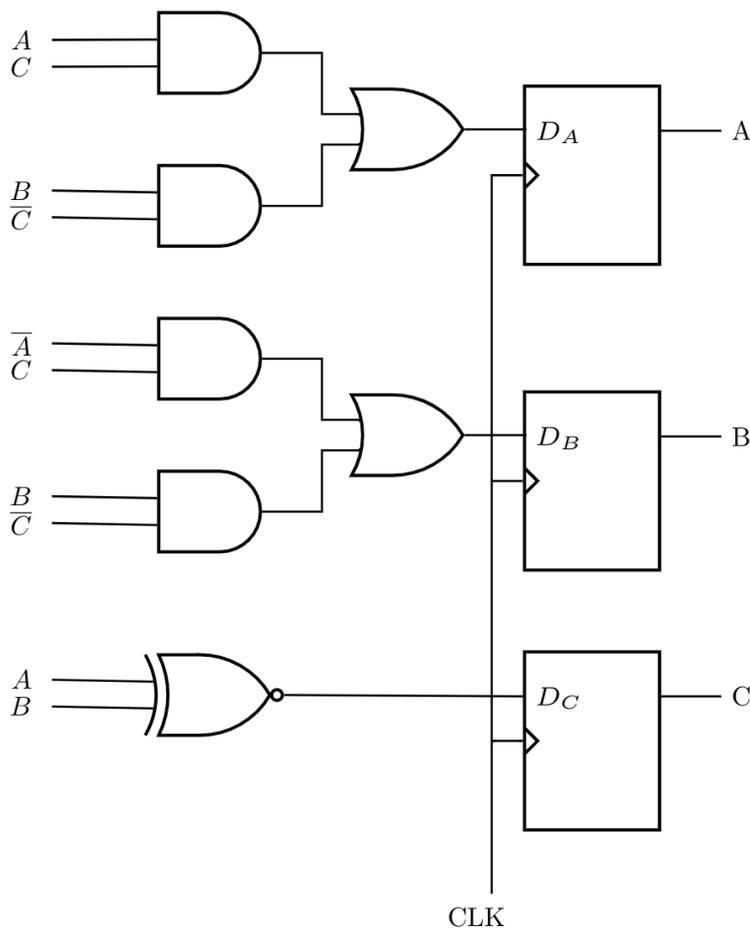
$$D_A = AC + B\bar{C}$$

$A \backslash BC$	00	01	11	10
0	0	1	1	1
1	0	0	0	1

$$D_B = \bar{A}C + B\bar{C}$$

$A \backslash BC$	00	01	11	10
0	1	1	0	0
1	0	0	1	1

$$D_C = \bar{A}\bar{B} + AB = A \odot B$$



29 votes

-- Praveen Saini (41.9k points)

4.31

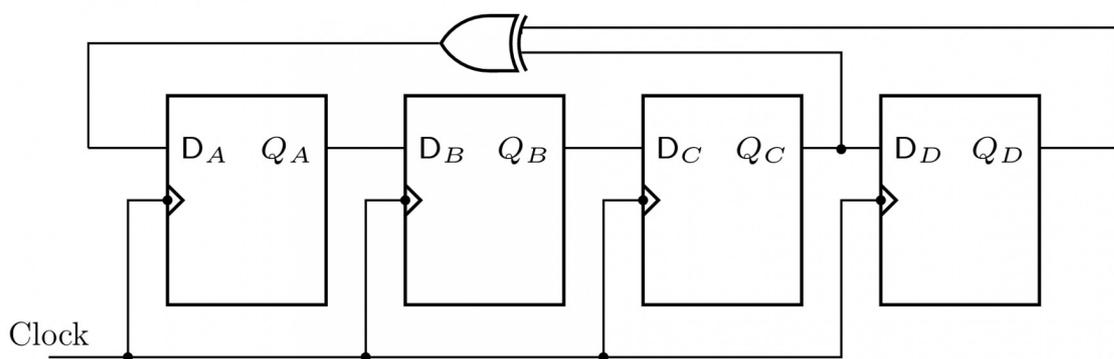
Shift Registers (2) top

4.31.1 Shift Registers: GATE CSE 1987 | Question: 13-a top

<https://gateoverflow.in/82607>



The below figure shows four D-type flip-flops connected as a shift register using a XOR gate. The initial state and three subsequent states for three clock pulses are also given.



State	Q_A	Q_B	Q_C	Q_D
Initial	1	1	1	1
After the first clock	0	1	1	1
After the second clock	0	0	1	1
After the third clock	0	0	0	1

The state $Q_A Q_B Q_C Q_D$ after the fourth clock pulse is

A. 0000

- B. 1111
- C. 1001
- D. 1000

Answer

4.31.2 Shift Registers: GATE CSE 1991 | Question: 06,a top

<https://gateoverflow.in/532>



Using D flip-flop gates, design a parallel-in/serial-out shift register that shifts data from left to right with the following input lines:

- i. Clock CLK
- ii. Three parallel data inputs A, B, C
- iii. Serial input S
- iv. Control input load/ $\overline{\text{SHIFT}}$.

Answer

Answers: Shift Registers

4.31.1 Shift Registers: GATE CSE 1987 | Question: 13-a top

<https://gateoverflow.in/82607>



Option (D) **1000**

$$Q_{An} = Q_C \oplus Q_D, Q_{Bn} = Q_A, Q_{Cn} = Q_B \text{ and } Q_{Dn} = Q_C$$

Q_A	Q_B	Q_C	Q_D
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	0

13 votes

-- Prajwal Bhat (7.6k points)

4.31.2 Shift Registers: GATE CSE 1991 | Question: 06,a top

<https://gateoverflow.in/532>



Refer the Logic diagram for the parallel-in/serial-out SHIFT REGISTER, using D flip-flop gates that shifts data from left to right in this video : <https://youtu.be/7LmBcGiiYwk>

0 votes

-- Pradip13 (17 points)

4.32

Static Hazard (1) top

4.32.1 Static Hazard: GATE CSE 2006 | Question: 38 top

<https://gateoverflow.in/1814>



Consider a Boolean function $f(w, x, y, z)$. Suppose that exactly one of its inputs is allowed to change at a time. If the function happens to be true for two input vectors $i_1 = \langle w_1, x_1, y_1, z_1 \rangle$ and $i_2 = \langle w_2, x_2, y_2, z_2 \rangle$, we would like the function to remain true as the input changes from i_1 to i_2 (i_1 and i_2 differ in exactly one bit position) without becoming false momentarily. Let $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$. Which of the following cube covers of f will ensure that the required property is satisfied?

- A. $\overline{w}xz, wxy, x\overline{y}z, xyz, wyz$
- B. $wxy, \overline{w}xz, wyz$
- C. $wx\overline{y}z, xz, w\overline{x}yz$
- D. $wxy, wyz, wxz, \overline{w}xz, x\overline{y}z, xyz$

Answer

Answers: Static Hazard

4.32.1 Static Hazard: GATE CSE 2006 | Question: 38 top

<https://gateoverflow.in/1814>



✓ The question is indirectly asking for static-1 hazard in the circuit - that is output becoming 0 momentarily when it is supposed to be 1.

Static 1 Hazard: Output going to 0 when it should remain 1

- Happens in a 2 level SOP implementation.
- Suppose only one AND gate (minterm) is 1 in an SOP implementation.
- A variable in that minterm changes causing the output of that AND gate to become 0 and another AND gate to be 1.
- Depending on the propagation delay of the gates, the output can momentarily become 0 before finalizing on 1. For example, consider $f = a'b' + ac$ and initially $a = 0, b = 0, c = 1$, so that output is 1. Now, if a changes to 1, again output should be 1 due to ac term. But if $a'b'$ turns to 0 before ac turns to 1, output can be momentarily 0 causing a static-1 hazard.
- Can be detected in a K-map if there are any adjacent 1's not covered by an implicant. i.e., to avoid static hazard, all adjacent 1's in a K-map must be covered by some implicant. In the below K-map, the implicant shown in green ensures no static-1 hazard.

		<i>bc</i>			
		00	01	11	10
<i>a</i>	0	1	1	0	0
	1	0	1	1	0

Here $f(w, x, y, z) = \sum(5, 7, 11, 12, 13, 15)$

So, K-map will be

		<i>yz</i>			
		00	01	11	10
<i>wx</i>	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

So, its minimized sum of product expression will be $xz + wx'y' + wyz$. Since all the minterms are overlapping, there is no chance of static hazard here.

Now, let's consider the options one by one:

A. $\overline{w}xz, wxy, \overline{xy}z, xyz, wyz$

		yz			
		00	01	11	10
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

Chance of static hazard.

Here, when y changes from 0 to 1, the gate for wyz should give 1 (from earlier 0, assuming $w = z = 1$) and that of $xy'z$ should give 0 (from earlier 1). But there is a possibility of circuit giving 0 (static 1 hazard) momentarily due to gate delays ($xy'z$ coming first and wyz coming later). In order to avoid this, we must add a gate with wxz also which ensure that all adjacent blocks in K -map are overlapped or a single variable change cannot momentarily change the circuit output.

B. $wxy, \bar{w}xz, wyz$

This is not correct as wxy is not a minterm for the given function

C. $wx\bar{y}z, xz, \bar{w}xyz$

		yz			
		00	01	11	10
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

Here, also static-1 hazard is possible as the middle 4 pairs are separated by 1 bit difference to both $wxy'z'$ as well as $wx'y'z$. Could have been avoided by using wxy' instead of $wxy'z'$ and wyz instead of $wx'y'z$ which will ensure that all neighboring blocks are overlapped.

D. $wx\bar{y}, wyz, wxz, \bar{w}xz, \bar{x}yz, xyz$

		yz			
		00	01	11	10
wx	00	0	0	0	0
	01	0	1	1	0
	11	1	1	1	0
	10	0	0	1	0

These minterms cover all the minterms of f and also, all the neighboring 1's are overlapped by minterms. So, no chance of hazard here, and hence is the required answer.

Correct Answer: D.

56 votes

4.33

Synchronous Asynchronous Circuits (4) top

4.33.1 Synchronous Asynchronous Circuits: GATE CSE 1991 | Question: 03-ii top

<https://gateoverflow.in/516>



Advantage of synchronous sequential circuits over asynchronous ones is:

A. faster operation

- B. ease of avoiding problems due to hazards
- C. lower hardware requirement
- D. better noise immunity
- E. none of the above

gate1991 digital-logic normal sequential-circuit synchronous-asynchronous-circuits multiple-selects

Answer

4.33.2 Synchronous Asynchronous Circuits: GATE CSE 1998 | Question: 16 top

https://gateoverflow.in/1730



Design a synchronous counter to go through the following states:

1, 4, 2, 3, 1, 4, 2, 3, 1, 4...

gate1998 digital-logic normal descriptive synchronous-asynchronous-circuits

goclasses.in

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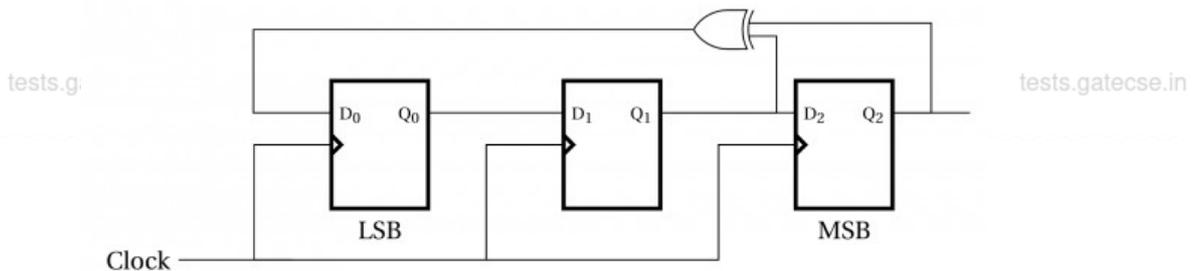
Answer

4.33.3 Synchronous Asynchronous Circuits: GATE CSE 2001 | Question: 2.12 top

https://gateoverflow.in/730



Consider the circuit given below with initial state $Q_0 = 1, Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$



Which one of the following is correct state sequence of the circuit?

- A. 1, 3, 4, 6, 7, 5, 2
- B. 1, 2, 5, 3, 7, 6, 4
- C. 1, 2, 7, 3, 5, 6, 4
- D. 1, 6, 5, 7, 2, 3, 4

gate2001-cse digital-logic normal synchronous-asynchronous-circuits

Answer

4.33.4 Synchronous Asynchronous Circuits: GATE CSE 2003 | Question: 44 top

https://gateoverflow.in/935



A 1-input, 2-output synchronous sequential circuit behaves as follows:

Let z_k, n_k denote the number of 0's and 1's respectively in initial k bits of the input ($z_k + n_k = k$). The circuit outputs 00 until one of the following conditions holds.

- $z_k - n_k = 2$. In this case, the output at the k -th and all subsequent clock ticks is 10.
- $n_k - z_k = 2$. In this case, the output at the k -th and all subsequent clock ticks is 01.

What is the minimum number of states required in the state transition graph of the above circuit?

- A. 5
- B. 6
- C. 7
- D. 8

gate2003-cse digital-logic synchronous-asynchronous-circuits normal

Answer



✓ Synchronization means less chance of hazards but can only increase the delay. So, synchronous circuits cannot have faster operation than asynchronous one but it is easier to avoid hazards in synchronous circuits. So, (A) is false and (B) is true.

(C) is false if we don't consider how to avoid the hazards in asynchronous circuits.

(D) Is not necessarily true - often asynchronous circuits have better noise immunity. Reasons are given here: <http://www.cs.columbia.edu/~nowick/async-applications-PIEEE-99-berkel-josephs-nowick-published.pdf>

https://en.wikipedia.org/wiki/Asynchronous_circuit

References



25 votes

-- Arjun Suresh (332k points)



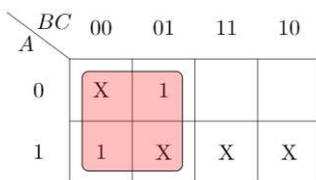
✓ Sequence given is as

1, 4, 2, 3, 1...

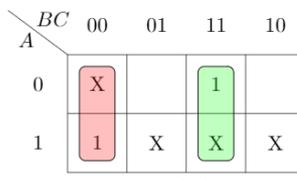
From the given sequence of states we can design the state table and Suppose we are using T-FF for sequential circuit of counter.

Present State			Next State			FF Inputs		
A	B	C	A ⁺	B ⁺	C ⁺	T _A	T _B	T _C
0	0	0	x	x	x	x	x	x
0	0	1	1	0	0	1	0	1
0	1	0	0	1	1	0	0	1
0	1	1	0	0	1	0	1	0
1	0	0	0	1	0	1	1	0
1	0	1	x	x	x	x	x	x
1	1	0	x	x	x	x	x	x
1	1	1	x	x	x	x	x	x

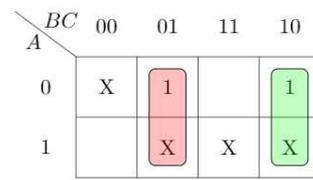
From the above table, we will find the equation of T_A, T_B and T_C



$T_A = B'$



$T_B = B'C' + BC$
 $T_B = B \odot C$

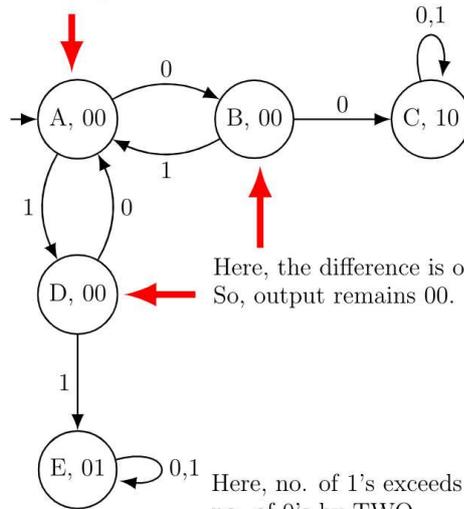


$T_C = B'C + BC'$
 $T_C = B \oplus C$

Initially difference between 0's and 1's is ZERO. So output is 00.

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Here, no. of 0's exceeds no. of 1's by TWO. Once this happens we will always output 10.

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Here, the difference is one. So, output remains 00.

classroom.g

assroom.gateover

Here, no. of 1's exceeds no. of 0's by TWO. Once this happens we will always output 01.

The Automaton will look like this. 😊

👍 97 votes

-- Rajendra Kumar Dangwal (1.2k points)

Answer Keys

4.1.1	N/A	4.1.2	N/A	4.1.3	N/A	4.1.4	B	4.1.5	B
4.1.6	A	4.1.7	B	4.1.8	19.2	4.1.9	B	4.1.10	-1
4.2.1	B	4.2.2	C	4.3.1	C	4.3.2	A	4.4.1	D
4.4.2	C	4.4.3	N/A	4.4.4	N/A	4.4.5	N/A	4.4.6	D
4.4.7	N/A	4.4.8	A	4.4.9	B	4.4.10	D	4.4.11	C
4.4.12	D	4.4.13	C	4.4.14	C	4.4.15	D	4.4.16	D
4.4.17	D	4.4.18	A	4.4.19	A	4.4.20	D	4.4.21	D
4.4.22	B	4.4.23	1	4.4.24	A	4.4.25	C	4.4.26	C
4.4.27	D	4.4.28	B	4.4.29	B;C;D	4.4.30	B	4.4.31	C
4.5.1	N/A	4.5.2	A	4.5.3	B	4.5.4	A	4.5.5	C
4.5.6	B	4.6.1	A	4.6.2	C	4.6.3	A	4.6.4	3
4.6.5	A	4.6.6	3	4.6.7	B	4.7.1	A	4.7.2	B
4.8.1	N/A	4.8.2	C	4.8.3	N/A	4.8.4	N/A	4.8.5	A;C
4.8.6	B	4.8.7	B	4.8.8	B	4.8.9	011	4.8.10	D
4.8.11	N/A	4.8.12	N/A	4.8.13	B	4.8.14	B	4.8.15	A
4.8.16	A	4.8.17	A	4.8.18	D	4.8.19	A	4.8.20	A
4.8.21	D	4.8.22	A	4.8.23	C	4.8.24	C	4.8.25	C
4.8.26	A	4.8.27	A	4.8.28	B	4.8.29	D	4.8.30	B

4.8.31	C	4.8.32	C	4.8.33	X	4.8.34	D	4.8.35	C
4.8.36	A	4.8.37	D	4.8.38	B	4.9.1	A	4.10.1	C
4.10.2	1034	4.11.1	B;C	4.11.2	N/A	4.11.3	N/A	4.11.4	D
4.11.5	D	4.11.6	A	4.11.7	C	4.12.1	N/A	4.12.2	N/A
4.12.3	A	4.12.4	C	4.12.5	D	4.12.6	3	4.12.7	4
4.12.8	B	4.12.9	D	4.12.10	D	4.13.1	D	4.14.1	D
4.14.2	C	4.15.1	N/A	4.15.2	C	4.15.3	A	4.15.4	B
4.15.5	2	4.15.6	D	4.16.1	C	4.16.2	N/A	4.16.3	N/A
4.16.4	N/A	4.16.5	N/A	4.16.6	C	4.16.7	D	4.16.8	D
4.16.9	B	4.17.1	N/A	4.17.2	N/A	4.17.3	B;C	4.17.4	A
4.18.1	D	4.18.2	B	4.18.3	A	4.18.4	C	4.18.5	-7.75 : -7.75
4.18.6	C	4.18.7	C	4.19.1	D	4.19.2	N/A	4.19.3	N/A
4.19.4	N/A	4.19.5	N/A	4.19.6	C	4.19.7	C	4.19.8	B
4.19.9	D	4.19.10	A	4.19.11	B	4.19.12	C	4.19.13	A
4.19.14	B	4.19.15	1	4.19.16	A	4.19.17	D	4.19.18	A
4.19.19	C	4.20.1	A;D	4.21.1	C	4.21.2	B	4.21.3	C
4.22.1	N/A	4.22.2	B	4.22.3	B	4.22.4	B	4.23.1	N/A
4.23.2	A	4.24.1	N/A	4.24.2	N/A	4.24.3	9	4.24.4	N/A
4.24.5	A	4.24.6	B	4.24.7	B	4.24.8	A	4.24.9	A
4.24.10	B	4.24.11	3	4.24.12	6 : 6	4.24.13	A	4.25.1	B
4.25.2	N/A	4.25.3	C	4.25.4	C	4.25.5	C	4.25.6	A
4.25.7	C	4.25.8	D	4.25.9	5	4.25.10	A	4.25.11	D
4.25.12	A	4.25.13	N/A	4.26.1	12	4.26.2	N/A	4.26.3	9
4.26.4	N/A	4.26.5	N/A	4.26.6	N/A	4.26.7	N/A	4.26.8	N/A
4.26.9	C	4.26.10	D	4.26.11	C	4.26.12	D	4.26.13	C
4.26.14	A;C	4.26.15	C	4.26.16	B	4.26.17	C	4.26.18	B
4.26.19	D	4.26.20	D	4.26.21	B	4.26.22	N/A	4.26.23	A
4.26.24	D	4.26.25	A	4.26.26	A	4.26.27	A	4.26.28	A
4.26.29	B	4.26.30	D	4.26.31	B	4.26.32	A	4.26.33	B
4.26.34	5	4.26.35	3	4.26.36	5	4.26.37	-11	4.26.38	1
4.26.39	C	4.26.40	D	4.26.41	0.502 : 0.504	4.26.42	C	4.26.43	C
4.26.44	A	4.26.45	3 : 3	4.26.46	B	4.26.47	A	4.26.48	A
4.26.49	C	4.26.50	A	4.26.51	B	4.27.1	False	4.28.1	C
4.28.2	A	4.29.1	N/A	4.29.2	D	4.29.3	D	4.29.4	B
4.30.1	C	4.30.2	N/A	4.30.3	33.33	4.30.4	N/A	4.30.5	A
4.30.6	N/A	4.31.1	D	4.31.2	N/A	4.32.1	D	4.33.1	B

4.33.2

N/A

4.33.3

B

4.33.4

A



System calls, Processes, Threads, Inter-process communication, Concurrency and synchronization. Deadlock. CPU scheduling. Memory management and Virtual memory. File systems. Disks is also under this

Mark Distribution in Previous GATE

Year	2021-1	2021-2	2020	2019	2018	2017-1	2017-2	2016-1	2016-2	Minimum	Average	Maximum
1 Mark Count	4	2	2	2	3	2	2	1	1	1	2.1	4
2 Marks Count	1	3	4	4	3	2	2	4	3	1	2.8	4
Total Marks	6	8	10	10	9	6	6	9	7	6	7.8	10

5.1.1 Context Switch: GATE CSE 1999 | Question: 2.12 [top](#)

<https://gateoverflow.in/1490>



Which of the following actions is/are typically not performed by the operating system when switching context from process A to process B ?

- Saving current register values and restoring saved register values for process B .
- Changing address translation tables.
- Swapping out the memory image of process A to the disk.
- Invalidating the translation look-aside buffer.

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gate1999 operating-system context-switch normal

Answer [🔗](#)

5.1.2 Context Switch: GATE CSE 2000 | Question: 1.20, ISRO2008-47 [top](#)

<https://gateoverflow.in/644>



Which of the following need not necessarily be saved on a context switch between processes?

- General purpose registers
- Translation look-aside buffer
- Program counter
- All of the above

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gate2000-cse operating-system easy isro2008 context-switch

Answer [🔗](#)

5.1.3 Context Switch: GATE CSE 2011 | Question: 6, UGCNET-June2013-III: 62 [top](#)

<https://gateoverflow.in/2108>



Let the time taken to switch from user mode to kernel mode of execution be T_1 while time taken to switch between two user processes be T_2 . Which of the following is correct?

- $T_1 > T_2$
- $T_1 = T_2$
- $T_1 < T_2$
- Nothing can be said about the relation between T_1 and T_2

gate2011-cse operating-system context-switch easy ugcnetjune2013iii

Answer [🔗](#)

Answers: Context Switch

5.1.1 Context Switch: GATE CSE 1999 | Question: 2.12 [top](#)

<https://gateoverflow.in/1490>



- ✓ Processes are generally swapped out from memory to Disk (secondary memory) when they are suspended. So. Processes are not swapped during context switching.

TLB : Whenever any page table entry is referred for the first time it is temporarily saved in TLB. Every element of this memory has a tag. And whenever anything is searched it is compared against TLB and we can get that entry/data with less memory access.

And Invalidation of TLB means resetting TLB which is necessary because a TLB entry may belong to any page table of any process thus resetting ensures that the entry corresponds to the process that we are searching for.

Hence, option (C) is correct.

👍 90 votes

-- Manish Joshi (20.5k points)

5.1.2 Context Switch: GATE CSE 2000 | Question: 1.20, ISRO2008-47 [top](#)

<https://gateoverflow.in/644>



✓ Answer: (B)

We don't need to save TLB or cache to ensure correct program resumption. They are just bonus for ensuring better performance. But PC, stack and registers must be saved as otherwise program cannot resume.

👍 52 votes

-- Rajarshi Sarkar (27.9k points)

5.1.3 Context Switch: GATE CSE 2011 | Question: 6, UGCNET-June2013-III: 62 [top](#)

<https://gateoverflow.in/2108>



✓ Time taken to switch two processes is very large as compared to time taken to switch between kernel and user mode of execution because :

When you switch processes, you have to do a context switch, save the PCB of previous process (note that the PCB of a process in Linux has over 95 entries), then save registers and then load the PCB of new process and load its registers etc.

When you switch between kernel and user mode of execution, OS has to just **change a single bit** at hardware level which is very fast operation.

So, answer is: (C).

👍 116 votes

-- Mojo Jojo (2.8k points)

Context switches can occur only in kernel mode. So, to do context switch first switch from user mode to kernel mode and then do context switch (save the PCB of the previous process and load the PCB of new process)

Context switch = user - kernel switch + save/load PCB + kernel-user switch

C is answer.

👍 79 votes

-- Sachin Mittal (15.8k points)

5.2 Deadlock Prevention Avoidance Detection (4) [top](#)

5.2.1 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 24 [top](#)

<https://gateoverflow.in/204098>



Consider a system with 3 processes that share 4 instances of the same resource type. Each process can request a maximum of K instances. Resources can be requested and releases only one at a time. The largest value of K that will always avoid deadlock is

gate2018-cse operating-system deadlock-prevention-avoidance-detection easy numerical-answers

Answer 🗨

5.2.2 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 39 [top](#)

<https://gateoverflow.in/204113>



In a system, there are three types of resources: E , F and G . Four processes P_0 , P_1 , P_2 and P_3 execute concurrently. At the outset, the processes have declared their maximum resource requirements using a matrix named Max as given below. For example, $\text{Max}[P_2, F]$ is the maximum number of instances of F that P_2 would require. The number of instances of the resources allocated to the various processes at any given state is given by a matrix named Allocation.

Consider a state of the system with the Allocation matrix as shown below, and in which 3 instances of E and 3 instances of F are only resources available.

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Allocation				Max			
	E	F	G		E	F	G
P_0	1	0	1	P_0	4	3	1
P_1	1	1	2	P_1	2	1	4
P_2	1	0	3	P_2	1	3	3
P_3	2	0	0	P_3	5	4	1

From the perspective of deadlock avoidance, which one of the following is true?

- A. The system is in *safe* state
- B. The system is not in *safe* state, but would be *safe* if one more instance of *E* were available
- C. The system is not in *safe* state, but would be *safe* if one more instance of *F* were available
- D. The system is not in *safe* state, but would be *safe* if one more instance of *G* were available

gate2018-cse operating-system deadlock-prevention-avoidance-detection normal

Answer

5.2.3 Deadlock Prevention Avoidance Detection: GATE CSE 2021 Set 2 | Question: 43 top

<https://gateoverflow.in/357497>



Consider a computer system with multiple shared resource types, with one instance per resource type. Each instance can be owned by only one process at a time. Owning and freeing of resources are done by holding a global lock (L). The following scheme is used to own a resource instance:

```
function OWNRESOURCE (Resource R)
  Acquire lock L // a global lock
  if R is available then
    Acquire R
    Release lock L
  else
    if R is owned by another process P then
      Terminate P, after releasing all resources owned by P
    Acquire R
    Restart P
    Release lock L
  end if
end if
end function
```

Which of the following choice(s) about the above scheme is/are correct?

- A. The scheme ensures that deadlocks will not occur
- B. The scheme may lead to live-lock
- C. The scheme may lead to starvation
- D. The scheme violates the mutual exclusion property

gate2021-cse-set2 multiple-selects operating-system deadlock-prevention-avoidance-detection

Answer

5.2.4 Deadlock Prevention Avoidance Detection: GATE IT 2004 | Question: 63 top

<https://gateoverflow.in/3706>



In a certain operating system, deadlock prevention is attempted using the following scheme. Each process is assigned a unique timestamp, and is restarted with the same timestamp if killed. Let P_h be the process holding a resource R , P_r be a process requesting for the same resource R , and $T(P_h)$ and $T(P_r)$ be their timestamps respectively. The decision to wait or preempt one of the processes is based on the following algorithm.

```
if T( $P_r$ ) < T( $P_h$ ) then
  kill  $P_r$ 
else wait
```

Which one of the following is TRUE?

- A. The scheme is deadlock-free, but not starvation-free
- B. The scheme is not deadlock-free, but starvation-free
- C. The scheme is neither deadlock-free nor starvation-free
- D. The scheme is both deadlock-free and starvation-free

gate2004-it operating-system normal deadlock-prevention-avoidance-detection

5.2.1 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 24

<https://gateoverflow.in/204098>

- ✓ Number of processes = 3
Number of Resources = 4

Let's distribute each process one less than maximum demand ($K - 1$) resources. i.e. $3(K - 1)$
Provide an additional resource to any of three processes for deadlock avoidance.

$$\text{Total resources} = 3(K - 1) + 1 = 3K - 2$$

Now, this $3K - 2$ should be less than or equal to the number of resources we have right now.

$$3K - 2 \leq 4$$

$$3K \leq 6$$

$$K \leq 2$$

So, largest value of $K = 2$

👍 68 votes

-- Digvijay (44.9k points)

5.2.2 Deadlock Prevention Avoidance Detection: GATE CSE 2018 | Question: 39

<https://gateoverflow.in/204113>

✓

Allocation				Max				Need=Max-Allocation			
Process	E	F	G	Process	E	F	G	Process	E	F	G
P_0	1	0	1	P_0	4	3	1	P_0	3	3	0
P_1	1	1	2	P_1	2	1	4	P_1	1	0	2
P_2	1	0	3	P_2	1	3	3	P_2	0	3	0
P_3	2	0	0	P_3	5	4	1	P_3	3	4	1

Available Resource (3, 3, 0)

With (3, 3, 0) we can satisfy the request of either P_0 or P_2 .

Let's assume request of P_0 satisfied.

After execution, it will release resources.

$$\text{Available Resource} = (3, 3, 0) + (1, 0, 1) = (4, 3, 1)$$

Give (0, 3, 0) out of (4, 3, 1) unit of resources to P_2 and P_2 will complete its execution.

After execution, it will release resources.

$$\text{Available Resource} = (4, 3, 1) + (1, 0, 3) = (5, 3, 4)$$

Allocate (1, 0, 2) out of (5, 3, 4) unit of resources to P_1 and P_1 will complete its execution.

After execution, it will release resources.

$$\text{Available Resource} = (5, 3, 4) + (1, 1, 2) = (6, 4, 6)$$

And finally, allocate resources to P_3 .

So, we have one of the possible safe sequence: $P_0 \rightarrow P_2 \rightarrow P_1 \rightarrow P_3$

Correct Answer: A

👍 18 votes

-- Digvijay (44.9k points)

5.2.3 Deadlock Prevention Avoidance Detection: GATE CSE 2021 Set 2 | Question: 43

<https://gateoverflow.in/357497>

- ✓ A system is in **Deadlock** when all the processes are in **Waiting** state. This is similar to a traffic jam where no vehicle moves.

A system is in **Livelock** when the processes do **repeated** work without any progress for the system (still no useful work). This is similar to a traffic jam where some vehicles reverse and then move forward hitting the same block again.

Now, both deadlock and livelock are **mutually exclusive** – at any point of time only one can happen in a system. But both of

them imply no progress for system and hence starvation for the processes involved.

Now, coming to the given question, any process can kick out another process and then acquire the needed resource and this can go in a **cyclic fashion ensuring a livelock**. There is no possibility of a deadlock as at any time a process is free to kick out another process. Since there is a possibility of livelock, starvation possibility is also there. So, options A, B and C are TRUE.

A process is acquiring the resource owned by another process only after terminating the other process. Hence there is no violation of mutual exclusion property here.

Correct Answer: A;B;C.

References



1 votes

-- Arjun Suresh (332k points)

5.2.4 Deadlock Prevention Avoidance Detection: GATE IT 2004 | Question: 63 [top](#)

<https://gateoverflow.in/3706>



✓ **Answer is (A).**

When the process wakes up again after it has been killed once or twice IT WILL HAVE SAME TIME-STAMP as it had WHEN IT WAS KILLED FIRST TIME. And that time stamp can never be greater than a process that was killed after that or a NEW process that may have arrived.

So every time when the killed process wakes up it MIGHT ALWAYS find a new process that will say "your time stamp is less than me and I take this resource", which of course is as we know, and that process will again be killed.

This may happen indefinitely if processes keep coming and killing that "INNOCENT" process every time it try to access.

So, **STARVATION is possible. Deadlock is not possible.**

70 votes

-- Sandeep_Uniyal (6.5k points)

5.3

Disk Scheduling (13) [top](#)

5.3.1 Disk Scheduling: GATE CSE 1989 | Question: 4-xii [top](#)

<https://gateoverflow.in/8822>



Disk requests come to disk driver for cylinders 10, 22, 20, 2, 40, 6 and 38, in that order at a time when the disk drive is reading from cylinder 20. The seek time is 6 msec per cylinder. Compute the total seek time if the disk arm scheduling algorithm is.

- A. First come first served.
- B. Closest cylinder next.

gate1989 descriptive operating-system disk-scheduling

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Answer

5.3.2 Disk Scheduling: GATE CSE 1990 | Question: 9b [top](#)

<https://gateoverflow.in/85678>



Assuming the current disk cylinder to be 50 and the sequence for the cylinders to be 1, 36, 49, 65, 53, 12, 3, 20, 55, 16, 65 and 78 find the sequence of servicing using

- 1. Shortest seek time first (SSTF) and
- 2. Elevator disk scheduling policies.

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gate1990 descriptive operating-system disk-scheduling

Answer

5.3.3 Disk Scheduling: GATE CSE 1995 | Question: 20 [top](#)

<https://gateoverflow.in/2658>



The head of a moving head disk with 100 tracks numbered 0 to 99 is currently serving a request at track 55. If the queue of requests kept in FIFO order is

which of the two disk scheduling algorithms FCFS (First Come First Served) and SSTF (Shortest Seek Time First) will require less head movement? Find the head movement for each of the algorithms.

gate1995 operating-system disk-scheduling normal descriptive

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Answer 

5.3.4 Disk Scheduling: GATE CSE 1999 | Question: 1.10 [top](#)

<https://gateoverflow.in/1463>



Which of the following disk scheduling strategies is likely to give the best throughput?

- A. Farthest cylinder next
- B. Nearest cylinder next
- C. First come first served
- D. Elevator algorithm

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gate1999 operating-system disk-scheduling normal

Answer 

5.3.5 Disk Scheduling: GATE CSE 2004 | Question: 12 [top](#)

<https://gateoverflow.in/1009>



Consider an operating system capable of loading and executing a single sequential user process at a time. The disk head scheduling algorithm used is First Come First Served (FCFS). If FCFS is replaced by Shortest Seek Time First (SSTF), claimed by the vendor to give 50% better benchmark results, what is the expected improvement in the I/O performance of user programs?

- A. 50%
- B. 40%
- C. 25%
- D. 0%

gate2004-cse operating-system disk-scheduling normal

Answer 

5.3.6 Disk Scheduling: GATE CSE 2009 | Question: 31 [top](#)

<https://gateoverflow.in/1317>



Consider a disk system with 100 cylinders. The requests to access the cylinders occur in following sequence:

4, 34, 10, 7, 19, 73, 2, 15, 6, 20

Assuming that the head is currently at cylinder 50, what is the time taken to satisfy all requests if it takes 1ms to move from one cylinder to adjacent one and shortest seek time first policy is used?

- A. 95 ms
- B. 119 ms
- C. 233 ms
- D. 276 ms

gate2009-cse operating-system disk-scheduling normal

Answer 

5.3.7 Disk Scheduling: GATE CSE 2014 Set 1 | Question: 19 [top](#)

<https://gateoverflow.in/1786>



Suppose a disk has 201 cylinders, numbered from 0 to 200. At some time the disk arm is at cylinder 100, and there is a queue of disk access requests for cylinders 30, 85, 90, 100, 105, 110, 135 and 145. If Shortest-Seek Time First (SSTF) is being used for scheduling the disk access, the request for cylinder 90 is serviced after servicing _____ number of requests.

gate2014-cse-set1 operating-system disk-scheduling numerical-answers normal

Answer 



Suppose the following disk request sequence (track numbers) for a disk with 100 tracks is given:

45, 20, 90, 10, 50, 60, 80, 25, 70.

Assume that the initial position of the R/W head is on track 50. The additional distance that will be traversed by the R/W head when the Shortest Seek Time First (SSTF) algorithm is used compared to the SCAN (Elevator) algorithm (assuming that SCAN algorithm moves towards 100 when it starts execution) is _____ tracks.

gate2015-cse-set1 operating-system disk-scheduling normal numerical-answers

Answer



Cylinder a disk queue with requests for I/O to blocks on cylinders 47, 38, 121, 191, 87, 11, 92, 10. The C-LOOK scheduling algorithm is used. The head is initially at cylinder number 63, moving towards larger cylinder numbers on its servicing pass. The cylinders are numbered from 0 to 199. The total head movement (in number of cylinders) incurred while servicing these requests is _____.

gate2016-cse-set1 operating-system disk-scheduling normal numerical-answers

Answer



Consider the following five disk five disk access requests of the form (request id, cylinder number) that are present in the disk scheduler queue at a given time.

$(P, 155), (Q, 85), (R, 110), (S, 30), (T, 115)$

Assume the head is positioned at cylinder 100. The scheduler follows Shortest Seek Time First scheduling to service the requests.

Which one of the following statements is FALSE?

- A. T is serviced before P .
- B. Q is serviced after S , but before T .
- C. The head reverses its direction of movement between servicing of Q and P .
- D. R is serviced before P .

gate2020-cse operating-system disk-scheduling

Answer



A disk has 200 tracks (numbered 0 through 199). At a given time, it was servicing the request of reading data from track 120, and at the previous request, service was for track 90. The pending requests (in order of their arrival) are for track numbers.

30 70 115 130 110 80 20 25.

How many times will the head change its direction for the disk scheduling policies SSTF (Shortest Seek Time First) and FCFS (First Come First Serve)?

- A. 2 and 3
- B. 3 and 3
- C. 3 and 4
- D. 4 and 4

gate2004-it operating-system disk-scheduling normal

Answer



The head of a hard disk serves requests following the shortest seek time first (SSTF) policy. The head is initially positioned at track number 180.

Which of the request sets will cause the head to change its direction after servicing every request assuming that the head does not change direction if there is a tie in SSTF and all the requests arrive before the servicing starts?

- A. 11, 139, 170, 178, 181, 184, 201, 265
- B. 10, 138, 170, 178, 181, 185, 201, 265
- C. 10, 139, 169, 178, 181, 184, 201, 265
- D. 10, 138, 170, 178, 181, 185, 200, 265

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gate2007-it operating-system disk-scheduling normal

Answer

5.3.13 Disk Scheduling: GATE IT 2007 | Question: 83 top

https://gateoverflow.in/3535



The head of a hard disk serves requests following the shortest seek time first (SSTF) policy.

What is the maximum cardinality of the request set, so that the head changes its direction after servicing every request if the total number of tracks are 2048 and the head can start from any track?

- A. 9
- B. 10
- C. 11
- D. 12

gate2007-it operating-system disk-scheduling normal

Answer

Answers: Disk Scheduling

5.3.1 Disk Scheduling: GATE CSE 1989 | Question: 4-xii top

https://gateoverflow.in/8822

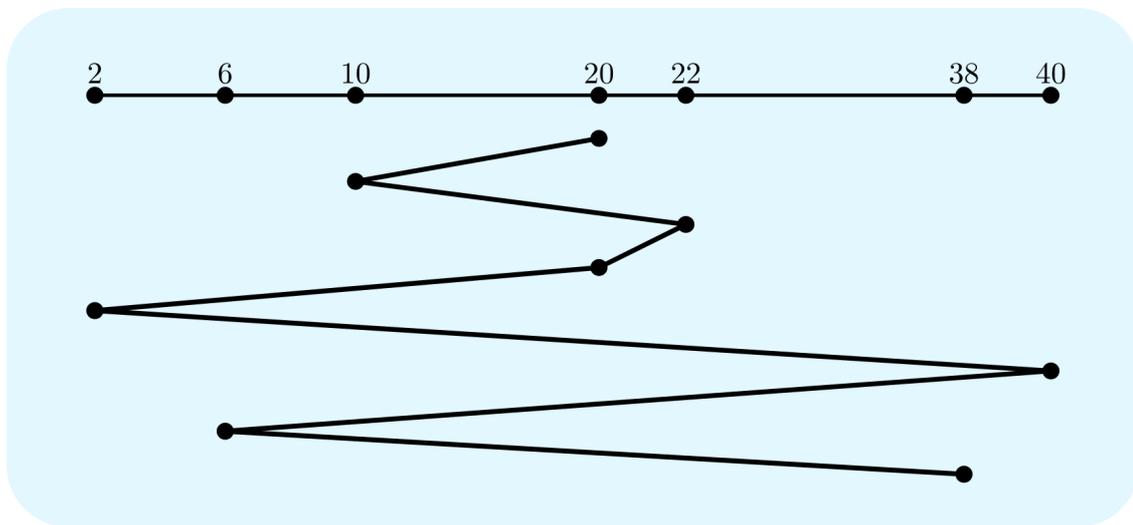


✓

A. In FCFS sequence will be $\Rightarrow 20, 10, 22, 20, 2, 40, 6, 38$

Total movement: $|20 - 10| + |10 - 22| + |22 - 20| + |20 - 2| + |2 - 40| + |40 - 6| + |6 - 38| = 146$

So total seek time = $146 \times 6 = 876\text{msec}$



FCFS

B. In **Closest cylinder next** sequence will be $\Rightarrow 20, 22, 10, 6, 2, 38, 40$

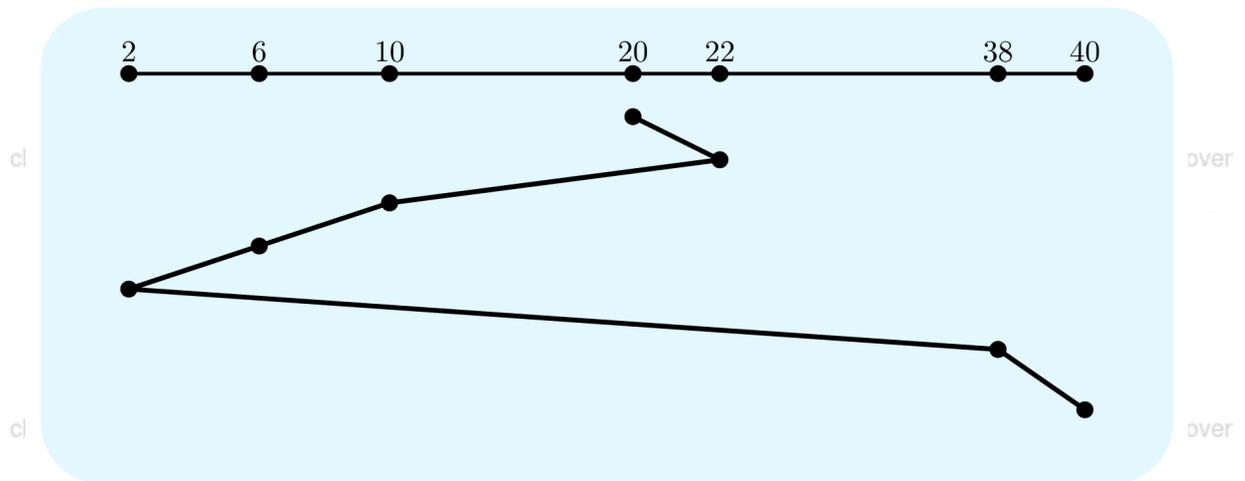
Total movement: $|20 - 22| + |22 - 10| + |10 - 6| + |6 - 2| + |2 - 38| + |38 - 40| = 60$

So total seek time = $60 \times 6 = 360\text{msec}$

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Closest cylinder next

👍 27 votes

-- Lokesh Dafale (8.2k points)

5.3.2 Disk Scheduling: GATE CSE 1990 | Question: 9b [top](#)

<https://gateoverflow.in/85678>



1. SSTF
Sequence will be $\Rightarrow 50, 49, 53, 55, 65, 65, 78, 36, 20, 16, 12, 3, 1$

2. Elevator disk scheduling (SCAN)
*Here, I assume
78 is the extreme point*
Sequence will be $\Rightarrow 50, 53, 55, 65, 65, 78, 49, 36, 20, 16, 12, 3, 1$

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! SCAN(Elevator) It scans down towards the nearest end first

👍 15 votes

-- Lokesh Dafale (8.2k points)

5.3.3 Disk Scheduling: GATE CSE 1995 | Question: 20 [top](#)

<https://gateoverflow.in/2658>



✓ FCFS : $55 \rightarrow 10 \rightarrow 70 \rightarrow 75 \rightarrow 23 \rightarrow 65 \Rightarrow 45 + 60 + 5 + 52 + 42 = 204$.

SSTF : $55 \rightarrow 65 \rightarrow 70 \rightarrow 75 \rightarrow 23 \rightarrow 10 \Rightarrow 10 + 5 + 5 + 52 + 13 = 85$

Hence, SSTF.

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👍 32 votes

-- kireeti (1k points)

5.3.4 Disk Scheduling: GATE CSE 1999 | Question: 1.10 [top](#)

<https://gateoverflow.in/1463>



- A. Farthest cylinder next \rightarrow This might be candidate for worst algorithm . This is false.
- B. Nearest cylinder next \rightarrow This is output.
- C. First come first served \rightarrow This will not give best throughput, It is random .
- D. Elevator algorithm \rightarrow This is good but issue is that once direction is fixed we don't come back, until we go all the other way. So it does not give best throughput.

Correct Answer: B

👍 36 votes

-- Akash Kanase (36k points)



- ✓ Question says "single sequential user process". So, all the requests to disk scheduler will be in sequence and each one will be blocking the execution and hence there is no use of any disk scheduling algorithm. Any disk scheduling algorithm gives the same input sequence and hence the improvement will be 0% for SSTF over FCFS.

Correct Answer: *D*

👍 74 votes

-- Arjun Suresh (332k points)



- ✓ Answer is **(B)**.
- $$= (50 - 34) + (34 - 20) + (20 - 19) + (19 - 15) + (15 - 10) + (10 - 7) + (7 - 6) + (6 - 4) + (4 - 2) + (73 - 2)$$
- $$= 16 + 14 + 1 + 4 + 5 + 3 + 1 + 2 + 2 + 71$$
- $$= 119 \text{ ms}$$

👍 25 votes

-- Sona Praneeth Akula (3.4k points)



- ✓ Requests are serviced in following order

100 105 110 90 85 135 145 30

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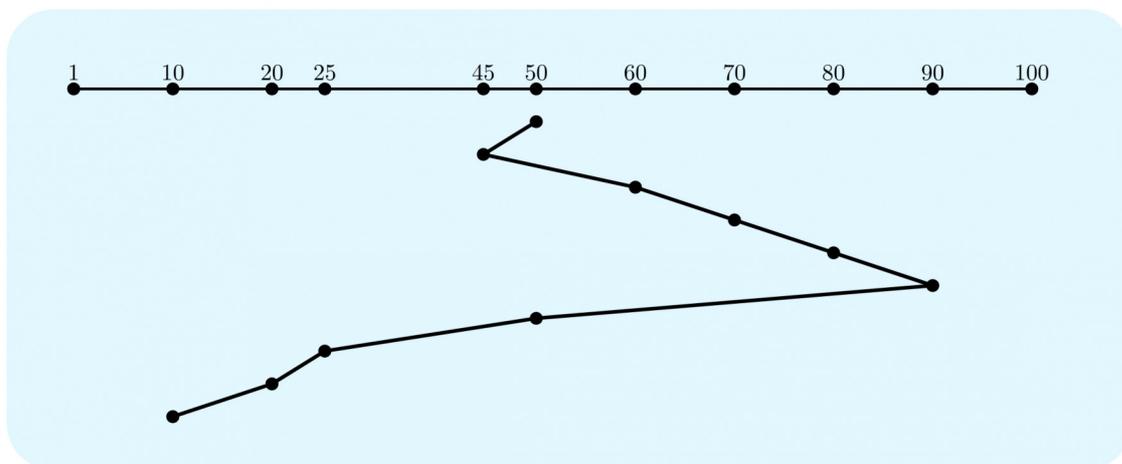
So, request of 90 is serviced after 3 requests.

👍 36 votes

-- Pooja Palod (24.1k points)



- ✓ Refer : <http://www.cs.iit.edu/~cs561/cs450/disksched/disksched.html>

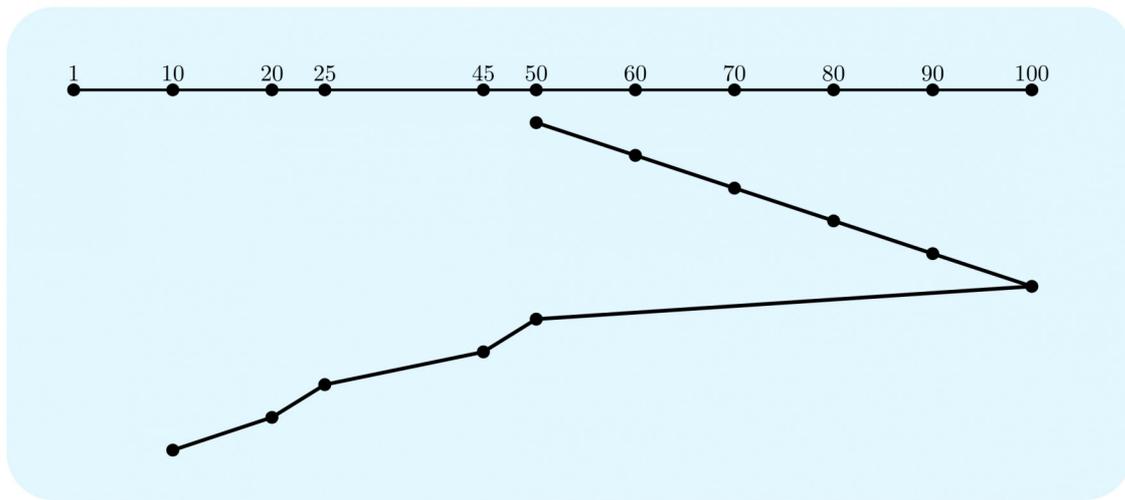


Shortest seek time first(SSTF)

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SCAN(Elevator)

So, for SSTF it takes 130 head movements and for SCAN it takes 140 head movements.

Hence, not additional but $140 - 130 = 10$ less head movements SSTF takes.

References



65 votes

-- Amar Vashishth (25.2k points)

5.3.9 Disk Scheduling: GATE CSE 2016 Set 1 | Question: 48

<https://gateoverflow.in/39716>



- ✓ 63 → 191 = 128
- 191 → 10 = 181
- 10 → 47 = 37
- Total = 346

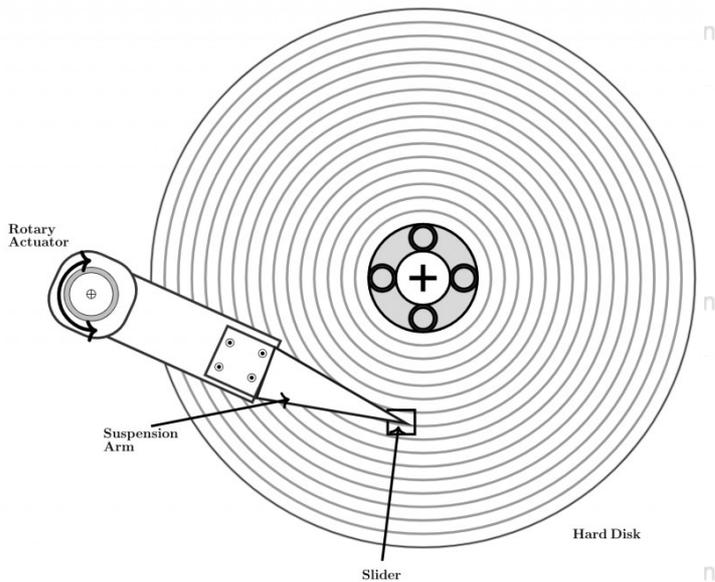
67 votes

-- Abhilash Panicker (7.6k points)

Answer is 346 as already calculated in answers here. Those having some doubt regarding long jump can check this image.

In the question Total Head Movements are asked. When Head reaches any End, **there is no mechanism for head to jump directly to some arbitrary track. It has to Move. So it has to move along the tracks to reach Track Request on other side. Therefore head will move and we must count it.**

Since the purpose of disk scheduling algorithms is to reduce such Head movements by finding an Optimal algorithm. If we ignore the move which is actually happening in disk, that doesn't serve the purpose of analyzing the algorithms.



32 votes

-- Anurag Semwal (6.7k points)

5.3.10 Disk Scheduling: GATE CSE 2020 | Question: 35 [top 5](#)

<https://gateoverflow.in/333196>

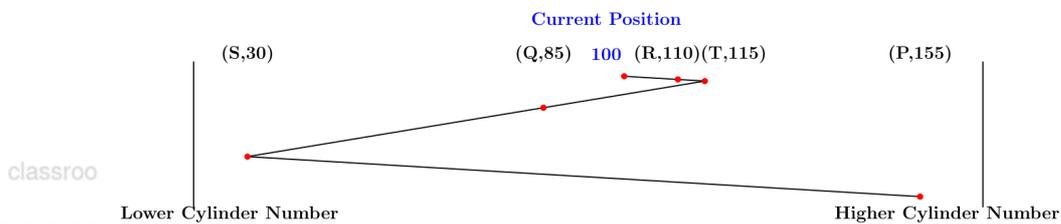


✓ Shortest Seek Time First (SSTF), selects the request with minimum to seek time first from the current head position.

In the given question disk requests are given in the form of $\langle \text{request id, cylinder number} \rangle$

Cylinder Queue: $(P, 155), (Q, 85), (R, 110), (S, 30), (T, 115)$

Head starts at: 100



- It is clear that R and T are serviced before P .
- Q is serviced when head is moving towards lower cylinders and P is serviced when head is moving towards higher cylinders thus reverses its direction at S .

Option B) is the correct answer

7 votes

-- Ashwani Kumar (1.3k points)

5.3.11 Disk Scheduling: GATE IT 2004 | Question: 62 [top 5](#)

<https://gateoverflow.in/3705>



✓ Answer is (C)

SSTF: (90) 120 115 110 130 80 70 30 25 20

Direction changes at 120, 110, 130

FCFS: (90) 120 30 70 115 130 110 80 20 25

direction changes at 120, 30, 130, 20

42 votes

-- Sandeep_Uniyal (6.5k points)

5.3.12 Disk Scheduling: GATE IT 2007 | Question: 82 [top 5](#)

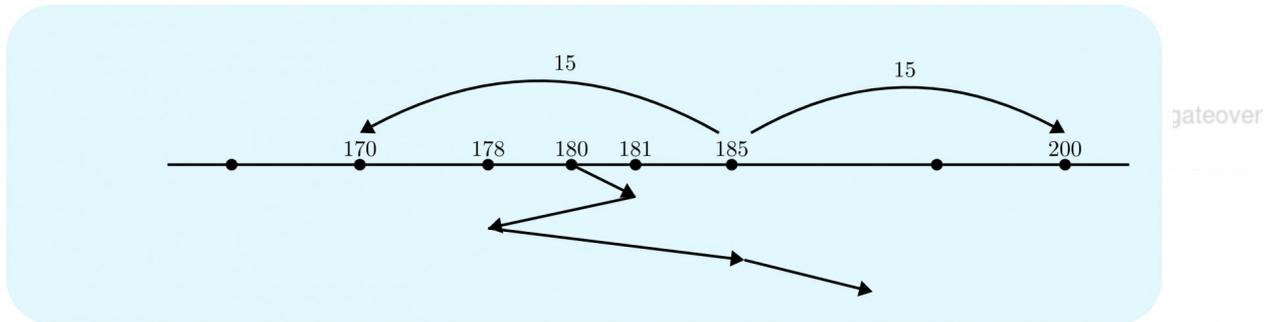
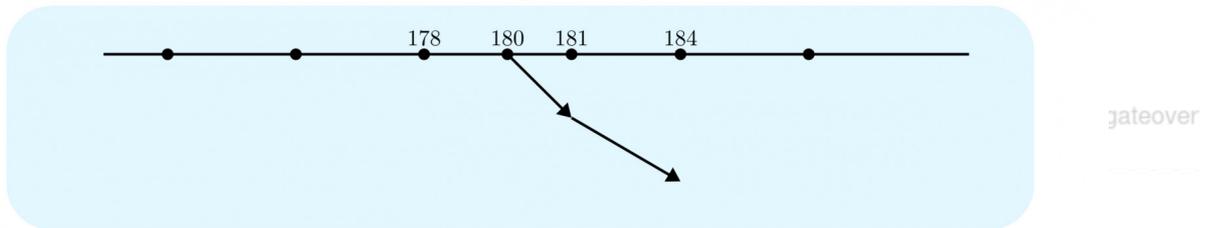
<https://gateoverflow.in/3534>



✓ It should be (B).

When the head starts from 180. It seeks the nearest track which is 181. Then, from 181 it seeks the nearest one which is 178 and 184. But the difference in both from 181 is same and as given in the question. If there is a tie then the head won't change its direction, and therefore to change the direction we need to consider 178. and thus we can eliminate option (A) and (C).

We need head direction change after every request service



Coming next to option (B) and (D).

Following the above procedure you'll see that option (D) is eliminated on similar ground. And thus you can say option (B) is correct.

25 votes

-- Gate Keeda (15.9k points)

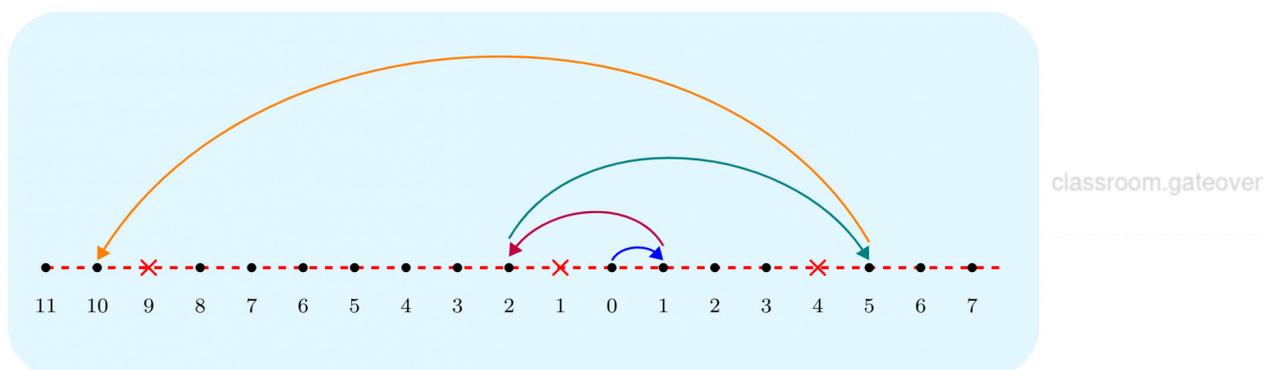


✓ We need **two** conditions to satisfy:

1. The **alternating direction** with **shortest seeks time first policy**.
2. Maximize the no. of requests.

The first condition can be satisfied by not having two requests in the equal distance from the current location. As shown below, we must not have request located in the **red marked** positions.

Now to maximize the no of request we need the requests to be located as **compact** as possible. Which can be done by just placing the request in the next position after the **red marked** position in a particular direction (the direction in which the head over need to move now to satisfy the 1st criteria).



Seek length sequences for maximum cardinality and alternating head movements:

- 1, 3, 7, 15, ...

- Or, $2^1 - 1, 2^2 - 1, 2^3 - 1, 2^4 - 1, \dots$
- We have 2048 tracks so, maximum swing (seek length) can be 2047
- Which corresponds to a seek length of $2^{11} - 1$ in the 11th service.

Correct Answer: C

👍 74 votes

-- Debashish Deka (40.8k points)

5.4

Disks (31) [top](#)

5.4.1 Disks: GATE CSE 1990 | Question: 7-c [top](#)

<https://gateoverflow.in/85406>



A certain moving arm disk-storage device has the following specifications:

- Number of tracks per surface = 404
- Track storage capacity = 130030 bytes.
- Disk speed = 3600 rpm
- Average seek time = 30 m secs.

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Estimate the average latency, the disk storage capacity, and the data transfer rate.

gate1990 operating-system disks descriptive

Answer [👍](#)

5.4.2 Disks: GATE CSE 1993 | Question: 6.7 [top](#)

<https://gateoverflow.in/2289>



A certain moving arm disk storage, with one head, has the following specifications:

- Number of tracks/recording surface = 200
- Disk rotation speed = 2400 rpm
- Track storage capacity = 62,500 bits

The average latency of this device is P ms and the data transfer rate is Q bits/sec. Write the values of P and Q.

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goclasses.in

tests.gatecse.in

gate1993 operating-system disks normal descriptive

Answer [👍](#)

5.4.3 Disks: GATE CSE 1993 | Question: 7.8 [top](#)

<https://gateoverflow.in/2296>



The root directory of a disk should be placed

- at a fixed address in main memory
- at a fixed location on the disk
- anywhere on the disk
- at a fixed location on the system disk
- anywhere on the system disk

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gate1993 operating-system disks normal

Answer [👍](#)

5.4.4 Disks: GATE CSE 1995 | Question: 14 [top](#)

<https://gateoverflow.in/2650>



If the overhead for formatting a disk is 96 bytes for a 4000 byte sector,

- Compute the unformatted capacity of the disk for the following parameters:
 - Number of surfaces: 8
 - Outer diameter of the disk: 12 cm
 - Inner diameter of the disk: 4 cm
 - Inner track space: 0.1 mm
 - Number of sectors per track: 20
- If the disk in (A) is rotating at 360 rpm, determine the effective data transfer rate which is defined as the number of bytes transferred per second between disk and memory.

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tests.gatecse.in

Answer

5.4.5 Disks: GATE CSE 1996 | Question: 23 top

<https://gateoverflow.in/2775>

A file system with a one-level directory structure is implemented on a disk with disk block size of $4K$ bytes. The disk is used as follows:

Disk-block 0	File Allocation Table, consisting of one 8-bit entry per data block, representing the data block address of the next data block in the file
Disk-block 1	Directory, with one 32 bit entry per file:
Disk-block 2	Data-block 1;
Disk-block 3	Data-block 2; etc.

- What is the maximum possible number of files?
- What is the maximum possible file size in blocks

Answer

5.4.6 Disks: GATE CSE 1997 | Question: 74 top

<https://gateoverflow.in/19704>

A program P reads and processes 1000 consecutive records from a sequential file F stored on device D without using any file system facilities. Given the following

- Size of each record = 3200 bytes
- Access time of D = 10 msec
- Data transfer rate of D = 800×10^3 bytes/second
- CPU time to process each record = 3 msec

What is the elapsed time of P if

- F contains unblocked records and P does not use buffering?
- F contains unblocked records and P uses one buffer (i.e., it always reads ahead into the buffer)?
- records of F are organized using a blocking factor of 2 (i.e., each block on D contains two records of F) and P uses one buffer?

Answer

5.4.7 Disks: GATE CSE 1998 | Question: 2-9 top

<https://gateoverflow.in/1681>

Formatting for a floppy disk refers to

- arranging the data on the disk in contiguous fashion
- writing the directory
- erasing the system data
- writing identification information on all tracks and sectors

Answer

5.4.8 Disks: GATE CSE 1998 | Question: 25-a top

<https://gateoverflow.in/1740>

Free disk space can be used to keep track of using a free list or a bit map. Disk addresses require d bits. For a disk with B blocks, F of which are free, state the condition under which the free list uses less space than the bit map.

gate1998 operating-system disks descriptive

Answer 

5.4.9 Disks: GATE CSE 1998 | Question: 25b [top](#)

<https://gateoverflow.in/41055>



Consider a disk with c cylinders, t tracks per cylinder, s sectors per track and a sector length s_L . A logical file d_i with fixed record length r_i is stored continuously on this disk starting at location (c_L, t_L, s_L) , where c_L, t_L and s_L are the cylinder, track and sector numbers, respectively. Derive the formula to calculate the disk address (i.e. cylinder, track and sector) of a logical record n assuming that $r_i = s_L$.

gate1998 operating-system disks descriptive

Answer 

5.4.10 Disks: GATE CSE 1999 | Question: 2-18, ISRO2008-46 [top](#)

<https://gateoverflow.in/1496>



Raid configurations of the disks are used to provide

- A. Fault-tolerance
- B. High speed
- C. High data density
- D. (A) & (B)

gate1999 operating-system disks easy isro2008

Answer 

5.4.11 Disks: GATE CSE 2001 | Question: 1.22 [top](#)

<https://gateoverflow.in/715>



Which of the following requires a device driver?

- A. Register
- B. Cache
- C. Main memory
- D. Disk

gate2001-cse operating-system disks easy

Answer 

5.4.12 Disks: GATE CSE 2001 | Question: 20 [top](#)

<https://gateoverflow.in/761>



Consider a disk with the 100 tracks numbered from 0 to 99 rotating at 3000 rpm. The number of sectors per track is 100 and the time to move the head between two successive tracks is 0.2 millisecond.

- A. Consider a set of disk requests to read data from tracks 32, 7, 45, 5 and 10. Assuming that the elevator algorithm is used to schedule disk requests, and the head is initially at track 25 moving up (towards larger track numbers), what is the total seek time for servicing the requests?
- B. Consider an initial set of 100 arbitrary disk requests and assume that no new disk requests arrive while servicing these requests. If the head is initially at track 0 and the elevator algorithm is used to schedule disk requests, what is the worst case time to complete all the requests?

gate2001-cse operating-system disks normal descriptive

Answer 

5.4.13 Disks: GATE CSE 2001 | Question: 8 [top](#)

<https://gateoverflow.in/749>



Consider a disk with the following specifications: 20 surfaces, 1000 tracks/surface, 16 sectors/track, data density 1 KB/sector, rotation speed 3000 rpm. The operating system initiates the transfer between the disk and the memory sector-wise. Once the head has been placed on the right track, the disk reads a sector in a single scan. It reads bits from the sector while the head is passing over the sector. The read bits are formed into bytes in a serial-in-parallel-out buffer and each byte is then transferred to memory. The disk

writing is exactly a complementary process.

For parts (C) and (D) below, assume memory read-write time = 0.1 microseconds/byte, interrupt driven transfer has an interrupt overhead = 0.4 microseconds, the DMA initialization, and termination overhead is negligible compared to the total sector transfer time. DMA requests are always granted.

- A. What is the total capacity of the desk?
- B. What is the data transfer rate?
- C. What is the percentage of time the CPU is required for this disk I/O for byte-wise interrupts driven transfer?
- D. What is the maximum percentage of time the CPU is held up for this disk I/O for cycle-stealing DMA transfer?

gate2001-cse operating-system disks normal descriptive

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Answer

5.4.14 Disks: GATE CSE 2003 | Question: 25, ISRO2009-12 top

<https://gateoverflow.in/915>



Using a larger block size in a fixed block size file system leads to

- A. better disk throughput but poorer disk space utilization
- B. better disk throughput and better disk space utilization
- C. poorer disk throughput but better disk space utilization
- D. poorer disk throughput and poorer disk space utilization

gate2003-cse operating-system disks normal isro2009

Answer

5.4.15 Disks: GATE CSE 2004 | Question: 49 top

<https://gateoverflow.in/1045>



A unix-style I-nodes has 10 direct pointers and one single, one double and one triple indirect pointers. Disk block size is 1 Kbyte, disk block address is 32 bits, and 48-bit integers are used. What is the maximum possible file size?

- A. 2^{24} bytes
- B. 2^{32} bytes
- C. 2^{34} bytes
- D. 2^{48} bytes

gate2004-cse operating-system disks normal

goclasses.in

tests.gatecse.in

Answer

5.4.16 Disks: GATE CSE 2005 | Question: 21 top

<https://gateoverflow.in/1357>



What is the swap space in the disk used for?

- A. Saving temporary html pages
- B. Saving process data
- C. Storing the super-block
- D. Storing device drivers

gate2005-cse operating-system disks easy

Answer

5.4.17 Disks: GATE CSE 2007 | Question: 11, ISRO2009-36, ISRO2016-21 top

<https://gateoverflow.in/1209>



Consider a disk pack with 16 surfaces, 128 tracks per surface and 256 sectors per track. 512 bytes of data are stored in a bit serial manner in a sector. The capacity of the disk pack and the number of bits required to specify a particular sector in the disk are respectively:

- A. 256 Mbyte, 19 bits
- B. 256 Mbyte, 28 bits
- C. 512 Mbyte, 20 bits

D. 64 Gbyte, 28 bits

gate2007-cse operating-system disks normal isro2016

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tests.gatecse.in

Answer

5.4.18 Disks: GATE CSE 2008 | Question: 32 top

https://gateoverflow.in/443



For a magnetic disk with concentric circular tracks, the seek latency is not linearly proportional to the seek distance due to

- A. non-uniform distribution of requests
- B. arm starting and stopping inertia
- C. higher capacity of tracks on the periphery of the platter
- D. use of unfair arm scheduling policies

gate2008-cse operating-system disks normal

Answer

5.4.19 Disks: GATE CSE 2009 | Question: 51 top

https://gateoverflow.in/1337



A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s \rangle$, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0^{th} sector is addresses as $\langle 0, 0, 0 \rangle$, the 1^{st} sector as $\langle 0, 0, 1 \rangle$, and so on

The address $\langle 400, 16, 29 \rangle$ corresponds to sector number:

- A. 505035
- B. 505036
- C. 505037
- D. 505038

gate2009-cse operating-system disks normal

Answer

5.4.20 Disks: GATE CSE 2009 | Question: 52 top

https://gateoverflow.in/4347



A hard disk has 63 sectors per track, 10 platters each with 2 recording surfaces and 1000 cylinders. The address of a sector is given as a triple $\langle c, h, s \rangle$, where c is the cylinder number, h is the surface number and s is the sector number. Thus, the 0^{th} sector is addresses as $\langle 0, 0, 0 \rangle$, the 1^{st} sector as $\langle 0, 0, 1 \rangle$, and so on

The address of the 1039^{th} sector is

- A. $\langle 0, 15, 31 \rangle$
- B. $\langle 0, 16, 30 \rangle$
- C. $\langle 0, 16, 31 \rangle$
- D. $\langle 0, 17, 31 \rangle$

gate2009-cse operating-system disks normal

Answer

5.4.21 Disks: GATE CSE 2011 | Question: 44 top

https://gateoverflow.in/2146



An application loads 100 libraries at startup. Loading each library requires exactly one disk access. The seek time of the disk to a random location is given as 10 ms. Rotational speed of disk is 6000 rpm. If all 100 libraries are loaded from random locations on the disk, how long does it take to load all libraries? (The time to transfer data from the disk block once the head has been positioned at the start of the block may be neglected.)

- A. 0.50 s
- B. 1.50 s
- C. 1.25 s
- D. 1.00 s

Answer 5.4.22 Disks: GATE CSE 2012 | Question: 41 [top](#)<https://gateoverflow.in/2149>

A file system with 300 GByte disk uses a file descriptor with 8 direct block addresses, 1 indirect block address and 1 doubly indirect block address. The size of each disk block is 128 Bytes and the size of each disk block address is 8 Bytes. The maximum possible file size in this file system is

- A. 3 KBytes
- B. 35 KBytes
- C. 280 KBytes
- D. dependent on the size of the disk

Answer 5.4.23 Disks: GATE CSE 2013 | Question: 29 [top](#)<https://gateoverflow.in/1540>

Consider a hard disk with 16 recording surfaces (0 – 15) having 16384 cylinders (0 – 16383) and each cylinder contains 64 sectors (0 – 63). Data storage capacity in each sector is 512 bytes. Data are organized cylinder-wise and the addressing format is (cylinder no., surface no., sector no.). A file of size 42797 KB is stored in the disk and the starting disk location of the file is (1200, 9, 40). What is the cylinder number of the last sector of the file, if it is stored in a contiguous manner?

- A. 1281
- B. 1282
- C. 1283
- D. 1284

Answer 5.4.24 Disks: GATE CSE 2014 Set 2 | Question: 20 [top](#)<https://gateoverflow.in/1977>

A FAT (file allocation table) based file system is being used and the total overhead of each entry in the FAT is 4 bytes in size. Given a 100×10^6 bytes disk on which the file system is stored and data block size is 10^3 bytes, the maximum size of a file that can be stored on this disk in units of 10^6 bytes is _____.

Answer 5.4.25 Disks: GATE CSE 2015 Set 1 | Question: 48 [top](#)<https://gateoverflow.in/8354>

Consider a disk pack with a seek time of 4 milliseconds and rotational speed of 10000 rotations per minute (RPM). It has 600 sectors per track and each sector can store 512 bytes of data. Consider a file stored in the disk. The file contains 2000 sectors. Assume that every sector access necessitates a seek, and the average rotational latency for accessing each sector is half of the time for one complete rotation. The total time (in milliseconds) needed to read the entire file is _____.

Answer 5.4.26 Disks: GATE CSE 2015 Set 2 | Question: 49 [top](#)<https://gateoverflow.in/8251>

Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50×10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is _____.

Answer 



Consider a storage disk with 4 platters (numbered as 0, 1, 2 and 3), 200 cylinders (numbered as 0, 1, . . . , 199), and 256 sectors per track (numbered as 0, 1, . . . 255). The following 6 disk requests of the form [sector number, cylinder number, platter number] are received by the disk controller at the same time:

[120, 72, 2], [180, 134, 1], [60, 20, 0], [212, 86, 3], [56, 116, 2], [118, 16, 1]

Currently head is positioned at sector number 100 of cylinder 80, and is moving towards higher cylinder numbers. The average power dissipation in moving the head over 100 cylinders is 20 milliwatts and for reversing the direction of the head movement once is 15 milliwatts. Power dissipation associated with rotational latency and switching of head between different platters is negligible.

The total power consumption in milliwatts to satisfy all of the above disk requests using the Shortest Seek Time First disk scheduling algorithm is _____

gate2018-cse operating-system disks numerical-answers

Answer



In a computer system, four files of size 11050 bytes, 4990 bytes, 5170 bytes and 12640 bytes need to be stored. For storing these files on disk, we can use either 100 byte disk blocks or 200 byte disk blocks (but can't mix block sizes). For each block used to store a file, 4 bytes of bookkeeping information also needs to be stored on the disk. Thus, the total space used to store a file is the sum of the space taken to store the file and the space taken to store the book keeping information for the blocks allocated for storing the file. A disk block can store either bookkeeping information for a file or data from a file, but not both.

What is the total space required for storing the files using 100 byte disk blocks and 200 byte disk blocks respectively?

- A. 35400 and 35800 bytes
- B. 35800 and 35400 bytes
- C. 35600 and 35400 bytes
- D. 35400 and 35600 bytes

gate2005-it operating-system disks normal

Answer



A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

What is the total amount of data that can be stored on the disk if it is used with a drive that rotates it with

- I. Constant Linear Velocity
- II. Constant Angular Velocity?

- A. I. 80 MB; II. 2040 MB
- B. I. 2040 MB; II 80 MB
- C. I. 80 MB; II. 360 MB
- D. I. 360 MB; II. 80 MB

gate2005-it operating-system disks normal

Answer



A disk has 8 equidistant tracks. The diameters of the innermost and outermost tracks are 1 cm and 8 cm respectively. The innermost track has a storage capacity of 10 MB.

If the disk has 20 sectors per track and is currently at the end of the 5th sector of the inner-most track and the head can move at a speed of 10 meters/sec and it is rotating at constant angular velocity of 6000 RPM, how much time will it take to read 1 MB contiguous data starting from the sector 4 of the outer-most track?

- A. 13.5 ms
- B. 10 ms
- C. 9.5 ms
- D. 20 ms

Answer 5.4.31 Disks: GATE IT 2007 | Question: 44, ISRO2015-34 [top](#)<https://gateoverflow.in/3479>

A hard disk system has the following parameters :

- Number of tracks = 500
- Number of sectors/track = 100
- Number of bytes /sector = 500
- Time taken by the head to move from one track to adjacent track = 1 ms
- Rotation speed = 600 rpm.

What is the average time taken for transferring 250 bytes from the disk ?

- A. 300.5 ms
- B. 255.5 ms
- C. 255 ms
- D. 300 ms

Answer 

Answers: Disks

5.4.1 Disks: GATE CSE 1990 | Question: 7-c [top](#)<https://gateoverflow.in/85406>

✓

1. Avg Latency = $\frac{1}{2} \times \frac{60}{R} = \frac{1}{2} \times \frac{60}{3600} = 8.33$ ms
2. Disk Storage Capacity = (We need a number of surface to calculate it) 404×130030 Bytes $\simeq 50$ MB per surface (approx)
3. Data transfer rate = Track capacity $\times \frac{R}{60} = 130030 \times \frac{3600}{60} = 7801.8$ kBps

 16 votes

-- Lokesh Dafale (8.2k points)

5.4.2 Disks: GATE CSE 1993 | Question: 6.7 [top](#)<https://gateoverflow.in/2289>

✓

RPM = 2400

So, in 60 s, the disk rotates 2400 times.

Average latency is the time for half a rotation = $0.5 \times 60/2400$ s = $3/240$ s = 12.5 ms.

In one full rotation, entire data in a track can be transferred. Track storage capacity = 62500 bits.

So, disk transfer rate = $62500 \times 2400/60$ s = 2.5×10^6 bps.

 62 votes

-- Arjun Suresh (332k points)

5.4.3 Disks: GATE CSE 1993 | Question: 7.8 [top](#)<https://gateoverflow.in/2296>

✓

File system uses directories which are the files containing the name and location of other file in the file system. Unlike other file, directory does not store the user data. Directories are the file that can point to other directories. Root directory point to various user directory. So they will be stored in such a way that user cannot easily modify them. They should be placed at fixed location on the disk.

Correct Answer: B

 39 votes

-- neha pawar (3.3k points)

✓ **For (A) part :**

No of track = Recording width/ inner space between track

$$\text{Recording width} = (\text{Outer Diameter} - \text{Inner Diameter})/2 = (12 - 4)/2 = 4 \text{ cm}$$

Therefore no. of track = $4 \text{ cm}/0.1 \text{ mm} = 400 \text{ track}$

Since they have ask capacity of unformatted disk , so no 96 bytes in 4000 bytes would be wasted for non data purpose

Whole 4000 is used

$$\text{So, total capacity} = 400 \times 8 \times 20 \times 4000 = 256 \times 10^6 \text{ Bytes} = \mathbf{256 \text{ MB}}$$

For (B) part :

Its is given 360 rotations in 60 seconds

That is 360 rotations = 60 sec

Therefore, 1 rotations will take $(1/6)$ sec

$$\text{In } (1/6) \text{ sec - we can read one track} = 20 \times (4000 - 96) B = 20 \times 3904 B$$

Then, in 1 sec it will be = $20 \times 3904 \times 6$ bytes = Data transfer rate = **468.480 KBps** (when we consider 1 Read/Write Head for all surface).

If we consider **1 Read/Write Heads per surface (which is default approach)**, then **number of surfaces = 8**

$$\text{Data transfer rate} = (468.480 \times 8) \text{ KBps} = 3747.84 \text{ KBps}$$

But for our convenience we consider only 1 surface, it reads from one surface at a time. As data transfer rate is measured wrt a single surface only .

Hence, for part B, the correct answer is **468.480 KBps**.

👍 40 votes

-- spriti1991 (1.5k points)



✓

a. Maximum possible number of files:

As per question, 32 bits (or 4 Bytes) are required per file. And there is only one block to store this, ie the Disk block 1, which is of size 4KB. So number of files possible is $4 \text{ KB}/4 \text{ Bytes} = 1 \text{ K}$ files possible.

b. Max file size:

As per question the Disk Block Address (FAT entry gives DBA) is of 8 bits. So, ideally the max file size should be $2^8 = 256$ Block size.. But question makes it clear that two blocks, DB0 and DB1, stores control information. So, effectively we have $256 - 2 = 254$ blocks with us and the max file size should be = $254 \times$ size of one block = $254 \times 4 \text{ KB} = 1016 \text{ KB}$.

👍 32 votes

-- Hunaif (575 points)



✓

- 1000 consecutive records
- Size of 1 record = 3200 Bytes
- Access Time of device $D = 10 \text{ ms}$
- Data Transfer Rate of device $D = 800 * 10^3$ Bytes per second.
- CPU time to process Each record = 3ms.
- Time to transfer 1 record (3200 Bytes) = $\frac{3200 \text{ Bytes}}{800 * 10^3} = 4 \text{ ms}$

(A) Unblocked records with No buffer. Hence, each time only when a record is fetched in its full entirety it will be processed.

Time to fetch = Access Time for D (Every time you'll access the device. This is also known as device latency) + (Data transfer time)

$$= 10\text{ms} + 4\text{ms} = 14\text{ms}$$

$$\text{Total time taken by CPU for each record} = \text{fetch} + \text{execute} = 14\text{ms} + 3\text{ms} = 17\text{ms}$$

Total time for program $p = 1000 * 17\text{ms} = 17\text{sec}$

(B) Unblocked records and

1 buffer. Records will be accessed one by one and for each record fetched into the buffer, the device delay has to be taken into account.

Time to bring one record into buffer = $10 + 4 = 14$ ms.

Now let us see how the program goes.

- At $t = 0\text{ms}$, the program starts and the buffer is empty.
- At $t = 14\text{ms}$, R_1 fetched into the buffer and CPU starts processing it.
- At $t = 17\text{ms}$, cpu has processed R_1 and waiting for more records.
- At $t = 28\text{ms}$, buffer gets filled with R_2 and CPU starts processing it.

To get the Total time of the program we think in terms of the last record because when it is processed, all others would already have been processed too!

Last record R_{1000} would be fetched at $t = 0 + 14 * 1000 = 14000$ ms and 3ms will be taken by CPU to process this.

So, total elapsed time of program $P = 14000 + 3 = 14003\text{ms} = 14.003\text{sec}$

**(C) Each disk block contains
2 records and Assuming buffer can hold
1 disk block at a time.**

So, 1 Block Size = $2 * 3200 = 6400$ Bytes

Time to read a block = $\frac{6400}{800 * 10^3} = 8\text{ms}$.

Each block read you have to incur the device access cost.

So, the total time to fetch one block and bring it into buffer = $10 + 8 = 18$ ms.

We have 1000 files and so we need to read in 500 blocks.

Each block has two records and therefore CPU time per block = 6ms.

Again to count the program time P , we think in terms of the last Block.

Last block would be fetched at $t = 0 + (18 * 500) = 9000$ ms.

After this 6 ms more to process 2 records present in the 500th block.

So, program time $P = 9000 + 6 = 9006\text{ms} = 9.006\text{sec}$.

👍 35 votes

-- Ayush Upadhyaya (28.4k points)

5.4.7 Disks: GATE CSE 1998 | Question: 2-9 [top](#)

<https://gateoverflow.in/1681>



✓ Answer is (D) .

! The formatted disk capacity is always less than the "raw" unformatted capacity specified by the disk's manufacturer, because some portion of each track is used for sector identification and for gaps (empty spaces) between sectors and at the end of the track.

Reference : https://en.wikipedia.org/wiki/Floppy_disk_format

References



👍 33 votes

-- Akash Kanase (36k points)

5.4.8 Disks: GATE CSE 1998 | Question: 25-a [top](#)

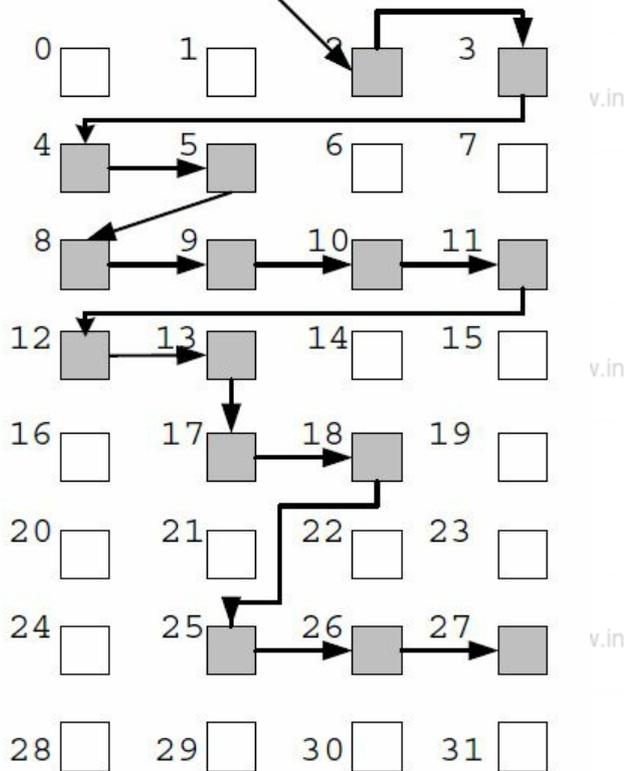
<https://gateoverflow.in/1740>



✓ Bit map maintains one bit for each block, If it is free then bit will be "0" if occupied then bit will be "1".
For space purpose, it doesn't matter what bit we are using, only matters that how many blocks are there.
For B blocks, Bit map takes space of " B " bits.

Free list is a list that maintains addresses of free blocks only. If we have 3 free blocks then it maintains 3 addresses in a list, if 4 free blocks then 4 address in a list and like that.

free-space list head



Given that we have F free blocks, therefore F addresses in a list, and each address size is d bits therefore Free list takes space of " Fd ".

condition under which the free list uses less space than the bit map: $Fd < B$

45 votes

-- Sachin Mittal (15.8k points)

5.4.9 Disks: GATE CSE 1998 | Question: 25b [top](#)

<https://gateoverflow.in/41055>



GIVEN: Consider a disk with c cylinders, t tracks per cylinder, s sectors per track

from this, we can conclude that 1 cylinder contains = $t*s$ sectors

and one track contains = s sectors

now we have to drive the formula of logical address n

so the cylinder no is $\lfloor \frac{n}{ts} \rfloor$

and track number will be floor of $((n \% ts) / s)$

and sector no will be $n \% s$

8 votes

-- Gurdeep (6.8k points)

5.4.10 Disks: GATE CSE 1999 | Question: 2-18, ISRO2008-46 [top](#)

<https://gateoverflow.in/1496>



✓

- A. Fault tolerance and
- B. High Speed

21 votes

-- GateMaster Prime (1.2k points)



- ✓ A disk driver is a device driver that allows a specific disk drive to communicate with the remainder of the computer. A good example of this driver is a floppy disk driver.

👍 32 votes

-- Bhagirathi Nayak (11.7k points)



- ✓ **Answer for (A):**

We are using SCAN - Elevator algorithms.

We will need to go from 25 → 99 → 5. (As we will move up all the way to 99, servicing all request, then come back to 5.)

So, total seeks = 74 + 94 = 168

Total time = 168 × 0.2 = 33.60000

- Answer for (B):**

We need to consider rotational latency too →

3000 rpm

I.e. 50 rps

$1 r = 1000/50 \text{ msec} = 20 \text{ msec}$

So, rotational latency = 20/2 = 10 msec per access.

In worst case we need to go from tracks 0 – 99. I.e. 99 seeks

Total time = 99 × 0.2 + 10 × 100 = 1019.8 msec = 1.019 sec

👍 36 votes

-- Akash Kanase (36k points)



- ✓ (a) $20 \times 1000 \times 16 \times 1KB = 3,20,000KB$

(b)

3000 rotations = 60 seconds

1 rotation = $\frac{60}{3000}$ seconds

1 rotation = 1 track = $\frac{1}{50}$ seconds

1 track = $16 \times 1KB = \frac{1}{50}$ seconds

800KB = 1 second

Hence, transfer rate = 800KB/s

(c) Data is transferred byte-wise; given in the question. gateoverflow.in

CPU read/write time for a byte = 0.1μs

Interrupt overhead (counted in CPU utilization time only) = 0.4μs

Transfer time for 1 byte data which took place at the rate of 800 KB/s = 1.25μs

Percentage of CPU time required for this job = $\frac{0.1 + 0.4}{0.4 + 0.1 + 1.25} \times 100 = 28.57\%$

(d) Percentage of CPU time held up for disk I/O for cycle stealing DMA transfer = $\frac{0.1 + 0}{1.25} \times 100 = 8.00\%$

👍 30 votes

-- Amar Vashishth (25.2k points)



- ✓ Answer is (A). Larger block size means less number of blocks to fetch and hence better throughput. But larger block size also means space is wasted when only small size is required.

👍 63 votes

-- Arjun Suresh (332k points)



- ✓ Size of Disk Block = 1024 Byte

Disk Blocks address = $4B$

No. of addresses per block $1024/4 = 256 = 2^8$ addresses

We have:

10 Direct

1 $SI = 2^8 \text{Indirect} \times 2^{10} = 2^{18} \text{Byte}$

1 $DI = 2^8 \text{SI} = (2^8)^2 \text{Direct} = 2^{16} \text{Direct} * * 2^{10} = 2^{26} \text{Byte}$

1 $TI = 2^8 \text{DI} = (2^8)^2 \text{SI} = (2^8)^3 = 2^{24} \text{Direct} = 2^{24} \times 2^{10} = 2^{34} \text{Byte.}$

So, total size = $2^{18} + 2^{26} + 2^{34} \text{ Byte} + 10240 \text{Byte}$. Which is nearly 2^{34} Bytes . (We don't have exact option available. Choose approximate one)

Answer \rightarrow (C)

👍 43 votes

-- Akash Kanase (36k points)



- ✓ Swap space(on the disk) is used by Operating System to store the pages that are swapped out of the memory due to less memory available on the disk. Interestingly the Android Operating System, which is Linux kernel under the hood has the swapping disabled and has its own way of handling "low memory" situations.

Pages are basically Process data, hence the answer is (B).

👍 30 votes

-- Sandeep Kumar (संदीप कुमार) (2.2k points)



- ✓ Answer is (A).

16 surfaces = 4 bits, 128 tracks = 7 bits, 256 sectors = 8 bits, sector size 512 bytes = 9 bits

Capacity of disk = $2^{4+7+8+9} = 2^{28} = 256 \text{ MB}$

To specify a particular sector we do not need sector size, so bits required = $4 + 7 + 8 = 19$

👍 38 votes

-- jayendra (6.7k points)



- ✓ The answer is B, because due to Inertia

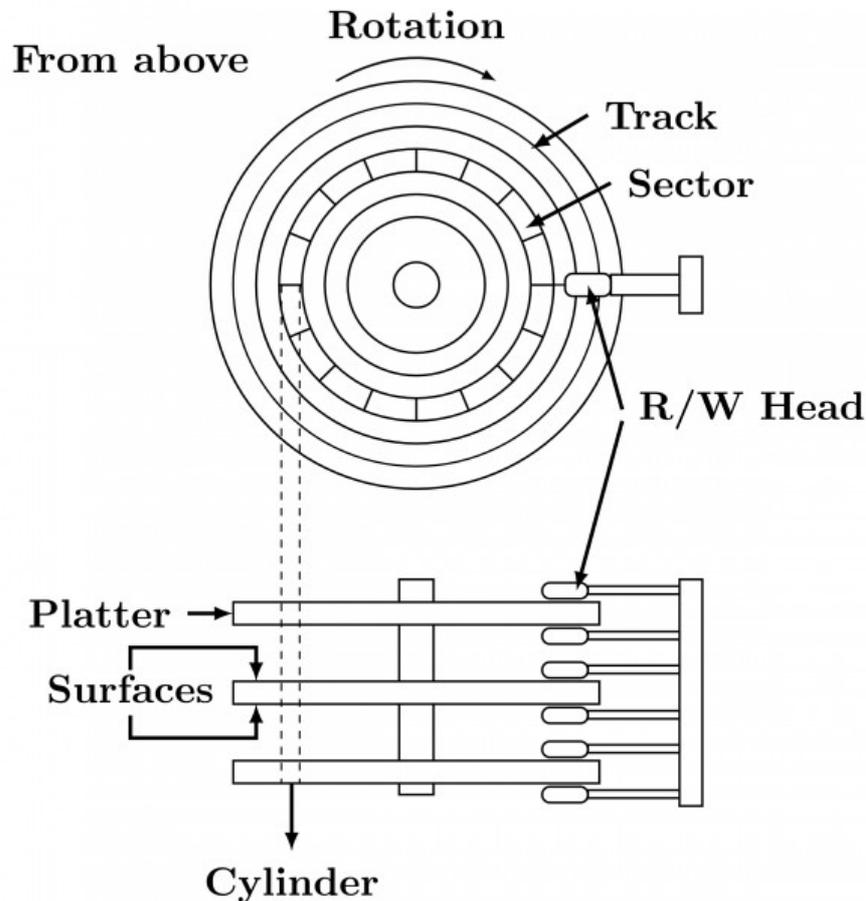
Whenever your read-write head moves from 1 track to another track, it has to face resistance due to change in state of motion including speed and direction, which is nothing but inertia. Hence the answer is B

👍 31 votes

-- spriti1991 (1.5k points)



- ✓ The data on a disk is ordered in the following way. It is first stored on the first sector of the first surface of the first cylinder. Then in the next sector, and next, until all the sectors on the first track are exhausted. Then it moves on to the first sector of the second surface (remains at the same cylinder), then next sector and so on. It exhausts all available surfaces for the first cylinder in this way. After that, it moves on to repeat the process for the next cylinder.



So, to reach to the cylinder numbered 400 (401^{th} cylinder) we need to skip $400 \times (10 \times 2) \times 63 = 504,000$ sectors.

Then, to skip to the 16^{th} surface of the cylinder numbered 400, we need to skip another $16 \times 63 = 1,008$ sectors.

Finally, to find the 29 sector, we need to move another 29 sectors.

In total, we moved $504,000 + 1,008 + 29 = 505,037$ sectors.

Hence, the answer to 51 is option (C).

👍 95 votes

-- Pragy Agarwal (18.3k points)



- ✓ 1039^{th} sector will be stored in track number $(1039 + 1)/63 = 16.5$ (as counting starts from 0 as given in question) and each track has 63 sectors. So, we need to go to 17^{th} track which will be numbered 16 and each cylinder has 20 tracks (10 platters \times 2 recording surface each). Number of extra sectors needed = $1040 - 16 \times 63 = 32$ and hence the sector number will be 31. So, option (C).

👍 47 votes

-- Pragy Agarwal (18.3k points)



- ✓ Disk access time = Seek time + Rotational latency + Transfer time (given that transfer time is neglected)
 Seek time = 10 ms
 Rotational speed = 6000 rpm

- $60\text{ s} \rightarrow 6000\text{ rotations}$
- $1\text{ rotation} \rightarrow 60/6000\text{ s}$
- $\text{Rotational latency} = 1/2 \times 60/6000\text{ s} = 5\text{ ms}$

Total time to transfer one library = $10 + 5 = 15\text{ ms}$
 \therefore Total time to transfer 100 libraries = $100 \times 15\text{ ms} = 1.5\text{ s}$

Correct Answer: *B*

👍 65 votes

-- neha pawar (3.3k points)

5.4.22 Disks: GATE CSE 2012 | Question: 41 [top](#)

<https://gateoverflow.in/2149>



- ✓ Direct block addressing will point to 8 disk blocks = $8 \times 128\text{ B} = 1\text{ KB}$

Singly Indirect block addressing will point to 1 disk block which has $128/8$ disc block addresses = $(128/8) \times 128\text{ B} = 2\text{ KB}$

Doubly indirect block addressing will point to 1 disk block which has $128/8$ addresses to disk blocks which in turn has $128/8$ addresses to disk blocks = $16 \times 16 \times 128\text{ B} = 32\text{ KB}$

Total = 35 KB

Answer is **(B)**

👍 61 votes

-- Vikrant Singh (11.2k points)

5.4.23 Disks: GATE CSE 2013 | Question: 29 [top](#)

<https://gateoverflow.in/1540>



- ✓ First convert $\langle 1200, 9, 40 \rangle$ into sector address.

$$(1200 \times 16 \times 64) + (9 \times 64) + 40 = 1229416$$

$$\text{Number of sectors to store file} = (42797\text{ KB})/512 = 85594$$

$$\text{Last sector to store file} = 1229416 + 85594 = 1315010$$

Now, do reverse engineering,

$$1315010/(16 \times 64) = 1284.189453 \text{ (1284 will be cylinder number and remaining sectors} = 194)$$

$$194/64 = 3.03125 \text{ (3 is surface number and remaining sectors are 2)}$$

$\therefore \langle 1284, 3, 1 \rangle$ is last sector address.

Correct Answer: *D*

👍 210 votes

-- Laxmi (793 points)

$42797\text{ KB} = 42797 \times 1024\text{ bytes}$ require $42797 \times 1024/512$ sectors = 85594 sectors.

$\langle 1200, 9, 40 \rangle$ is the starting address. So, we can have 24 sectors in this recording surface. Remaining 85570 sectors.

85570 sectors require $\lceil \frac{85570}{64} \rceil = 1338$ recording surfaces. We start with recording surface 9, so we can have 7 more in the given cylinder. So, we have $1338 - 7 = 1331$ recording surfaces left.

In a cylinder, we have 16 recording surfaces. So, 1331 recording surfaces require $\lceil \frac{1331}{16} \rceil = 84$ different cylinders.

The first cylinder (after the current one) starts at 1201. So, the last one should be 1284.

$\langle 1284, 3, 1 \rangle$ will be the end address. $(1331 - 16 \times 83 + 1 - 1 = 3)$ (3 surfaces full and 1 partial and -1 since address starts from 0), and $85570 - 1337 \times 64 - 1 = 1$

👍 37 votes

-- Arjun Suresh (332k points)



- ✓ Each datablock will have its entry.

$$\text{So, Total Number of entries in the FAT} = \frac{\text{Disk Capacity}}{\text{Block size}} = \frac{100MB}{1KB} = 100K$$

Each entry takes up $4B$ as overhead

$$\text{So, space occupied by overhead} = 100K \times 4B = 400KB = 0.4MB$$

We have to give space to Overheads on the same file system and at the rest available space we can store data.

$$\text{So, assuming that we use all available storage space to store a single file} = \text{Maximum file size} = \\ \text{Total File System size} - \text{Overhead} = 100MB - 0.4MB = 99.6MB$$

👍 88 votes

-- Kalpish Singhal (1.6k points)



- ✓ Since each sector requires a seek,

$$\text{Total time} = 2000 \text{ (seek time + avg. rotational latency + data transfer time)}$$

Since data transfer rate is not given, we can take that in 1 rotation, all data in a track is read. i.e., in $60/10000 = 6$ ms, 600×512 bytes are read. So, time to read 512 bytes = $6/600$ ms = 0.01 ms

$$= 2000 \times (4 \text{ ms} + 60 \times 1000/2 \times 10000 + 0.01)$$

$$= 2000 \times (7.01 \text{ ms})$$

$$= 14020 \text{ ms.}$$

<http://www.csee.umbc.edu/~olano/611s06/storage-io.pdf>

References



👍 69 votes

-- Arjun Suresh (332k points)



- ✓ Average time to read/write = Avg. seek time + Avg. rotational delay + Effective transfer time

$$\text{Rotational delay} = \frac{60}{15} = 4 \text{ ms}$$

$$\text{Avg. rotational delay} = \frac{1}{2} \times 4 = 2 \text{ ms}$$

$$\text{Avg. seek time} = 2 \times 2 = 4 \text{ ms}$$

$$\text{Disk transfer time} = \frac{512 \text{ Bytes}}{50 \times 10^6 \text{ Bytes/sec}} = 0.0102 \text{ ms}$$

$$\text{Effective transfer time} = 10 \times \text{disk transfer time} = 0.102 \text{ ms}$$

$$\text{So, avg. time to read/write} = 4 + 2 + 0.0102 + 0.102 = 6.11 \text{ ms} \approx \mathbf{6.1 \text{ ms}}$$

Reference: <http://www.csc.villanova.edu/~japaridz/8400/sld012.htm>

References



👍 74 votes

-- Arjun Suresh (332k points)

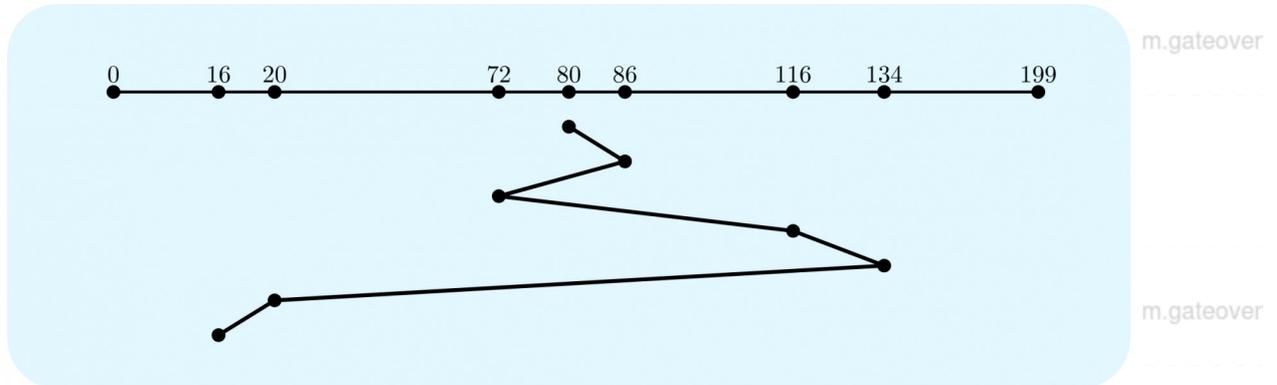


- ✓ Shortest Seek Time First (SSTF), selects the request with minimum to seek time first from the current head position.

In the given question disk requests are given in the form of $\langle \text{sectorNo, cylinderNo, platterNo} \rangle$.

Cylinder Queue : 72, 134, 20, 86, 116, 16

Head starts at : 80



Shortest seek time first(SSTF)

Total head movements in SSTF = $(86 - 80) + (86 - 72) + (134 - 72) + (134 - 16) = 200$

- Power dissipated in moving 100 cylinder = 20 mW
- Power dissipated by 200 movements (say P_1) = $0.2 * 200 = 40$ mW
- Power dissipated in reversing head direction once = 15 mW
- Number of times head changes its direction = 3
- Power dissipated in reversing head direction (say P_2) = $3 * 15 = 45$ mW

Total Power Consumption is $P_1 + P_2 = 85$ mW

Hence, 85 mW is the correct answer.

👍 48 votes

-- Ashwani Kumar (13k points)



- ✓ for 100 bytes block:

$11050 = 111$ blocks requiring $111 \times 4 = 444$ bytes of bookkeeping info which requires another 5 disk blocks. So, totally

$111 + 5 = 116$ disk blocks. Similarly,

$4990 = 50 + (50 \times 4)/100 = 52$

$5170 = 52 + (52 \times 4)/100 = 55$

$12640 = 127 + (127 \times 4/100) = 133$

 $356 \times 100 = 35600$ bytes

For 200 bytes block:

$56 + (56 \times 4/200) = 58$

$25 + (25 \times 4/200) = 26$

$26 + (26 \times 4/200) = 27$

$64 + (64 \times 4/200) = 66$

 $177 \times 200 = 35400$

So, (C) option.

👍 48 votes

-- Viral Kapoor (1.9k points)



- ✓ • With **Constant Linear Velocity, CLV**, the density of bits is uniform from cylinder to cylinder. Because there are more sectors in outer cylinders, the disk spins slower when reading those cylinders, causing the rate of bits passing under the read-write head to remain constant. This is the approach used by modern CDs and DVDs.
- With **Constant Angular Velocity, CAV**, the disk rotates at a constant angular speed, with the bit density decreasing on outer cylinders. (These disks would have a constant number of sectors per track on all cylinders.)
- $CLV = 10 + 20 + 30 + 40 + \dots = 360$
- $CAV = 10 \times 8 = 80$ so answer should be (D)

Edit:- for CLV disk capacity

let track diameters like 1cm, 2cm... 8cm.

As described that density is uniform.

So all tracks has equal storage density.

Track capacity = storage density \times circumference ($2 \times \pi \times r$)

For 1st track. $10MB = \text{density} \times 2 \times \pi \times 1$

Density = $10/\pi$. MB/cm

For 2nd track capacity = density \times circumference

= $(10/\pi) \times (\pi \times 2)MB = 20MB$

Now each track capacity can be calculated and added for disk capacity

👍 72 votes

-- spriti1991 (1.5k points)

5.4.30 Disks: GATE IT 2005 | Question: 81-b [top](#)

<https://gateoverflow.in/3846>



- ✓ Total Time = Seek + Rotation + Transfer.

Seek Time :

Current Track 1

Destination Track 8

Distance Required to travel = $4 - 0.5 = 3.5 \text{ Cm}$

Time required = $10 \text{ m/s} = 1 \text{ Cm/ms} = 3.5 \text{ ms}$ [Time= Distance / Speed]

Rotation Time:

6000 RPM in 60 sec

100 RPS in 1 sec

1 Revolution in 10 ms

1 Revolution = Covering entire Track

1 Track = 20 sector

1 sector required = $10/20 = 0.5 \text{ ms}$

Disk is constantly Rotating so when head moved from inner most track to outer most track total movement of disk

= $(3.5/0.5) = 7$ sectors

Which means that when disk reached outer most track head was at end of 12th sector

Total Rotational Delay = Time required to go from end of 12 to end of 3 = 11 sectors

1 sector = 0.5 ms so 11 sector = **5.5ms**

Transfer Time

Total Data in Outer most track = 10 MB

Data in single Sector = $10 \text{ MB}/20 = 0.5 \text{ MB}$

Data required to read = 1 MB = 2 sector

Time required to read data = $2 \times 0.5 = 1 \text{ ms}$

Total Time = Seek + Rotation + Transfer = 3.5ms + 5.5ms + 1ms = 10 ms

Correct Answer: B

👍 95 votes

-- Keval Malde (13.3k points)

✓ **option (D)**

Explanation

Avg. time to transfer = Avg. seek time + Avg. rotational delay + Data transfer time

Avg Seek Time

given that : time to move between successive tracks is 1 ms

time to move from track 1 to track 1 : 0ms

time to move from track 1 to track 2 : 1ms

time to move from track 1 to track 3 : 2ms

..

..

time to move from track 1 to track 500 : 499ms

$$\text{Avg Seek time} = \frac{\sum 0+1+2+3+\dots+499}{500}$$

$$= \mathbf{249.5 \text{ ms}}$$

Avg Rotational Delay

RMP : 600

600 rotations in 60 sec

one Rotation takes 60/600 sec = 0.1 sec

Avg Rotational Delay = $\frac{0.1}{2}$ { usually $\frac{\text{Rotation time}}{2}$ is taken as Avg Roational Delay }

$$= .05 \text{ sec}$$

$$= \mathbf{50 \text{ ms}}$$

Data Transfer Time

One 1 Roatation we can read data on one complete track .

$$= 100 \times 500 = 50,000 \text{ B data is read in one complete rotation}$$

one complete rotation takes 0.1 s (we seen above)

0.1 → 50,000 bytes.

$$250 \text{ bytes} \rightarrow 0.1 \times 250/50,000 = \mathbf{0.5 \text{ ms}}$$

Avg. time to transfer= **Avg. seek time**+ **Avg. rotational delay**+ **Data transfer time**

$$= \mathbf{249.5 + 50 + 0.5}$$

$$= \mathbf{300 \text{ ms}}$$

 161 votes

-- Akhil Nadh PC (16.5k points)

5.5

File System (6) top 

In the index allocation scheme of blocks to a file, the maximum possible size of the file depends on

- the size of the blocks, and the size of the address of the blocks.
- the number of blocks used for the index, and the size of the blocks.
- the size of the blocks, the number of blocks used for the index, and the size of the address of the blocks.
- None of the above

gate2002-cse operating-system normal file-system

Answer 



The data blocks of a very large file in the Unix file system are allocated using

- A. continuous allocation
- B. linked allocation
- C. indexed allocation
- D. an extension of indexed allocation

gate2008-cse file-system operating-system normal

Answer



In a file allocation system, which of the following allocation scheme(s) can be used if no external fragmentation is allowed ?

1. Contiguous
2. Linked
3. Indexed

- A. 1 and 3 only
- B. 2 only
- C. 3 only
- D. 2 and 3 only

gate2017-cse-set2 operating-system file-system normal

Answer



The index node (inode) of a Unix-like file system has 12 direct, one single-indirect and one double-indirect pointers. The disk block size is 4 kB, and the disk block address is 32-bits long. The maximum possible file size is (rounded off to 1 decimal place) _____ GB

gate2019-cse numerical-answers operating-system file-system

Answer



Consider a linear list based directory implementation in a file system. Each directory is a list of nodes, where each node contains the file name along with the file metadata, such as the list of pointers to the data blocks. Consider a given directory `foo`.

Which of the following operations will necessarily require a full scan of `foo` for successful completion?

- A. Creation of a new file in `foo`
- B. Deletion of an existing file from `foo`
- C. Renaming of an existing file in `foo`
- D. Opening of an existing file in `foo`

gate2021-cse-set1 multiple-selects operating-system file-system

Answer



In a particular Unix OS, each data block is of size 1024 bytes, each node has 10 direct data block addresses and three additional addresses: one for single indirect block, one for double indirect block and one for triple indirect block. Also, each block can contain addresses for 128 blocks. Which one of the following is approximately the maximum size of a file in the file system?

- A. 512 MB
- B. 2 GB
- C. 8 GB
- D. 16 GB

Answers: File System

5.5.1 File System: GATE CSE 2002 | Question: 2.22 [top](#) <https://gateoverflow.in/852>

- ✓ In Index allocation size of maximum file can be derived like following:

No of addressable blocks using one Index block (A) = Size of block / Size of block address

No of block addresses available for addressing one file (B) =

No of Maximum blocks we can use for the Index * No of addressable blocks using one Index block (A)

Size of File = B * Size of Block

So, it is clear that:

Answer is (C).

A & B are incomplete.

 49 votes

-- Akash Kanase (36k points)

5.5.2 File System: GATE CSE 2008 | Question: 20 [top](#) <https://gateoverflow.in/418>

- ✓ The data blocks of a very large file in the unix file system are allocated using an extension of indexed allocation or EXT2 file system. Hence, option (D) is the right answer.

 44 votes

-- Kalpna Bhargav (2.5k points)

5.5.3 File System: GATE CSE 2017 Set 2 | Question: 08 [top](#) <https://gateoverflow.in/118437>

- ✓ Both Linked and Indexed allocation free from external fragmentation

Refer:galvin

Reference: <https://webservices.ignou.ac.in/virtualcampus/adit/course/cst101/block4/unit4/cst101-b14-u4-06.htm>

References



 39 votes

-- Aboveallplayer (12.5k points)

5.5.4 File System: GATE CSE 2019 | Question: 42 [top](#) <https://gateoverflow.in/302806>

- ✓ Given 12 direct, 1 single indirect, 1 double indirect pointers

Size of Disk block = $4kB$

Disk Block Address = 32 bit = $4B$

Number of addresses= Size of disk block/address size = $\frac{4kB}{4B} = 2^{10}$

Maximum possible file size= $12 * 4kB + 2^{10} * 4kB + 2^{10} * 2^{10} * 4kB$

= $4.00395 GB \simeq 4 GB$

Hence $4GB$ is the correct answer
classroom.gateoverflow.in
20 votes

gateoverflow.in

classroom.gateover
-- Ashwani Kumar (13k points)

5.5.5 File System: GATE CSE 2021 Set 1 | Question: 15 top

https://gateoverflow.in/357437



✓ Correct Options: A, C

(Note: In the question it's given "which of the following options require a full scan of foo for successful completion". Meaning the best algorithm scans the list entirely for each type of input to verify the correctness of the procedure and ,can't partially scan and complete for any particular instance...)

Each File in Directory is uniquely referenced by its **name**. So **different files** must have **different names!**

So,

- A. **Creation of a New File:** For creating new file, we've to check whether the new name is same as the existing files. Hence, the linked list must be scanned in its entirety.
- B. **Deletion of an Existing File:** Deletion of a file doesn't give rise to name conflicts, hence if the node representing the files is found earlier, it can be deleted without a through scan.
- C. **Renaming a File:** Can give rise to name conflicts, same reason can be given as option A.
- D. **Opening of existing file:** same reason as option B.

4 votes

-- NIKHIL SHARMA (605 points)

5.5.6 File System: GATE IT 2004 | Question: 67 top

https://gateoverflow.in/3710



✓ Answer: (B)

Maximum file size = 10×1024 Bytes + $1 \times 128 \times 1024$ Bytes + $1 \times 128 \times 128 \times 1024$ Bytes
+ $1 \times 128 \times 128 \times 128 \times 1024$ Bytes = approx $2 GB$.

35 votes

-- Rajarshi Sarkar (27.9k points)

5.6

Fork (5) top

5.6.1 Fork: GATE CSE 2005 | Question: 72 top

https://gateoverflow.in/765



```
Consider the following code fragment:  
if (fork() == 0)  
{  
    a = a + 5;  
    printf("%d, %p n", a, &a);  
}  
else  
{  
    a = a - 5;  
    printf ("%d, %p n", a, &a);  
}
```

Let u, v be the values printed by the parent process and x, y be the values printed by the child process. Which one of the following is **TRUE**?

- A. $u = x + 10$ and $v = y$
- B. $u = x + 10$ and $v! = y$
- C. $u + 10 = x$ and $v = y$
- D. $u + 10 = x$ and $v! = y$

gate2005-cse operating-system fork normal

Answer



A process executes the following code

```
for(i=0; i<n; i++) fork();
```

The total number of child processes created is

- A. n
- B. $2^n - 1$
- C. 2^n
- D. $2^{n+1} - 1$

gate2008-cse

operating-system

fork

normal

Answer



A process executes the code

```
fork();
fork();
fork();
```

The total number of **child** processes created is

- A. 3
- B. 4
- C. 7
- D. 8

gate2012-cse

operating-system

easy

fork

Answer



The following C program is executed on a Unix/Linux system :

```
#include<unistd.h>
int main()
{
    int i;
    for(i=0; i<10; i++)
        if(i%2 == 0)
            fork();
    return 0;
}
```

The total number of child processes created is _____ .

gate2019-cse

numerical-answers

operating-system

fork

Answer



A process executes the following segment of code :

```
for(i = 1; i <= n; i++)
    fork ();
```

The number of new processes created is

- A. n
- B. $((n(n+1))/2)$
- C. $2^n - 1$
- D. $3^n - 1$

gate2004-it

operating-system

fork

easy

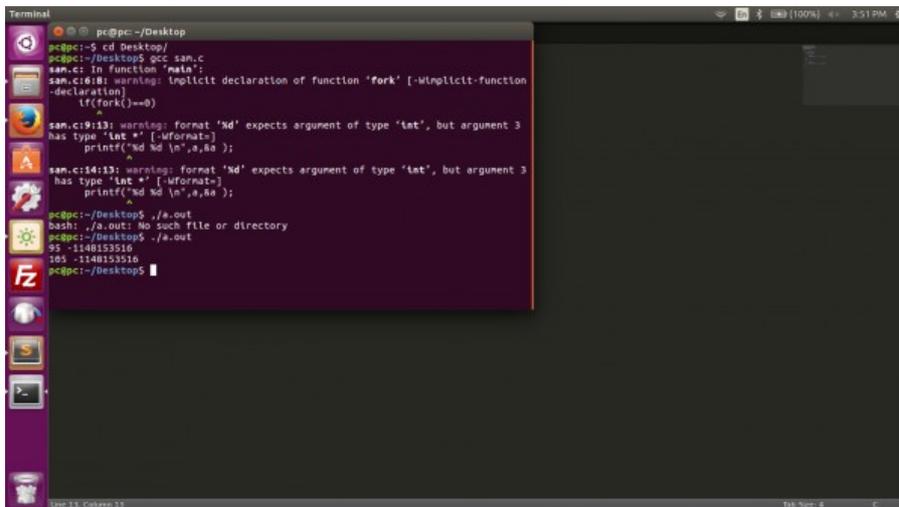
Answer



✓ It should be **Option C**.

```
#include<stdio.h>
#include<stdlib.h>
void main()
{
    int a =100;
    if(fork()==0)
    {
        a=a+5;
        printf("%d %d \n",a, &a );
    }
    else
    {
        a=a-5;
        printf("%d %d \n",a, &a );
    }
}
```

Output:



Fork returns 0 when it is a child process.

```
if ( fork == 0)
```

Is true when it is child . Child increment value of a .

In the above output:

- 95 is printed by parent : **u**
- 105 is printed by child : **x**
- ⇒ **u + 10 = x**

The logical addresses remains the same between the parent and child processes.

Hence, answer should be:

u + 10 = x and v = y

61 votes

-- Akhil Nadh PC (16.5k points)

(c) is the answer. Child is incrementing a by 5 and parent is decrementing a by 5. So, x = u + 10.

During fork(), address space of parent is copied for the child. So, any modifications to child variable won't affect the parent variable or vice-versa. But this copy is for physical pages of memory. The logical addresses remains the same between the parent and child processes.

27 votes

-- gatecse (63.3k points)



✓ Each fork() creates a child which start executing from that point onward. So, number of child processes created will be

$2^n - 1$.

At each fork, the number of processes doubles like from $1 - 2 - 4 - 8 \dots 2^n$. Of these except 1, all are child processes.

Reference: https://gateoverflow.in/3707/gate2004-it_64

References



34 votes

-- Arjun Suresh (332k points)

5.6.3 Fork: GATE CSE 2012 | Question: 8 top

<https://gateoverflow.in/40>



- ✓ At each fork() the no. of processes becomes doubled. So, after 3 fork calls, the total no. of processes will be 8. Out of this 1 is the parent process and 7 are child processes. So, total number of child processes created is 7.

42 votes

-- Arjun Suresh (332k points)

5.6.4 Fork: GATE CSE 2019 | Question: 17 top

<https://gateoverflow.in/302831>



- ✓ Answer is 31
Fork is called whenever i is even, so we can re-write the code as

```
for(i=0; i<10; i=i+2)
    fork();
```

fork() will be called 5 times ($i = 0, 2, 4, 6, 8$)

∴ Total number of process $2^5 = 32$

Total number of child process would be $2^5 - 1 = 31$

17 votes

-- Abhishek Shaw (1.1k points)

5.6.5 Fork: GATE IT 2004 | Question: 64 top

<https://gateoverflow.in/3707>



- ✓ Option (C).

At each fork, the number of processes doubles like from $1 - 2 - 4 - 8 \dots 2^n$. Of these except 1, all are child processes.

35 votes

-- prakash (237 points)

5.7

Inter Process Communication (1) top

5.7.1 Inter Process Communication: GATE CSE 1997 | Question: 3.7 top

<https://gateoverflow.in/2238>



I/O redirection

- A. implies changing the name of a file
- B. can be employed to use an existing file as input file for a program
- C. implies connecting 2 programs through a pipe
- D. None of the above

gate1997 operating-system normal inter-process-communication

Answer ⬇

Answers: Inter Process Communication



✓ Answer: (B)

Typically, the syntax of these characters is as follows, using < to redirect input, and > to redirect output.

```
command1 > file1
```

executes command1, placing the output in file1, as opposed to displaying it at the terminal, which is the usual destination for standard output. This will clobber any existing data in file1.

Using,

```
command1 < file1
```

executes command1, with file1 as the source of input, as opposed to the keyboard, which is the usual source for standard input.

```
command1 < infile > outfile
```

combines the two capabilities: command1 reads from infile and writes to outfile.

👍 35 votes

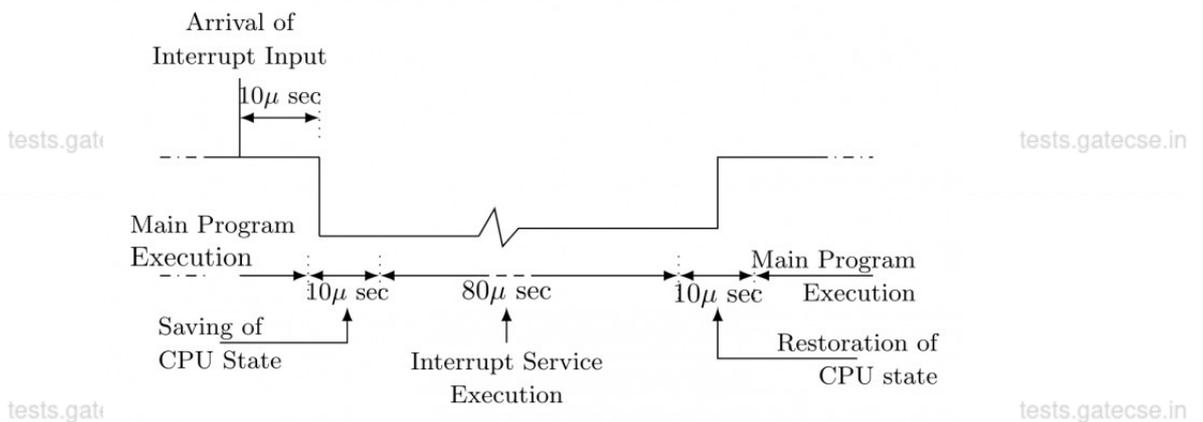
-- Rajarshi Sarkar (27.9k points)

5.8

Interrupts (8) [top](#)



The details of an interrupt cycle are shown in figure.



Given that an interrupt input arrives every 1 msec, what is the percentage of the total time that the CPU devotes for the main program execution.

gate1993 operating-system interrupts normal descriptive

Answer 🗣️



The correct matching for the following pairs is:

(A) Disk Scheduling	(1) Round robin
(B) Batch Processing	(2) SCAN
(C) Time-sharing	(3) LIFO
(D) Interrupt processing	(4) FIFO

- A. A-3 B-4 C-2 D-1
- B. A-4 B-3 C-2 D-1
- C. A-2 B-4 C-1 D-3
- D. A-3 B-4 C-3 D-2

Answer 5.8.3 Interrupts: GATE CSE 1997 | Question: 3.8 [top](#)<https://gateoverflow.in/2239>

When an interrupt occurs, an operating system

- A. ignores the interrupt
- B. always changes state of interrupted process after processing the interrupt
- C. always resumes execution of interrupted process after processing the interrupt
- D. may change state of interrupted process to 'blocked' and schedule another process.

gate1997 operating-system interrupts normal

Answer 5.8.4 Interrupts: GATE CSE 1998 | Question: 1.18 [top](#)<https://gateoverflow.in/1656>

Which of the following devices should get higher priority in assigning interrupts?

- A. Hard disk
- B. Printer
- C. Keyboard
- D. Floppy disk

gate1998 operating-system interrupts normal

Answer 5.8.5 Interrupts: GATE CSE 1999 | Question: 1.9 [top](#)<https://gateoverflow.in/1462>

Listed below are some operating system abstractions (in the left column) and the hardware components (in the right column)

(A)	Thread	1.	Interrupt
(B)	Virtual address space	2.	Memory
(C)	File system	3.	CPU
(D)	Signal	4.	Disk

- A. (A) – 2 (B) – 4 (C) – 3 (D) – 1
- B. (A) – 1 (B) – 2 (C) – 3 (D) – 4
- C. (A) – 3 (B) – 2 (C) – 4 (D) – 1
- D. (A) – 4 (B) – 1 (C) – 2 (D) – 3

gate1999 operating-system easy interrupts virtual-memory disks

Answer 5.8.6 Interrupts: GATE CSE 2001 | Question: 1.12 [top](#)<https://gateoverflow.in/705>

A processor needs software interrupt to

- A. test the interrupt system of the processor
- B. implement co-routines
- C. obtain system services which need execution of privileged instructions
- D. return from subroutine

gate2001-cse operating-system interrupts easy

Answer 



A computer handles several interrupt sources of which of the following are relevant for this question.

- Interrupt from CPU temperature sensor (raises interrupt if CPU temperature is too high)
- Interrupt from Mouse (raises Interrupt if the mouse is moved or a button is pressed)
- Interrupt from Keyboard (raises Interrupt if a key is pressed or released)
- Interrupt from Hard Disk (raises Interrupt when a disk read is completed)

Which one of these will be handled at the **HIGHEST** priority?

- Interrupt from Hard Disk
- Interrupt from Mouse
- Interrupt from Keyboard
- Interrupt from CPU temperature sensor

gate2011-cse

operating-system

interrupts

normal

Answer



The following are some events that occur after a device controller issues an interrupt while process L is under execution.

- P. The processor pushes the process status of L onto the control stack
- Q. The processor finishes the execution of the current instruction
- R. The processor executes the interrupt service routine
- S. The processor pops the process status of L from the control stack
- T. The processor loads the new PC value based on the interrupt

Which of the following is the correct order in which the events above occur?

- QPTRS
- PTRSQ
- TRPQS
- QTPRS

gate2018-cse

operating-system

interrupts

normal

Answer

Answers: Interrupts



- ✓ Time to service an interrupt = saving of cpu state + ISR execution + restoring of CPU state
= $(80 + 10 + 10) \times 10^{-6} = 100$ **microseconds**

For every 1 ms an interrupt occurs which is served for 100 microseconds

1 ms \rightarrow 1000 microseconds

After every 1000 microseconds of main code execution, 100 microseconds for interrupt overhead exists.

Thus, for every 1000 microseconds, $(1000 - 100) = 900$ microseconds of main program and 100 microseconds of interrupt overhead exists.

Thus, 900/1000 is usage of CPU to execute main program

% of CPU time used to execute main program is $(900/1000) \times 100 = 90.00\%$.

29 votes

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-- Surabhi Kador (819 points)



- ✓ (C) is answer. Interrupt processing is LIFO because when we are processing an interrupt, we disable the interrupts originating from lower priority devices so lower priority interrupts can not be raised. If an interrupt is detected then it means that it has higher priority than currently executing interrupt so this new interrupt will preempt the current interrupt so, LIFO. Other

matches are easy

44 votes

-- ashish gusai (523 points)

5.8.3 Interrupts: GATE CSE 1997 | Question: 3.8 top 5

https://gateoverflow.in/2239



✓ Think about this:
When a process is running and after time slot is over, who schedules new process?
- Scheduler.

But to run "scheduler" itself, we have to first schedule scheduler.
This is catch here, We need hardware support to schedule scheduler. That is hardware timer. When timer expires, then hardware generates interrupt and scheduler gets schedule.
Now after servicing that interrupt, scheduler may schedule another process.

This was about Hardware interrupt.

Now think if user invokes a system call, System call in effect leads to interrupt, and after this interrupt CPU resumes execution of current running process.

Conclusion: Its about type of interrupt being serviced.
Options with "always" are false.

Hence, option (D).

78 votes

-- Sachin Mittal (15.8k points)

5.8.4 Interrupts: GATE CSE 1998 | Question: 1.18 top 5

https://gateoverflow.in/1655



✓ It should be a Hard disk. I don't think there is a rule like that. But hard disk makes sense compared to others here.

<http://www.ibm1130.net/functional/IOInterrupts.html>

References



33 votes

-- Arjun Suresh (332k points)

5.8.5 Interrupts: GATE CSE 1999 | Question: 1.9 top 5

https://gateoverflow.in/1462



✓ Answer: (C) A - 3, B - 2, C - 4, D - 1

(A)	Thread	3.	CPU
(B)	Virtual address space	2.	Memory
(C)	File system	4.	Disk
(D)	Signal	1.	Interrupt

Why?

- Thread & Process are handled by CPU.
- Virtual Address Space is a type of memory address.
- File System is used for disk management.
- Interrupt is a type of signal from Hardware/Software source.

29 votes

-- Siddharth Mahapatra (1.2k points)

5.8.6 Interrupts: GATE CSE 2001 | Question: 1.12 top 5

https://gateoverflow.in/705



✓ Answer is (C).

(A) and (B) are obviously incorrect. In (D) no need to change mode while returning from any subroutine. therefore software interrupt is not needed for that. But in (C) to execute any privileged instruction processor needs software interrupt while changing mode.

👍 37 votes

-- jayendra (6.7k points)

5.8.7 Interrupts: GATE CSE 2011 | Question: 11 [top](#)

<https://gateoverflow.in/2113>



✓ Answer should be (D) Higher priority interrupt levels are assigned to requests which, if delayed or interrupted, could have serious consequences. Devices with high speed transfer such as magnetic disks are given high priority, and slow devices such as keyboard receive low priority. We know that mouse pointer movements are more frequent than keyboard ticks. So its obvious that its data transfer rate is higher than keyboard. Delaying a CPU temperature sensor could have serious consequences, overheat can damage CPU circuitry. From the above information we can conclude that priorities are-

CPU temperature sensor > Hard Disk > Mouse > Keyboard

👍 54 votes

-- Tejas Jaiswal (559 points)

5.8.8 Interrupts: GATE CSE 2018 | Question: 9 [top](#)

<https://gateoverflow.in/204083>



✓ Answer should be A.

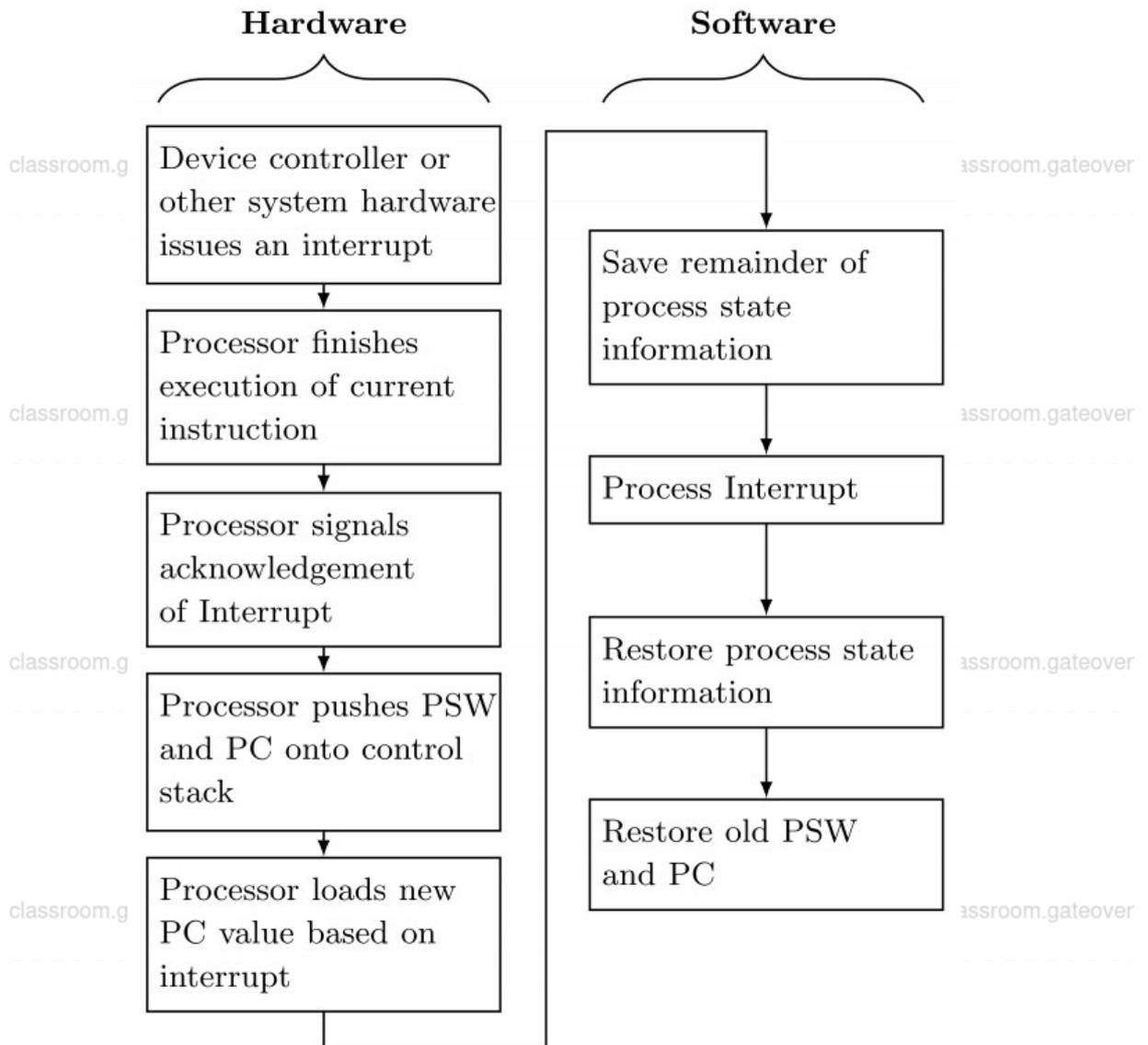


Fig: *Simple Interrupt Processing*

37 votes

-- Ayush Upadhyaya (28.4k points)

5.9

Io Handling (6) top

5.9.1 Io Handling: GATE CSE 1996 | Question: 1.20, ISRO2008-56 top

<https://gateoverflow.in/2724>



Which of the following is an example of spooled device?

- A. A line printer used to print the output of a number of jobs
- B. A terminal used to enter input data to a running program
- C. A secondary storage device in a virtual memory system
- D. A graphic display device

gate1996 operating-system io-handling normal isro2008

Answer

Which of the following is an example of a spooled device?

- A. The terminal used to enter the input data for the C program being executed
- B. An output device used to print the output of a number of jobs
- C. The secondary memory device in a virtual storage system
- D. The swapping area on a disk used by the swapper

gate1998 operating-system io-handling easy

Answer 

Which one of the following is true for a CPU having a single interrupt request line and a single interrupt grant line?

- A. Neither vectored interrupt nor multiple interrupting devices are possible
- B. Vectored interrupts are not possible but multiple interrupting devices are possible
- C. Vectored interrupts and multiple interrupting devices are both possible
- D. Vectored interrupts are possible but multiple interrupting devices are not possible

gate2005-cse operating-system io-handling normal

Answer 

Normally user programs are prevented from handling I/O directly by I/O instructions in them. For CPUs having explicit I/O instructions, such I/O protection is ensured by having the I/O instruction privileged. In a CPU with memory mapped I/O, there is no explicit I/O instruction. Which one of the following is true for a CPU with memory mapped I/O?

- A. I/O protection is ensured by operating system routine(s)
- B. I/O protection is ensured by a hardware trap
- C. I/O protection is ensured during system configuration
- D. I/O protection is not possible

gate2005-cse operating-system io-handling normal

Answer 

What is the bit rate of a video terminal unit with 80 characters/line, 8 bits/character and horizontal sweep time of 100 μ s (including 20 μ s of retrace time)?

- A. 8 Mbps
- B. 6.4 Mbps
- C. 0.8 Mbps
- D. 0.64 Mbps

gate2004-it operating-system io-handling easy isro2011

Answer 

Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O band-width?

- A. Transparent DMA and Polling interrupts

- B. Cycle-stealing and Vectored interrupts
- C. Block transfer and Vectored interrupts
- D. Block transfer and Polling interrupts

gate2006-it operating-system io-handling dma normal

Answer 

Answers: Io Handling

5.9.1 Io Handling: GATE CSE 1996 | Question: 1.20, ISRO2008-56 top 5<https://gateoverflow.in/2724>

✓ Answer is (A).

Spooling(simultaneous peripheral operations online) is a technique in which an intermediate device such as disk is interposed between process and low speed i/o device. For ex. in printer if a process attempt to print a document but printer is busy printing another document, the process, instead of waiting for printer to become available,write its output to disk. When the printer become available the data on disk is printed. Spooling allows process to request operation from peripheral device without requiring that the device be ready to service the request.

 50 votes

-- neha pawar (3.3k points)

5.9.2 Io Handling: GATE CSE 1998 | Question: 1.29 top 5<https://gateoverflow.in/1666>

✓ Answer : Option (B)

SPOOLing (Simultaneous Peripheral Operations OnLine) is a technique in which an intermediate device such as disk is interposed between process and low speed I/O device like a printer. If a process attempts to print a document but printer is busy printing another document, the process, instead of waiting for printer to become available, write its output to disk. When the printer become available the data on disk is printed. Spooling allows process to request operations from peripheral devices without requiring that the device be ready to service the request.

 20 votes

-- Tilak D. Nanavati (2.9k points)

5.9.3 Io Handling: GATE CSE 2005 | Question: 19 top 5<https://gateoverflow.in/1355>

✓ (C) is the correct answer. We can use one Interrupt line for all the devices connected and pass it through OR gate. On receiving by the CPU, it executes the corresponding ISR and after exec INTA is sent via one line. For Vectored Interrupts it is always possible if we implement in daisy chain mechanism.

Ref : [Click Here](#)

References

 29 votes

-- confused_luck (741 points)

5.9.4 Io Handling: GATE CSE 2005 | Question: 20 top 5<https://gateoverflow.in/1356>

✓ Option (A). User applications are not allowed to perform I/O in user mode - All I/O requests are handled through system calls that must be performed in kernel mode.

 45 votes

-- Vikrant Singh (11.2k points)



✓ Answer: (B)

Bit rate of a video terminal unit = $80 \times 8 \text{ bits}/100\mu\text{s} = 6.4 \text{ Mbps}$

👍 22 votes

-- Rajarshi Sarkar (27.9k points)



✓ CPU get highest bandwidth in transparent DMA and polling. but it asked for I/O bandwidth not cpu bandwidth so option (A) is wrong.

In case of Cycle stealing, in each cycle time device send data then wait again after few CPU cycle it sends to memory . So option (B) is wrong.

In case of Polling CPU takes the initiative so I/O bandwidth can not be high so option (D) is wrong .

Consider Block transfer, in each single block device send data so bandwidth (means the amount of data) must be high . This makes option (C) correct.

👍 38 votes

-- Bikram (58.4k points)

5.10

Memory Management (9) [top](#)

Let the page reference and the working set window be $ccdbcecead$ and 4, respectively. The initial working set at time $t = 0$ contains the pages $\{a, d, e\}$, where a was referenced at time $t = 0$, d was referenced at time $t = -1$, and e was referenced at time $t = -2$. Determine the total number of page faults and the average number of page frames used by computing the working set at each reference.

gate1992 operating-system memory-management normal descriptive

Answer



A computer installation has $1000k$ of main memory. The jobs arrive and finish in the following sequences.

```
Job 1 requiring 200k arrives
Job 2 requiring 350k arrives
Job 3 requiring 300k arrives
Job 1 finishes
Job 4 requiring 120k arrives
Job 5 requiring 150k arrives
Job 6 requiring 80k arrives
```

A. Draw the memory allocation table using Best Fit and First Fit algorithms.

B. Which algorithm performs better for this sequence?

gate1995 operating-system memory-management normal descriptive

Answer



A 1000 Kbyte memory is managed using variable partitions but no compaction. It currently has two partitions of sizes 200 Kbyte and 260 Kbyte respectively. The smallest allocation request in Kbyte that could be denied is for

- A. 151
- B. 181
- C. 231
- D. 541

gate1996 operating-system memory-management normal

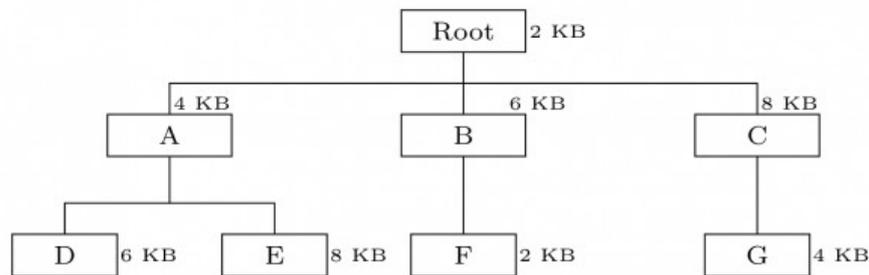
Answer 

5.10.4 Memory Management: GATE CSE 1998 | Question: 2.16 [top](#)

<https://gateoverflow.in/1689>



The overlay tree for a program is as shown below:



What will be the size of the partition (in physical memory) required to load (and run) this program?

- A. 12 KB
- B. 14 KB
- C. 10 KB
- D. 8 KB

gate1998 operating-system normal memory-management

Answer 

5.10.5 Memory Management: GATE CSE 2014 Set 2 | Question: 55 [top](#)

<https://gateoverflow.in/2022>



Consider the main memory system that consists of 8 memory modules attached to the system bus, which is one word wide. When a write request is made, the bus is occupied for 100 nanoseconds (ns) by the data, address, and control signals. During the same 100 ns, and for 500 ns thereafter, the addressed memory module executes one cycle accepting and storing the data. The (internal) operation of different memory modules may overlap in time, but only one request can be on the bus at any time. The maximum number of stores (of one word each) that can be initiated in 1 millisecond is _____

gate2014-cse-set2 operating-system memory-management numerical-answers normal

Answer 

5.10.6 Memory Management: GATE CSE 2015 Set 2 | Question: 30 [top](#)

<https://gateoverflow.in/8145>



Consider 6 memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB, where KB refers to kilobyte. These partitions need to be allotted to four processes of sizes 357 KB, 210 KB, 468 KB, 491 KB in that order. If the best-fit algorithm is used, which partitions are NOT allotted to any process?

- A. 200 KB and 300 KB
- B. 200 KB and 250 KB
- C. 250 KB and 300 KB
- D. 300 KB and 400 KB

gate2015-cse-set2 operating-system memory-management easy

Answer 

5.10.7 Memory Management: GATE CSE 2020 | Question: 11 [top](#)

<https://gateoverflow.in/333220>



Consider allocation of memory to a new process. Assume that none of the existing holes in the memory will exactly fit the process's memory requirement. Hence, a new hole of smaller size will be created if allocation is made in any of the existing holes. Which one of the following statement is TRUE?

- A. The hole created by first fit is always larger than the hole created by next fit.
- B. The hole created by worst fit is always larger than the hole created by first fit.
- C. The hole created by best fit is never larger than the hole created by first fit.
- D. The hole created by next fit is never larger than the hole created by best fit.

Answer

5.10.8 Memory Management: GATE IT 2006 | Question: 56 top

https://gateoverflow.in/3600



For each of the four processes $P_1, P_2, P_3,$ and P_4 . The total size in kilobytes (KB) and the number of segments are given below.

Process	Total size (in KB)	Number of segments
P_1	195	4
P_2	254	5
P_3	45	3
P_4	364	8

The page size is 1 KB. The size of an entry in the page table is 4 bytes. The size of an entry in the segment table is 8 bytes. The maximum size of a segment is 256 KB. The paging method for memory management uses two-level paging, and its storage overhead is P . The storage overhead for the segmentation method is S . The storage overhead for the segmentation and paging method is T . What is the relation among the overheads for the different methods of memory management in the concurrent execution of the above four processes?

- A. $P < S < T$
- B. $S < P < T$
- C. $S < T < P$
- D. $T < S < P$

Answer

5.10.9 Memory Management: GATE IT 2007 | Question: 11 top

https://gateoverflow.in/3444



Let a memory have four free blocks of sizes $4k, 8k, 20k, 2k$. These blocks are allocated following the best-fit strategy. The allocation requests are stored in a queue as shown below.

Request No	J1	J2	J3	J4	J5	J6	J7	J8
Request Sizes	2k	14k	3k	6k	6k	10k	7k	20k
Usage Time	4	10	2	8	4	1	8	6

The time at which the request for $J7$ will be completed will be

- A. 16
- B. 19
- C. 20
- D. 37

Answer

Answers: Memory Management

5.10.1 Memory Management: GATE CSE 1992 | Question: 12-b top

https://gateoverflow.in/43582



✓ Window size of working set = 4

Initial pages in the working set window = $\{e, d, a\}$

Incoming page	Time	Working set window	Hit/ Miss	Current window size
c	1	{e, d, a, c}	miss	4
c	2	{d, a, c}	hit	3
d	3	{a, c, d}	hit	3
b	4	{c, d, b}	miss	3
c	5	{d, b, c}	hit	3
e	6	{d, b, c, e}	miss	4
c	7	{b, c, e}	hit	3
e	8	{c, e}	hit	2
a	9	{c, e, a}	miss	3
d	10	{c, e, a, d}	miss	4

Total number of page faults = 5.

Average no. of page frames used by window set = $(4 + 3 + 3 + 3 + 3 + 4 + 3 + 2 + 3 + 4)/10 = 32/10 = 3.2$

👍 51 votes

-- Dhananjay Kumar Sharma (18.8k points)

5.10.2 Memory Management: GATE CSE 1995 | Question: 5 [top](#)

<https://gateoverflow.in/2641>



✓ Initial there is 1000k main memory available.

Then job 1 arrive and occupied 200k, then job 2 arrive, occupy 350k, after that job 3 arrive and occupy 300k (assume continuous allocation) now free memory is $1000 - 850(200 + 350 + 300) = 150k$ (till these jobs first fit and best fit are same)

Now, job 1 is finished. So, that space is also free. So, here 200k slot and 150k slots are free.

Now, job 4 arrives which is 120k.

Case 1:

- First fit, so it will be in 200 k slot (free slot) and now free is = $200 - 120 = 80k$,
- Now 150k arrive which will be in 150 k slot
- Then, 80k arrive which will occupy in 80k slot ($200 - 120$) so, all jobs will be allocated successfully.

Case 2:

- Best fit : 120k job will occupy best fit free space which is 150k so, now remaining $150 - 120 = 30k$,
- Then 150k job arrive it will be occupied in 200k slot, which is best fit for this job. So, free space = $200 - 150 = 50$,
- Now, job 80k arrive, but there is no continuous 80k memory free. So, it will not be allocated successfully.

So, first fit is better.

👍 27 votes

-- minal (13.1k points)

5.10.3 Memory Management: GATE CSE 1996 | Question: 2.18 [top](#)

<https://gateoverflow.in/2747>



✓ The answer is (B). Since the total size of the memory is 1000 KB, let's assume that the partitioning for the current allocation is done in such a way that it will leave minimum free space.

Partitioning the 1000 KB as below will allow gaps of 180 KB each and hence a request of 181 KB will not be met.

[180 KB - 200 KB - 180 KB - 260 KB - 180 KB] . The reasoning is more of an intuition rather than any formula.

👍 70 votes

-- kireeti (1k points)

5.10.4 Memory Management: GATE CSE 1998 | Question: 2.16 [top](#)

<https://gateoverflow.in/1689>



✓ "To enable a process to be larger than the amount of memory allocated to it, we can use overlays. The idea of overlays is to keep in memory only those instructions and data that are needed at any given time. When other instructions are needed, they are loaded into space occupied previously by instructions that are no longer needed." For the above program, maximum memory will be required when running code portion present at leaves. Max requirement = (max of requirements of D, E, F, and G).
 $= MAX(12, 14, 10, 14) = 14$ (Answer)

44 votes

-- learncp (1.1k points)

5.10.5 Memory Management: GATE CSE 2014 Set 2 | Question: 55 [top](#)

<https://gateoverflow.in/2022>



- ✓ When a write request is made, the bus is occupied for 100 ns. So, between 2 writes at least 100 ns interval must be there.

Now, after a write request, for $100 + 500 = 600$ ns, the corresponding memory module is busy storing the data. But, assuming the next stores are to a different memory module (we have totally 8 modules in question), we can have consecutive stores at intervals of 100 ns. So, maximum number of stores in 1 ms

$$= 10^{-3} \times 1 / (100 \times 10^{-9}) = 10,000$$

73 votes

-- Arjun Suresh (332k points)

5.10.6 Memory Management: GATE CSE 2015 Set 2 | Question: 30 [top](#)

<https://gateoverflow.in/8145>



- ✓ Option (A) is correct because we have 6 memory partitions of sizes 200 KB, 400 KB, 600 KB, 500 KB, 300 KB and 250 KB and the partition allotted to the process using best fit is given below:

357 KB process allotted at partition 400 KB.
210 KB process allotted at partition 250 KB
468 KB process allotted at partition 500 KB
491 KB process allotted at partition 600 KB

So, we have left only two partitions 200 KB and 300 KB

30 votes

-- Anoop Sonkar (4.1k points)

5.10.7 Memory Management: GATE CSE 2020 | Question: 11 [top](#)

<https://gateoverflow.in/333220>



- ✓ Best fit will search for the smallest block which is able to accommodate the request. So, the hole created by the Best Fit is always **less than or equal** to the hole created using any other method.

Worst fit search for the biggest possible block which is able to accommodate the request. It might be the case that block biggest possible block may be in the first block and both worst and first fit select the same block.

So, we can't say that hole formed by worst fit is always greater than first. The size of the hole can be same too. (B) is false

Ans: (C) Hole created by the best fit is never larger than the hole created by first fit,

The hole created by the Best Fit is equal to the hole created by first fit when the first fit happens to select the smallest block which can accommodate the required size.

13 votes

-- Srinivas_Reddy_Kotla (775 points)

5.10.8 Memory Management: GATE IT 2006 | Question: 56 [top](#)

<https://gateoverflow.in/3600>



For 2-level paging.

Page size is 1KB. So, no. of pages required for $P_1 = 195$. An entry in page table is of size 4 bytes and assuming an inner level page table takes the size of a page (this information is not given in question), we can have up to 256 entries in a second level page table and we require only 195 for P_1 . Thus only 1 second level page table is enough. So, memory overhead = 1KB (for first level) (again assumed as page size as not explicitly told in question) + 1KB for second level = 2KB.

For P_2 and P_3 also, we get 2KB each and for P_4 we get $1 + 2 = 3KB$ as it requires 1 first level page table and 2 second level page tables ($364 > 256$). So, total overhead for their concurrent execution = $2 \times 3 + 3 = 9KB$.

Thus $P = 9KB$.

For Segmentation method

Ref: <http://web.cs.wpi.edu/~cs3013/b02/week6-segmentation/week6-segmentation.html>

P_1 uses 4 segments \rightarrow 4 entries in segment table = $4 \times 8 = 32$ bytes.

Similarly, for P_2, P_3 and P_4 we get $5 \times 8, 3 \times 8$ and 8×8 bytes respectively and the total overhead will be $32 + 40 + 24 + 64 = 160$ bytes.

So, $S = 160B$.

For Segmentation with Paging

Here we segment first and then page. So, we need the page table size. We are given maximum size of a segment is $256 KB$ and page size is $1KB$ and thus we require 256 entries in the page table. So, total size of page table = $256 \times 4 = 1024$ bytes (exactly 1 page size).

So, now for P_1 we require 1 segment table of size 32 bytes plus 4 page table of size $1KB$ for the 4 segments. Similarly,

P_2 - 40 bytes and 5 KB
 P_3 - 24 bytes and 3 KB
 P_4 - 64 bytes and 8 KB .

Thus total overhead = 160 bytes + 4 $KB + 5 KB + 3 KB + 8 KB = 20480 + 160 = 20640$ bytes.

So, $T = 20640B$.

So, answer will be (B)- $S < P < T$.

References



79 votes

-- Arjun Suresh (332k points)



✓ PS: Since the block sizes are given, we cannot assume further splitting of them.

Also, the question implies a multiprocessing environment and we can assume the execution of a process is not affecting other process' runtime.

At t=0			At t=8		
Memory Block	Size	Job	Memory Block	Size	Job
A	4k	J3 (finishes at t = 2)	A	4k	
B	8k	J4 (finishes at t = 8)	B	8k	J5 (finishes at t=12)
C	20k	J2 (finishes at t = 10)	C	20k	J2 (finishes at t = 10)
D	2k	J1 (finishes at t=4)	D	2k	

At t=10			At t=11		
Memory Block	Size	Job	Memory Block	Size	Job
A	4k		A	4k	
B	8k	J5 (finishes at t=12)	B	8k	J5 (finishes at t=12)
C	20k	J6 (finishes at t = 11)	C	20k	J7 (finishes at t = 19)
D	2k		D	2k	

So, $J7$ finishes at $t = 19$.

Reference: <http://thumbsup2life.blogspot.fr/2011/02/best-fit-first-fit-and-worst-fit-memory.html>

Correct Answer: B

References



overflow.in

gateoverflow.in

classroom.gateover

57 votes

-- Arjun Suresh (332k points)

5.11

Os Protection (3) top

5.11.1 Os Protection: GATE CSE 1999 | Question: 1.11, UGCNET-Dec2015-II: 44 top

https://gateoverflow.in/1464



System calls are usually invoked by using

- A. a software interrupt
- B. polling
- C. an indirect jump
- D. a privileged instruction

gate1999 operating-system normal ugcnetdec2015ii os-protection

Answer

5.11.2 Os Protection: GATE CSE 2001 | Question: 1.13 top

https://gateoverflow.in/706



A CPU has two modes -- privileged and non-privileged. In order to change the mode from privileged to non-privileged

- A. a hardware interrupt is needed
- B. a software interrupt is needed
- C. a privileged instruction (which does not generate an interrupt) is needed
- D. a non-privileged instruction (which does not generate an interrupt) is needed

gate2001-cse operating-system normal os-protection

Answer

5.11.3 Os Protection: GATE IT 2005 | Question: 19, UGCNET-June2012-III: 57 top

https://gateoverflow.in/3764



A user level process in Unix traps the signal sent on a Ctrl-C input, and has a signal handling routine that saves appropriate files before terminating the process. When a Ctrl-C input is given to this process, what is the mode in which the signal handling routine executes?

- A. User mode
- B. Kernel mode
- C. Superuser mode
- D. Privileged mode

gate2005-it operating-system os-protection normal ugcnetjune2012iii

Answer

Answers: Os Protection

5.11.1 Os Protection: GATE CSE 1999 | Question: 1.11, UGCNET-Dec2015-II: 44 top

https://gateoverflow.in/1464



✓ Software interrupt is the answer.

Privileged instruction cannot be the answer as system call is done from user mode and privileged instruction cannot be done from user mode.

44 votes

-- Arjun Suresh (332k points)



Answer should be (D). Changing from privileged to non-privileged doesn't require an interrupt unlike from non-privileged to privileged. Also, to loose a privilege we don't need a privileged instruction though a privileged instruction does no harm.

http://web.cse.ohio-state.edu/~teodores/download/teaching/cse675.au08/CSE675.02_MIPS-ISA_part3.pdf

References



eoverflow.in

gateoverflow.in

classroom.gateover

👍 64 votes

-- Arjun Suresh (332k points)



- When an user send an input to the process it can not be in privileged mode as it is coming from an user so option D , Privileged mode can not be possible here ..

Now see , kernel mode = Privileged mode

- That means both option B and option D are equal. As option D can not be possible , option B also false.
- There is nothing called superuser mode so option C is clearly wrong .
- Only option A is left , when an user input come like ' ctrl+c' the signal handling routine **executes in user mode only as a user level** process in UNIX traps the signal.

Hence option A is correct answer.

👍 37 votes

-- Bikram (58.4k points)



The following page addresses, in the given sequence, were generated by a program:

1 2 3 4 1 3 5 2 1 5 4 3 2 3

This program is run on a demand paged virtual memory system, with main memory size equal to 4 pages. Indicate the page references for which page faults occur for the following page replacement algorithms.

- LRU
- FIFO

Assume that the main memory is initially empty.

gate1993 operating-system page-replacement normal descriptive

Answer [👍](#)



A memory page containing a heavily used variable that was initialized very early and is in constant use is removed then

- LRU page replacement algorithm is used
- FIFO page replacement algorithm is used
- LFU page replacement algorithm is used
- None of the above

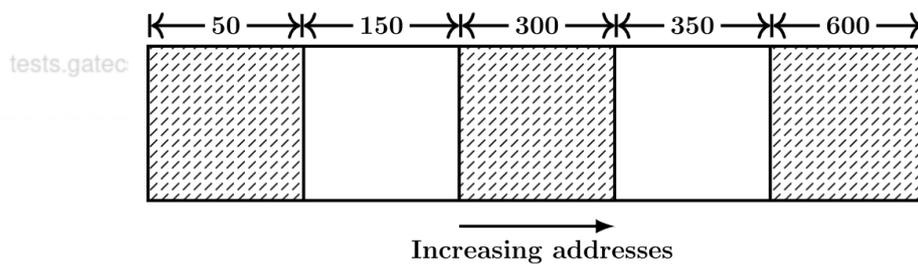
gate1994 operating-system page-replacement easy

Answer 

5.12.3 Page Replacement: GATE CSE 1994 | Question: 1.24 [top](#) 

<https://gateoverflow.in/2467>

Consider the following heap (figure) in which blank regions are not in use and hatched region are in use.



The sequence of requests for blocks of sizes 300, 25, 125, 50 can be satisfied if we use

- A. either first fit or best fit policy (any one)
- B. first fit but not best fit policy
- C. best fit but not first fit policy
- D. None of the above

gate1994 operating-system page-replacement normal

Answer 

5.12.4 Page Replacement: GATE CSE 1995 | Question: 1.8 [top](#) 

<https://gateoverflow.in/2595>

Which of the following page replacement algorithms suffers from Belady's anomaly?

- A. Optimal replacement
- B. LRU
- C. FIFO
- D. Both (A) and (C)

gate1995 operating-system page-replacement normal

Answer 

5.12.5 Page Replacement: GATE CSE 1995 | Question: 2.7 [top](#) 

<https://gateoverflow.in/2619>

The address sequence generated by tracing a particular program executing in a pure demand based paging system with 100 records per page with 1 free main memory frame is recorded as follows. What is the number of page faults?

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0370

- A. 13
- B. 8
- C. 7
- D. 10

gate1995 operating-system page-replacement normal

Answer 

5.12.6 Page Replacement: GATE CSE 1997 | Question: 3.10, ISRO2008-57, ISRO2015-64 [top](#) 

<https://gateoverflow.in/2241>

Dirty bit for a page in a page table

- A. helps avoid unnecessary writes on a paging device
- B. helps maintain LRU information
- C. allows only read on a page
- D. None of the above

gate1997 operating-system page-replacement easy isro2008 isro2015

Answer 5.12.7 Page Replacement: GATE CSE 1997 | Question: 3.5 [top](#) <https://gateoverflow.in/2236>

Locality of reference implies that the page reference being made by a process

- A. will always be to the page used in the previous page reference
- B. is likely to be to one of the pages used in the last few page references
- C. will always be to one of the pages existing in memory
- D. will always lead to a page fault

gate1997 operating-system page-replacement easy

Answer 5.12.8 Page Replacement: GATE CSE 1997 | Question: 3.9 [top](#) <https://gateoverflow.in/2240>

Thrashing

- A. reduces page I/O
- B. decreases the degree of multiprogramming
- C. implies excessive page I/O
- D. improve the system performance

gate1997 operating-system page-replacement easy

Answer 5.12.9 Page Replacement: GATE CSE 2001 | Question: 1.21 [top](#) <https://gateoverflow.in/714>

Consider a virtual memory system with FIFO page replacement policy. For an arbitrary page access pattern, increasing the number of page frames in main memory will

- A. always decrease the number of page faults
- B. always increase the number of page faults
- C. sometimes increase the number of page faults
- D. never affect the number of page faults

gate2001-cse operating-system page-replacement normal

Answer 5.12.10 Page Replacement: GATE CSE 2002 | Question: 1.23 [top](#) <https://gateoverflow.in/828>

The optimal page replacement algorithm will select the page that

- A. Has not been used for the longest time in the past
- B. Will not be used for the longest time in the future
- C. Has been used least number of times
- D. Has been used most number of times

gate2002-cse operating-system page-replacement easy

Answer 5.12.11 Page Replacement: GATE CSE 2004 | Question: 21, ISRO2007-44 [top](#) <https://gateoverflow.in/1018>

The minimum number of page frames that must be allocated to a running process in a virtual memory environment is determined by

- A. the instruction set architecture
- B. page size
- C. number of processes in memory
- D. physical memory size

gate2004-cse operating-system virtual-memory page-replacement normal isro2007

Answer

5.12.12 Page Replacement: GATE CSE 2005 | Question: 22, ISRO2015-36 [top](#)

<https://gateoverflow.in/1358>



Increasing the RAM of a computer typically improves performance because:

- A. Virtual Memory increases
- B. Larger RAMs are faster
- C. Fewer page faults occur
- D. Fewer segmentation faults occur

gate2005-cse operating-system page-replacement easy isro2015

Answer

5.12.13 Page Replacement: GATE CSE 2007 | Question: 56 [top](#)

<https://gateoverflow.in/1254>



A virtual memory system uses First In First Out (FIFO) page replacement policy and allocates a fixed number of frames to a process. Consider the following statements:

P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate.

Q: Some programs do not exhibit locality of reference.

Which one of the following is TRUE?

- A. Both P and Q are true, and Q is the reason for P
- B. Both P and Q are true, but Q is not the reason for P.
- C. P is false but Q is true
- D. Both P and Q are false.

gate2007-cse operating-system page-replacement normal

Answer

5.12.14 Page Replacement: GATE CSE 2007 | Question: 82 [top](#)

<https://gateoverflow.in/43510>



A process has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string): **1, 2, 1, 3, 7, 4, 5, 6, 3, 1**

If optimal page replacement policy is used, how many page faults occur for the above reference string?

- A. 7
- B. 8
- C. 9
- D. 10

gate2007-cse operating-system page-replacement normal

Answer

5.12.15 Page Replacement: GATE CSE 2007 | Question: 83 [top](#)

<https://gateoverflow.in/43510>



A process, has been allocated 3 page frames. Assume that none of the pages of the process are available in the memory initially. The process makes the following sequence of page references (reference string): **1, 2, 1, 3, 7, 4, 5, 6, 3, 1**

Least Recently Used (LRU) page replacement policy is a practical approximation to optimal page replacement. For the above reference string, how many more page faults occur with LRU than with the optimal page replacement policy?

- A. 0
- B. 1
- C. 2
- D. 3

gate2007-cse normal operating-system page-replacement

Answer

5.12.16 Page Replacement: GATE CSE 2009 | Question: 9, ISRO2016-52 top

<https://gateoverflow.in/1301>



In which one of the following page replacement policies, Belady's anomaly may occur?

- A. FIFO
- B. Optimal
- C. LRU
- D. MRU

gate2009-cse operating-system page-replacement normal isro2016

Answer

5.12.17 Page Replacement: GATE CSE 2010 | Question: 24 top

<https://gateoverflow.in/2203>



A system uses FIFO policy for system replacement. It has 4 page frames with no pages loaded to begin with. The system first accesses 100 distinct pages in some order and then accesses the same 100 pages but now in the reverse order. How many page faults will occur?

- A. 196
- B. 192
- C. 197
- D. 195

gate2010-cse operating-system page-replacement normal

Answer

5.12.18 Page Replacement: GATE CSE 2012 | Question: 42 top

<https://gateoverflow.in/2150>



Consider the virtual page reference string

1, 2, 3, 2, 4, 1, 3, 2, 4, 1

on a demand paged virtual memory system running on a computer system that has main memory size of 3 page frames which are initially empty. Let LRU, FIFO and OPTIMAL denote the number of page faults under the corresponding page replacement policy. Then

- A. $OPTIMAL < LRU < FIFO$
- B. $OPTIMAL < FIFO < LRU$
- C. $OPTIMAL = LRU$
- D. $OPTIMAL = FIFO$

gate2012-cse operating-system page-replacement normal

Answer

5.12.19 Page Replacement: GATE CSE 2014 Set 1 | Question: 33 top

<https://gateoverflow.in/1805>



Assume that there are 3 page frames which are initially empty. If the page reference string is 1, 2, 3, 4, 2, 1, 5, 3, 2, 4, 6 the number of page faults using the optimal replacement policy is _____.

gate2014-cse-set1 operating-system page-replacement numerical-answers

Answer



A computer has twenty physical page frames which contain pages numbered 101 through 120. Now a program accesses the pages numbered 1, 2, ..., 100 in that order, and repeats the access sequence **THRICE**. Which one of the following page replacement policies experiences the same number of page faults as the optimal page replacement policy for this program?

- A. Least-recently-used
- B. First-in-first-out
- C. Last-in-first-out
- D. Most-recently-used

gate2014-cse-set2

operating-system

page-replacement

ambiguous

goclasses.in

tests.gatecse.in

Answer



A system uses 3 page frames for storing process pages in main memory. It uses the Least Recently Used (**LRU**) page replacement policy. Assume that all the page frames are initially empty. What is the total number of page faults that will occur while processing the page reference string given below?

4, 7, 6, 1, 7, 6, 1, 2, 7, 2

gate2014-cse-set3

operating-system

page-replacement

numerical-answers

normal

goclasses.in

tests.gatecse.in

Answer



Consider a main memory with five-page frames and the following sequence of page references: 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3. Which one of the following is true with respect to page replacement policies First In First Out (FIFO) and Least Recently Used (LRU)?

- A. Both incur the same number of page faults
- B. FIFO incurs 2 more page faults than LRU
- C. LRU incurs 2 more page faults than FIFO
- D. FIFO incurs 1 more page faults than LRU

gate2015-cse-set1

operating-system

page-replacement

normal

goclasses.in

tests.gatecse.in

Answer



Consider a computer system with ten physical page frames. The system is provided with an access sequence $(a_1, a_2, \dots, a_{20}, a_1, a_2, \dots, a_{20})$, where each a_i is a distinct virtual page number. The difference in the number of page faults between the last-in-first-out page replacement policy and the optimal page replacement policy is _____.

gate2016-cse-set1

operating-system

page-replacement

normal

numerical-answers

goclasses.in

tests.gatecse.in

Answer



In which one of the following page replacement algorithms it is possible for the page fault rate to increase even when the number of allocated frames increases?

- A. LRU (Least Recently Used)
- B. OPT (Optimal Page Replacement)
- C. MRU (Most Recently Used)
- D. FIFO (First In First Out)

goclasses.in

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gate2016-cse-set2

operating-system

page-replacement

easy

Answer



Recall that Belady's anomaly is that the page-fault rate may *increase* as the number of allocated frames increases. Now, consider the following statements:

- S_1 : Random page replacement algorithm (where a page chosen at random is replaced) suffers from Belady's anomaly.
- S_2 : LRU page replacement algorithm suffers from Belady's anomaly.

Which of the following is CORRECT?

- A. S_1 is true, S_2 is true
- B. S_1 is true, S_2 is false
- C. S_1 is false, S_2 is true
- D. S_1 is false, S_2 is false

gate2017-cse-set1

page-replacement

operating-system

normal

Answer



In the context of operating systems, which of the following statements is/are correct with respect to paging?

- A. Paging helps solve the issue of external fragmentation
- B. Page size has no impact on internal fragmentation
- C. Paging incurs memory overheads
- D. Multi-level paging is necessary to support pages of different sizes

gate2021-cse-set1

multiple-selects

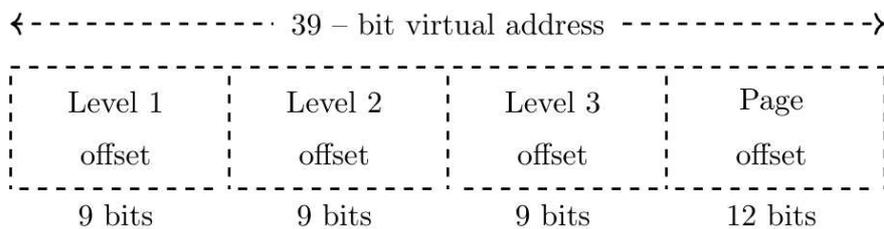
operating-system

page-replacement

Answer



Consider a three-level page table to translate a 39-bit virtual address to a physical address as shown below:



The page size is 4 KB ($1\text{KB} = 2^{10}$ bytes) and page table entry size at every level is 8 bytes. A process P is currently using 2GB ($1\text{GB} = 2^{30}$ bytes) virtual memory which is mapped to 2GB of physical memory. The minimum amount of memory required for the page table of P across all levels is _____ KB.

gate2021-cse-set2

numerical-answers

operating-system

memory-management

page-replacement

Answer



The address sequence generated by tracing a particular program executing in a pure demand paging system with 100 bytes per page is

0100, 0200, 0430, 0499, 0510, 0530, 0560, 0120, 0220, 0240, 0260, 0320, 0410.

Suppose that the memory can store only one page and if x is the address which causes a page fault then the bytes from addresses x to $x + 99$ are loaded on to the memory.

How many page faults will occur?

- A. 0
- B. 4
- C. 7

gate2007-it

tests.gatecse.in

operating-system

memory-management

page-replacement

Answer

gate2007-it operating-system virtual-memory page-replacement normal

Answer

5.12.29 Page Replacement: GATE IT 2007 | Question: 58 [top](#)<https://gateoverflow.in/3500>

A demand paging system takes 100 time units to service a page fault and 300 time units to replace a dirty page. Memory access time is 1 time unit. The probability of a page fault is p . In case of a page fault, the probability of page being dirty is also p . It is observed that the average access time is 3 time units. Then the value of p is

- A. 0.194
- B. 0.233
- C. 0.514
- D. 0.981

gate2007-it operating-system page-replacement probability normal

Answer

5.12.30 Page Replacement: GATE IT 2008 | Question: 41 [top](#)<https://gateoverflow.in/3351>

Assume that a main memory with only 4 pages, each of 16 bytes, is initially empty. The CPU generates the following sequence of virtual addresses and uses the Least Recently Used (LRU) page replacement policy.

0, 4, 8, 20, 24, 36, 44, 12, 68, 72, 80, 84, 28, 32, 88, 92 [goclasses.in](#)[tests.gatecse.in](#)

How many page faults does this sequence cause? What are the page numbers of the pages present in the main memory at the end of the sequence?

- A. 6 and 1, 2, 3, 4
- B. 7 and 1, 2, 4, 5
- C. 8 and 1, 2, 4, 5
- D. 9 and 1, 2, 3, 5

gate2008-it operating-system page-replacement normal

Answer

Answers: Page Replacement

5.12.1 Page Replacement: GATE CSE 1993 | Question: 21 [top](#)<https://gateoverflow.in/2318>

- ✓ LRU : 1, 2, 3, 4, 5, 2, 4, 3, 2
- FIFO : 1, 2, 3, 4, 5, 1, 2, 3

17 votes

-- Digvijay (44.9k points)

5.12.2 Page Replacement: GATE CSE 1994 | Question: 1.13 [top](#)<https://gateoverflow.in/2454>

- ✓ FIFO replaces a page which was brought into memory first will be removed first so since the variable was initialized very early. it is in the set of first in pages. so it will be removed answer: (B) if you use LRU - since it is used constantly it is a recently used item always. so cannot be removed. If you use LFU - the frequency of the page is more since it is in constant use. So cannot be replaced.

34 votes

-- Sankaranarayanan P.N (8.5k points)

5.12.3 Page Replacement: GATE CSE 1994 | Question: 1.24 [top](#)<https://gateoverflow.in/2467>

- ✓ In the first fit, block requests will be satisfied from the first free block that fits it.
 - The request for 300 will be satisfied by a 350 size block reducing the free size to 50.
 - Request for 25, satisfied by 150 size block, reducing it to 125.
 - Request for 125 satisfied by 125 size block.

- And request for 50 satisfied by the 50 size block.

So, all requests can be satisfied.

In the best fit strategy, a block request is satisfied by the smallest block that can fit it.

- The request for 300 will be satisfied by a 350 size block reducing the free size to 50.
- Request for 25, satisfied by 50 size block as its the smallest size that fits 25, reducing it to 25.
- Request for 125, satisfied by 150 size block, reducing it to 25.

Now, the request for 50 cannot be satisfied as the two 25 size blocks are not contiguous.

So, answer **(B)**.

👍 31 votes

-- Arjun Suresh (332k points)

5.12.4 Page Replacement: GATE CSE 1995 | Question: 1.8 top

<https://gateoverflow.in/2595>



✓ Answer is **(C)**.

FIFO suffers from Belady's anomaly. Optimal replacement never suffers from Belady's anomaly.

👍 17 votes

-- jayendra (6.7k points)

5.12.5 Page Replacement: GATE CSE 1995 | Question: 2.7 top

<https://gateoverflow.in/2619>



✓

- 0100 – 1 page fault. Records 0100 – 0199 in memory
- 0200 – 2 page faults. Records 0200 – 0299 in memory
- 0430 – 3 page faults. Records 0400 – 0499 in memory
- 0499 – 3 page faults. Records 0400 – 0499 in memory
- 0510 – 4 page faults. Records 0500 – 0599 in memory
- 0530 – 4 page faults. Records 0500 – 0599 in memory
- 0560 – 4 page faults. Records 0500 – 0599 in memory
- 0120 – 5 page faults. Records 0100 – 0199 in memory
- 0220 – 6 page faults. Records 0200 – 0299 in memory
- 0240 – 6 page faults. Records 0200 – 0299 in memory
- 0260 – 6 page faults. Records 0200 – 0299 in memory
- 0320 – 7 page faults. Records 0300 – 0399 in memory
- 0370 – 7 page faults. Records 0300 – 0399 in memory

So, (C) - 7 page faults.

👍 55 votes

-- Arjun Suresh (332k points)

5.12.6 Page Replacement: GATE CSE 1997 | Question: 3.10, ISRO2008-57, ISRO2015-64 top

<https://gateoverflow.in/2241>



✓ The dirty bit allows for a performance optimization. A page on disk that is paged in to physical memory, then read from, and subsequently paged out again does not need to be written back to disk, since the page hasn't changed. However, if the page was written to after it's paged in, its dirty bit will be set, indicating that the page must be written back to the backing store
answer: **(A)**

👍 52 votes

-- Sankaranarayanan P.N (8.5k points)

5.12.7 Page Replacement: GATE CSE 1997 | Question: 3.5 top

<https://gateoverflow.in/2234>



✓ Answer is **(B)**

Locality of reference is also called as principle of locality. It means that same data values or related storage locations are frequently accessed. This in turn saves time. There are mainly three types of principle of locality:

1. temporal locality
2. spatial locality
3. sequential locality

This is required because in programs related data are stored in consecutive locations and in loops same locations are referred again and again

28 votes

-- Neeraj7375 (1.1k points)

5.12.8 Page Replacement: GATE CSE 1997 | Question: 3.9 [top](#)

<https://gateoverflow.in/2240>



✓ (C)- implies excessive page I/O

http://en.wikipedia.org/wiki/Thrashing_%28computer_science%29

References



ateoverflow.in

gateoverflow.in

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28 votes

-- Sankaranarayanan P.N (8.5k points)

5.12.9 Page Replacement: GATE CSE 2001 | Question: 1.21 [top](#)

<https://gateoverflow.in/714>



✓ Answer is (C).

Belady **anomaly** is the name given to the phenomenon in which increasing the number of page frames results in an increase in the number of page faults for certain memory access patterns. This phenomenon is commonly experienced when using the First in First Out (**FIFO**) page replacement algorithm

References



ateoverflow.in

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21 votes

-- dheerajkhanna (143 points)

5.12.10 Page Replacement: GATE CSE 2002 | Question: 1.23 [top](#)

<https://gateoverflow.in/828>



✓ Optimal page replacement algorithm will always select the page that will not be used for the longest time in the future for replacement, and that is why the it is called optimal page replacement algorithm. Hence, **(B)** choice.

36 votes

-- Arjun Suresh (332k points)

5.12.11 Page Replacement: GATE CSE 2004 | Question: 21, ISRO2007-44 [top](#)

<https://gateoverflow.in/1018>



✓ Its instruction set architecture .if you have no indirect addressing then you need at least two pages in physical memory. One for instruction (code part) and another for if the data references memory.if there is one level of indirection then you will need at least three pages one for the instruction(code) and another two for the indirect addressing. If there three indirection then minimum 4 frames are allocated.

<http://stackoverflow.com/questions/11213013/minimum-page-frames>

References



ateoverflow.in

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64 votes

-- Prasanna Ranganathan (3.9k points)



✓ So, answer → (C).

1. Virtual Memory increases → This option is false. Because Virtual Memory of Computer do not depend on RAM. Virtual Memory concept itself was introduced so Programs larger than RAM can be executed.
2. Larger RAMs are faster → No This option is false. Size of ram does not determine it's speed, Type of ram does, SRAM is faster, DRAM is slower.
3. Fewer page faults occur → This is true, more pages can be in Main memory .
4. Fewer segmentation faults occur → "Segementation Fault" → A **segmentation fault** (aka segfault) is a common condition that causes programs to crash; they are often associated with a file named core . Segfaults are caused by a program trying to read or write an illegal memory location. It is clear that segmentation fault is not related to size of main memory. This is false.

👍 61 votes

-- Akash Kanase (36k points)



✓ P: Increasing the number of page frames allocated to a process sometimes increases the page fault rate.

This is true,

example : FIFO suffers from [Bélády's anomaly](#) which means that on Increasing the number of page frames allocated to a process it may sometimes increase the total number of page faults.

Q: Some programs do not exhibit locality of reference.

This is true : it is easy to write a program which jumps around a lot & which do not exhibit locality of reference.

Example : Assume that array is stored in Row Major order & We are accessing it in column major order.

So, answer is **option (B)**. (As there is no relation between P & Q. As it is clear from example, they are independent.)

References



👍 55 votes

-- Akash Kanase (36k points)



✓ Optimal replacement policy means a page which is "farthest" in the future to be accessed will be replaced next.

Frame 0	1
Frame 1	2 7 4 5 6
Frame 2	3

3 initial page faults for pages 1, 2, 3 and then for pages 7, 4, 5, 6 ⇒ 7 page faults occur.

Answer is (A).

👍 18 votes

-- Pooja Palod (24.1k points)



✓ Using *LRU* = 9 Page Fault

Using Optimal = 7 Page Fault

So, LRU-OPTIMAL = 2

Option (C).

17 votes

-- Manoj Kumar (26.7k points)

5.12.16 Page Replacement: GATE CSE 2009 | Question: 9, ISRO2016-52 [top](#)

<https://gateoverflow.in/1301>



It is (A).

http://en.wikipedia.org/wiki/B%C3%A9%C3%A1dy%27s_anomaly

References



17 votes

-- Gate Keeda (15.9k points)

5.12.17 Page Replacement: GATE CSE 2010 | Question: 24 [top](#)

<https://gateoverflow.in/2203>



Answer is (A).

When we access 100 distinct page in some order (for example 1, 2, 3 . . . 100) then total number of page faults = 100. At last, the 4 page frames will contain the pages 100, 99, 98 and 97. When we reverse the string (100, 99, 98, . . . , 1) then first four page accesses will not cause the page fault because they are already present in page frames. But the remaining 96 page accesses will cause 96 page faults. So, total number of page faults = 100 + 96 = 196.

35 votes

-- neha pawar (3.3k points)

5.12.18 Page Replacement: GATE CSE 2012 | Question: 42 [top](#)

<https://gateoverflow.in/2150>



Page fault for LRU = 9, FIFO = 6, OPTIMAL = 5

Answer is (B).

18 votes

-- Keith Kr (4.5k points)

5.12.19 Page Replacement: GATE CSE 2014 Set 1 | Question: 33 [top](#)

<https://gateoverflow.in/1805>



In Optimal page replacement a page which will be farthest accessed in future will be replaced first.

Here, we have 3 page frames. Since, initially they are empty the first 3 distinct page references will cause page faults.

After 3 distinct page accesses we have :

Page Frames
1 2 3

Next Use Order
2 1 3

Based on the Next Use Order, the next replacement will be 3. Proceeding like this we get

Request :

Page Frames
1 2 4

Next Use Order
2 1 4

 - Miss.

Request :

Page Frames
1 2 4

Next Use Order
2 1 4

 - Hit.

Request :

Page Frames
1 2 4

Next Use Order
2 4 1

 - Hit.

Request :

Page Frames
5 2 4

Next Use Order
2 4 5

 - Miss.

Request	Page Frames	Next Use Order	
3	3 2 4	2 4 3	- Miss.
Request	Page Frames	Next Use Order	
2	3 2 4	4 3 2	- Hit.
Request	Page Frames	Next Use Order	
4	1 2 4	4 3 2	- Hit.
Request	Page Frames	Next Use Order	
6	1 2 6	2 1 6	- Miss.

(When multiple pages are not going to be accessed again in future, replacing **any** of them is allowed in Optimal page replacement algorithm)

Now, counting the misses which includes the 3 initial ones we get number of page faults as $3 + 4 = 7$.

Correct Answer: 7.

6 votes

-- Arjun Suresh (332k points)

5.12.20 Page Replacement: GATE CSE 2014 Set 2 | Question: 33

<https://gateoverflow.in/1992>



It will be (D) i.e Most-recently-used.

To be clear "repeats the access sequence THRICE" means totally the sequence of page numbers are accessed 4 times though this is not important for the answer here.

If we go optimal page replacement algorithm it replaces the page which will be least used in near future.

Now we have frame size 20 and reference string is

1, 2, ..., 100, 1, 2, ..., 100, 1, 2, ..., 100, 1, 2, ..., 100

First 20 accesses will cause page faults - the initial pages are no longer used and hence optimal page replacement replaces them first. Now, for page 21, according to reference string page 1 will be used again after 100 and similarly 2 will be used after 1 so, on and so the least likely to be used page in future is page 20. So, for 21st reference page 20 will be replaced and then for 22nd page reference, page 21 will be replaced and so on which is MOST RECENTLY USED page replacement policy.

PS: Even for Most Recently Used page replacement at first all empty (invalid) pages frames are replaced and then only most recently used ones are replaced.

67 votes

-- Kalpish Singhal (1.6k points)

5.12.21 Page Replacement: GATE CSE 2014 Set 3 | Question: 20

<https://gateoverflow.in/2054>



Total page faults = 6.

4	7	6	1	7	6	1	2	7	2
		\boxed{F}	6	6	6	6	6	\boxed{F}	7
	\boxed{F}	7	7	7	7	7	\boxed{F}	2	2
\boxed{F}	4	4	\boxed{F}	1	1	1	1	1	1

⇒ 6 faults

Another way of answering the same.

6	6	7	7
7	2	2	2
1	1	1	1

⇒ 3 faults + 3 initial access faults = 6 page faults

OR

7
2
1

⇒ 3 faults + 3 initial access faults = 6 page faults

22 votes

-- Akhil Nadh PC (1.6k points)

5.12.22 Page Replacement: GATE CSE 2015 Set 1 | Question: 47

https://gateoverflow.in/8353



Requested Page references are 3, 8, 2, 3, 9, 1, 6, 3, 8, 9, 3, 6, 2, 1, 3 and number of page frames is 5.

In FIFO Page replacement will take place in sequence in pattern First In first Out, as following

Request	3	8	2	3	9	1	6	3	8	9	3	6	2	1	3
Frame 5						1	1	1	1	1	1	1	1	1	1
Frame 4					9	9	9	9	9	9	9	9	2	2	2
Frame 3			2	2	2	2	2	2	8	8	8	8	8	8	8
Frame 2		8	8	8	8	8	8	3	3	3	3	3	3	3	3
Frame 1	3	3	3	3	3	3	6	6	6	6	6	6	6	6	6
Miss/hit	F	F	F	H	F	F	F	F	F	H	H	H	F	H	H

Number of Faults = 9. Number of Hits = 6

Using Least Recently Used (LRU) page replacement will be the page which is visited least recently (which is not used for the longest time), as following:

Request	3	8	2	3	9	1	6	3	8	9	3	6	2	1	3
Frame 5						1	1	1	1	1	1	1	2	2	2
Frame 4					9	9	9	9	9	9	9	9	9	9	9
Frame 3			2	2	2	2	2	2	8	8	8	8	8	1	1
Frame 2		8	8	8	8	8	6	6	6	6	6	6	6	6	6
Frame 1	3	3	3	3	3	3	3	3	3	3	3	3	3	3	3
Miss/hit	F	F	F	H	F	F	F	H	F	H	H	H	F	F	H

Number of Faults = 9. Number of Hits = 6

So, both incur the same number of page faults.

Correct Answer: A

31 votes

-- Raghuvveer Dhakad (1.6k points)

5.12.23 Page Replacement: GATE CSE 2016 Set 1 | Question: 49

https://gateoverflow.in/39711



Answer is 1.

In LIFO first 20 are page faults followed by next 9 hits then next 11 page faults. (After a10, a11 replaces a10, a12 replaces a11 and so on)

In optimal first 20 are page faults followed by next 9 hits then next 10 page faults followed by last page hit.

70 votes

-- Krishna murthy (271 points)

5.12.24 Page Replacement: GATE CSE 2016 Set 2 | Question: 20

https://gateoverflow.in/39559



Option D. FIFO suffers from Belady's anomaly.

Check this out:

- https://gateoverflow.in/1301/gate2009_9
- https://gateoverflow.in/1254/gate2007_56
- https://gateoverflow.in/2595/gate1995_1-8

References



19 votes

-- Shashank Chavan (2.4k points)

5.12.25 Page Replacement: GATE CSE 2017 Set 1 | Question: 40 top 5

<https://gateoverflow.in/118323>



✓ A page replacement algorithm suffers from Belady's anomaly when it is not a stack algorithm.

A stack algorithm is one that satisfies the inclusion property. The inclusion property states that, at a given time, the contents(pages) of a memory of size k page-frames is a subset of the contents of memory of size $k + 1$ page-frames, for the same sequence of accesses. The advantage is that running the same algorithm with more pages(i.e. larger memory) will never increase the number of page faults.

Is LRU a stack algorithm?

Yes, LRU is a stack algorithm. Therefore, it doesn't suffer from Belady's anomaly.

Ref : [Ref1](#) and [Ref2](#)

Is Random page replacement algorithm a stack algorithm?

No, as it may choose a page to replace in FIFO manner or in a manner which does not satisfy inclusion property. This means it could suffer from Belady's anomaly.

∴ (B) should be answer.

References



65 votes

-- Kantikumar (3.4k points)

5.12.26 Page Replacement: GATE CSE 2021 Set 1 | Question: 11 top 5

<https://gateoverflow.in/357441>



✓ Pages are divided into fixed size slots , so no external fragmentation

But applications smaller than page size cause internal fragmentation

Page tables take extra pages in memory. Therefore incur extra cost

Correct ans A and C

2 votes

-- Meetdoshi90 (281 points)

5.12.27 Page Replacement: GATE CSE 2021 Set 2 | Question: 48 top 5

<https://gateoverflow.in/357489>



✓ Given :

- Virtual address (VA) = 39 bits
- Page size = 4KB
- Physical address (PA) = 2GB
- Page table entry size (PTE) = 8B
- Three level pages tables with address division (9, 9, 9, 12)

Three level pages tables with address division (9, 9, 9, 12) means:

- 9 most significant bits for indexing into the level-1(outer level),
- 9 bits for the level-2 index,
- 9 bits for the level-3 index, and
- 12 bits for the offset within a page.

The entries of the level-1 page table are pointers to a level-2 page table, the entries of the level-2 page table are pointers to a level-3 page table, and the entries of the level-3 page table are PTEs that contain actual frame number where our desired word resides.

9 bits for a level means 2^9 entries in one-page table of that level.

For our process P :

P is using 2 GB of its VM. The rest of its VM is unused.

2 GB VM will have $2 \text{ GB} / 4 \text{ KB} = 2^{19}$ Pages.

But level 3 page table has only 2^9 entries. So, one-page table of level 3 can point to 2^9 pages of VM only, So, we need 2^{10} level-3 page tables of process P .

So, at level-3, we have 2^{10} page tables, So, we need 2^{10} entries in Level-2 But level 2 page table has only 2^9 entries, so, one-page table of level 2 can only point to 2^9 page tables of level-3, So, we need 2 level-2 page tables.

So, we need 1 Level-1 page table to point to level-2 page tables.

So, for process P , we need only 1 Level-1 page table, 2 level-2 page tables, and 2^{10} level-3 page tables.

Note that All the page tables, at every level, have same size which is $2^9 \times 8 \text{ B} = 2^{12} \text{ B} = 4 \text{ KB}$

(Because every page table at every level has 2^9 entries and Page table entry size at every level is 8 B)

So, in total, we need $1 + 2 + 2^{10}$ page tables (1 Level-1, 2 Level-2, 2^{10} level-3), and each page table size is 4 KB

So, total page tables size = $1027 \times 4 \text{ KB} = 4108 \text{ KB}$

So, the answer is 4108.

NOTE :

In this question, in place of Multilevel paging, If we had used Single Level Page table (also known as Flat level page table OR linear page table), then size of page table would be 1 GB.

Single Level Page Table :

Single-Level Page Tables are single linear array of page-table entries (PTEs). Each PTE contains information about the page, such as its physical page number ("frame" number) as well as status bits, such as whether or not the page is valid, and other bits. the i th entry in the array gives the frame number in which the i th page is stored.

- Virtual address(VA) = 39 bits
- Page size = 4 KB

So, number of pages in Virtual address space (VAS) of each process = $2^{39} \text{ B} / 4 \text{ KB} = 2^{27}$

So, we need 2^{27} entries in the page table. Each PTE size = 8 B

So, size of page table for the process = $2^{29} \times 8 \text{ B} = 1 \text{ GB}$

NOTE that Single level paging CANNOT take advantage of the unused space by the process. The single level page table needs one entry per page. Furthermore, since the process has a very sparse virtual address space, so, the vast majority of these PTEs would simply be marked invalid. BUT space taken by single level page table will be 1GB only. It only depends on the virtual address space, NOT depend on the used memory of process.

A Common Mistake that students make :

In this question, if in place of Multilevel paging, If we had used Single Level Page table, then what would be size of page table ??

The mistake is that some students will consider 2 GB memory that the process is using, and will get answer $(2 \text{ GB} / 4 \text{ KB}) \times 8 \text{ B} = 4 \text{ MB}$ which is wrong.

Remember that the CORE reason why we use multilevel paging in place of single level paging is that we want to reduce size of page table by taking advantage of unused space of process and making most entries in the outer level page table as invalid entries.

- https://people.cs.umass.edu/~emery/classes/cmpsci377/current/notes/lecture_15_vm.pdf
- <https://www.youtube.com/watch?v=PKy9Jxc3blw>
- <https://www.youtube.com/watch?v=pcTAoyzW2rY>

References



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6 votes

-- Deepak Poonia (23.4k points)

5.12.28 Page Replacement: GATE IT 2007 | Question: 12 top

<https://gateoverflow.in/3445>



- ✓ 0100 - page fault, addresses till 199 in memory
- 0200 - page fault, addresses till 299 in memory
- 0430 - page fault, addresses till 529 in memory
- 0499 - no page fault
- 0510 - no page fault
- 0530 - page fault, addresses till 629 in memory
- 0560 - no page fault
- 0120 - page fault, addresses till 219 in memory
- 0220 - page fault, addresses till 319 in memory
- 0240 - no page fault
- 0260 - no page fault
- 0320 - page fault, addresses till 419 in memory
- 0410 - no page fault
- So, 7 is the answer- (C)

67 votes

-- Arjun Suresh (332k points)

5.12.29 Page Replacement: GATE IT 2007 | Question: 58 top

<https://gateoverflow.in/3500>



$$p(p \times 300 + (1 - p) \times 100) + (1 - p) \times 1 = 3$$

$$\implies p(300p + 100 - 100p) + 1 - p = 3$$

$$\implies 200p^2 + 99p - 2 = 0$$

After solving this equation using Sridharacharya formula: $\frac{-b \pm \sqrt{b^2 - 4ac}}{2a}$, we get

$$p \approx 0.0194.$$

72 votes

-- Laxmi (793 points)

5.12.30 Page Replacement: GATE IT 2008 | Question: 41 top

<https://gateoverflow.in/3351>



- ✓ At first we have to translate the given virtual addresses (which addresses a byte) to page addresses (which again is virtual but addresses a page). This can be done simply by dividing the virtual addresses by page size and taking the floor value (equivalently by removing the page offset bits). Here, page size is 16 bytes which requires 4 offset bits. So, 0, 4, 8, 20, 24, 36, 44, 12, 68, 72, 80, 84, 28, 32, 88, 92 \implies 0, 0, 0, 1, 1, 2, 2, 0, 4, 4, 5, 5, 1, 2, 5, 5

We have 4 spaces for a page and there will be a replacement only when a 5th distinct page comes. Lets see what happens for the sequence of memory accesses:

Incoming Virtual Address	Page Address	No. of Page Faults	Pages in Memory in LRU Order
0	0	1	0
4	0	1	0
8	0	1	0
20	1	2	0, 1
24	1	2	0, 1
36	2	3	0, 1, 2
44	2	3	0, 1, 2
12	0	3	1, 2, 0
68	4	4	1, 2, 0, 4
72	4	4	1, 2, 0, 4
80	5	5	2, 0, 4, 5
84	5	5	2, 0, 4, 5
28	1	6	0, 4, 5, 1
32	2	7	4, 5, 1, 2
88	5	7	4, 1, 2, 5
92	5	7	4, 1, 2, 5

So, (B) choice.

69 votes

-- Arjun Suresh (332k points)

5.13

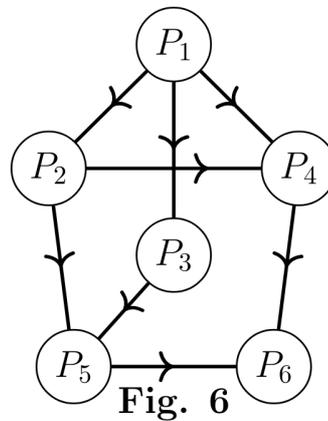
Precedence Graph (3) [top](#)

5.13.1 Precedence Graph: GATE CSE 1989 | Question: 11b [top](#)

<https://gateoverflow.in/91096>



Consider the following precedence graph (Fig.6) of processes where a node denotes a process and a directed edge from node P_i to node P_j implies; that P_i must complete before P_j commences. Implement the graph using FORK and JOIN constructs. The actual computation done by a process may be indicated by a comment line.



gate1989 descriptive operating-system precedence-graph process-synchronization

Answer

5.13.2 Precedence Graph: GATE CSE 1991 | Question: 01-xii [top](#)

<https://gateoverflow.in/508>



A given set of processes can be implemented by using only **parbegin/parend** statement, if the precedence graph of these processes is _____

gate1991 operating-system normal precedence-graph fill-in-the-blanks

Answer



Draw the precedence graph for the concurrent program given below

```

S1
parbegin
  begin
    S2:S4
  end;
  begin
    S3;
    parbegin
      S5;
      begin
        S6:S8
      end
    parend
  end;
end;
S7
parend;
S9
    
```

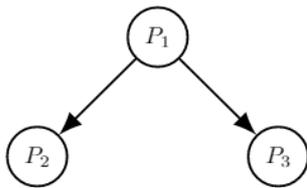
gate1992 operating-system normal concurrency precedence-graph descriptive

Answer

Answers: Precedence Graph

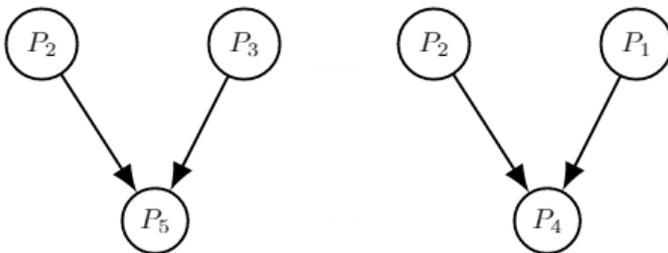


Step 1 :



- P_1
- fork L_1
- P_2
- fork L_2
- L_1 : fork L_2
- P_3
- goto L_3

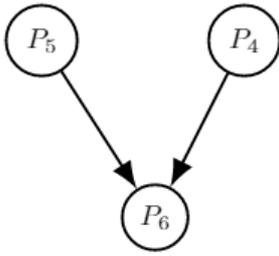
Step 2 :



and

- L_2 : Join C_1
- P_4
- goto L_4
- L_3 : Join C_2
- P_5
- goto L_4

Step 3 :



- L_4 : Join C_3
- P_6

3 votes

-- pankaj borah (41 points)

5.13.2 Precedence Graph: GATE CSE 1991 | Question: 01-xii top 5

<https://gateoverflow.in/508>



✓ A given set of processes can be implemented by using only **parbegin/parend** statement, if the precedence graph of these processes is **properly nested**

Reference : <http://nob.cs.ucdavis.edu/classes/ecs150-2008-04/handouts/sync.pdf>

1. It should be closed under par begin and par end.
2. Process execute concurrently.

https://gateoverflow.in/1739/gate1998_24#viewbutton

In this question precedence graph is nested.

1. All the process execute concurrently, closed under par begin and par end.
2. If you see all the serial execution come then signal the resource and and parallel process down the value (resource) similar all the process which are which are dependent to other one, other one release the resource then it will be got that with down and after release the its own resource. In the sense all the process are executing concurrently.

References



15 votes

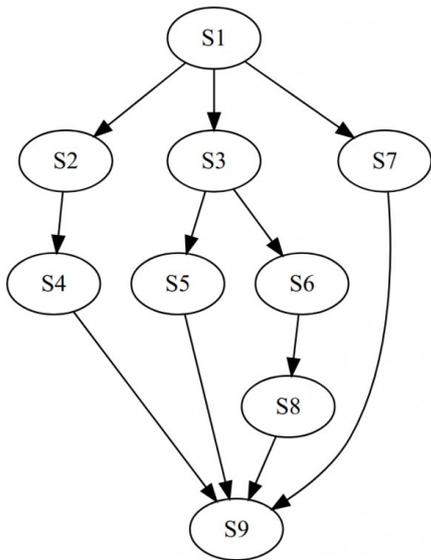
-- minal (13.1k points)

5.13.3 Precedence Graph: GATE CSE 1992 | Question: 12-a top 5

<https://gateoverflow.in/591>



✓ parbegin-parend shows parallel execution while begin-end shows serial execution



21 votes

-- Sheshang M. Ajwalia (2.6k points)

5.14

Process (4)

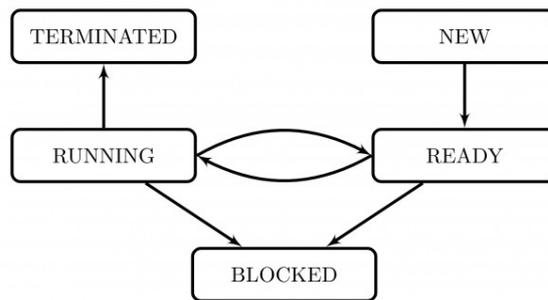
5.14.1 Process: GATE CSE 1996 | Question: 1.18

<https://gateoverflow.in/2722>



The process state transition diagram in the below figure is representative of

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- A. a batch operating system
- B. an operating system with a preemptive scheduler
- C. an operating system with a non-preemptive scheduler
- D. a uni-programmed operating system

gate1996 operating-system normal process

Answer

5.14.2 Process: GATE CSE 2001 | Question: 2.20

<https://gateoverflow.in/738>



Which of the following does not interrupt a running process?

- A. A device
- B. Timer
- C. Scheduler process
- D. Power failure

gate2001-cse operating-system easy process

Answer



Which combination of the following features will suffice to characterize an OS as a multi-programmed OS?

- More than one program may be loaded into main memory at the same time for execution
- If a program waits for certain events such as I/O, another program is immediately scheduled for execution
- If the execution of a program terminates, another program is immediately scheduled for execution.

- (a)
- (a) and (b)
- (a) and (c)
- (a), (b) and (c)

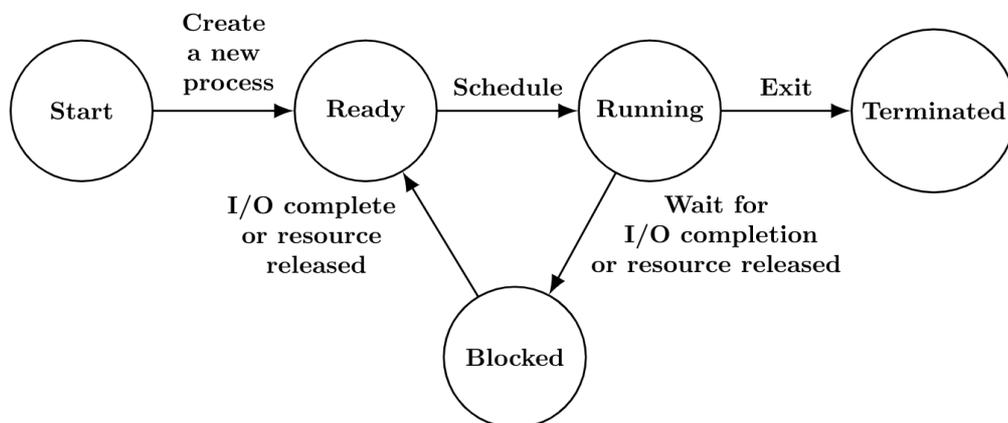
gate2002-cse operating-system normal process

Answer



The process state transition diagram of an operating system is as given below.

Which of the following must be FALSE about the above operating system?



- It is a multiprogrammed operating system
- It uses preemptive scheduling
- It uses non-preemptive scheduling
- It is a multi-user operating system

gate2006-it operating-system normal process

Answer

Answers: Process



- ✓ Answer is **(B)**. The transition from running to ready indicates that the process in the running state can be preempted and brought back to ready state.

35 votes

-- kireeti (1k points)



- ✓ Answer is **(C)**.

Timer and disk both makes interrupt and power failure will also interrupt the system. Only a scheduler process will not interrupt the running process as scheduler process gets called only when no other process is running (preemption if any would have happened before scheduler starts execution).

Quote from wikipedia

In the Linux kernel, the scheduler is called after each timer interrupt (that is, quite a few times per second). It determines what process to run next based on a variety of factors, including priority, time already run, etc. The implementation of preemption in other kernels is likely to be similar.

<https://www.quora.com/How-does-the-timer-interrupt-invoke-the-process-scheduler>

References



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52 votes

-- jayendra (6.7k points)

5.14.3 Process: GATE CSE 2002 | Question: 2.21 [top](#)

<https://gateoverflow.in/851>



✓ (A) and (B) suffice multi programming concept. For multi programming more than one program should be in memory and if any program goes for Io another can be scheduled to use CPU as shown below:

So ans is (B).

52 votes

-- Pooja Palod (24.1k points)

5.14.4 Process: GATE IT 2006 | Question: 13 [top](#)

<https://gateoverflow.in/3552>



✓ **Answer (B).**

Explanation:

- A. It is a multiprogrammed operating system.
Correct, it has ready state. We can have multiple processes in ready state here so this is Multiprogrammed OS.
- B. It uses preemptive scheduling
False : There is no arrow transition from running to ready state. So, this is non preemptive.
- C. It uses non-preemptive scheduling
True.
- D. It is a multi-user operating system.
We can have multiple user processes in ready state. So, this is also correct.

42 votes

-- Akash Kanase (36k points)

5.15

Process Scheduling (43) [top](#)

5.15.1 Process Scheduling: GATE CSE 1988 | Question: 2xa [top](#)

<https://gateoverflow.in/93951>



State any undesirable characteristic of the following criteria for measuring performance of an operating system:

Turn around time

gate1988 normal descriptive operating-system process-scheduling

Answer

5.15.2 Process Scheduling: GATE CSE 1988 | Question: 2xb [top](#)

<https://gateoverflow.in/93953>



State any undesirable characteristic of the following criteria for measuring performance of an operating system:

Waiting time

Answer

5.15.3 Process Scheduling: GATE CSE 1990 | Question: 1-vi top

<https://gateoverflow.in/83850>



The highest-response ratio next scheduling policy favours _____ jobs, but it also limits the waiting time of _____ jobs.

Answer

5.15.4 Process Scheduling: GATE CSE 1993 | Question: 7.10 top

<https://gateoverflow.in/2298>



Assume that the following jobs are to be executed on a single processor system

Job Id	CPU Burst Time
p	4
q	1
r	8
s	1
t	2

The jobs are assumed to have arrived at time 0^+ and in the order p, q, r, s, t . Calculate the departure time (completion time) for job p if scheduling is round robin with time slice 1

- A. 4
- B. 10
- C. 11
- D. 12
- E. None of the above

Answer

5.15.5 Process Scheduling: GATE CSE 1995 | Question: 1.15 top

<https://gateoverflow.in/2602>



Which scheduling policy is most suitable for a time shared operating system?

- A. Shortest Job First
- B. Round Robin
- C. First Come First Serve
- D. Elevator

Answer

5.15.6 Process Scheduling: GATE CSE 1995 | Question: 2.6 top

<https://gateoverflow.in/2618>



The sequence _____ is an optimal non-preemptive scheduling sequence for the following jobs which leaves the CPU idle for _____ unit(s) of time.

Job	Arrival Time	Burst Time
1	0.0	9
2	0.6	5
3	1.0	1

- A. {3, 2, 1}, 1
- B. {2, 1, 3}, 0
- C. {3, 2, 1}, 0
- D. {1, 2, 3}, 5

Answer 

5.15.7 Process Scheduling: GATE CSE 1996 | Question: 2.20, ISRO2008-15 [top](#)

<https://gateoverflow.in/2749>



Four jobs to be executed on a single processor system arrive at time 0 in the order A, B, C, D . Their burst CPU time requirements are 4, 1, 8, 1 time units respectively. The completion time of A under round robin scheduling with time slice of one time unit is

- A. 10
- B. 4
- C. 8
- D. 9

Answer 

5.15.8 Process Scheduling: GATE CSE 1998 | Question: 2.17, UGCNET-Dec2012-III: 43 [top](#)

<https://gateoverflow.in/1690>



Consider n processes sharing the CPU in a round-robin fashion. Assuming that each process switch takes s seconds, what must be the quantum size q such that the overhead resulting from process switching is minimized but at the same time each process is guaranteed to get its turn at the CPU at least every t seconds?

- A. $q \leq \frac{t - ns}{n - 1}$
- B. $q \geq \frac{t - ns}{n - 1}$
- C. $q \leq \frac{t - ns}{n + 1}$
- D. $q \geq \frac{t - ns}{n + 1}$

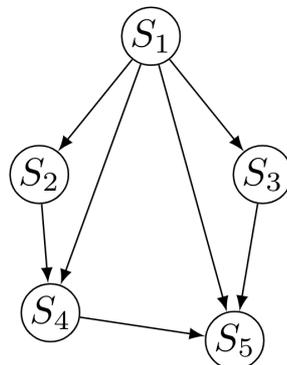
Answer 

5.15.9 Process Scheduling: GATE CSE 1998 | Question: 24 [top](#)

<https://gateoverflow.in/1739>



- a. Four jobs are waiting to be run. Their expected run times are 6, 3, 5 and x . In what order should they be run to minimize the average response time?
- b. Write a concurrent program using par begin-par end to represent the precedence graph shown below.



Answer 

5.15.10 Process Scheduling: GATE CSE 1998 | Question: 7-b [top](#)

<https://gateoverflow.in/12963>



In a computer system where the 'best-fit' algorithm is used for allocating 'jobs' to 'memory partitions', the following situation

was encountered:

Partitions size in KB	4K 8K 20K 2K
Job sizes in KB	2K 14K 3K 6K 6K 10K 20K 2K
Time for execution	4 10 2 1 4 1 8 6

When will the 20K job complete?

gate1998 operating-system process-scheduling normal

Answer

5.15.11 Process Scheduling: GATE CSE 2002 | Question: 1.22 top

<https://gateoverflow.in/827>



Which of the following scheduling algorithms is non-preemptive?

- A. Round Robin
- B. First-In First-Out
- C. Multilevel Queue Scheduling
- D. Multilevel Queue Scheduling with Feedback

gate2002-cse operating-system process-scheduling easy

Answer

5.15.12 Process Scheduling: GATE CSE 2003 | Question: 77 top

<https://gateoverflow.in/963>



A uni-processor computer system only has two processes, both of which alternate 10 ms CPU bursts with 90 ms I/O bursts. Both the processes were created at nearly the same time. The I/O of both processes can proceed in parallel. Which of the following scheduling strategies will result in the *least* CPU utilization (over a long period of time) for this system?

- A. First come first served scheduling
- B. Shortest remaining time first scheduling
- C. Static priority scheduling with different priorities for the two processes
- D. Round robin scheduling with a time quantum of 5 ms

gate2003-cse operating-system process-scheduling normal

Answer

5.15.13 Process Scheduling: GATE CSE 2004 | Question: 46 top

<https://gateoverflow.in/1043>



Consider the following set of processes, with the arrival times and the CPU-burst times given in milliseconds.

Process	Arrival Time	Burst Time
P1	0	5
P2	1	3
P3	2	3
P4	4	1

What is the average turnaround time for these processes with the preemptive shortest remaining processing time first (SRPT) algorithm?

- A. 5.50
- B. 5.75
- C. 6.00
- D. 6.25

gate2004-cse operating-system process-scheduling normal

Answer



Consider three CPU-intensive processes, which require 10, 20 and 30 time units and arrive at times 0, 2 and 6, respectively. How many context switches are needed if the operating system implements a shortest remaining time first scheduling algorithm? Do not count the context switches at time zero and at the end.

- A. 1
- B. 2
- C. 3
- D. 4

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isro2009

Answer



Consider three processes (process id 0, 1, 2 respectively) with compute time bursts 2, 4 and 8 time units. All processes arrive at time zero. Consider the longest remaining time first (LRTF) scheduling algorithm. In LRTF ties are broken by giving priority to the process with the lowest process id. The average turn around time is:

- A. 13 units
- B. 14 units
- C. 15 units
- D. 16 units

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Answer



Consider three processes, all arriving at time zero, with total execution time of 10, 20 and 30 units, respectively. Each process spends the first 20% of execution time doing I/O, the next 70% of time doing computation, and the last 10% of time doing I/O again. The operating system uses a shortest remaining compute time first scheduling algorithm and schedules a new process either when the running process gets blocked on I/O or when the running process finishes its compute burst. Assume that all I/O operations can be overlapped as much as possible. For what percentage of time does the CPU remain idle?

- A. 0%
- B. 10.6%
- C. 30.0%
- D. 89.4%

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process-scheduling

normal

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Answer



Group 1 contains some CPU scheduling algorithms and Group 2 contains some applications. Match entries in Group 1 to entries in Group 2.

Group I	Group II
(P) Gang Scheduling	(1) Guaranteed Scheduling
(Q) Rate Monotonic Scheduling	(2) Real-time Scheduling
(R) Fair Share Scheduling	(3) Thread Scheduling

- A. P – 3; Q – 2; R – 1
- B. P – 1; Q – 2; R – 3
- C. P – 2; Q – 3; R – 1
- D. P – 1; Q – 3; R – 2

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process-scheduling

normal

Answer



An operating system used Shortest Remaining System Time first (SRT) process scheduling algorithm. Consider the arrival times and execution times for the following processes:

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Process	Execution Time	Arrival Time
P1	20	0
P2	25	15
P3	10	30
P4	15	45

What is the total waiting time for process P_2 ?

- A. 5
- B. 15
- C. 40
- D. 55

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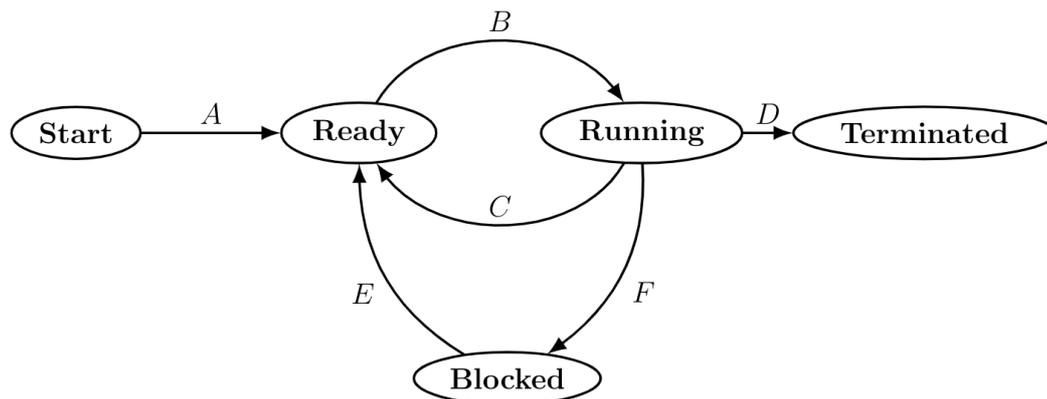
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gate2007-cse operating-system process-scheduling normal

Answer



In the following process state transition diagram for a uniprocessor system, assume that there are always some processes in the ready state:



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Now consider the following statements:

- I. If a process makes a transition D , it would result in another process making transition A immediately.
- II. A process P_2 in blocked state can make transition E while another process P_1 is in running state.
- III. The OS uses preemptive scheduling.
- IV. The OS uses non-preemptive scheduling.

Which of the above statements are TRUE?

- A. I and II
- B. I and III
- C. II and III
- D. II and IV

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gate2009-cse operating-system process-scheduling normal

Answer



Which of the following statements are true?

- I. Shortest remaining time first scheduling may cause starvation
- II. Preemptive scheduling may cause starvation

III. Round robin is better than FCFS in terms of response time

- A. I only
- B. I and III only
- C. II and III only
- D. I, II and III

gate2010-cse operating-system process-scheduling easy

Answer

5.15.21 Process Scheduling: GATE CSE 2011 | Question: 35 top

https://gateoverflow.in/1737



Consider the following table of arrival time and burst time for three processes P_0 , P_1 and P_2 .

Process	Arrival Time	Burst Time
P_0	0 ms	9
P_1	1 ms	4
P_2	2 ms	9

The pre-emptive shortest job first scheduling algorithm is used. Scheduling is carried out only at arrival or completion of processes. What is the average waiting time for the three processes?

- A. 5.0 ms
- B. 4.33 ms
- C. 6.33 ms
- D. 7.33 ms

gate2011-cse operating-system process-scheduling normal

Answer

5.15.22 Process Scheduling: GATE CSE 2012 | Question: 31 top

https://gateoverflow.in/1419



Consider the 3 processes, P_1 , P_2 and P_3 shown in the table.

Process	Arrival Time	Time Units Required
P_1	0	5
P_2	1	7
P_3	3	4

The completion order of the 3 processes under the policies FCFS and RR2 (round robin scheduling with CPU quantum of 2 time units) are

- A. FCFS: P_1, P_2, P_3 RR2: P_1, P_2, P_3
- B. FCFS: P_1, P_3, P_2 RR2: P_1, P_3, P_2
- C. FCFS: P_1, P_2, P_3 RR2: P_1, P_3, P_2
- D. FCFS: P_1, P_3, P_2 RR2: P_1, P_2, P_3

gate2012-cse operating-system process-scheduling normal

Answer

5.15.23 Process Scheduling: GATE CSE 2013 | Question: 10 top

https://gateoverflow.in/1419



A scheduling algorithm assigns priority proportional to the waiting time of a process. Every process starts with zero (the lowest priority). The scheduler re-evaluates the process priorities every T time units and decides the next process to schedule. Which one of the following is **TRUE** if the processes have no I/O operations and all arrive at time zero?

- A. This algorithm is equivalent to the first-come-first-serve algorithm.
- B. This algorithm is equivalent to the round-robin algorithm.
- C. This algorithm is equivalent to the shortest-job-first algorithm.
- D. This algorithm is equivalent to the shortest-remaining-time-first algorithm.

gate2013-cse operating-system process-scheduling normal

Answer

5.15.24 Process Scheduling: GATE CSE 2014 Set 1 | Question: 32 [top](#)

<https://gateoverflow.in/1803>



Consider the following set of processes that need to be scheduled on a single CPU. All the times are given in milliseconds.

Process Name	Arrival Time	Execution Time
A	0	6
B	3	2
C	5	4
D	7	6
E	10	3

Using the *shortest remaining time first* scheduling algorithm, the average process turnaround time (in msec) is _____.

gate2014-cse-set1 operating-system process-scheduling numerical-answers normal

Answer

5.15.25 Process Scheduling: GATE CSE 2014 Set 2 | Question: 32 [top](#)

<https://gateoverflow.in/1991>



Three processes A , B and C each execute a loop of 100 iterations. In each iteration of the loop, a process performs a single computation that requires t_c CPU milliseconds and then initiates a single I/O operation that lasts for t_{io} milliseconds. It is assumed that the computer where the processes execute has sufficient number of I/O devices and the OS of the computer assigns different I/O devices to each process. Also, the scheduling overhead of the OS is negligible. The processes have the following characteristics:

Process id	t_c	t_{io}
A	100 ms	500 ms
B	350 ms	500 ms
C	200 ms	500 ms

The processes A , B , and C are started at times 0, 5 and 10 milliseconds respectively, in a pure time sharing system (round robin scheduling) that uses a time slice of 50 milliseconds. The time in milliseconds at which process C would **complete** its first I/O operation is _____.

gate2014-cse-set2 operating-system process-scheduling numerical-answers normal

Answer

5.15.26 Process Scheduling: GATE CSE 2014 Set 3 | Question: 32 [top](#)

<https://gateoverflow.in/2066>



An operating system uses *shortest remaining time first* scheduling algorithm for pre-emptive scheduling of processes. Consider the following set of processes with their arrival times and CPU burst times (in milliseconds):

Process	Arrival Time	Burst Time
P1	0	12
P2	2	4
P3	3	6
P4	8	5

The average waiting time (in milliseconds) of the processes is _____.

gate2014-cse-set3 operating-system process-scheduling numerical-answers normal

Answer

5.15.27 Process Scheduling: GATE CSE 2015 Set 1 | Question: 46 [top](#)

<https://gateoverflow.in/8330>



Consider a uniprocessor system executing three tasks T_1 , T_2 and T_3 each of which is composed of an infinite sequence of jobs (or instances) which arrive periodically at intervals of 3, 7 and 20 milliseconds, respectively. The priority of each task is the inverse of its period, and the available tasks are scheduled in order of priority, which is the highest priority task scheduled first. Each instance of T_1 , T_2 and T_3 requires an execution time of 1, 2 and 4 milliseconds, respectively. Given that all tasks initially arrive at

the beginning of the 1st millisecond and task preemptions are allowed, the first instance of T_3 completes its execution at the end of _____ milliseconds.

gate2015-cse-set1 operating-system process-scheduling normal numerical-answers

Answer 

5.15.28 Process Scheduling: GATE CSE 2015 Set 3 | Question: 1 [top](#) 

<https://gateoverflow.in/8390>



The maximum number of processes that can be in *Ready* state for a computer system with n CPUs is :

- A. n
- B. n^2
- C. 2^n
- D. Independent of n

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gate2015-cse-set3 operating-system process-scheduling easy

Answer 

5.15.29 Process Scheduling: GATE CSE 2015 Set 3 | Question: 34 [top](#) 

<https://gateoverflow.in/8492>



For the processes listed in the following table, which of the following scheduling schemes will give the lowest average turnaround time?

Process	Arrival Time	Process Time
A	0	3
B	1	6
C	4	4
D	6	2

- A. First Come First Serve
- B. Non-preemptive Shortest job first
- C. Shortest Remaining Time
- D. Round Robin with Quantum value two

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gate2015-cse-set3 operating-system process-scheduling normal

Answer 

5.15.30 Process Scheduling: GATE CSE 2016 Set 1 | Question: 20 [top](#) 

<https://gateoverflow.in/39655>



Consider an arbitrary set of CPU-bound processes with unequal CPU burst lengths submitted at the same time to a computer system. Which one of the following process scheduling algorithms would minimize the average waiting time in the ready queue?

- A. Shortest remaining time first
- B. Round-robin with the time quantum less than the shortest CPU burst
- C. Uniform random
- D. Highest priority first with priority proportional to CPU burst length

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gate2016-cse-set1 operating-system process-scheduling normal

Answer 

5.15.31 Process Scheduling: GATE CSE 2016 Set 2 | Question: 47 [top](#) 

<https://gateoverflow.in/39625>



Consider the following processes, with the arrival time and the length of the CPU burst given in milliseconds. The scheduling algorithm used is preemptive shortest remaining-time first.

Process	Arrival Time	Burst Time
P_1	0	10
P_2	3	6
P_3	7	1
P_4	8	3

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The average turn around time of these processes is _____ milliseconds.

gate2016-cse-set2 operating-system process-scheduling normal numerical-answers

Answer 

5.15.32 Process Scheduling: GATE CSE 2017 Set 1 | Question: 24 [top](#)

<https://gateoverflow.in/118304>



Consider the following CPU processes with arrival times (in milliseconds) and length of CPU bursts (in milliseconds) as given below:

Process	Arrival Time	Burst Time
P_1	0	7
P_2	3	3
P_3	5	5
P_4	6	2

If the pre-emptive shortest remaining time first scheduling algorithm is used to schedule the processes, then the average waiting time across all processes is _____ milliseconds.

gate2017-cse-set1 operating-system process-scheduling numerical-answers

Answer 

5.15.33 Process Scheduling: GATE CSE 2017 Set 2 | Question: 51 [top](#)

<https://gateoverflow.in/118558>



Consider the set of process with arrival time (in milliseconds), CPU burst time (in milliseconds) and priority (0 is the highest priority) shown below. None of the process have I/O burst time

Process	Arrival Time	Burst Time	Priority
P_1	0	11	2
P_2	5	28	0
P_3	12	2	3
P_4	2	10	1
P_5	9	16	4

The average waiting time (in milli seconds) of all the process using premtive priority scheduling algorithm is _____

gate2017-cse-set2 operating-system process-scheduling numerical-answers

Answer 

5.15.34 Process Scheduling: GATE CSE 2019 | Question: 41 [top](#)

<https://gateoverflow.in/302807>



Consider the following four processes with arrival times (in milliseconds) and their length of CPU bursts (in milliseconds) as shown below:

Process	P_1	P_2	P_3	P_4
Arrival Time	0	1	3	4
CPU burst time	3	1	3	Z

These processes are run on a single processor using preemptive Shortest Remaining Time First scheduling algorithm. If the average waiting time of the processes is 1 millisecond, then the value of Z is _____

gate2019-cse numerical-answers operating-system process-scheduling

Answer 

5.15.35 Process Scheduling: GATE CSE 2020 | Question: 12 [top](#)

<https://gateoverflow.in/333219>



Consider the following statements about process state transitions for a system using preemptive scheduling.

- I. A running process can move to ready state.
- II. A ready process can move to running state.

- III. A blocked process can move to running state.
- IV. A blocked process can move to ready state.

Which of the above statements are TRUE?

- A. I, II, and III only
- B. II and III only
- C. I, II, and IV only
- D. I, II, III and IV only

gate2020-cse operating-system process-scheduling

Answer

5.15.36 Process Scheduling: GATE CSE 2020 | Question: 50 [top](#) <https://gateoverflow.in/333181>

Consider the following set of processes, assumed to have arrived at time 0. Consider the CPU scheduling algorithms Shortest Job First (SJF) and Round Robin (RR). For RR, assume that the processes are scheduled in the order P_1, P_2, P_3, P_4 .

Processes	P_1	P_2	P_3	P_4
Burst time (in ms)	8	7	2	4

If the time quantum for RR is 4 ms, then the absolute value of the difference between the average turnaround times (in ms) of SJF and RR (round off to 2 decimal places is _____)

gate2020-cse numerical-answers operating-system process-scheduling

Answer

5.15.37 Process Scheduling: GATE CSE 2021 Set 1 | Question: 25 [top](#) <https://gateoverflow.in/357426>

Three processes arrive at time zero with CPU bursts of 16, 20 and 10 milliseconds. If the scheduler has prior knowledge about the length of the CPU bursts, the minimum achievable average waiting time for these three processes in a non-preemptive scheduler (rounded to nearest integer) is _____ milliseconds.

gate2021-cse-set1 operating-system process-scheduling numerical-answers

Answer

5.15.38 Process Scheduling: GATE CSE 2021 Set 2 | Question: 14 [top](#) <https://gateoverflow.in/357526>

Which of the following statement(s) is/are correct in the context of CPU scheduling?

- A. Turnaround time includes waiting time
- B. The goal is to only maximize CPU utilization and minimize throughput
- C. Round-robin policy can be used even when the CPU time required by each of the processes is not known apriori
- D. Implementing preemptive scheduling needs hardware support

gate2021-cse-set2 multiple-selects operating-system process-scheduling

Answer

5.15.39 Process Scheduling: GATE IT 2005 | Question: 60 [top](#) <https://gateoverflow.in/3821>

We wish to schedule three processes P_1, P_2 and P_3 on a uniprocessor system. The priorities, CPU time requirements and arrival times of the processes are as shown below.

Process	Priority	CPU time required	Arrival time (hh:mm:ss)
P1	10 (highest)	20 sec	00 : 00 : 05
P2	9	10 sec	00 : 00 : 03
P3	8 (lowest)	15 sec	00 : 00 : 00

We have a choice of preemptive or non-preemptive scheduling. In preemptive scheduling, a late-arriving higher priority process can

preempt a currently running process with lower priority. In non-preemptive scheduling, a late-arriving higher priority process must wait for the currently executing process to complete before it can be scheduled on the processor.

What are the turnaround times (time from arrival till completion) of P_2 using preemptive and non-preemptive scheduling respectively?

- A. 30 sec, 30 sec
- B. 30 sec, 10 sec
- C. 42 sec, 42 sec
- D. 30 sec, 42 sec

gate2005-it operating-system process-scheduling normal

Answer

5.15.40 Process Scheduling: GATE IT 2006 | Question: 12 top

<https://gateoverflow.in/3551>



In the working-set strategy, which of the following is done by the operating system to prevent thrashing?

- I. It initiates another process if there are enough extra frames.
- II. It selects a process to suspend if the sum of the sizes of the working-sets exceeds the total number of available frames.

- A. I only
- B. II only
- C. Neither I nor II
- D. Both I and II

gate2006-it operating-system process-scheduling normal

Answer

5.15.41 Process Scheduling: GATE IT 2006 | Question: 54 top

<https://gateoverflow.in/3597>



The arrival time, priority, and duration of the CPU and I/O bursts for each of three processes P_1, P_2 and P_3 are given in the table below. Each process has a CPU burst followed by an I/O burst followed by another CPU burst. Assume that each process has its own I/O resource.

Process	Arrival Time	Priority	Burst duration (CPU)	Burst duration (I/O)	Burst duration (CPU)
P_1	0	2	1	5	3
P_2	2	3 (lowest)	3	3	1
P_3	3	1 (highest)	2	3	1

The multi-programmed operating system uses preemptive priority scheduling. What are the finish times of the processes P_1, P_2 and P_3 ?

- A. 11, 15, 9
- B. 10, 15, 9
- C. 11, 16, 10
- D. 12, 17, 11

gate2006-it operating-system process-scheduling normal

Answer

5.15.42 Process Scheduling: GATE IT 2007 | Question: 26 top

<https://gateoverflow.in/3459>



Consider n jobs $J_1, J_2 \dots J_n$ such that job J_i has execution time t_i and a non-negative integer weight w_i . The weighted mean completion time of the jobs is defined to be $\frac{\sum_{i=1}^n w_i T_i}{\sum_{i=1}^n w_i}$, where T_i is the completion time of job J_i . Assuming that there is only one processor available, in what order must the jobs be executed in order to minimize the weighted mean completion time of the jobs?

- A. Non-decreasing order of t_i
- B. Non-increasing order of w_i
- C. Non-increasing order of $w_i t_i$
- D. Non-increasing order of w_i/t_i

Answer

5.15.43 Process Scheduling: GATE IT 2008 | Question: 55 top

https://gateoverflow.in/3365



If the time-slice used in the round-robin scheduling policy is more than the maximum time required to execute any process, then the policy will

- A. degenerate to shortest job first
- B. degenerate to priority scheduling
- C. degenerate to first come first serve
- D. none of the above

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Answer

Answers: Process Scheduling

5.15.1 Process Scheduling: GATE CSE 1988 | Question: 2xa top

https://gateoverflow.in/93951



By the way the turnaround time should not be a metre to evaluate the performance of an OS .

But here they ask so

Undesirable is that : (i) long burst process are running first and smaller run after long.

4 votes

classroom.gateover
-- hem chandra joshi (2.9k points)

5.15.2 Process Scheduling: GATE CSE 1988 | Question: 2xb top

https://gateoverflow.in/93953



✓ "Waiting time" is one of the metric for deciding the schedule of processes. If the OS tries to minimize the average waiting time of the processes it'll follow the **Shortest Remaining Time First** algorithm which though reduces the average waiting time of processes can still cause a long burst time process to starve.

0 votes

-- Arjun Suresh (332k points)

5.15.3 Process Scheduling: GATE CSE 1990 | Question: 1-vi top

https://gateoverflow.in/83850



✓ **Highest response ratio next (HRRN)** scheduling is a non-preemptive discipline, similar to shortest job next (SJN), in which the priority of each job is dependent on its estimated run time, and also the amount of time it has spent waiting.

Jobs gain higher priority the longer they wait, which prevents indefinite waiting or in other words what we say starvation. In fact, the jobs that have spent a long time waiting compete against those estimated to have short run times.

$$\text{Priority} = \frac{\text{waiting time} + \text{estimated runtime}}{\text{estimated runtime}}$$

So, the conclusion is it gives priority to those processes which have less burst time (or execution time) but also takes care of the waiting time of longer processes, thus preventing starvation.

So, the answer is "*shorter, longer*"

48 votes

-- HABIB MOHAMMAD KHAN (67.5k points)

5.15.4 Process Scheduling: GATE CSE 1993 | Question: 7.10 top

https://gateoverflow.in/2298



✓ Answer: (C)

Execution order: *p q r s t p r t p r p r r r r r*

24 votes

-- Rajarshi Sarkar (27.9k points)



✓ Answer is Round Robin (RR), option (B).

Now question is Why RR is most suitable for time shared OS?

First of all we are discussing about **Time shared OS**, so obviously **We need to consider pre-emption**.

So, FCFS and Elevator these 2 options removed first, remain SJF and RR from two remaining options.

Now in case of pre-emptive SJF which is also known as shortest remaining time first or SRTF (where we can predict the next burst time using exponential averaging), SRTF would *NOT be optimal* than RR.

- There is **no starvation** in case of RR, since every process shares a time slice.
- But In case of SRTF, **there can be a starvation**, in **worse case** you may have the highest priority process, with a huge burst time have to wait. That means long process may have to wait indefinite time in case of SRTF.

That's why RR can be chosen over SRTF in case of time shared OS.

👍 44 votes

-- Bikram (58.4k points)

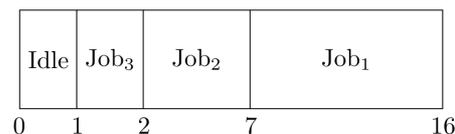


✓ Answer is (A).

Here, in option B and C they have given CPU idle time is 0 which is not possible as per schedule (B) and (C). So, (B) and (C) are eliminated.

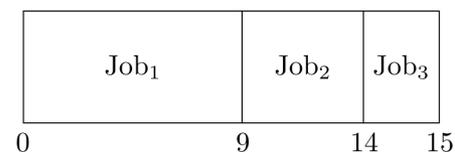
Now, lets see (A) and (D):

For (A),



So, idle time is between 0 and 1 which is 1 in case of option (A).

For option (D),



We can see that there is no idle time at all, but in option given idle time is 5, which is not matching with our chart so option (D) is eliminated.

Therefore, the correct sequence is option (A).

👍 43 votes

-- jayendra (6.7k points)



✓ The completion time of A will be 9 Unit.

Hence, option (D) is correct.

Here, is the sequence (Consider each block takes one time unit)

A	B	C	D	A	C	A	C	A
---	---	---	---	---	---	---	---	---

Completion time of A will be 9.

👍 29 votes

-- Muktinath Vishwakarma (23.9k points)



✓ Answer: (A)

Each process runs for q period and if there are n process: $p_1, p_2, p_3, \dots, p_n$.

Then p_1 's turn comes again when it has completed time quanta for remaining process p_2 to p_n , i.e, it would take at most $(n-1)q$ time.

So,, each process in round robin gets its turn after $(n-1)q$ time when we don't consider overheads but if we consider overheads then it would be $ns + (n-1)q$

So, we have $ns + (n-1)q \leq t$

👍 77 votes

-- Rajarshi Sarkar (27.9k points)



✓

- a. Here, all we need to do for minimizing response time is to run jobs in increasing order of burst time.
b. Schedule shorter jobs first, which will decrease the waiting time of longer jobs, and consequently average waiting time and average response time decreases.

- c.
6, 3, 5 and x .

If $X < 3 < 5 < 6$, then order should be $x, 3, 5, 6$

If $3 < 5 < 6 < x$, then order is $3, 5, 6, x$.

If $3 < x < 5 < 6$, then order is $3, x, 5, 6$. If $5 < x < 6$, then order is $3, 5, x, 6$.

Idea is that if you have $S_1 \rightarrow S_2$ then you create new semaphore a , assume that initial value of all semaphores is 0. Then S_2 thread will invoke $P(a)$ & will get blocked. When S_1 get executed, after that it'll do $V(a)$ which will enable S_2 to run. Do like this for all edges in graph.

Let me write program for it.

Begin

Semaphores a, b, c, d, e, f, g

ParBegin $S_1 V(a) V(b) V(c) V(d)$ Parent

ParBegin $P(a) S_2 V(e)$ Parent

ParBegin $P(b) S_3 V(f)$ Parent

ParBegin $P(c) P(e) S_4 V(g)$ Parent

ParBegin $P(d) P(f) P(g) S_5$ Parent

End

IF you reverse engineer this program you can get how this diagram came.

Parbegin Parent – Parallel execution

P – Down, V – Up

👍 30 votes

-- Akash Kanase (36k points)



✓ The partitions are $4k, 8k, 20k, 2k$, now due to the best-fit algorithm,

1. Size of $2k$ job will fit in $2k$ partition and execute for 4 unit
2. Size of $14k$ job will be fit in $20k$ partition and execute for 10 unit
3. Size of $3k$ job will be fit in $4k$ partition and execute for 2 unit
4. Size of $6k$ job will be fit in $8k$ partition now execute for 1 unit. All partitions are full.

And next job size of $10k$ (5) wait for the partition of $20k$ and after completion of no. 2 job, job no. 5 will be executed for 1 unit (10 to 11). Now, $20k$ is also waiting for a partition of $20k$ because it is the best fit for it. So after completion of job 5, it will be fit. So, it will execute for 8 unit which is 11 to 19. So, at 19 unit $20k$ job will be completed.

The answer should be 19 units.

32 votes

-- minal (13.1k points)

5.15.11 Process Scheduling: GATE CSE 2002 | Question: 1.22

https://gateoverflow.in/827



- A. Here we preempt when Time quantum is expired.
- B. We never preempt, so answer is (B) FIFO
- C. Here we preempt when process of higher priority arrives.
- D. Here we preempt when process of higher priority arrives or when time slice of higher level finishes & we need to move process to lower priority.

38 votes

-- Akash Kanase (36k points)

5.15.12 Process Scheduling: GATE CSE 2003 | Question: 77

https://gateoverflow.in/963



CPU utilization = CPU burst time/Total time.

FCFS:

- from 0 – 10 : process 1
- from 10 – 20 : process 2
- from 100 – 110 : process 1
- from 110 – 120 : process 2
-

So, in every 100 ms, CPU is utilized for 20 ms, CPU utilization = 20%

SRTF:

Same as FCFS as CPU burst time is same for all the processes

Static priority scheduling:

Suppose process 1 is having higher priority. Now, the scheduling will be same as FCFS. If process 2 is having higher priority, then the scheduling will be as FCFS with process 1 and process 2 interchanged. So, CPU utilization remains at 20%

Round Robin:

Time quantum given as 5 ms.

- from 0 – 5 : process 1
- from 5 – 10 : process 2
- from 10 – 15 : process 1
- from 15 – 20 : process 2
- from 105 – 110 : process 1
- from 110 – 115 : process 2
-

So, in 105 ms, 20 ms of CPU burst is there. So, utilization = 20/105 = 19.05%

19.05 is less than 20, so answer is (D).

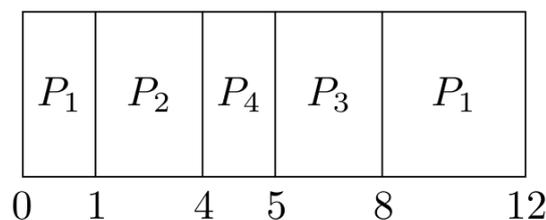
(Round robin with time quantum 10ms would have made the CPU utilization same for all the schedules)

132 votes

-- Arjun Suresh (332k points)

5.15.13 Process Scheduling: GATE CSE 2004 | Question: 46

https://gateoverflow.in/1043



Process	Waiting Time = (Turnaround Time - Burst time)	Turnaround Time = (Completion Time - Arrival Time)
P1	7	12
P3	0	3
P2	3	6
P4	0	1

Average turnaround time = $12 + 3 + 6 + 1/4 = 22/4 = 5.5$

Correct Answer: A

25 votes

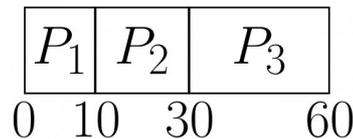
-- Pooja Palod (24.1k points)

5.15.14 Process Scheduling: GATE CSE 2006 | Question: 06, ISRO2009-14 top

<https://gateoverflow.in/885>



Processes execute as per the following Gantt chart



So, here only 2 switching possible (when we did not consider the starting and ending switching)

now here might be confusion that at $t = 2$ p_1 is preempted and check that available process have shortest job time or not, but he did not get anyone so it should not be consider as context switching.(same happened at $t = 6$)

Reference: <http://stackoverflow.com/questions/8997616/does-a-context-switch-occur-in-a-system-whose-ready-queue-has-only-one-process-a>(thanks to anurag_s)

Answer is (B)

References



53 votes

-- minal (13.1k points)

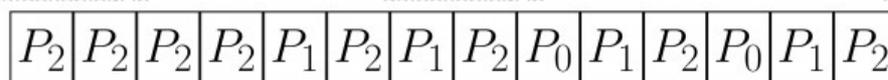
5.15.15 Process Scheduling: GATE CSE 2006 | Question: 64 top

<https://gateoverflow.in/1842>



A.

Gantt Chart is as follows.



Scheduling Table

P.ID	A.T	B.T	C.T	T.A.T.	W.T.
P0	0	2	12	12	10
P1	0	4	13	13	9
P2	0	8	14	14	6
TOTAL				39	25

A.T.= Arrival Time

B.T.= Burst Time

C.T.= Completion Time.

T.A.T.= Turn Around Time

W.T.= Waiting Time.

Average TAT = 39/3 = 13 units.

👍 37 votes

-- Gate Keeda (15.9k points)

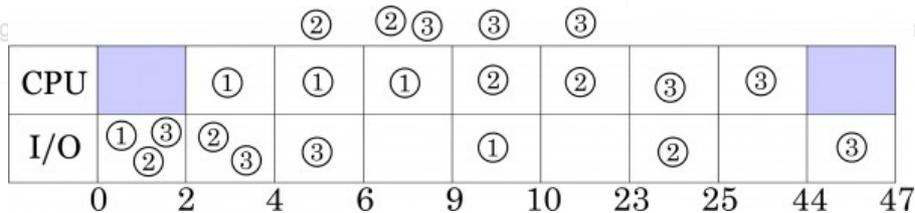
5.15.16 Process Scheduling: GATE CSE 2006 | Question: 65 top

<https://gateoverflow.in/1843>



✓

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$$\text{CPU Idle time} = \frac{2+3}{47} \times 100 = 10.6383\%$$

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Answer is option (B).

👍 74 votes

-- Amar Vashishth (25.2k points)

5.15.17 Process Scheduling: GATE CSE 2007 | Question: 16 top

<https://gateoverflow.in/1214>



✓

(A) is the answer.

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- http://en.wikipedia.org/wiki/Rate-monotonic_scheduling
- http://en.wikipedia.org/wiki/Gang_scheduling
- http://en.wikipedia.org/wiki/Fair-share_scheduling

References



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👍 37 votes

-- Arjun Suresh (332k points)

5.15.18 Process Scheduling: GATE CSE 2007 | Question: 55 top

<https://gateoverflow.in/1313>



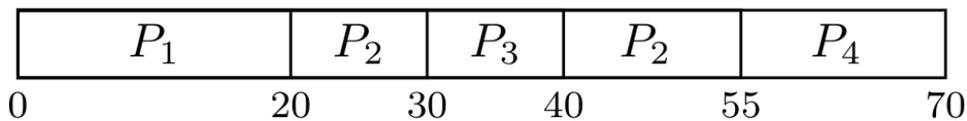
✓

The answer is (B).

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Gantt Chart

Waiting time for process P₂ = Completion time – Arrival time – burst time = 55–15–25 = 15

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👍 24 votes

-- Gate Keeda (15.9k points)

5.15.19 Process Scheduling: GATE CSE 2009 | Question: 32 top

<https://gateoverflow.in/1318>



- ✓ 1. If a process makes a transition D , it would result in another process making transition A immediately. - This is false. It is not said anywhere that one process terminates, another process immediately come into Ready state. It depends on availability of process to run & Long term Scheduler.
- 2. A process P_2 in blocked state can make transition E while another process P_2 is in running state. - This is correct. There is no dependency between running process & Process getting out of blocked state.
- 3. The OS uses preemptive scheduling. :- This is true because we got transition C from Running to Ready.
- 4. The OS uses non-preemptive scheduling. Well as previous statement is true, this becomes false.

So answer is (C) II and III .

👍 45 votes

-- Akash Kanase (36k points)

5.15.20 Process Scheduling: GATE CSE 2010 | Question: 25 [top](#)

<https://gateoverflow.in/2204>



✓ Answer is (D).

I. In SRTF ,job with the shorest CPU burst will be scheduled first bcz of this process with large CPU burst may suffer from starvation

II. In preemptive scheduling , suppose process P_1 is executing in CPU and after some time process P_2 with high priority then P_1 will arrive in ready queue then p_1 is prrempted and p_2 will brought into CPU for execution. In this way if process which is arriving in ready queue is of higher priority then p_1 , then p_1 is always preempted and it may possible that it suffer from starvation.

III. Round robin will give better response time then FCFS ,in FCFS when process is executing ,it executed upto its complete burst time, but in round robin it will execute upto time quantum.

👍 46 votes

-- neha pawar (3.3k points)

5.15.21 Process Scheduling: GATE CSE 2011 | Question: 35 [top](#)

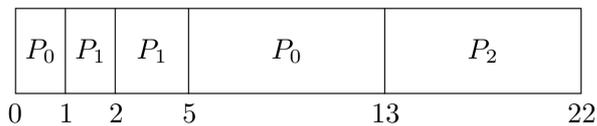
<https://gateoverflow.in/2137>



✓ Answer is (A).

5ms

Gantt Chart



$$\text{Average Waiting Time} = \frac{(0 + 4) + (0) + (11)}{3} = 5\text{ms.}$$

👍 26 votes

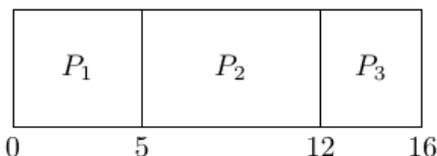
-- Sona Praneeth Akula (3.4k points)

5.15.22 Process Scheduling: GATE CSE 2012 | Question: 31 [top](#)

<https://gateoverflow.in/1749>



✓ **FCFS** First Come First Server



RR2

In Round Robin We are using the concept called Ready Queue.

Note

at $t = 2$,

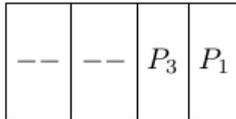
- P_1 finishes and sent to Ready Queue
- P_2 arrives and schedules P_2

This is the Ready Queue



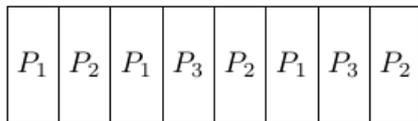
At $t = 3$

- P_3 arrives at ready queue



At $t = 4$

- P_1 is scheduled as it is the first process to arrive at Ready Queue



Option (C) is correct

43 votes

-- Akhil Nadh PC (16.5k points)

5.15.23 Process Scheduling: GATE CSE 2013 | Question: 10 [top](#)

<https://gateoverflow.in/1419>



- ✓ (B) Because here the quanta for round robin is T units, after a process is scheduled it gets executed for T time units and waiting time becomes least and it again gets chance when every other process has completed T time units.

50 votes

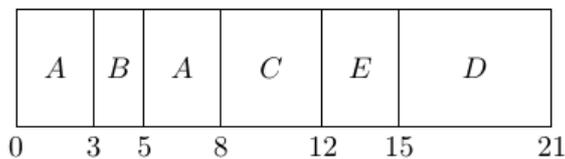
-- debanjan sarkar (2.9k points)

5.15.24 Process Scheduling: GATE CSE 2014 Set 1 | Question: 32 [top](#)

<https://gateoverflow.in/1803>



✓



$$\text{Average Turnaround Time} = \frac{(8-0) + (5-3) + (12-5) + (21-7) + (15-10)}{5}$$

$$= \frac{36}{5} = 7.2$$

So, answer is 7.2 ms

28 votes

-- Jay (831 points)

5.15.25 Process Scheduling: GATE CSE 2014 Set 2 | Question: 32 [top](#)

<https://gateoverflow.in/1991>



- ✓ Gantt chart : $ABCABCBCBC$
 C completes its CPU burst at = 500 milli second.

IO time = 500 milli second
 C completes 1st IO burst at $t = 500 + 500 = 1000$ ms

49 votes

-- Digvijay (44.9k points)

5.15.26 Process Scheduling: GATE CSE 2014 Set 3 | Question: 32

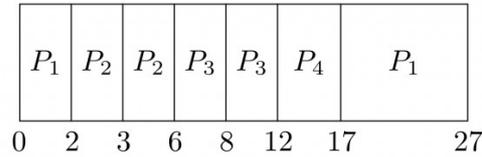
<https://gateoverflow.in/2066>



✓

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Gantt Chart

Process	Arrival Time	Burst Time	Completion Time	Turn Around Time	Waiting Time = CT - BT - AT
P1	0	12	27	27	15
P2	2	4	6	4	0
P3	3	6	12	9	3
P4	8	5	17	9	4

Average Waiting Time = $(15 + 0 + 3 + 4)/4 = 5.5$ msec

23 votes

-- Sourav Roy (2.9k points)

5.15.27 Process Scheduling: GATE CSE 2015 Set 1 | Question: 46

<https://gateoverflow.in/8390>



✓

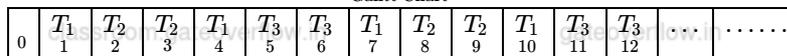
Answer is 12

T_1, T_2 and T_3 have infinite instances, meaning infinite burst times. Here, problem say Run " T_1 for 1 ms", " T_2 for 2 ms", and " T_3 for 4ms". i.e., every task is run in parts. Now for timing purpose we consider t for the end of cycle number t .

- $T_1 : 0, 3, 6, 9, 12, \dots \infty$ (T_1 repeats every 3 ms)
- $T_2 : 0, 7, 14, 21, \dots \infty$ (T_2 repeats every 7 ms)
- $T_3 : 0, 20, 40, 60, \dots \infty$ (T_3 repeats every 20 ms)

1. Priority of $T_1 = \frac{1}{3}$
2. Priority of $T_2 = \frac{1}{7}$
3. Priority of $T_3 = \frac{1}{20}$

Gantt Chart



At $t = 0$, No process is available
 At $t = 2$, T_2 runs because it has higher priority than T_3 and no instance of T_1 present
 At $t = 4$, We have T_1 arrive again and T_3 waiting but T_1 runs because it has higher priority
 At $t = 5$, T_3 runs because no instance of T_1 or T_2 is present
 At $t = 11$, T_3 runs because no instance of T_1 or T_2 is present
 At $t = 12$, T_3 continue run because no instance of T_1 or T_2 is present and first instance of T_3 completes

88 votes

-- Prashant Singh (47.2k points)

5.15.28 Process Scheduling: GATE CSE 2015 Set 3 | Question: 1

<https://gateoverflow.in/8390>



✓

(D) independent of n .

The number of processes that can be in READY state depends on the Ready Queue size and is independent of the number of CPU's.

54 votes

-- Arjun Suresh (332k points)



- ✓ Turn Around Time = Completion Time – Arrival Time

FCFS

Average turn around time = $[3 \text{ for A} + (2 + 6) \text{ for B} + (5 + 4) \text{ for C} + (7 + 2) \text{ for D}] / 4 = 7.25$

Non-preemptive Shortest Job First

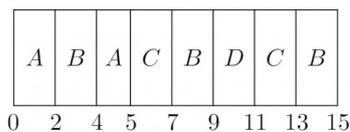
Average turn around time = $[3 \text{ for A} + (2 + 6) \text{ for B} + (3 + 2) \text{ for D} + (7 + 4) \text{ for C}] = 6.75$

Shortest Remaining Time

Average turn around time
= $[3 \text{ for A} + (2 + 1) \text{ for B} + (0 + 4) \text{ for C} + (2 + 2) \text{ for D} + (6 + 5) \text{ for remaining B}] / 4 = 6.25$

Round Robin

Average turn around time =
 $[2 \text{ for A (B comes after 1)}$
 $+ (1 + 2) \text{ for B \{C comes\}}$
 $+ (2 + 1) \text{ for A (A finishes after 3 cycles with turnaround time of } 2 + 3 = 5)$
 $+ (1 + 2) \text{ for C \{D comes\}}$
 $+ (3 + 2) \text{ for B}$
 $+ (3 + 2) \text{ for D (D finishes with turnaround time of } 3 + 2 = 5)$
 $+ (4 + 2) \text{ for C (C finishes with turnaround time of } 3 + 6 = 9)$
 $+ (4 + 2) \text{ for B (B finishes after turnaround time of } 3 + 5 + 6 = 14)]$
 $/ 4$
 $= 8.25$



Shortest Remaining Time First scheduling which is the preemptive version of the SJF scheduling is provably optimal for the shortest waiting time and hence always gives the best (minimal) turn around time (waiting time + burst time). So, we can directly give the answer here.

Correct Answer: C

👍 43 votes

-- Arjun Suresh (332k points)



- ✓ Answer should be (A) SRTF
 SJF minimizes average waiting time. Probably optimal.
 Now, here as all processes arrive at the same time, SRTF would be same as SJF. and hence, the answer.

Reference: <http://www.cs.columbia.edu/~junfeng/10sp-w4118/lectures/113-sched.pdf> See Slide 16,17 and 23

References

👍 50 votes

-- Abhilash Panicker (7.6k points)



- ✓ SRTF Preemptive hence,

$P_1 P_2 P_3 P_2 P_4 P_1$
 0 3 7 8 10 13 20

Process TAT=Completion time – Arrival time

P_1 20

P_2 7

P_3 1

P_4 5

AvgTAT= $33/4 = 8.25$

👍 39 votes

-- Shashank Chavan (2.4k points)

5.15.32 Process Scheduling: GATE CSE 2017 Set 1 | Question: 24 [top](#)

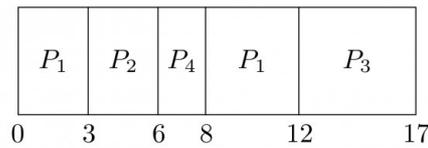
<https://gateoverflow.in/118304>



✓ [classroom.gateoverflow.in](#)

[gateoverflow.in](#)

[classroom.gateoverflow.in](#)



Gantt Chart

Process	Arrival Time	Burst Time	Completion Time	Turn Around Time	Waiting Time = CT - BT - AT
P1	0	7	12	12	5
P2	3	3	6	3	0
P3	5	5	17	12	7
P4	6	2	8	2	0

Average Waiting Time = $\frac{(5+0+7+0)}{4} = 3$ milliseconds

👍 35 votes

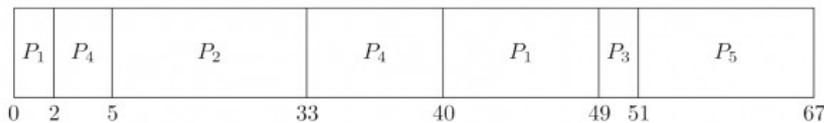
-- Ahwan Mishra (10.2k points)

5.15.33 Process Scheduling: GATE CSE 2017 Set 2 | Question: 51 [top](#)

<https://gateoverflow.in/118558>



✓ Gantt Chart for above problem looks like :



Waiting Time = Completion time – Arrival time – Burst Time

$$\sum AT = 0 + 5 + 12 + 2 + 9 = 28$$

$$\sum BT = 11 + 28 + 2 + 10 + 16 = 67$$

$$\sum CT = 67 + 51 + 49 + 40 + 33 = 240$$

$$\text{Waiting time} = 240 - 28 - 67 = 145$$

$$\text{Average Waiting Time} = \frac{145}{5} = 29 \text{ msec.}$$

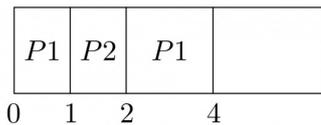
👍 55 votes

-- Manish Joshi (20.5k points)

5.15.34 Process Scheduling: GATE CSE 2019 | Question: 41 [top](#)

<https://gateoverflow.in/302807>





Till $t = 4$, the waiting time of $P1 = 1$ and $P2 = 0$ and $P3 = 1$ but $P3$ has not started yet.

Case 1:

Note that if $P4$ burst time is less than $P3$ then $P4$ will complete and after that $P3$ will complete. Therefore Waiting time of $P4$ should be 0. And total waiting time of $P3 = 1 + (\text{Burst time of } P4)$ because until $P4$ completes $P3$ does not get a chance.

$$\text{Then average waiting time} = \frac{1+0+(1+x)+0}{4} = 1$$

$$\frac{2+x}{4} = 1 \Rightarrow x = 2.$$

Case 2:

Note that if $P4$ burst time is greater than $P3$ then $P4$ will complete after $P3$ will complete. Therefore, Waiting time of $P3$ remains the same. And total waiting time of $P4 = (\text{Burst time of } P3)$ because until $P3$ completes $P4$ does not get a chance.

$$\text{Then average waiting time} = \frac{1+0+1+3}{4} = 1$$

$$\frac{5}{4} \neq 1 \Rightarrow \text{This case is invalid.}$$

Correct Answer: 2

31 votes

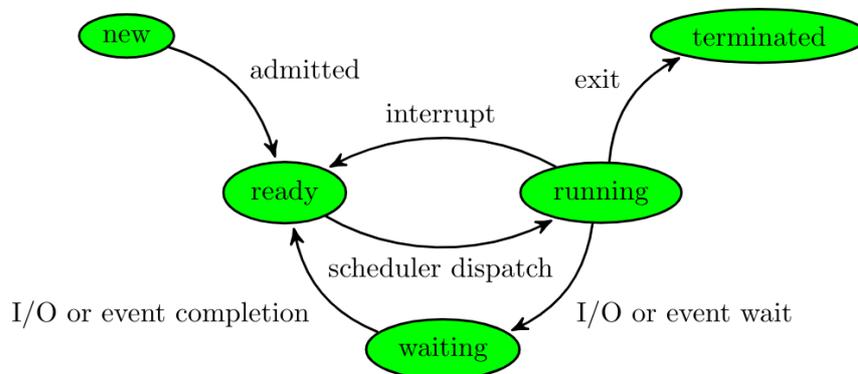
-- Shaik Masthan (50.4k points)

5.15.35 Process Scheduling: GATE CSE 2020 | Question: 12

<https://gateoverflow.in/333219>



A blocked process cannot go to running state directly. Except (III), every option is viable.



Answer-(C)

14 votes

-- Ayush Upadhyaya (28.4k points)

5.15.36 Process Scheduling: GATE CSE 2020 | Question: 50

<https://gateoverflow.in/333181>



SJF:

Process	Burst Time	Completion Time	Turn Around Time
P_1	8	21	21
P_2	7	13	13
P_3	2	2	2
P_4	4	6	6

$$\text{Average Turn-Around Time} : \frac{21+13+2+6}{4} = 10.5$$

RR:

Process	Burst Time	Completion Time	Turn Around Time
P_1	8	18	18
P_2	7	21	21
P_3	2	10	10
P_4	4	14	14

Average Turn-Around Time : $\frac{18+21+10+14}{4} = 15.75$

Absolute Difference = $|10.5 - 15.75| = 5.25$.

👍 5 votes

-- Aditya Patel (775 points)

5.15.37 Process Scheduling: GATE CSE 2021 Set 1 | Question: 25 [top](#)

<https://gateoverflow.in/357426>



✓ We get **minimum achievable average waiting time using SJF scheduling**.

Lets just name these processes for explanation purpose only as $A = 16, B = 20$ and $C = 10$.

Order them according to burst time as $C < A < B$

C will not wait for anyone, schedule first (wait time = 0)

A will wait for only C (wait time = 10)

B will wait for both C and A (wait time = 10 + 16)

Average wait time = $\frac{0+10+(10+16)}{3} = \frac{36}{3} = 12$.

No need to make any table or chart.

This is all for explaining purpose, you can actually ans this within 10-15 sec after reading the complete question.

👍 2 votes

-- Nikhil Dhama (2.5k points)

5.15.38 Process Scheduling: GATE CSE 2021 Set 2 | Question: 14 [top](#)

<https://gateoverflow.in/357528>



✓

- A. Turnaround time includes waiting time
 - TRUE. Turnaround Time = Waiting Time + Burst Time
- B. The goal is to only maximize CPU utilization and minimize throughput
 - FALSE. CPU scheduling must aim to maximize CPU utilization as well as throughput. Throughput of CPU scheduling is defined as the number of processes completed in unit time. SJF scheduling gives the highest throughput.
- C. Round-robin policy can be used even when the CPU time required by each of the processes is not known apriori
 - TRUE. Round-robin scheduling gives a fixed time quantum to each process and for this there is no requirement to know the CPU time of the process apriori (which is not the case say for shortest remaining time first).
- D. Implementing preemptive scheduling needs hardware support
 - TRUE. Preemptive scheduling needs hardware support to manage context switch which includes saving the execution state of the current process and then loading the next process.

Correct Answer: A;C;D

Reference: [Stanford Notes](#)

References



👍 1 votes

-- Arjun Suresh (332k points)

5.15.39 Process Scheduling: GATE IT 2005 | Question: 60 [top](#)

<https://gateoverflow.in/3821>



✓ Answer will be **(D)**.

TAT = Completion Time - Arrival Time.

The Gantt Chart for Non Preemptive scheduling will be (0)P3, (15)P1, (35)P2(45).

From above this can be inferred easily that completion time for P2 is 45, for P1 is 35 and P3 is 15.

Gantt Chart for Preemptive- (0)P3, (1)P3, (2)P3, (3)P2, (4)P2, (5)P1, (25)P2, (33)P3(45) .

Similarly take completion time from above for individual processes and subtract it from the Arrival time to get TAT.

31 votes

-- Gate Keeda (15.9k points)

5.15.40 Process Scheduling: GATE IT 2006 | Question: 12

https://gateoverflow.in/3551



✓ Extract from Galvin "If there are enough extra frames, another process can be initiated. If the sum of the working-set sizes increases, exceeding the total number of available frames, the operating system selects a process to suspend. The process's pages are written out (swapped), and its frames are reallocated to other processes. The suspended process can be restarted later."

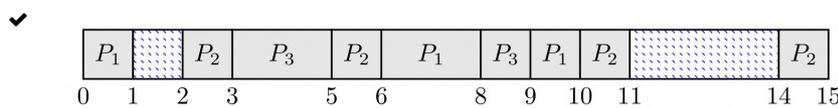
So Option (D)

57 votes

-- Danish (3.4k points)

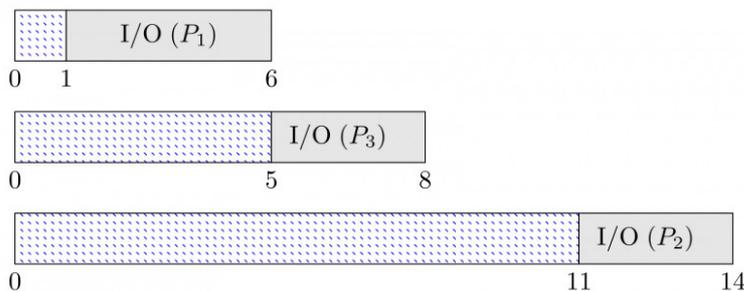
5.15.41 Process Scheduling: GATE IT 2006 | Question: 54

https://gateoverflow.in/3597



GIVEN : assuming that each process has its own i/o resource.

(GANTT CHART FOR I/O OF PROCESSOR P₁, P₂, P₃)



EXPLANATION :

Here, P₂ has the least priority and P₁ has the highest.

P₁ enters CPU at 0 and utilizes it for 1 time unit. Then it performs i/o for 5 time units.

Then P₂ enters at time unit 2 and requires 3 time units of CPU. But P₃ whose priority is greater than P₂ arrives at time unit 3.

So, P₂ IS **PREEMPTED** (only 1 unit of P₂ is done out of 3 units. Therefore 2 units of P₂ are left out) AND P₃ ACQUIRES THE CPU. Once P₃ finishes, P₂ enters the CPU to complete its pending 2 units job at time unit 5. AGAIN BY THEN P₁ finishes its i/o and arrives with a higher priority. Therefore of 2 units P₂ performs only one unit and the CPU is given to P₁. Then when P₁ is performing in CPU, P₃ completes its i/o and arrives with a higher priority. Thus the CPU is given to P₃ (1 UNIT IS USED). **P₃ FINISHES AT TIME UNIT 9. NOW PRIORITY OF P₁ IS MORE THAN P₂, SO, CPU IS USED BY P₁. P₁ FINISHES BY TIME UNIT 10. THEN CPU IS ALLOCATED FOR PROCESS P₂. P₂ PERFORMS REST OF ITS WORK AND FINISHES AT TIME UNIT 15.**

THEREFORE,

FINISH TIME OF P₁, P₂, P₃ ARE 10, 15 AND 9 RESPECTIVELY. ☺

Correct Answer: B

29 votes

-- Tejashwini B (139 points)



✓ Lets take an example:

Process	Weight	Execution time
P_1	1	3
P_2	2	5
P_3	3	2
p_4	4	4

For option 1 non decreasing t_i

$$= (3 \times 2 + 1 \times 5 + 4 \times 9 + 2 \times 14) / 10 = (6 + 5 + 36 + 28) / 10 = 7.5$$

For option 2 non increasing w_i

$$= (4 \times 4 + 3 \times 6 + 2 \times 11 + 1 \times 14) / 10 = (16 + 18 + 22 + 14) / 10 = 7$$

For option 3 non increasing $w_i t_i$

$$= (16 + 2 \times 9 + 3 \times 11 + 1 \times 14) / 10 = (16 + 18 + 33 + 14) / 10 = 8.1$$

For option 4 non increasing w_i / t_i

$$= (3 \times 2 + 4 \times 6 + 2 \times 11 + 1 \times 14) / 10 = (6 + 10 + 22 + 14) / 10 = 6.6$$

Minimum weighted mean obtained from non increasing w_i / t_i (**option D**)

The solution above is a classical example of greedy algorithm - that is at every point we choose the best available option and this leads to a global optimal solution. In this problem, we require to minimize the weighted mean completion time and the denominator in it is independent of the order of execution of the jobs. So, we just need to focus on the numerator and try to reduce it. Numerator here is a factor of the job weight and its completion time and since both are multiplied, our greedy solution must be

- to execute the shorter jobs first (so that remaining jobs have smaller completion time) and
- to execute highest weighted jobs first (so that it is multiplied by smaller completion time)

So, combining both we can use w_i / t_i to determine the execution order of processes - which must then be executed in non-increasing order.

👍 111 votes

-- khush tak (5.9k points)



✓ Answer is (C).

RR follows FCFS with time slice if time slice is larger than the max time required to execute any process then it is simply converged into fcfs as every process will finish in first cycle itself

👍 29 votes

-- sanjay (36.6k points)



A critical region is

- One which is enclosed by a pair of P and V operations on semaphores.
- A program segment that has not been proved bug-free.
- A program segment that often causes unexpected system crashes.
- A program segment where shared resources are accessed.

gate1987 operating-system process-synchronization

Answer [👍](#)

(a) Critical region	(p) Hoare's monitor
(b) Wait/Signal	(q) Mutual exclusion
(c) Working Set	(r) Principle of locality
(d) Deadlock	(s) Circular Wait

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match-the-following gate1990 operating-system process-synchronization

Answer

5.16.5 Process Synchronization: GATE CSE 1991 | Question: 11,a top

<https://gateoverflow.in/538>



Consider the following scheme for implementing a critical section in a situation with three processes P_i, P_j and P_k .

```
Pi;
repeat
  flag[i] := true;
  while flag [j] or flag[k] do
    case turn of
      j: if flag [j] then
        begin
          flag [i] := false;
          while turn != i do skip;
          flag [i] := true;
        end;
      k: if flag [k] then
        begin
          flag [i] := false;
          while turn != i do skip;
          flag [i] := true
        end
    end
  end
  critical section
  if turn = i then turn := j;
  flag [i] := false
  non-critical section
until false;
```

a. Does the scheme ensure mutual exclusion in the critical section? Briefly explain.

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gate1991 process-synchronization normal operating-system descriptive

Answer

5.16.6 Process Synchronization: GATE CSE 1991 | Question: 11,b top

<https://gateoverflow.in/4300>



Consider the following scheme for implementing a critical section in a situation with three processes P_i, P_j and P_k .

```
Pi;
repeat
  flag[i] := true;
  while flag [j] or flag[k] do
    case turn of
      j: if flag [j] then
        begin
          flag [i] := false;
          while turn != i do skip;
          flag [i] := true;
        end;
      k: if flag [k] then
        begin
          flag [i] := false;
          while turn != i do skip;
          flag [i] := true
        end
    end
  end
  critical section
  if turn = i then turn := j;
  flag [i] := false
  non-critical section
until false;
```

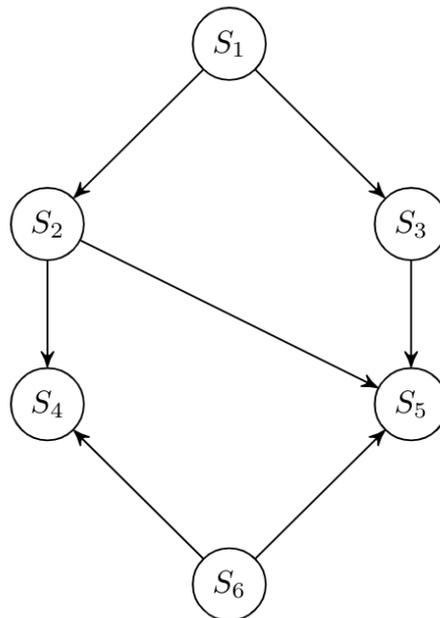
Is there a situation in which a waiting process can never enter the critical section? If so, explain and suggest modifications to the code to solve this problem

gate1991 process-synchronization normal operating-system descriptive

Answer



Write a concurrent program using `parbegin-parend` and semaphores to represent the precedence constraints of the statements S_1 to S_6 , as shown in figure below.



gate1993 operating-system process-synchronization normal descriptive

Answer



A. Draw a precedence graph for the following sequential code. The statements are numbered from S_1 to S_6

```

S1      read n
S2      i := 1
S3      if i > n next
S4      a(i) := i+1
S5      i := i+1
S6      next : write a(i)
  
```

B. Can this graph be converted to a concurrent program using `parbegin-parend` construct only?

gate1994 operating-system process-synchronization normal descriptive

Answer



Consider the following program segment for concurrent processing using semaphore operators P and V for synchronization. Draw the precedence graph for the statements S_1 to S_9 .

```

var
a,b,c,d,e,f,g,h,i,j,k : semaphore;
begin
cobegin
  begin S1; V(a); V(b) end;
  begin P(a); S2; V(c); V(d) end;
  begin P(c); S4; V(e) end;
  begin P(d); S5; V(f) end;
  begin P(e); P(f); S7; V(k) end;
  begin P(b); S3; V(g); V(h) end;
  begin P(g); S6; V(i) end;
  begin P(h); P(i); S8; V(j) end;
  begin P(j); P(k); S9 end;
coend
end;
  
```

gate1995 operating-system process-synchronization normal descriptive

Answer

5.16.10 Process Synchronization: GATE CSE 1996 | Question: 1.19, ISRO2008-61 top

<https://gateoverflow.in/2723>



A critical section is a program segment

- A. which should run in a certain amount of time
- B. which avoids deadlocks
- C. where shared resources are accessed
- D. which must be enclosed by a pair of semaphore operations, P and V

gate1996 operating-system process-synchronization easy isro2008

Answer

5.16.11 Process Synchronization: GATE CSE 1996 | Question: 2.19 top

<https://gateoverflow.in/2748>



A solution to the Dining Philosophers Problem which avoids deadlock is to

- A. ensure that all philosophers pick up the left fork before the right fork
- B. ensure that all philosophers pick up the right fork before the left fork
- C. ensure that one particular philosopher picks up the left fork before the right fork, and that all other philosophers pick up the right fork before the left fork
- D. None of the above

gate1996 operating-system process-synchronization normal

Answer

5.16.12 Process Synchronization: GATE CSE 1996 | Question: 21 top

<https://gateoverflow.in/2773>



The concurrent programming constructs fork and join are as below:

Fork <label> which creates a new process executing from the specified label

Join <variable> which decrements the specified synchronization variable (by 1) and terminates the process if the new value is not 0.

Show the precedence graph for $S_1, S_2, S_3, S_4,$ and S_5 of the concurrent program below.

```
N = 2
M = 2
Fork L3
Fork L4
S1
L1 : join N
S3
L2 : join M
S5
L3 : S2
Goto L1
L4 : S4
Goto L2
Next:
```

gate1996 operating-system process-synchronization normal descriptive

Answer

5.16.13 Process Synchronization: GATE CSE 1997 | Question: 6.8 top

<https://gateoverflow.in/2264>



Each Process $P_i, i = 1 \dots 9$ is coded as follows

```
repeat
  P(mutex)
  {Critical section}
  V(mutex)
forever
```

The code for P_{10} is identical except it uses $V(mutex)$ in place of $P(mutex)$. What is the largest number of processes that can be inside the critical section at any moment?

- A. 1
- B. 2
- C. 3
- D. None

gate1997 operating-system process-synchronization normal

Answer

5.16.14 Process Synchronization: GATE CSE 1997 | Question: 73 <https://gateoverflow.in/19703>



A concurrent system consists of 3 processes using a shared resource R in a non-preemptible and mutually exclusive manner. The processes have unique priorities in the range $1 \dots 3$, 3 being the highest priority. It is required to synchronize the processes such that the resource is always allocated to the highest priority requester. The pseudo code for the system is as follows.

Shared data

```
mutex:semaphore = 1; /* initialized to 1 */
process[3]:semaphore = 0; /*all initialized to 0 */
R_requested [3]:boolean = false; /*all initialized to false */
busy: boolean = false; /*initialized to false */
```

Code for processes

```
begin process
my-priority:integer;
my-priority:=___; /*in the range 1..3*/
repeat
  request_R(my-priority);
  P (proceed [my-priority]);
  {use shared resource R}
  release_R (my-priority);
forever
end process;
```

Procedures

```
procedure request_R(priority);
P(mutex);
if busy = true then
  R_requested [priority]:=true;
else
begin
  V(proceed [priority]);
  busy:=true;
end
V(mutex)
```

Give the pseudo code for the procedure `release_R`.

gate1997 operating-system process-synchronization descriptive

Answer

5.16.15 Process Synchronization: GATE CSE 1998 | Question: 1.30 <https://gateoverflow.in/1667>



When the result of a computation depends on the speed of the processes involved, there is said to be

- A. cycle stealing
- B. race condition
- C. a time lock
- D. a deadlock

gate1998 operating-system easy process-synchronization

Answer



A certain processor provides a 'test and set' instruction that is used as follows:

TSET register, flag

This instruction atomically copies flag to register and sets flag to 1. Give pseudo-code for implementing the entry and exit code to a critical region using this instruction.

gate1999 operating-system process-synchronization normal descriptive

Answer



Consider the following solution to the producer-consumer problem using a buffer of size 1. Assume that the initial value of count is 0. Also assume that the testing of count and assignment to count are atomic operations.

```

Producer:
Repeat
    Produce an item;
    if count = 1 then sleep;
    place item in buffer.
    count = 1;
    Wakeup(Consumer);
Forever
  
```

```

Consumer:
Repeat
    if count = 0 then sleep;
    Remove item from buffer;
    count = 0;
    Wakeup(Producer);
    Consume item;
Forever;
  
```

Show that in this solution it is possible that both the processes are sleeping at the same time.

gate1999 operating-system process-synchronization normal descriptive

Answer



Let $m[0] \dots m[4]$ be mutexes (binary semaphores) and $P[0] \dots P[4]$ be processes. Suppose each process $P[i]$ executes the following:

```

wait (m[i]); wait (m(i+1) mod 4);
.....
release (m[i]); release (m(i+1) mod 4);
  
```

This could cause

- Thrashing
- Deadlock
- Starvation, but not deadlock
- None of the above

gate2000-cse operating-system process-synchronization normal

Answer



a. Fill in the boxes below to get a solution for the reader-writer problem, using a single binary semaphore, mutex (initialized to 1) and busy waiting. Write the box numbers (1, 2 and 3), and their contents in your answer book.

L1:

```

int R = 0, W = 0;

Reader () {
    wait (mutex);
    if (W == 0) {
        R = R + 1;
        _____ (1)
    }
    else {
        _____ (2)
        goto L1;
    }
    .../* do the read*/
    wait (mutex);
    R = R - 1;
    signal (mutex);
}

```

L2:

```

Writer () {
    wait (mutex);
    if (_____) { _____ (3)
        signal (mutex);
        goto L2;
    }
    W=W+1;
    signal (mutex);
    .../*do the write*/
    wait (mutex);
    W=0;
    signal (mutex);
}

```

b. Can the above solution lead to starvation of writers?

gate2000-cse operating-system process-synchronization normal descriptive

Answer

5.16.20 Process Synchronization: GATE CSE 2001 | Question: 2.22 top <https://gateoverflow.in/740>



Consider Peterson's algorithm for mutual exclusion between two concurrent processes i and j. The program executed by process i is shown below.

```

repeat
    flag[i] = true;
    turn = j;
    while (P) do no-op;
    Enter critical section, perform actions, then
    exit critical section
    Flag[i] = false;
    Perform other non-critical section actions.
Until false;

```

For the program to guarantee mutual exclusion, the predicate P in the while loop should be

- A. flag[j] = true and turn = i
- B. flag[j] = true and turn = j
- C. flag[i] = true and turn = j
- D. flag[i] = true and turn = i

gate2001-cse operating-system process-synchronization normal

Answer

5.16.21 Process Synchronization: GATE CSE 2002 | Question: 18-a top <https://gateoverflow.in/871>



Draw the process state transition diagram of an OS in which (i) each process is in one of the five states: created, ready, running, blocked (i.e., sleep or wait), or terminated, and (ii) only non-preemptive scheduling is used by the OS. Label the transitions appropriately.

gate2002-cse operating-system process-synchronization normal descriptive

Answer

5.16.22 Process Synchronization: GATE CSE 2002 | Question: 18-b top <https://gateoverflow.in/205818>



The functionality of atomic TEST-AND-SET assembly language instruction is given by the following C function

```

int TEST-AND-SET (int *x)
{
    int y;

```

```

A1: y=*x;
A2: *x=1;
A3: return y;
}

```

- i. Complete the following C functions for implementing code for entering and leaving critical sections on the above TEST-AND-SET instruction.

```

int mutex=0;
void enter-cs()
{
    while(.....);
}
void leave-cs()
{ .....;
}

```

- ii. Is the above solution to the critical section problem deadlock free and starvation-free?
 iii. For the above solution, show by an example that mutual exclusion is not ensured if TEST-AND-SET instruction is not atomic?

gate2002-cse operating-system process-synchronization normal descriptive

Answer

5.16.23 Process Synchronization: GATE CSE 2002 | Question: 20

<https://gateoverflow.in/873>



The following solution to the single producer single consumer problem uses semaphores for synchronization.

```

#define BUFFSIZE 100
buffer buf[BUFFSIZE];
int first = last = 0;
semaphore b_full = 0;
semaphore b_empty = BUFFSIZE

void producer()
{
    while(1) {
        produce an item;
        p1:.....;
        put the item into buff (first);
        first = (first+1)%BUFFSIZE;
        p2: .....;
    }
}

void consumer()
{
    while(1) {
        c1:.....
        take the item from buf[last];
        last = (last+1)%BUFFSIZE;
        c2:.....;
        consume the item;
    }
}

```

- A. Complete the dotted part of the above solution.
 B. Using another semaphore variable, insert one line statement each immediately after $p1$, immediately before $p2$, immediately after $c1$ and immediately before $c2$ so that the program works correctly for multiple producers and consumers.

gate2002-cse operating-system process-synchronization normal descriptive

Answer

5.16.24 Process Synchronization: GATE CSE 2003 | Question: 80

<https://gateoverflow.in/964>



Suppose we want to synchronize two concurrent processes P and Q using binary semaphores S and T . The code for the processes P and Q is shown below.

Process P:	Process Q:
<pre> while(1){ W: print '0'; print '0'; X: } </pre>	<pre> while(1){ Y: print '1'; print '1'; Z: } </pre>

Synchronization statements can be inserted only at points W , X , Y , and Z

Which of the following will always lead to an output starting with '001100110011'?

- A. $P(S)$ at W , $V(S)$ at X , $P(T)$ at Y , $V(T)$ at Z , S and T initially 1
- B. $P(S)$ at W , $V(T)$ at X , $P(T)$ at Y , $V(S)$ at Z , S initially 1, and T initially 0
- C. $P(S)$ at W , $V(T)$ at X , $P(T)$ at Y , $V(S)$ at Z , S and T initially 1
- D. $P(S)$ at W , $V(S)$ at X , $P(T)$ at Y , $V(T)$ at Z , S initially 1, and T initially 0

gate2003-cse operating-system process-synchronization normal

Answer

5.16.25 Process Synchronization: GATE CSE 2003 | Question: 81 [top](#)

<https://gateoverflow.in/43574>



Suppose we want to synchronize two concurrent processes P and Q using binary semaphores S and T . The code for the processes P and Q is shown below.

Process P:	Process Q:
while(1) {	while(1) {
W:	Y:
print '0';	print '1';
print '0';	print '1';
X:	Z:
}	}

Synchronization statements can be inserted only at points W , X , Y , and Z

Which of the following will ensure that the output string never contains a substring of the form 01^n0 and 10^n1 where n is odd?

- A. $P(S)$ at W , $V(S)$ at X , $P(T)$ at Y , $V(T)$ at Z , S and T initially 1
- B. $P(S)$ at W , $V(T)$ at X , $P(T)$ at Y , $V(S)$ at Z , S and T initially 1
- C. $P(S)$ at W , $V(S)$ at X , $P(S)$ at Y , $V(S)$ at Z , S initially 1
- D. $V(S)$ at W , $V(T)$ at X , $P(S)$ at Y , $P(T)$ at Z , S and T initially 1

gate2003-cse operating-system process-synchronization normal

Answer

5.16.26 Process Synchronization: GATE CSE 2004 | Question: 48 [top](#)

<https://gateoverflow.in/1044>



Consider two processes P_1 and P_2 accessing the shared variables X and Y protected by two binary semaphores S_X and S_Y respectively, both initialized to 1. P and V denote the usual semaphore operators, where P decrements the semaphore value, and V increments the semaphore value. The pseudo-code of P_1 and P_2 is as follows:

P_1 :	P_2 :
While true do {	While true do {
$L_1 : \dots\dots$	$L_3 : \dots\dots$
$L_2 : \dots\dots$	$L_4 : \dots\dots$
$X = X + 1;$	$Y = Y + 1;$
$Y = Y - 1;$	$X = X - 1;$
$V(S_X);$	$V(S_Y);$
$V(S_Y);$	$V(S_X);$
}	}

In order to avoid deadlock, the correct operators at L_1 , L_2 , L_3 and L_4 are respectively.

- A. $P(S_Y), P(S_X); P(S_X), P(S_Y)$
- B. $P(S_X), P(S_Y); P(S_Y), P(S_X)$
- C. $P(S_X), P(S_X); P(S_Y), P(S_Y)$
- D. $P(S_X), P(S_Y); P(S_X), P(S_Y)$

Answer

5.16.27 Process Synchronization: GATE CSE 2006 | Question: 61 [top](#)<https://gateoverflow.in/1839>

The atomic *fetch-and-set* x, y instruction unconditionally sets the memory location x to 1 and fetches the old value of x in y without allowing any intervening access to the memory location x . Consider the following implementation of P and V functions on a binary semaphore S .

```
void P (binary_semaphore *s) {
    unsigned y;
    unsigned *x = &(s->value);
    do {
        fetch-and-set x, y;
    } while (y);
}

void V (binary_semaphore *s) {
    S->value = 0;
}
```

Which one of the following is true?

- The implementation may not work if context switching is disabled in P
- Instead of using *fetch-and-set*, a pair of normal load/store can be used
- The implementation of V is wrong
- The code does not implement a binary semaphore

Answer

5.16.28 Process Synchronization: GATE CSE 2006 | Question: 78 [top](#)<https://gateoverflow.in/1853>

Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and S be a binary semaphore with the usual P and V functions. Consider the following C implementation of a barrier with line numbers shown on left.

```
void barrier (void) {
```

```
1: P(S);
2: process_arrived++;
3: V(S);
4: while (process_arrived !=3);
5: P(S);
6: process_left++;
7: if (process_left==3) {
8:     process_arrived = 0;
9:     process_left = 0;
10: }
11: V(S);
```

```
}
```

The variables *process_arrived* and *process_left* are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

The above implementation of barrier is incorrect. Which one of the following is true?

- The barrier implementation is wrong due to the use of binary semaphore S
- The barrier implementation may lead to a deadlock if two barrier in invocations are used in immediate succession.
- Lines 6 to 10 need not be inside a critical section
- The barrier implementation is correct if there are only two processes instead of three.

Answer

5.16.29 Process Synchronization: GATE CSE 2006 | Question: 79 [top](#)<https://gateoverflow.in/43564>

Barrier is a synchronization construct where a set of processes synchronizes globally i.e., each process in the set arrives at the barrier and waits for all others to arrive and then all processes leave the barrier. Let the number of processes in the set be three and S be a binary semaphore with the usual P and V functions. Consider the following C implementation of a barrier with line numbers shown on left.

```
void barrier (void) {
```

```
1 P(S);
2 process_arrived++;
3 V(S);
4 while (process_arrived !=3);
5 P(S);
6 process_left++;
7 if (process_left==3) {
8 process_arrived = 0;
9 process_left = 0;
10 }
11 V(S);
```

```
}
```

The variables `process_arrived` and `process_left` are shared among all processes and are initialized to zero. In a concurrent program all the three processes call the barrier function when they need to synchronize globally.

Which one of the following rectifies the problem in the implementation?

- A. Lines 6 to 10 are simply replaced by `process_arrived--`
- B. At the beginning of the barrier the first process to enter the barrier waits until `process_arrived` becomes zero before proceeding to execute $P(S)$.
- C. Context switch is disabled at the beginning of the barrier and re-enabled at the end.
- D. The variable `process_left` is made private instead of shared

gate2006-cse operating-system process-synchronization normal

Answer 

5.16.30 Process Synchronization: GATE CSE 2007 | Question: 58 [top](#) 

<https://gateoverflow.in/1256>



Two processes, P_1 and P_2 , need to access a critical section of code. Consider the following synchronization construct used by the processes:

<pre>/* P1 */ while (true) { wants1 = true; while (wants2 == true); /* Critical Section */ wants1 = false; } /* Remainder section */</pre>	<pre>/* P2 */ while (true) { wants2 = true; while (wants1 == true); /* Critical Section */ wants2=false; } /* Remainder section */</pre>
--	--

Here, `wants1` and `wants2` are shared variables, which are initialized to false.

Which one of the following statements is TRUE about the construct?

- A. It does not ensure mutual exclusion.
- B. It does not ensure bounded waiting.
- C. It requires that processes enter the critical section in strict alteration.
- D. It does not prevent deadlocks, but ensures mutual exclusion.

gate2007-cse operating-system process-synchronization normal

Answer 

5.16.31 Process Synchronization: GATE CSE 2009 | Question: 33 [top](#) 

<https://gateoverflow.in/1319>



The `enter_CS()` and `leave_CS()` functions to implement critical section of a process are realized using test-and-set instruction as follows:

```
void enter_CS(X)
{
    while(test-and-set(X));
}

void leave_CS(X)
{
    X = 0;
}
```

In the above solution, X is a memory location associated with the CS and is initialized to 0. Now consider the following statements:

- I. The above solution to *CS* problem is deadlock-free
- II. The solution is starvation free
- III. The processes enter *CS* in FIFO order
- IV. More than one process can enter *CS* at the same time

Which of the above statements are TRUE?

- A. (I) only
- B. (I) and (II)
- C. (II) and (III)
- D. (IV) only

gate2009-cse operating-system process-synchronization normal

Answer 

5.16.32 Process Synchronization: GATE CSE 2010 | Question: 23 [top](#)

<https://gateoverflow.in/2202>



Consider the methods used by processes *P1* and *P2* for accessing their critical sections whenever needed, as given below. The initial values of shared boolean variables *S1* and *S2* are randomly assigned.

Method used by P1	Method used by P2
while ($S1 == S2$); Critical Section $S1 = S2$;	while ($S1 != S2$); Critical Section $S2 = \text{not}(S1)$;

Which one of the following statements describes the properties achieved?

- A. Mutual exclusion but not progress
- B. Progress but not mutual exclusion
- C. Neither mutual exclusion nor progress
- D. Both mutual exclusion and progress

gate2010-cse operating-system process-synchronization normal

Answer 

5.16.33 Process Synchronization: GATE CSE 2010 | Question: 45 [top](#)

<https://gateoverflow.in/2347>



The following program consists of 3 concurrent processes and 3 binary semaphores. The semaphores are initialized as $S0 = 1$, $S1 = 0$ and $S2 = 0$.

Process P0	Process P1	Process P2
while (true) { wait ($S0$); print '0'; release ($S1$); release ($S2$); }	wait ($S1$); release ($S0$);	wait ($S2$); release ($S0$);

How many times will process *P0* print '0'?

- A. At least twice
- B. Exactly twice
- C. Exactly thrice
- D. Exactly once

gate2010-cse operating-system process-synchronization normal

Answer 



$Fetch_And_Add(X,i)$ is an atomic Read-Modify-Write instruction that reads the value of memory location X , increments it by the value i , and returns the old value of X . It is used in the pseudocode shown below to implement a busy-wait lock. L is an unsigned integer shared variable initialized to 0. The value of 0 corresponds to lock being available, while any non-zero value corresponds to the lock being not available.

```
AcquireLock(L) {
    while (Fetch_And_Add(L,1))
        L = 1;
}

ReleaseLock(L) {
    L = 0;
}
```

This implementation

- fails as L can overflow
- fails as L can take on a non-zero value when the lock is actually available
- works correctly but may starve some processes
- works correctly without starvation

gate2012-cse operating-system process-synchronization normal

Answer [↕](#)



A shared variable x , initialized to zero, is operated on by four concurrent processes W, X, Y, Z as follows. Each of the processes W and X reads x from memory, increments by one, stores it to memory, and then terminates. Each of the processes Y and Z reads x from memory, decrements by two, stores it to memory, and then terminates. Each process before reading x invokes the P operation (i.e., wait) on a counting semaphore S and invokes the V operation (i.e., signal) on the semaphore S after storing x to memory. Semaphore S is initialized to two. What is the maximum possible value of x after all processes complete execution?

- 2
- 1
- 1
- 2

gate2013-cse operating-system process-synchronization normal

Answer [↕](#)



A certain computation generates two arrays a and b such that $a[i] = f(i)$ for $0 \leq i < n$ and $b[i] = g(a[i])$ for $0 \leq i < n$. Suppose this computation is decomposed into two concurrent processes X and Y such that X computes the array a and Y computes the array b . The processes employ two binary semaphores R and S , both initialized to zero. The array a is shared by the two processes. The structures of the processes are shown below.

Process X:

```
private i;
for (i=0; i < n; i++) {
    a[i] = f(i);
    ExitX(R, S);
}
```

Process Y:

```
private i;
for (i=0; i < n; i++) {
    EntryY(R, S);
    b[i] = g(a[i]);
}
```

Which one of the following represents the **CORRECT** implementations of ExitX and EntryY?

A. `ExitX(R, S) {`
`P(R);`
`V(S);`
`}`
`EntryY(R, S) {`
`P(S);`
`V(R);`
`}`

B. `ExitX(R, S) {`

```
V(R);
V(S);
}
EntryY(R, S) {
P(R);
P(S);
}
```

C.

```
ExitX(R, S) {
P(S);
V(R);
}
EntryY(R, S) {
V(S);
P(R);
}
```

D.

```
ExitX(R, S) {
V(R);
P(S);
}
EntryY(R, S) {
V(S);
P(R);
}
```

gate2013-cse operating-system process-synchronization normal

Answer

5.16.37 Process Synchronization: GATE CSE 2014 Set 2 | Question: 31 [top](#)

<https://gateoverflow.in/1990>



Consider the procedure below for the *Producer-Consumer* problem which uses semaphores:

```
semaphore n = 0;
semaphore s = 1;
```

```
void producer()
{
while(true)
{
produce();
semWait(s);
addToBuffer();
semSignal(s);
semSignal(n);
}
}
```

```
void consumer()
{
while(true)
{
semWait(s);
semWait(n);
removeFromBuffer();
semSignal(s);
consume();
}
}
```

Which one of the following is **TRUE**?

- A. The producer will be able to add an item to the buffer, but the consumer can never consume it.
- B. The consumer will remove no more than one item from the buffer.
- C. Deadlock occurs if the consumer succeeds in acquiring semaphore *s* when the buffer is empty.
- D. The starting value for the semaphore *n* must be 1 and not 0 for deadlock-free operation.

gate2014-cse-set2 operating-system process-synchronization normal

Answer

5.16.38 Process Synchronization: GATE CSE 2015 Set 1 | Question: 9 [top](#)

<https://gateoverflow.in/8121>



The following two functions *P1* and *P2* that share a variable *B* with an initial value of 2 execute concurrently.

<pre>P1() { C = B - 1; B = 2 * C; }</pre>	<pre>P2(){ D = 2 * B; B = D - 1; }</pre>
---	--

The number of distinct values that B can possibly take after the execution is _____.

gate2015-cse-set1 | operating-system | process-synchronization | normal | numerical-answers

Answer

5.16.39 Process Synchronization: GATE CSE 2015 Set 3 | Question: 10 <https://gateoverflow.in/8405>



Two processes X and Y need to access a critical section. Consider the following synchronization construct used by both the processes

Process X	Process Y
<pre> /* other code for process X */ while (true) { varP = true; while (varQ == true) { /* Critical Section */ varP = false; } } /* other code for process X */ </pre>	<pre> /* other code for process Y */ while (true) { varQ = true; while (varP == true) { /* Critical Section */ varQ = false; } } /* other code for process Y */ </pre>

Here $varP$ and $varQ$ are shared variables and both are initialized to false. Which one of the following statements is true?

- A. The proposed solution prevents deadlock but fails to guarantee mutual exclusion
- B. The proposed solution guarantees mutual exclusion but fails to prevent deadlock
- C. The proposed solution guarantees mutual exclusion and prevents deadlock
- D. The proposed solution fails to prevent deadlock and fails to guarantee mutual exclusion

gate2015-cse-set3 | operating-system | process-synchronization | normal

Answer

5.16.40 Process Synchronization: GATE CSE 2016 Set 2 | Question: 48 <https://gateoverflow.in/39600>



Consider the following two-process synchronization solution.

PROCESS 0	Process 1
<pre> Entry: loop while (turn == 1); (critical section) Exit: turn = 1; </pre>	<pre> Entry: loop while (turn == 0); (critical section) Exit: turn = 0; </pre>

The shared variable $turn$ is initialized to zero. Which one of the following is TRUE?

- A. This is a correct two- process synchronization solution.
- B. This solution violates mutual exclusion requirement.
- C. This solution violates progress requirement.
- D. This solution violates bounded wait requirement.

gate2016-cse-set2 | operating-system | process-synchronization | normal

Answer



A multithreaded program P executes with x number of threads and uses y number of locks for ensuring mutual exclusion while operating on shared memory locations. All locks in the program are *non-reentrant*, i.e., if a thread holds a lock l , then it cannot re-acquire lock l without releasing it. If a thread is unable to acquire a lock, it blocks until the lock becomes available. The *minimum* value of x and the *minimum* value of y together for which execution of P can result in a deadlock are:

- A. $x = 1, y = 2$
- B. $x = 2, y = 1$
- C. $x = 2, y = 2$
- D. $x = 1, y = 1$

gate2017-cse-set1

operating-system

process-synchronization

normal

Answer



Consider the following solution to the producer-consumer synchronization problem. The shared buffer size is N . Three semaphores *empty*, *full* and *mutex* are defined with respective initial values of $0, N$ and 1 . Semaphore *empty* denotes the number of available slots in the buffer, for the consumer to read from. Semaphore *full* denotes the number of available slots in the buffer, for the producer to write to. The placeholder variables, denoted by P, Q, R and S , in the code below can be assigned either *empty* or *full*. The valid semaphore operations are: *wait()* and *signal()*.

Producer:	Consumer:
do {	do {
wait (P);	wait (R);
wait (mutex);	wait (mutex);
//Add item to buffer	//consume item from buffer
signal (mutex);	signal (mutex);
signal (Q);	signal (S);
}while (1);	}while (1);

Which one of the following assignments to P, Q, R and S will yield the correct solution?

- A. $P : full, Q : full, R : empty, S : empty$
- B. $P : empty, Q : empty, R : full, S : full$
- C. $P : full, Q : empty, R : empty, S : full$
- D. $P : empty, Q : full, R : full, S : empty$

gate2018-cse

operating-system

process-synchronization

normal

Answer



Consider three concurrent processes P_1, P_2 and P_3 as shown below, which access a shared variable D that has been initialized to 100.

P_1	P_2	P_3
:	:	:
:	:	:
$D = D + 20$	$D = D - 50$	$D = D + 10$
:	:	:
:	:	:

The processes are executed on a uniprocessor system running a time-shared operating system. If the minimum and maximum possible values of D after the three processes have completed execution are X and Y respectively, then the value of $Y - X$ is

gate2019-cse

numerical-answers

operating-system

process-synchronization



Consider the following snapshot of a system running n concurrent processes. Process i is holding X_i instances of a resource R , $1 \leq i \leq n$. Assume that all instances of R are currently in use. Further, for all i , process i can place a request for at most Y_i additional instances of R while holding the X_i instances it already has. Of the n processes, there are exactly two processes p and q such that $Y_p = Y_q = 0$. Which one of the following conditions guarantees that no other process apart from p and q can complete execution?

- A. $X_p + X_q < \text{Min}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- B. $X_p + X_q < \text{Max}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- C. $\text{Min}(X_p, X_q) \geq \text{Min}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$
- D. $\text{Min}(X_p, X_q) \leq \text{Max}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\}$



The semaphore variables full, empty and mutex are initialized to 0, n and 1, respectively. Process P_1 repeatedly adds one item at a time to a buffer of size n , and process P_2 repeatedly removes one item at a time from the same buffer using the programs given below. In the programs, K , L , M and N are unspecified statements.

```

P1
while (1) {
    K;
    P(mutex);
    Add an item to the buffer;
    V(mutex);
    L;
}
    
```

```

P2
while (1) {
    M;
    P(mutex);
    Remove an item from the buffer;
    V(mutex);
    N;
}
    
```

The statements K , L , M and N are respectively

- A. P(full), V(empty), P(full), V(empty)
- B. P(full), V(empty), P(empty), V(full)
- C. P(empty), V(full), P(empty), V(full)
- D. P(empty), V(full), P(full), V(empty)



Given below is a program which when executed spawns two concurrent processes :

```

semaphore X := 0;
/* Process now forks into concurrent processes P1 & P2 */
    
```

P1	P2
repeat forever	repeat forever
V(X);	P(X);
Compute;	Compute;
P(X);	V(X);

Consider the following statements about processes $P1$ and $P2$:

- I. It is possible for process $P1$ to starve.
- II. It is possible for process $P2$ to starve.

Which of the following holds?

- A. Both (I) and (II) are true.
- B. (I) is true but (II) is false.
- C. (II) is true but (I) is false
- D. Both (I) and (II) are false

gate2005-it operating-system process-synchronization normal

Answer

5.16.47 Process Synchronization: GATE IT 2005 | Question: 42 top 9

<https://gateoverflow.in/3789>



Two concurrent processes P_1 and P_2 use four shared resources R_1, R_2, R_3 and R_4 , as shown below.

P1	P2
Compute;	Compute;
Use R_1 ;	Use R_1 ;
Use R_2 ;	Use R_2 ;
Use R_3 ;	Use R_3 ;
Use R_4 ;	Use R_4 ;

Both processes are started at the same time, and each resource can be accessed by only one process at a time. The following scheduling constraints exist between the access of resources by the processes:

- P_2 must complete use of R_1 before P_1 gets access to R_1 .
- P_1 must complete use of R_2 before P_2 gets access to R_2 .
- P_2 must complete use of R_3 before P_1 gets access to R_3 .
- P_1 must complete use of R_4 before P_2 gets access to R_4 .

There are no other scheduling constraints between the processes. If only binary semaphores are used to enforce the above scheduling constraints, what is the minimum number of binary semaphores needed?

- A. 1
- B. 2
- C. 3
- D. 4

gate2005-it operating-system process-synchronization normal

Answer

5.16.48 Process Synchronization: GATE IT 2006 | Question: 55 top 9

<https://gateoverflow.in/3598>



Consider the solution to the bounded buffer producer/consumer problem by using general semaphores S, F , and E . The semaphore S is the mutual exclusion semaphore initialized to 1. The semaphore F corresponds to the number of free slots in the buffer and is initialized to N . The semaphore E corresponds to the number of elements in the buffer and is initialized to 0.

Producer Process	Consumer Process
Produce an item;	Wait(E);
Wait(F);	Wait(S);
Wait(S);	Remove an item from the buffer;
Append the item to the buffer;	Signal(S);
Signal(S);	Signal(F);
Signal(E);	Consume the item;

Which of the following interchange operations may result in a deadlock?

- I. Interchanging Wait (F) and Wait (S) in the Producer process
 - II. Interchanging Signal (S) and Signal (F) in the Consumer process
- A. (I) only
 - B. (II) only
 - C. Neither (I) nor (II)
 - D. Both (I) and (II)

Answer 5.16.49 Process Synchronization: GATE IT 2007 | Question: 10 [top](#) <https://gateoverflow.in/3443> 

Processes P_1 and P_2 use `critical_flag` in the following routine to achieve mutual exclusion. Assume that `critical_flag` is initialized to `FALSE` in the main program.

```
get_exclusive_access ( )
{
    if (critical_flag == FALSE) {
        critical_flag = TRUE ;
        critical_region () ;
        critical_flag = FALSE;
    }
}
```

Consider the following statements.

- It is possible for both P_1 and P_2 to access `critical_region` concurrently.
- This may lead to a deadlock.

Which of the following holds?

- (i) is false (ii) is true
- Both (i) and (ii) are false
- (i) is true (ii) is false
- Both (i) and (ii) are true

Answer 5.16.50 Process Synchronization: GATE IT 2007 | Question: 56 [top](#) <https://gateoverflow.in/3498> 

Synchronization in the classical readers and writers problem can be achieved through use of semaphores. In the following incomplete code for readers-writers problem, two binary semaphores `mutex` and `wrt` are used to obtain synchronization

```
wait (wrt)
writing is performed
signal (wrt)
wait (mutex)
readcount = readcount + 1
if readcount = 1 then S1
S2
reading is performed
S3
readcount = readcount - 1
if readcount = 0 then S4
signal (mutex)
```

The values of S_1, S_2, S_3, S_4 , (in that order) are

- signal (`mutex`), wait (`wrt`), signal (`wrt`), wait (`mutex`)
- signal (`wrt`), signal (`mutex`), wait (`mutex`), wait (`wrt`)
- wait (`wrt`), signal (`mutex`), wait (`mutex`), signal (`wrt`)
- signal (`mutex`), wait (`mutex`), signal (`mutex`), wait (`mutex`)

Answer 5.16.51 Process Synchronization: GATE IT 2008 | Question: 53 [top](#) <https://gateoverflow.in/3363> 

The following is a code with two threads, producer and consumer, that can run in parallel. Further, S and Q are binary semaphores equipped with the standard P and V operations.

```
semaphore S = 1, Q = 0;
integer x;

producer:                consumer:
while (true) do          while (true) do
    P(S);                 P(Q);
    x = produce ();       consume (x);
    V(Q);                 V(S);
done                      done
```

Which of the following is TRUE about the program above?

- A. The process can deadlock
- B. One of the threads can starve
- C. Some of the items produced by the producer may be lost
- D. Values generated and stored in 'x' by the producer will always be consumed before the producer can generate a new value

gate2008-it operating-system process-synchronization normal

Answer

Answers: Process Synchronization

5.16.1 Process Synchronization: GATE CSE 1987 | Question: 1-xvi top  <https://gateoverflow.in/80362>

✓ A critical region is a program segment where shared resources are accessed, that's why we synchronize in the critical section.

PS: It is not necessary that we must use semaphore for critical section access (any other mechanism for mutual exclusion can also be used) and neither do sections enclosed by P and V operations are called critical sections.

Correct Answer : D.

34 votes

-- kirti singh (2.6k points)

5.16.2 Process Synchronization: GATE CSE 1987 | Question: 8a top  <https://gateoverflow.in/82433>

12 readers are reading means each reader has incremented the value of ar , making final value of ar to be 12.

Also each of the reader has executed $grantread$ in which rr is incremented to the value of ar making value of rr to be 12 finally.

31 writers are waiting means each writer on arrival has incremented the value of aw , making final value of aw to be 31.

Value of rw is incremented in $grantwrite$ only when value of rr is 0 but as 12 readers are already reading, this cannot happen, making value of rw to be 0.

Whenever read is granted in $grantread$, it means value of $reading$ semaphore is incremented to number of reader process using $V(reading)$. But before entering the read section, each reader decrements the $reading$ semaphore by 1 using $P(reading)$. The fact that 12 readers are reading means that 12 $V(reading)$ operations were performed and the 12 reader processes before entering read section have performed $P(reading)$ each to decrement the value of $reading$ semaphore to 0 again.

Since 12 readers are already reading, value of rr is non-zero because of which $V(writing)$ is not executed leaving the value of $writing$ semaphore to be 0.

NO, group of readers will not starve writers as readers execute $V(reading)$ in $grantread$ only when aw is 0 i.e. no writer is waiting allowing writer to execute first.

YES, writers can starve readers as writers execute $V(writing)$ without caring about readers (ar).

The solution is **incorrect** because:

In reader-writer problem, only single process needs to write at a time.

But in proposed solution, consider the case: When one process is writing and another write process arrives then it is also granted write using $V(writing)$ without caring about the first process which is still writing.

6 votes

-- Pratik Gawali (897 points)

5.16.3 Process Synchronization: GATE CSE 1988 | Question: 10iib top  <https://gateoverflow.in/94393>

✓ the above solution for the critical section isn't correct because it **satisfies Mutual exclusion and Progress** but it **violates the bounded waiting**.

Here is a sample run

```
suppose turn =j initially;
```

P_i runs its first statement then P_j runs its first statement then P_i run 2, 3, 4 statement, It will block on statement 4

Now P_j start executing its statements goes to critical section and then $flag[j] = false$

Now suppose P_j comes again immediately after execution then it will again execute its critical section and then $flag[j] = false$

Now if P_j is coming continuously then process P_i will suffer starvation.

the correct implementation (for Bounded waiting) is, at the exit section we have to update the turn variable at the exit section.

```
repeat
  flag[i]:= true;
  while turn != i
  do begin
    while flag [j] do skip
    turn:=i;
  end
  critical section
  flag[i]:=false;
  turn=j;
until false
```

10 votes

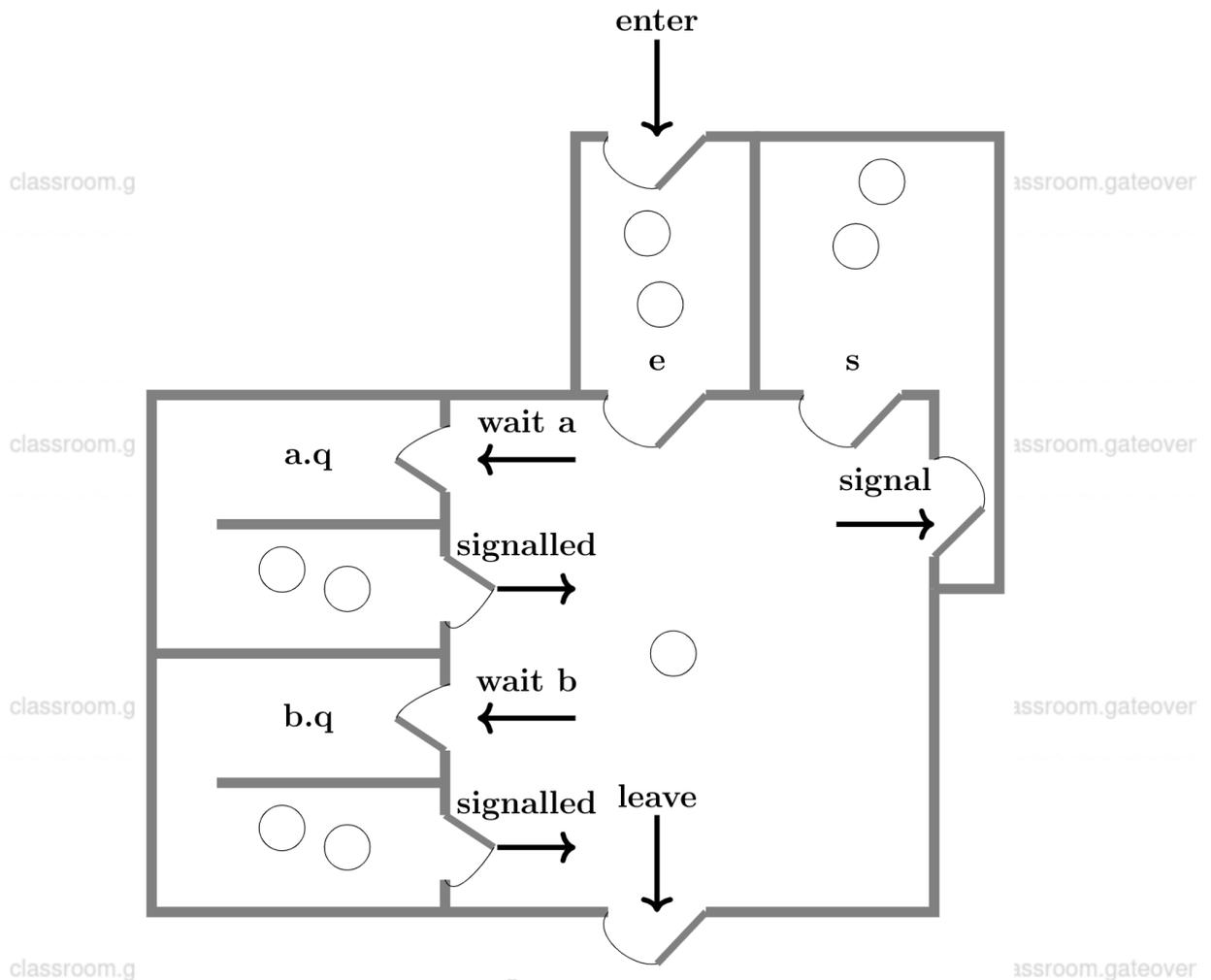
-- Aakashpatel (153 points)



✓ A. **Circular Wait** is one of the conditions for **deadlock**.

B. To avoid race conditions, the execution of **critical sections** must be **mutually exclusive** (e.g., at most one process can be in its critical section at any time).

C. Monitors using blocking condition variables are often called **Hoare-style monitors** or **signal-and-urgent-wait monitors**.



D. **locality** is commonly used to determine the number of assigned pages. The number of pages that meet the requirement of locality is called a **working set**.

(a) Critical region	(q) Mutual exclusion
(b) Wait/Signal	(p) Hoare's monitor
(c) Working Set	(r) Principle of locality
(d) Deadlock	(s) Circular Wait

22 votes

-- Pankaj Kumar (7.8k points)

5.16.5 Process Synchronization: GATE CSE 1991 | Question: 11,a top

<https://gateoverflow.in/538>



Pre-requisite: Assume all 3 processes have same implementation of code except flag variable indices changes accordingly for P_j and P_k and turn is shared variable among 3 process.

The condition:

while flag [j] or flag[k] do
ensures **mutual exclusion** as no process can enter critical section until flag of other processes is false.

Consider the case: turn = k

P_j wants to enter the critical section. It enters the critical section easily as

flag [k] or flag[i]

will be false and the loop will break.

Now, while P_j is executing in its critical section P_i arrives. For P_i :

flag [j] or flag[k]

will be true and it will enter the while loop. Since, turn = k, P_i will execute the loop:

while turn != i do skip;

Now, even if P_j finishes executing its critical section, it will execute:

if turn = j then turn := k;

which is false and thus the turn will remain k making P_i to execute an infinite loop until P_k arrives which can update turn = i.

So if P_k never arrives P_i will be waiting indefinitely.

8 votes

-- Pratik Gawali (897 points)

5.16.6 Process Synchronization: GATE CSE 1991 | Question: 11,b top

<https://gateoverflow.in/4300>



“the process which use critical section should hold turn variable otherwise other waiting process will wait for indefinite time if some process does not wants to enter in cs”

1. progress not satisfied
2. no deadlock

4 votes

-- indra kumar sahu (203 points)

5.16.7 Process Synchronization: GATE CSE 1993 | Question: 22 top

<https://gateoverflow.in/2319>



✓

```

parbegin
cl
begin s1 parbegin V(a) V(b) parend end

```

```

begin P(a) S2 parbegin V(c) V(e) parend end
begin P(b) S3 V(d) end
begin P(f) P(c) S4 end
begin P(g) P(d) P(e) S5 end
begin S6 parbegin V(f) V(g) parend end
parend

```

Here, the statement between parbegin and parend can execute in any order. But the precedence graph shows the order in which the statements should be executed. This strict ordering is achieved using the semaphores.

Initially all the semaphores are 0.

For S_1 there is no need of semaphore because it is the first one to execute.

Next S_2 can execute only when S_1 finishes. For this we have a semaphore a which on signal executed by S_1 , gets value 1. Now S_2 which is doing a wait on a can continue execution making $a = 0$;

Likewise this is followed for all other statements.

26 votes

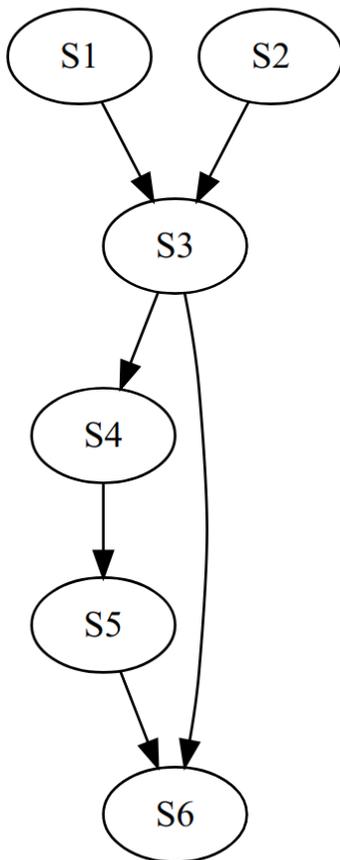
-- Sourav Roy (2.9k points)

5.16.8 Process Synchronization: GATE CSE 1994 | Question: 27

<https://gateoverflow.in/2523>



Following must be the correct precedence graph, S_1 and S_2 are independent, hence these can be executed in parallel.



For all those nodes which are independent we can execute them in parallel by creating a separate process for each node like S_1 and S_2 . There is an edge from S_3 to S_6 it means, until the process which executes S_3 finishes its work, we can't start the process which will execute S_6 .

For more understanding watch the following NPTEL lectures on process management:



Video:

[classroom.gateoverflow.in](https://www.gateoverflow.in)

[gateoverflow.in](https://www.gateoverflow.in)

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19 votes

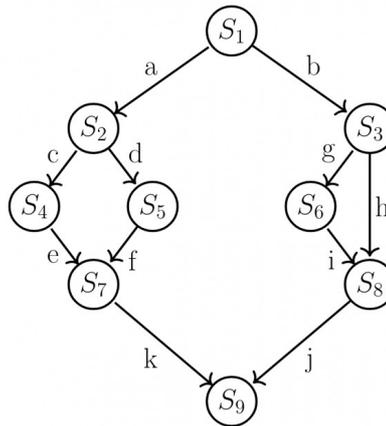
-- Manu Thakur (34k points)

5.16.9 Process Synchronization: GATE CSE 1995 | Question: 19 top

https://gateoverflow.in/2656



Precedence graph will be formed as:



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46 votes

-- neha pawar (3.3k points)

5.16.10 Process Synchronization: GATE CSE 1996 | Question: 1.19, ISRO2008-61 top

https://gateoverflow.in/2723



- A. There is no time guarantee for critical section.
- B. Critical section by default doesn't avoid deadlock. While using critical section, programmer must ensure deadlock is avoided.
- C. is the answer
http://en.wikipedia.org/wiki/Critical_section
- D. This is not a requirement of critical section. Only when semaphore is used for critical section management, this becomes a necessity. But, semaphore is just ONE of the ways for managing critical section.

References



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32 votes

-- Gate Keeda (15.9k points)

5.16.11 Process Synchronization: GATE CSE 1996 | Question: 2.19 top

https://gateoverflow.in/2748



Acc. to me it should be (C) because: according to condition, out of all, one philosopher will get both the forks. So, deadlock should not be there.

32 votes

-- Sneha Goel (819 points)

5.16.12 Process Synchronization: GATE CSE 1996 | Question: 21 top

https://gateoverflow.in/2773



✓ S_1, S_2, S_3, S_4 and S_5 are the statements to be executed.

Fork() creates a child to execute in parallel.

There will be 3 processes running concurrently.

One will execute S_1 , 2nd will execute S_2 and 3rd will execute S_4 .

Initially there is one process which started execution. Suppose this process name is P_0 .

It executes $N = 2, M = 2$ and after that it executes

Fork: L_3 ,

At L_3 there is a statement S_2 , Fork creates a new process suppose P_1 which starts its execution from level L_3 , means it starts executing S_2 .

P_0 executes fork L_4 , it creates another new process P_2 which starts its execution from level L_4 means it starts executing S_4 .

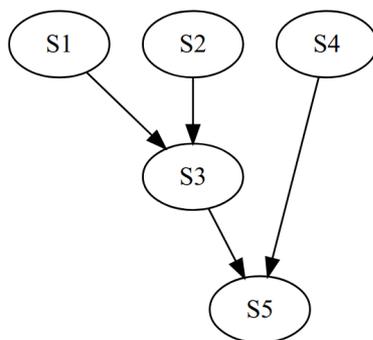
When P_1 finishes executing S_2 , it executes next line which is goto L_1 .

When P_2 finishes executing S_4 , it executes next line which is goto L_2 .

L_1 is executed by both processes P_0 (which has executed S_1) and P_1 (which has executed S_2)

Hence, S_1 and S_2 are combined together, as either P_0 or P_1 will terminate ($\because N = 2$) and only one process will continue its execution.

Similarly L_2 is executed by two processes P_2 (which executed S_4) and one of P_0 or P_1 (which executed S_3). So, S_4 and S_3 are joined together, as one of them will terminate ($\because M = 2$) and then one which survives will execute the final statement S_5 .



www.csc.lsu.edu/~rkannan/Fork_Cobegin_Creationtime.docx

<http://www.cis.temple.edu/~giorgio/old/cis307s96/readings/precedence.html>

References



👍 37 votes

-- Manu Thakur (34k points)

5.16.13 Process Synchronization: GATE CSE 1997 | Question: 6.8 top

<https://gateoverflow.in/2264>



✓ Answer is (D).

If initial value is 1//execute P_1 or P_{10} first

If initial value is 0, P_{10} can execute and make the value 1.

Since the both code (i.e. P_1 to P_9 and P_{10}) can be executed any number of times and code for P_{10} is

```
repeat
{
    V(mutex)
    C.S.
    V(mutex)
}
forever
```

Now, let me say P_1 is in Critical Section (CS)

then P_{10} comes executes the CS (up on mutex)

now P_2 comes (down on mutex)

now P_{10} moves out of CS (again binary semaphore will be 1)

now P_3 comes (down on mutex)
now P_{10} come (up on mutex)
now P_4 comes (down on mutex)
So, if we take P_{10} out of CS recursively all 10 process can be in CS at same time using Binary semaphore only.

67 votes

-- Kalpish Singhal (1.6k points)

5.16.14 Process Synchronization: GATE CSE 1997 | Question: 73 [top](#)

<https://gateoverflow.in/19703>



✓

```
procedure release_R(priority)
begin
P(mutex); //only one process must be executing the following part at a time
R_requested[priority] = false; //this process has requested,
//allocated the resource and now finished using it
for (i = 3 downto 1) //starting from highest priority process
begin
if R_requested[i] then
begin
V(proceed[i]); //Process i is now given access to resource
break;
end
end
if (!R_requested[0] && !R_requested[1] && !R_requested[2]) then
busy = false; //no process is waiting and so next incoming resource
//can be served without any wait
V(mutex); //any other process can now request/release resource
end
```

5 votes

-- Arjun Suresh (332k points)

5.16.15 Process Synchronization: GATE CSE 1998 | Question: 1.30 [top](#)

<https://gateoverflow.in/1667>



✓

When final result depends on ordering of processes it is called [Race condition](#).
Speed of processes corresponds to ordering of processes.

References



50 votes

-- Digvijay (44.9k points)

5.16.16 Process Synchronization: GATE CSE 1999 | Question: 20-a [top](#)

<https://gateoverflow.in/1519>



✓

1. TSET $R1$, flag
2. CMP $R1$, #0
3. JNZ Step1
4. $[CS]$
5. Store $\$M[Flag]$, #0

16 votes

-- Manu Thakur (34k points)

5.16.17 Process Synchronization: GATE CSE 1999 | Question: 20-b [top](#)

<https://gateoverflow.in/205817>



✓

1. **Run the Consumer Process**, Test the condition inside "if" (It is given that the testing of count is atomic operation), and since the Count value is initially 0, condition becomes True. **After Testing (But BEFORE "Sleep" executes in consumer process), Preempt the Consumer Process.**

2. **Now Run Producer Process completely** (All statements of Producer process). (Note that in Producer Process, 5th line of code, "Wakeup(Consumer);" will not cause anything because Consumer Process hasn't Slept yet (We had Preempted Consumer process before It could go to sleep). Now at the end of One pass of Producer process, Count value is now 1. So, Now if we again run Producer Process, "if" condition becomes true and **Producer Process goes to sleep.**

3. **Now run the Preempted Consumer process, And It also Goes to Sleep. (Because it executes the Sleep code).**

So, Now Both Processes are sleeping at the same time.

5.16.18 Process Synchronization: GATE CSE 2000 | Question: 1.21 top

https://gateoverflow.in/645



✓ P0 : m[0]; m[1]

P1 : m[1]; m[2]

P2 : m[2]; m[3]

P3 : m[3]; m[0]

P4 : m[4]; m[1]

p0 holding m0 waiting for m1

p1 holding m1 waiting for m2

p2 holding m2 waiting for m3

p3 holding m3 waiting for m0

p4 holding m4 waiting for m1

So its circular wait and no process can go into critical section even though its free hence

Answer: (B) Deadlock.

5.16.19 Process Synchronization: GATE CSE 2000 | Question: 20 top

https://gateoverflow.in/691



✓ There are four conditions that must be satisfied by any reader-writer problem solution

1. When a reader is reading, no writer must be allowed.
2. Multiple readers should be allowed.
3. When a writer is writing, no reader must be allowed.
4. Multiple writers (more than 1) should not be allowed.

Now, here mutex is a semaphore variable that will be used to modify the variables R and W in a mutually exclusive way.

The reader code should be like below

```
Reader()
L1: wait(mutex);
if(w==0){ //no Writer present, so allow Readers to come.

R=R+1; //increment the number of readers presently reading by 1.

signal(mutex); //Reader is allowed to enter,
//number of readers present "R"
//is incremented and now make mutex available so that other readers
//can come.
}
else{ //means some writer is writing,so release mutex, and try to
//gain access to mutex again by looping back to L1.

signal(mutex);
goto L1;
}
/*reading performed*/
wait(mutex);
R=R-1;
signal(mutex);
```

Value of variable R indicates the number of readers presently reading and the value of W indicates if 1, that some writer is present.

Writer code should be like below

```
Writer()
L2: wait(mutex);
if(R>0 || W!=0) //means if even one reader is present or one writer is writing
//deny access to this writer process and ask this to release
//mutex and loop back to L2.
{
signal(mutex);
goto L2;
}
//code will come here only if no writer or no reader was present.

W=1; //indicate that a writer has come.

signal(mutex); //now after updating W safely, release mutex, for other writers and
//readers to place their request.

/*Write performed*/
//writer will leave so change Value of W in a mutual exclusive manner.
wait(mutex);
W=0;
signal(mutex);
```

This will satisfy all requirements of the solution to the reader-writer problem.

(B) Yes, writers can starve. There can be the scenario that whenever a writer tries to enter, it finds some reader ($R! = 0$), or another writer process ($W! = 0$) and it can keep waiting forever. Bounded Waiting for the writer's processes is not ensured.

77 votes

-- Ayush Upadhyaya (28.4k points)

5.16.20 Process Synchronization: GATE CSE 2001 | Question: 2.22

<https://gateoverflow.in/740>



✓ Answer is Option B as used in Peterson's solution for Two Process Critical Section Problem which guarantees

1. Mutual Exclusion
2. Progress
3. Bounded Waiting

Both i and j are concurrent processes. So, whichever process wants to enter critical section(CS) that will execute the given code.

A process i shows it's interest to enter CS by setting $flag[i] = TRUE$ and only when i leaves CS it sets $flag[i] = FALSE$.

From this it's clear that when some process wants to enter CS then it must check value of $flag[]$ of the other process.

∴ " $flag[j] == TRUE$ " must be one condition that must be checked by process i .

Here, the $turn$ variable specifies whose turn is next i.e. which process can enter the CS next time. " $turn$ " acts like an unbiased scheduler, it ensures giving fair chance to the processes for execution. When a process sets $flag[]$ value, then $turn$ value is set equal to other process so that same process is not executed again (strict alteration when both processes are ready). i.e., usage of turn variable here ensures "Bounded Waiting" property.

Before entering CS every process needs to check whether other process has shown interest first and which process is scheduled by the $turn$ variable. If other process is not ready, $flag[other]$ will be false and the current process can enter the CS irrespective of the value of $turn$. Thus, the usage of $flag$ variable ensures "Progress" property.

If $flag[other] = TRUE$ and $turn = other$, then the process has to wait until one of the conditions becomes false. (because it is the turn of other process to enter CS). This ensures Mutual Exclusion.

Thus, ans is (b).

** one interesting point that can be observed is, if 2 processes wants to enter the CS, the process which executes " $turn = j$ " statement first is always the first one to enter the CS (after the other process executes $turn = j$).

35 votes

-- SameekshaGupta (787 points)

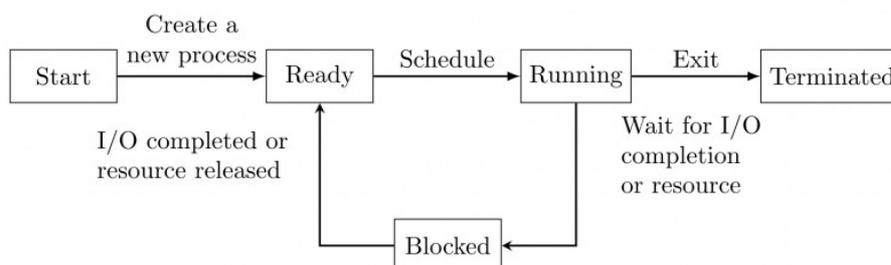
5.16.21 Process Synchronization: GATE CSE 2002 | Question: 18-a

<https://gateoverflow.in/871>



✓ Process state transition diagram for an OS which satisfy the below two criteria will be as follows:

- i. each process is in one of the five states: created, ready, running, blocked (i.e., sleep or wait), or terminated, and
- ii. only non-preemptive scheduling is used by the OS.



If in question it is asked about the preemptive scheduling then after the running state a process directly go to ready state.

15 votes

-- Shubhgupta (6.5k points)



Solution will be

```
void enter_cs()
{
    while(TestAndSet(&mutex));
}
void leave_cs()
{
    mutex=0;
}
```

Here there are two possible cases

Case (I) Test And Set is **not ATOMIC**: Consider a scenario where first, a process P1 comes, successfully executed enter_cs() and sets mutex to 1. Now, suppose another process P2 comes and executes while(TestAndSet(&mutex)) to gain access to CS.

Suppose after executing line

`y=*x=1` (mutex is one presently)

P2 gets preempted.

Now P1, resumes and sets mutex to 0.

Now P2 resumes, and executes remaining lines of TestAndSet,

`*x=1` (mutex is assigned value 1, value 0 lost permanently)

`return y; //1` will be returned.

Now, P2 and any other process which tries to execute enter_cs() will keep looping indefinitely. Now not even process P1 can come.

So, deadlock will occur eventually.

And Deadlock implies starvation so starvation is also there. (But starvation does not imply deadlock).

Yes, in this case, the mutual exclusion will not hold.

Suppose initially mutex=0.

Process P1 comes and executes the first iteration of while loop of enter_cs-->TestAndSet(&mutex)

`y=*x; //0` will be stored in y.

Suppose after executing this line of TestAndSet, P1 gets preempted and process P2 comes.

It also executes while loop of enter_cs() and executes TestAndSet(&mutex)

`y=*x; //0` will be stored because mutex was not changed to 1.

`*x=1; //mutex` changed to 1.

`return y. //0` will be returned.

Now P2 exits while loop and gains entry into CS.

Say, P1 resumes, and it executes the remaining line of TestAndSet and it returns 0.

P1, also exits while loop of enter_cs() and comes into CS.

Mutual exclusion is broken!!.

Case (II): TestAndSet is ATOMIC: Mutual exclusion will hold, because the first process to execute TestAndSet when mutex will be 0, will enter CS and rest all other processes will keep looping in the while loop of enter_cs().

Deadlock will not occur, because all other processes, which are looping in the while loop, will do so until mutex!=0. When the process which is in the CS leaves, it sets mutex=0, and one of the waiting processes which successfully finds mutex=0 AND executes the TestAndSet when mutex=0, will gain access to CS.

Starvation will occur, because as you can see in the code, no piece of code can be seen which is responsible for providing access to waiting processes in a fair shared manner. It might happen that one process always finds mutex to be 1, while rest all other processes are able to enter and leave CS, one at a time.

If some code is added to the leave-section(), which ensures that the waiting processes are given chance to enter CS in the order the request was placed, then starvation won't occur. In short, **here BOUNDED WAITING is not ensured**. If BOUNDED WAITING is ensured, STARVATION will not occur.

👍 14 votes

-- Ayush Upadhyaya (28.4k points)



- ✓ a) In Producer Consumer problem Producer produce item and makes the buffer full and after that Consumer consumes that item and makes the buffer empty

Here b_empty and b_full are two semaphore values

```
p1: P(Empty)
```

means, Producer have to wait only if buffer is full and it waits for consumer to remove at least one item. (See, Empty being initialized to BUFFSIZE)

```
p2: V(Full)
```

buffer is filled, now it gives signal to consumer that it can start consuming

```
c1: P(Full)
```

means here consumer have to wait only if buffer is empty, and it waits for Producer to fill the buffer

```
c2: V(Empty)
```

Now buffer is empty and Empty semaphore gives signal to the producer that it can start filling

It is same as giving water to a thirsty man.

Here u are giving water in a glass to that thirsty man, so u are producer here

and the man drinks and makes the glass empty, so he is consumer here

- b) If there are multiple user we can use mutex semaphore, so that exclusively one could enter in Critical section at a time. i.e.

```
p1: P(Empty)
   P(mutex)
p2: V(mutex)
   V(Full)
c1: P(Full)
   P(mutex)
c2: V(mutex)
   V(Empty)
```

PS: One thing to see is P(mutex) is after P(Full) and P(empty)- otherwise deadlock can happen when buffer is full and a producer gets mutex or if buffer is empty and a consumer gets mutex.

👍 27 votes

-- srestha (85.2k points)

5.16.24 Process Synchronization: GATE CSE 2003 | Question: 80 [top](#)

<https://gateoverflow.in/964>



- ✓ To get pattern 001100110011

Process P should be executed first followed by Process Q.

So, at Process P : $W P(S) \quad X V(T)$

And at Process Q : $Y P(T) \quad Z V(S)$

With $S = 1$ and $T = 0$ initially (only P has to be run first then only Q is run. Both processes run on alternate way starting with P)

So, answer is (B).

👍 30 votes

-- Pooja Palod (24.1k points)

5.16.25 Process Synchronization: GATE CSE 2003 | Question: 81 [top](#)

<https://gateoverflow.in/43574>



- ✓ output shouldn't contain substring of given form means no concurrent execution process P as well as Q. one semaphore is enough

So ans is (C)

👍 43 votes

-- Pooja Palod (24.1k points)

5.16.26 Process Synchronization: GATE CSE 2004 | Question: 48 [top](#)

<https://gateoverflow.in/1044>



- ✓ A. deadlock p1 : line1|p2:line3| p1: line2(block) |p2 :line4(block)

So, here p_1 want $s(x)$ which is held by p_2 and p_2 want $s(y)$ which is held by p_1 .
So, its **circular wait (hold and wait condition)**. So. there is **deadlock**.

- B. **deadlock** p_1 : line 1| p_2 line 3| p_1 : line 2(block) | p_2 : line 4(block)
Som here p_1 wants s_y which is held by p_2 and p_2 wants s_x which is held by p_1 . So its **circular wait (hold and wait) so, deadlock**.
- C. p_1 :line 1| p_2 : line 3| p_2 line 4 (block) | p_1 line 2 (block) here, p_1 wants s_x and p_2 wants s_y , but both will not be release by its process p_1 and p_2 because there is no way to release them. So, stuck in **deadlock**.
- D. p_1 :line 1 | p_2 : line 3 (block because need s_x) | p_1 line 2| p_2 : still block | p_1 : execute cs then up the value of s_x | p_2 :line 3 line 4(block need s_y)| p_1 up the s_y | p_2 :lin4 4 and easily get cs .
We can start from p_2 also, as I answered according only p_1 , but we get same answer.
So, **option (D)** is correct

👍 37 votes

-- minal (13.1k points)

5.16.27 Process Synchronization: GATE CSE 2006 | Question: 61 [top](#)

<https://gateoverflow.in/1839>



- A. **Answer** :- This is correct because the implementation may not work if context switching is disabled in P , then process which is currently blocked may never give control to the process which might eventually execute V . So Context switching is must !
- B. If we use normal load & Store instead of Fetch & Set there is good chance that more than one Process sees S .value as 0 & then mutual exclusion wont be satisfied. So this option is wrong.
- C. Here we are setting $S \rightarrow$ value to 0, which is correct. (As in fetch & Set we wait if value of $S \rightarrow$ value is 1. So implementation is correct. This option is wrong.
- D. I don't see why this code does not implement binary semaphore, only one Process can be in critical section here at a time. So this is binary semaphore & Option (D) is wrong

👍 90 votes

-- Akash Kanase (36k points)

5.16.28 Process Synchronization: GATE CSE 2006 | Question: 78 [top](#)

<https://gateoverflow.in/1853>



(B) is the correct answer.

Let 3 processes p_1, p_2, p_3 arrive at the barrier and after 4th step $process_arrived=3$ and the processes enter the barrier. Now suppose process p_1 executes the complete code and makes $process_left=1$, and tries to re-enter the barrier. Now, when it executes 4th step, $process_arrived=4$. p_1 is now stuck. At this point all other processes p_2 and p_3 also execute their section of code and resets $process_arrived=0$ and $process_left=0$. Now, p_2 and p_3 also try to re-enter the barrier making $process_arrived=2$. At this point all processes have arrived, but $process_arrived!=3$. Hence, no process can re-enter into the barrier, therefore DEADLOCK!!

👍 122 votes

-- GateMaster Prime (1.2k points)

5.16.29 Process Synchronization: GATE CSE 2006 | Question: 79 [top](#)

<https://gateoverflow.in/43564>



The implementation is incorrect because if two barrier invocations are used in immediate succession the system will fall into a DEADLOCK.

Here's how: Let all three processes make $process_arrived$ variable to the value 3, as soon as it becomes 3 previously stuck processes at the while loop are now free, to move out of the while loop.

But for instance let say one process moves out and has bypassed the next if statement & moves out of the barrier function and The SAME process is invoked again(its second invocation) while other processes are preempted still.

That process on its second invocation makes the $process_arrived$ variable to 4 and gets stuck forever in the while loop with other processes.

At this point of time they are in DEADLOCK. as only 3 processes were in the system and all are now stuck in while loop.

Q.79 answer = **option (B)**

option (A) here is false as there will always be a need for some process to help some other process to move out of that while loop waiting. Not all processes together can be said to be completed at a time.

option (C) is false. If context switch is disabled then the process who was stuck in while loop will remain there forever and no other process can play a role in bringing it out of there as Context Switch will be required to bring that other process in the system to do the job.

option (D) is false. everyone will be in a loop forever, if that happens.

option (B) is TRUE. at the beginning of the barrier the 1st process to enter Critical section should wait until process_arrived becomes zero(i.e. before starting its second invocation). this is to prevent it from making process_arrived value greater than 3 i.e. rectifying the flaw observed in Q.78

👍 41 votes

-- Amar Vashishth (25.2k points)

5.16.30 Process Synchronization: GATE CSE 2007 | Question: 58 [top](#)

<https://gateoverflow.in/1256>



- ✓ $P1$ can do $wants1 = true$ and then $P2$ can do $wants2 = true$. Now, both $P1$ and $P2$ will be waiting in the while loop indefinitely without any progress of the system - deadlock.

When $P1$ is entering critical section it is guaranteed that $wants1 = true$ ($wants2$ can be either true or false). So, this ensures $P2$ won't be entering the critical section at the same time. In the same way, when $P2$ is in critical section, $P1$ won't be able to enter critical section. So, mutual exclusion condition satisfied.

So, **D** is the correct choice.

Suppose $P1$ first enters critical section. Now suppose $P2$ comes and waits for CS by making $wants2 = true$. Now, $P1$ cannot get access to CS before $P2$ gets and similarly if $P1$ is in wait, $P2$ cannot continue more than once getting access to CS. Thus, there is a bound (of 1) on the number of times another process gets access to CS after a process requests access to it and hence bounded waiting condition is satisfied.

<https://cs.stackexchange.com/questions/63730/how-to-satisfy-bounded-waiting-in-case-of-deadlock>

References



👍 69 votes

-- Arjun Suresh (332k points)

5.16.31 Process Synchronization: GATE CSE 2009 | Question: 33 [top](#)

<https://gateoverflow.in/1319>



- ✓ The answer is (A) only.

The solution satisfies:

1. Mutual Exclusion as test-and-set is an indivisible (atomic) instruction (makes option (IV) wrong)
2. Progress as at initially X is 0 and at least one process can enter critical section at any time.

But no guarantee that a process eventually will enter CS and hence option (IV) is false. Also, no ordering of processes is maintained and hence III is also false.

So, eliminating all the 3 choices remains **A**.

👍 39 votes

-- Gate Keeda (15.9k points)

5.16.32 Process Synchronization: GATE CSE 2010 | Question: 23 [top](#)

<https://gateoverflow.in/2202>



- ✓ Answer is (A). In this mutual exclusion is satisfied, only one process can access the critical section at particular time but here progress will not be satisfied because suppose when $s1 = 1$ and $s2 = 0$ and process $p1$ is not interested to enter into critical section but $p2$ wants to enter critical section. $P2$ is not able to enter critical section in this as only when $p1$ finishes execution,

then only P_2 can enter (then only $s_1 = s_2$ condition be satisfied).

Progress will not be satisfied when any process which is not interested to enter into the critical section will not allow other interested process to enter into the critical section. When P_1 wants to enter the critical section it might need to wait till P_2 enters and leaves the critical section (or vice versa) which might never happen and hence progress condition is violated.

👍 77 votes

-- neha pawar (3.3k points)

5.16.33 Process Synchronization: GATE CSE 2010 | Question: 45 [top](#)

<https://gateoverflow.in/2347>



- ✓ First P_0 will enter the while loop as S_0 is 1. Now, it releases both S_1 and S_2 and one of them must execute next. Let that be P_1 . Now, P_0 will be waiting for P_1 to finish. But in the mean time P_2 can also start execution. So, there is a chance that before P_0 enters the second iteration both P_1 and P_2 would have done release (S_0) which would make S_1 1 only (as it is a binary semaphore). So, P_0 can do only one more iteration printing '0' two times.

If P_2 does release (S_0) only after P_0 starts its second iteration, then P_0 would do three iterations printing '0' three times.

If the semaphore had 3 values possible (an integer semaphore and not a binary one), exactly three '0's would have been printed.

Correct Answer: A, at least twice

👍 49 votes

-- Arjun Suresh (332k points)

5.16.34 Process Synchronization: GATE CSE 2012 | Question: 32 [top](#)

<https://gateoverflow.in/1750>



- ✓ A process acquires a lock only when $L = 0$. When L is 1, the process repeats in the while loop- there is no overflow because after each increment to L , L is again made equal to 1. So, the only chance of overflow is if a large number of processes (larger than `sizeof(int)`) execute the check condition of while loop but not $L = 1$, which is highly improbable.

Acquire Lock gets success only when Fetch_And_Add gets executed with $L = 0$. Now suppose P_1 acquires lock and make $L = 1$. P_2 waits for a lock iterating the value of L between 1 and 2 (assume no other process waiting for lock). Suppose when P_1 releases lock by making $L = 0$, the next statement P_2 executes is $L = 1$. So, value of L becomes 1 and no process is in critical section ensuring L can never be 0 again. Thus, (B) choice.

To correct the implementation we have to replace Fetch_And_Add with Fetch_And_Make_Equal_1 and remove $L = 1$ in `AcquireLock(L)`.

👍 163 votes

-- Arjun Suresh (332k points)

5.16.35 Process Synchronization: GATE CSE 2013 | Question: 34 [top](#)

<https://gateoverflow.in/1545>



- ✓ Since, initial value of semaphore is 2, two processes can enter critical section at a time- this is bad and we can see why.

Say, X and Y be the processes. X increments x by 1 and Z decrements x by 2. Now, Z stores back and after this X stores back. So, final value of x is 1 and not -1 and two Signal operations make the semaphore value 2 again. So, now W and Z can also execute like this and the value of x can be **2 which is the maximum possible** in any order of execution of the processes.

(If the semaphore is initialized to 1, processed would execute correctly and we get the final value of x as -2 .)

👍 91 votes

-- Arjun Suresh (332k points)

5.16.36 Process Synchronization: GATE CSE 2013 | Question: 39 [top](#)

<https://gateoverflow.in/1550>



- ✓
- A. X is waiting on R and Y is waiting on X . So, both cannot proceed.
- B. Process X is doing Signal operation on R and S without any wait and hence multiple signal operations can happen on the binary semaphore so Process Y won't be able to get exactly n successful wait operations. i.e., Process Y may not be able to complete all the iterations.
- C. Process X does Wait(S) followed by Signal(R) while Process Y does Signal(S) followed by Wait(R). So, this ensures that no two iterations of either X or Y can proceed without an iteration of the other being executed in between. i.e., this ensures that all n iterations of X and Y succeeds and hence the **answer**.
- D. Process X does Signal(R) followed by Wait(S) while Process Y does Signal(S) followed by Wait(R). There is a problem here that X can do two Signal(R) operation without a Wait(R) being done in between by Y . This happens in the following

scenario:

Process Y : Does Signal (S); Wait(R) fails; goes to sleep.

Process X : Does Signal(R); Wait(S) succeeds; In next iteration Signal(R) again happens;

So, this can result in some Signal operations getting lost as the semaphore is a binary one and thus Process Y may not be able to complete all the iterations. If we change the order of Signal(S) and Wait(R) in EntryY, then (D) option also can work.

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123 votes

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-- Arjun Suresh (332k points)

5.16.37 Process Synchronization: GATE CSE 2014 Set 2 | Question: 31 top ↗

https://gateoverflow.in/1990



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A. **False** : Producer = P (let), consumer = C (let) , once producer produce the item and put into the buffer. It will up the s and n to 1, so consumer can easily consume the item. So, option (A) Is false.

Code can be execute in this way: $P : 1\ 2\ 3\ 4\ 5$ | $C : 1\ 2\ 3\ 4\ 5$. So, consumer can consume item after adding the item to buffer.

B. **Is also False**, because whenever item is added to buffer means after producing the item, consumer can consume the item or we can say remove the item, if here statement is like the consumer will remove no more than one item from the buffer just after the removing one then it will be true (due $n = 0$ then, it will be blocked) but here only asking about the consumer will remove no more than one item from the buffer so, its false.

C. **is true** , statement says if consumer execute first means buffer is empty. Then execution will be like this.
 $C : 1$ (wait on s , $s = 0$ now) 2 (BLOCK $n = -1$) | $P : 1\ 2$ (wait on s which is already 0 so, it now block). So, c wants n which is held by producer or we can say up by only producer and P wants s , which will be up by only consumer. (**circular wait**) surely there is **deadlock**.

D. **is false**, if $n = 1$ then, also it will not free from deadlock.
For the given execution: $C : 1\ 2\ 3\ 4\ 5\ 1\ 2$ (BLOCK) | $P : 1\ 2$ (BLOCK) so, deadlock.
(here, 1 2 3 4 5 are the lines of the given code)

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Hence, answer is (C)

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70 votes

-- minal (13.1k points)

5.16.38 Process Synchronization: GATE CSE 2015 Set 1 | Question: 9 top ↗

https://gateoverflow.in/8121



3 distinct values {2, 3, 4}

$$P1 - P2 : B = 3$$

$$P2 - P1 : B = 4$$

$$P1 - P2 - P1 : B = 2$$

44 votes

-- Anoop Sonkar (4.1k points)

5.16.39 Process Synchronization: GATE CSE 2015 Set 3 | Question: 10 top ↗

https://gateoverflow.in/8405



When both processes try to enter critical section simultaneously, both are allowed to do so since both shared variables varP and varQ are true. So, clearly there is **NO mutual exclusion**. Also, **deadlock is prevented** because mutual exclusion is one of the necessary condition for deadlock to happen. Hence, answer is (A).

92 votes

-- Tanaya Pradhan (701 points)

5.16.40 Process Synchronization: GATE CSE 2016 Set 2 | Question: 48 top ↗

https://gateoverflow.in/39600



There is strict alternation i.e. after completion of process 0 if it wants to start again. It will have to wait until process 1 gives the lock.

This violates progress requirement which is, that no other process outside critical section can stop any other interested process from entering the critical section.

Hence the answer is that it violates the progress requirement.

The given solution does not violate bounded waiting requirement.

Bounded waiting is : There exists a bound, or limit, on the number of times other processes are allowed to enter their critical

sections after a process has made request to enter its critical section and before that request is granted.

Here there are only two processes and when process 0 enters CS, next entry is reserved for process 1 and vice-versa (strict alteration). So, bounded waiting condition is satisfied here.

Correct Answer: C

65 votes

-- bahirNaik (2.4k points)

5.16.41 Process Synchronization: GATE CSE 2017 Set 1 | Question: 27

<https://gateoverflow.in/118307>



✓ If we see definition of **reentrant Lock** :

In computer science, the **reentrant mutex (recursive mutex, recursive lock)** is particular type of mutual exclusion (mutex) device that may be locked multiple times by the same process/thread, **without causing a deadlock**.

https://en.wikipedia.org/wiki/Reentrant_mutex

A **Re-entrantLock** is *owned* by the thread last successfully locking, but not yet unlocking it. A thread invoking **lock** will return, successfully acquiring the lock, when the lock is not owned by another thread. **The method will return immediately if the current thread already owns the lock** <https://docs.oracle.com/javase/7/docs/api/java/util/concurrent/locks/ReentrantLock.html>

Reentrant property is provided, so that a process who owns a lock, can acquire same lock multiple times. Here it is non-reentrant as given, process cant own same lock multiple times. So if a thread tries to acquire already owned lock, will get blocked, and this is a deadlock.

Here, the answer is (D).

References



64 votes

-- harkirat31 (367 points)

5.16.42 Process Synchronization: GATE CSE 2018 | Question: 40

<https://gateoverflow.in/204114>



✓ Empty denotes number of Filled slots.

Full number of empty slots.

So, Producer must dealing with Empty and Consumer deals with Full

Producer must checks Full i.e. decrease Full by 1 before entering and Consumer check with Empty decrease Full by 1 before entering

So, (C) must be answer.

25 votes

-- Prashant Singh (47.2k points)

5.16.43 Process Synchronization: GATE CSE 2019 | Question: 23

<https://gateoverflow.in/302825>



✓ $D = 100$

Arithmetic operations are not ATOMIC.

These are three step process:

1. Read
2. Calculate
3. Update

Maximum value:

Run P2 for Read and Calculate. $D = 100$

Run P1 for read and calculate. $D = 100$

Run P2 update. $D = 50$

Run P1 update. $D = 110$

Run P2 read, calculate and update. $D = 130$

Minimum Value:

Run P1, P2, P3 for Read and Calculate. $D = 100$

Run P1 update. $D = 110$

Run P3 update. $D = 120$

Run P2 update. $D = 50$

Difference between Maximum and Minimum = $130 - 50 = 80$

👍 29 votes

-- Digvijay (44.9k points)

5.16.44 Process Synchronization: GATE CSE 2019 | Question: 39 [top](#) ▶

https://gateoverflow.in/302809



The process P , holds X_p resources currently and it doesn't request any new resources. Therefore after some time, it will completes it's execution and release the resources which it holds.

The process Q , holds X_q resources currently and it doesn't request any new resources. Therefore after some time, it will completes it's execution and release the resources which it holds.

Total available resources after completion of P and $Q = X_p + X_q$.

If these resources can not satisfy any process new requests, then no process will be able to completes it's execution.

$X_p + X_q < \text{Min}\{Y_k \mid 1 \leq k \leq n, k \neq p, k \neq q\} \implies$ delivers that no process going to completes except P and Q . Answer is (A)

👍 23 votes

-- Shaik Masthan (50.4k points)

5.16.45 Process Synchronization: GATE IT 2004 | Question: 65 [top](#) ▶

https://gateoverflow.in/3708



- ✓ P_1 is the producer. So, it must wait for full condition. But semaphore `full` is initialized to 0 and semaphore `empty` is initialized to n , meaning `full = 0` implies no item and `empty = n` implies space for n items is available. So, P_1 must wait for semaphore `empty - K - P(empty)` and similarly P_2 must wait for semaphore `full - M - P(full)`. After accessing the critical section (producing/consuming item) they do their respective V operation. Thus option D.

👍 49 votes

-- Arjun Suresh (332k points)

5.16.46 Process Synchronization: GATE IT 2005 | Question: 41 [top](#) ▶

https://gateoverflow.in/3788



- ✓ Check : [What is Starvation?](#)

Here P_2 can go in infinite waiting while process P_1 executes infinitely long.

Also, it can be the case that the Process P_1 starves for ∞ long time on the semaphore S, after it has successfully executed its critical section once, while P_2 executes infinitely long.

Both P_1 and P_2 can starve for ∞ long period of time.

Answer is **option A**.

References



👍 63 votes

-- Amar Vashishth (25.2k points)

5.16.47 Process Synchronization: GATE IT 2005 | Question: 42 [top](#) ▶

https://gateoverflow.in/3789



- ✓ Answer is (B)

It needs two semaphores. $X = 0, Y = 0$

P1	P2
P(X)	
	R1
	V(X)
R1	P(Y)
R2	
V(Y)	
P(X)	R2
	R3
	V(X)
R3	P(Y)
R4	
V(Y)	
	R4

85 votes

-- Sandeep_Uniyal (6.5k points)

5.16.48 Process Synchronization: GATE IT 2006 | Question: 55 [top 5](#)

<https://gateoverflow.in/3598>



- ✓ Suppose the slots are full $\rightarrow F = 0$. Now, if $\text{Wait}(F)$ and $\text{Wait}(S)$ are interchanged and $\text{Wait}(S)$ succeeds, The producer will wait for $\text{Wait}(F)$ which is never going to succeed as Consumer would be waiting for $\text{Wait}(S)$. So, deadlock can happen.

If $\text{Signal}(S)$ and $\text{Signal}(F)$ are interchanged in Consumer, deadlock won't happen. It will just give priority to a producer compared to the next consumer waiting.

So, answer (A)

62 votes

-- Arjun Suresh (332k points)

5.16.49 Process Synchronization: GATE IT 2007 | Question: 10 [top 5](#)

<https://gateoverflow.in/3443>



- ✓ (C) Both process can run the critical section concurrently. Lets say p_1 starts and it enters inside if clause and just after its entertence and before execution of $\text{critical_flag} = \text{TRUE}$, a context switch happens and p_2 also gets entrance since the flag is still false. So, now both process are in critical section! So, (i) is true. (ii) is false there is no way that flag is true and no process' are inside the if clause, if someone enters the critical section, it will definitely make $\text{flag} = \text{false}$. So. no. deadlock.

57 votes

-- Vicky Bajoria (4.1k points)

5.16.50 Process Synchronization: GATE IT 2007 | Question: 56 [top 5](#)

<https://gateoverflow.in/3498>



- ✓ Answer is (C)

S1: if readcount is 1 i.e., some reader is reading, DOWN on wrt so that no writer can write.

S2: After readcount has been updated, UP on mutex.

S3: DOWN on mutex to update readcount

S4: If readcount is zero i.e., no reader is reading, UP on wrt to allow some writer to write

26 votes

-- Sandeep_Uniyal (6.5k points)

5.16.51 Process Synchronization: GATE IT 2008 | Question: 53 [top 5](#)

<https://gateoverflow.in/3363>



- ✓ Producer: consumer: while (true) do while (true) do 1 $P(S)$; 1 $P(Q)$; 2 $x = \text{produce}()$; 2 $\text{consume}(x)$; 3 $V(Q)$; 3 $V(S)$; done done

Lets explain the working of this code.

It is mentioned that P and C execute parallelly.

P : 123

1. S value is 1, down on 1 makes it 0. Enters the statement 2.

2. Item produced.
3. Up on Q is done (Since the queue of Q is empty, value of Q up to 1).

This being an infinite while loop should infinitely iterate.

In the next iteration of while loop $st1$ is executed.

But S is already 0, further down on 0 sends P to blocked list of S . P is blocked.

C Consumer is scheduled.

Down on Q . value makes $Q.value = 0$;

Enters the statement 2, consumes the item.

Up on S , now instead of changing the value of S . value to 1, wakes up the blocked process on Q 's queue. Hence process P is awoken. P resumes from statement 2, since it was blocked at statement 1. So, P now produces the next item.

So, consumer consumes an item before producer produces the next item.

(D) Answer

(A) Deadlock cannot happen as both producer and consumer are operating on different semaphores (no hold and wait)

(B) No starvation happens because there is alternation between P and Consumer. Which also makes them have bounded waiting.

👍 34 votes

-- Sourav Roy (2.9k points)

5.17

Resource Allocation (26) top ⬆

5.17.1 Resource Allocation: GATE CSE 1988 | Question: 11 top ⬆

https://gateoverflow.in/94397



A number of processes could be in a deadlock state if none of them can execute due to non-availability of sufficient resources. Let $P_i, 0 \leq i \leq 4$ represent five processes and let there be four resource types $r_j, 0 \leq j \leq 3$. Suppose the following data structures have been used.

Available: A vector of length 4 such that if $Available[i] = k$, there are k instances of resource type r_j available in the system.

Allocation: A 5×4 matrix defining the number of each type currently allocated to each process. If $Allocation[i, j] = k$ then process p_i is currently allocated k instances of resource type r_j .

Max: A 5×4 matrix indicating the maximum resource need of each process. If $Max[i, j] = k$ then process p_i , may need a maximum of k instances of resource type r_j in order to complete the task.

Assume that system allocated resources only when it does not lead into an unsafe state such that resource requirements in future never cause a deadlock state. Now consider the following snapshot of the system.

	Allocation				Max				Available
	r_0	r_1	r_2	r_3	r_0	r_1	r_2	r_3	
p_0	0	0	1	2	0	0	1	2	r_0 r_1 r_2 r_3 1 5 2 0
p_1	1	0	0	0	1	7	5	0	
p_2	1	3	5	4	2	3	5	6	
p_3	0	6	3	2	0	6	5	2	
p_4	0	0	1	4	0	6	5	6	

Is the system currently in a safe state? If yes, explain why.

gate1988 normal descriptive operating-system resource-allocation

Answer ⬆

5.17.2 Resource Allocation: GATE CSE 1989 | Question: 11a top ⬆

https://gateoverflow.in/91093



- i. A system of four concurrent processes, P, Q, R and S , use shared resources A, B and C . The sequences in which processes, P, Q, R and S request and release resources are as follows:

- Process P: 1. P requests A
2. P requests B
3. P releases A
4. P releases B
- Process Q: 1. Q requests C
2. Q requests A
3. Q releases C
4. P releases A
- Process R: 1. R requests B
2. R requests C
3. R releases B
4. R releases C
- Process S: 1. S requests A
2. S requests C
3. S releases A
4. S releases C

If a resource is free, it is granted to a requesting process immediately. There is no preemption of granted resources. A resource is taken back from a process only when the process explicitly releases it.

Can the system of four processes get into a deadlock? If yes, give a sequence (ordering) of operations (for requesting and releasing resources) of these processes which leads to a deadlock.

- ii. Will the processes always get into a deadlock? If your answer is no, give a sequence of these operations which leads to completion of all processes.
- iii. What strategies can be used to prevent deadlocks in a system of concurrent processes using shared resources if preemption of granted resources is not allowed?

descriptive gate1989 operating-system resource-allocation

Answer 

5.17.3 Resource Allocation: GATE CSE 1992 | Question: 02-xi [top](#)

<https://gateoverflow.in/568>



A computer system has 6 tape devices, with n processes competing for them. Each process may need 3 tape drives. The maximum value of n for which the system is guaranteed to be deadlock-free is:

- A. 2
- B. 3
- C. 4
- D. 1

gate1992 operating-system resource-allocation normal multiple-selects

Answer 

5.17.4 Resource Allocation: GATE CSE 1993 | Question: 7.9, UGCNET-Dec2012-III: 41 [top](#)

<https://gateoverflow.in/2297>



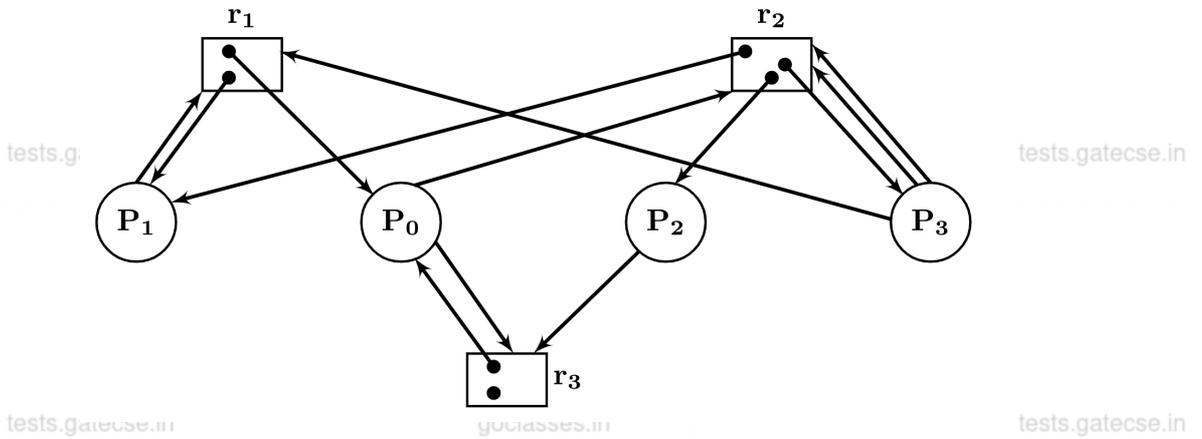
Consider a system having m resources of the same type. These resources are shared by 3 processes A , B , and C which have peak demands of 3, 4, and 6 respectively. For what value of m deadlock will not occur?

- A. 7
- B. 9
- C. 10
- D. 13
- E. 15

gate1993 operating-system resource-allocation normal ugcnetdec2012iii multiple-selects



Consider the resource allocation graph in the figure.



- A. Find if the system is in a deadlock state
- B. Otherwise, find a safe sequence



A computer system uses the Banker's Algorithm to deal with deadlocks. Its current state is shown in the table below, where P₀, P₁, P₂ are processes, and R₀, R₁, R₂ are resource types.

	Maximum Need			Current Allocation			Available			
	R ₀	R ₁	R ₂	R ₀	R ₁	R ₂	R ₀	R ₁	R ₂	
P ₀	4	1	2	P ₀	1	0	2	2	2	0
P ₁	1	5	1	P ₁	0	3	1			
P ₂	1	2	3	P ₂	1	0	2			

- A. Show that the system can be in this state
- B. What will the system do on a request by process P₀ for one unit of resource type R₁?



An operating system contains 3 user processes each requiring 2 units of resource R. The minimum number of units of R such that no deadlocks will ever arise is

- A. 3
- B. 5
- C. 4
- D. 6



An operating system handles requests to resources as follows.

A process (which asks for some resources, uses them for some time and then exits the system) is assigned a unique timestamp when it starts. The timestamps are monotonically increasing with time. Let us denote the timestamp of a process P by $TS(P)$.

When a process P requests for a resource the OS does the following:

- i. If no other process is currently holding the resource, the OS awards the resource to P .
- ii. If some process Q with $TS(Q) < TS(P)$ is holding the resource, the OS makes P wait for the resources.
- iii. If some process Q with $TS(Q) > TS(P)$ is holding the resource, the OS restarts Q and awards the resources to P . (Restarting means taking back the resources held by a process, killing it and starting it again with the same timestamp)

When a process releases a resource, the process with the smallest timestamp (if any) amongst those waiting for the resource is awarded the resource.

- A. Can a deadlock over arise? If yes, show how. If not prove it.
- B. Can a process P ever starve? If yes, show how. If not prove it.

gate1997 operating-system resource-allocation normal descriptive

Answer



A computer has six tape drives, with n processes competing for them. Each process may need two drives. What is the maximum value of n for the system to be deadlock free?

- A. 6
- B. 5
- C. 4
- D. 3

gate1998 operating-system resource-allocation normal

Answer



Which of the following is not a valid deadlock prevention scheme?

- A. Release all resources before requesting a new resource.
- B. Number the resources uniquely and never request a lower numbered resource than the last one requested.
- C. Never request a resource after releasing any resource.
- D. Request and all required resources be allocated before execution.

gate2000-cse operating-system resource-allocation normal

Answer



Two concurrent processes P_1 and P_2 want to use resources R_1 and R_2 in a mutually exclusive manner. Initially, R_1 and R_2 are free. The programs executed by the two processes are given below.

Program for P1:	Program for P2:
S1: While ($R1$ is busy) do no-op;	Q1: While ($R1$ is busy) do no-op;
S2: Set $R1 \leftarrow$ busy;	Q2: Set $R1 \leftarrow$ busy;
S3: While ($R2$ is busy) do no-op;	Q3: While ($R2$ is busy) do no-op;
S4: Set $R2 \leftarrow$ busy;	Q4: Set $R2 \leftarrow$ busy;
S5: Use $R1$ and $R2$;	Q5: Use $R1$ and $R2$;
S6: Set $R1 \leftarrow$ free;	Q6: Set $R2 \leftarrow$ free;
S7: Set $R2 \leftarrow$ free;	Q7: Set $R1 \leftarrow$ free;

- A. Is mutual exclusion guaranteed for $R1$ and $R2$? If not show a possible interleaving of the statements of $P1$ and $P2$ such mutual exclusion is violated (i.e., both $P1$ and $P2$ use $R1$ and $R2$ at the same time).
- B. Can deadlock occur in the above program? If yes, show a possible interleaving of the statements of $P1$ and $P2$ leading to deadlock.
- C. Exchange the statements $Q1$ and $Q3$ and statements $Q2$ and $Q4$. Is mutual exclusion guaranteed now? Can deadlock occur?

gate2001-cse operating-system resource-allocation normal descriptive

Answer 

5.17.12 Resource Allocation: GATE CSE 2005 | Question: 71 [top](#)

<https://gateoverflow.in/1394>



Suppose n processes, P_1, \dots, P_n share m identical resource units, which can be reserved and released one at a time. The maximum resource requirement of process P_i is s_i , where $s_i > 0$. Which one of the following is a sufficient condition for ensuring that deadlock does not occur?

- A. $\forall i, s_i < m$
- B. $\forall i, s_i < n$
- C. $\sum_{i=1}^n s_i < (m + n)$
- D. $\sum_{i=1}^n s_i < (m \times n)$

gate2005-cse operating-system resource-allocation normal

Answer 

5.17.13 Resource Allocation: GATE CSE 2006 | Question: 66 [top](#)

<https://gateoverflow.in/1344>



Consider the following snapshot of a system running n processes. Process i is holding x_i instances of a resource R , $1 \leq i \leq n$. Currently, all instances of R are occupied. Further, for all i , process i has pending a request for an additional y_i instances while holding the x_i instances it already has. There are exactly two processes p and q and such that $y_p = y_q = 0$. Which one of the following can serve as a necessary condition to guarantee that the system is not approaching a deadlock?

- A. $\min(x_p, x_q) < \max_{k \neq p, q} y_k$
- B. $x_p + x_q \geq \min_{k \neq p, q} y_k$
- C. $\max(x_p, x_q) > 1$
- D. $\min(x_p, x_q) > 1$

gate2006-cse operating-system resource-allocation normal

Answer 

5.17.14 Resource Allocation: GATE CSE 2007 | Question: 57 [top](#)

<https://gateoverflow.in/1255>



A single processor system has three resource types X, Y and Z , which are shared by three processes. There are 5 units of each resource type. Consider the following scenario, where the column **alloc** denotes the number of units of each resource type allocated to each process, and the column **request** denotes the number of units of each resource type requested by a process in order to complete execution. Which of these processes will finish **LAST**?



A system has n resources R_0, \dots, R_{n-1} , and k processes P_0, \dots, P_{k-1} . The implementation of the resource request logic of each process P_i is as follows:

if($i \% 2 == 0$) { if($i < n$) request R_i ; if($i + 2 < n$) request R_{i+2} ; } else { if($i < n$) request R_{n-i} ; if($i + 2 < n$) request R_n .

In which of the following situations is a deadlock possible?

- A. $n = 40, k = 26$
- B. $n = 21, k = 12$
- C. $n = 20, k = 10$
- D. $n = 41, k = 19$

gate2010-cse

operating-system

resource-allocation

normal

Answer



Three concurrent processes X, Y , and Z execute three different code segments that access and update certain shared variables. Process X executes the P operation (i.e., *wait*) on semaphores a, b and c ; process Y executes the P operation on semaphores b, c and d ; process Z executes the P operation on semaphores c, d , and a before entering the respective code segments. After completing the execution of its code segment, each process invokes the V operation (i.e., *signal*) on its three semaphores. All semaphores are binary semaphores initialized to one. Which one of the following represents a deadlock-free order of invoking the P operations by the processes?

- A. $X : P(a)P(b)P(c) \ Y : P(b)P(c)P(d) \ Z : P(c)P(d)P(a)$
- B. $X : P(b)P(a)P(c) \ Y : P(b)P(c)P(d) \ Z : P(a)P(c)P(d)$
- C. $X : P(b)P(a)P(c) \ Y : P(c)P(b)P(d) \ Z : P(a)P(c)P(d)$
- D. $X : P(a)P(b)P(c) \ Y : P(c)P(b)P(d) \ Z : P(c)P(d)P(a)$

gate2013-cse

operating-system

resource-allocation

normal

Answer



An operating system uses the *Banker's algorithm* for deadlock avoidance when managing the allocation of three resource types X, Y , and Z to three processes P_0, P_1 , and P_2 . The table given below presents the current system state. Here, the *Allocation matrix* shows the current number of resources of each type allocated to each process and the *Max matrix* shows the maximum number of resources of each type required by each process during its execution.

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	Allocation			Max		
	X	Y	Z	X	Y	Z
P₀	0	0	1	8	4	3
P₁	3	2	0	6	2	0
P₂	2	1	1	3	3	3

tests.gatecse.in

There are 3 units of type X , 2 units of type Y and 2 units of type Z still available. The system is currently in a **safe** state. Consider the following independent requests for additional resources in the current state:

REQ1: P_0 requests 0 units of X , 0 units of Y and 2 units of Z

REQ2: P_1 requests 2 units of X , 0 units of Y and 0 units of Z

Which one of the following is **TRUE**?

- A. Only REQ1 can be permitted.
- B. Only REQ2 can be permitted.
- C. Both REQ1 and REQ2 can be permitted.
- D. Neither REQ1 nor REQ2 can be permitted.

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gate2014-cse-set1

operating-system

resource-allocation

normal

Answer



A system contains three programs and each requires three tape units for its operation. The minimum number of tape units which the system must have such that deadlocks never arise is _____.

gate2014-cse-set3 operating-system resource-allocation numerical-answers easy

Answer



A system has 6 identical resources and N processes competing for them. Each process can request at most 2 requests. Which one of the following values of N could lead to a deadlock?

- A. 1
- B. 2
- C. 3
- D. 4

gate2015-cse-set2 operating-system resource-allocation easy

Answer



Consider the following policies for preventing deadlock in a system with mutually exclusive resources.

- I. Process should acquire all their resources at the beginning of execution. If any resource is not available, all resources acquired so far are released.
- II. The resources are numbered uniquely, and processes are allowed to request for resources only in increasing resource numbers
- III. The resources are numbered uniquely, and processes are allowed to request for resources only in decreasing resource numbers
- IV. The resources are numbered uniquely. A processes is allowed to request for resources only for a resource with resource number larger than its currently held resources

Which of the above policies can be used for preventing deadlock?

- A. Any one of (I) and (III) but not (II) or (IV)
- B. Any one of (I), (III) and (IV) but not (II)
- C. Any one of (II) and (III) but not (I) or (IV)
- D. Any one of (I), (II), (III) and (IV)

gate2015-cse-set3 operating-system resource-allocation normal

Answer



Consider the following proposed solution for the critical section problem. There are n processes : $P_0 \dots P_{n-1}$. In the code, function `pmax` returns an integer not smaller than any of its arguments .For all i , $t[i]$ is initialized to zero.

Code for P_i ,

```
do {
    c[i]=1; t[i]= pmax (t[0],...,t[n-1])+1; c[i]=0;
    for every j != i in {0,...,n-1} {
        while (c[j]);
        while (t[j] != 0 && t[j] <=t[i]);
    }
    Critical Section;
    t[i]=0;
    Remainder Section;
} while (true);
```

Which of the following is TRUE about the above solution?

- A. At most one process can be in the critical section at any time
- B. The bounded wait condition is satisfied
- C. The progress condition is satisfied
- D. It cannot cause a deadlock

Answer 5.17.24 Resource Allocation: GATE CSE 2017 Set 2 | Question: 33 [top](#) <https://gateoverflow.in/118375>

A system shares 9 tape drives. The current allocation and maximum requirement of tape drives for that processes are shown below:

	Process	Current Allocation	Maximum Requirement
tests.gatecse.in	P1	3	7
	P2	1	6
	P3	3	5

Which of the following best describes current state of the system?

- A. Safe, Deadlocked
- B. Safe, Not Deadlocked
- C. Not Safe, Deadlocked
- D. Not Safe, Not Deadlocked

Answer 5.17.25 Resource Allocation: GATE IT 2005 | Question: 62 [top](#) <https://gateoverflow.in/3823>

Two shared resources R_1 and R_2 are used by processes P_1 and P_2 . Each process has a certain priority for accessing each resource. Let T_{ij} denote the priority of P_i for accessing R_j . A process P_i can snatch a resource R_k from process P_j if T_{ik} is greater than T_{jk} .

Given the following :

- I. $T_{11} > T_{21}$
- II. $T_{12} > T_{22}$
- III. $T_{11} < T_{21}$
- IV. $T_{12} < T_{22}$

Which of the following conditions ensures that P_1 and P_2 can never deadlock?

- A. (I) and (IV)
- B. (II) and (III)
- C. (I) and (II)
- D. None of the above

Answer 5.17.26 Resource Allocation: GATE IT 2008 | Question: 54 [top](#) <https://gateoverflow.in/3364>

An operating system implements a policy that requires a process to release all resources before making a request for another resource. Select the TRUE statement from the following:

- A. Both starvation and deadlock can occur
- B. Starvation can occur but deadlock cannot occur
- C. Starvation cannot occur but deadlock can occur
- D. Neither starvation nor deadlock can occur

Answer 

Answers: Resource Allocation



✓ Here, we are asked to "Avoid Deadlock" and Bankers Algorithm is the algorithm for this.

The crux of the algorithm is to allocate resources to a process only if there exist a **safe sequence after** the allocation. i.e., after allocating the requested resources there exist a sequence of execution of the processes such that deadlock would not happen. There can be multiple safe sequences but we need to get any one of them to say that a state is safe.

Now coming to the given question, first lets make the NEED matrix which shows the future need of all the processes and can be obtained by $\text{Max} - \text{Allocation}$.

	Max				Allocation				Need					
	r_0	r_1	r_2	r_3	r_0	r_1	r_2	r_3	r_0	r_1	r_2	r_3		
p_0	0	0	1	2	p_0	0	0	1	2	p_0	0	0	0	0
p_1	1	7	5	0	p_1	1	0	0	0	p_1	0	7	5	0
p_2	2	3	5	6	p_2	1	3	5	4	p_2	1	0	0	2
p_3	0	6	5	2	p_3	0	6	3	2	p_3	0	0	2	0
p_4	0	6	5	6	p_4	0	0	1	4	p_4	0	6	4	2

Since P_0 does not require any more resource we can finish this first releasing 1 instance of r_2 and 2 instances of r_3 . Thus our Available vector becomes

$$[1 \ 5 \ 2 \ 0] + [0 \ 0 \ 1 \ 2] = [1 \ 5 \ 3 \ 2].$$

Now, either p_2 or p_3 can finish as both their requirements are not greater than the Available vector. Say, p_2 finishes. It releases $[2 \ 3 \ 5 \ 6]$ and our Available becomes

$$[1 \ 5 \ 3 \ 2] + [2 \ 3 \ 5 \ 6] = [3 \ 8 \ 8 \ 8].$$

Now, any of p_1, p_3, p_4 can finish and so we do not need to proceed further to determine that the state is safe. One of the possible safe sequence is

$$p_0 - p_2 - p_1 - p_3 - p_4.$$

👍 5 votes

-- Arjun Suresh (332k points)



i) Assuming only one instance of a resource is available,

- Process P: Hold A, request B
- Process Q: Hold C, request A
- Process R: Hold B, request C
- Process S: Request A, request C

In this instance, Process P,Q,R and S are waiting for the release of resources among each other and none of them can proceed. This is deadlock.

ii) Any sequential ordering will be free from deadlock. An instance(concurrent) can be:

Process P	Process Q	Process R	Process S
request A			
request B			
release A	request C		
release B	request A		
	release C		
	release A	request B	
		request C	
		release B	request A
		release C	
		request C	

All the requests of all processes are satisfied and leads to completion of all processes.

iii) To prevent deadlock:

- Resources can be shared (violating mutual exclusion)
- Not allowing processes to hold a resource and request for another(violating hold and wait)
- Break circular wait by allocating resources in some order
- Banker's algorithm(safe state)- to avoid deadlock

👍 9 votes

-- Manoja Rajalakshmi Aravindakshan (7.7k points)

5.17.3 Resource Allocation: GATE CSE 1992 | Question: 02-xi [top](#)

<https://gateoverflow.in/568>



- ✓ Allocate max-1 resources to all processes and add one more resource to any process (Pigeon hole principle) so that this particular process can be completed (resources can be freed) and there is no deadlock.

Max resources required is 3.

$$\therefore (3 - 1) * n + 1 = 6$$

$$n = \lfloor \frac{5}{2} \rfloor = 2$$

Correct Answer: A

👍 10 votes

-- Manoja Rajalakshmi Aravindakshan (7.7k points)

Answer: (A).

For $n = 3$, $2 - 2 - 2$ combination of resources leads to deadlock.

For $n = 2$, $3 - 3$ is the maximum need and that can always be satisfied.

👍 18 votes

-- Rajarshi Sarkar (27.9k points)

5.17.4 Resource Allocation: GATE CSE 1993 | Question: 7.9, UGCNET-Dec2012-III: 41 [top](#)

<https://gateoverflow.in/2297>



- ✓ **13 and 15.**

Consider the worst scenario: all processes require one more instance of the resource. So, P_1 would have got 2, $P_2 - 3$ and $P_3 - 5$. Now, if one more resource is available at least one of the processes could be finished and all resources allotted to it will be free which will lead to other processes also getting freed. So, $2 + 3 + 5 = 10$ would be the maximum value of m so that a deadlock can occur.

👍 41 votes

-- Arjun Suresh (332k points)

5.17.5 Resource Allocation: GATE CSE 1994 | Question: 28 [top](#)

<https://gateoverflow.in/2524>



- ✓ From the RAG we can make the necessary matrices.

	Allocation			Future Need		
	r_1	r_2	r_3	r_1	r_2	r_3
P_0	1	0	1	0	1	1
P_1	1	1	0	1	0	0
P_2	0	1	0	0	0	1
P_3	0	1	0	1	2	0

- Total = (2 3 2)
- Allocated = (2 3 1)
- Available = Total - Allocated = (0 0 1)

P_2 's need (0 0 1) can be met

And it releases its held resources after running to completion

$$A = (0 \ 0 \ 1) + (0 \ 1 \ 0) = (0 \ 1 \ 1)$$

P_0 's need (0 1 1) can be met

and it releases

$$A = (0 \ 1 \ 1) + (1 \ 0 \ 1) = (1 \ 1 \ 2)$$

P_1 's needs can be met (1 0 0) and it releases

$$A = (1 \ 1 \ 2) + (1 \ 1 \ 0) = (2 \ 2 \ 2)$$

P_3 's need can be met

So, the safe sequence will be $P_2 - P_0 - P_1 - P_3$.

37 votes

-- Sourav Roy (2.9k points)

5.17.6 Resource Allocation: GATE CSE 1996 | Question: 22 top 5

<https://gateoverflow.in/2774>



Allocation				MAX NEED				Future Need			
	R0	R1	R2		R0	R1	R2		R0	R1	R2
P0	1	0	2	P0	4	1	2	P0	3	1	0
P1	0	3	1	P1	1	5	1	P1	1	2	0
P2	1	0	2	P2	1	2	3	P2	0	2	1

Available = (2 2 0)

$P1(1 \ 2 \ 0)$'s needs can be met. $P1$ executes and completes releases its allocated resources.

$$A = (2 \ 2 \ 0) + (0 \ 3 \ 1) = (2 \ 5 \ 1)$$

Further $P2(0 \ 2 \ 1)$ s needs can be met.

$$A = (2 \ 5 \ 1) + (1 \ 0 \ 2) = (3 \ 5 \ 3)$$

next $P0$ s needs can be met.

Thus safe sequence exists $P1P2P0$.

Next Request $P0(010)$

Allocation				MAX NEED				Future Need			
	R0	R1	R2		R0	R1	R2		R0	R1	R2
P0	1	0+1=1	2	P0	4	1	2	P0	3	0	0
P1	0	3	1	P1	1	5	1	P1	1	2	0
P2	1	0	2	P2	1	2	3	P2	0	2	1

Available = (2 2 - 1 = 1 0)

Here, also not a single request need by any process can be made.

- System is in safe state.
- Since request of $P0$ can not be met, system would delay the request and wait till resources are available.

24 votes

-- Sourav Roy (2.9k points)

5.17.7 Resource Allocation: GATE CSE 1997 | Question: 6.7 top 5

<https://gateoverflow.in/2263>



If we have X number of resources where X is sum of $r_i - 1$ where r_i is the resource requirement of process i , we might have a deadlock. But if we have one more resource, then as per Pigeonhole principle, one of the process must complete and this can eventually lead to all processes completing and thus no deadlock.

Here, $n = 3$ and $r_i = 2$ for all i . So, in order to avoid deadlock **minimum** no. of resources required

$$= \sum_{i=1}^3 (2 - 1) + 1 = 3 + 1 = 4.$$

PS: Note the **minimum** word, any higher number will also cause no deadlock.

Correct Answer: C

👍 18 votes

-- hriday (161 points)

5.17.8 Resource Allocation: GATE CSE 1997 | Question: 75 top 9

<https://gateoverflow.in/19705>



- A. **Can Deadlock occur. No, because every time Older Process who wants some resources which are already acquired by some younger process. In this condition Younger will be killed and release its resources which is now taken by now older process. So never more than one process will wait for some resources indefinitely. Timestamp will also be unique.**
- B. **Can a process Starve. No, because every time when Younger process is getting killed, it is restarted with same timestamp which he had at time of killing. So it will act as an elder even after killing for all those who came after it..**

There is No starvation. Consider this scenario:

Say a process p_{12} with TS 12 and another process p_{11} with timestamp 11 so, p_{12} gets killed but again come with **same timestamp**. As timestamp is increasing for newly enter process so at next process p_{13} enter with timestamp 13 which have greater timestamp than p_{12} so, p_{12} gets executed. Hence there is no starvation possible.

👍 35 votes

-- sonu (1.8k points)

5.17.9 Resource Allocation: GATE CSE 1998 | Question: 1.32 top 9

<https://gateoverflow.in/1669>



Each process needs 2 drives

Consider this scenario

P_1	P_2	P_3	P_4	P_5	P_6
1	1	1	1	1	1

This is scenario when a deadlock would happen, as each of the process is waiting for 1 more process to run to completion. And there are no more Resources available as max 6 reached. If we could have provided one more R to any of the process, any of the process could have executed to completion, then released its resources, which further when assigned to other and then other would have broken the deadlock situation.

In case of processes, if there are less than 6 processes, then no deadlock occurs.

Consider the maximum case of 5 processes.

P_1	P_2	P_3	P_4	P_5
1	1	1	1	1

In this case system has 6 resources max, and hence we still have 1 more R left which can be given to any of the processes, which in turn runs to completion, releases its resources and in turn others can run to completion too.

Answer (B).

👍 29 votes

-- Sourav Roy (2.9k points)

5.17.10 Resource Allocation: GATE CSE 2000 | Question: 2.23 top 9

<https://gateoverflow.in/670>



The answer is (C).

- A. is valid. Which dissatisfies Hold and Wait but ends up in starvation.
- B. is valid. Which is used to dissatisfy circular wait.
- C. is invalid.
- D. is valid and is used to dissatisfy Hold and Wait.

👍 36 votes

-- Gate Keeda (15.9k points)



A. Mutual exclusion is not guaranteed;

Initially both $R1$ and $R2$ are free.
Now, consider the scenario:

$P1$ will start and check the condition ($R1 == \text{busy}$) it will be evaluated as false and $P1$ will be preempted.
Then, $P2$ will start and check the condition ($R1 == \text{busy}$) it will be evaluated as false and $P2$ will be preempted.
Now, again $P1$ will start execution and set $R1 = \text{busy}$ then preempted again.
Then $P2$ will start execution and set $R1 = \text{busy}$ which was already updated by $P1$ and now $P2$ will be preempted.
After that $P1$ will start execution and same scenario happen again with both $P1$ and $P2$.
Both set $R2 = \text{busy}$ and enter into critical section together.

Hence, Mutual exclusion is not guaranteed.

B. Here, deadlock is not possible, because at least one process is able to proceed and enter into critical section.

C. If $Q1$ and $Q3$; $Q2$ and $Q4$ will be interchanged then Mutual exclusion is guaranteed but deadlock is possible.

Here, both process will not be able to enter critical section together.

For deadlock:

If $P1$ sets $R1 = \text{busy}$ and then preempted, and $P2$ sets $R2 = \text{busy}$ then preempted.
In this scenario no process can proceed further, as both holding the resource that is required by other to enter into CS.

Hence, deadlock will be there.

30 votes

-- jayendra (6.7k points)



To ensure deadlock never happens allocate resources to each process in following manner:

Worst Case Allocation (maximum resources in use without any completion) will be $(\text{max requirement} - 1)$ allocations for each process. i.e., $s_i - 1$ for each i

Now, if $\sum_{i=1}^n (s_i - 1) \leq m$ dead lock can occur if m resources are split equally among the n processes and all of them will be requiring one more resource instance for completion.

Now, if we add just one more resource, one of the process can complete, and that will release the resources and this will eventually result in the completion of all the processes and deadlock can be avoided. i.e., to avoid deadlock

$$\sum_{i=1}^n (s_i - 1) + 1 \leq m$$

$$\Rightarrow \sum_{i=1}^n s_i - n + 1 \leq m$$

$$\Rightarrow \sum_{i=1}^n s_i < (m + n).$$

Correct Answer: C

104 votes

-- Digvijay (44.9k points)



B. $x_p + x_q \geq \min_{k \neq p, q} y_k$

The question asks for "necessary" condition to guarantee no deadlock. i.e., without satisfying this condition "deadlock" MUST be there.

Both the processes p and q have no additional requirements and can be finished releasing $x_p + x_q$ resources. Using this we can finish one more process only if condition B is satisfied.

PS: Condition B just ensures that the system can proceed from the current state. It does not guarantee that there won't be a deadlock before all processes are finished.

👍 65 votes

-- Arjun Suresh (332k points)

5.17.14 Resource Allocation: GATE CSE 2007 | Question: 57 top ⤴

<https://gateoverflow.in/1255>



✓ The answer is (C).

Available Resources

X	Y	Z
0	1	2

Now, P_1 will execute first, As it meets the needs. After completion, The available resources are updated.

Updated Available Resources

X	Y	Z
2	1	3

Now P_0 will complete the execution, as it meets the needs.

After completion of P_0 the table is updated and then P_2 completes the execution.

Thus P_2 completes the execution in the last.

👍 27 votes

-- Gate Keeda (15.9k points)

5.17.15 Resource Allocation: GATE CSE 2008 | Question: 65 top ⤴

<https://gateoverflow.in/488>



✓ (A). In deadlock prevention, we just need to ensure one of the four necessary conditions of deadlock doesn't occur. So, it may be the case that a resource request might be rejected even if the resulting state is safe. (One example, is when we impose a strict ordering for the processes to request resources).

Deadlock avoidance is less restrictive than deadlock prevention. Deadlock avoidance is like a police man and deadlock prevention is like a traffic light. The former is less restrictive and allows more concurrency.

Reference: <http://www.cs.jhu.edu/~yairamir/cs418/os4/tsld010.htm>

References



👍 72 votes

-- Arjun Suresh (332k points)

5.17.16 Resource Allocation: GATE CSE 2009 | Question: 30 top ⤴

<https://gateoverflow.in/1316>



✓ At $t = 3$, the process P_1 has to wait because available $R_1 = 1$, but P_1 needs 2 R_1 . so P_1 is blocked.

Similarly, at various times what is happening can be analyzed by the table below.

		R1(3)	R2(2)	R3(3)	R4(2)
	t=0	3	0	1	1
	t=1	3	0	0	1
Block P1	t=2	1	0	0	0
	t=3	1	0	0	0
	t=4	0	0	0	0
Unblock P1	t=5	1	1	0	0
	t=6	1	1	1	0
Block P1	t=7	1	0	2	0
	t=8	2	0	2	1
Unblock P1	t=9	2	1	3	0
	t=10				

There are no processes in deadlock, hence (A) is right choice

👍 73 votes

-- Sachin Mittal (15.8k points)

5.17.17 Resource Allocation: GATE CSE 2010 | Question: 46 top ⬆

<https://gateoverflow.in/2348>



- ✓ From the resource allocation logic, it's clear that even numbered processes are taking even numbered resources and all even numbered processes share no more than 1 resource. Now, if we make sure that all odd numbered processes take odd numbered resources without a cycle, then deadlock cannot occur. The "else" case of the resource allocation logic, is trying to do that. But, if n is odd, R_{n-i} and R_{n-i-2} will be even and there is possibility of deadlock, when two processes requests the same R_i and R_j . So, only B and D are the possible answers.

Now, in D , we can see that P_0 requests R_0 and R_2 , P_2 requests R_2 and R_4 , so on until, P_{18} requests R_{18} and R_{20} . At the same time P_1 requests R_{40} and R_{38} , P_3 requests R_{38} and R_{36} , so on until, P_{17} requests R_{24} and R_{22} . i.e.; there are no two processes requesting the same two resources and hence there can't be a cycle of dependencies which means, no deadlock is possible.

But for B , P_8 requests R_8 and R_{10} and P_{11} also requests R_{10} and R_8 . Hence, a deadlock is possible. (Suppose P_8 comes first and occupies R_8 . Then P_{11} comes and occupies R_{10} . Now, if P_8 requests R_{10} and P_{11} requests R_8 , there will be deadlock)

Correct Answer: B

👍 279 votes

-- Arjun Suresh (332k points)

5.17.18 Resource Allocation: GATE CSE 2013 | Question: 16 top ⬆

<https://gateoverflow.in/1438>



- ✓ For deadlock-free invocation, X, Y and Z must access the semaphores in the same order so that there won't be a case where one process is waiting for a semaphore while holding some other semaphore. This is satisfied only by option B.

In option A, X can hold a and wait for c while Z can hold c and wait for a
In option C, X can hold b and wait for c, while Y can hold c and wait for b
In option D, X can hold a and wait for c while Z can hold c and wait for a

So, a deadlock is possible for all choices except B.

<http://www.eee.metu.edu.tr/~halici/courses/442/Ch5%20Deadlocks.pdf>

References



👍 56 votes

-- Arjun Suresh (332k points)

5.17.19 Resource Allocation: GATE CSE 2014 Set 1 | Question: 31 top ⬆

<https://gateoverflow.in/1800>



- ✓ Option (B)

Request 1 if permitted does not lead to a safe state.

After allowing Req 1,

	Allocated			Max			Requirement		
P0	0	0	3	8	4	3	8	4	0
P1	3	2	0	6	2	0	3	0	0
P2	2	1	1	3	3	3	1	2	2

Available : $X = 3, Y = 2, Z = 0$

Now we can satisfy $P1$'s requirement completely. So Available becomes : $X = 6, Y = 4, Z = 0$.

Since, Z is not available now, neither $P0$'s nor $P2$'s requirement can be satisfied. So. it is an unsafe state.

👍 36 votes

-- Poulami Das (167 points)

5.17.20 Resource Allocation: GATE CSE 2014 Set 3 | Question: 31 top

<https://gateoverflow.in/2065>



✓ Up to, 6 resources, there can be a case that all process have 2 each and dead lock can occur. With 7 resources, at least one process's need is satisfied and hence it must go ahead and finish and release all 3 resources it held. So, no dead lock is possible.

👍 25 votes

-- Arjun Suresh (332k points)

For these type of problems in which every process is making same number of requests, use the formula

$$n \cdot (m - 1) + 1 \leq r$$

where,

n = no. of processes

m = resource requests made by processes

r = no. of resources

So, in above problem we get $3 \cdot (3 - 1) + 1 \leq r \implies r \geq 7$

Minimum number of resource required to avoid deadlock is 7.

👍 31 votes

-- neha pawar (3.3k points)

5.17.21 Resource Allocation: GATE CSE 2015 Set 2 | Question: 23 top

<https://gateoverflow.in/8114>



✓ $3 \times 2 = 6$

$4 \times 2 = 8$

I guess a question can't get easier than this- (D) choice. (Also, we can simply take the greatest value among choice for this question)

[There are 6 resources and all of them must be in use for deadlock. If the system has no other resource dependence, $N = 4$ cannot lead to a deadlock. But if $N = 4$, the system can be in deadlock in presence of other dependencies.

Why $N = 3$ cannot cause deadlock? It can cause deadlock, only if the system is already in deadlock and so the deadlock is independent of the considered resource. Till $N = 3$, all requests for considered resource will always be satisfied and hence there won't be a waiting and hence no deadlock with respect to the considered resource.]

👍 36 votes

-- Arjun Suresh (332k points)

5.17.22 Resource Allocation: GATE CSE 2015 Set 3 | Question: 52 top

<https://gateoverflow.in/8561>



✓ A deadlock will not occur if any one of the below four conditions are prevented:

1. **hold and wait**
2. **mutual exclusion**
3. **circular wait**

4. no-preemption

Now,

Option-1 if implemented violates 1 so deadlock cannot occur.

Option-2 if implemented violates circular wait (making the dependency graph acyclic)

Option-3 if implemented violates circular wait (making the dependency graph acyclic)

Option-4 it is equivalent to options 2 and 3

So, the correct option is 4 as all of them are methods to prevent deadlock.

http://www.cs.uic.edu/~jbell/CourseNotes/OperatingSystems/7_Deadlocks.html

References



69 votes

-- Tamojit Chatterjee (1.9k points)

5.17.23 Resource Allocation: GATE CSE 2016 Set 1 | Question: 50 top 5

<https://gateoverflow.in/39719>



Answer is (A)

```
while (t[j] != 0 && t[j] <=t[i]);
```

This ensures that when a process i reaches Critical Section, all processes j which started before it must have its $t[j] = 0$. This means no two process can be in critical section at same time as one of them must be started earlier.

! returns an integer not smaller

is the issue here for deadlock. This means two processes can have same t value and hence

```
while (t[j] != 0 && t[j] <=t[i]);
```

can go to infinite wait. ($t[j] == t[i]$). Starvation is also possible as there is nothing to ensure that a request is granted in a timed manner. But bounded waiting (as defined in Galvin) is guaranteed here as when a process i starts and gets $t[i]$ value, no new process can enter critical section before i (as their t value will be higher) and this ensures that access to critical section is granted only to a finite number of processes (those which started before) before eventually process i gets access.

But in some places bounded waiting is defined as finite waiting (see one [here](#) from CMU) and since deadlock is possible here, bounded waiting is not guaranteed as per that definition.

References



78 votes

-- Arjun Suresh (332k points)

Given question is a wrongly modified version of actual bakery algorithm, used for N-process critical section problem.

Bakery algorithm code goes as follows : (as in William stalling book page 209, 7th edition)

```
Entering[i] = true;
Number[i] = 1 + max(Number[1], ..., Number[NUM_THREADS]);
Entering[i] = false;

for (integer j = 1; j <= NUM_THREADS; j++) {
    // Wait until thread j receives its number:
    while (Entering[j]) {
        /* nothing */
    }

    // Wait until all threads with smaller numbers or with the same
```

```

// number, but with higher priority, finish their work:
while ((Number[j] != 0) && ((Number[j], j) < (Number[i], i))) {
    /* nothing */
}
}

<Critical Section>

Number[i] = 0;
/*remainder section */

```

code explanation:

The important point here is that due to lack of atomicity of `max` function multiple processes may calculate the same `Number`.

In that situation to choose between two processes, we prioritize the lower `process_id`.

`(Number[j], j) < (Number[i], i)` this is a tuple comparison and it allows us to correctly select **only one** process out of `i` and `j`. but not both (when `Number[i] = Number[j]`)

Progress and Deadlock:

The testing condition given in the question is `while (t[j] != 0 && t[j] <= t[i]);` which creates deadlock for both `i` and `j` (and possibly more) processes which have calculated their `Numbers` as the same value. C and D are wrong.

Bounded waiting :

If the process `i` is waiting and looping inside the for loop. Why is it waiting there ? Two reasons,

1. Its number value is not yet the minimum positive value.
2. Or, its Number value is equal to some other's Number value.

Reason1 does not dissatisfy bounded waiting , because if the process `i` has the `Number` value = 5 then all processes having less positive `Number` will enter CS first and will exit. Then Process `i` will definitely get a chance to enter into CS.

Reason2 dissatisfy bounded waiting because assume process 3 and 4 are fighting with the equal `Number` value of 5. whenever one of them (say 4) is scheduled by the short term scheduler to the CPU, it goes on looping on `Number[3] <= Number[4]` .Similarly with process 3 also. But when they are removed from the Running state by the scheduler , other processes may continue normal operation. So for process 3 and 4 although they have requested very early, because of their own reason, other processes are getting a chance of entering into CS. B is wrong.

note : in this all the processes go into deadlock anyway after a while.

How mutual exclusion is satisfied ?

Now we assume all processes calculate their `Number` value as distinct.

And categorize all concurrent `N` processes into three groups;

1. Processes which are now testing the while condition inside the for loop.
2. Processes which are now in the reminder section.
3. Processes which are now about to calculate its `Number` values.

In *Category 1*, assume process `i` wins the testing condition, that means no one else can win the test because `i` has the lowest positive value among the 1st category of processes.

Category 3 processes will calculate `Number` value more than the `Number` of `i` using `max` the function.

Same goes with *Category 2* processes if they ever try to re-enter.

detail of bakery algorithm [Link1](#) and [Link2](#) and [Link3_page53](#)

References



👍 45 votes

-- Debashish Deka (40.8k points)



Process	Current Allocation	Max Requirement	Need
P1	3	7	4
P2	1	6	5
P3	3	5	2

Given there are total 9 tape drives,

So, according to the above table we can see we have currently allocated (7 tape drive), so **currently Available tape drives = 2**

So, *P3* can use it and after using it will release it 3 resources **New Available = 5**

then *P1* can use it and will release it 3 resources so **New Available = 8**

and lastly *P2* so, all the process are in **SAFE STATE** and there will be **NO DEADLOCK**

Safe Sequence will be **P3 → P2 → P1** or **P3 → P1 → P2**.

Answer will be (B) only.

42 votes

-- Abhishek Mitra (509 points)

5.17.25 Resource Allocation: GATE IT 2005 | Question: 62 top

<https://gateoverflow.in/3823>



- ✓ If any process has highest priority over all the resources then it can snatch any resource from any other process and so no deadlock can occur with another process as this highest priority process will eventually finish and release all the resources for the other less priority process.

In case of (I) and (II) process 1 has given highest priority over all the resources and hence deadlock cannot occur.

Similarly, in the case of (III) and (IV) process 2 has given highest priority over all the resources and hence deadlock cannot occur.

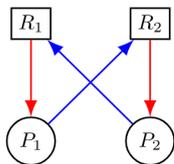
If we consider option (A) (I) and (IV)

- $T_{11} > T_{21}$ // for resource 1, process 1 has the highest priority
- $T_{22} > T_{12}$ // for resource 2, process 2 has highest priority

Let *P1* be holding *R1* and waiting for *R2*.

Let *P2* be holding *R2* and waiting for *R1*.

This is deadlock as neither is releasing its held resources.



Similarly in option B also deadlock can occur.

Correct **answer : C**

27 votes

-- Dharmendra Lodhi (2.7k points)

5.17.26 Resource Allocation: GATE IT 2008 | Question: 54 top

<https://gateoverflow.in/3364>



- ✓ Answer: **(B)**

Starvation can occur as each time a process requests a resource it has to release all its resources. Now, maybe the process has not used the resources properly yet. This will happen again when the process requests another resource. So, the process starves for proper utilisation of resources.

Deadlock will not occur as it is similar to a deadlock prevention scheme.

31 votes

-- Rajarshi Sarkar (27.9k points)

5.18

Runtime Environments (3) top



Match the pairs in the following questions by writing the corresponding letters only.

(a) Buddy system	(p) Run time type specification
(b) Interpretation	(q) Segmentation
(c) Pointer type	(r) Memory allocation
(d) Virtual memory	(s) Garbage collection

gate1991

operating-system

normal

match-the-following

runtime-environments

goclasses.in

tests.gatecse.in

Answer



The correct matching for the following pairs is

(A) Activation record	(1) Linking loader
(B) Location counter	(2) Garbage collection
(C) Reference counts	(3) Subroutine call
(D) Address relocation	(4) Assembler

- A. A-3 B-4 C-1 D-2
 B. A-4 B-3 C-1 D-2
 C. A-4 B-3 C-2 D-1
 D. A-3 B-4 C-2 D-1

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goclasses.in

tests.gatecse.in

Answer



Dynamic linking can cause security concerns because

- A. Security is dynamic
 B. The path for searching dynamic libraries is not known till runtime
 C. Linking is insecure
 D. Cryptographic procedures are not available for dynamic linking

gate2002-cse

operating-system

runtime-environments

easy

Answer

Answers: Runtime Environments



✓ (a) – (r), (b) – (p), (c) – (s), (d) – (q)

21 votes

-- Gate Keeda (15.9k points)



✓ **(D) Option**

Each time a sub routine is called, its activation record is created.

An assembler uses location counter value to give address to each instruction which is needed for relative addressing as well as for jump labels.

Reference count is used by garbage collector to clear the memory whose reference count becomes 0.

Linker Loader is a loader which can load several compiled codes and link them together into a single executable. Thus it needs to do relocation of the object codes.

👍 56 votes

-- Arjun Suresh (332k points)

5.18.3 Runtime Environments: GATE CSE 2002 | Question: 2.20 [top](#)

<https://gateoverflow.in/850>



- A. Nonsense option, No idea why it is here.
- B. The path for searching dynamic libraries is not known till runtime -> This seems most correct answer.
- C. This is not true. Linking in itself not insecure.
- D. There is no relation between Cryptographic procedures & Dynamic linking.

👍 46 votes

-- Akash Kanase (36k points)

5.19 Semaphores (8) [top](#)

5.19.1 Semaphores: GATE CSE 1990 | Question: 1-vii [top](#)

<https://gateoverflow.in/83851>



Semaphore operations are atomic because they are implemented within the OS _____.

gate1990 operating-system semaphores process-synchronization fill-in-the-blanks goclases.in

tests.gatecse.in

Answer

5.19.2 Semaphores: GATE CSE 1992 | Question: 02.x, ISRO2015-35 [top](#)

<https://gateoverflow.in/564>



At a particular time of computation, the value of a counting semaphore is 7. Then 20 P operations and 15 V operations were completed on this semaphore. The resulting value of the semaphore is :

- A. 42
- B. 2
- C. 7
- D. 12

gate1992 operating-system semaphores easy isro2015 multiple-selects process-synchronization

Answer

5.19.3 Semaphores: GATE CSE 1998 | Question: 1.31 [top](#)

<https://gateoverflow.in/1668>



A counting semaphore was initialized to 10. Then $6P$ (wait) operations and $4V$ (signal) operations were completed on this semaphore. The resulting value of the semaphore is

- A. 0
- B. 8
- C. 10
- D. 12

gate1998 operating-system process-synchronization semaphores easy

Answer

5.19.4 Semaphores: GATE CSE 2008 | Question: 63 [top](#)

<https://gateoverflow.in/486>



The P and V operations on counting semaphores, where s is a counting semaphore, are defined as follows:

$P(s)$: $s = s - 1$;
If $s < 0$ then wait;

$V(s)$: $s = s + 1$;
If $s \leq 0$ then wake up process waiting on s ;

Assume that P_b and V_b the wait and signal operations on binary semaphores are provided. Two binary semaphores x_b and y_b are used to implement the semaphore operations $P(s)$ and $V(s)$ as follows:

```

P(s) :
    P_b(x_b);
    s = s - 1;
    if (s < 0)
    {
        V_b(x_b);
        P_b(y_b);
    }
    else V_b(x_b);

```

```

V(s) :
    P_b(x_b);
    s = s + 1;
    if (s ≤ 0) V_b(y_b);
    V_b(x_b);

```

The initial values of x_b and y_b are respectively

- A. 0 and 0
- B. 0 and 1
- C. 1 and 0
- D. 1 and 1

gate2008-cse operating-system normal semaphores

Answer

5.19.5 Semaphores: GATE CSE 2016 Set 2 | Question: 49

<https://gateoverflow.in/39576>



Consider a non-negative counting semaphore S . The operation $P(S)$ decrements S , and $V(S)$ increments S . During an execution, 20 $P(S)$ operations and 12 $V(S)$ operations are issued in some order. The largest initial value of S for which at least one $P(S)$ operation will remain blocked is _____

gate2016-cse-set2 operating-system semaphores normal numerical-answers

Answer

5.19.6 Semaphores: GATE CSE 2020 | Question: 34

<https://gateoverflow.in/333197>



Each of a set of n processes executes the following code using two semaphores a and b initialized to 1 and 0, respectively. Assume that count is a shared variable initialized to 0 and not used in CODE SECTION P.

CODE SECTION P

```

wait(a); count=count+1;
if (count==n) signal(b);
signal(a); wait(b); signal(b);

```

CODE SECTION Q

What does the code achieve?

- A. It ensures that no process executes CODE SECTION Q before every process has finished CODE SECTION P.
- B. It ensures that two processes are in CODE SECTION Q at any time.
- C. It ensures that all processes execute CODE SECTION P mutually exclusively.
- D. It ensures that at most $n - 1$ processes are in CODE SECTION P at any time.

gate2020-cse operating-system semaphores

Answer

5.19.7 Semaphores: GATE CSE 2021 Set 1 | Question: 46

<https://gateoverflow.in/357405>



Consider the following pseudocode, where S is a semaphore initialized to 5 in line #2 and counter is a shared variable initialized to 0 in line #1. Assume that the increment operation in line #7 is *not* atomic.

```

1. int counter = 0;
2. Semaphore S = init(5);
3. void parop(void)
4. {
5.     wait(S);

```

```

6.      wait(S);
7.      counter++;
8.      signal(S);
9.      signal(S);
10.   }

```

If five threads execute the function `parop` concurrently, which of the following program behavior(s) is/are possible?

- A. The value of `counter` is 5 after all the threads successfully complete the execution of `parop`
- B. The value of `counter` is 1 after all the threads successfully complete the execution of `parop`
- C. The value of `counter` is 0 after all the threads successfully complete the execution of `parop`
- D. There is a deadlock involving all the threads

gate2021-cse-set1 multiple-selects operating-system process-synchronization semaphores

Answer

5.19.8 Semaphores: GATE IT 2006 | Question: 57 [top](#)

<https://gateoverflow.in/3601>



The wait and signal operations of a monitor are implemented using semaphores as follows. In the following,

- x is a condition variable,
- `mutex` is a semaphore initialized to 1,
- `x_sem` is a semaphore initialized to 0,
- `x_count` is the number of processes waiting on semaphore `x_sem`, initially 0,
- `next` is a semaphore initialized to 0,
- `next_count` is the number of processes waiting on semaphore `next`, initially 0.

The body of each procedure that is visible outside the monitor is replaced with the following:

```

P(mutex);
...
body of procedure
...
if (next_count > 0)
    V(next);
else
    V(mutex);

```

Each occurrence of `x.wait` is replaced with the following:

```

x_count = x_count + 1;
if (next_count > 0)
    V(next);
else
    V(mutex);
----- E1;
x_count = x_count - 1;

```

Each occurrence of `x.signal` is replaced with the following:

```

if (x_count > 0)
{
    next_count = next_count + 1;
    ----- E2;
    P(next);
    next_count = next_count - 1;
}

```

For correct implementation of the monitor, statements $E1$ and $E2$ are, respectively,

- A. $P(x_sem), V(next)$
- B. $V(next), P(x_sem)$
- C. $P(next), V(x_sem)$
- D. $P(x_sem), V(x_sem)$

gate2006-it operating-system process-synchronization semaphores normal

Answer

Answers: Semaphores



- ✓ The concept of semaphores is used for synchronization.
Semaphore is an integer with a difference. Well, actually a few differences.
You set the value of the integer when you create it, but can never access the value directly after that; you must use one of the semaphore functions to adjust it, and you cannot ask for the current value.
There are semaphore functions to increment or decrement the value of the integer by one.
Decrementing is a (possibly) blocking function. If the resulting semaphore value is negative, the calling thread or process is blocked, and cannot continue until some other thread or process increments it.
Incrementing the semaphore when it is negative causes one (and only one) of the threads blocked by this semaphore to become unblocked and runnable.

Therefore, all semaphore operations are atomic. Implemented in kernel,

👍 24 votes

-- Neeraj7375 (1.1k points)



- ✓ The answer is option **B**.

Currently semaphore is 7 so, after 20 P(wait) operation it will come to -13 then for 15 V(signal) operation the value comes to 2.

👍 32 votes

-- sanjeev_zerocode (295 points)



- ✓ Answer is option **(B)**

Initially semaphore is 10, then 6 down operations are performed means $(10 - 6 = 4)$ and 4 up operations means $(4 + 4 = 8)$

So, at last option **(B)** 8 is correct.

👍 29 votes

-- Kalpna Bhargav (2.5k points)



- ✓ Answer is **(C)**.

Reasoning :-

First let me explain what is counting semaphore & How it works. Counting semaphore gives count, i.e. no of processes that can be in Critical section at same time. Here value of S denotes that count. So suppose $S = 3$, we need to be able to have 3 processes in Critical section at max. Also when counting semaphore S has negative value we need to have Absolute value of S as no of processes waiting for critical section.

(A) & (B) are out of option, because Xb must be 1, otherwise our counting semaphore will get blocked without doing anything. Now consider options (C) & (D).

Option (D) :-

$$Yb = 1, Xb = 1$$

Assume that initial value of $S = 2$. (At max 2 processes must be in Critical Section.)

We have 4 processes, P_1, P_2, P_3 & P_4 .

P_1 enters critical section, It calls $P(s), S = S - 1 = 1$. As $S > 1$, we do not call $Pb(Yb)$.

P_2 enters critical section, It calls $P(s), S = S - 1 = 0$. As $S > 0$ we do not call $Pb(Yb)$.

Now P_3 comes, it should be blocked but when it calls $P(s), S = S - 1 = 0 - 1 = -1$ As $S < 0$, Now we do call $Pb(Yb)$. Still P_3 enters into critical section & We do not get blocked as Yb 's Initial value was 1.

This violates property of counting semaphore. S is now -1 , & No process is waiting. Also we are allowing 1 more process than what counting semaphore permits.

If Yb would have been 0, P_3 would have been blocked here & So Answer is (C).

$Pb(yb)$;

5.19.5 Semaphores: GATE CSE 2016 Set 2 | Question: 49 top 5<https://gateoverflow.in/39576>

- ✓ Answer: (7). Take any sequence of $20P$ and $12V$ operations, atleast one process will always remain blocked.

5.19.6 Semaphores: GATE CSE 2020 | Question: 34 top 5<https://gateoverflow.in/33197>

- ✓ Answer: A. It ensures that no process executes CODE SECTION Q before every process has finished CODE SECTION P.

Explanation

In short, semaphore 'a' controls mutually exclusive execution of statement count+=1 and semaphore 'b' controls entry to CODE SECTION Q when all the process have executed CODE SECTION P. As checked by given condition $\text{if}(\text{count}==n)$ signal(b); the semaphore 'b' is initialized to 0 and only increments when this condition is TRUE. (Side fact, processes do not enter the CODE SECTION Q in mutual exclusion, the moment all have executed CODE SECTION P, process will enter CODE SECTION Q in any order.)

Detailed explanation:-

Consider this situation as the processes need to execute three stages- Section P, then the given code and finally Section Q.

It is evident that semaphores do not control Section P hence, **There is no restriction in execution of P.**

Now, we are given 2 semaphores 'a' and 'b' initialized to '1' and '0' respectively.

Take an example of 3 processes (hence $n=3$, $\text{count}=0$ (initially)) and lets say first of them has finished executing Section P and enters the given code. It does following changes:-

- will execute `wait(a)` hence making semaphore $a=0$
- increment the count from 0 to 1 (first time)
- If $(\text{count}==n)$ evaluates FALSE and hence signal(b) is not executed.** So semaphore b remains 0
- `signal(a)` hence making semaphore $a=1$
- `wait(b)` But since semaphore b is already 0, **The process will be in blocked/waiting state.**

First out of the three processes is unable to enter the CODE SECTION Q !

Now say second process completes CODE SECTION P and starts executing the given code. It can be concluded that it will follow the same sequence (5 steps) as mentioned above and status of variables will be:- $\text{count} = 2$ (still $\text{count} < n$), semaphore $a=1$, semaphore $b=0$ (no change)

Finally the last process finishes execution of CODE SECTION P.

It will follow same steps 1 and 2 making semaphore $a=0$ and **count = 3**

3. if $(\text{count}==n)$ evaluates TRUE! and hence signal(b) is executed marking semaphore $b = 1$ FOR THE FIRST TIME.

4 and 5 will be executed the same way.

Now the moment this last process signaled b, the previously blocked process will be able to execute `wait(b)` and the very next moment execute `signal(b)` to allow other blocked/waiting process to proceed.

This way all the processes enter CODE SECTION Q after executing CODE SECTION P.

5.19.7 Semaphores: GATE CSE 2021 Set 1 | Question: 46 top 5<https://gateoverflow.in/357405>

- ✓ **Correct Options: A,B,D**

The given code allows up to 2 threads to be in the critical section as the initial value of semaphore is 5 and 2 wait operations are necessary to enter the critical section ($\lfloor 5/2 \rfloor = 2$).

In the critical section the increment operation is not atomic. So, multiple threads entering the critical section simultaneously can cause race condition.

-
- Assume that the 5 threads execute sequentially with no interleaving then after each thread ends the counter value increments by 1. Hence after 5 threads finish, counter value will be incremented 5 times from 0 to 5. **Possible.**
 - Let's assume that a process used 2 waits and reads the counter value and didn't update the value yet, all the other process let's say the other processes executed sequentially incremented and stored the value as 4 but since the value isn't written the first process yet the current value is overwritten by the first process as 1. **Possible**
 - There exists no pattern of execution in which the process increments the current value and completes while maintaining 0 as the counter value. **Not possible**
 - Assume that all the process use up the first wait operation, the semaphore value will now become zero and deadlock

would've occurred. **Possible**

4 votes

-- Cringe is my middle name... (885 points)

5.19.8 Semaphores: GATE IT 2006 | Question: 57 [top](#)

<https://gateoverflow.in/3601>



- `x_count` is the number of processes waiting on semaphore `x_sem`, initially 0,

`x_count` is incremented and decremented in `x.wait`, which shows that in between them `wait(x_sem)` must happen which is `P(x_sem)`. Correspondingly `V(x_sem)` must happen in `x.signal`. So, D choice.

What is a [monitor](#)?

References



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18 votes

-- Arjun Suresh (332k points)

5.20

System Call (1) [top](#)

5.20.1 System Call: GATE CSE 2021 Set 1 | Question: 14 [top](#)

<https://gateoverflow.in/357438>



Which of the following standard *C* library functions will *always* invoke a system call when executed from a single-threaded process in a UNIX/Linux operating system?

- A. `exit`
- B. `malloc`
- C. `sleep`
- D. `strlen`

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multiple-selects

operating-system

system-call

Answer

Answers: System Call

5.20.1 System Call: GATE CSE 2021 Set 1 | Question: 14 [top](#)

<https://gateoverflow.in/357438>



System calls are used to get some service from operating system which generally requires some higher level of privilege.

This question uses two important words “always” and “standard C library functions”.

Let's check options

1. **exit**- This is a function defined in standard C library and it **always** invokes system call every time, flushes the streams, and terminates the caller.
2. **malloc** – This is a function defined in standard C library and it **does not always** invoke the system call. When a process is created, certain amount of heap memory is already allocated to it, when required to expand or shrink that memory, it internally uses `sbrk/brk` system call on Unix/Linux. i.e., **not every malloc** call needs a system call but if the current allocated size is not enough, it'll do a system call to get more memory.
3. **sleep**- This is not even standard C library function, it is a POSIX standard C library function. Unix and Windows uses different header files for it. Now as question has said the *following standard C library* function, let's consider it as that way. Yes it **always** invokes the system call.
4. **strlen** – This is a function defined in standard C library and **doesn't** require any system call to perform its function of calculating the string length.

Answer : A,C

4 votes

-- Persistent (89 points)

5.21

Threads (8) [top](#)



Consider the following statements with respect to user-level threads and kernel-supported threads

- I. context switch is faster with kernel-supported threads
- II. for user-level threads, a system call can block the entire process
- III. Kernel supported threads can be scheduled independently
- IV. User level threads are transparent to the kernel

Which of the above statements are true?

- A. (II), (III) and (IV) only
- B. (II) and (III) only
- C. (I) and (III) only
- D. (I) and (II) only

gate2004-cse operating-system threads normal

Answer



Consider the following statements about user level threads and kernel level threads. Which one of the following statements is FALSE?

- A. Context switch time is longer for kernel level threads than for user level threads.
- B. User level threads do not need any hardware support.
- C. Related kernel level threads can be scheduled on different processors in a multi-processor system.
- D. Blocking one kernel level thread blocks all related threads.

gate2007-cse operating-system threads normal

Answer



A thread is usually defined as a light weight process because an Operating System (OS) maintains smaller data structure for a thread than for a process. In relation to this, which of the following statement is correct?

- A. OS maintains only scheduling and accounting information for each thread
- B. OS maintains only CPU registers for each thread
- C. OS does not maintain virtual memory state for each thread
- D. OS does not maintain a separate stack for each thread

gate2011-cse operating-system threads normal ugcnetjune2013iii

Answer



Which one of the following is FALSE?

- A. User level threads are not scheduled by the kernel.
- B. When a user level thread is blocked, all other threads of its process are blocked.
- C. Context switching between user level threads is faster than context switching between kernel level threads.
- D. Kernel level threads cannot share the code segment.

gate2014-cse-set1 operating-system threads normal

Answer



Threads of a process share

- A. global variables but not heap
- B. heap but not global variables
- C. neither global variables nor heap
- D. both heap and global variables

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gate2017-cse-set1

operating-system

threads

Answer



Which of the following is/are shared by all the threads in a process?

- I. Program counter
- II. Stack
- III. Address space
- IV. Registers

- A. (I) and (II) only
- B. (III) only
- C. (IV) only
- D. (III) and (IV) only

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gate2017-cse-set2

operating-system

threads

Answer



Consider the following multi-threaded code segment (in a mix of C and pseudo-code), invoked by two processes P_1 and P_2 , and each of the processes spawns two threads T_1 and T_2 :

```
int x = 0; // global
Lock L1; // global
main () {
    create a thread to execute foo(); // Thread T1
    create a thread to execute foo(); // Thread T2
    wait for the two threads to finish execution;
    print(x);
}

foo() {
    int y = 0;
    Acquire L1;
    x = x + 1;
    y = y + 1;
    Release L1;
    print(y);
}
```

Which of the following statement(s) is/are correct?

- A. Both P_1 and P_2 will print the value of x as 2.
- B. At least of P_1 and P_2 will print the value of x as 4.
- C. At least one of the threads will print the value of y as 2.
- D. Both T_1 and T_2 , in both the processes, will print the value of y as 1.

gate2021-cse-set2

multiple-selects

operating-system

threads

Answer



Which one of the following is NOT shared by the threads of the same process ?

- A. Stack
- B. Address Space
- C. File Descriptor Table
- D. Message Queue

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Answer

Answers: Threads

5.21.1 Threads: GATE CSE 2004 | Question: 11 top

<https://gateoverflow.in/1008>

✓ Answer: (A)

- I. User level thread switching is faster than kernel level switching. So, (I) is false.
- II. is true.
- III. is true.
- IV. User level threads are transparent to the kernel

In case of Computing transparent means functioning without being aware. In our case user level threads are functioning without kernel being aware about them. So (IV) is actually correct.

👍 61 votes

-- Akash Kanase (36k points)

User level threads can switch almost as fast as a procedure call. Kernel supported threads switch much slower. So, I is false.

II, III and IV are TRUE. So A.

"The kernel knows nothing about user-level threads and manages them as if they were single-threaded processes"

Ref: <http://stackoverflow.com/questions/15983872/difference-between-user-level-and-kernel-supported-threads>

References



👍 32 votes

-- Arjun Suresh (332k points)

5.21.2 Threads: GATE CSE 2007 | Question: 17 top

<https://gateoverflow.in/1215>

✓ Answer: (D)

- A. Context switch time is longer for kernel level threads than for user level threads. — This is True, as Kernel level threads are managed by OS and Kernel maintains lot of data structures. There are many overheads involved in Kernel level thread management, which are not present in User level thread management !
- B. User level threads do not need any hardware support.— This is true, as User level threads are implemented by Libraries programmably, Kernel does not sees them.
- C. Related kernel level threads can be scheduled on different processors in a multi-processor system.— This is true.
- D. Blocking one kernel level thread blocks all related threads. — This is false. If it had been user Level threads this would have been true, (In One to one, or many to one model !) Kernel level threads are independent.

👍 50 votes

-- Akash Kanase (36k points)

5.21.3 Threads: GATE CSE 2011 | Question: 16, UGCNET-June2013-III: 65 top

<https://gateoverflow.in/2115>

✓ Answer to this question is (C).

Many of you would not agree at first So here I explain it how.

OS , on per thread basis, maintains ONLY TWO things : CPU Register state and Stack space. It does not maintain anything else for individual thread. Code segment and Global variables are shared. Even TLB and Page Tables are also shared since they belong to same process.

- A. option (A) would have been correct if 'ONLY' word were not there. It NOT only maintains register state BUT stack space also.

- B. is obviously FALSE
- C. is TRUE as it says that OS does not maintain VIRTUAL Memory state for individual thread which is TRUE
- D. This is also FALSE.

83 votes

-- Sandeep_Uniyal (6.5k points)

5.21.4 Threads: GATE CSE 2014 Set 1 | Question: 20 top

<https://gateoverflow.in/1787>



✓ (D) is the answer. Threads can share the Code segments. They have only separate Registers and stack.

User level threads are scheduled by the thread library and kernel knows nothing about it. So, A is TRUE.

When a user level thread is blocked, all other threads of its process are blocked. So, B is TRUE. (With a multi-threaded kernel, user level threads can make non-blocking system calls without getting blocked. But in this option, it is explicitly said 'a thread is blocked'.)

Context switching between user level threads is faster as they actually have no context-switch- nothing is saved and restored while for kernel level thread, Registers, PC and SP must be saved and restored. So, C also TRUE.

Reference: http://www.cs.cornell.edu/courses/cs4410/2008fa/homework/hw1_soln.pdf

References



49 votes

-- Sandeep_Uniyal (6.5k points)

5.21.5 Threads: GATE CSE 2017 Set 1 | Question: 18 top

<https://gateoverflow.in/118298>



✓ A thread shares with other threads a process's (to which it belongs to) :

- Code section
- Data section (static + heap)
- Address Space
- Permissions
- Other resources (e.g. files)

Therefore, (D) is the answer.

52 votes

-- Kantikumar (3.4k points)

5.21.6 Threads: GATE CSE 2017 Set 2 | Question: 07 top

<https://gateoverflow.in/118240>



✓ Thread is light weight process, and every thread have its own, stack, register, and PC (one of the register in CPU contain address of next instruction to be executed), so only address space that is shared by all thread for a single process. So, option (B) is correct answer.

35 votes

-- 2018 (5.5k points)

5.21.7 Threads: GATE CSE 2021 Set 2 | Question: 42 top

<https://gateoverflow.in/357498>



✓ Each process has its own address space.

1. P_1 :

Two threads T_{11}, T_{12} are created in main.

Both execute foo function and threads don't wait for each other. Due to explicit locking mechanism here mutual exclusion is there and hence no race condition inside foo().

y being thread local, both the threads will print the value of y as 1.

Due to the wait in main, the print(x) will happen only after both the threads finish. So, x will have become 2.

PS: Even if x was not assigned 0 explicitly in C all global and static variables are initialized to 0 value.

2. P_2 :

Same thing happens here as P_1 as this is a different process. For sharing data among different processes mechanisms like shared memory, files, sockets etc must be used.

So, the correct answer here is A and D.

- Suppose wait is removed from the main(). Then the possible x values can be 0, 1, 2 as the main thread as well as the two created threads can execute in any order.
- Suppose locking mechanism is removed from foo() and assignments are not atomic. (If increment is atomic here, then locking is not required). Then race condition can happen and so one of the increments can overwrite the other. So, in main, x value printed can be either 1 or 2.
- Now suppose we had just one process which does a fork() inside main before creating the threads. How the answer should change?

6 votes

-- Arjun Suresh (332k points)

5.21.8 Threads: GATE IT 2004 | Question: 14 top

<https://gateoverflow.in/3655>



✓ Stack is not shared

29 votes

-- Sankaranarayanan P.N (8.5k points)

5.22

Virtual Memory (39) top

5.22.1 Virtual Memory: GATE CSE 1989 | Question: 2-iv top

<https://gateoverflow.in/87081>



Match the pairs in the following:

(A) Virtual memory	(p) Temporal Locality
(B) Shared memory	(q) Spatial Locality
(C) Look-ahead buffer	(r) Address Translation
(D) Look-aside buffer	(s) Mutual Exclusion

match-the-following gate1989 operating-system virtual-memory

Answer

5.22.2 Virtual Memory: GATE CSE 1990 | Question: 1-v top

<https://gateoverflow.in/83833>



Under paged memory management scheme, simple lock and key memory protection arrangement may still be required if the _____ processors do not have address mapping hardware.

gate1990 operating-system virtual-memory fill-in-the-blanks

Answer

5.22.3 Virtual Memory: GATE CSE 1990 | Question: 7-b top

<https://gateoverflow.in/85404>



In a two-level virtual memory, the memory access time for main memory, $t_M = 10^{-8}$ sec, and the memory access time for the secondary memory, $t_D = 10^{-3}$ sec. What must be the hit ratio, H such that the access efficiency is within 80 percent of its maximum value?

gate1990 descriptive operating-system virtual-memory

Answer

5.22.4 Virtual Memory: GATE CSE 1991 | Question: 03-xi top

<https://gateoverflow.in/525>



Indicate all the false statements from the statements given below:

- The amount of virtual memory available is limited by the availability of the secondary memory
- Any implementation of a critical section requires the use of an indivisible machine- instruction ,such as test-and-set.

- C. The use of monitors ensure that no dead-locks will be caused .
- D. The LRU page-replacement policy may cause thrashing for some type of programs.
- E. The best fit techniques for memory allocation ensures that memory will never be fragmented.

gate1991 operating-system virtual-memory normal multiple-selects

Answer 

5.22.5 Virtual Memory: GATE CSE 1994 | Question: 1.21 top

<https://gateoverflow.in/2464>



Which one of the following statements is true?

- A. Macro definitions cannot appear within other macro definitions in assembly language programs
- B. Overlaying is used to run a program which is longer than the address space of a computer
- C. Virtual memory can be used to accommodate a program which is longer than the address space of a computer
- D. It is not possible to write interrupt service routines in a high level language

gate1994 operating-system normal virtual-memory

Answer 

5.22.6 Virtual Memory: GATE CSE 1995 | Question: 1.7 top

<https://gateoverflow.in/2594>



In a paged segmented scheme of memory management, the segment table itself must have a page table because

- A. The segment table is often too large to fit in one page
- B. Each segment is spread over a number of pages
- C. Segment tables point to page tables and not to the physical locations of the segment
- D. The processor's description base register points to a page table

gate1995 operating-system virtual-memory normal

Answer 

5.22.7 Virtual Memory: GATE CSE 1995 | Question: 2.16 top

<https://gateoverflow.in/2628>



In a virtual memory system the address space specified by the address lines of the CPU must be _____ than the physical memory size and _____ than the secondary storage size.

- A. smaller, smaller
- B. smaller, larger
- C. larger, smaller
- D. larger, larger

gate1995 operating-system virtual-memory normal

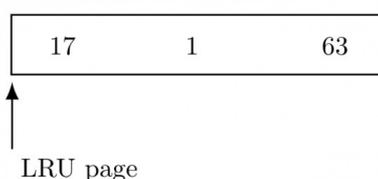
Answer 

5.22.8 Virtual Memory: GATE CSE 1996 | Question: 7 top

<https://gateoverflow.in/2759>



A demand paged virtual memory system uses 16 bit virtual address, page size of 256 bytes, and has 1 Kbyte of main memory. LRU page replacement is implemented using the list, whose current status (page number is decimal) is



For each hexadecimal address in the address sequence given below,

00FF, 010D, 10FF, 11B0

indicate

- i. the new status of the list
- ii. page faults, if any, and
- iii. page replacements, if any.

gate1996 operating-system virtual-memory normal descriptive

Answer

5.22.9 Virtual Memory: GATE CSE 1998 | Question: 2.18, UGCNET-June2012-III: 48

<https://gateoverflow.in/1691>



If an instruction takes i microseconds and a page fault takes an additional j microseconds, the effective instruction time if on the average a page fault occurs every k instruction is:

- A. $i + \frac{j}{k}$
- B. $i + (j \times k)$
- C. $\frac{i + j}{k}$
- D. $(i + j) \times k$

gate1998 operating-system virtual-memory easy ugcnetjune2012iii

Answer

5.22.10 Virtual Memory: GATE CSE 1999 | Question: 19

<https://gateoverflow.in/1518>



A certain computer system has the segmented paging architecture for virtual memory. The memory is byte addressable. Both virtual and physical address spaces contain 2^{16} bytes each. The virtual address space is divided into 8 non-overlapping equal size segments. The memory management unit (MMU) has a hardware segment table, each entry of which contains the physical address of the page table for the segment. Page tables are stored in the main memory and consists of 2 byte page table entries.

- a. What is the minimum page size in bytes so that the page table for a segment requires at most one page to store it? Assume that the page size can only be a power of 2.
- b. Now suppose that the pages size is 512 bytes. It is proposed to provide a TLB (Transaction look-aside buffer) for speeding up address translation. The proposed TLB will be capable of storing page table entries for 16 recently referenced virtual pages, in a fast cache that will use the direct mapping scheme. What is the number of tag bits that will need to be associated with each cache entry?
- c. Assume that each page table entry contains (besides other information) 1 valid bit, 3 bits for page protection and 1 dirty bit. How many bits are available in page table entry for storing the aging information for the page? Assume that the page size is 512 bytes.

gate1999 operating-system virtual-memory normal descriptive

Answer

5.22.11 Virtual Memory: GATE CSE 1999 | Question: 2.10

<https://gateoverflow.in/1488>



A multi-user, multi-processing operating system cannot be implemented on hardware that does not support

- A. Address translation
- B. DMA for disk transfer
- C. At least two modes of CPU execution (privileged and non-privileged)
- D. Demand paging

gate1999 operating-system normal virtual-memory

Answer



Which of the following is/are advantage(s) of virtual memory?

- A. Faster access to memory on an average.
- B. Processes can be given protected address spaces.
- C. Linker can assign addresses independent of where the program will be loaded in physical memory.
- D. Program larger than the physical memory size can be run.

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gate1999 operating-system virtual-memory easy

Answer



Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

- A. 1.9999 milliseconds
- B. 1 millisecond
- C. 9.999 microseconds
- D. 1.9999 microseconds

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gate2000-cse operating-system easy virtual-memory

Answer



Where does the swap space reside?

- A. RAM
- B. Disk
- C. ROM
- D. On-chip cache

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gate2001-cse operating-system easy virtual-memory

Answer



Which of the following statements is false?

- A. Virtual memory implements the translation of a program's address space into physical memory address space
- B. Virtual memory allows each program to exceed the size of the primary memory
- C. Virtual memory increases the degree of multiprogramming
- D. Virtual memory reduces the context switching overhead

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gate2001-cse operating-system virtual-memory normal

Answer



Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size is 4 KB, what is the approximate size of the page table?

- A. 16 MB
- B. 8 MB
- C. 2 MB
- D. 24 MB

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gate2001-cse operating-system virtual-memory normal

Answer 

5.22.17 Virtual Memory: GATE CSE 2002 | Question: 19 [top](#)

<https://gateoverflow.in/872>



A computer uses $32 - \textit{bit}$ virtual address, and $32 - \textit{bit}$ physical address. The physical memory is byte addressable, and the page size is 4 Kbytes. It is decided to use two level page tables to translate from virtual address to physical address. Equal number of bits should be used for indexing first level and second level page table, and the size of each table entry is 4 bytes.

- Give a diagram showing how a virtual address would be translated to a physical address.
- What is the number of page table entries that can be contained in each page?
- How many bits are available for storing protection and other information in each page table entry?

gate2002-cse operating-system virtual-memory normal descriptive

Answer 

5.22.18 Virtual Memory: GATE CSE 2003 | Question: 26 [top](#)

<https://gateoverflow.in/916>



In a system with 32 bit virtual addresses and 1 KB page size, use of one-level page tables for virtual to physical address translation is not practical because of

- the large amount of internal fragmentation
- the large amount of external fragmentation
- the large memory overhead in maintaining page tables
- the large computation overhead in the translation process

gate2003-cse operating-system virtual-memory normal

Answer 

5.22.19 Virtual Memory: GATE CSE 2003 | Question: 78 [top](#)

<https://gateoverflow.in/788>



A processor uses 2 - *level* page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest 0.5 ns)

- 1.5 ns
- 2 ns
- 3 ns
- 4 ns

gate2003-cse operating-system normal virtual-memory

Answer 

5.22.20 Virtual Memory: GATE CSE 2003 | Question: 79 [top](#)

<https://gateoverflow.in/43578>



A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Suppose a process has only the following pages in its virtual address space: two contiguous code pages starting at virtual address $0x00000000$, two contiguous data pages starting at virtual address $0x00400000$, and a stack page starting at virtual address $0xFFFFF000$. The amount of memory required for storing the page tables of this process is

- A. 8 KB
- B. 12 KB
- C. 16 KB
- D. 20 KB

gate2003-cse operating-system normal virtual-memory

Answer

5.22.21 Virtual Memory: GATE CSE 2006 | Question: 62, ISRO2016-50 top

<https://gateoverflow.in/1840>



A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

- A. 11 bits
- B. 13 bits
- C. 15 bits
- D. 20 bits

gate2006-cse operating-system virtual-memory normal isro2016

Answer

5.22.22 Virtual Memory: GATE CSE 2006 | Question: 63, UGCNET-June2012-III: 45 top

<https://gateoverflow.in/1841>



A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?

- A. Efficient implementation of multi-user support is no longer possible
- B. The processor cache organization can be made more efficient now
- C. Hardware support for memory management is no longer needed
- D. CPU scheduling can be made more efficient now

gate2006-cse operating-system virtual-memory normal ugcnetjune2012iii

Answer

5.22.23 Virtual Memory: GATE CSE 2008 | Question: 67 top

<https://gateoverflow.in/490>



A processor uses 36 bit physical address and 32 bit virtual addresses, with a page frame size of 4 Kbytes. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows:

- Bits 30 – 31 are used to index into the first level page table.
- Bits 21 – 29 are used to index into the 2nd level page table.
- Bits 12 – 20 are used to index into the 3rd level page table.
- Bits 0 – 11 are used as offset within the page.

The number of bits required for addressing the next level page table(or page frame) in the page table entry of the first, second and third level page tables are respectively

- A. 20,20,20
- B. 24,24,24
- C. 24,24,20
- D. 25,25,24

gate2008-cse operating-system virtual-memory normal

Answer

5.22.24 Virtual Memory: GATE CSE 2009 | Question: 10 top

<https://gateoverflow.in/1302>



The essential content(s) in each entry of a page table is / are

- A. Virtual page number

- B. Page frame number
- C. Both virtual page number and page frame number
- D. Access right information

gate2009-cse operating-system virtual-memory easy

Answer 

5.22.25 Virtual Memory: GATE CSE 2009 | Question: 34 [top](#)

<https://gateoverflow.in/1320>



A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because

- A. It reduces the memory access time to read or write a memory location.
- B. It helps to reduce the size of page table needed to implement the virtual address space of a process
- C. It is required by the translation lookaside buffer.
- D. It helps to reduce the number of page faults in page replacement algorithms.

gate2009-cse operating-system virtual-memory easy

Answer 

5.22.26 Virtual Memory: GATE CSE 2011 | Question: 20, UGCNET-June2013-II: 48 [top](#)

<https://gateoverflow.in/2122>



Let the page fault service time be 10 milliseconds(ms) in a computer with average memory access time being 20 nanoseconds (ns). If one page fault is generated every 10^6 memory accesses, what is the effective access time for memory?

- A. 21 ns
- B. 30 ns
- C. 23 ns
- D. 35 ns

gate2011-cse operating-system virtual-memory normal ugcnetjune2013ii

Answer 

5.22.27 Virtual Memory: GATE CSE 2013 | Question: 52 [top](#)

<https://gateoverflow.in/379>



A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T_1), which occupies exactly one page. Each entry of T_1 stores the base address of a page of the second-level table (T_2). Each entry of T_2 stores the base address of a page of the third-level table (T_3). Each entry of T_3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the size of a page in KB in this computer?

- A. 2
- B. 4
- C. 8
- D. 16

gate2013-cse operating-system virtual-memory normal

Answer 

5.22.28 Virtual Memory: GATE CSE 2013 | Question: 53 [top](#)

<https://gateoverflow.in/43294>



A computer uses 46-bit virtual address, 32-bit physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T_1), which occupies exactly one page. Each entry of T_1 stores the base address of a page of the second-level table (T_2). Each entry of T_2 stores the base address of a page of the third-level table (T_3). Each entry of T_3 stores a page table entry (PTE). The PTE is 32 bits in size. The processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes.

What is the minimum number of page colours needed to guarantee that no two synonyms map to different sets in the processor cache of this computer?

- A. 2
- B. 4
- C. 8
- D. 16

gate2013-cse normal operating-system virtual-memory

Answer 

5.22.29 Virtual Memory: GATE CSE 2014 Set 3 | Question: 33 [top](#) 

<https://gateoverflow.in/2067>



Consider a paging hardware with a *TLB*. Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the *TLB* and 80 milliseconds to access the physical memory. If the *TLB* hit ratio is 0.6, the effective memory access time (in milliseconds) is _____.

gate2014-cse-set3 operating-system virtual-memory numerical-answers normal

Answer 

5.22.30 Virtual Memory: GATE CSE 2015 Set 1 | Question: 12 [top](#) 

<https://gateoverflow.in/8186>



Consider a system with byte-addressable memory, 32 – bit logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in megabytes is _____.

gate2015-cse-set1 operating-system virtual-memory easy numerical-answers

Answer 

5.22.31 Virtual Memory: GATE CSE 2015 Set 2 | Question: 25 [top](#) 

<https://gateoverflow.in/8120>



A computer system implements a 40 – bit virtual address, page size of 8 kilobytes, and a 128 – entry translation look-aside buffer (*TLB*) organized into 32 sets each having 4 ways. Assume that the *TLB* tag does not store any process id. The minimum length of the *TLB* tag in bits is _____.

gate2015-cse-set2 operating-system virtual-memory easy numerical-answers

Answer 

5.22.32 Virtual Memory: GATE CSE 2015 Set 2 | Question: 47 [top](#) 

<https://gateoverflow.in/8247>



A computer system implements 8 kilobyte pages and a 32 – bit physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is _____ bits.

gate2015-cse-set2 operating-system virtual-memory normal numerical-answers

Answer 

5.22.33 Virtual Memory: GATE CSE 2016 Set 1 | Question: 47 [top](#) 

<https://gateoverflow.in/39690>



Consider a computer system with 40-bit virtual addressing and page size of sixteen kilobytes. If the computer system has a one-level page table per process and each page table entry requires 48 bits, then the size of the per-process page table is _____ megabytes.

gate2016-cse-set1 operating-system virtual-memory easy numerical-answers

Answer 

5.22.34 Virtual Memory: GATE CSE 2018 | Question: 10 [top](#) 

<https://gateoverflow.in/204084>



Consider a process executing on an operating system that uses demand paging. The average time for a memory access in the system is M units if the corresponding memory page is available in memory, and D units if the memory access causes a page fault.

It has been experimentally measured that the average time taken for a memory access in the process is X units.

Which one of the following is the correct expression for the page fault rate experienced by the process.

- A. $(D - M)/X - M$
- B. $(X - M)/D - M$
- C. $(D - X)/D - M$
- D. $(X - M)/D - X$

gate2018-cse operating-system virtual-memory normal

Answer

5.22.35 Virtual Memory: GATE CSE 2019 | Question: 33

<https://gateoverflow.in/302815>



Assume that in a certain computer, the virtual addresses are 64 bits long and the physical addresses are 48 bits long. The memory is word addressable. The page size is 8 kB and the word size is 4 bytes. The Translation Look-aside Buffer (TLB) in the address translation path has 128 valid entries. At most how many distinct virtual addresses can be translated without any TLB miss?

- A. 16×2^{10}
- B. 256×2^{10}
- C. 4×2^{20}
- D. 8×2^{20}

gate2019-cse operating-system virtual-memory

Answer

5.22.36 Virtual Memory: GATE CSE 2020 | Question: 53

<https://gateoverflow.in/333178>



Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. The average memory access time in ns (round off to 1 decimal places) is _____

gate2020-cse numerical-answers operating-system virtual-memory

Answer

5.22.37 Virtual Memory: GATE IT 2004 | Question: 66

<https://gateoverflow.in/3709>



In a virtual memory system, size of the virtual address is 32-bit, size of the physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

- A. 2
- B. 10
- C. 12
- D. 14

gate2004-it operating-system virtual-memory normal

Answer

5.22.38 Virtual Memory: GATE IT 2008 | Question: 16

<https://gateoverflow.in/3276>



A paging scheme uses a Translation Look-aside Buffer (TLB). A TLB-access takes 10 ns and the main memory access takes 50 ns. What is the effective access time(in ns) if the TLB hit ratio is 90% and there is no page-fault?

- A. 54
- B. 60
- C. 65
- D. 75

gate2008-it operating-system virtual-memory normal

Answer

5.22.39 Virtual Memory: GATE IT 2008 | Question: 56

https://gateoverflow.in/3366



Match the following flag bits used in the context of virtual memory management on the left side with the different purposes on the right side of the table below.

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Name of the bit	Purpose
I. Dirty	a. Page initialization
II. R/W	b. Write-back policy
III. Reference	c. Page protection
IV. Valid	d. Page replacement policy

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- A. I-d, II-a, III-b, IV-c
- B. I-b, II-c, III-a, IV-d
- C. I-c, II-d, III-a, IV-b
- D. I-b, II-c, III-d, IV-a

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gate2008-it operating-system virtual-memory easy

Answer

Answers: Virtual Memory

5.22.1 Virtual Memory: GATE CSE 1989 | Question: 2-iv

https://gateoverflow.in/87081



✓

(A) Virtual memory	(r) Address Translation
(B) Shared memory	(s) Mutual Exclusion
(C) Look-ahead buffer	(q) Spatial Locality
(D) Look-aside buffer	(p) Temporal Locality

<https://gateoverflow.in/3304/difference-between-translation-buffer-translation-buffer>

References



24 votes

-- Prashant Singh (47.2k points)

5.22.2 Virtual Memory: GATE CSE 1990 | Question: 1-v

https://gateoverflow.in/83833



i/o processors because processor will issue address for device controller and if there is no translation hardware then it ain't gonna be peachy.

14 votes

-- ashish gusai (523 points)

5.22.3 Virtual Memory: GATE CSE 1990 | Question: 7-b

https://gateoverflow.in/85404



In 2 level virtual memory, for every memory access, we need 2 page table access (TLB is missing in the question) and 1 memory access for data. In the question TLB is not mentioned (old architecture). So, best case memory access time

$$= 3 \times 10^{-8} \text{ s.}$$

We are given

$$3 \times 10^{-8} = 0.8 \left[\begin{matrix} 3 \times 10^{-8} \\ \text{2 for Page Tables and 1 Mem} \end{matrix} + (1 - h) \times 10^{-3} \right]$$

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(For above, the main memory access time and page table access times are included for all memory accesses -- hence h is not multiplied with 3×10^{-8})

$$\implies 0.6 \times 10^{-8} = 0.8 \times 10^{-3} - 0.8h \times 10^{-3} \implies h = \frac{8 \times 10^{-4} - 6 \times 10^{-9}}{8 \times 10^{-4}} = 1 - 0.75 \times 10^{-5} \approx 99.99\%$$

46 votes

-- Arjun Suresh (332k points)

5.22.4 Virtual Memory: GATE CSE 1991 | Question: 03-xi top

<https://gateoverflow.in/525>



✓

- A. True.
- B. This is false. Example:- Peterson's solution is a purely software-based solution without the use of hardware. https://en.wikipedia.org/wiki/Peterson's_algorithm
- C. False. Reference: [https://en.wikipedia.org/wiki/Monitor_\(synchronization\)](https://en.wikipedia.org/wiki/Monitor_(synchronization))
- D. True. This will happen if the page getting replaced is immediately referred to in the next cycle.
- E. False. Memory can get fragmented with the best fit.

References



29 votes

-- Akash Kanase (36k points)

5.22.5 Virtual Memory: GATE CSE 1994 | Question: 1.21 top

<https://gateoverflow.in/2464>



✓

- A. Is TRUE.
- B. False. [Overlaying](#) is used to increase the address space usage when physical memory is limited on systems where virtual memory is absent. But it cannot increase the address space (logical) of a computer.
- C. False. Like above is true for physical memory but here it is specified address space which should mean logical address space.
- D. Is false. We can write in high level language just that the [performance will be bad](#).

References



24 votes

-- Arjun Suresh (332k points)

5.22.6 Virtual Memory: GATE CSE 1995 | Question: 1.7 top

<https://gateoverflow.in/2594>



✓

Option (B) is true for segmented paging(segment size becomes large so paging done on each segment) which is different from paged segmentation(segment table size becomes large and paging done on segment table)

Here option (A) is true, as segment table are sometimes too large to keep in one pages. So, segment table divided into pages. Thus page table for each Segment Table pages are created.

For reference, read below:

<https://stackoverflow.com/questions/16643180/differences-or-similarities-between-segmented-paging-and-paged-segmentation>
Differences or similarities between Segmented paging and Paged segmentation scheme.

References

[classroom.gateoverflow.in](https://stackoverflow.com/questions/16643180/differences-or-similarities-between-segmented-paging-and-paged-segmentation)

[gateoverflow.in](https://stackoverflow.com/questions/16643180/differences-or-similarities-between-segmented-paging-and-paged-segmentation)

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44 votes

-- Anurag Semwal (6.7k points)

5.22.7 Virtual Memory: GATE CSE 1995 | Question: 2.16 top

https://gateoverflow.in/2628



✓ Answer is (C).

Primary memory < virtual memory < secondary memory

We can extend VM upto the size of disk(secondary memory).

27 votes

-- jayendra (6.7k points)

5.22.8 Virtual Memory: GATE CSE 1996 | Question: 7 top

https://gateoverflow.in/2759



✓ Given that page size is 256 bytes (2^8) and Main memory (MM) is 1KB (2^{10}).

So total number of pages that can be accommodated in MM = $\frac{2^{10}}{2^8} = 4$.

So, essentially, there are 4 frames that can be used for paging (or page replacements).

The current sequence of pages in memory shows 3 pages (17, 1, 63). So, there is 1 empty frame left. It also says that the least recently used page is 17.

Now, since page size given is 8 bits wide (256 B), and virtual memory is of 16 bit, we can say that 8 bits are used for offset. The given address sequence is hexadecimal can be divided accordingly:

Page Number in Hexadecimal	Offset	Page Number in Decimal
00	FF	0
01	0D	1
10	FF	16
11	B0	17

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We only need the Page numbers, which can be represented in decimal as: 0, 1, 16, 17.

Now, if we apply LRU algorithm to the existing frame with these incoming pages, we get the following states:

0	Miss	17	1	63	0
1	Hit	17	1	63	0
16	Miss	16	1	63	0
17	Miss	16	1	17	0

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- New status of the list is **16 1 17 0**.
- Number of page faults = **3**.
- Page replacements are indicated above.

70 votes

-- Ashis Kumar Sahoo (699 points)

5.22.9 Virtual Memory: GATE CSE 1998 | Question: 2.18, UGCNET-June2012-III: 48 top

https://gateoverflow.in/1691



✓ Page fault rate = $\frac{1}{k}$

Page hit rate = $1 - \frac{1}{k}$

Service time = i

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Page fault service time = $i + j$

Effective memory access time,

$$= \frac{1}{k} \times (i + j) + \left(1 - \frac{1}{k}\right) \times i$$

$$= \frac{(i + j)}{k} + i - \frac{i}{k}$$

$$= \frac{i}{k} + \frac{j}{k} + i - \frac{i}{k}$$

$$= i + \frac{j}{k}$$

So, option (A) is correct.

👍 48 votes

-- shashi shekhar (437 points)

5.22.10 Virtual Memory: GATE CSE 1999 | Question: 19 top

<https://gateoverflow.in/1518>



✓

a. Size of each segment = $\frac{2^{16}}{8} = 2^{13}$

Let the size of page be 2^k bytes

We need a page table entry for each page. For a segment of size 2^{13} , number of pages required will be

2^{13-k} and so we need 2^{13-k} page table entries. Now, the size of these many entries must be less than or equal to the page size, for the page table of a segment to be requiring at most one page. So,

$$2^{13-k} \times 2 = 2^k \text{ (As a page table entry size is 2 bytes)}$$

$$k = 7 \text{ bits}$$

$$\text{So, page size} = 2^7 = 128 \text{ bytes}$$

b. The TLB is placed after the segment table.

Each segment will have $\frac{2^{13}}{2^9} = 2^4$ page table entries

So, all page table entries of a segment will reside in the cache and segment number will differentiate between page table entry of each segment in the TLB cache.

$$\text{Total segments} = 8$$

Therefore 3 bits of tag is required

c. Number of Pages for a segment = $\frac{2^{16}}{2^9} = 2^7$

Bits needed for page frame identification

$$= 7 \text{ bits}$$

+1 valid bit

+3 page protection bits

+1 dirty bit

= 12 bits needed for a page table entry

$$\text{Size of each page table entry} = 2 \text{ bytes} = 16 \text{ bits}$$

$$\text{Number of bits left for aging} = 16 - 12 = 4 \text{ bits}$$

👍 36 votes

-- Danish (3.4k points)



- ✓ Answer should be both (A) and (C) (Earlier GATE questions had multiple answers and marks were given only if all correct answers were selected).
Address translation is needed to provide memory protection so that a given process does not interfere with another. Otherwise we must fix the number of processors to some limit and divide the memory space among them -- which is not an "efficient" mechanism.

We also need at least 2 modes of execution to ensure user processes share resources properly and OS maintains control. This is not required for a single user OS like early version of MS-DOS.

Demand paging and DMA enhances the performances- not a strict necessity.

Ref: Hardware protection section in Galvin

👍 49 votes

-- Arjun Suresh (332k points)



- ✓ Virtual memory provides an interface through which processes access the physical memory. So,
- Is false as direct access can never be slower.
 - Is true as without virtual memory it is difficult to give protected address space to processes as they will be accessing physical memory directly. No protection mechanism can be done inside the physical memory as processes are dynamic and number of processes changes from time to time.
 - Position independent can be produced even without virtual memory support.
 - This is one primary use of virtual memory. Virtual memory allows a process to run using a virtual address space and as and when memory space is required, pages are swapped in/out from the disk if physical memory gets full.

So, answer is (B) and (D).

👍 46 votes

-- Arjun Suresh (332k points)



- ✓ Since nothing is told about page tables, we can assume page table access time is included in memory access time.

So, average memory access time

$$\begin{aligned} &= .9999 \times 1 + 0.0001 \times 10,000 \\ &= 0.9999 + 1 \\ &= 1.9999 \text{ microseconds} \end{aligned}$$

Correct Answer: D

👍 46 votes

-- Arjun Suresh (332k points)



- ✓ Option (B) is correct.

Swap space is the area on a hard disk which is part of the Virtual Memory of your machine, which is a combination of accessible physical memory (RAM) and the swap space. Swap space temporarily holds memory pages that are inactive. Swap space is used when your system decides that it needs physical memory for active processes and there is insufficient unused physical memory available. If the system happens to need more memory resources or space, inactive pages in physical memory are then moved to the swap space therefore freeing up that physical memory for other uses. Note that the access time for swap is slower therefore do not consider it to be a complete replacement for the physical memory. Swap space can be a dedicated swap partition (recommended), a swap file, or a combination of swap partitions and swap files.

👍 57 votes

-- Manoj Kumar (26.7k points)



✓ (D) should be the answer.

(A) - MMU does this translation but MMU is part of VM (hardware).

(B), (C) - The main advantage of VM is the increased address space for programs, and independence of address space, which allows more degree of multiprogramming as well as option for process security.

(D) - VM requires switching of page tables (this is done very fast via switching of pointers) for the new process and thus it is theoretically slower than without VM. In anyway VM doesn't directly decrease the context switching overhead.

👍 58 votes

-- Arjun Suresh (332k points)



✓ Number of pages = $2^{32}/4KB = 2^{20}$ as we need to map every possible virtual address.

So, we need 2^{20} entries in the page table. Physical memory being 64 MB, a physical address must be 26 bits and a page (of size 4KB) address needs $26 - 12 = 14$ address bits. So, each page table entry must be at least 14 bits.

So, total size of page table = $2^{20} \times 14 \text{ bits} \approx 2 \text{ MB}$ (assuming PTE is 2 bytes)

Correct Answer: C

👍 54 votes

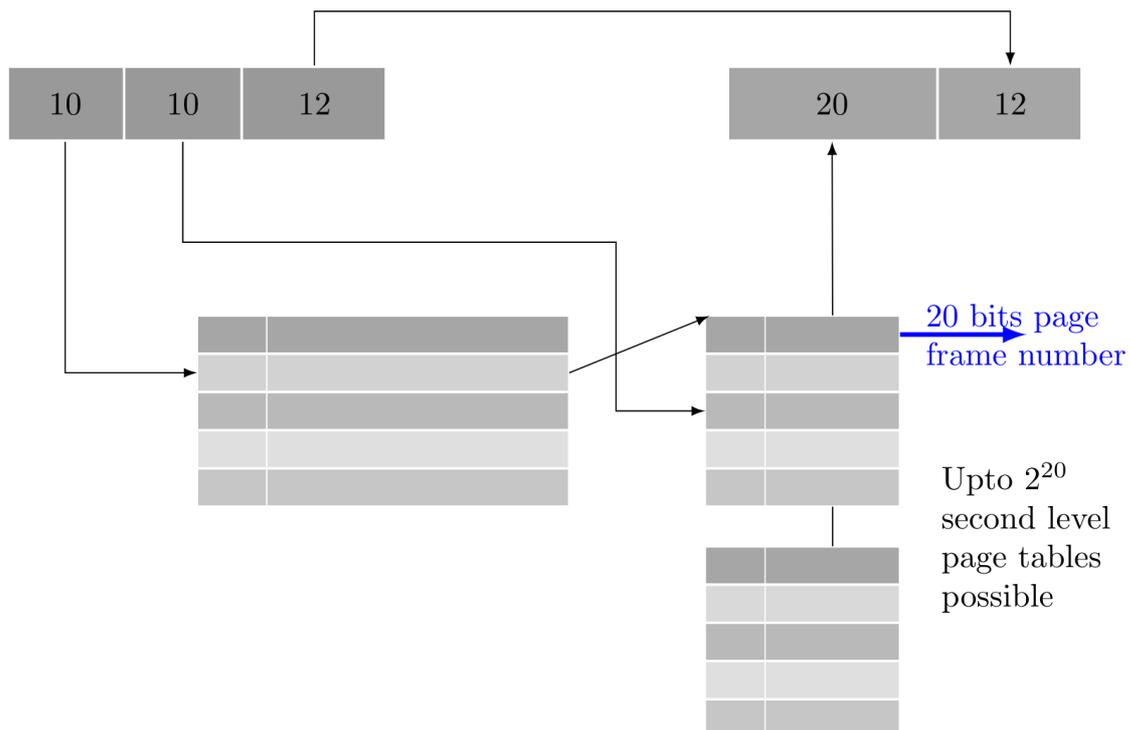
-- Arjun Suresh (332k points)



- VA = 32 bits
- PA = 32 bits
- Page size = 4 KB = $2^{12} B$
- PTE = 4 B

Since page size is 4 KB we need $\lg 4K = 12$ bits as offset bits.

(A) It is given that equal number of bits should be used for indexing first level and second level page table. So, out of the remaining $32 - 12 = 20$ bits 10 bits each must be used for indexing into first level and second level page tables as follows:



(B) Since 10 bits are used for indexing to a page table, number of page table entries possible = $2^{10} = 1024$. This is same for both first level as well as second level page tables.

(C)

Frame no = 32 bit (Physical Address) - 12 (Offset) = 20

No. of bits available for Storing Protection and other information in second level page table

$$= 4 \times 8 - 20$$

$$= 32 - 20 = 12 \text{ bits}$$

No. of bits in first level page table to address a second level page table is \log_2 of

$$\frac{\text{Physical memory size}}{\# \text{Entries in a Second level page table} \times \text{PTE size}}$$

$$= \log_2 \left[\frac{2^{32}}{2^{10} \times 4} \right]$$

$$= \log_2 (2^{20})$$

$$= 20 \text{ bits.}$$

So here also, the no. of bits available for storing protection and other information = $32 - 20 = 12 \text{ bits}$.

👍 43 votes

-- Akash Kanase (36k points)

5.22.18 Virtual Memory: GATE CSE 2003 | Question: 26 [top](#)

<https://gateoverflow.in/916>



✓

- A. Internal fragmentation exists only in the last level of paging.
- B. There is no External fragmentation in the paging.
- C. $\frac{2^{32}}{2^{10}} = 2^{22} = 4M$ entries in the page table which is very large. (Answer)
- D. Not much relevant.

👍 38 votes

-- Abhishek Singhal (233 points)

5.22.19 Virtual Memory: GATE CSE 2003 | Question: 78 [top](#)

<https://gateoverflow.in/788>



✓

78. It's given cache is physically addressed. So, address translation is needed for all memory accesses. (I assume page table lookup happens after TLB is missed, and main memory lookup after cache is missed)

$$\begin{aligned} \text{Average access time} &= \text{Average address translation time} + \text{Average memory access time} \\ &= 1 \text{ ns} \\ &\quad (\text{TLB is accessed for all accesses}) \\ &+ 2 \times 10 \times 0.04 \\ &\quad (2 \text{ page tables accessed from main memory in case of TLB miss}) \\ &+ \text{Average memory access time} \\ &= 1.8 \text{ ns} + \text{Cache access time} + \text{Average main memory access time} \\ &= 1.8 \text{ ns} + 1 \times 0.9 \quad (90\% \text{ cache hit}) \\ &+ 0.1 \times (10+1) \quad (\text{main memory is accessed for cache misses only}) \\ &= 1.8 \text{ ns} + 0.9 + 1.1 \\ &= 3.8 \text{ ns} \end{aligned}$$

We assumed that page table is in main memory and not cached. This is given in question also, though they do not explicitly say that page tables are not cached. But in practice this is common as given [here](#). So, in such a system,

$$\begin{aligned} \text{Average address translation time} &= 1 \text{ ns} \quad (\text{TLB is accessed for all accesses}) \\ &+ 2 \times 0.04 \times [0.9 \times 1 + 0.1 \times 10] \\ &\quad (2 \text{ page tables accessed in case of TLB miss and they go through cache}) \\ &= 1 \text{ ns} + 1.9 \times .08 \\ &= 1.152 \text{ ns} \end{aligned}$$

$$\text{and average memory access time} = 1.152 \text{ ns} + 2 \text{ ns} = 3.152 \text{ ns}$$

! If the same thing is repeated now probably you would get marks for both. 2003 is a long way back -- then page table caching never existed as given in the SE answers. Since it exists now, IIT profs will make this clear in question itself.

References



88 votes

-- gatecse (63.3k points)

5.22.20 Virtual Memory: GATE CSE 2003 | Question: 79 [top](#)

<https://gateoverflow.in/43578>



✓ First level page table is addressed using 10 bits and hence contains 2^{10} entries. Each entry is 4 bytes and hence this table requires 4 KB. Now, the process uses only 3 unique entries from this 1024 possible entries (two code pages starting from $0x00000000$ and two data pages starting from $0x00400000$ have same first 10 bits). Hence, there are only 3 second level page tables. Each of these second level page tables are also addressed using 10 bits and hence of size 4 KB. So,

total page table size of the process
= 4 KB + 3 * 4 KB
= 16 KB

Correct Answer: C

78 votes

-- Arjun Suresh (332k points)

5.22.21 Virtual Memory: GATE CSE 2006 | Question: 62, ISRO2016-50 [top](#)

<https://gateoverflow.in/1940>



✓ The page size of 4 KB. So, offset bits are 12 bits.
So, the remaining bits of virtual address, $32 - 12 = 20$ bits, will be used for indexing.

Number of sets = $128/4 = 32$ (4-way set) \implies 5 bits.

So, tag bits = $20 - 5 = 15$ bits.

Correct option C.

50 votes

-- Vicky Bajoria (4.1k points)

5.22.22 Virtual Memory: GATE CSE 2006 | Question: 63, UGCNET-June2012-III: 45 [top](#)

<https://gateoverflow.in/1941>



✓ A is the best answer here.
Virtual memory provides

1. increased address space for processes
2. memory protection
3. relocation

So, when we don't need more address space, even if we get rid of virtual memory, we need hardware support for the other two. Without hardware support for memory protection and relocation, we can design a system (by either doing them in software or by partitioning the memory for different users) but those are highly inefficient mechanisms. i.e., there we have to divide the physical memory equally among all users and this limits the memory usage per user and also restricts the maximum number of users.

84 votes

-- Arjun Suresh (332k points)

5.22.23 Virtual Memory: GATE CSE 2008 | Question: 67 [top](#)

<https://gateoverflow.in/490>



✓ Physical address is 36 bits. So, number of bits to represent a page frame = $36 - 12 = 24$ bits (12 offset bits as given in question to address 4 KB assuming byte addressing). So, each entry in a third level page table must have 24 bits for addressing the page frames.

A page in logical address space corresponds to a page frame in physical address space. So, in logical address space also we need 12 bits as offset bits. From the logical address which is of 32 bits, we are now left with $32 - 12 = 20$ bits; these 20 bits will be divided into three partitions (as given in the question) so that each partition represents 'which entry' in the i^{th} level page table we are referring to.

- An entry in level i page table determines 'which page table' at $(i + 1)^{th}$ level is being referred.

Now, there is only 1 first level page table. But there can be many second level and third level page tables and "how many" of these exist depends on the physical memory capacity. (In actual the no. of such page tables depend on the memory usage of a given process, but for addressing we need to consider the worst case scenario). The simple formula for getting the number of page tables possible at a level is to divide the available physical memory size by the size of a given level page table.

$$\begin{aligned} \text{Number of third level page tables possible} &= \frac{\text{Physical memory size}}{\text{Size of a third level page table}} \\ &= \frac{2^{36}}{\text{Number of entries in a single third level page table} \times \text{Size of an entry}} \\ &= \frac{2^{36}}{2^9 \times 4} \because (\text{bits } 12-20 \text{ gives } 9 \text{ bits}) \\ &= \frac{2^{36}}{2^{11}} \\ &= 2^{25} \end{aligned}$$

PS: No. of third level page tables possible means the no. of distinct addresses a page table can have. At any given time, no. of page tables at level j is equal to the no. of entries in the level $j - 1$, but here we are considering the **possible** page table addresses.

<http://www.cs.utexas.edu/~lorenzo/corsi/cs372/06F/hw/3sol.html> See Problem 3, second part solution - It clearly says that we should not assume that page tables are page aligned (page table size need not be same as page size unless told so in the question and different level page tables can have different sizes).

So, we need 25 bits in second level page table for addressing the third level page tables.

Similarly we need to find the no. of possible second level page tables and we need to address each of them in first level page table.

Now,

$$\begin{aligned} \text{Number of second level page tables possible} &= \frac{\text{Physical memory size}}{\text{Size of a second level page table}} \\ &= \frac{2^{36}}{\text{Number of entries in a single second level page table} \times \text{Size of an entry}} \\ &= \frac{2^{36}}{2^9 \times 4} \because (\text{bits } 21-29 \text{ gives } 9 \text{ bits}) \\ &= \frac{2^{36}}{2^{11}} \\ &= 2^{25} \end{aligned}$$

So, we need 25 bits for addressing the second level page tables as well.

So, answer is **(D)**.

Video Explanation for Multi-level Paging: <https://youtu.be/bArypfVmPb8>

(Edit:-

There is nothing to edit for such awesome explanation but just adding one of my comment if it is useful - [comment](#). However if anyone finds something to add (or correct) then feel free to do that in my comment.)

References



👍 233 votes

-- Arjun Suresh (332k points)

5.22.24 Virtual Memory: GATE CSE 2009 | Question: 10 top

<https://gateoverflow.in/1302>



✓ It is **(B)**.

The page table contains the page frame number essentially.

👍 25 votes

-- Gate Keeda (15.9k points)

5.22.25 Virtual Memory: GATE CSE 2009 | Question: 34 top

<https://gateoverflow.in/1320>



✓ Option -> **(B)**

A. It reduces the memory access time to read or write a memory location. -> No This is false. Actually because of multi level

paging we increase no of memory accesses.

- B. It helps to reduce the size of page table needed to implement the virtual address space of a process -> This is **true**, In case of big virtual memory page, size of Page table can also be too huge to fit in single Page. So we do multi level paging.
- C. It is required by the translation lookaside buffer.-> Examiner was not being enough creative here, This is false & There is no relation. This option is just given for no reason !
- D. It helps to reduce the number of page faults in page replacement algorithms.-> This is false, we might increase no of page faults. (Due to second / third level page not in memory here !) So this is false.

41 votes

-- Akash Kanase (36k points)

5.22.26 Virtual Memory: GATE CSE 2011 | Question: 20, UGCNET-June2013-II: 48 top

<https://gateoverflow.in/2122>



- ✓ Open slides 12-13 to check :

<http://web.cs.ucla.edu/~ani/classes/cs111.08w/Notes/Lecture%2016.pdf>

$$\begin{aligned} \text{EMAT} &= \frac{1}{10^6} \times 10 \text{ ms} + \left(1 - \frac{1}{10^6}\right) \times 20 \text{ ns} \\ &= 29.99998 \text{ ns} \\ &\approx 30 \text{ ns} \end{aligned}$$

Answer = **option B**

References



61 votes

-- Amar Vashishth (25.2k points)

5.22.27 Virtual Memory: GATE CSE 2013 | Question: 52 top

<https://gateoverflow.in/379>



- ✓ Let the page size be x .

Since virtual address is 46 bits, we have total number of pages = $\frac{2^{46}}{x}$

We should have an entry for each page in last level page table which here is $T3$. So, Number of entries in $T3$ (sum of entries across all possible $T3$ tables) = $\frac{2^{46}}{x}$

Each entry takes 32 bits = 4 bytes. So, total size of $T3$ tables = $\frac{2^{46}}{x} \times 4 = \frac{2^{48}}{x}$ bytes

Now, no. of $T3$ tables will be Total size of $T3$ tables/page table size and for each of these page tables, we must have a $T2$ entry.

Taking $T3$ size as page size, no. of entries across all $T2$ tables = $\frac{\frac{2^{48}}{x}}{x} = \frac{2^{48}}{x^2}$

Now, no. of $T2$ tables (assuming $T2$ size as page size) = $\frac{2^{48}}{x^2} \times 4 \text{ bytes} = \frac{2^{50}}{x^2} = \frac{2^{50}}{x^3}$.

Now, for each of these page table, we must have an entry in $T1$.

So, number of entries in $T1$ = $\frac{2^{50}}{x^3}$

And size of $T1$ = $\frac{2^{50}}{x^3} \times 4 = \frac{2^{52}}{x^3}$

Given in question, size of $T1$ is page size which we took as x . So,

$$x = \frac{2^{52}}{x^3}$$

$$\implies x^4 = 2^{52}$$

$$\implies x = 2^{13}$$

$$\implies x = 8 \text{ KB}$$

Correct Answer: C

👍 144 votes

-- Arjun Suresh (332k points)

I already put it as [comment](#), in case if one skipped it.

One other method to find page size-

We know that all levels page tables must be completely full except outermost, the outermost page table may occupy whole page or less. But in question, it is given that Outermost page table occupies whole page.

Now let page size is 2^p Bytes.

Given that PTE = 32 bits = 4 Bytes = 2^2 Bytes.

Number of entries in any page of any pagetable = page size/PTE = $\frac{2^p}{2^2} = 2^{p-2}$.

Therefore Logical address split is

$\boxed{p-2} \boxed{p-2} \boxed{p-2} \boxed{p}$

logical address space is 46 bits as given. Hence. equation becomes,

$$(p-2) + (p-2) + (p-2) + p = 46$$

$$\Rightarrow p = 13.$$

Therefore, page size is 2^{13} Bytes = **8KB**.

References



👍 137 votes

-- Sachin Mittal (15.8k points)

5.22.28 Virtual Memory: GATE CSE 2013 | Question: 53 [top ⤴](#)

<https://gateoverflow.in/43294>



✓ Let the page size be x .

Since virtual address is 46 bits, we have total number of pages = $\frac{2^{46}}{x}$

We should have an entry for each page in last level page table which here is $T3$. So,

Number of entries in $T3$ (sum of entries across all possible $T3$ tables) = $\frac{2^{46}}{x}$

Each entry takes 32 bits = 4 bytes. So, total size of $T3$ tables = $\frac{2^{46}}{x} \times 4 = \frac{2^{48}}{x}$ bytes

Now, no. of $T3$ tables will be Total size of $T3$ tables/page table size and for each of these page tables, we must have a $T2$ entry.

Taking $T3$ size as page size, no. of entries across all $T2$ tables

$$= \frac{\frac{2^{48}}{x}}{x} = \frac{2^{48}}{x^2}$$

Now, no. of $T2$ tables (assuming $T2$ size as pagesize) = $\frac{2^{48}}{x^2} \times 4$ bytes = $\frac{2^{50}}{x^2} = \frac{2^{50}}{x^3}$.

Now, for each of these page table, we must have an entry in $T1$. So, number of entries in $T1$

$$= \frac{2^{50}}{x^3}$$

And size of $T1$ = $\frac{2^{50}}{x^3} \times 4 = \frac{2^{52}}{x^3}$

Given in question, size of $T1$ is page size which we took as x . So,

$$x = \frac{2^{52}}{x^3}$$

$$\Rightarrow x^4 = 2^{52}$$

$$\Rightarrow x = 2^{13} = 8KB$$

Min. no. of page color bits = No. of set index bits + no. of offset bits – no. of page index bits (This ensures no synonym maps to different sets in the cache)

We have 1MB cache and 64B cache block size. So,

$$\text{number of sets} = 1MB / (64 \text{ B} \times \text{Number of blocks in each set}) = 16K / 16(16 \text{ way set associative}) = 1K = 2^{10}$$

So, we need 10 index bits. Now, each block being $64(2^6)$ bytes means we need 6 offset bits.

And we already found page size = $8KB = 2^{13}$, so 13 bits to index a page

Thus, no. of page color bits = $10 + 6 - 13 = 3$.

With 3 page color bits we need to have $2^3 = 8$ different page colors

More Explanation:

A synonym is a physical page having multiple virtual addresses referring to it. So, what we want is no two synonym virtual addresses to map to two different sets, which would mean a physical page could be in two different cache sets. This problem never occurs in a physically indexed cache as indexing happens via physical address bits and so one physical page can never go to two different sets in cache. In virtually indexed cache, we can avoid this problem by ensuring that the bits used for locating a cache block (index+offset) of the virtual and physical addresses are the same.

In our case we have 6 offset bits +10 bits for indexing. So, we want to make these 16 bits same for both physical and virtual address. One thing is that the page offset bits –13 bits for 8 KB page, is always the same for physical and virtual addresses as they are never translated. So, we don't need to make these 13 bits same. We have to only make the remaining $10 + 6 - 13 = 3$ bits same. Page coloring is a way to do this. Here, all the physical pages are colored and a physical page of one color is mapped to a virtual address by OS in such a way that a set in cache always gets pages of the same color. So, in order to make the 3 bits same, we take all combinations of it ($2^3 = 8$) and colors the physical pages with 8 colors and a cache set always gets a page of one color only. (In page coloring, it is the job of OS to ensure that the 3 bits are the same).

<http://ece.umd.edu/courses/enee646.F2007/Cekleov1.pdf>

<http://cseweb.ucsd.edu/classes/fa14/cse240A-a/pdf/08/CSE240A-MBT-L18-VirtualMemory.ppt.pdf>

https://en.wikipedia.org/wiki/CPU_cache#Address_translation

https://en.wikipedia.org/wiki/Cache_coloring

Correct Answer: C

References



👍 52 votes

-- Arjun Suresh (332k points)

5.22.29 Virtual Memory: GATE CSE 2014 Set 3 | Question: 33 top ⤴

<https://gateoverflow.in/2067>



- ✓ EMAT = TLB hit × (TLB access time + memory access time) + TLB miss(TLB access time + page table access time + memory access time)

$$= 0.6(10 + 80) + 0.4(10 + 80 + 80)$$

$$= 54 + 68$$

$$= 122 \text{ msec}$$

👍 54 votes

-- neha pawar (3.3k points)

5.22.30 Virtual Memory: GATE CSE 2015 Set 1 | Question: 12 top ⤴

<https://gateoverflow.in/8186>



- ✓ total no of pages = $\frac{2^{32}}{2^{12}} = 2^{20}$

We need a PTE for each page and an entry is 4 bytes. So,
 page table size = $4 \times 2^{20} = 2^{22} B = 4MB$

39 votes

-- Anoop Sonkar (4.1k points)



Ans $40 - (5 + 13) = 22$ bits

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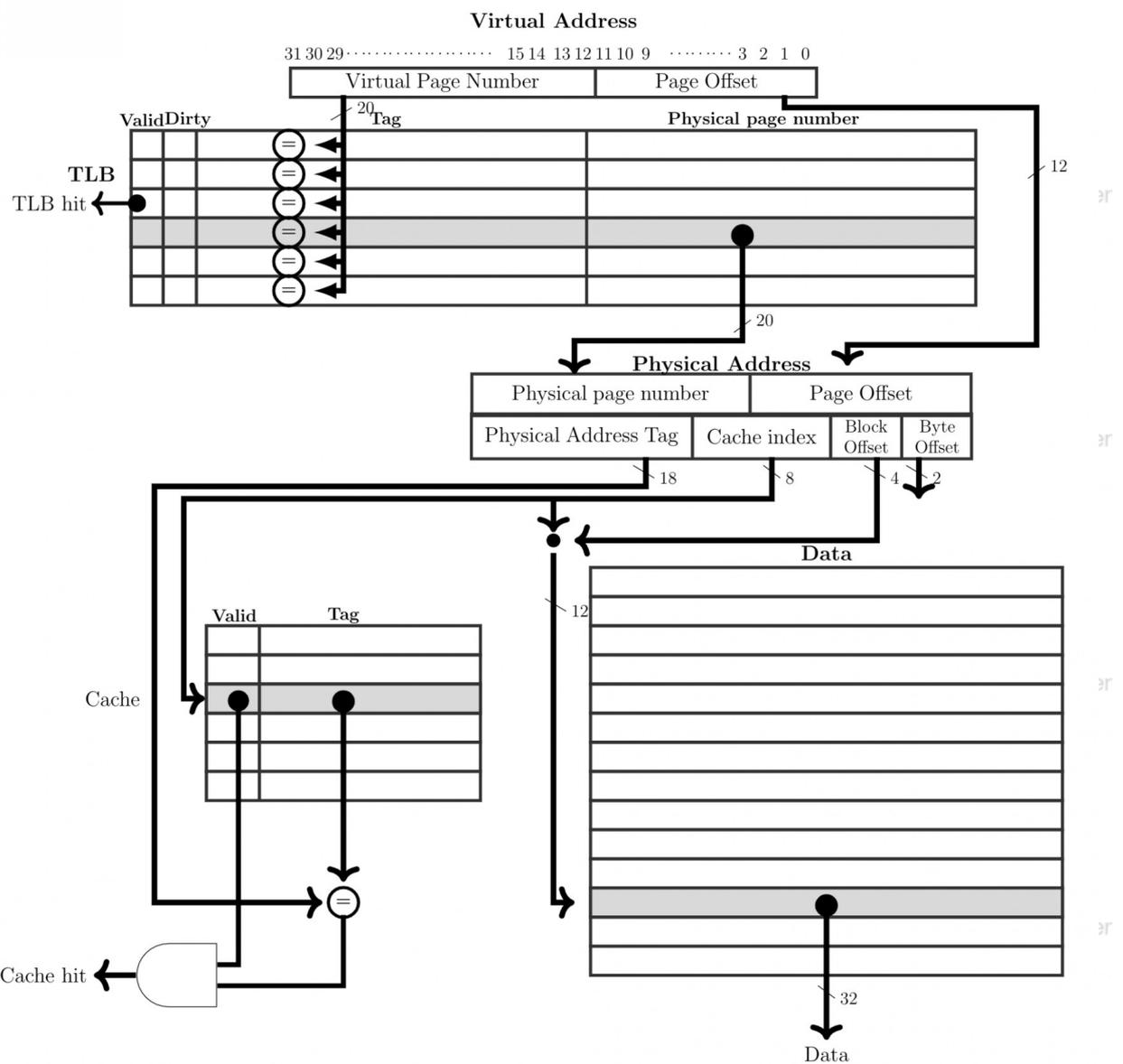
TLB maps a virtual address to the physical address of the page. (The lower bits of page address (page offset bits) are not used in TLB as they are the same for virtual as well as physical addresses). Here, for 8 kB page size we require 13 page offset bits.

In TLB we have 32 sets and so virtual address space is divided into 32 using 5 set bits. (Associativity doesn't affect the set bits as they just adds extra slots in each set).

So, number of tag bits = $40 - 5 - 13 = 22$

Following diagram shows how TLB and Cache works:

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63 votes

-- Vikrant Singh (11.2k points)



- ✓ 8 KB pages means 13 offset bits.
For 32 bit physical address, $32 - 13 = 19$ page frame bits must be there in each PTE (Page Table Entry).
We also have 1 valid bit, 1 dirty bit and 3 permission bits.
So, total size of a PTE (Page Table Entry) = $19 + 5 = 24$ bits = 3 bytes.

Given in question, maximum page table size = 24 MB

Page table size = No. of PTEs \times size of an entry

So, no. of PTEs = $24MB/3B = 8M$

Virtual address supported = No. of PTEs \times Page size (As we need a PTE for each page and assuming single-level paging)

= $8M \times 8KB$

= 64GB = 2^{36} Bytes

So, length of virtual address supported = 36 bits (assuming byte addressing)

👍 77 votes

classroom.gateover

-- Arjun Suresh (332k points)



- ✓ No. of pages (N) = 2^{26} = No. of entries in Page Table
Page Table Entry Size (E) = 6 bytes

So, Page Table Size = $n \times e = 2^{26} \times 6$ bytes = 384 MB

👍 45 votes

classroom.gateover

-- G VENKATESWARLU (461 points)



- ✓ Let P be the page fault rate.

Average memory access time = $(1 - \text{page fault rate}) \times \text{memory access time when no page fault} + \text{Page fault rate} \times \text{Memory access time when page fault}$.

$$X = (1 - P)M + PD$$

$$X = M + P(D - M)$$

$$P = (X - M)/(D - M)$$

(B) is the answer.

👍 47 votes

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-- Hemant Parihar (11.9k points)



- ✓ TLB Entry:

Page Number	Frame Number
-------------	--------------

Memory is word addressable.

- Word size = 4 Bytes
- Page size = 8 KB = 2^{11} words
- Virtual Memory size = 2^{64} words
- Number of pages possible = 2^{53}
- Number of bits required for Page number = 53 bits
- Number of bits required for Page offset = $64 - 53 = 11$ bits

At a time TLB contains $128 = 2^7$ distinct page numbers.

If a page number is found in TLB then there will be a hit for all the words (Word addresses) of that Page.

1 - page hit implies 2^{11} distinct virtual address hits.

So 2^7 page hit implies $2^7 \times 2^{11} = 2^8 \times 2^{10} = 256 \times 2^{10}$ virtual address hits

Option B. At most, 256×2^{10} distinct virtual addresses can be translated without any TLB miss.

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✓ Given,

1. Main Memory access time: 100 ns
2. TLB lookup time: 20 ns
3. Time to transfer one page to/from disk: 5000 ns
4. TLB hit ratio: 0.95
5. Page fault rate: 0.10
6. 20 % of page faults needs to be written back to disk

Hence, effective memory access time =

$$0.95(20 + 100) + 0.05\{0.90(20 + 100 + 100) + 0.10[0.80(20 + 100 + 5000 + 100) + 0.20(20 + 100 + 5000 + 5000 + 100)]\}$$

$$= 155.0 \text{ ns}$$

Explanation:

If there is a TLB hit, you just need to access the memory. If there is a miss 1 TLB lookup was wasted,

1. You need to lookup the page table for the entry and then access the required location, requiring 2 memory accesses - Assuming No Page fault occurs.
2. If there is a page fault, Then 1 memory access was wasted (you can only know that the page is not present in memory by checking the corresponding page entry in the page table). 80 % of the time, you'll only be fetching a page from secondary storage which takes 5000 ns, 20% of the time, you'll need to write a dirty page back to disk and bring the page (which caused the page fault) back to main memory, requiring 5000 + 5000 ns

- For all memory accesses in a system with virtual memory we need Virtual Address to Physical Address translation and this goes through TLB.
- On TLB hit, we get the physical address.
- On TLB miss, we have to do page table access which always resides in physical memory (no page fault possible here).
- In the question it is given 1– level page table is used. So, TLB miss will need one physical memory access to get the physical address.
- Question mentions page fault rate as 10% and this should default to 10 page faults every 100 memory accesses. (Since TLB miss rate is 5% and for normal program run a TLB hit and page fault cannot happen for a memory access (can happen for invalid memory accesses), it is also possible to consider page fault rate as 10% of all TLB misses. See the last part of the answer for this.)

In the question page transfer time is given. This is different from page fault service time which includes the page transfer time + the memory access time as once the page is filled, a new memory access is initiated.

So, Average Memory Access Time = Address Translation Time + Data Retrieval Time

$$= \text{TLB access time} + \text{TLB Miss ratio} \times \text{Page Table Access time} + \text{Main memory access time} + \text{Page fault rate} \times (\text{Page transfer time} + \text{Main memory access time})$$

$$= 20 + 0.05 \times 100 + 100 + 0.1 \times (5000 + 20 + 0.05 \times 100 + 100) + 0.1 \times 0.2 \times 5000$$

$$= 20 + 5 + 100 + 512.5 + 100$$

$$= 737.5 \text{ ns}$$

PS: If the question had given page fault service time also as 5000 answer will be
 $20 + 0.05 \times 100 + 0.9 \times 100 + 0.1 \times 5000 + 0.1 \times 0.2 \times 5000 = 25 + 90 + 500 + 100 = 715 \text{ ns}$

"Assume that the TLB hit ratio is 95%, page fault rate is 10%"

If this statement is changed to

"Assume that the TLB hit ratio is 95%, and **when TLB miss happens** page fault rate is 10%"

Average Memory Access Time = Address Translation Time + Data Retrieval Time

$$= \text{TLB access time} + \text{TLB Miss ratio} \times \text{Page Table Access time} + \text{Main memory access time} + \text{Page fault rate} \times (\text{Page transfer time} + \text{Main memory access time})$$

$$= 20 + 0.05 \times 100 + 100 + 0.05 \times 0.1 \times (5000 + 20 + 0.05 \times 100 + 100) + 0.05 \times 0.1 \times 0.2 \times 5000$$

$$= 20 + 5 + 100 + 25.625 + 5$$

$$= 155.625 \text{ ns}$$

If "memory access being restarted" is ignored for page fault, this will be

$$\begin{aligned}
&= 20 + 0.05 \times 100 + 100 + 0.05 \times 0.1 \times (5000) + 0.05 \times 0.1 \times 0.2 \times 5000 \\
&= 20 + 5 + 100 + 25 + 5 \\
&= 155 \text{ ns}
\end{aligned}$$

Ideally the answer key should be 715 – 738 due to the confusion in the meaning of page transfer time as most standard resources use page fault service time instead.

If we assume page fault rate is given "only when TLB miss happens" answer should be 155 – 155.7

A previous year question where page fault rate "per instruction" is clearly mentioned in question: <https://gateoverflow.in/318/gate2004-47>. This GATE2020 question is VERY POORLY framed and must be challenged.

Another similar question where TLB miss is taken as per memory access is given below (See the equation used in 3-e)

https://gateoverflow.in/?qa=blob&qa_blobid=5047954265438465988

References



21 votes

-- Arjun Suresh (332k points)

5.22.37 Virtual Memory: GATE IT 2004 | Question: 66 top

<https://gateoverflow.in/3709>



✓ Answer is (D).

Page table entry must contain bits for representing frames and other bits for storing information like dirty bit, reference bit etc

$$\text{No. of frames (no. of possible pages)} = \text{Physical memory size} / \text{Page size} = 2^{30} / 2^{12} = 2^{18}$$

$$18 + x = 32 \quad (\text{PT entry size} = 32 \text{ bit})$$

$$x = 14 \text{ bits}$$

37 votes

-- neha pawar (3.3k points)

5.22.38 Virtual Memory: GATE IT 2008 | Question: 16 top

<https://gateoverflow.in/3276>



✓ Effective access time = hit ratio × time during hit + miss ratio × time during miss

In both cases TLB is accessed and assuming page table is accessed from memory only when TLB misses.

$$= 0.9 \times (10 + 50) + 0.1 \times (10 + 50 + 50)$$

$$= 54 + 11 = 65$$

Correct Answer: C

41 votes

-- Arjun Suresh (332k points)

5.22.39 Virtual Memory: GATE IT 2008 | Question: 56 top

<https://gateoverflow.in/3366>



✓ Option (D).

Dirty bit : The **dirty bit** is set when the processor writes to (modifies) this memory. The **bit** indicates that its associated block of memory has been modified and has not been saved to storage yet. **Dirty bits** are used by the CPU cache and in the page replacement algorithms of an operating system.

R/W bit : If the bit is set, the page is read/write. Otherwise when it is not set, the page is read-only.

Reference bit is used in a version of FIFO called second chance (SC) policy, in order to avoid replacement of heavily used page.. It is set to one when a page is used heavily and periodically set to 0. Since it is used in a version FIFO which is a page replacement policy, this bit is come under category of page replacement.

Valid bit is not used for page replacement. It is not used in any page replacement policy. It tells the page in the memory is valid or not. If it is valid it is directly used and if it is not then a fresh page is loaded. So, basically it is page initialization, because we are not replacing, it is initializing, we not knocking out somebody, we are filling empty space, so initialization, so option (D).

👍 63 votes

-- Vicky Bajoria (4.1k points)

Answer Keys

5.1.1	C	5.1.2	B	5.1.3	C	5.2.1	2	5.2.2	A
5.2.3	A;B;C	5.2.4	A	5.3.1	N/A	5.3.2	N/A	5.3.3	N/A
5.3.4	B	5.3.5	D	5.3.6	B	5.3.7	3	5.3.8	10
5.3.9	346	5.3.10	B	5.3.11	C	5.3.12	B	5.3.13	C
5.4.1	N/A	5.4.2	N/A	5.4.3	B	5.4.4	N/A	5.4.5	N/A
5.4.6	9.006	5.4.7	D	5.4.8	N/A	5.4.9	N/A	5.4.10	D
5.4.11	D	5.4.12	A	5.4.13	800	5.4.14	A	5.4.15	C
5.4.16	B	5.4.17	A	5.4.18	B	5.4.19	C	5.4.20	C
5.4.21	B	5.4.22	B	5.4.23	D	5.4.24	99.55 : 99.65	5.4.25	14020
5.4.26	6.1 : 6.2	5.4.27	85	5.4.28	C	5.4.29	D	5.4.30	B
5.4.31	D	5.5.1	C	5.5.2	D	5.5.3	D	5.5.4	4.0 : 4.1
5.5.5	A;C	5.5.6	B	5.6.1	C	5.6.2	B	5.6.3	C
5.6.4	31	5.6.5	C	5.7.1	B	5.8.1	90.00	5.8.2	C
5.8.3	D	5.8.4	A	5.8.5	C	5.8.6	C	5.8.7	D
5.8.8	A	5.9.1	A	5.9.2	B	5.9.3	C	5.9.4	A
5.9.5	B	5.9.6	C	5.10.1	3.2	5.10.2	N/A	5.10.3	B
5.10.4	B	5.10.5	10000	5.10.6	A	5.10.7	C	5.10.8	C
5.10.9	B	5.11.1	A	5.11.2	D	5.11.3	B	5.12.1	N/A
5.12.2	B	5.12.3	B	5.12.4	C	5.12.5	C	5.12.6	A
5.12.7	B	5.12.8	C	5.12.9	C	5.12.10	B	5.12.11	A
5.12.12	C	5.12.13	B	5.12.14	A	5.12.15	C	5.12.16	A
5.12.17	A	5.12.18	B	5.12.19	7	5.12.20	D	5.12.21	6
5.12.22	A	5.12.23	1	5.12.24	D	5.12.25	B	5.12.26	A;C
5.12.27	4108 : 4108	5.12.28	C	5.12.29	A	5.12.30	B	5.13.1	N/A
5.13.2	N/A	5.13.3	N/A	5.14.1	B	5.14.2	C	5.14.3	B
5.14.4	B	5.15.1	N/A	5.15.2	N/A	5.15.3	N/A	5.15.4	C
5.15.5	B	5.15.6	A	5.15.7	D	5.15.8	A	5.15.9	N/A
5.15.10	19	5.15.11	B	5.15.12	D	5.15.13	A	5.15.14	B
5.15.15	A	5.15.16	B	5.15.17	A	5.15.18	B	5.15.19	C
5.15.20	D	5.15.21	A	5.15.22	C	5.15.23	B	5.15.24	7.2
5.15.25	1000	5.15.26	5.5	5.15.27	12	5.15.28	D	5.15.29	C

5.15.30	A	5.15.31	8.25	5.15.32	3	5.15.33	29	5.15.34	2
5.15.35	C	5.15.36	5.25:5.26	5.15.37	12 : 12	5.15.38	A;C;D	5.15.39	D
5.15.40	D	5.15.41	B	5.15.42	D	5.15.43	C	5.16.1	D
5.16.2	N/A	5.16.3	N/A	5.16.4	N/A	5.16.5	N/A	5.16.6	N/A
5.16.7	N/A	5.16.8	N/A	5.16.9	N/A	5.16.10	C	5.16.11	C
5.16.12	N/A	5.16.13	D	5.16.14	N/A	5.16.15	B	5.16.16	N/A
5.16.17	N/A	5.16.18	B	5.16.19	N/A	5.16.20	B	5.16.21	N/A
5.16.22	N/A	5.16.23	N/A	5.16.24	B	5.16.25	C	5.16.26	D
5.16.27	A	5.16.28	B	5.16.29	B	5.16.30	D	5.16.31	A
5.16.32	A	5.16.33	A	5.16.34	B	5.16.35	D	5.16.36	C
5.16.37	C	5.16.38	3	5.16.39	A	5.16.40	C	5.16.41	D
5.16.42	C	5.16.43	80	5.16.44	A	5.16.45	D	5.16.46	A
5.16.47	B	5.16.48	A	5.16.49	C	5.16.50	C	5.16.51	D
5.17.1	N/A	5.17.2	N/A	5.17.3	A	5.17.4	D;E	5.17.5	N/A
5.17.6	N/A	5.17.7	C	5.17.8	N/A	5.17.9	B	5.17.10	C
5.17.11	N/A	5.17.12	C	5.17.13	B	5.17.14	C	5.17.15	A
5.17.16	A	5.17.17	B	5.17.18	B	5.17.19	B	5.17.20	7
5.17.21	D	5.17.22	D	5.17.23	A	5.17.24	B	5.17.25	C
5.17.26	B	5.18.1	N/A	5.18.2	D	5.18.3	B	5.19.1	N/A
5.19.2	B	5.19.3	B	5.19.4	C	5.19.5	7	5.19.6	A
5.19.7	A;B;D	5.19.8	D	5.20.1	A;C	5.21.1	A	5.21.2	D
5.21.3	C	5.21.4	D	5.21.5	D	5.21.6	B	5.21.7	A;D
5.21.8	A	5.22.1	N/A	5.22.2	N/A	5.22.3	99.99	5.22.4	B;C;E
5.22.5	A	5.22.6	A	5.22.7	C	5.22.8	N/A	5.22.9	A
5.22.10	N/A	5.22.11	A;C	5.22.12	B;D	5.22.13	D	5.22.14	B
5.22.15	D	5.22.16	C	5.22.17	N/A	5.22.18	C	5.22.19	D
5.22.20	C	5.22.21	C	5.22.22	C	5.22.23	D	5.22.24	B
5.22.25	B	5.22.26	B	5.22.27	C	5.22.28	C	5.22.29	122
5.22.30	4	5.22.31	22	5.22.32	36	5.22.33	384	5.22.34	B
5.22.35	B	5.22.36	155:156	5.22.37	D	5.22.38	C	5.22.39	D

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