



<http://www.montblanc-project.eu>

# The next generation supercomputer

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**Disclaimer:** Not only I speak for myself ... All references to unavailable products are speculative, taken from web sources. There is no commitment from ARM, Samsung, TI, Nvidia, Bull, or others, implied.

# Project goals

- To develop an **European** Exascale approach
- Based on embedded **power-efficient technology**



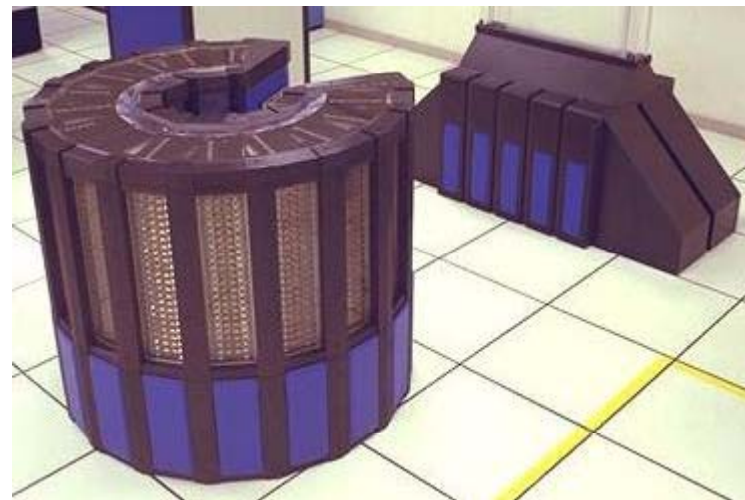
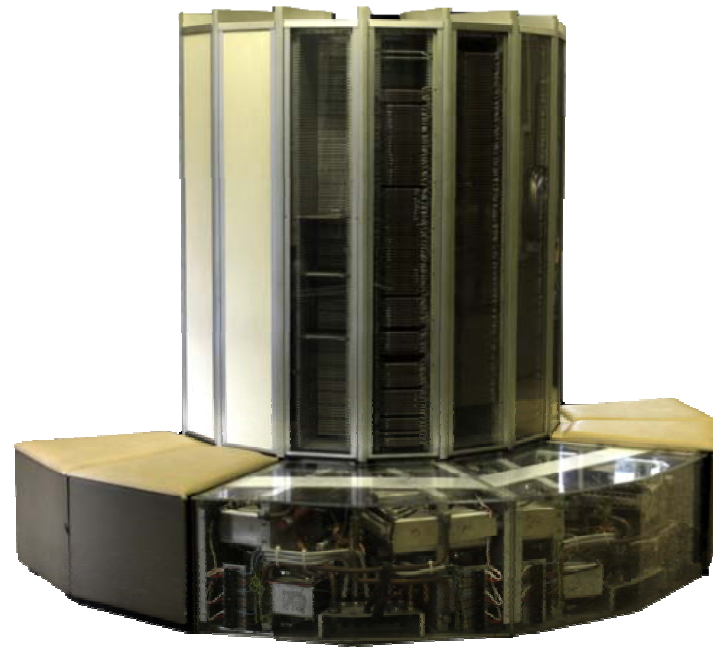
- Objectives
  - Develop a first prototype system, limited by available technology
  - Design a Next Generation system, to overcome the limitations
  - Develop a set of Exascale applications targeting the new system

# Outline

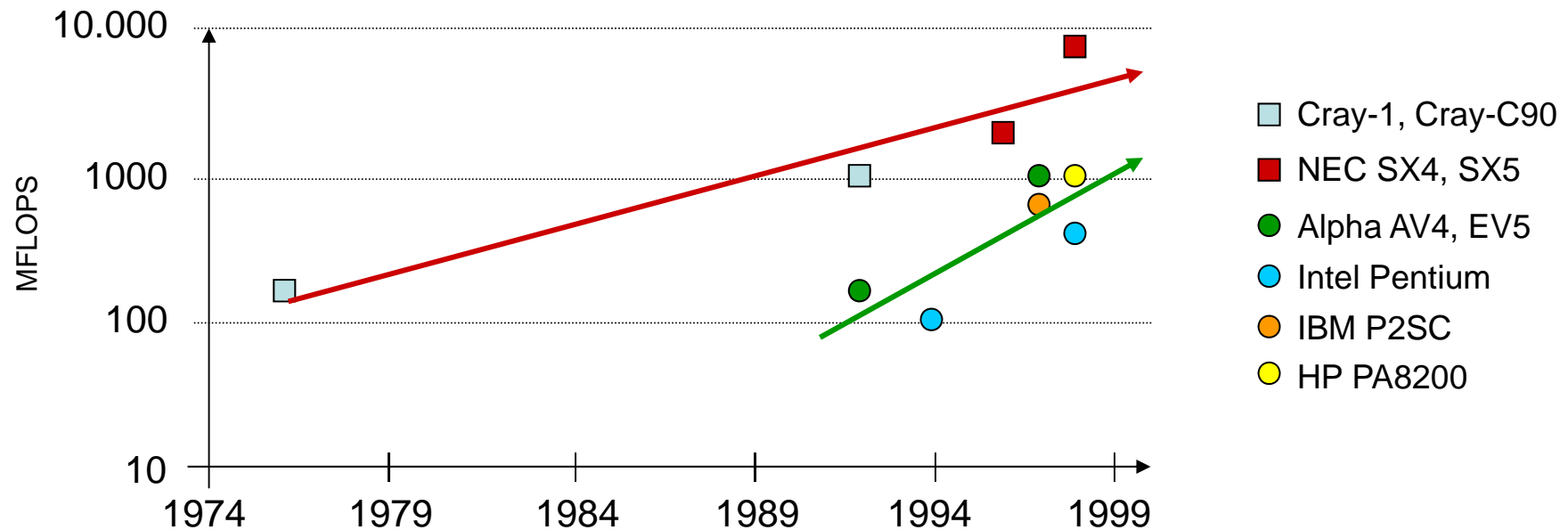
- A bit of history
  - Vector supercomputers
  - Commodity supercomputers
  - The next step in the commodity chain
- Supercomputers from mobile components
  - Killer mobile examples
  - Mont-Blanc architecture strawman
  - Rely on OmpSs to handle the challenges
- BSC prototype roadmap
- Mont-Blanc project goals and milestones

# In the beginning ... there were only supercomputers

- Built to order
  - Very few of them
- Special purpose hardware
  - Very expensive
- Control Data, Convex, ...
- Cray-1
  - 1975, 160 MFLOPS
    - 80 units, 5-8 M\$
- Cray X-MP
  - 1982, 800 MFLOPS
- Cray-2
  - 1985, 1.9 GFLOPS
- Cray Y-MP
  - 1988, 2.6 GFLOPS
- Fortran+vectorizing compilers



# The Killer Microprocessors

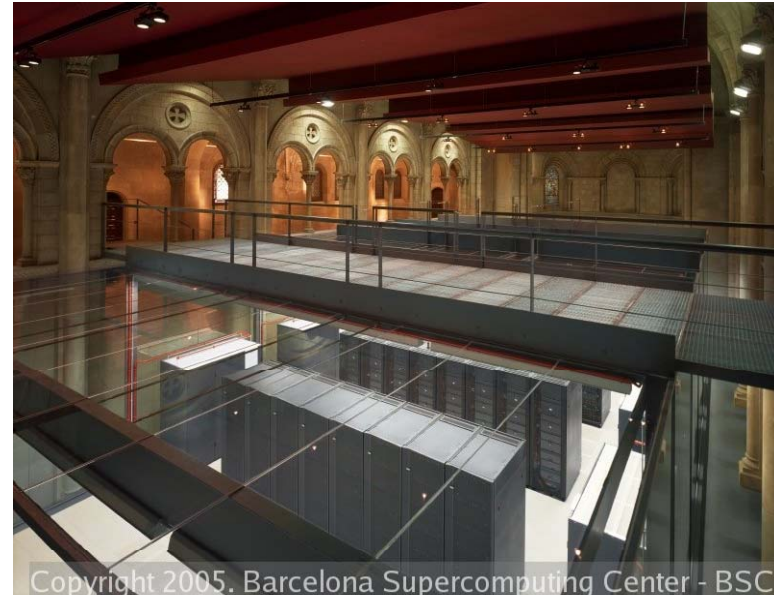


- Microprocessors killed the Vector supercomputers
  - They were not faster ...
  - ... but they were significantly cheaper and greener
- Need 10 microprocessors to achieve the performance of 1 Vector CPU
  - SIMD vs. MIMD programming paradigms

# Then, commodity took over special purpose



- ASCI Red, Sandia
  - 1997, 1 TFLOPS (Linpack),
  - 9298 cores @ 200 Mhz
  - 1.2 Tbytes
  - Intel Pentium Pro
    - Upgraded to Pentium II Xeon, 1999, 3.1 Tflops

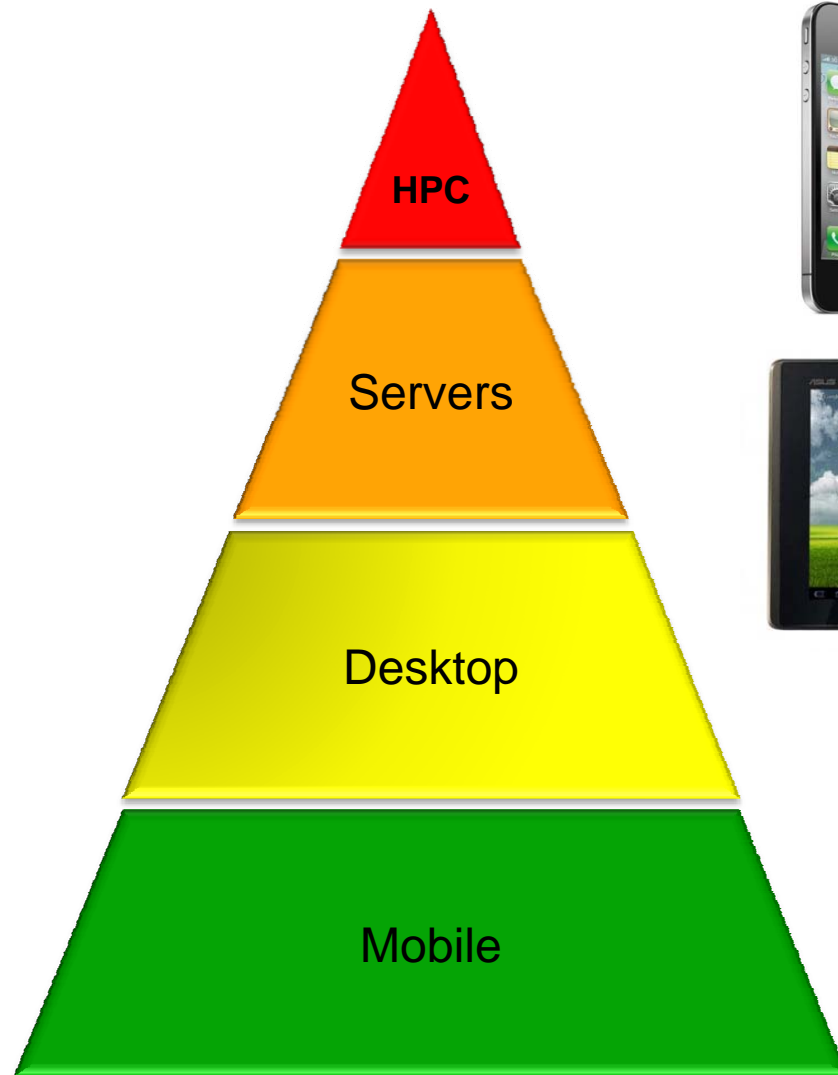


- MareNostrum, BSC
  - 2004, 20 TFLOPS
  - IBM PowerPC 970 FX
    - Blade enclosure
  - Myrinet + 1 GbE network
  - SuSe Linux

Message-Passing Programming Models

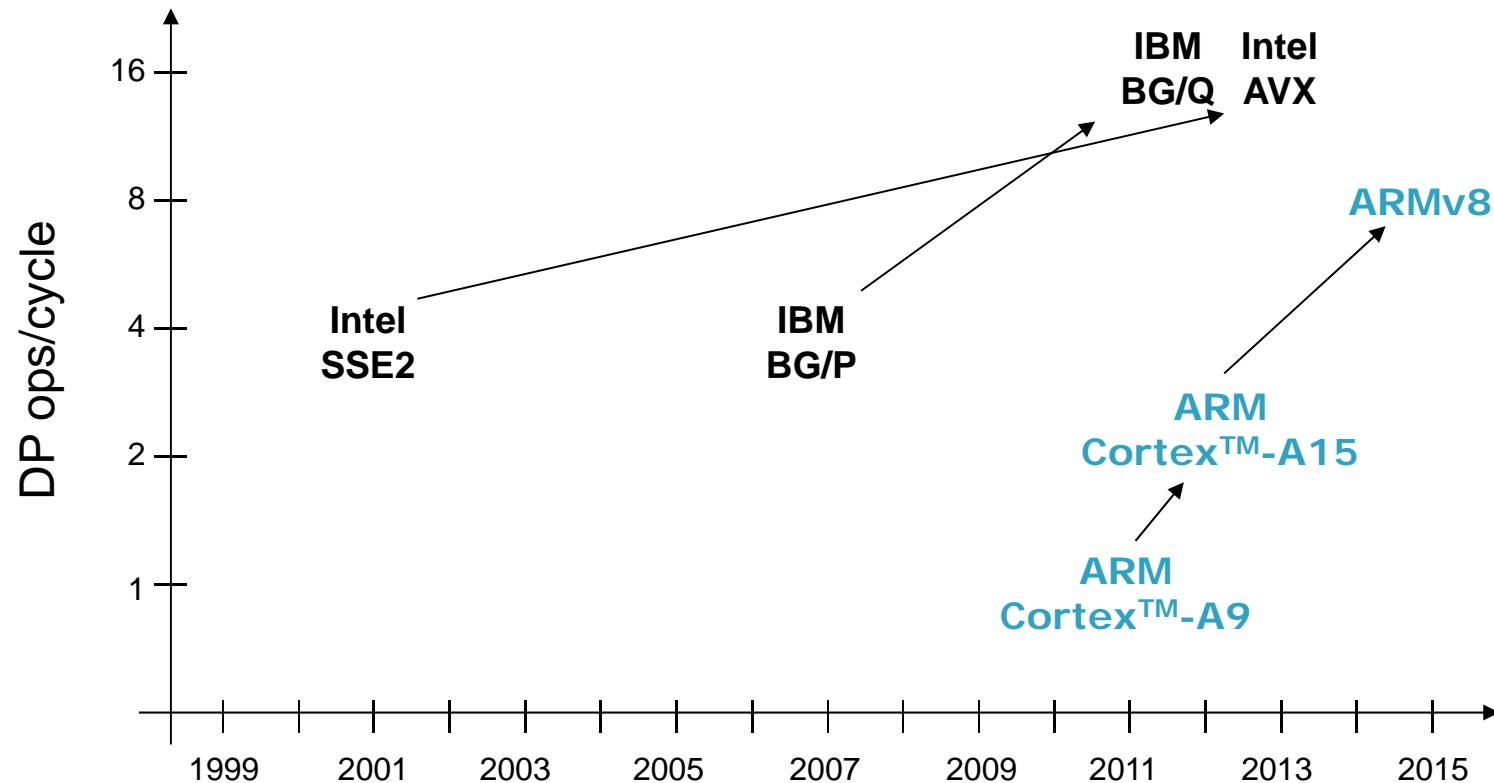


# The next step in the commodity chain



- Total cores in Jun'12 Top500
  - 13.5 Mcores
- Tablets sold in Q4 2011
  - 27 Mtablets
- Smartphones sold Q4 2011
  - > 100 Mphones

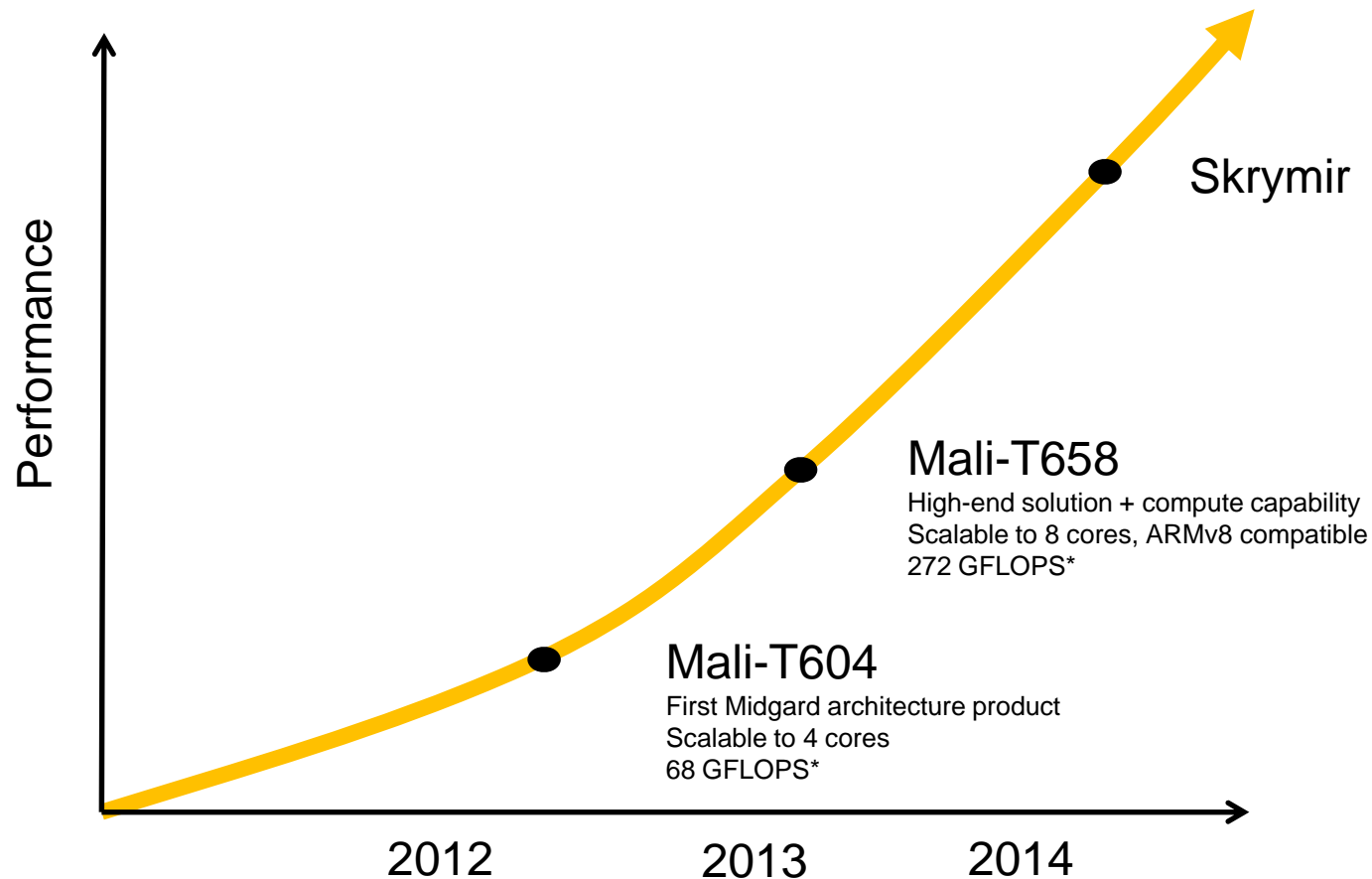
# ARM Processor improvements in DP FLOPS



- IBM BG/Q and Intel AVX implement DP in 256-bit SIMD
  - 8 DP ops / cycle
- ARM quickly moved from optional floating-point to state-of-the-art
  - ARMv8 ISA introduces DP in the NEON instruction set (128-bit SIMD)



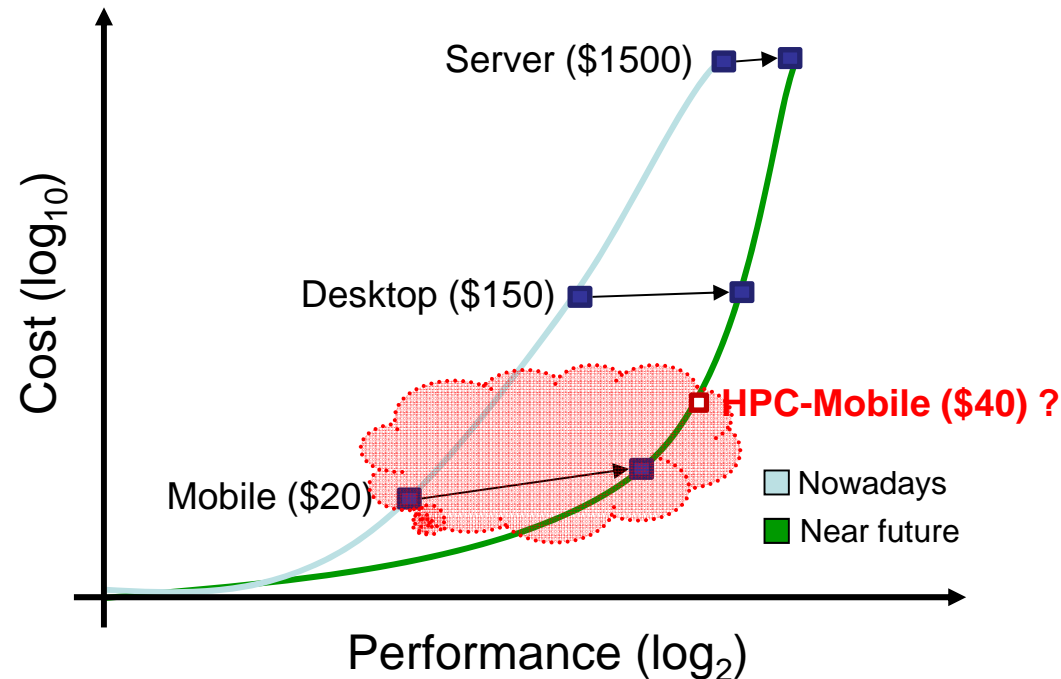
# Integrated ARM GPU performance



- GPU compute performance increases faster than Moore's Law

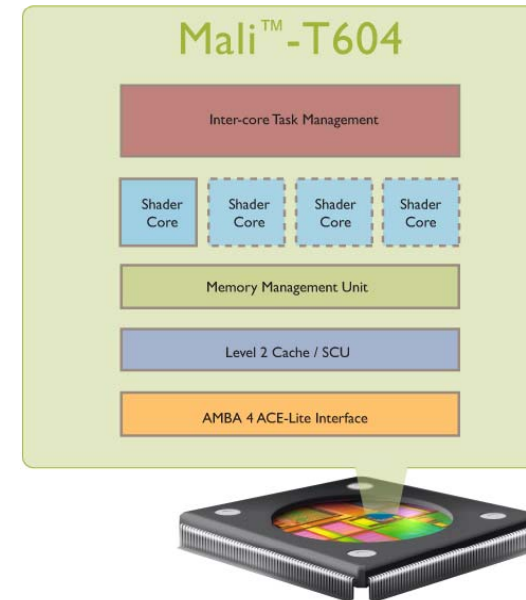
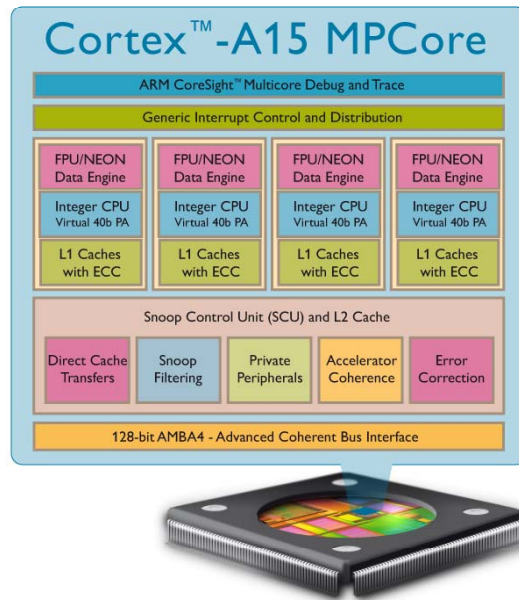
\* Data from web sources, not an ARM commitment

# Are the “Killer Mobiles™” coming?

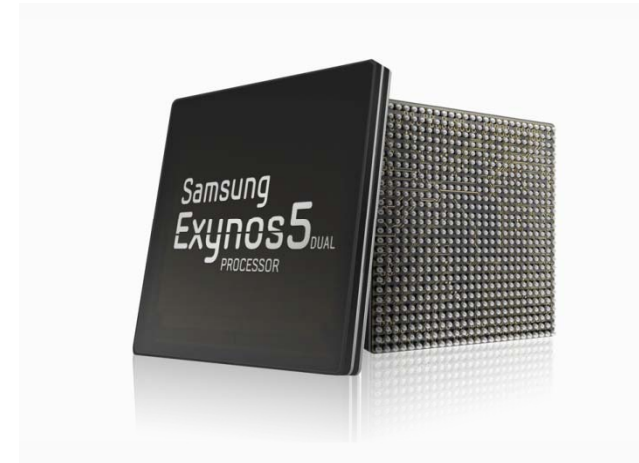


- Where is the sweet spot? Maybe in the low-end ...
  - Today ~ 1:8 ratio in performance, 1:100 ratio in cost
  - Tomorrow ~ 1:2 ratio in performance, still 1:100 in cost ?
- The same reason why microprocessors killed supercomputers
  - Not so much performance ... but much lower cost, and power

# Samsung Exynos 5 Dual Superphone SoC

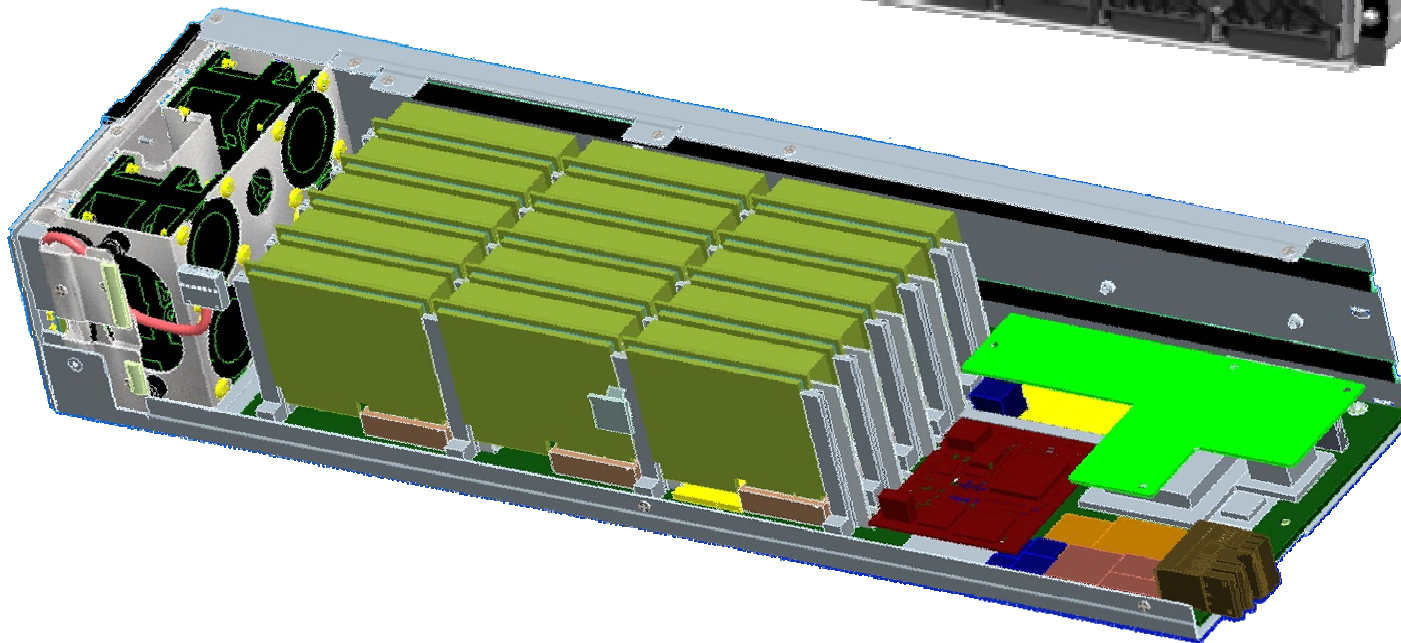


- 32nm HKMG
- Dual-core ARM Cortex-A15 @ 1.7 GHz
- Quad-core ARM Mali T604
  - OpenCL 1.1
- Dual-channel DDR3
- USB 3.0 to 1 GbE bridge
- **All in a low-power mobile socket**

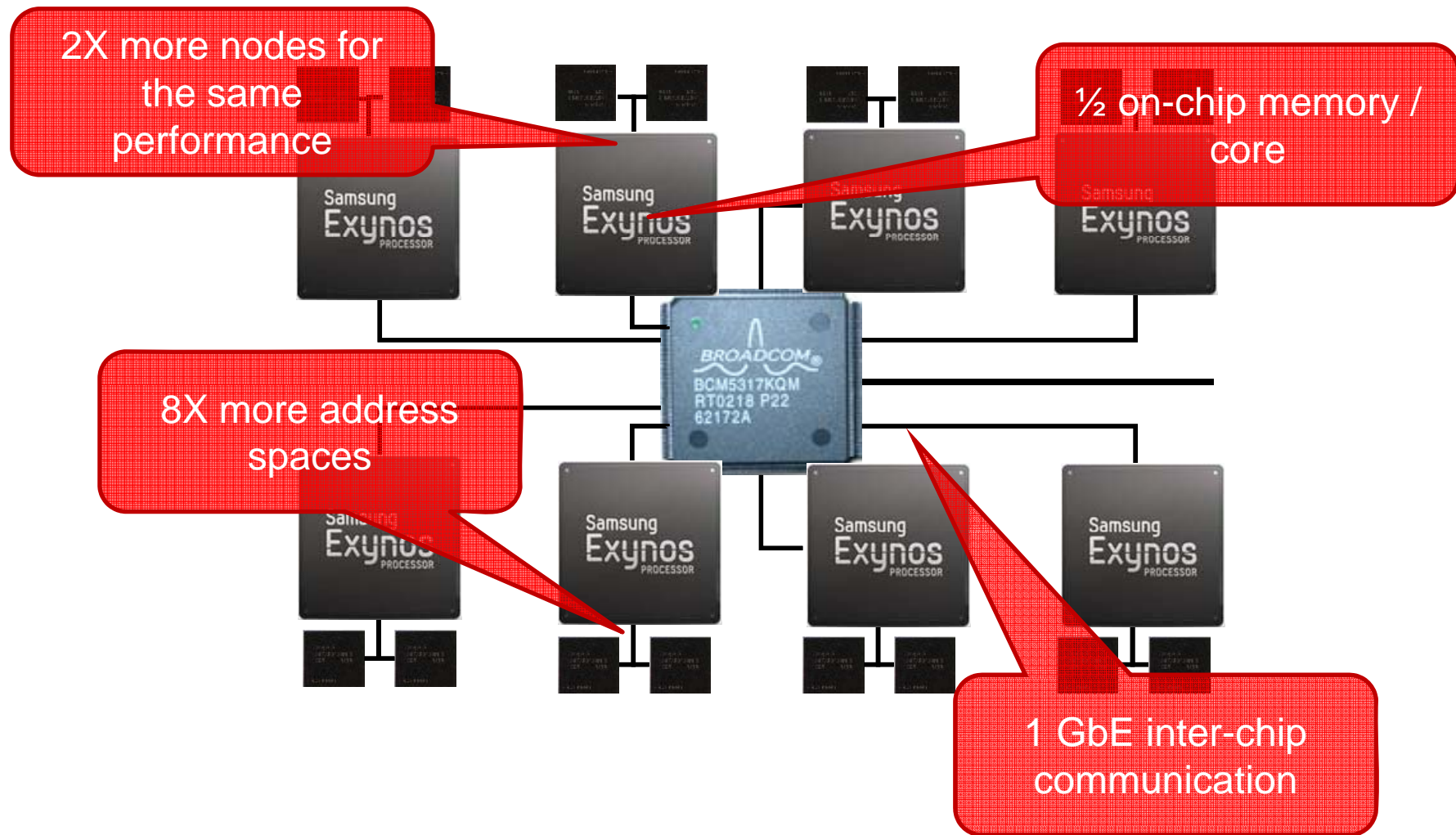


# High density packaging architecture

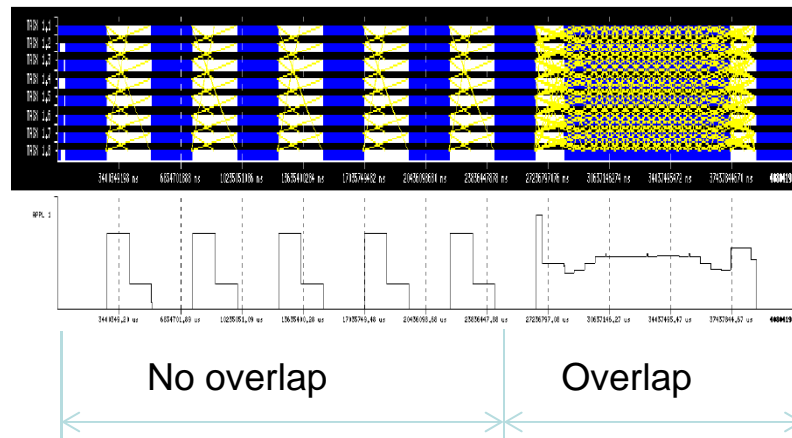
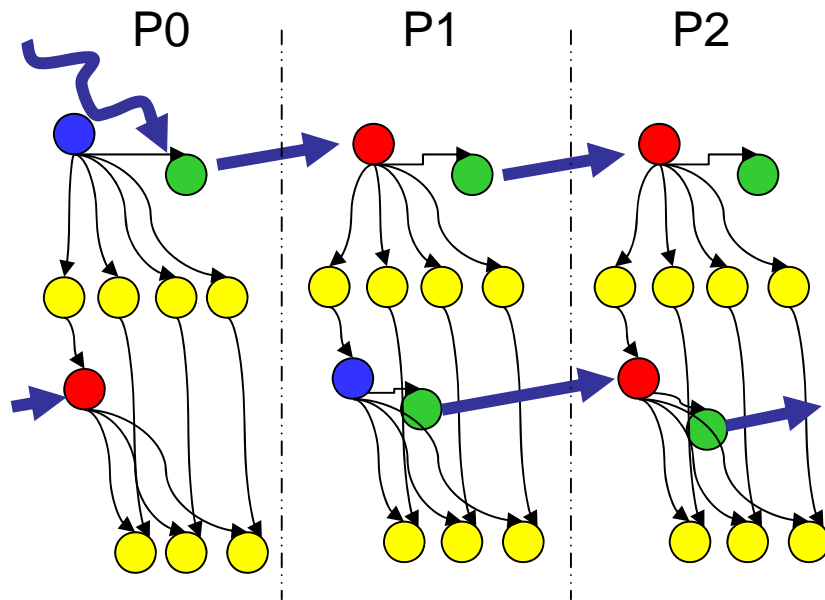
- Standard BullX blade enclosure
- Multiple compute nodes per blade
  - Additional level of interconnect, on-blade network



# There is no free lunch

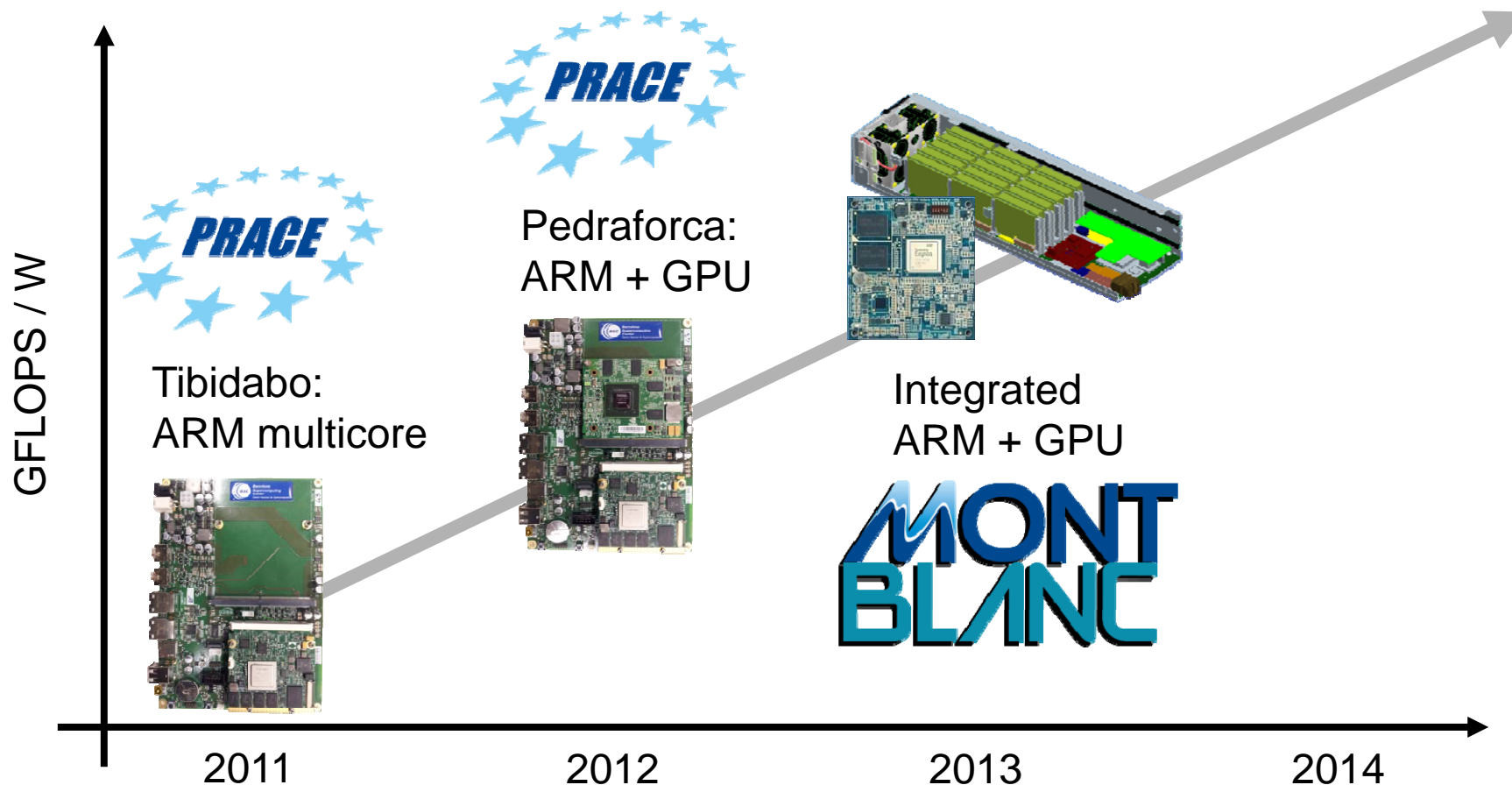


# OmpSs runtime layer manages architecture complexity



- Programmer exposed a simple architecture
- Task graph provides lookahead
  - Exploit knowledge about the future
- Automatically handle all of the architecture challenges
  - Strong scalability
  - Multiple address spaces
  - Low cache size
  - Low interconnect bandwidth
- Enjoy the positive aspects
  - Energy efficiency
  - Low cost

# BSC ARM-based prototype roadmap

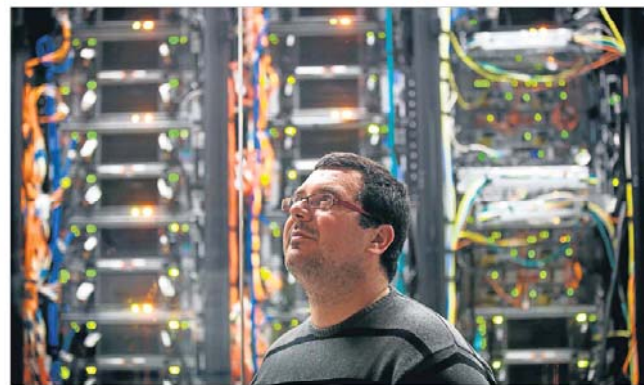


- Prototypes are critical to accelerate software development
  - System software stack + applications



# Very high expectations ...

- High media impact of ARM-based HPC
- Scientific, HPC, general press quote Mont-Blanc objectives
  - Highlighted by Eric Schmidt, Google Executive Chairman, at the EC's Innovation Convention



Científicos líderes. Alex Ramírez, jefe de equipo del Barcelona Supercomputing Center, en la UPC. Detrás de él, la joya de la entidad, el Mare Nostrum

## El supercibercerebro

• Barcelona construye el primer megaordenador del mundo basado en teléfonos móviles

OSCAR MUÑOZ

En un pequeño cuarto de uno de los edificios consagrados a la investigación del Campus Nord de la Universitat Politècnica de Catalunya (UPC) toma forma lo que para muchos es una seria amenaza a la supremacía tecnológica estadounidense y símbolo en el campo de los ordenadores gigantes. Allí, un equipo de científicos construye el que será el primer superordenador del mundo basado en los teléfonos móviles. La idea es aprovechar la eficiencia en el consumo energético de los

smartphones y de las tabletas que la mayor parte del tiempo no están enchufados a la red eléctrica y funcionan sin subvencionarse para aumentar la capacidad de cálculo sin disparar el gasto energético. Todo un reto que debe dar respuesta a las necesidades crecientes de las empresas e instituciones, que piden o

platanos, programas, simulación cada vez más complicados. Este es el objetivo del gran Mont-Blanc, liderado por el

lento y que da cuenta de la prisa que la capital catalana

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## WIRED ENTERPRISE

IT HAPPENS

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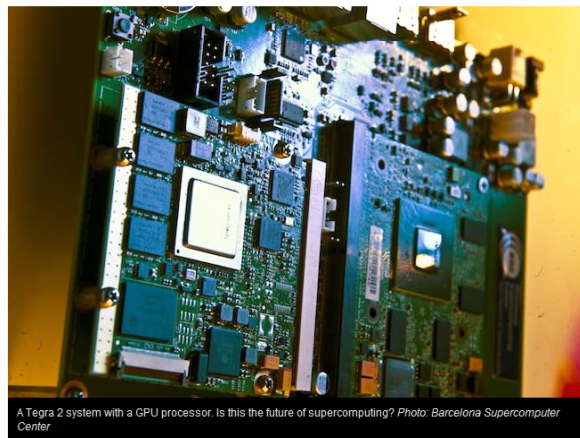
### Barcelona Supercomputer ARMED For Assault on World's Fastest Machines

By Robert McMillan April 3, 2012 | 6:30 am | Categories: Hardware, Microprocessors, Servers

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A Tegra 2 system with a GPU processor. Is this the future of supercomputing? Photo: Barcelona Supercomputer Center



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Technology News and Insights

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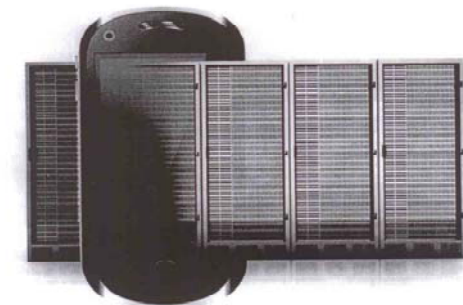
By Don Clark

Supercomputers, once built from handcrafted circuitry, were transformed when companies started assembling them from inexpensive PC-style microprocessors. Researchers in Barcelona are placing an early bet that the next big leap will be cellphone chips.

The [Barcelona Supercomputing Center](#) said Monday it is developing what it believes is the first supercomputer based on the ARM Holdings chip designs used in Nvidia called Tegra as well as Nvidia graphics processing units, or GPUs—the kind of chips used in videogame systems, which are also shaking up the supercomputer market.



Behind the experiment is a power struggle—that is, a struggle to control the power consumption of supercomputers, which take up huge data centers and draw the



## From mobile phone to supercomputer?

Tom Wilkie looks at the emerging strategies for Exascale computing

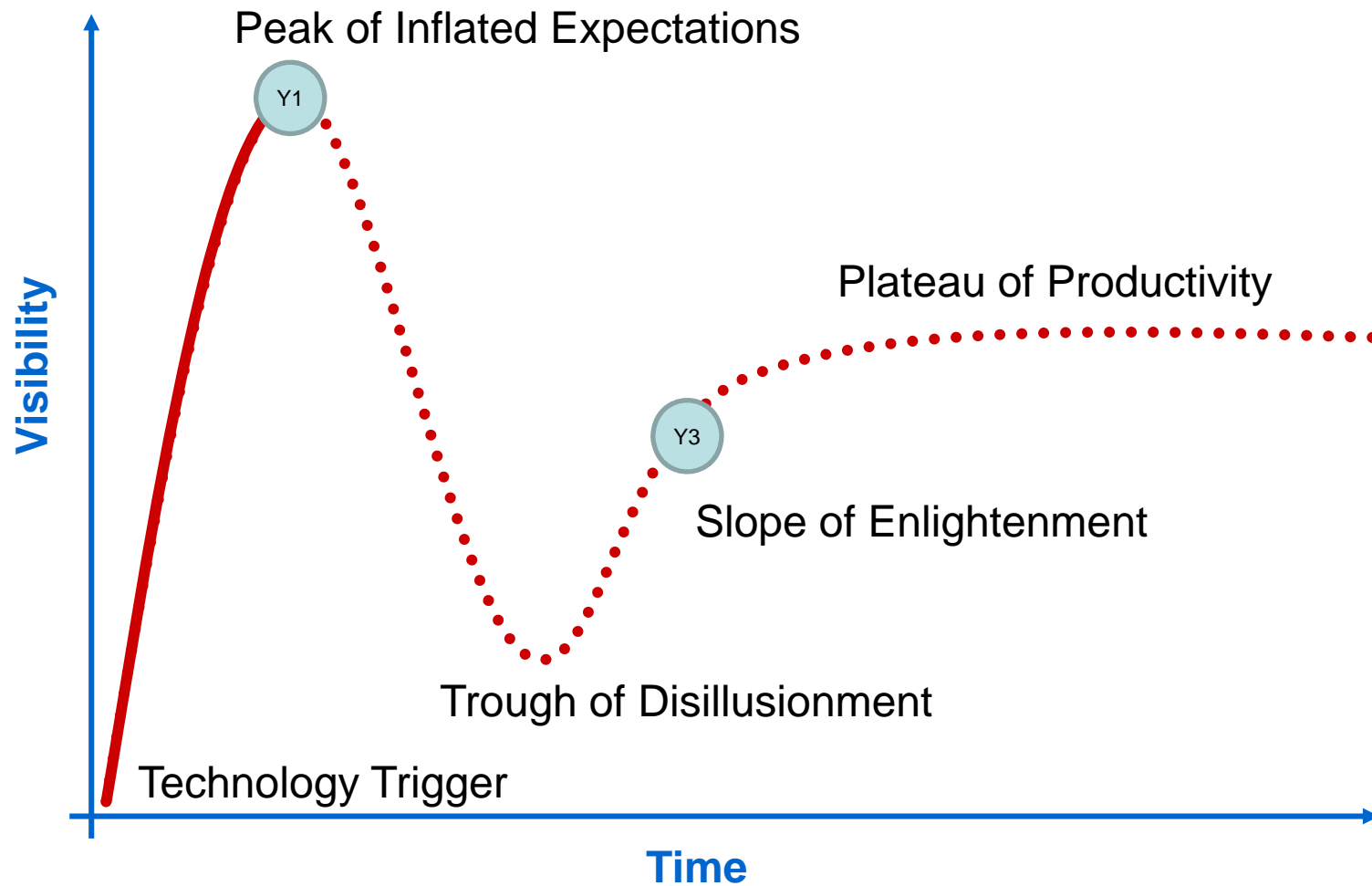
■ In early February, just after this issue of

machines consume somewhere around 1MW to 10MW of power annually, costing between \$1M and \$10M at current US prices. Exascale machines will run a thousand times faster, so one can afford simply to scale up existing technology for no-one could face annual electricity bills of more than \$5 billion.

are currently used in mobile phones and embedded applications because these guys have been facing power density limitations from the beginning—they work with battery-operated devices where energy consumption was always an issue. But Ramsey does not believe that it will

# MONT-BLANC

# The hype curve



- We'll see how deep it gets on the way down ...

# Conclusions

- Mont-Blanc architecture is shaping up
  - ARM multicore + integrated OpenCL accelerator
  - Ethernet NIC
  - High density packaging
- OmpSs programming model port to OpenCL
- Applications being ported to tasking model
- Stay tuned!



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