http://www.montblanc-project.eu

The next generation supercomputer

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Disclaimer: Not only I speak for myself ... All references to unavailable products are speculative, taken from web sources. There is no commitment from ARM, Samsung, TI, Nvidia, Bull, or others, implied.

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Project goals

- To develop an **European** Exascale approach
- Based on embedded **power-efficient technology**

- Objetives
  - Develop a first prototype system, limited by available technology
  - Design a Next Generation system, to overcome the limitations
  - Develop a set of Exascale applications targeting the new system

Outline

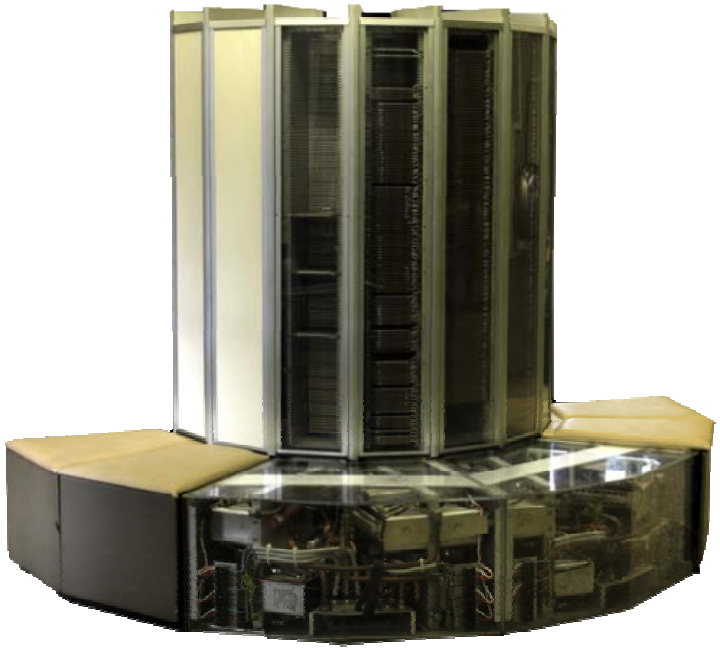
- A bit of history
  - Vector supercomputers
  - Commodity supercomputers
  - The next step in the commodity chain
- Supercomputers from mobile components
  - Killer mobile examples
  - Mont-Blanc architecture strawman
  - Rely on OmpSs to handle the challenges
- BSC prototype roadmap
- Mont-Blanc project goals and milestones

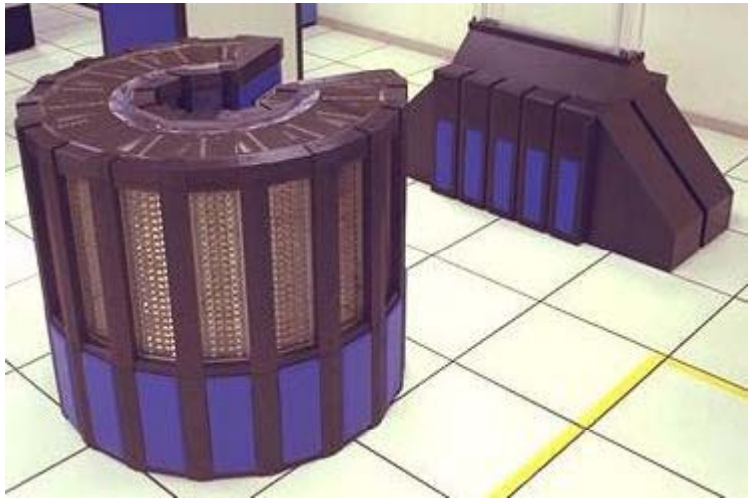
In the beginning ... there were only supercomputers

- Built to order
  - Very few of them
- Special purpose hardware
  - Very expensive

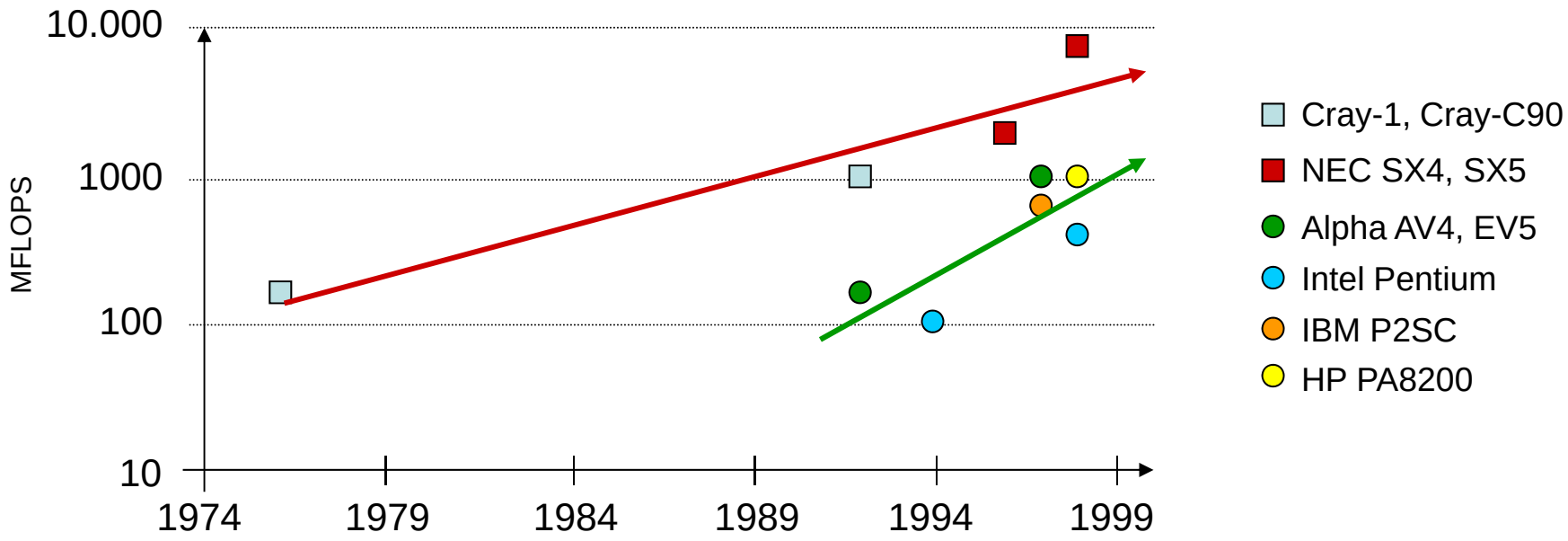
- Control Data, Convex, ...
- Cray-1
  - 1975, 160 MFLOPS
    - 80 units, 5-8 M$
- Cray X-MP
  - 1982, 800 MFLOPS
- Cray-2
  - 1985, 1.9 GFLOPS
- Cray Y-MP
  - 1988, 2.6 GFLOPS

- Fortran+vectorizing compilers



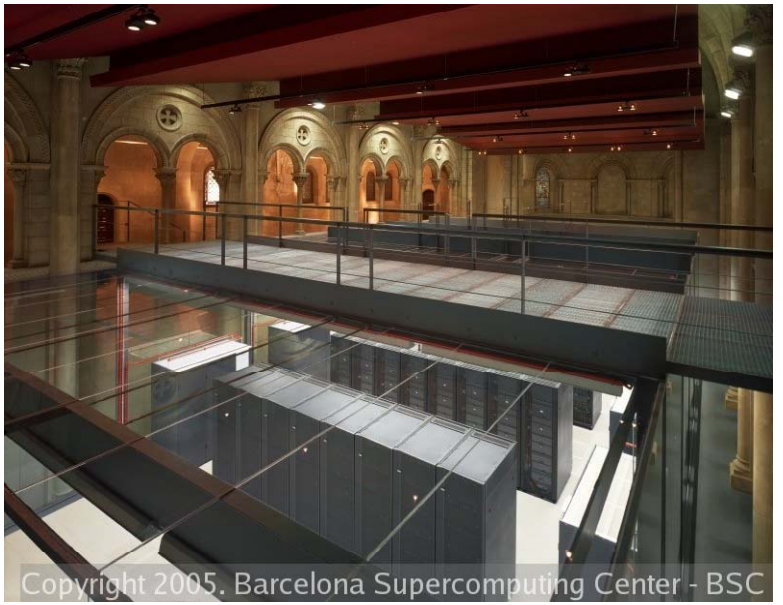


The Killer Microprocessors



- Microprocessors killed the Vector supercomputers
  - They were not faster ...
  - ... but they were significantly cheaper and greener
- Need 10 microprocessors to achieve the performance of 1 Vector CPU
  - SIMD vs. MIMD programming paradigms

Then, commodity took over special purpose

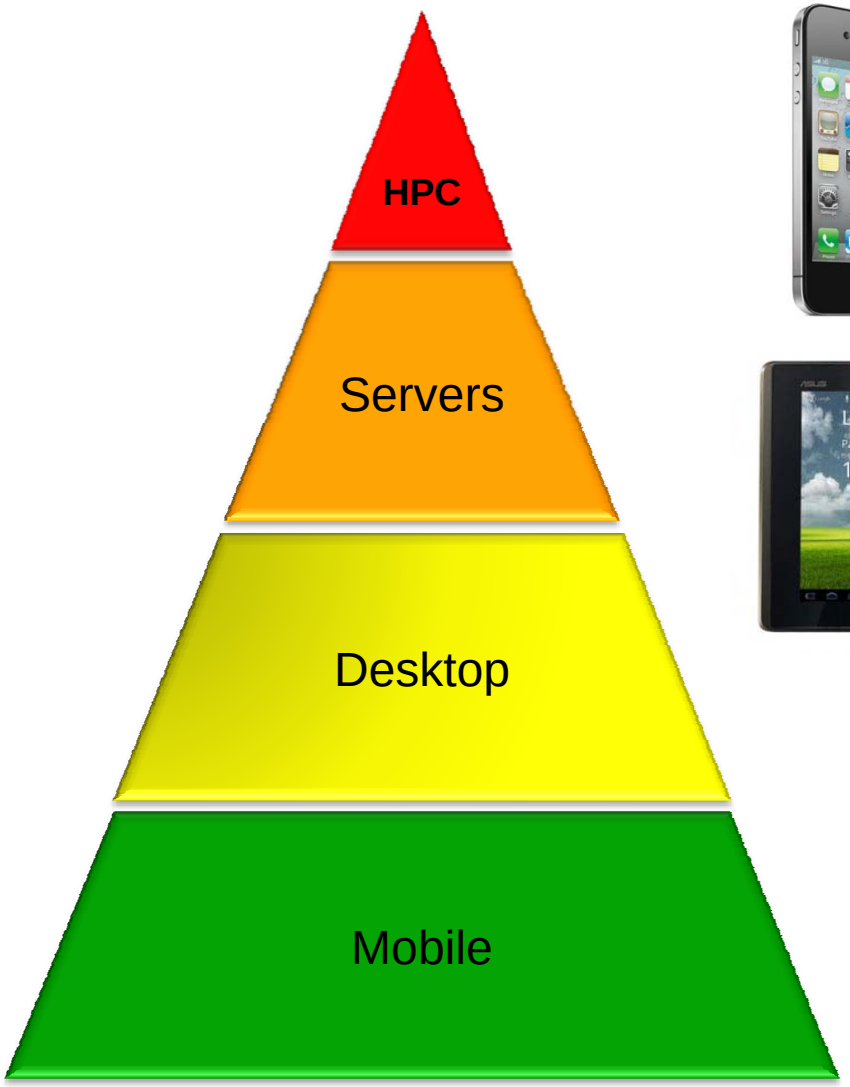


- ASCI Red, Sandia
  - 1997, 1 TFLOPS (Linpack),
  - 9298 cores @ 200 Mhz
  - 1.2 Tbytes
  - Intel Pentium Pro
    - Upgraded to Pentium II Xeon, 1999, 3.1 Tflops

- MareNostrum, BSC
  - 2004, 20 TFLOPS
  - IBM PowerPC 970 FX
    - Blade enclosure
  - Myrinet + 1 GbE network
  - SuSe Linux

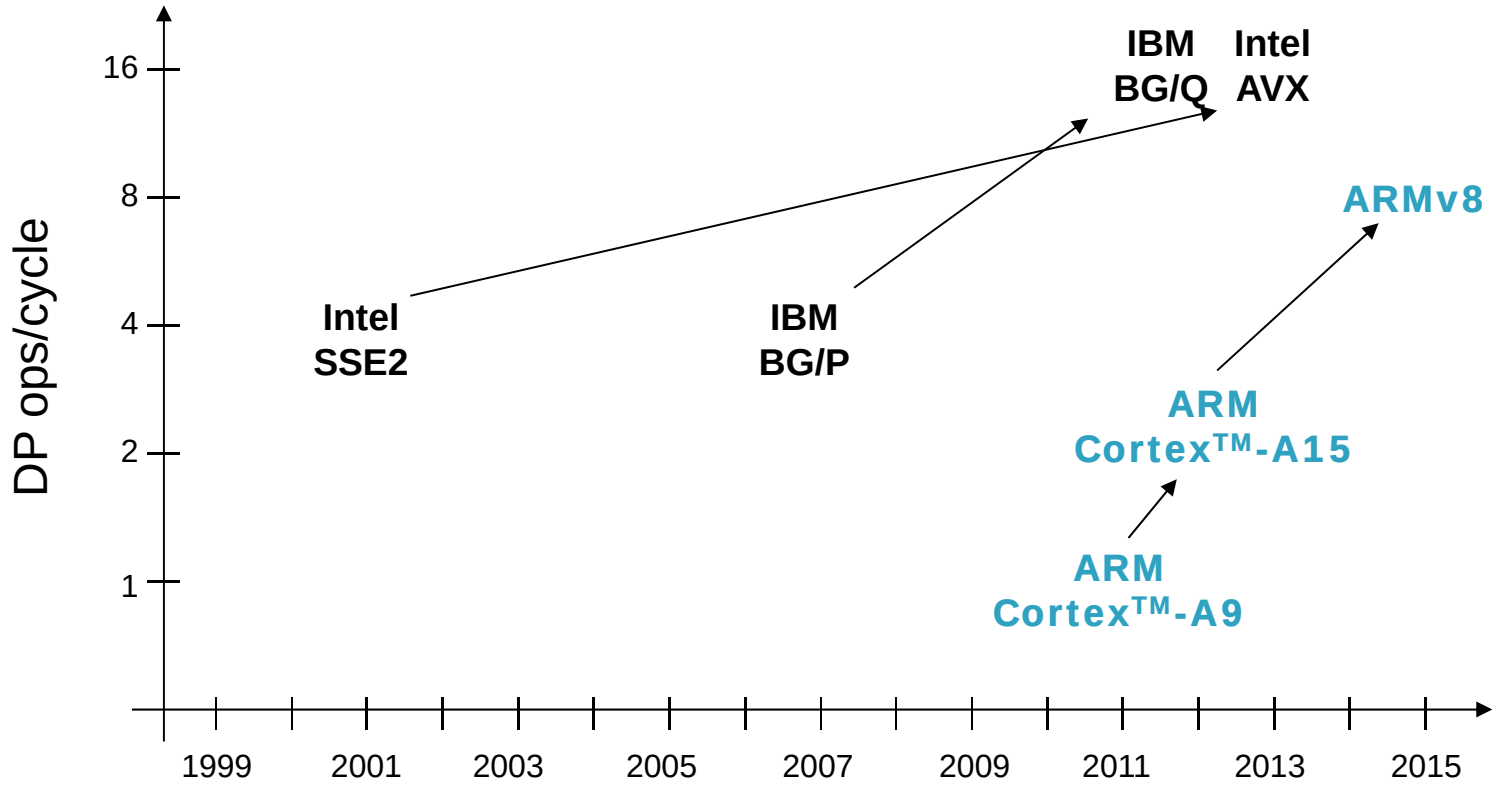
Message-Passing Programming Models

The next step in the commodity chain



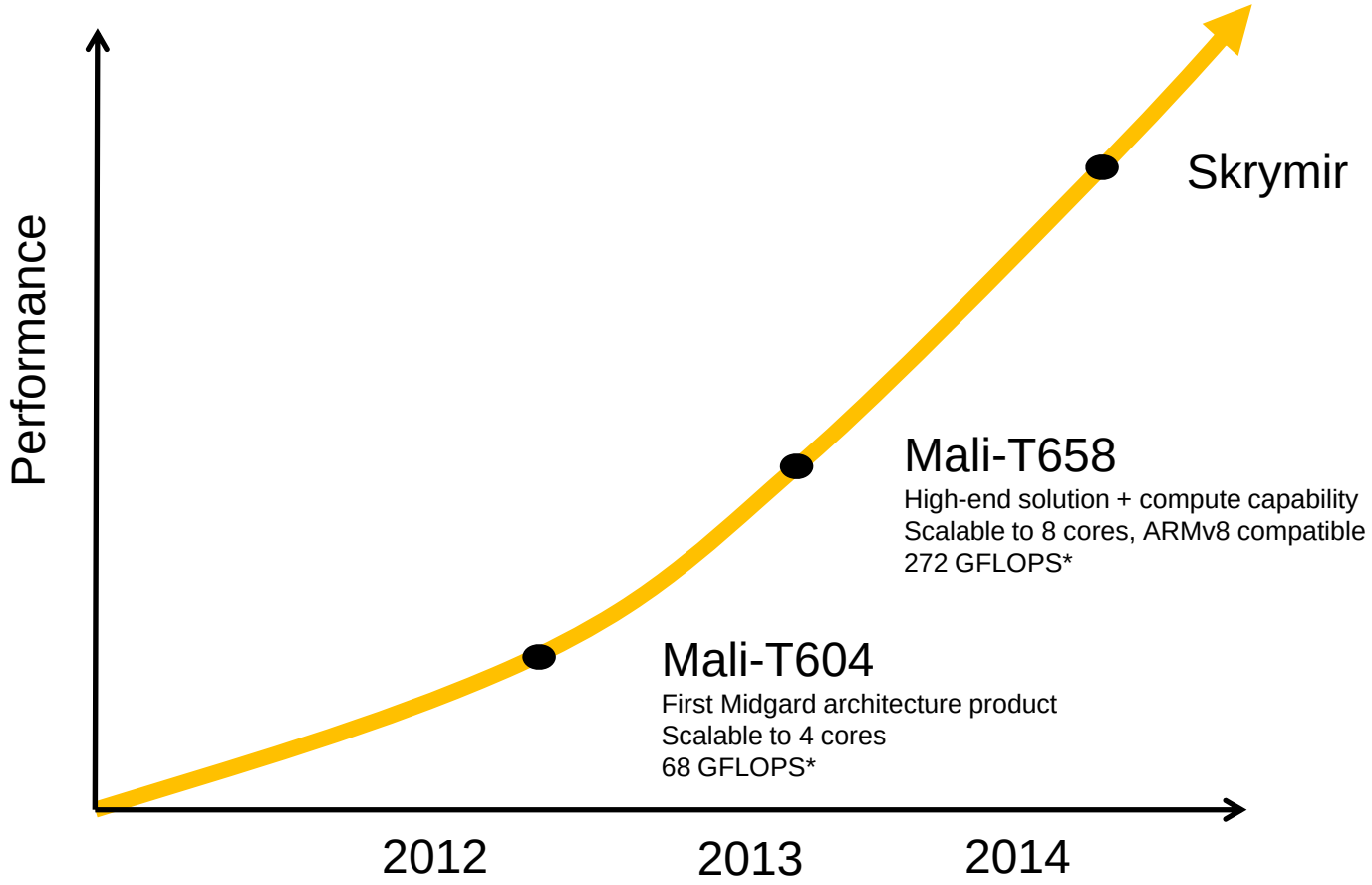
- Total cores in Jun'12 Top500
  - 13.5 Mcores
- Tablets sold in Q4 2011
  - 27 Mtablets
- Smartphones sold Q4 2011
  - > 100 Mphones

ARM Processor improvements in DP FLOPS



- IBM BG/Q and Intel AVX implement DP in 256-bit SIMD
  - 8 DP ops / cycle
- ARM quickly moved from optional floating-point to state-of-the-art
  - ARMv8 ISA introduces DP in the NEON instruction set (128-bit SIMD)

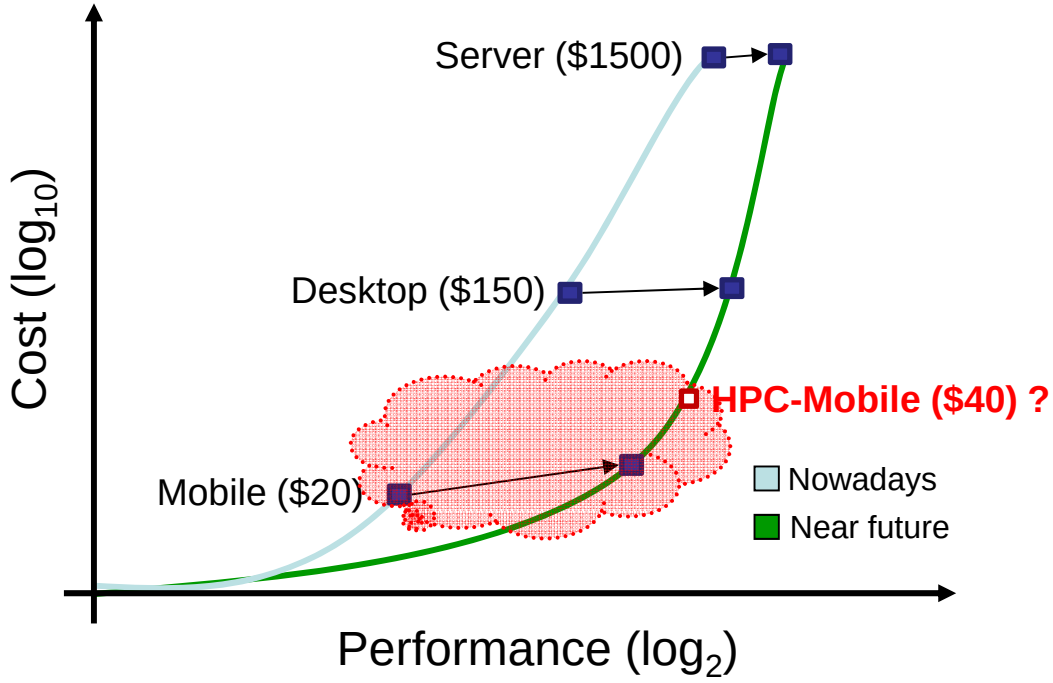
Integrated ARM GPU performance



- GPU compute performance increases faster than Moore's Law

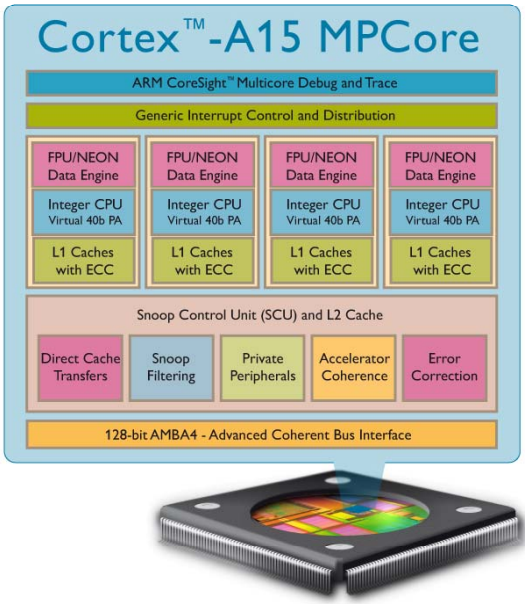
* Data from web sources, not an ARM commitment

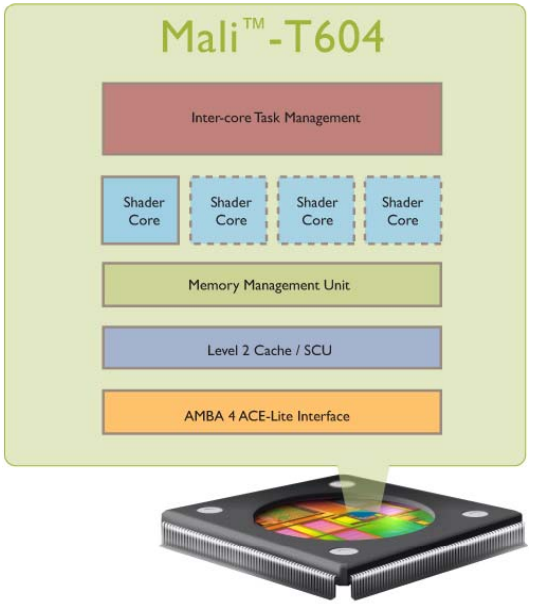
Are the “Killer Mobiles™" coming?



- Where is the sweet spot? Maybe in the low-end ...
  - Today ~ 1:8 ratio in performance, 1:100 ratio in cost
  - Tomorrow ~ 1:2 ratio in performance, still 1:100 in cost ?
- The same reason why microprocessors killed supercomputers
  - Not so much performance ... but much lower cost, and power

Samsung Exynos 5 Dual Superphone SoC





- 32nm HKMG
- Dual-core ARM Cortex-A15 @ 1.7 GHz
- Quad-core ARM Mali T604
  - OpenCL 1.1
- Dual-channel DDR3
- USB 3.0 to 1 GbE bridge

- **All in a low-power mobile socket**

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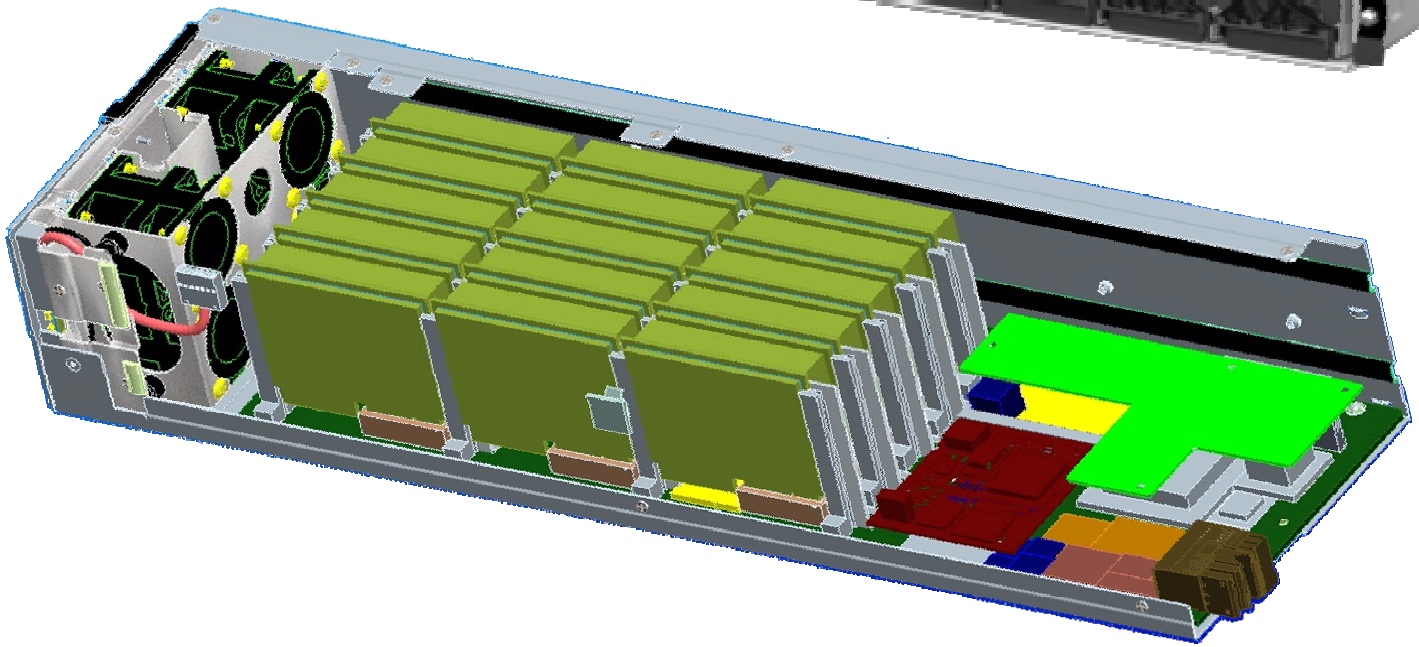
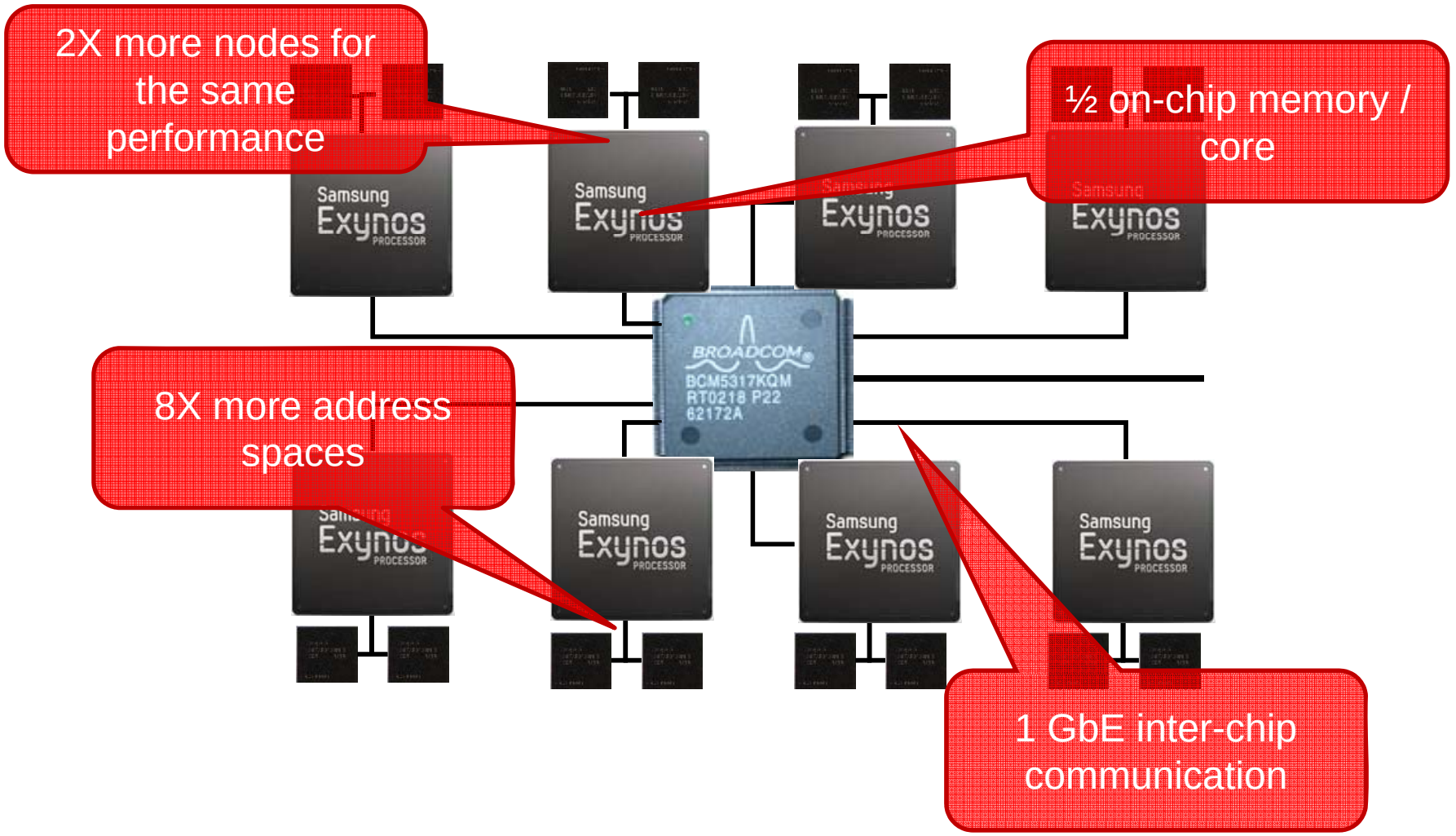
High density packaging architecture

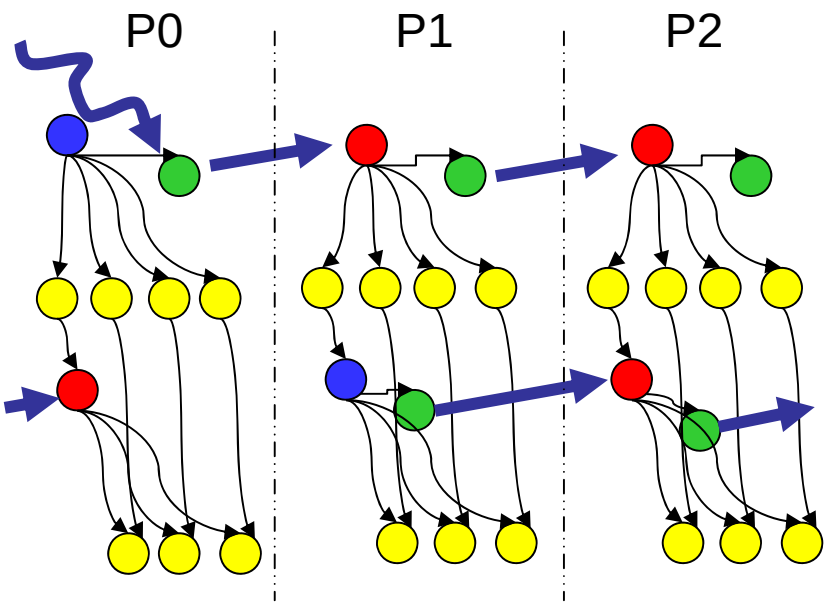
- Standard BullX blade enclosure
- Multiple compute nodes per blade
  - Additional level of interconnect, on-blade network

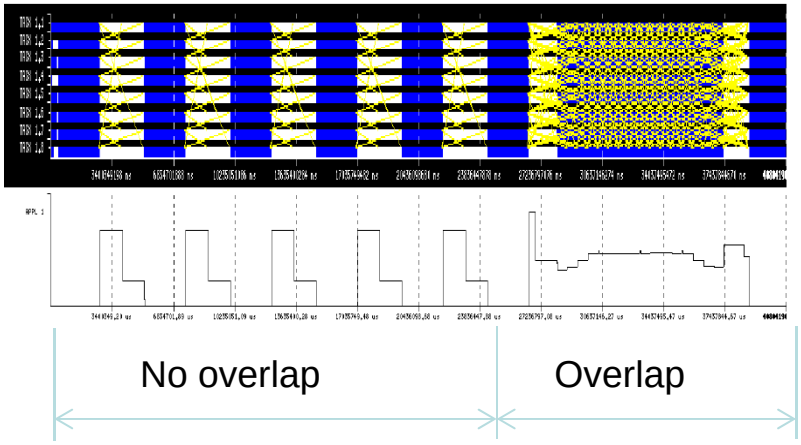


There is no free lunch



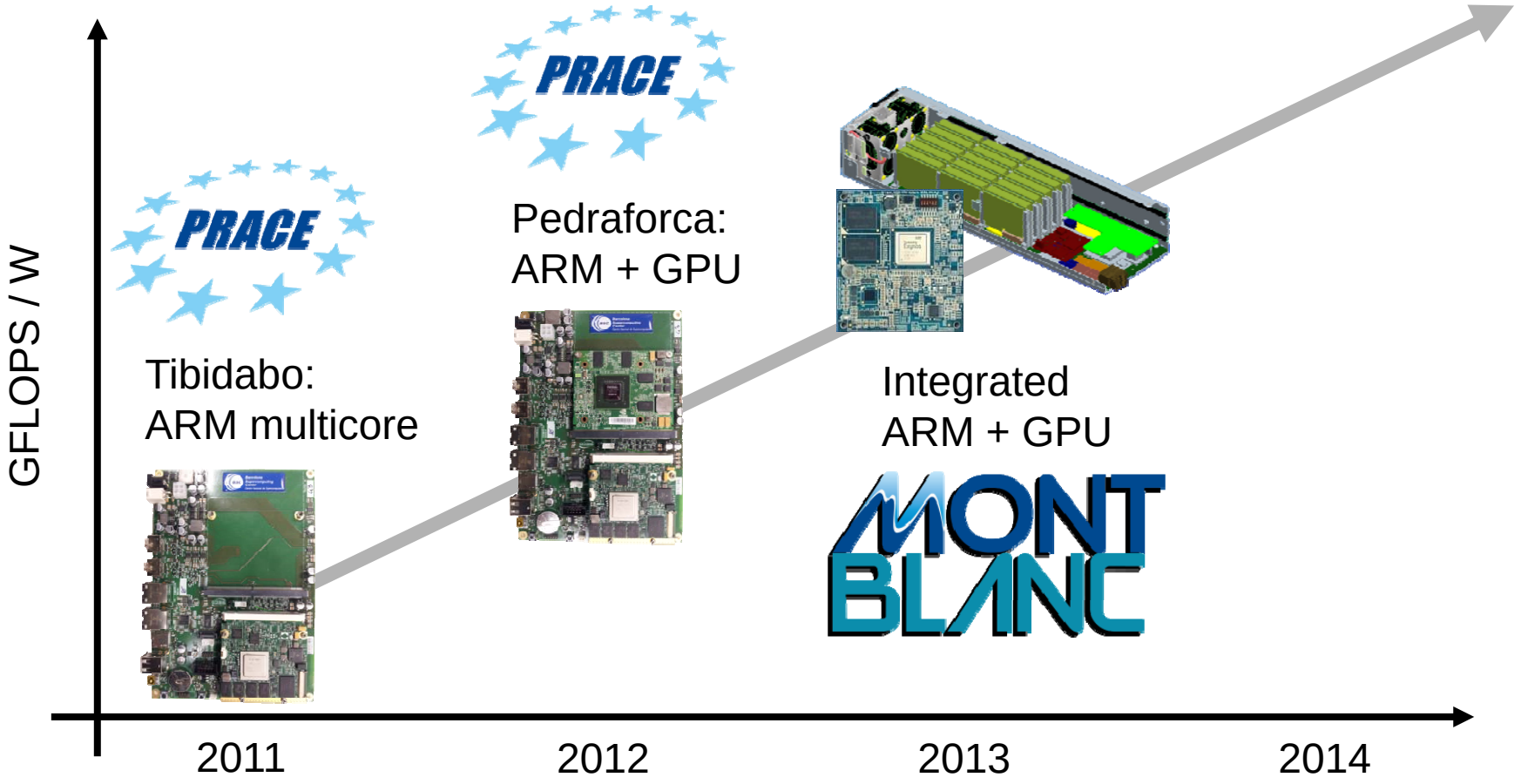
OmpSs runtime layer manages architecture complexity





- Programmer exposed a simple architecture
- Task graph provides lookahead
  - Exploit knowledge about the future
- Automatically handle all of the architecture challenges
  - Strong scalability
  - Multiple address spaces
  - Low cache size
  - Low interconnect bandwidth
- Enjoy the positive aspects
  - Energy efficiency
  - Low cost

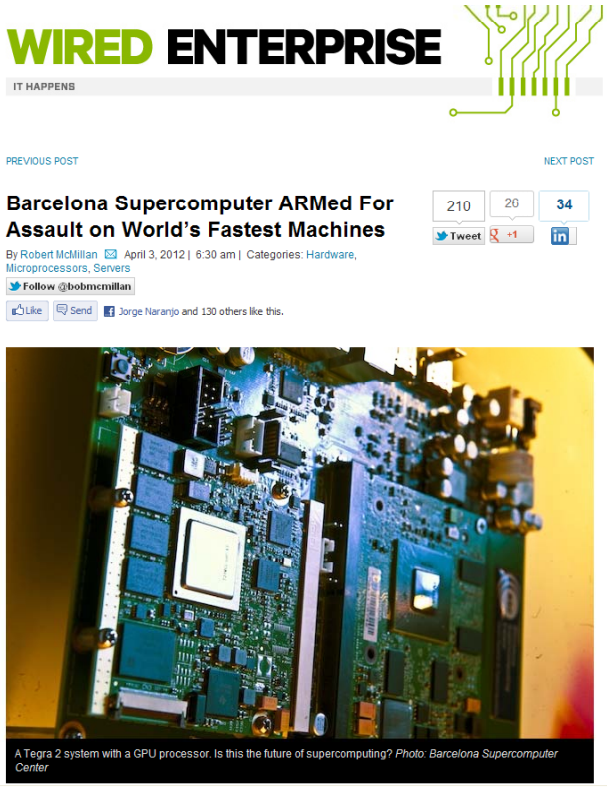
BSC ARM-based prototype roadmap

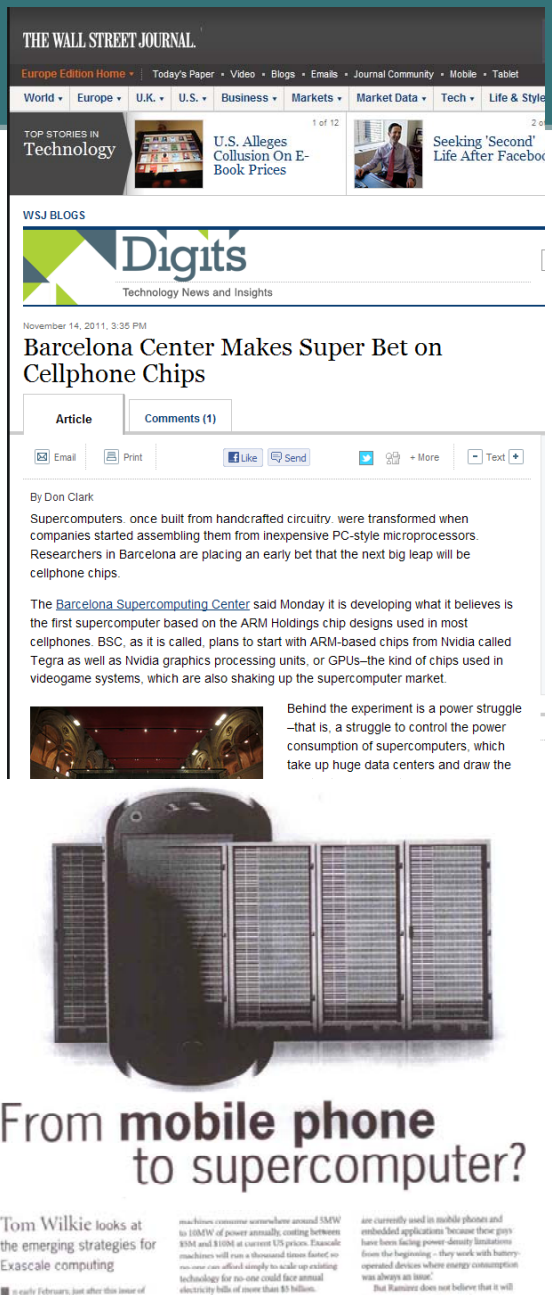


- Prototypes are critical to accelerate software development
  - System software stack + applications

Very high expectations ...

- High media impact of ARM-based HPC
- Scientific, HPC, general press quote Mont-Blanc objectives
  - Highlighted by Eric Schmidt, Google Executive Chairman, at the EC's Innovation Convention





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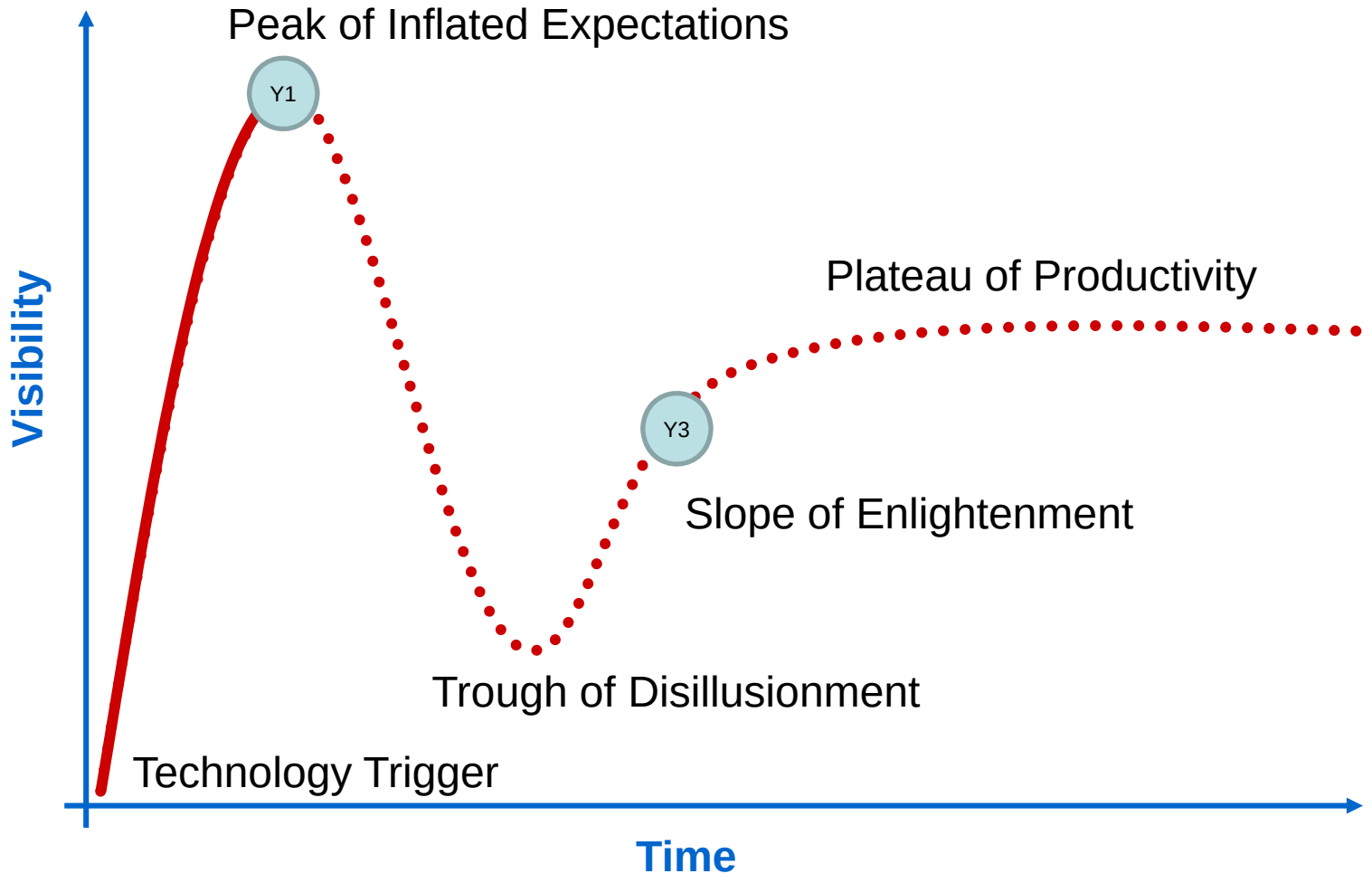
The hype curve



- We'll see how deep it gets on the way down ...

Conclusions

- Mont-Blanc architecture is shaping up
  - ARM multicore + integrated OpenCL accelerator
  - Ethernet NIC
  - High density packaging
- OmpSs programming model port to OpenCL
- Applications being ported to tasking model

- Stay tuned!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