## Honeywell RedLINK reverse-engineering experiments

The project is to create hardware and software to understand the Honeywell RedLINK wireless HVAC communication, and then build compatible devices.

Honeywell uses (and licenses to Mitsubishi) a proprietary wireless network to communicate among thermostats, temperature sensors, and wireless receivers connected to heating and air condition equipment like fancoils and heat pumps. They do not publicly document the details.

The network is similar to WiFi, but not the same. It is frequency-hopping spread spectrum communication in the 902-926 Mhz band. Data is sent in small packets up to about 30 bytes.

This project is a work in progress, and I will post updates here from time to time. As of 7 May 2015, I've built a Sniffer to decode the traffic between the Honeywell microprocessor in a remote temperature sensor and the TI CC1101 RF transceiver. I see how the chip is configured (and reconfigured when the frequency changes), and I see some examples of packets sent by the sensor.

Here are possible next steps:

- capture more examples of packets from other devices and try to deduce the format and protocol
- build a board with an Arduino that controls an RF transceiver and can send and receive commands (I'm going to try using the Anaren A1101R09A-EM1 evaluation board)

This is all a leisure-time activity, so it's not clear how quickly I will make more progress.
-- Len Shustek

## RedLINK CC1101 RF transceiver configuration

| reg <br> addr | name | value in hex | interpretation |
| :---: | :---: | :---: | :---: |
| 00 | GDO 2 | 06 | output is "sync word sent/rcvd" |
| 01 | GDO 1 | OD | output is "serial data out" |
| 02 | GDO 0 | $\begin{aligned} & 2 \mathrm{~F} . \\ & 38 \end{aligned}$ | output is sometimes "hardwired to 0" and sometimes "CLK XOSC/16" |
| 03 | FIFO threshold | 47 | ADC retention, threshold is 32 bytes TX, 32 bytes RX (of 64-byte FIFOs) |
| 04/05 | sync word | 63xx, | where xx varies with the channel number; see table below |
| 06 | packet length | 63 | 99 bytes (but not used in variable-packet mode) |
| 07 | packet control 1 | 44 | ```preamble quality threshold 2 no autoflush of RX FIFO on bad CRC append 2 status bytes to packet RSSI (dBm signal power), CRC OK, LQI) no address check``` |
| 08 | packet control 0 | 45 | ```data whitening on normal FIFO mode CRC enabled variable packet length, set by first byte after sync word``` |
| 09 | device address | $\begin{array}{ll} 0, & \text { or } \\ 06 \end{array}$ | (for packet filtering) |
| OA | channel number | varies | hops among 50 values; see table below |
| 0B | frequency control 1 | 06 | IF frequency: 152 Khz |
| OC | frequency control 0 | 00 | frequency offset for base, in units of 1587 Hz (none) |
| $\begin{aligned} & \text { OD/OE } \\ & \text { /OF } \end{aligned}$ | frequency control word (H/M/L, 24 bits) | $\begin{aligned} & \text { 22B333 } \\ & \text { 22B330 } \end{aligned}$ | $\begin{aligned} & 2,274,099 * 396.7=902.1350 \mathrm{Mhz} \text { (only at init) } \\ & 2,274,096 * 396.7=902.1338 \mathrm{Mhz} \text { (all other times) } \end{aligned}$ |
| 10 | modem config 4 | CA | $\begin{aligned} & \mathrm{BW}=26 \mathrm{MHz} /(8 *(4+00) * 2 * * 3)=26 \mathrm{Mhz} /(32 * 8)=101.5 \mathrm{Khz} \\ & \text { symbol rate exponent }=10 \end{aligned}$ |
| 11 | modem config 3 | 83 | ```symbol rate mantissa = 0x83 = 131 symbol rate = 26 Mhz * (256+131)*2**10)/2**28 = 38.383 Kb``` |
| 12 | modem config 2 | 12 | enable DC blocking, GFSK modulation, disable Manchester, $16 / 16$ sync word bits |
| 13 | modem config 1 | 62 | disable forward error correction, 16 preamble bytes, chan spacing exponent $=2$ |
| 14 | modem config 0 | F8 | chan spacing mantissa $=248$. default spacing $=199.951 \mathrm{Khz}$ |
| 15 | deviation | 34 | exp=3, man=4; deviation $=19.0 \mathrm{Khz}$ |
| 16 | state machine 2 | 07 | default (end-of-packet timeout for sync) |
| 17 | state machine 1 | 00 | CCA always, go idle after packet sent or received |


| 18 | state machine 0 | 18 | calibrate when going to RX or TX from idle; <br> expire count 64 (149-155 usec) |
| :--- | :--- | :--- | :--- |
| 19 | freq offset config | 16 | gain 3K, K/2, sat BWchan/4 |
| 1A | bit sync config | 6 C | defaults |
| 1B | AGC control 2 | 43 |  |
| 1C | AGC control 1 | 40 |  |
| 1D | AGC control 0 | 91 |  |
| 1E/1F | event timeout (H/L) | 876 B | default $=34,667$, or 1 second |
| 20 | wake on radio control | F8 | default |
| 21 | RX config | 56 | default |
| 22 | TX config | 10 | default (select PATABLE entry 0) |
| 23 | freq cal 3 | E9 |  |
| 24 | freq cal 2 | 2 A |  |
| 25 | freq cal 1 | 00 |  |
| 26 | freq cal 0 | $1 F$ |  |
| 27 | RC osc config 1 | 41 |  |
| 28 | RC osc config 0 | 00 |  |
| 29 | freq calib ctl | 59 | default |
| 2A | prod test | $7 F$ | default |
| 2B | AGC test | 3F | default |
| 2C | test2 | 81 |  |
| 2D | test1 | 35 |  |
| 2E | test0 | 09 |  |
| $\ldots$ |  |  |  |
| 3E | PATABLE (power amp) | C0 | default, always |

## Other notes

JimmySwimmy says RedLINK uses "50 channels, 903 to $926.4 \mathrm{Mhz}, 69 \mathrm{Khz}$ each channel, 400 Khz spacing". Based on the CC1101 configuration, I see 101.5 Khz bandwidth channels with spacing of 199.9 Khz.

With a base frequency of 902.13 Mhz and a maximum observed channel number of $0 \times 79=121$, that implies that the highest frequency is $902.13+121 * .1999=926.31$, which just fits into the allowed band.

In the US the FCC requires a minimum of 50 channels for $1 W$ operation in this band, and a channel change at least every 400 msec ; see http://www.ti.com.cn/cn/lit/an/swra077/swra077.pdf.

Here is the observed frequency-hopping sequence of 50 channel numbers that Honeywell uses and changes every 2.685 msec . That's 372.44 times per second. It goes through all 50 channels in 134.25 msec.
$71,38,75,49,0 C, 51,14,06,42,20,5 \mathrm{D}, 04,3 \mathrm{E}, 1 \mathrm{~A}, 57,1 \mathrm{C}, 59,79,3 \mathrm{C}, ~ 1 \mathrm{E}, ~ 5 \mathrm{~B}, 5 \mathrm{~F}, ~ 22,63,2 \mathrm{E}$, $46,0 A, 61,2 \mathrm{C}, 53,16,32,6 \mathrm{~F}, 3 \mathrm{~A}, 77,4 \mathrm{~F}, 12,44,08,6 \mathrm{D}, 30,4 \mathrm{D}, 10,18,55,36,73,0 \mathrm{E}, 4 \mathrm{~B}, 34$

Here is the low byte of the sync word corresponding to each channel; the high byte is always 63.
$98,81,9 A, 88,6 \mathrm{~F}, ~ 8 \mathrm{C}, ~ 73,6 \mathrm{C}, ~ 85,79,92,6 \mathrm{~B}, 84,76,8 \mathrm{~F}, 77,90,9 \mathrm{C}, ~ 83,78,91,93,7 \mathrm{~A}, 95,7 \mathrm{C}, ~$ 87, 6E, 94, 7B, 8D, 74, 7E, 97, 82, 9B, 8B, 72, 86, 6D, 96, 7D, 8A, 71, 75, 8E, 80, 99, 70, 89, 7F

I'm guessing these are just stored in a table, not generated by an algorithm in the microprocessor.

The CC1101 chip takes 712-724 usec to calibrate after each frequency hop, so the blanking interval is 787-799 usec.

- Receiver enables receive every 2.685 msec in normal channel sequence, 134.25 msec around
- On channel 49, waits 90.326 msec , then skips to 3 A and continues normally with 77 - 90.326 msec is 33.64 channels
- On channel 36, waits 86.544 msec , then skips to 4 F (40?? chans away) and continues normally with 12 o 86.544 msec is 32.232 channels
- On channel 49, waits 88.620 msec then skips to 12 (33 chans away) and continues normally with 44 - 88.620 msec is 33 channels
- On channel 0C, waits, 88.620 msec , then skips to 44 (33 chans away) and continues normally with 08 o 88.620 msec is 33 channels
- On channel 51, waits 88.619 msec , then skips to 08 (33 chans away) and continues normally with 6D - 88.619 msec is 33 channels
- With rcv enb on chan 04 , sends 22 bytes on chans 3E, 1A, 57, and 1C (normal sequence) 59 msec apart - 59 msec is 22 channels
- Then wait 15 msec and rcv enb on chan 77 (19 chans away) then 4 F , $12 \ldots$ (normal sequence)
- 15 msec is 5.6 channels
- With rcv enb on chan 20 for 142 msec , sends 13 bytes on chan 5D (normal sequence), then enb rcv 5D - 142 msec is 52.88 channels
- Then waits 15 msec and rcv enb $1 E$ ( 9 chans away) and then normal rcv sequence - 15 msec is 5.6 chans
- On channel 53, waits 88.620 msec then skips to 3 E (33 chans away) and continues normally with $1 A$ - 88.620 msec is 33 chans
- With rcv enb on chan 77 for 142 msec sends 13 bytes on chan $4 F$ (normal sequence) then enb rcv $4 F$
- Then waits 11.7 msec and rcv enb 18 ( 8 chans away) and then normal rcv sequence
- 11.7 msec is 4.3 chans
- With rcv enb on chan $4 F$ for 142 msec sends 13 bytes on chan 12 (normal sequence) then enb rcv 12
- Then waits 87.6 msec and rcv enb 22 (36 chans away) and then normal rcv sequence - 87.6 msec is 32.6 chans
- With rcv enb on chan $0 E$ for 142 msec , sends 13 bytes on chan $4 B$ (normal sequence) then enb rcv $4 B$
- Then waits 11.7 msec and rcv enb 14 ( 8 chans away) and then normal rcv sequence
- On channel 73, waits 86.2 msec . then skips to 53 ( 33 chans away) and continues normally with 16
- On channel 0E, waits 88.6 msec , then skips to 16 (33 chans away) and continues normally with 32
- On channel $4 B$, waits 88.6 msec , then skips to 32 ( 33 chans away) and continues normally with $6 F$
- On channel 34, waits 88.6 msec , then skips to 6 F ( 33 chans away) and continues normally with $3 A$
- On channel 38, waits 86.2 msec , then skips to 77 ( 33 chans away) and continues normally with $4 F$
- On channel 75, waits 88.6 msec , then skips to 4 F ( 33 chans away) and continues normally with 12
- On channel 49, waits 107.4 mse, then skips to 36 (42 chans away) and continues normally with 73
- 107.4 msec is 40.00 chans
- On channel 14, waits 91.13 msec , then skips to 34 (43 chans away) and continues normally with 71
- On channel 4D, waits 135 msec and receives $10+5$ bytes on 4 D then sends 22 bytes on 4 D
- Rcv enb on 4B (7 chans away) and then continues normally with 34
- On channel 79, waits 14.9 msec and receives $10+5$ bytes on 79 , then sends 14 bytes on 79

Packet exchange:
rcvr: 22 bytes,

It sends 19 or 22 byte packets every $1 / 2$ second or so.
19 x 8 at 38.383 Khz would be 3.96 msec
22 x 8 at 38.383 Khz would be 4.58 msec
At 38.383 Khz symbol rate, each byte would take 208 usec. Each bit would take 26 usec.
But on the scope, small packets take 82 usec, large take 275 usec. What's going on? That's much faster than the symbol rate as computed above.

Packets start with 16 preamble bytes (or more if data isn't in the FIFO yet), then 2 bytes of sync, then length, then data, then 2-byte CRC. So a 22 byte data packet really takes $16+2+1+22+2=43$ bytes.

For the 275 usec packets it looks on the scope like 48 bytes $+2 * 7$ bytes +1 byte $=63$ bytes? Each of the 48 bytes takes 2 usec with 1.5 usec between. Thus 3.5 usec/byte.
(Is that per bit with GFSK? Still doesn't comport with 19 or 22 byte packets.)
**** UPDATE: the scope traces are misleading; it's seeing communication with the CC1101 chip!!

The receiver changes listening channels every 2.685 msec , yet somehow it receives the packet! How does it know the frequency?

The temp sensor uses the same 50 channels, but in a different sequence that doesn't depend on the timing. It always uses two adjacent channels of the normal sequence, sometimes forward, sometimes reversed.

Example transmitted data packets from the Honeywell C7189R1004 indoor temperature sensor when not linked to any receiver:

122330 OB FF FE E8 1F F0 000087821200 E8 1F FF 81
12232003 FF FE E 81 F FO 000087821200 E 81 F FF 81 (chan 1E, 44, 08)
1223 F 43 F FF FE E8 1F F0 000087821200 E 81 F FF 81
$1503 \quad 31$ E4 E8 1F E8 1F F0 0100 0A $1280 \quad 00463407$ ED 7 F FF 06 ff ff ff next freq?
1503 9F 3D E8 1F E8 1F F0 0100 0A 128000463408 BC 7F FF 06
15035665 E 81 F E 81 F FO 0100 OA 128000463408 BC 7 F FF 00
150302 F 5 E 81 F E 81 F F0 0100 0A 128000463408 C 47 F FF 00
$150351 \quad 61$ E8 1F E8 1F F0 0100 OA 1280
150316 A9 E8 1F E8 1F F0 0100 0A 128000463408 C 7 7F FF 00
15033124 E 81 F E 81 F F0 $0100 \mathrm{OA} 1280 \quad 00463408 \mathrm{CC} 7 \mathrm{~F}$ FF 00
15039873 E 81 F E 81 F F0 0100 0A 128000463308 D2 7 F FF 00
1503 E 9 7A E8 1F E8 1F F0 0100 0A 128000463308 D7 7F FF 00
150335 9A E8 1F E8 1F FO 0100 0A 128000463308 DC 7F FF 00
$15030153 \mathrm{E} 8 \quad 1 \mathrm{~F}$ E8 1 F F0 0100 0A 1280
1503 A 3 EE E 81 F E 81 F FO 0100 A 128000463308 E 27 F FF 00
150379 FB E8 1F E8 1F F0 0100 0A $1280 \quad 00463308$ E4 7 F FF 00
150303 E 5 E 81 F E 81 F F 00100 0A 128000463308 EA 7 F FF 00
1503 FB AF E8 1F E8 1F F0 0100 OA 128000463308 E 7 7F FF 00
1503 2A E2 E8 1F E8 1F F0 0100 OA 1280
1503 F 24 F E8 1F E8 1F F0 0100 0A 128000463308 EC 7 F FF 00
150361 EF E8 1F E8 1F F0 0100 OA 128000463308 EF 7 F FF 00
1503 FD BD E8 1F E8 1F F0 0100 OA 128000463208 F 27 F FF 00
1503 EA DC E8 1F E8 1F F0 0100 OA 128000463208 F2 7 F FF 00
15035965 E 81 F E 81 F FO 0100 OA 128000463208 F 27 F FF 00
1503 B 54 F E8 1F E8 1F F0 0100 0A 128000463208 EF 7 F FF 00
15030905 E 81 F E8 1F F0 0100 0A 128000463208 F 27 F FF 00
150367 2D E8 1F E8 1F FO 01

1503 A5 50 E8 1F E8 1F F0 0100 OA 128000463208 F2 7 F FF 00
1503 7D 6B E8 1F E8 1F F0 0100 0A 128000463208 FA 7F FF 00
15038321 E8 1F E8 1F F0 0100 OA 128000463208 F7 7F FF 00 1503 D5 21 E8 1F E8 1F F0 0100 OA 128000463208 FD 7 F FF 00 ... missing chan 3A
1503 5A 5B E8 1F E8 1F FO 0100 OA 128000463208 FD 7F FF 00 1503 E2 97 E8 1F E8 1F F0 0100 OA 12 8000463208 FA 7F FF 00
 $1503604 D E 81 F E 81 F \operatorname{FO} 0100$ 0A $128000463209077 F \operatorname{FF} 00$

(chan 63, 2E, 73)
(chan 0E)
(chan 4B)
(chan 06)
(chan 42)
(chan 6D)
(chan 30)
(chan 49)
(chan 0C)
(chan 1A)
(chan 57)
(chan 4F)
(chan 12)
(chan 14)
(chan 51)
(chan 4D)
(chan 10)
(chan 5D)
(chan 20)
(chan 32)
(chan 6F)
(chan 71)
(chan 34)
(chan 75)
(chan 38)
(chan 16)
(chan 53)
(chan 77)
(chan 59)
(chan 1C)
(chan 18)
(chan 55)
(chan 22)
reset


|  | 03 | E | 1 F E8 | 1F FO | 010 |  | 0A 12 | 80 | 0 | 46 |  | 8 | F | F |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | 03 | FD BD E8 | 1 F E | 1 F | 01 | 00 0 | A 12 | 80 | 00 | 46 | 32 | 08 | F2 | 7 F | F | 00 |  | 5D) |
| 15 | 03 E | EA DC E8 | 1 F E8 | 1 F F0 | 010 | 00 0 | OA 12 | 80 | 00 | 46 | 32 | 08 | F2 | 7F | FF | 00 |  | 20) |
| 15 | 03 | 5965 E8 | 1F E8 | 1 F F0 | 010 | 00 0 | OA 12 | 80 | 00 | 46 | 32 | 08 | F2 | 7F | FF | 00 | (cha | 32) |
| 15 | 03 B | B5 4F E8 | 1 F E8 | 1 F F0 | 010 | 000 | OA 12 | 80 | 00 | 46 | 32 | 08 | EF | 7 F | FF | 00 |  | 6F) |
|  | 03 | 0905 E 8 | 1F E8 | 1 F | 01 | 0 | A 12 | 80 | 00 | 46 | 32 | 08 | F2 | 7 F | FF | 0 |  | 71) |
|  | 03 | 67 2D E8 | E | 1 F | 010 | 00 0 | 12 | 80 | 00 | 46 | 32 | 08 | 2 | 7 F | FF | 00 |  | 34) |
|  | 03 | C8 E9 E8 | 1 F E8 | 1 F F | 01 | 00 0 | OA 1 | 80 | 00 | 46 | 32 | 08 | F5 | 7 F | FF | 00 |  | 5) |
| 5 | 03 A | A5 50 E8 | 1 F E8 | $1 \mathrm{~F} \mathrm{F0}$ | 010 | 00 0 | OA 12 | 80 | 00 | 46 | 32 | 08 | F2 | 7F | FF | 00 |  |  |
| 5 | 03 | 7D 6B E8 | 1 F E | 1 F F0 | 01 | 00 0 | OA 12 | 80 | 00 | 46 | 32 | 08 | FA | 7F | FF | 00 |  | 16) |
| 15 | 03 | 8321 E8 | 1 F E | 1F F0 | 01 | 00 0 | OA 12 | 80 | 00 | 46 | 32 | 08 | F7 | 7 F | FF | 00 |  | 53) |
| 15 | 03 D | D5 21 E8 | 1 F E8 | 1 F FO | 01 | O | OA 12 | 80 | 00 | 46 | 32 | 08 | FD | 7 F | FF | 00 |  | 77) |
| 5 | 03 | 1D BD E8 | 1 F E8 | 1 F F0 | 010 | 0 | 0A 12 | 80 | 00 | 46 | 32 | 08 | FD | 7 F | FF | 0 |  | 3A) |
| 5 | 03 | 5A 5B E8 | 1 F E8 | 1 F F0 | 010 | 00 | OA 12 | 80 | 00 | 46 | 32 | 08 | FD | 7 F | FF | 00 |  | 59) |
| 5 | 03 E | E2 97 E8 | 1F E8 | 1 F F0 | 010 | 000 | 0A 12 | 80 | 00 | 46 | 32 | 08 | FA | 7 F | FF | 00 | ch | 1C) |
| 15 | 03 | CB 4C E8 | 1 F E8 | 1 F F0 | 010 | 000 | 0A 12 | 80 | 00 | 46 | 32 | 09 | 05 | 7 F | FF | 00 | (ch | 18) |
| 15 | 03 | 60 4D E8 | 1 F E8 | 1 F F0 | 010 | 000 | 0A 12 | 80 | 00 | 46 | 32 | 09 | 07 | F | FF | 00 | (chan | 55) |
| 5 | 03 B | B5 D1 E8 | F E | 1 F F | 010 | 000 | OA 12 | 80 | 0 | 46 | 32 | 09 | 02 | 7 F | FF | 00 | ( C | 22) |

## Does RedLINK use the IEEE 802.15 .4 standard, like ZigBee?

If so, then the packet format after the length byte would need to be like this:
General Frame Format

| octets: 2 | $\mathbf{1}$ | $0 / 2$ | $0 / 2 / 8$ | $0 / 2$ | $0 / 2 / 8$ | variable | $\mathbf{2}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frame <br> control | Sequence <br> number | Destination <br> PAN <br> identifier | Destination <br> address | Source <br> PAN <br> identifier | Source <br> address | Frame <br> payload | Frame <br> sequence <br> check |


| bits: $0=2$ | 3 | $\mathbf{4}$ | 5 | 6 | $\mathbf{7 - 9}$ | $\mathbf{1 0 - 1 1}$ | $12-13$ | $\mathbf{1 4 - 1 5}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Frame <br> type | Security <br> enabled | Frame <br> pending | Ack. <br> requested | Intra <br> PAN | Reserved | Dst addr <br> mode | Reserved | Sre addr <br> mode |

- IEEE 64-bit extended addresses (globally unique)
- 16-bit "short" addresses (unique within a PAN)
- Optional 16-bit source / destination PAN identifiers
- max. frame size 127 octets; max. frame header 25 octets
"All frame formats in this subclause are depicted in the order in which they are transmitted by the PHY, from left to right, where the leftmost bit is transmitted first in time. Bits within each field are numbered from 0 (leftmost and least significant) to $k-1$ (rightmost and most significant), where the length of the field is $k$ bits. Fields that are longer than a single octet are sent to the PHY in the order from the octet containing the lowest numbered bits to the octet containing the highest numbered bits."

I'm not sure how to interpret that because I don't know which way the TI CC1101 chip sends. But of the four interpretations of the $0 x 2330$ frame control we see (23 30, 30 23, bits reversed or not), the only one that has no bits in reserved fields on is 0011000000100011 , which means "data packet, security enabled, 16-bit dst addr, 64-bit src addr". It seems unlikely that the address sizes would be different. And that only leaves 5 bytes of payload.

So I don't think RedLINK is using 802.15.4.

