GateMateA1-EVB

User Manual

Rev.1.0 January 2024

olimex.com

Table of Contents

What is Cologne Chip GateMateA1

The GateMateTM FPGA family of Cologne Chip AG addresses all application requirements of small to medium size FPGAs. Logic capacity, power consumption, package size and PCB compatibility are best in class. GateMateTM FPGAs combine these features with lowest cost in industry making the devices well suited from University projects to high volume applications. Because of the outstanding circuit size/cost ratio, new applications now can use the benefits of FPGAs.

All this is based on a novel FPGA architecture combining CPE programmable elements with a smart routing engine. The CPE architecture allows an efficient building of arbitrarily-sized multipliers. Memory aware applications can use block RAMs with bit widths of 1 to 80 bits.

General Purpose IOs (GPIOs) can use different voltage levels from 1.2 to 2.5 Volt. All GPIOs can be configured as single-ended or LVDS differential pairs. Furthermore a high speed SerDes interface is available.

FPGA designs are synthesized using the Yosys framework. The free Cologne Chip P&R-software generates the FPGA bitstream.

A Static Timing Analysis (STA) is also performed and gives evidence about critical paths and the overall performance of a design. The design can be simulated using Verilog netlist and SDF timing extraction.

The devices are manufactured using GlobalfoundriesTM 28 nm SLP (Super Low Power) process. Due to manufacturing in Europe, there is no danger of trade restrictions or high taxation.

CCGM1A1 has these features:

- Logic Cells 20,480 CPE correspond to: 20,480 8-Input-LUT trees or, 40,960 4-Input-LUT trees with 40,960 FF/Latches
- Block RAM Total 1,280 Kb: 20Kb blocks: 64, 40Kb blocks: 32
- PLLs 4
- SerDes 5 Gb/s 1
- I/Os single-ended: 162, differential: 81, 1.2V to 2.5V, double data rate (DDR) support
- Performance Modes Low Power, Economy, Speed (0.9V – 1.1V)
- Package 324 balls 0.8mm fine pitch ball grid array (FBGA), 15x15 mm

GateMateA1-EVB features:

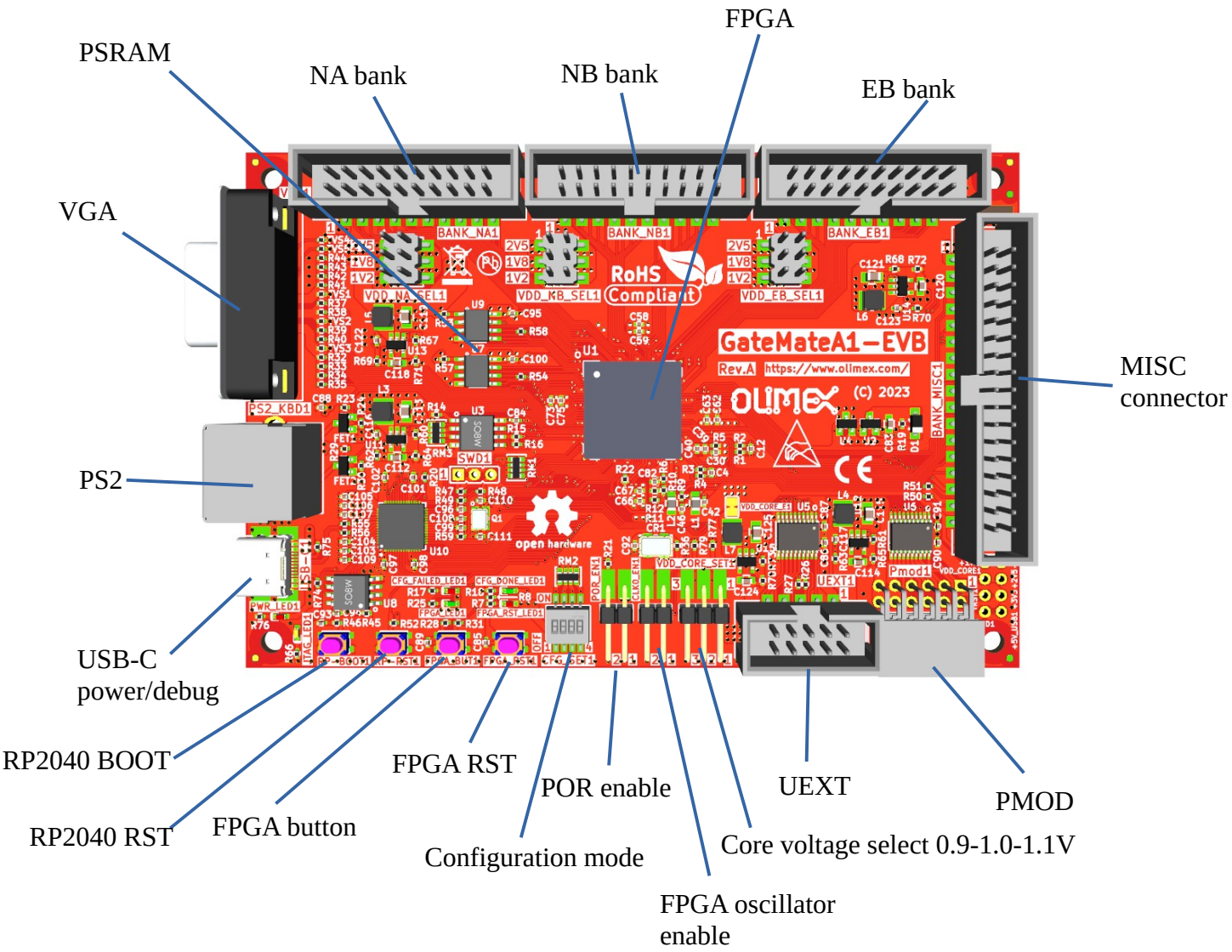
- CCGM1A1 FPGA with 20480 logic cells
- PSRAM 64Mbit
- RP2040 processor for programing and debugging
- 2MB configuration Flash
- 4 buttons
- USB-C for power supply and programming
- PS2 connector
- VGA connector
- 4 Banks with signals with selectable levels 1.2V 1.8V 2.5V
- PMOD with level shifters
- UEXT with level shifters
- Power LED
- User LED
- 4 sections configuration slide switch
- Dimensions: 120 x 80 mm

Order codes for GateMateA1-EVB:

GateMateA1-EVB	commercial grade -40+85C board with internal antenna
USB-CABLE-A-TO-C-1M	USB-C cable
UEXT modules	- different sensors, relays, LCDs, RTC, GSM, GPS etc accessories which can be connected to UEXT connector

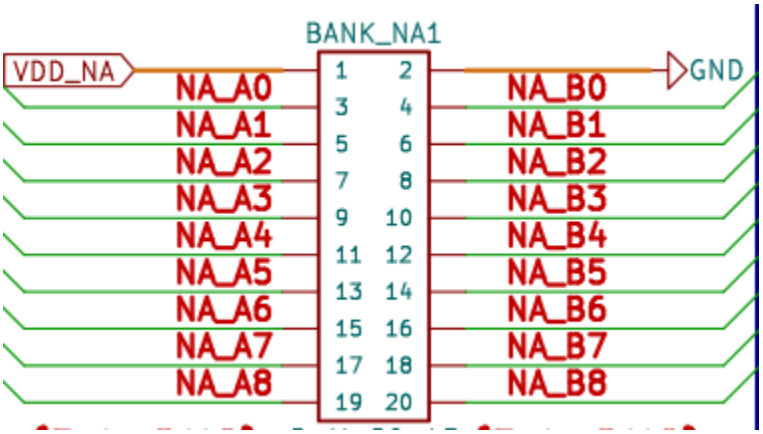
HARDWARE

GateMateA1-EVB layout:



GateMateA1-EVB GPIOs:

NA



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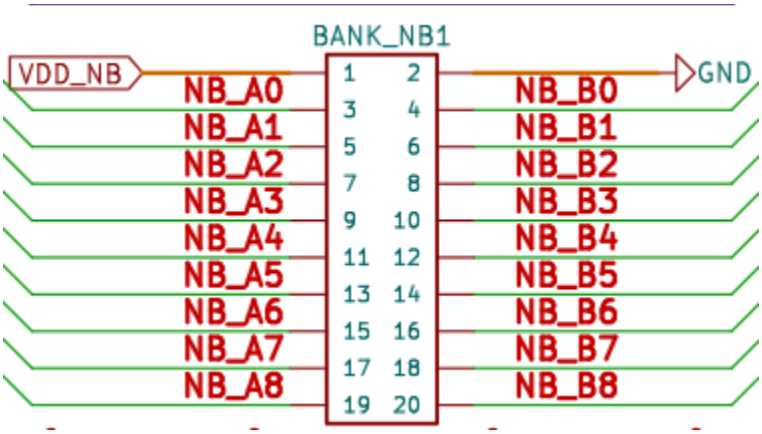

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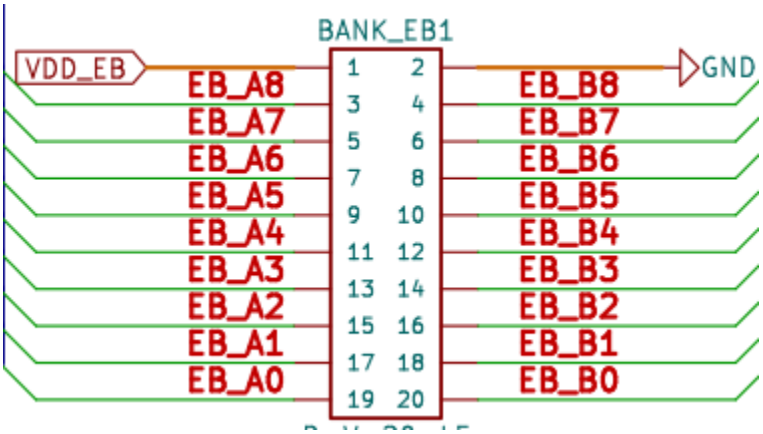
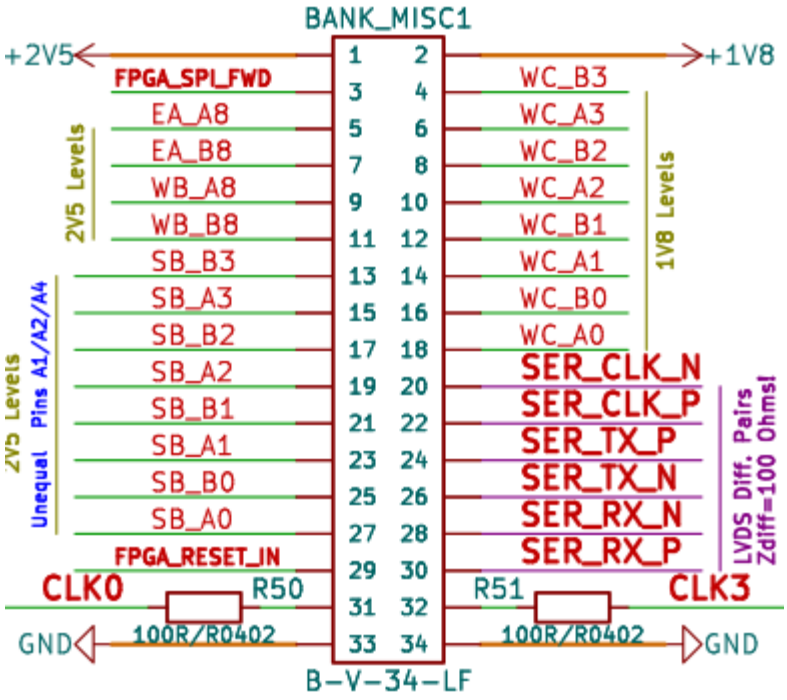
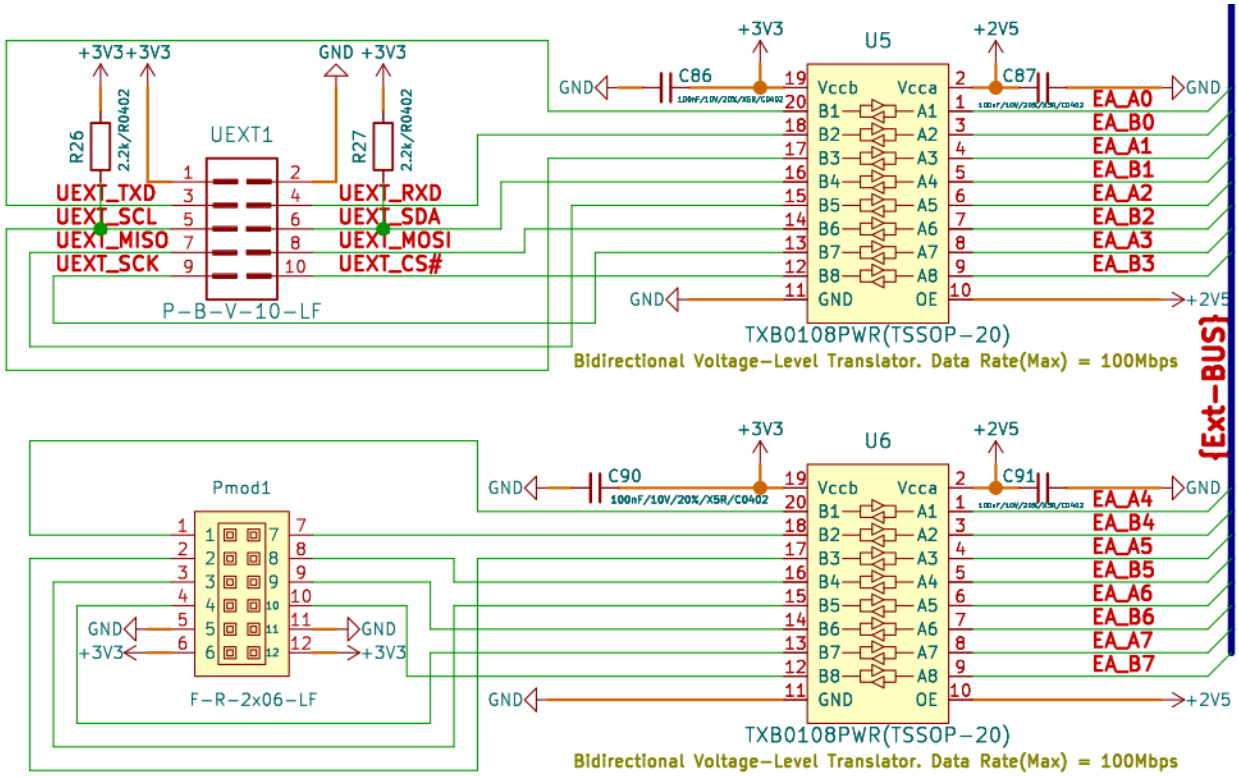


MISC



UEXT and PMOD



GateMateA1-EVB schematics:

GateMateA1-EVB latest schematic is on GitHub

GateMateA1-EVB power supply:

GateMateA1-EVB can be powered by USB-C connector.

The Core voltage can be changed between: 0.9-1.0-1.1V

The bank power supply can be selected between 1.2-1.8-2.5V

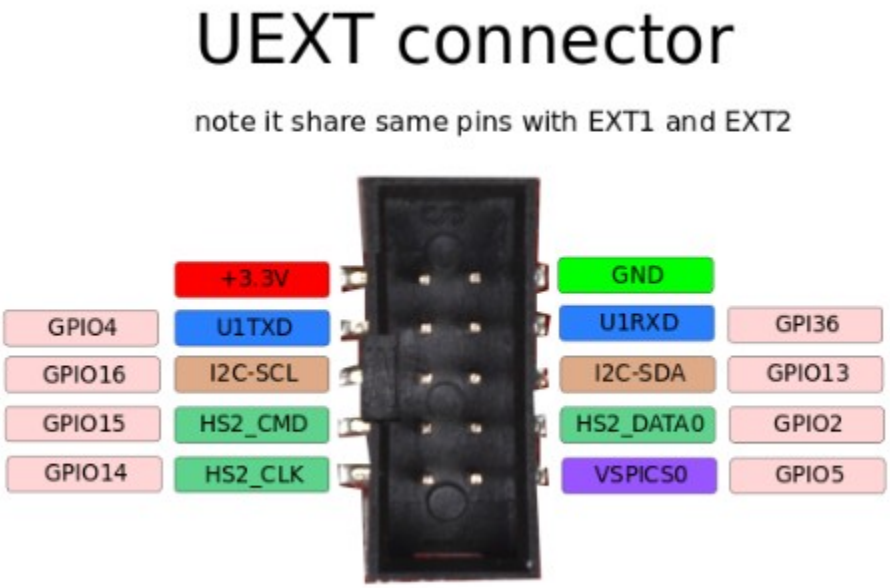
UEXT and PMOD are with 3.3V voltage levels.

UEXT connector:

UEXT connector stands for Universal EXTension connector and contain +3.3V, GND, I2C, SPI, UART signals.

UEXT connector can be in different shapes.

The original UEXT connector is 0.1” 2.54mm step boxed plastic connector. All signals are with 3.3V levels.



Olimex has developed number of MODULES with this connector. There are temperature, humidity, pressure, magnetic field, light sensors. Modules with LCDs, LED matrix, Relays, Bluetooth, Zigbee, WiFi, GSM, GPS, RFID, RTC, EKG, sensors and etc.

SOFTWARE:

Cologne Chip: Toolchain Installation guide

RP2040 firmware: pico-dirty-jtag

Cologne Chip example: Logic Analizer

Revision History

Revision 1.0 January 2024