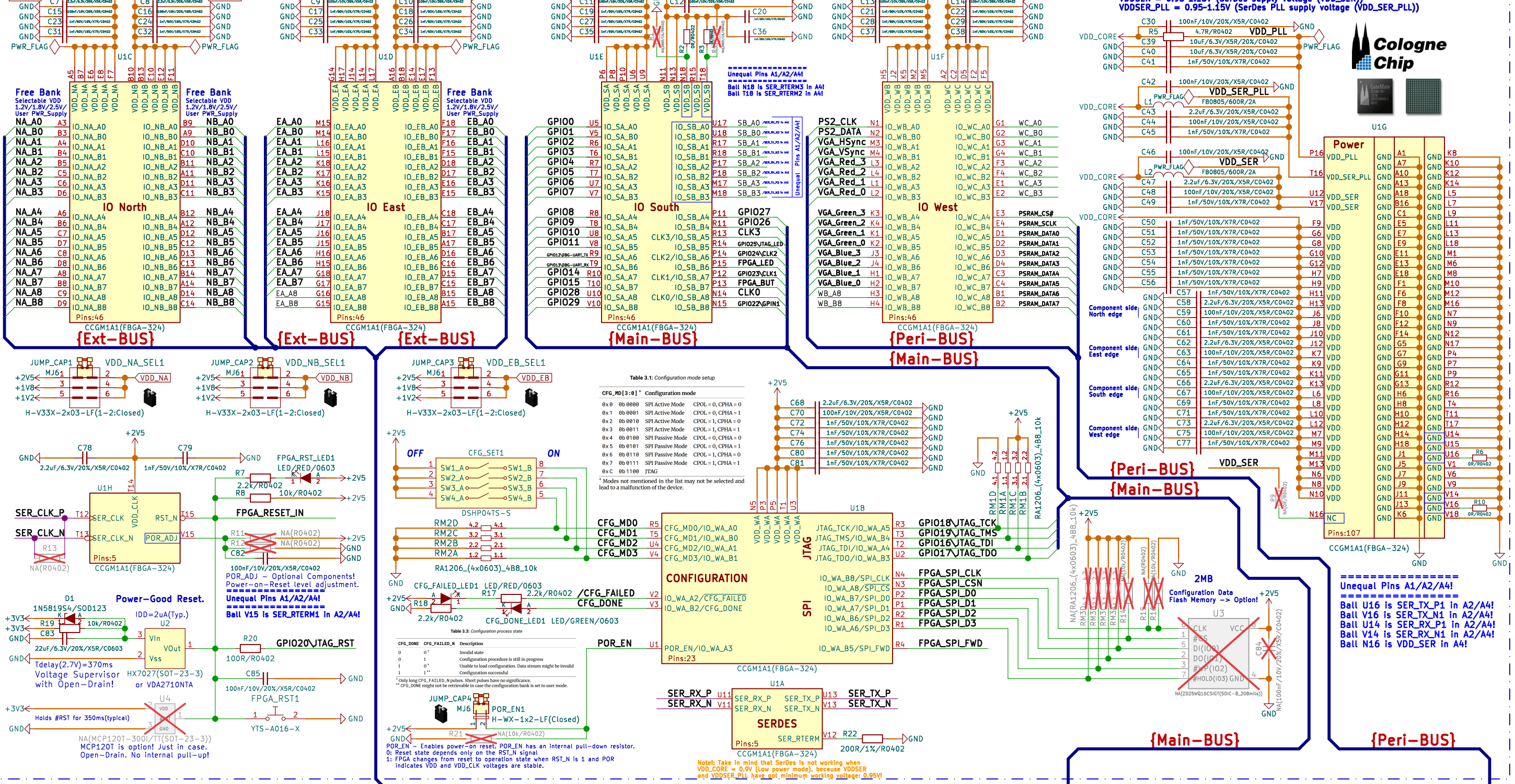
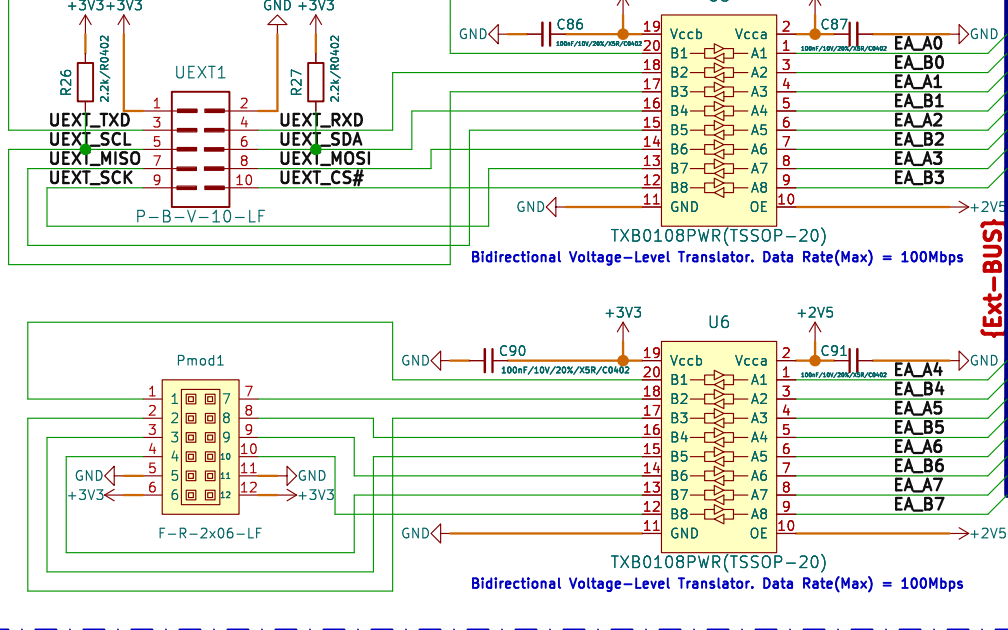


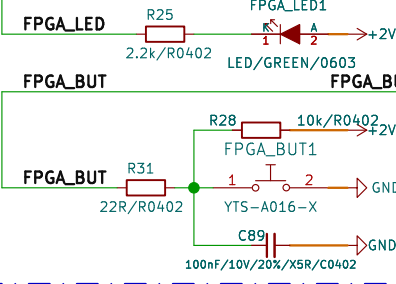
The schematic shows a multi-stage voltage divider network. It starts with VDD_NA connected to a resistor R1 (10k) leading to node C1 (+2V5). From C1, a resistor R2 (10k) leads to node C2 (GND), and another resistor R3 (10k) leads to node C3 (+2V5). Node C3 is connected to a resistor R4 (10k) leading to node C4 (GND), and another resistor R5 (10k) leads to node C5 (+2V5). Node C5 is connected to a resistor R6 (10k) leading to node C6 (GND), and another resistor R7 (10k) leads to node C7 (+2V5). The final output is +2V5.



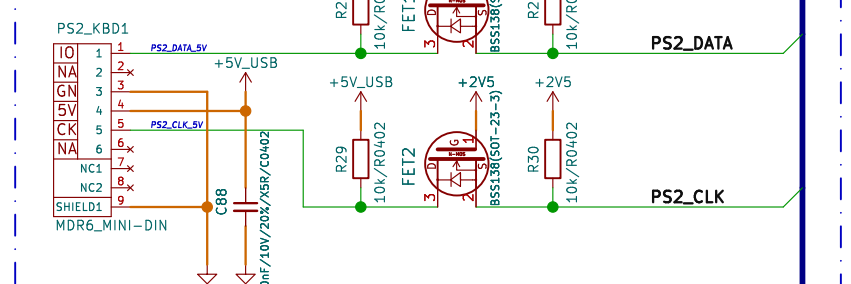
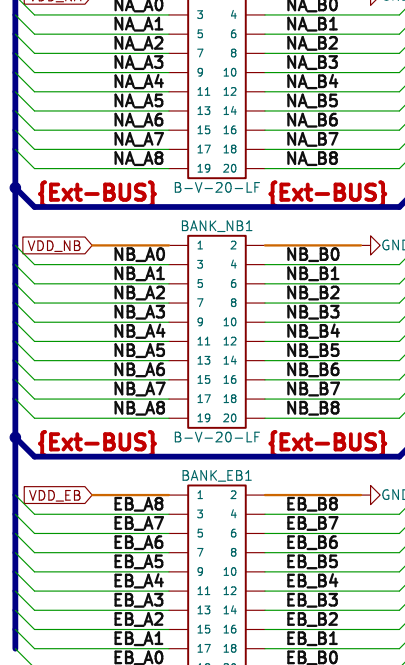
+3V3 U5



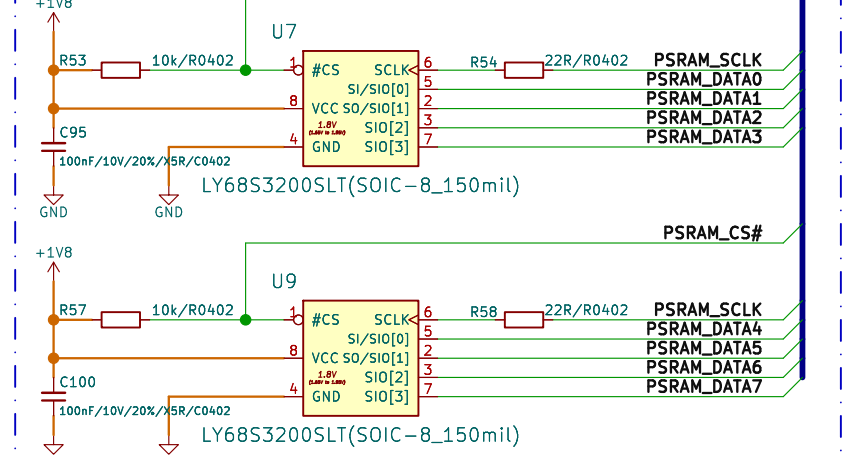
FPGA_LED FPGA_LED



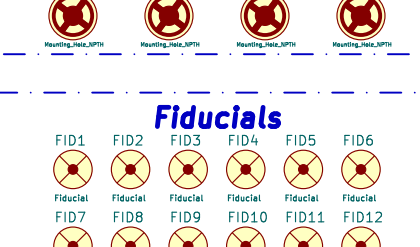
BANK_NA1



Clock rate: 100MHz(max) for fast read



MH1 MH2 MH3 MH4



Revis. Os Seguros:

