Summary of Problems and Experiences during the Processor Development based on Chisel

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Outline

- A Short Introduction to Chisel
  - Features and Benefits
  - Where to Learn Chisel
- Sharing of Experience Using Chisel
  - Problems We Met
  - Experiences Sharing
  - Syntactic Salt
  - …
- A RTL designer's perspective for Chisel

1. A Short Introduction to Chisel

IS

- Object-Oriented Programming
- Various and Convenient Hardware Generator
- Overall Signal Connection

Features

✓Improved readability and much shorter lines of code

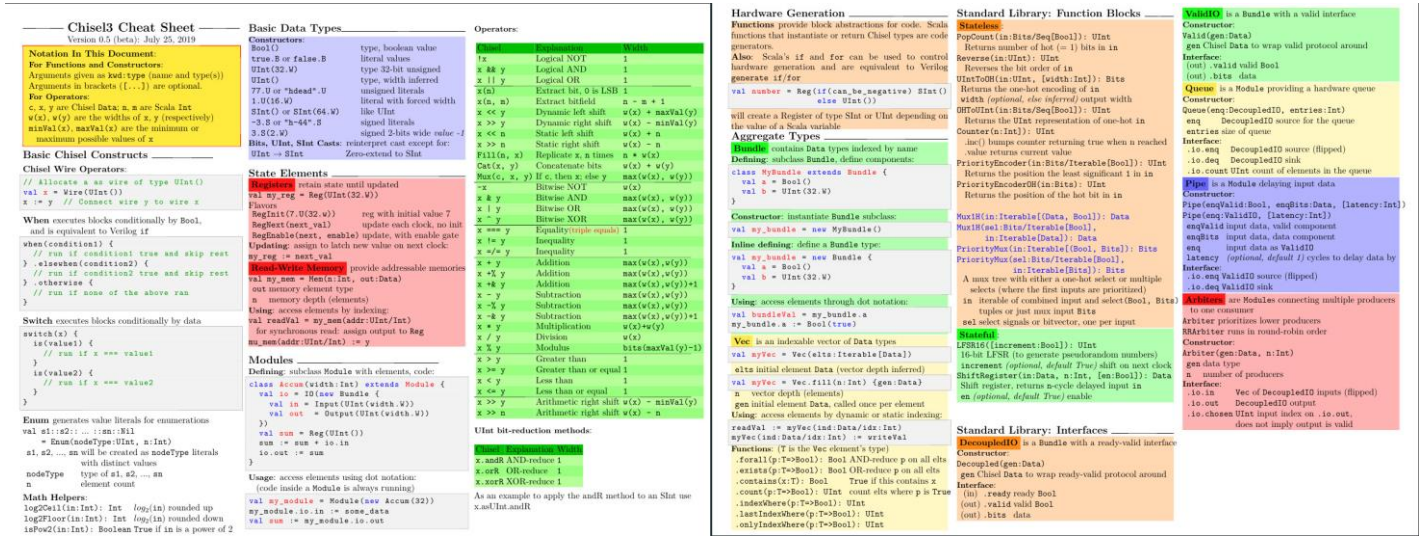
✓Flexible hardware module writing

✓Make designers focus on design, not some dirty work

Benefits

Where to Learn?

Advice: 2 pages of chisel-cheatsheet and an 896 pages scala book(just kidding…).



chisel-cheatsheet (colored version)
https://github.com/freechipsproject/chisel-cheatsheet/pull/2

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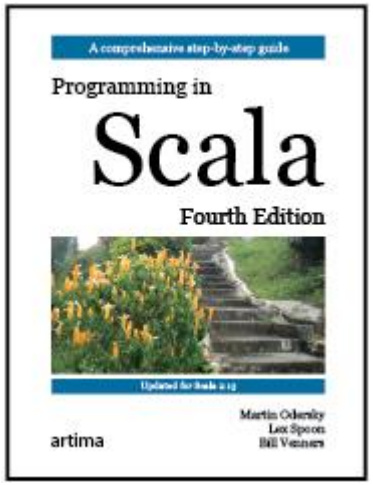


Programming in Scala(available online)

- Other excellent learning resources
  - chisel-cookbook https://www.chisel-lang.org/chisel3/docs/introduction.html
  - chisel-bootcamp https://github.com/freechipsproject/chisel-bootcamp
  - chisel-book(pdf) https://github.com/schoeberl/chisel-book

2. Problems & Experience Using Chisel

Software thinking

vs

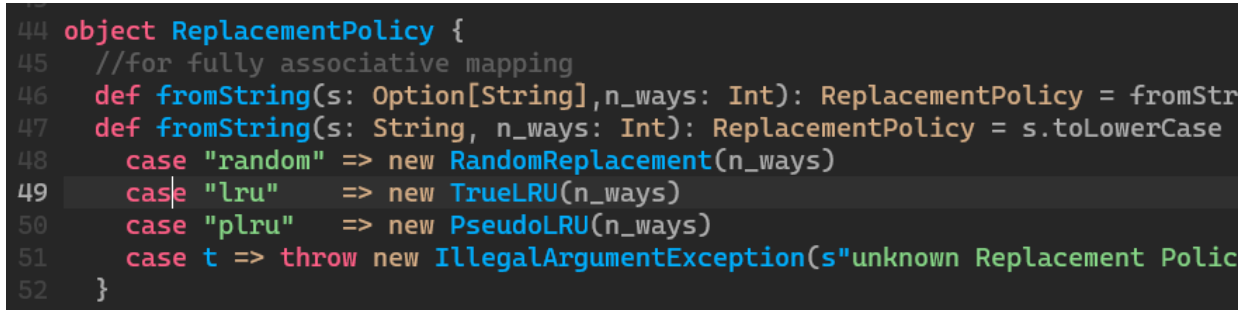
Hardware thinking

Advice you may need

`def` is not for object declaration

```
class RandomReplacement(n_ways: Int) extends
 ReplacementPolicy {
  //...
  def nBits = 16
  def perSet = false
  //..
```

```
  def ptwl2replacer = ReplacementPolicy.
fromString(Some("plru"))
  /*
     ...
   */
  ptwl2replacer.access(hitWay)
  val victimway = ptwl2replacer.way()
```



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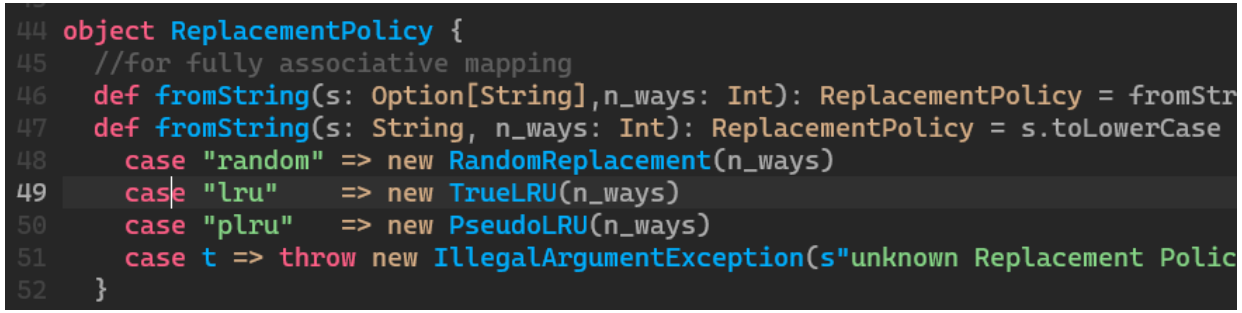

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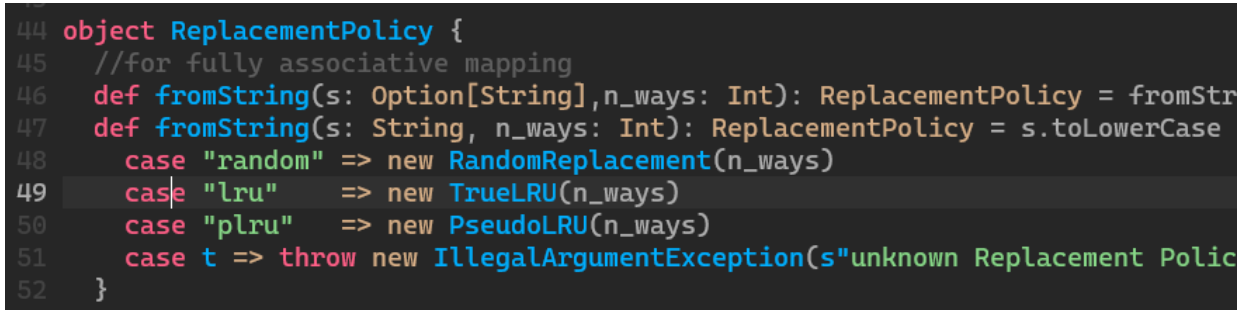

```
object ReplacementPolicy {
  //for fully associative mapping
  def fromString(s: Option[String],n_ways: Int): ReplacementPolicy = fromStr
  def fromString(s: String, n_ways: Int): ReplacementPolicy = s.toLowerCase
    case "random" => new RandomReplacement(n_ways)
    case "lru"    => new TrueLRU(n_ways)
    case "plru"   => new PseudoLRU(n_ways)
    case t => throw new IllegalArgumentException(s"unknown Replacement Polic
  }
```

Victim way will always be the first(way 0)

Advice: Use `def` to declare methods, and `val` to declare objects

Cat-map problem

```
// Is there an MSHR free for this request?
val mshr_validOH = Cat(mshrs.map(_.io.status.valid).reverse)
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Cat with no reverse

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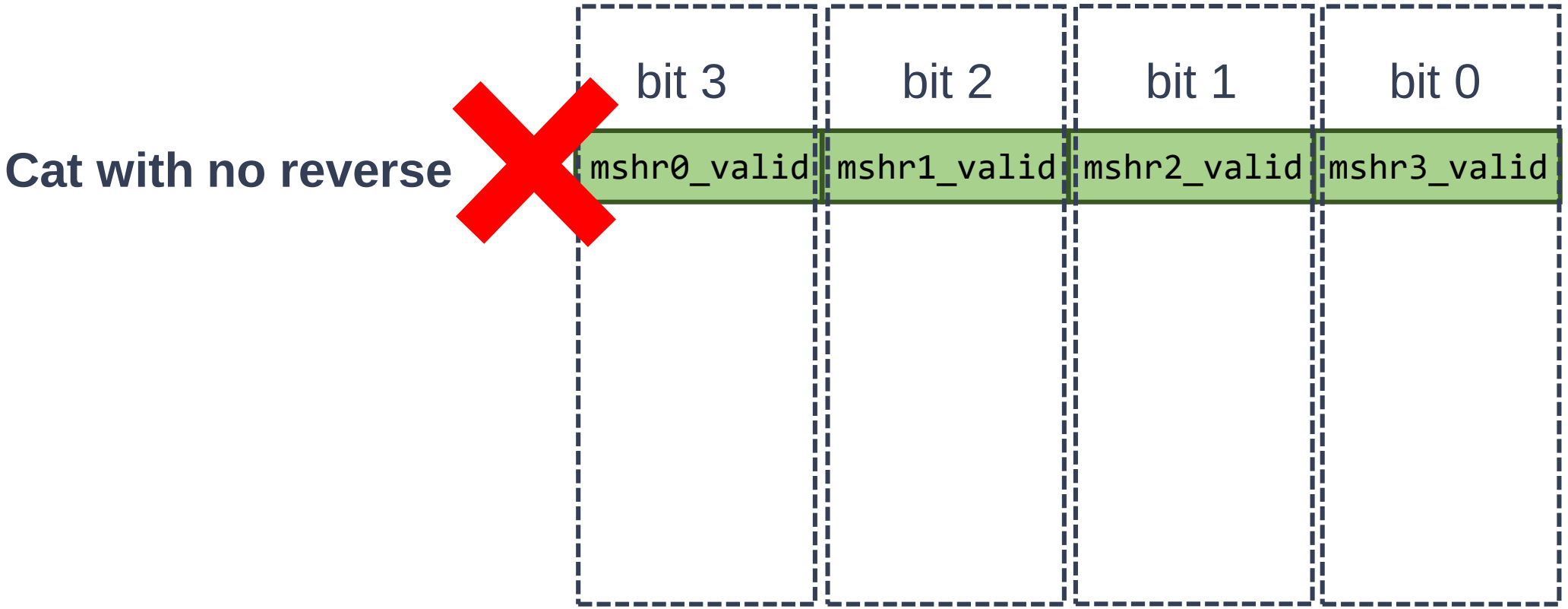

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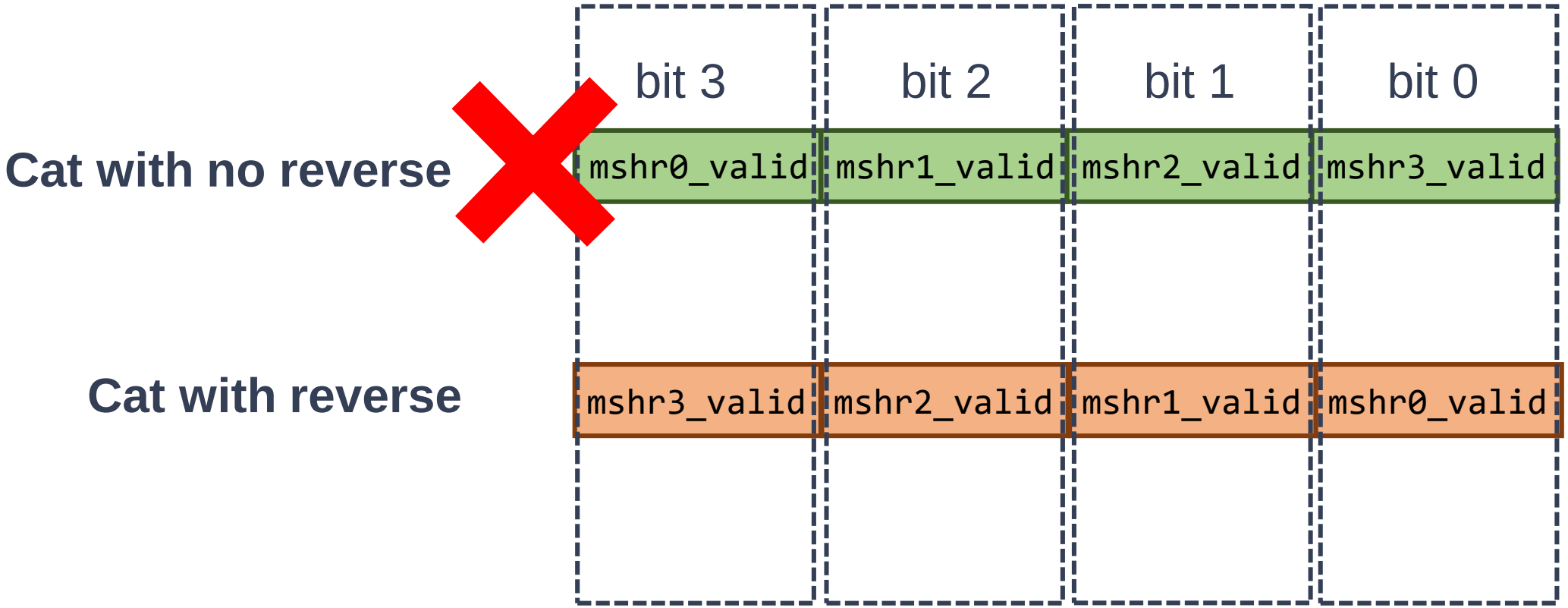

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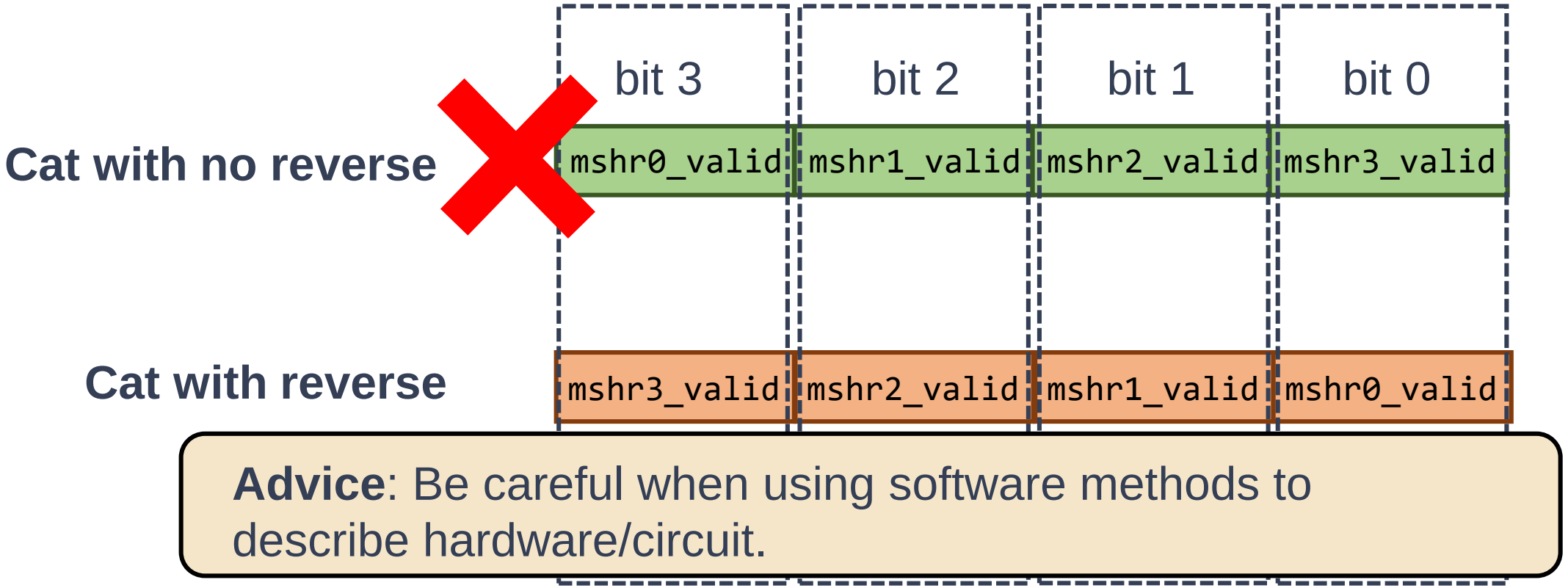
Cat → Hardware thinking

map → Software thinking



Advice: Be careful when using software methods to describe hardware/circuit.

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wire [255:0] _T_2 = validArray >> _T_1; //
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Advice: In `Cat` operation, you must specify the bit width for the immediate value of `UInt` type

Width! Width! Width!

Perhaps we need some syntactic salt?

```
[warn] value 'w.U' in Cat has
no width information!
```

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Advice: In `Cat` operation, it is recommended to specify the bit width for the immediate value of `UInt` type

Care about your `DontCare`

```
val bundleA <> DontCare
// lots of code
bundleA.signal1 := true.B
bundleA.signal2 := 1.U
bundleA.signal4 := 2.U
//...
bundleA.signalx := 3.U
// bundleA.signal3 is set to false.B

//forget...
when(bundleA.signal1 && bundleA.signal3){
  //...
}
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Perhaps we need some syntactic salt?

```
[warn]signal3 in bundleA has been used but was connected to DontCare
```

Advice: Do not use `DontCare` for make a temporary assignment to a bundle.

Competitive assignment

Defination: Reassignment of the same variable (a wire/register) in the same cycle

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In an implicit competition assignment, f(x) is not a one-to-one function, that is, f(x1) = f(x2) but x1 != x2.

Competitive assignment

```
//exu write back, update some info
for((wb,i) <- io.exuWriteback.zipWithIndex) {
    val wbIdx = wb.bits.redirect.ftqIdx.value
    // ...
    when(cfiUPdate.taken && offset < cfiIndex_vec(wbIdx).bits){
        cfiIndex_vec(wbIdx).valid := true.B
        cfiIndex_vec(wbIdx).bits  := offset
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```
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Advice: Ensure that your assignment in the loop will not cause implicit competitive assignment.

3. A developer’s perspective for Chisel

- Excellent HDL
- A lot of syntactic sugar
- Free developers from dirty work
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- Some software thinking may cause problems
- Be familiar to Scala before using Chisel
- Ensure that the hardware (verilog) is consistent with what you wrote with Chisel

Summary

Advice: Use `def` to declare methods, and `val` to declare constants or objects

Advice: Be careful when using software methods to describe hardware/circuit.

Advice: In `Cat` operation, it is recommended to specify the bit width for the immediate value of `UInt` type

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THANKS!

Q & A