



北京开源芯片研究院  
BEIJING INSTITUTE OF OPEN SOURCE CHIP

# 香山服务器IP当前状态和路线图

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2024-08-22

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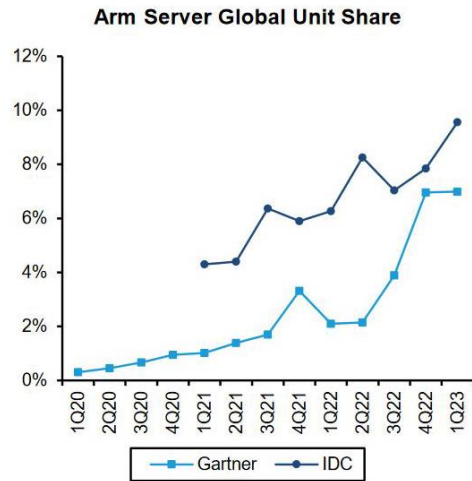
# 为什么要做服务器芯片IP

# 市场及产品价值：服务器市场潜力大

	2020	2021	2022	2023	2024	2025	2026	2027
Non-X86 Servers	<b>\$8,848 M</b>	\$9,239 M	\$12,269 M	\$14,984 M	\$16,240 M	\$18,208 M	\$20,256 M	\$23,571 M
Growth	-	4.4%	32.8%	22.1%	8.4%	12.1%	11.2%	16.4%
X86 Servers	<b>\$85,281 M</b>	\$93,396 M	\$110,955 M	\$113,487 M	\$127,407 M	\$140,120 M	\$153,483 M	\$165,568 M
Growth	-	9.5%	18.8%	2.3%	12.3%	10.0%	9.5%	7.9%
Total	\$94,130 M	\$102,601 M	\$123,224 M	\$128,471 M	\$143,647 M	\$158,328 M	\$173,739 M	\$189,139 M
Total Growth	-	9.0%	20.1%	4.3%	11.8%	10.2%	9.7%	8.9%

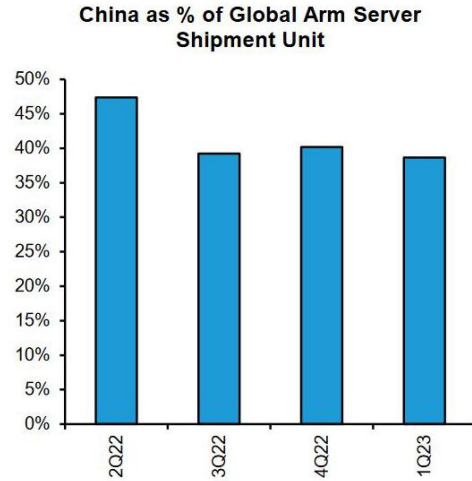
<https://gigalight.medium.com/global-ai-server-market-surges-to-50-billion-in-2023-expected-to-exceed-50-share-by-2027-cb5ec8de5ed9>

EXHIBIT 4: Estimates from market researchers differ but the rise of Arm CPU in servers is clear and consistent.

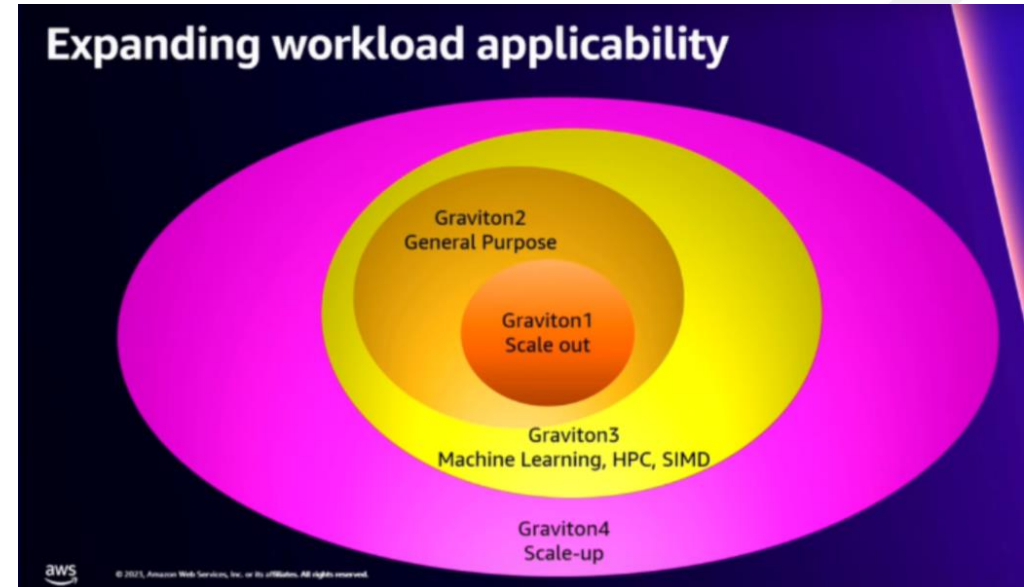


Source: Gartner, IDC and Bernstein analysis

EXHIBIT 5: We estimate nearly 10% of servers now have Arm CPUs, with roughly 40% used by China.



Source: Gartner, Bernstein analysis



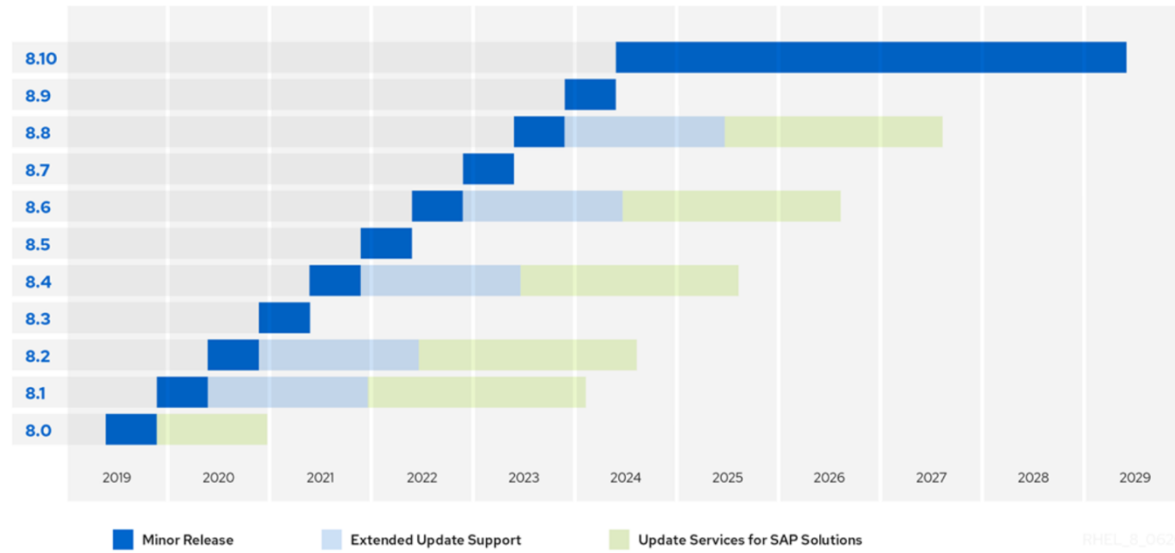
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<https://www.tomshardware.com/news/china-arm-servers>

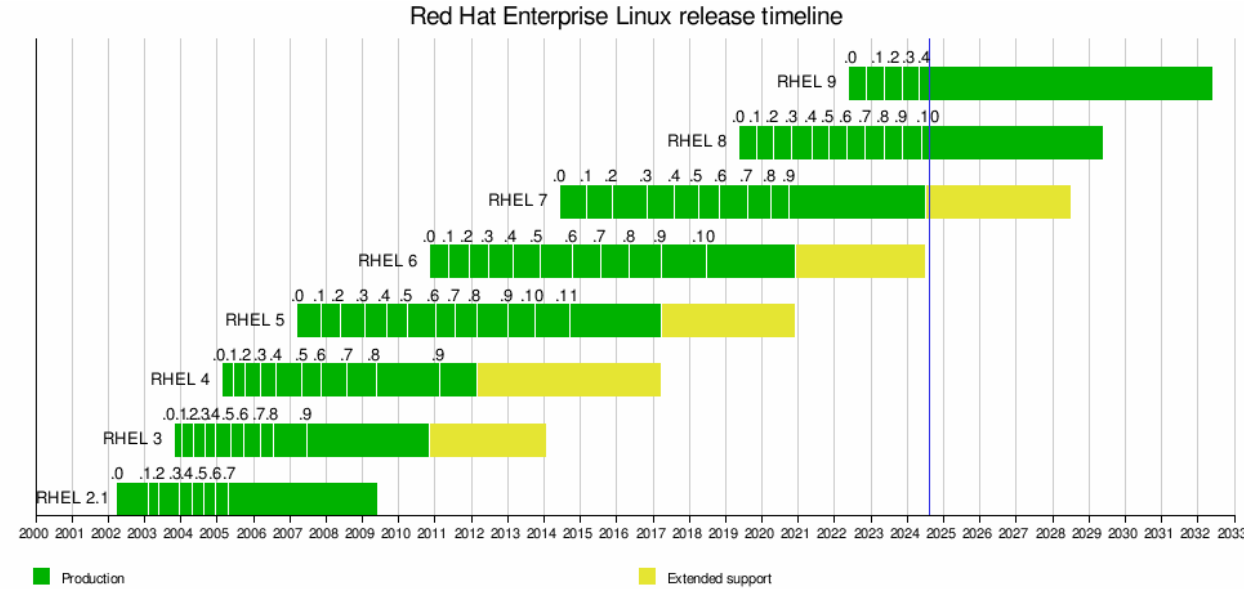
AWS re:invent

# 服务器场景适合开源项目发展

RHEL 8 Planning Guide<sup>viii</sup>



<https://access.redhat.com/support/policy/updates/errata>

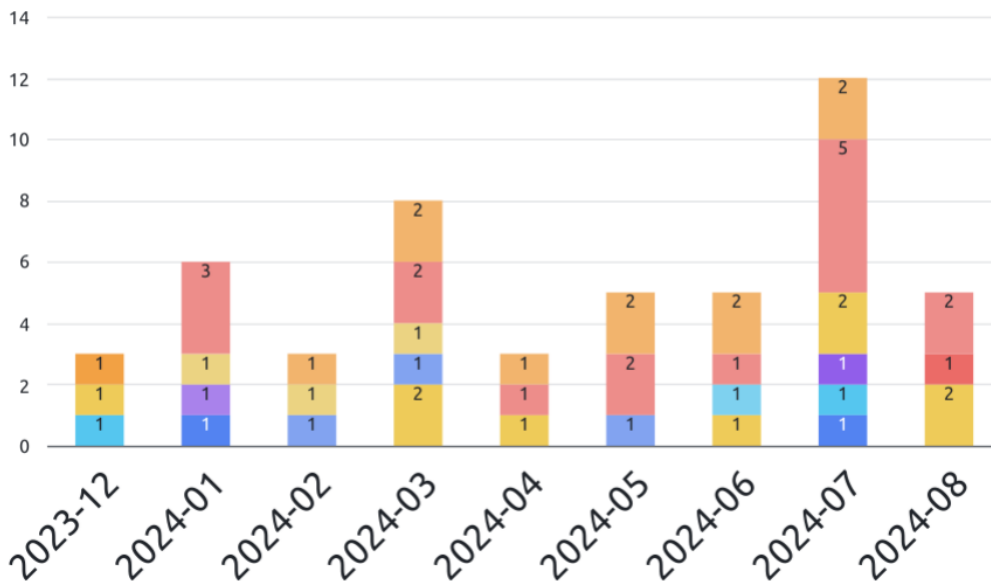
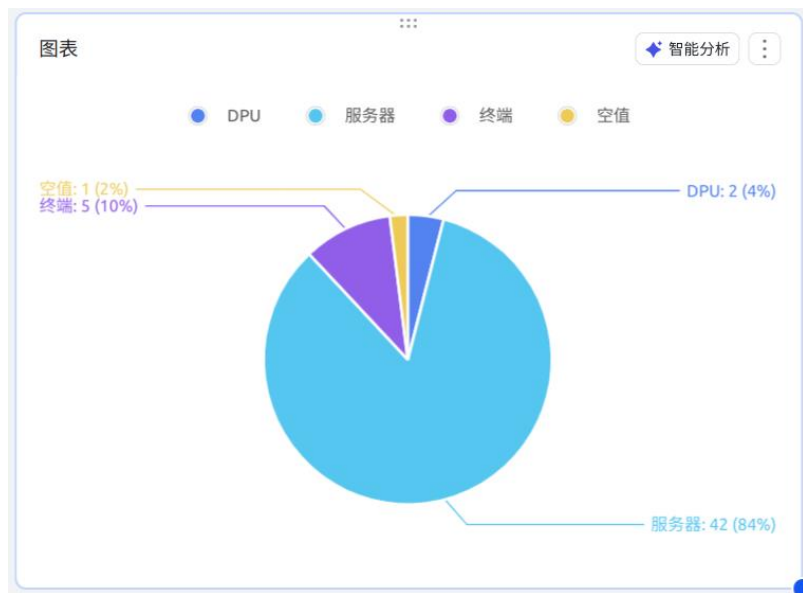


**10年支持周期，一直使用同一个内核**  
**Kernel version: 4.18**  
**release: 2018.8.12**

**内核大版本3年一次升级**  
**RHEL 8: 2019**  
**RHEL 9: 2022**

# 会员很需要服务器CPU IP

大部分(84%)是服务器场景



图一：会员交流统计

表一：会员交付目标

会员单位	场景	交付版本	CPU CHI版本	RVI规范	产品形态
A	服务器	XS-K V2	Issue E.b	RVA23必选; server SOC spec (部分)	多die多socket
B	服务器	XS-K V2	Issue E.b	RVA23必选; server SOC spec (部分)	多die多socket
C	服务器	XS-K V2	Issue B	RVA23必选; server SOC spec (部分)	多die多socket
D	终端	XS-K V2	Issue E.b	RVA23必选;	单die
...	...	...	...	...	...

服务器客户交付更明确



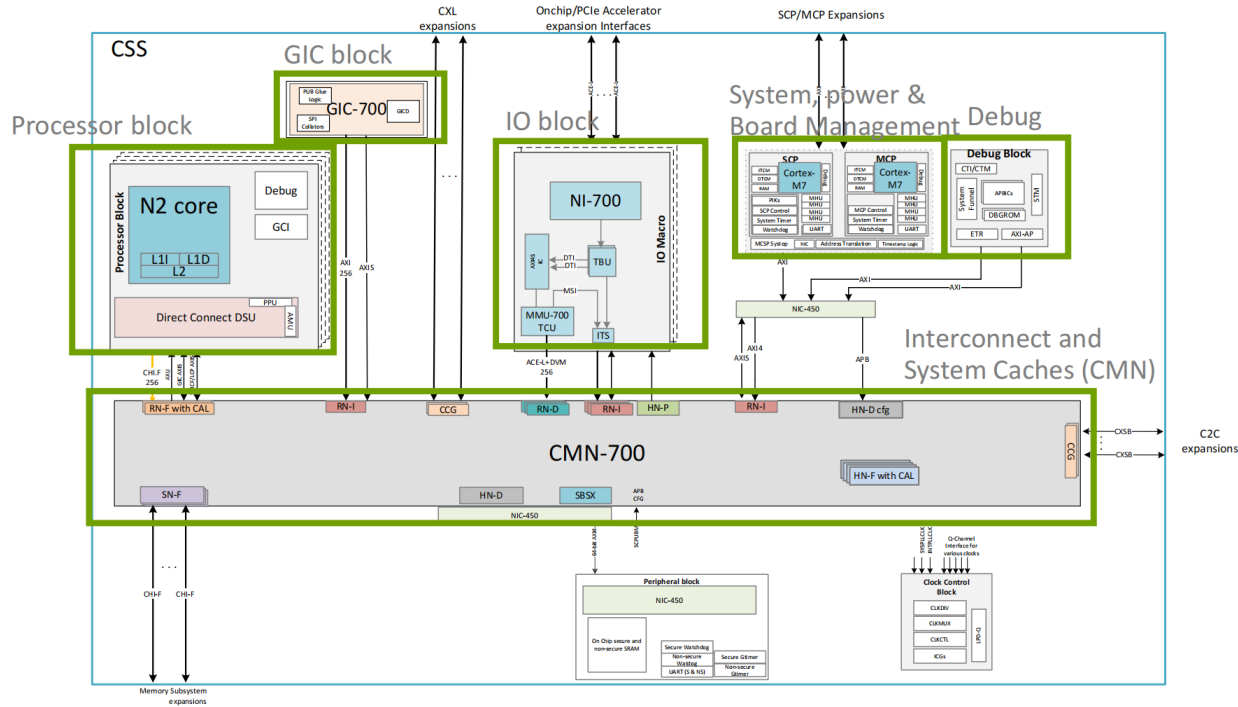
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# 需要哪些服务器芯片IP



# ARM服务器IP生态

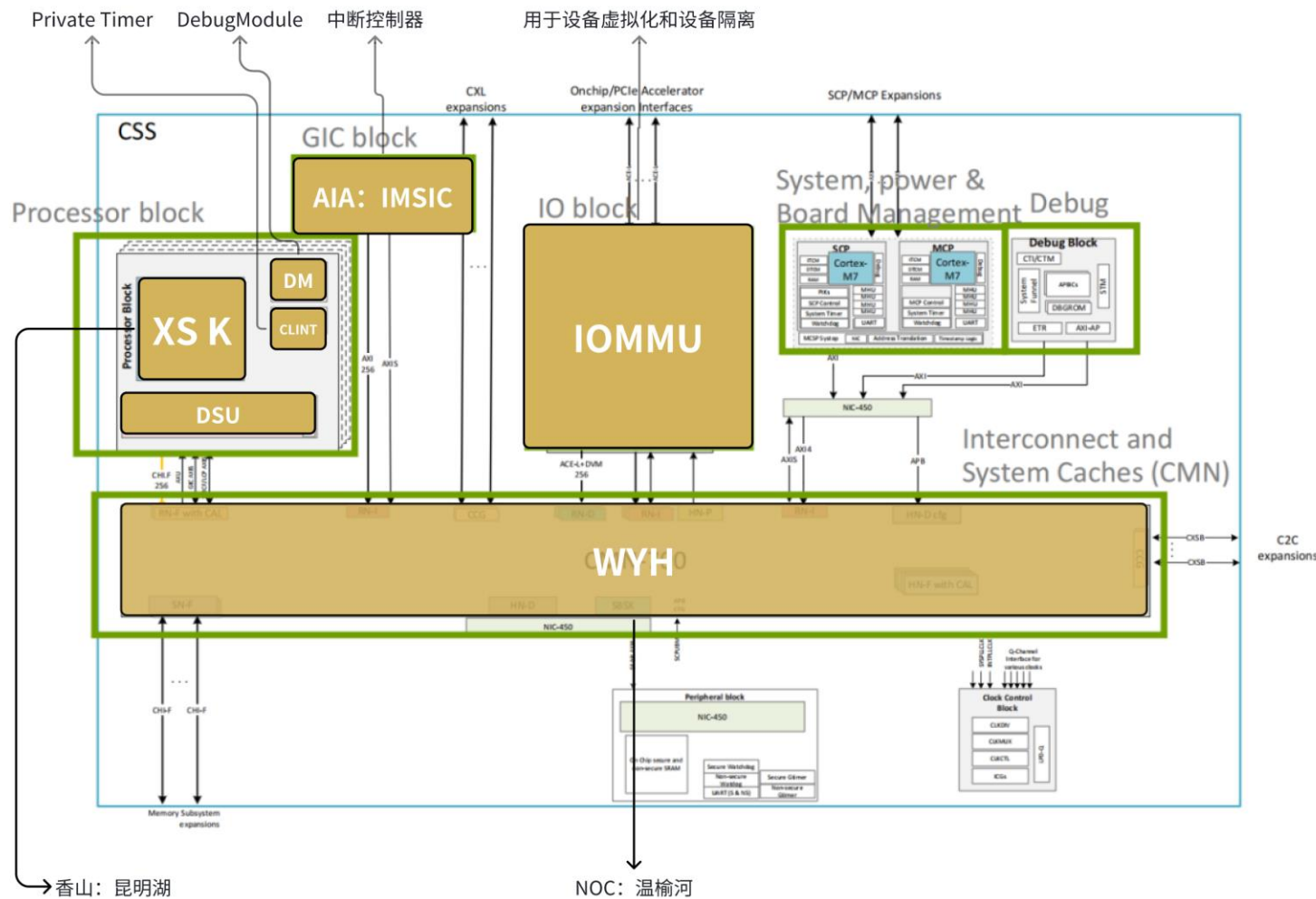


RD-N2 complies with, or includes components that comply with, the following specifications:

- Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile
- Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3 and version 4
- AMBA® 5 CHI Architecture Specification, issue E
- Arm® Server Base System Architecture, version 6.0
- AMBA® AXI and ACE Protocol Specification
- Arm® System Memory Management Unit Architecture Specification, SMMU architecture version 3
- Arm® CoreSight™ Base System Architecture, version 1.0
- Arm® Power Policy Unit Architecture Specification, version 1.1
- Arm® Power Control System Architecture, version 2.0
- Arm® Debug Interface Architecture Specification ADIv6.0



# 开芯院IP生态



## 相关上游规范

- RISC-V server platform specification
  - RVA profile
  - RISC-V server SOC specification
  - **B**oot and **R**untime **S**ervices specification
  - RISC-V platform security model
- Certification (Certification Steering Committee)



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# 香山当前状态

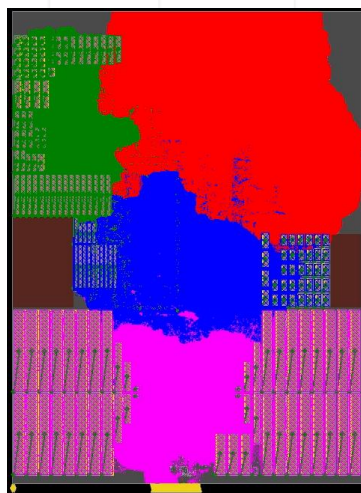
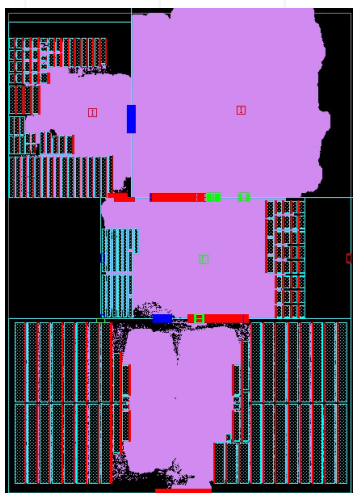


# 昆明湖已经完成的工作 (V1)

项目 Kunminghu 模块 Partition 版本 20240118-v01...

历史 \*最多选择5个

bucket	WNS	TNS	level	buf/inv	skew	rc	delta	pathgroup
740	-0.047	-0.095	19	8	0.028	0.052	0.007	frontend_backend
2	-0.040	-3.306	22	3	-0.062	0.027	0.000	backend_memblock
718	-0.040	-13.265	15	2	-0.030	0.028	0.000	backend_memblock
11	-0.040	-4.353	24	5	-0.055	0.041	0.003	backend_memblock
1	-0.037	-1.951	30	6	0.000	0.066	0.005	memblock_backend
31	-0.033	-2.807	24	13	0.003	0.124	0.023	backend_backend



- ❑ N7工艺, TT0P85V85C, 11层METAL; OCV, clock derate 1.05/0.95, uncertainty 20ps
- ❑ Floorplan: 1500um\*1840um, density=~60%
- ❑ 结论: TT0P9V85C下, 各个模块内部和端口已达3GHz

SPECint 2006 @ 3GHz		SPECfp 2006 @ 3GHz	
400.perlbench	36.65	410.bwaves	55.37
401.bzip2	24.28	416.gamess	43.77
403.gcc	47.69	433.milc	35.82
429.mcf	57.85	434.zeusmp	44.43
445.gobmk	31.71	435.gromacs	30.39
456.hmmer	39.57	436.cactusADM	46.22
458.sjeng	31.50	437.leslie3d	39.51
462.libquantum	125.49	444.namd	37.45
464.h264ref	57.38	447.deall	73.55
471.omnetpp	42.24	450.soplex	55.74
473.astar	30.74	453.povray	55.86
483.xalancbmk	75.54	454.Calculix	16.49
<b>GEOMEAN</b>	<b>44.98</b>	459.GemsFDTD	34.22
基于程序片段的分数估计, 非完整SPEC06评估, 和真实芯片实际性能有偏差		465.tonto	34.24
		470.lbm	85.61
		481.wrf	39.58
		482.sphinx3	57.07
		<b>GEOMEAN</b>	<b>43.39</b>

单核SPECint2006得分 14.99/GHz

# 昆明湖已经完成的工作（续）

## V2R1

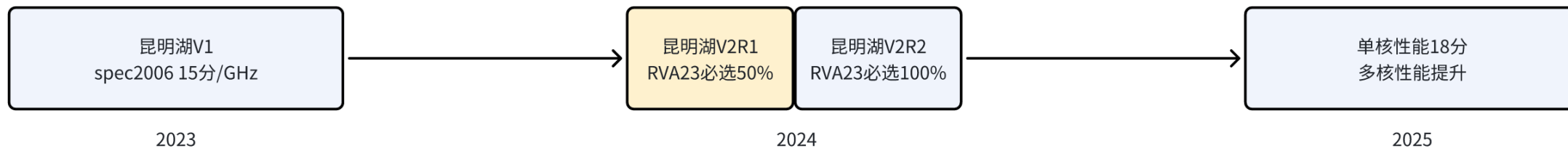
- **RVA23必选完善ing**
- **向量三次迭代获得性能正收益**
- **原生CHI改造，支持CHI Issue B子集**

## 持续推进香山开源发行版的发展

- **gem5**
- **NEMU**
- **开芯编译器**
- **固件和Linux发行版upstreaming**
- **xiangshan CPU IP**
- **uncore IP**
- **NOC IP**
- ...

Class	Transaction	Current Support
1 Read	ReadNoSnp	Yes
2 Read	ReadNotSharedDirty	Yes
3 Read	ReadUnique	Yes
4 Dataless	MakeUnique	Yes
5 Dataless	Evict	Yes
6 Write	WriteNoSnpPtl	Yes
7 Write	WriteNoSnpFull	Yes
8 Write	WriteBackFull	Yes
9 Snoop	SnpOnceFwd	Yes
10 Snoop	SnpOnce	Yes
11 Snoop	SnpStashUnique	Yes
12 Snoop	SnpStashShared	Yes
13 Snoop	SnpCleanFwd	Yes

14 Snoop	SnpClean	Yes
15 Snoop	SnpNotSharedDirtyFwd	Yes
16 Snoop	SnpNotSharedDirty	Yes
17 Snoop	SnpSharedFwd	Yes
18 Snoop	SnpShared	Yes
19 Snoop	SnpUniqueFwd	Yes
20 Snoop	SnpUnique	Yes
21 Snoop	SnpUniqueStash	Yes
22 Snoop	SnpCleanShared	Yes
23 Snoop	SnpCleanInvalid	Yes
24 Snoop	SnpMakeInvalid	Yes
25 Snoop	SnpMakeInvalidStash	Yes
26 Snoop	SnpDVMOp	Yes



# 单核性能满足需求，多核差距很大

1	feature	Neoverse N2 CSS	XS-KMH V2R1(2024/06)
2	spec2006(GHz)	15	<b>15</b>
3	Address space	VA 48bit, PA 48bit	<b>VA39bit, PA 36bit</b>
4	memory region	find-grained	<b>coarse-grained</b>
5	outstanding transaction	memory, uncache memory, MMIO	<b>memory</b>
6	Time keeping	private timer(with global timestamp)	<b>global timer</b>
7	NMI	Yes	<b>No</b>
8	vector	NEON/SVE/SVE2	<b>V</b>
9	Performance monitor	Yes	<b>Yes</b>
10	Trace	Yes	<b>No</b>
11	CPU virtualization	CPU, memory	<b>CPU, memory(performance?)</b>
12	Interrupt virtualization	GIC	<b>AIA csr and IMSIC(UT finish)</b>
13	misalignment access	Yes	<b>No</b>
14	cache maintenance	Yes	<b>No</b>
15	Atomic	L1\$, L2\$, SLC with cas	<b>Only D\$ lrsc</b>

1	feature	Neoverse N2 CSS	XS-KMH V2R1(2024/06)
16	CPU interface	CHI Issue E.b	<b>CHI Issue B(subset)</b>
17	power	retention, power down	<b>gating</b>
18	nr of cores	up to 128	<b>up to 4</b>
19	CPU subsystem	Yes	<b>NO(Yes for tilelink)</b>
20	RAS	I\$ parity, D\$ ECC, L2\$ ECC	<b>I\$ parity, D\$ ECC(Default OFF)</b>
21	IOMMU	Yes(SMMU)	<b>open source(note1)</b>
22	HW page table A/D update	Yes	<b>No</b>
23	multi-channel ddr	Yes	<b>No</b>
24	memory interleave	Yes	<b>No</b>
25	multi-channel PCIe	Yes	<b>No</b>
26	Die2Die support	Yes	<b>No</b>
27	memory tag	Yes(MTE, PAC)	<b>No</b>
28	cache partition and monitor	Yes(MPAM)	<b>No</b>

V2R2主要解决服务器和嵌入式公共特性，与嵌入式场景的差异

- 36位VA，PA；
- 核数量少；
- 不需要跨die。

服务器基本功能	(服务器基本功能: 内部计划, 不对外承诺)
服务器公共能力	note1: poor performance, lack functionality
服务器高级特性	

下一代需满足32核以上服务器需求

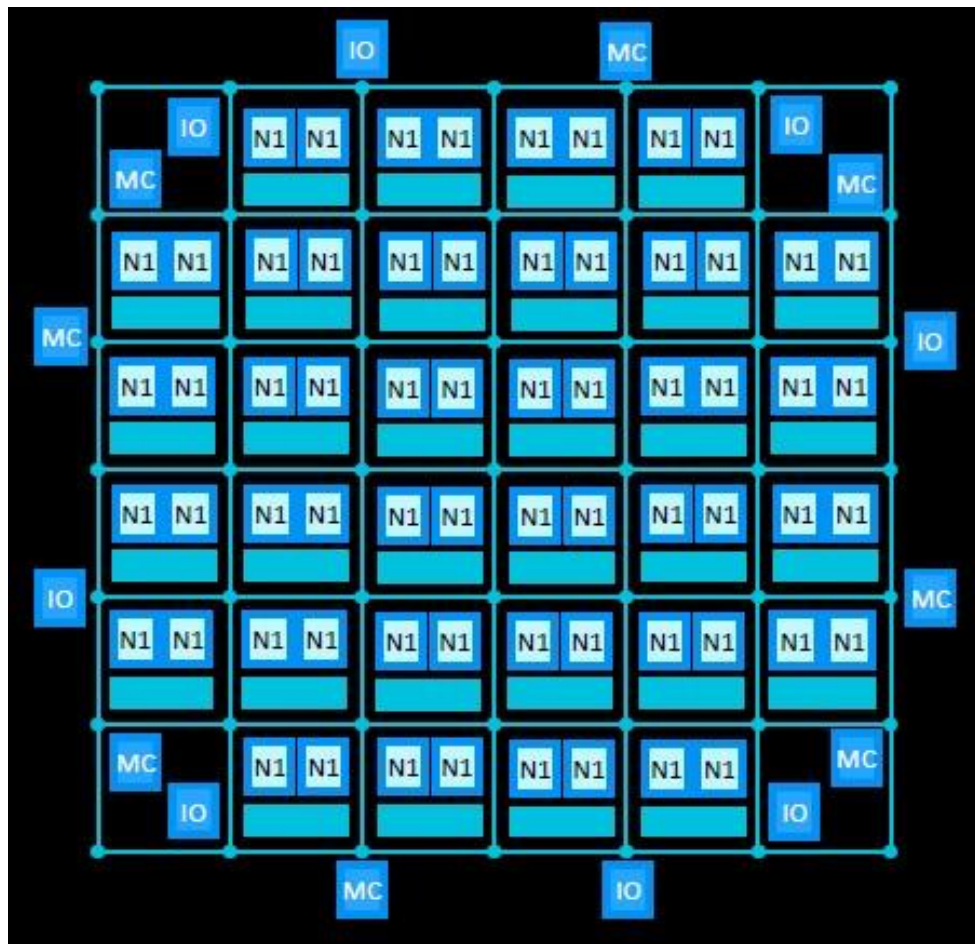


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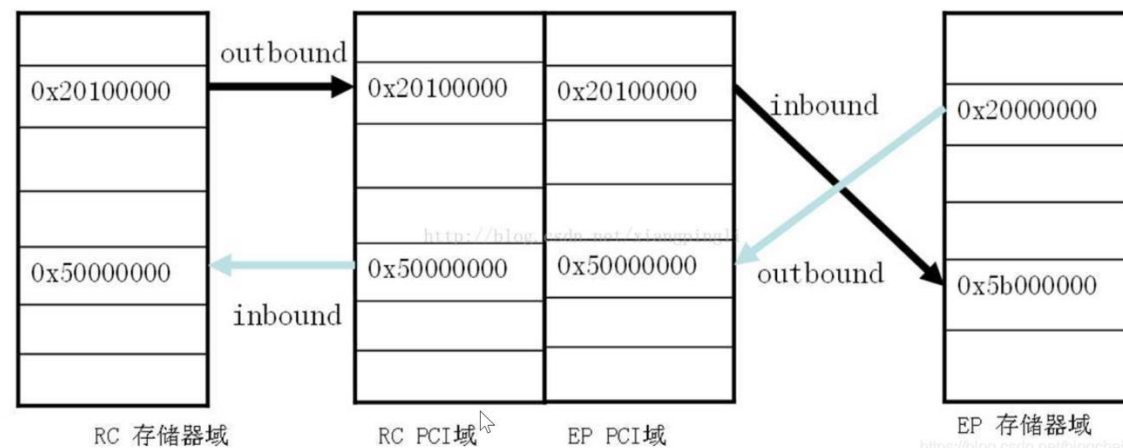
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# 香山要怎么支持服务器生态

# 支持多核，多PCIe，多通道MC

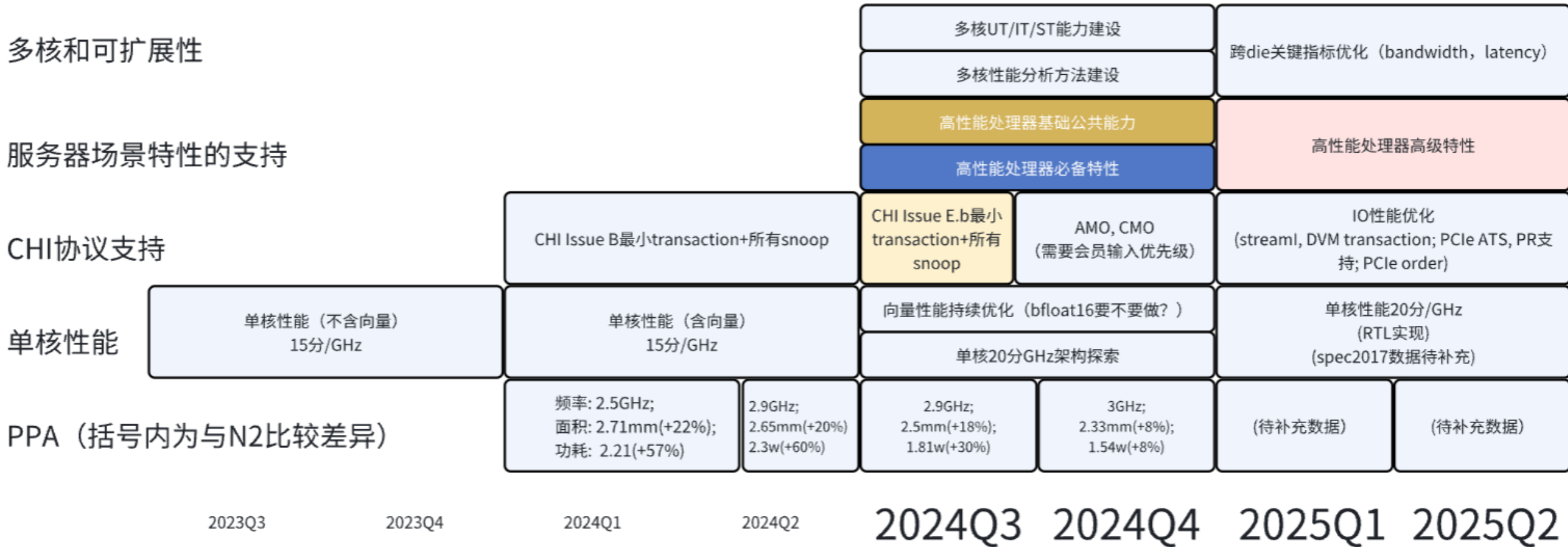


- 满足多核可扩展性
- 满足CPU与多PCIe的双向数据传输
- 配合多通道memory做优化
- 性能建模
- ...



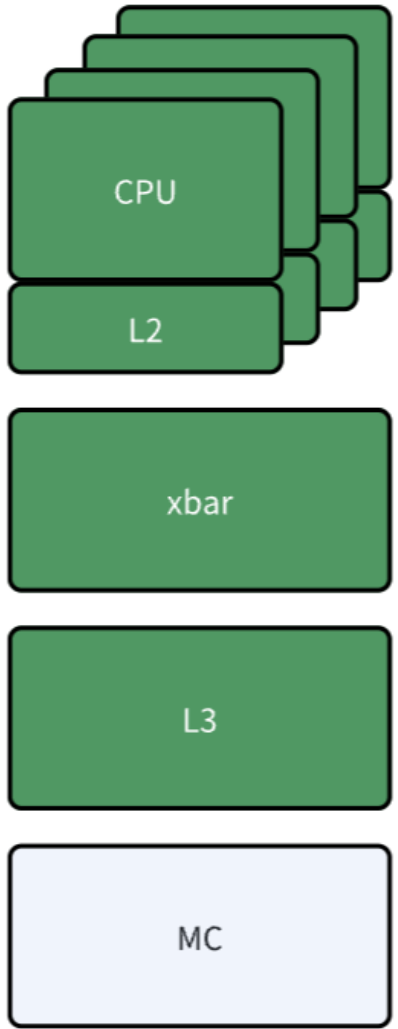
# 一年时间完成对服务器生态的支持

软件生态同步支持，参见明天openEuler同期活动。





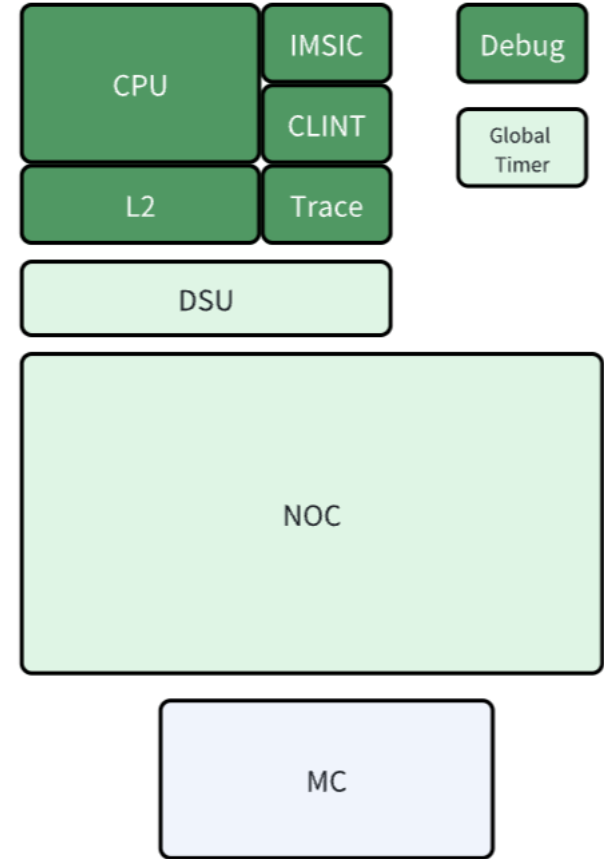
# 交付形态 (从4核到支持64核)



已有交付方式：  
CPU subsys交付

服务器场景，  
分四部分交付

- CPU subsystem
- DebugModule
- Global Timer
- NOC(依赖开芯院内部项目)



2024年提供  
2025年提供

- 暂不支持cluster。
- 2024年H2 多核验证支持4-8核
- NOC指WYH(温榆河)。竞合伙伴的商业IP不在交付范围之内。例如ARM CMN-600, CMN-700; 可以提供技术支持。
- DSU处于研发状态，2024Q3暂时无法提供。可以提供CHI, TL, AXI等接口的异步桥。

# Q3, Q4具体目标

1	feature	Neoverse N2 CSS	XS-KMH V2R1(2024/06)	Q3	Q4
2	spec2006(GHz)	15	<b>15</b>		
3	Address space	VA 48bit, PA 48bit	<b>VA39bit, PA 36bit</b>	<b>SV48, PA48</b>	
4	memory region	find-grained	<b>coarse-grained</b>	<b>Svpbmt</b>	
5	outstanding transaction	memory, uncache memory, MMIO	memory	Yes(lack MMIO OT)	<b>Yes</b>
6	Time keeping	private timer(with global timestamp)	<b>CLINT</b>	<b>CLINT, sstc</b>	
7	NMI	Yes	<b>No</b>	<b>Yes(ss1p13)</b>	
8	vector	NEON/SVE/SVE2	<b>V</b>		
9	Performance monitor	Yes	<b>Shcounterenw,Sscopmf,Sscounterenw,Zihpm</b>		
10	Debug	coresight debug	<b>Debug 0.13</b>		
11	Trace	Yes	<b>No</b>	<b>E-trace</b>	
12	CPU virtualization	CPU, memory	<b>H,Shgatpa. Shvsatpa. Shvstvecd (性能持续优化)</b>		
13	Interrupt virtualization	GIC	<b>AIA csr and IMSIC(UT finish)</b>		
14	misalignment access	Yes	<b>No</b>	Zicclsm(wo vector)	<b>Zicclsm(w vector)</b>
15	cache maintenance	Yes	<b>No</b>	<b>zicbom,zicboz,zicbop</b>	
16	Atomic	L1\$, L2\$, SLC with cas	<b>Only D\$ lrsc</b>	(Ziccamoa)	<b>Zacas, Ziccamoc</b>

服务器基本功能	(服务器基本功能: 内部计划, 不对外承诺)
服务器公共能力	note1: poor performance, lack functionality
服务器高级特性	

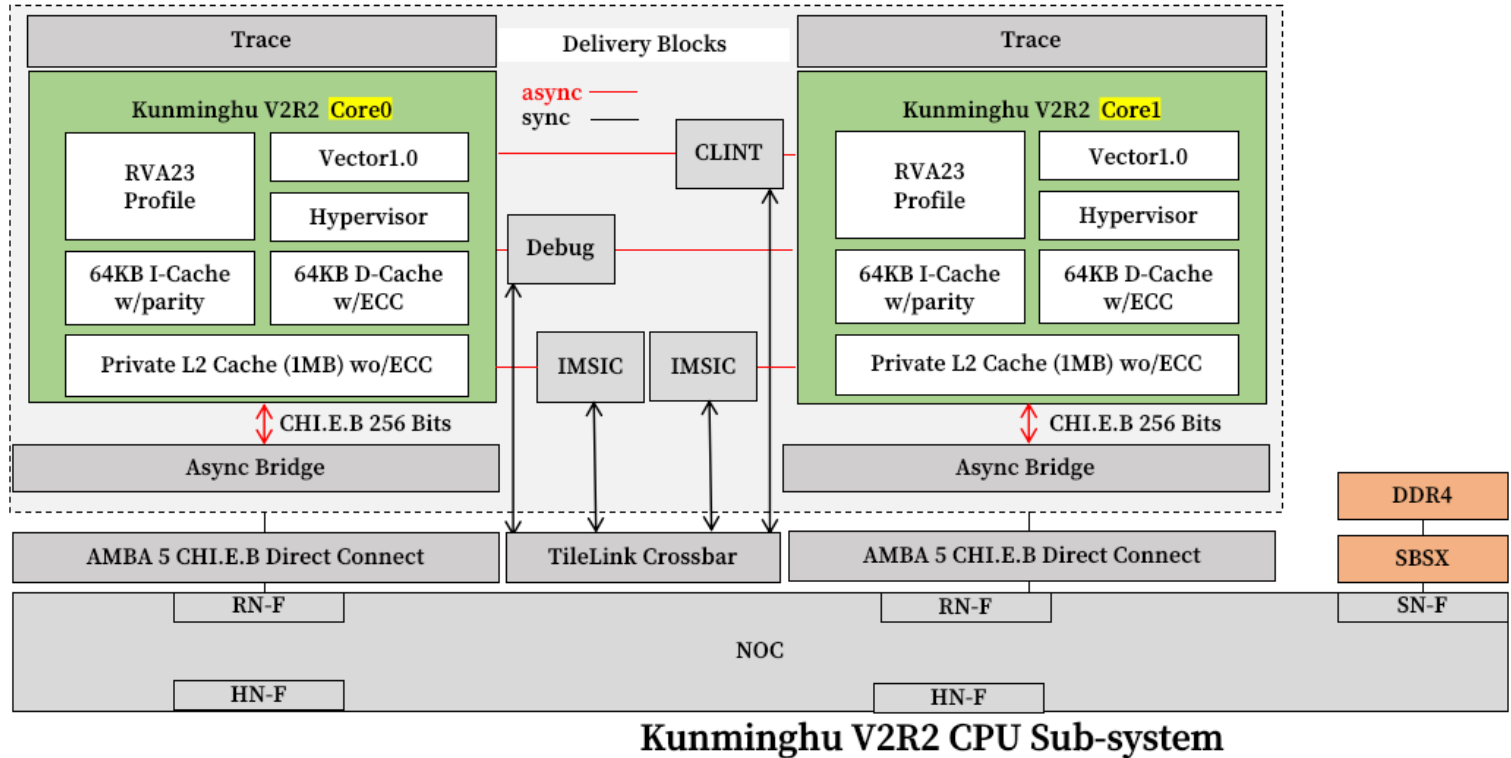
# Q3, Q4具体目标 (续)

	feature	Neoverse N2 CSS	XS-KMH V2R1(2024/06)	Q3	Q4
17	CPU interface	CHI Issue E.b	CHI Issue B(subset)	CHI Issue B&E.b(subset)	Yes(with AMO, CMO)
18	power	retention, power down	gating	retention?	Yes(maybe ARM P channel/Q channel)
19	HW page table A/D update	Yes	No		Yes(svadu)
20	nr of cores	up to 128	up to 2		Yes(up to 16)
21	CPU subsystem	Yes	NO(Yes for tilelink)		Yes
22	RAS	I\$ parity, D\$ ECC, L2\$ ECC	I\$ parity, D\$ ECC(Default OFF)	(I\$ parity + D\$ ECC on)	Yes
23	IOMMU	Yes(SMMU)	open source(note1)		Yes(wo PCIe)
24	DFT&MBIST	Yes	No	Yes	
25	Security	Realm	No		机密虚拟机
26	multi-channel ddr	Yes	No		
27	memory interleave	Yes	No		
28	multi-channel PCIe	Yes	No		
29	Die2Die support	Yes	No		
30	memory tag	Yes(MTE, PAC)	No		
31	cache partition and monitor	Yes(MPAM)	No		

服务器基本功能	(服务器基本功能: 内部计划, 不对外承诺)
服务器公共能力	note1: poor performance, lack functionality
服务器高级特性	

# 昆明湖V2R2项目-交付Highlight

- **1个主IP** (右上图)
  - CPU Core
- **6个系统IP** (右上图)
  - CLINT
  - Debug
  - Trace
  - AsyncBridge
  - AIA
  - IOMMU
- **3套系统集成和系统原型验证** (右下图)
  - VCS
  - Palladium
  - FPGA
- **DI<=3**: 致命缺陷个数\*10+严重缺陷个数\*3+一般缺陷个数\*1+提示缺陷个数\*0.1



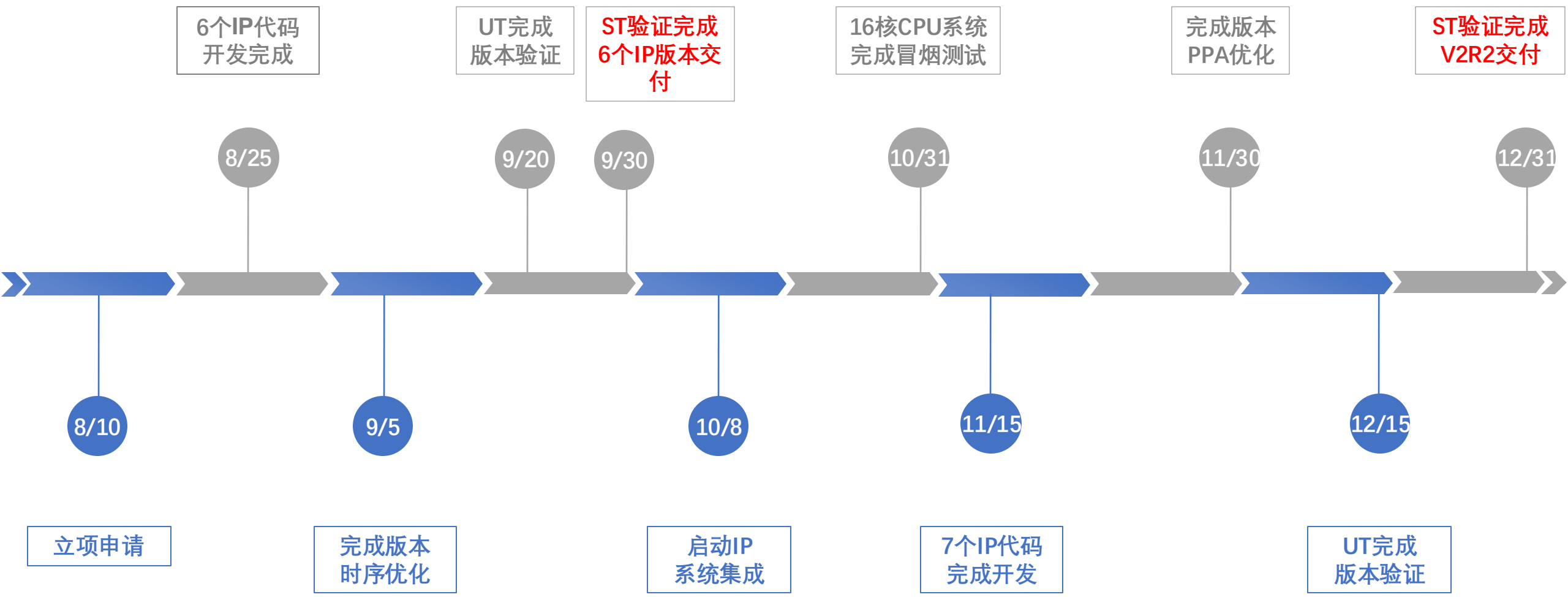
## 可扩展的工具流程 Extendable Tools Flow

- **Picker / MLVP / XCOMM**
- **Verilator / VCS / Xcelium Flow**
- **Xilinx FPGA flow**
- **Palladium Flow**
- **Coretools / Socrates / ...**

```
[majiyue@node001 build]$ make
GEN      Makefile
HOSTCC   scripts/basic/fixden
CC-VLOG  uvm_compile
CC-CLOG  ipcatalog/vip/memory_model/glbl.y.o
CC-VLOG  ipcatalog/vip/memory_model/ddr4_model.sv.o
GEN-IP   ipcatalog/vip/svt/options
CC-VLOG  ipcatalog/vip/svt/svt.uvm.pkg.o
GEN-IP   ipcatalog/darc/mc_2rank_cfg.f
...
GEN-BD   common/mcu/ddrc_init_mcu.bd
CC-VLOG  common/mcu/ddrc_init_mcu.bd.o
GEN-XCI  common/mcu/mc_clk_gen.xci
CC-VLOG  common/mcu/mc_clk_gen.xci.o
LD-LIB   common/mcu/mc_clk_gen/synopsys_sim.setup -> ./synopsys_sim.setup
ELAB     nanhu -> top=test_top_glbl
...
SYNTH    nanhu.synth.dcp -> top: fpga_top <INCREMENTAL>
IMPL     nanhu.impl.dcp <INCREMENTAL>
GEN-BIT  nanhu.bit
```

VCS UUM Flow
SNPS IP/VIP Flow
Xilinx IPI Flow
Xilinx FPGA Flow

# V2R2版本交付里程碑计划(2024年)



# RVA23全表

	A	B	C	D	E	F	G	H	I	J	K	L
1		Finished before 20240630					2024Q3		2024Q4	2025Q1	No plan	
2	RVA23 U mandatory	A	C	D	F	M	Zicclsm(scalar only)		Zicclsm	Zcb		
3		V	Zicntr	Zihpm	Ziccif	Ziccamo	Zicbom	Zvfhmin	Zawrs	Zihintntl		
4		Zba	Zbb	Zbs	Zic64b	Zicsr	Zicbop	Zfhmin	Zihintpause			
5		Zicboz	Zkt	Zicond	Za64rs		Zfa		Supm			
6		Ziccrse	Zcmop	Zvbb	Zvkt		Zimop					
7	RVA24 U mandatory								Zacas			
8									Ziccamoc			
9	RVA23 S mandatory	Zifencei	Svbare	Sv39	Svade	Ssccptr	Svpbmt		Ssnpm			
10		Svinval	H	Ss1p13	Sstvecd	Ssu64xl	Svnapot					
11		Sstvala	Shtvala	Shgatpa	Ssstateen	Sscofpmf	Sstc					
12		Shvstvecd	Shvsatpa	Shvstvala	Sscouterenw	Shcounterenw						
13	Server mandatory (RVA23 S optional)						Sv48	sv48x4	Svadu			
14	RVA23 U optional	zbc	Zvfh				Zama16b			Zfh	Zvksg	Zvkng
15											Zfbfmin	Zvfbfmin
16											Zvbc	Zvbfwma
17	RVA23 S optional	Sdext								Svptc	Sv57	Zkr
18											Ssstrict	



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Thanks

