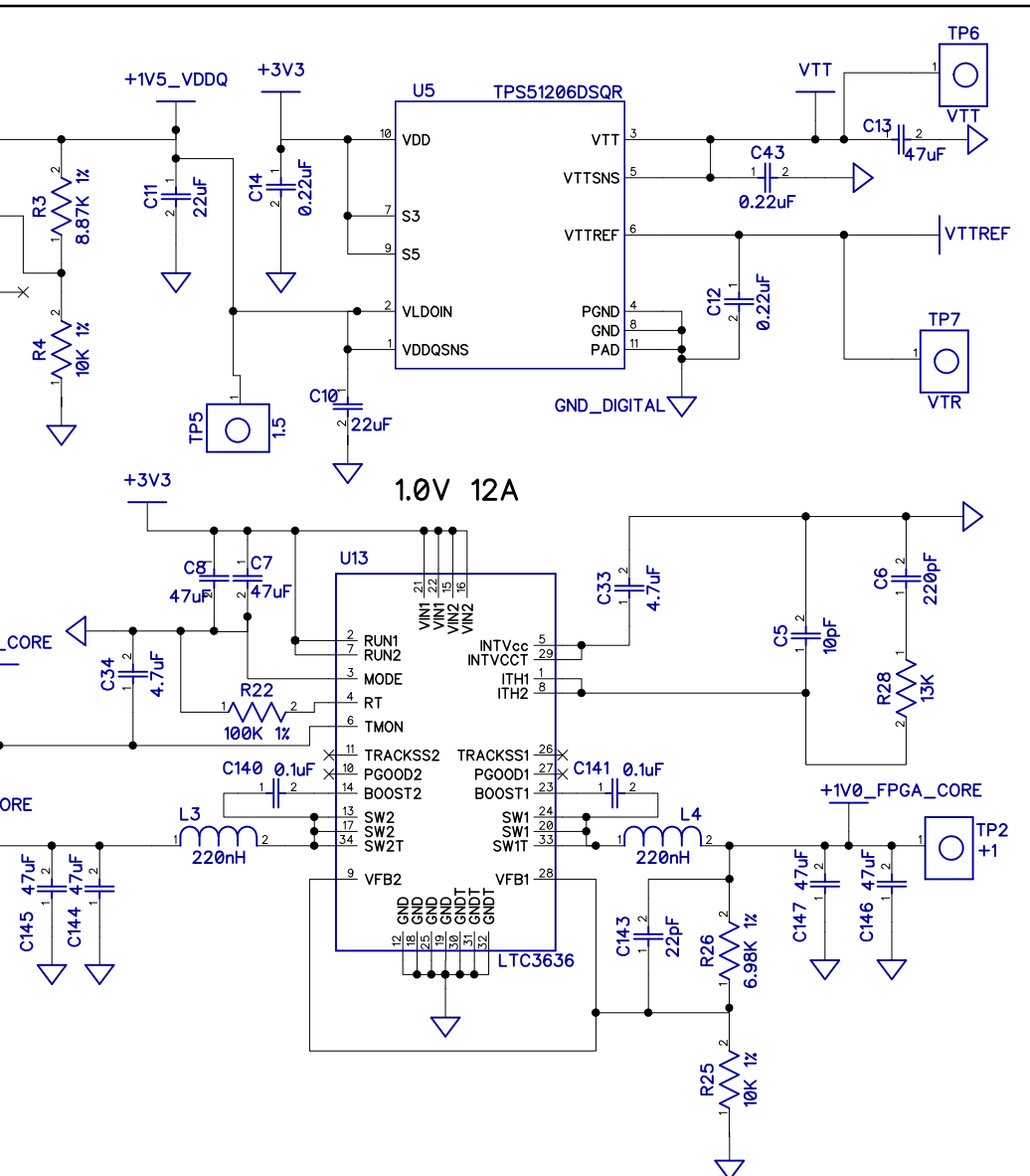
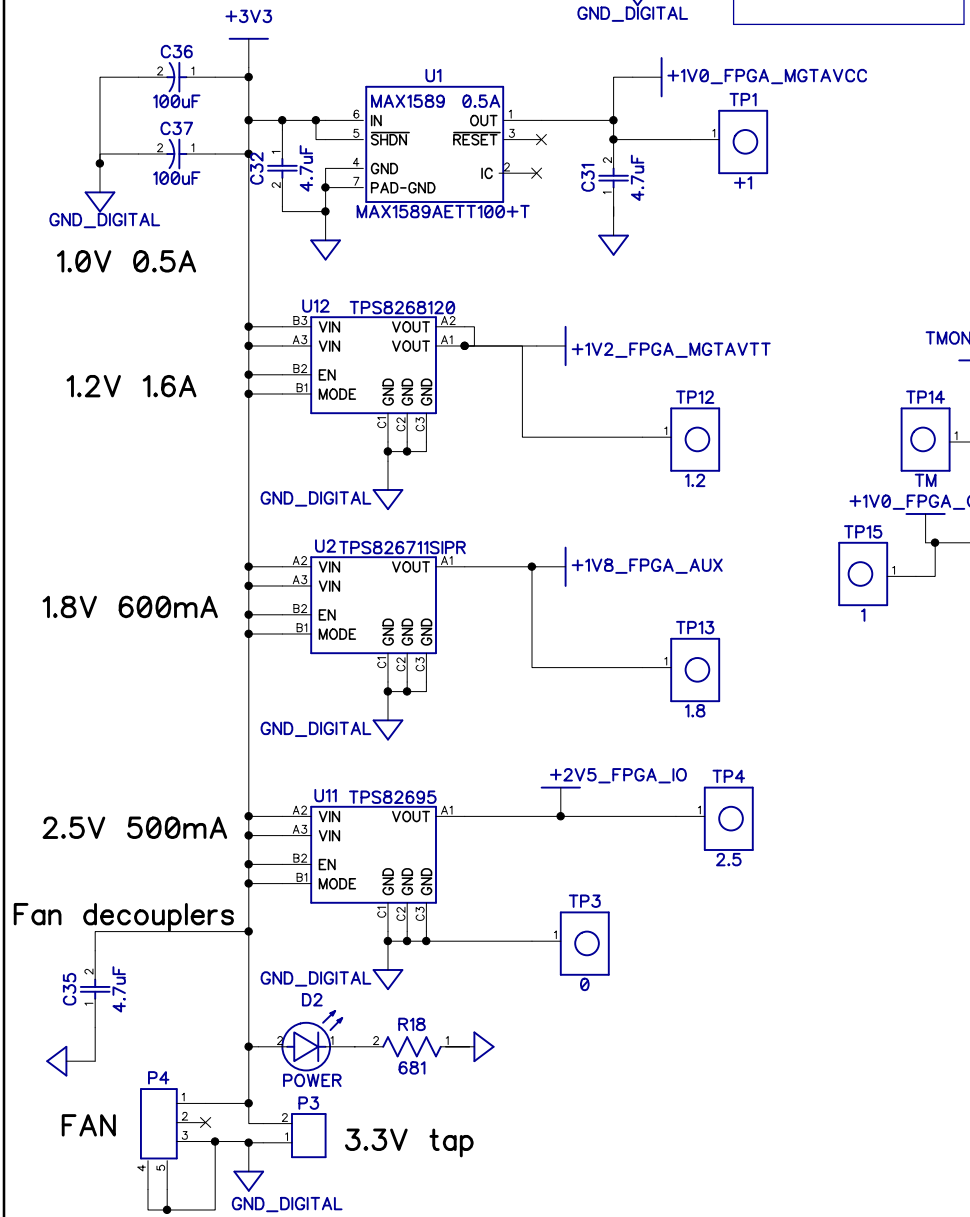


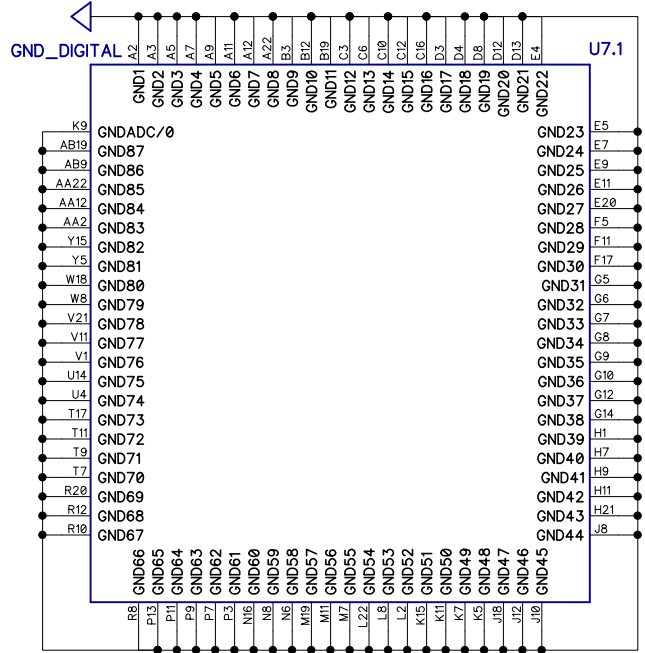
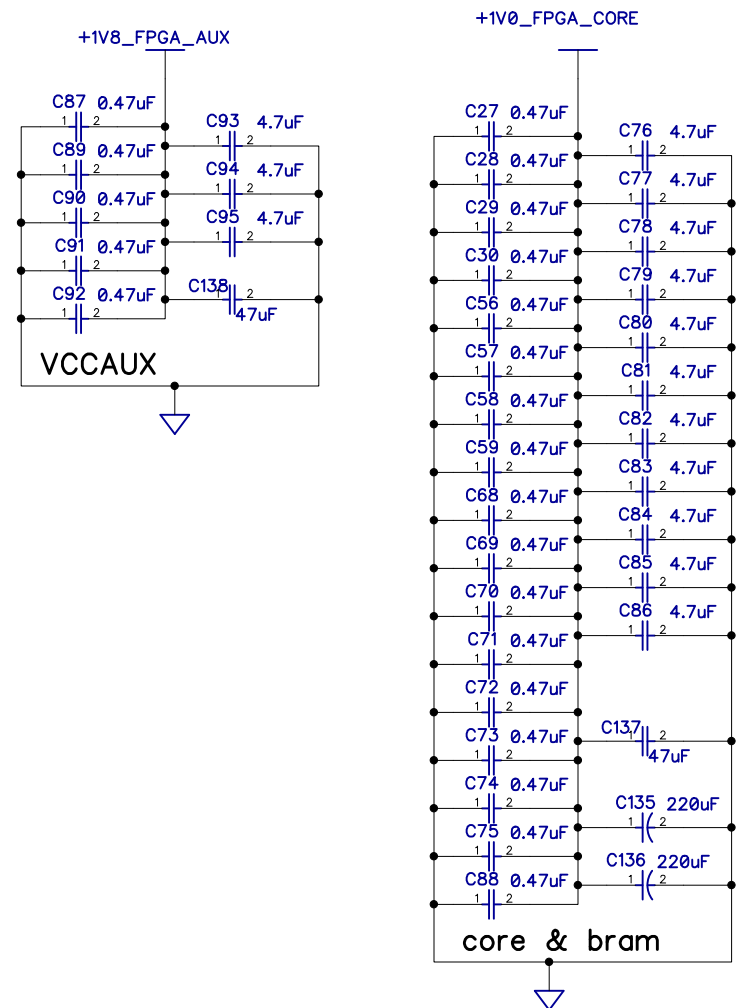
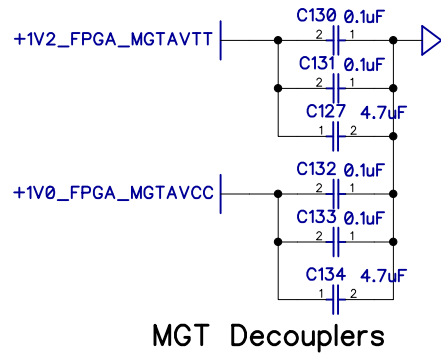
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Title Block Diagram		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

Voltage	Current	Purpose
+1.5	3A	DDR3 VDD
+0.75	1.5A	DDR VTT
+0.75	100mA	DDR VTT ref
+1.0	12A	FPGA core
+1.0	0.5A	MGT supply
+1.2	1A	MGT supply
+1.8	0.6A	FPGA Aux
+2.5	0.5A	LVDS I/O

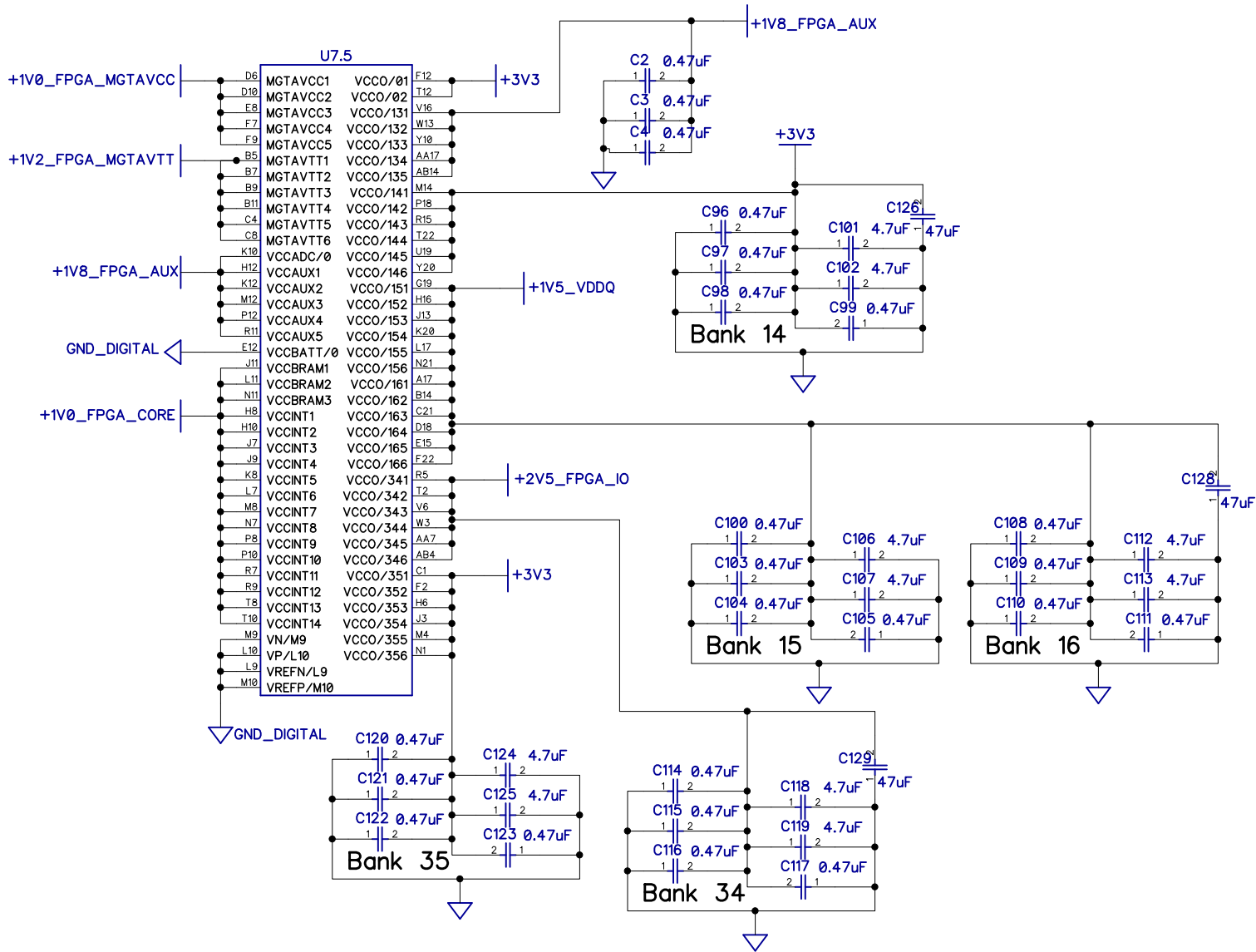


Title		Power	
Size	Number	Rev	
Date	Drawn by		
Filename	Sheet		



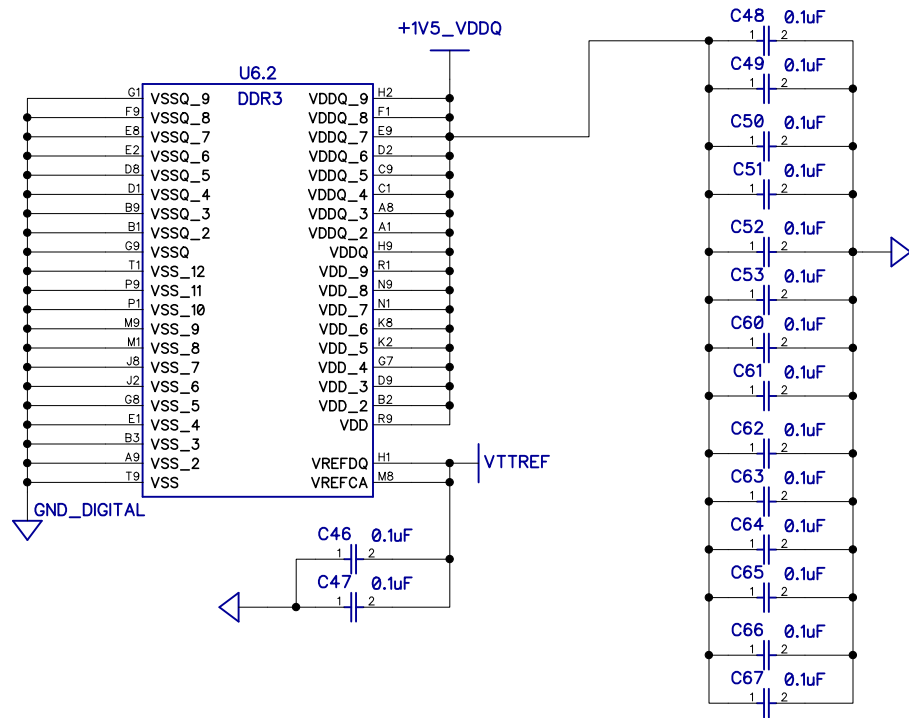
Bars	Value
0	
1 (A)	0.1uF
2 (B)	4.7uF
3 (C)	0.47uF

Title		
FPGA power and decoupling		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	

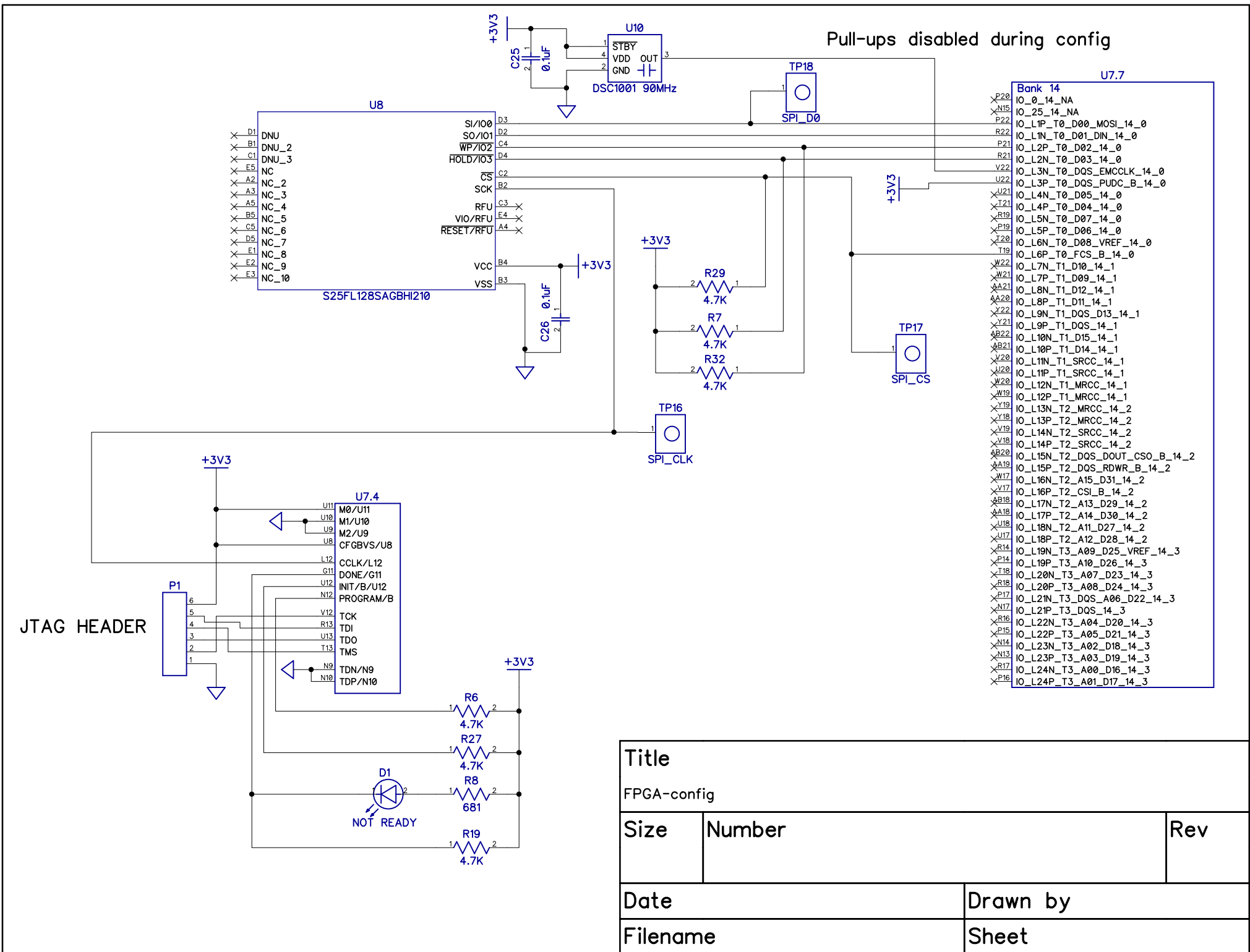


Bank	Voltage	Purpose
0	3.3	SPI, JTAG
13	3.3	Unused (NA on A50)
14	3.3	Config & 3.3V IO
15	1.5	DDR Addr/CTL
16	1.5	DDR data
34	2.5	LVDS I/O
35	3.3	3.3V I/O

Title		
FPGA I/O decoupling		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	



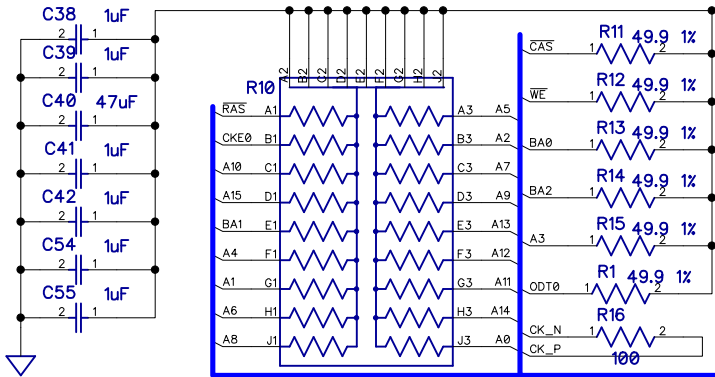
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DRAM Power and decoupling		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	



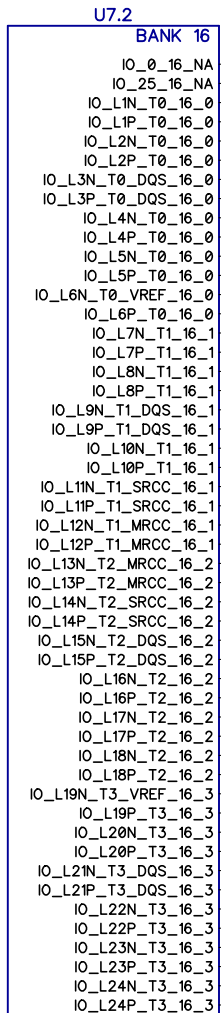
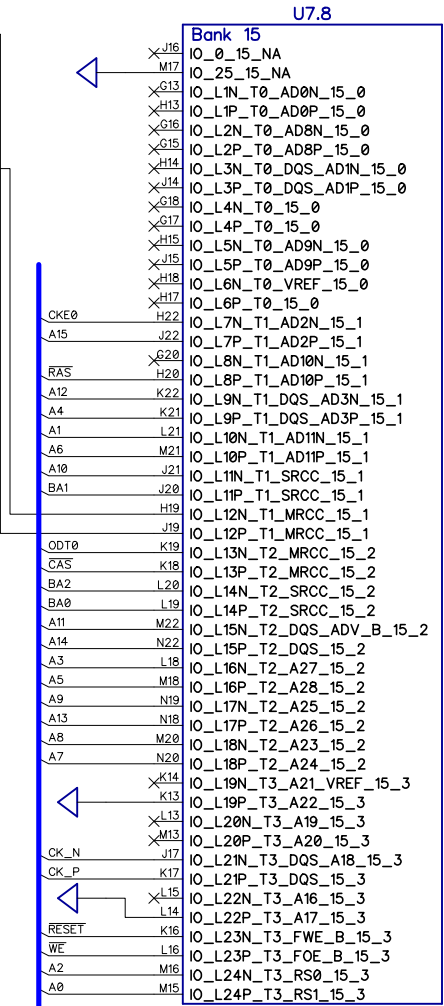
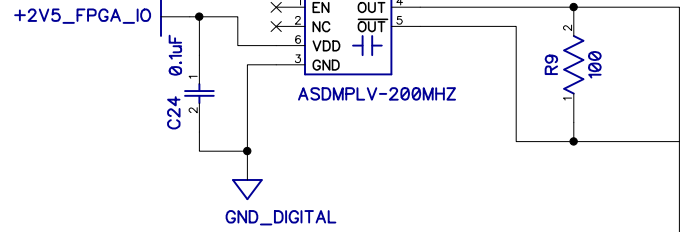
Title		
FPGA-config		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	

VTT Island decouplers

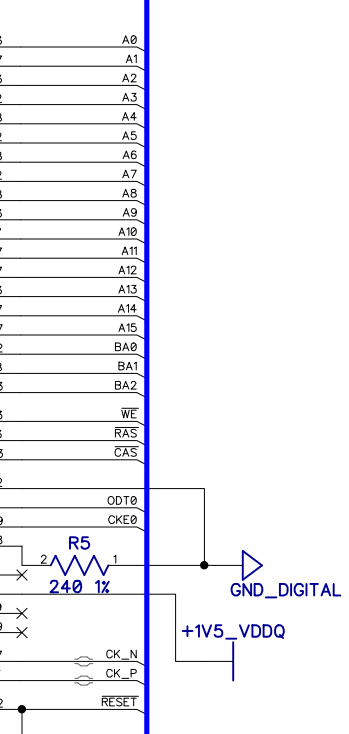
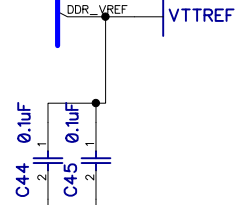
DDR Termination



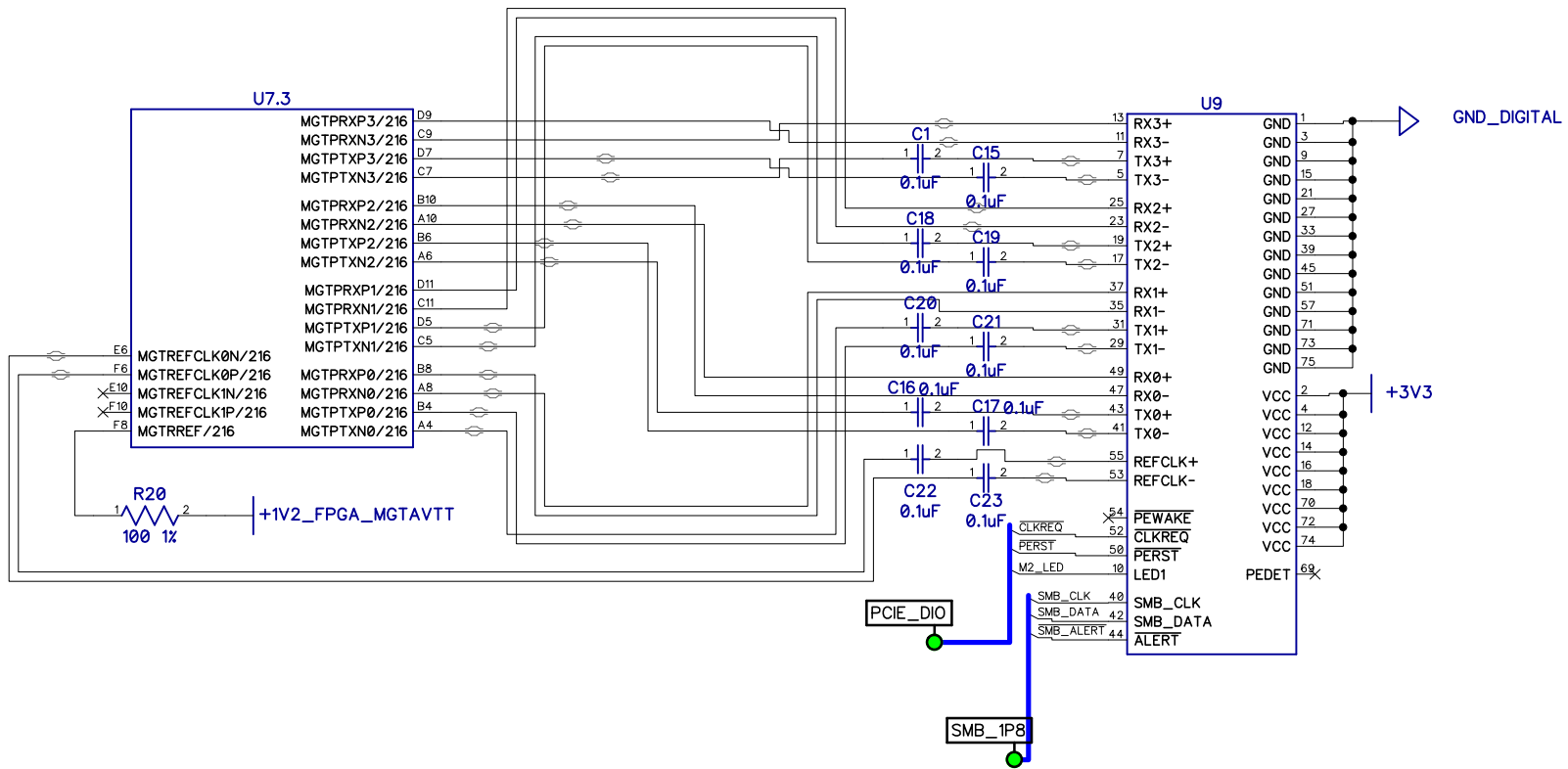
200MHz DDR clock



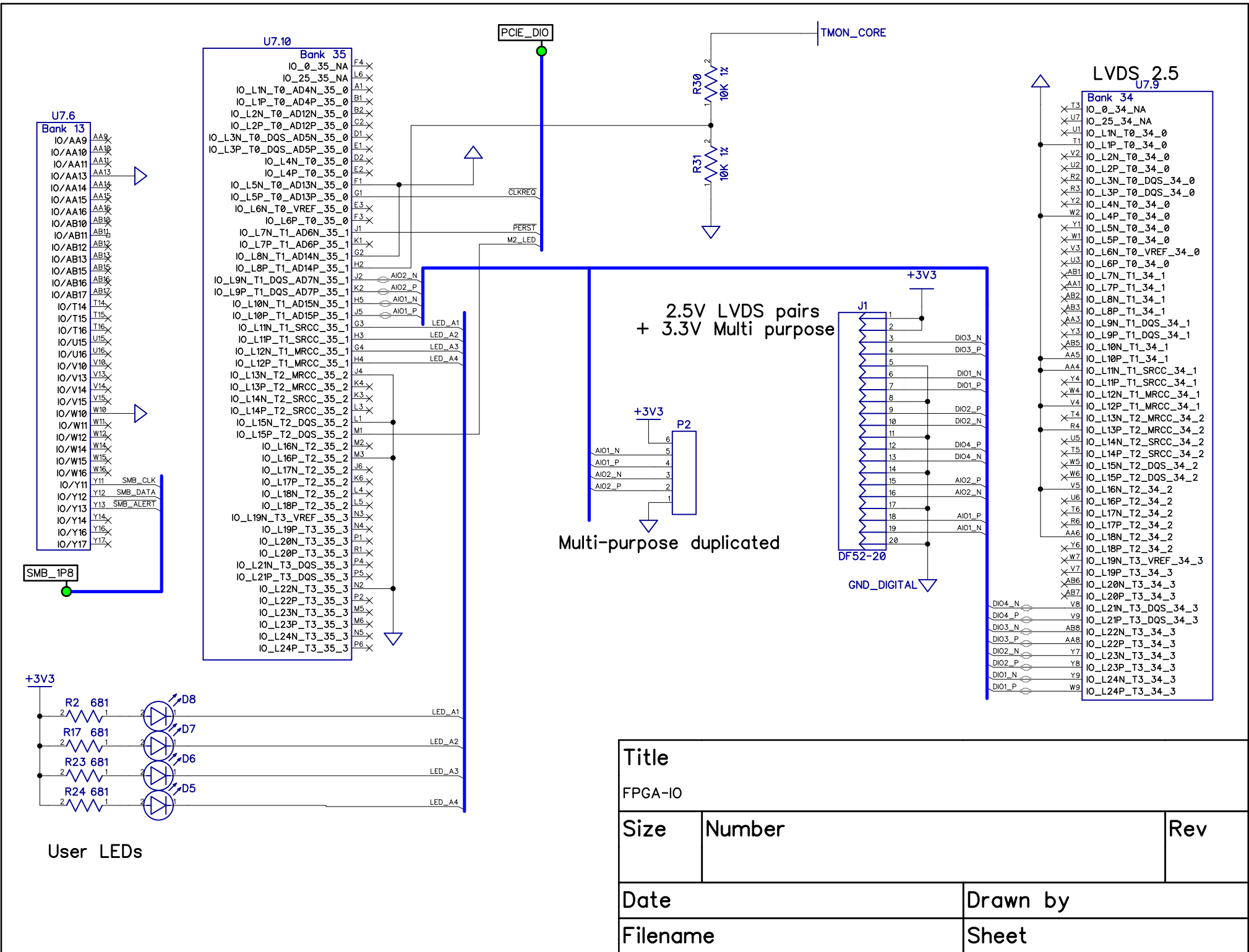
FPGA VTTRef decouplers



Title		DDR	
Size	Number	Rev	
Date	Drawn by		
Filename	Sheet		

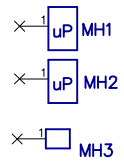


Title		
FPGA-MGT		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	

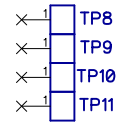


Title		
FPGA-IO		
Size	Number	Rev
Date	Drawn by	
Filename	Sheet	

Heatsink mounting holes/standoffs



Stencil Alignment Pads



Title		
Mechanical		
Size	Number	Rev
Date		Drawn by
Filename		Sheet

REV	Date	DESC
Z2	3/10/2019	Fixed faulty power supply wiring
Z1	10/15/2018	Initial release

Title		
Revision history		
Size	Number	Rev
2018-05-11	DPR	
NiteFury	Sheet	