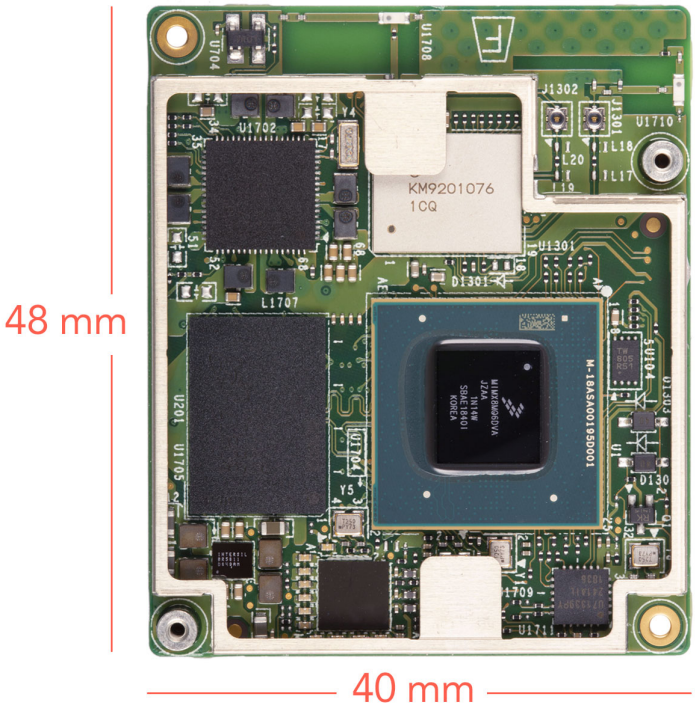
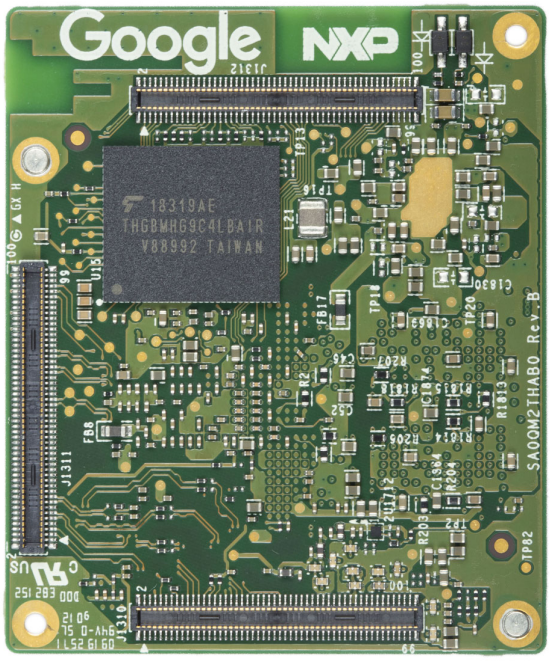
Coral

System-On-Module Datasheet

Version 1.2





Version 1.2 (August 2019)

Features

- NXP i.MX 8M SoC
  - Quad-core ARM Cortex-A53, plus Cortex-M4F
  - 2D/3D Vivante GC7000 Lite GPU and VPU
- Google Edge TPU ML accelerator
- Cryptographic coprocessor
- Wi-Fi 2x2 MIMO (802.11b/g/n/ac 2.4/5GHz)
- Bluetooth 4.2
- 8GB eMMC
- 1GB LPDDR4
- USB 3.0
- Gigabit Ethernet
- HDMI and MIPI-DSI
- MIPI-CSI-2
- Up to 95x GPIO (including SPI, I2C, PWM, UART, SAI, and SDIO)

Overview

The Coral System-on-Module (SoM) is a fully-integrated system that helps you build embedded systems that demand fast machine learning (ML) inferencing. It contains NXP's iMX8M system-on-chip (SoC), eMMC memory, LPDDR4 RAM, Wi-Fi, and Bluetooth, but its unique power comes from Google's Edge TPU coprocessor.

The Edge TPU is a small ASIC designed by Google that provides high performance ML inferencing with a low power cost. For example, it can execute state-of-the-art mobile vision models such as MobileNet v2 at 400 FPS, in a power efficient manner. This on-device processing reduces latency, increases data privacy, and removes the need for a high-bandwidth connection used to perform ML inferencing in the cloud.

Key benefits of the SoM:

- High-speed and low-power ML inferencing (4 TOPS @2W)
- A complete Linux system (running Mendel, a Debian derivative)
- Small footprint (40 x 48 mm)

The SoM is also included in the **Coral Dev Board**, which is a single-board computer that enables fast prototyping and evaluation of the standalone SoM.

Table of contents

System components

Table 1. Available SoM components and features

Feature	Details
Main system-on-chip (i.MX8M)	
Arm Cortex-A53 MPCore platform	Quad symmetric Cortex-A53 processors: • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Support L1 cache RAMs protection with parity/ECC Support of 64-bit Armv8-A architecture: • 1 MB unified L2 cache • Support L2 cache RAMs protection with ECC • Frequency of 1.5 GHz
Arm Cortex-M4 core platform	• 16 KB L1 Instruction Cache • 16 KB L1 Data Cache • 256 KB tightly coupled memory (TCM)
Graphic Processing Unit (GPU)	• Vivante GC7000Lite • 4 shaders • 267 million triangles/sec • 1.6 Gigapixel/sec • 32 GFLOPs 32-bit or 64 GFLOPs 16-bit • Supports OpenGL ES 1.1, 2.0, 3.0, 3.1, Open CL 1.2, and Vulkan
Video Processing Unit (VPU)	• 4Kp60 HEVC/H.265 main, and main 10 decoder • 4Kp60 VP9 and 4Kp30 AVC/H.264 decoder (requires full system resources) • 1080p60 MPEG-2, MPEG-4p2, VC-1, VP8, RV9, AVS, MJPEG, H.263 decoder

Feature	Details
I/O connectivity	• 2x USB 3.0/2.0 controllers with integrated PHY interfaces • 1x Ultra Secure Digital Host Controller (uSDHC) interfaces • 1x Gigabit Ethernet controller with support for EEE, Ethernet AVB, and IEEE 1588 • 2x UART modules • 2x I2C modules • 2x SPI modules • 16x GPIO lines with interrupt capability • 4x PWM lines • Input/output multiplexing controller (IOMUXC) to provide centralized pad control Note: The list above is the number of signals available to the baseboard (after considering SoC signals used by the SoM).
On-chip memory	• Boot ROM (128 KB) • On-chip RAM (128 KB + 32 KB)
External memory	• 32/16-bit DRAM interface: LPDDR4-3200, DDR4-2400, DDR3L-1600 • 8-bit NAND-Flash • eMMC 5.0 Flash • SPI NOR Flash • QuadSPI Flash with support for XIP

Feature	Details
Display	HDMI Display Interface: • HDMI 2.0a supporting one display up to 1080p • Upscale and downscale between 4K and HD video (requires full system resources) • 20+ Audio interfaces 32-bit @ 384 kHz fs, with Time Division Multiplexing (TDM) support • SPDIF input and output • Audio Return Channel (ARC) on HDMI MIPI-DSI Display Interface: • MIPI-DSI 4 channels supporting one display, resolution up to 1920 x 1080 at 60 Hz • LCDIF display controller • Output can be LCDIF output or DC display controller output
Audio	• 1x SPDIF input and output • 2x synchronous audio interface (SAI) modules supporting I2S, AC97, TDM, and codec/DSP interfaces • 1x SAI for 8 Tx channels for HDMI output audio • 1x SPDIF input for HDMI ARC input
Camera	• 2x MIPI-CSI2 camera inputs (4-lane each)
Security	• Resource Domain Controller (RDC) supports four domains and up to eight regions • Arm TrustZone (TZ) architecture • On-chip RAM (OCRAM) secure region protection using OCRAM controller • High Assurance Boot (HAB) • Cryptographic acceleration and assurance (CAAM) module • Secure non-volatile storage (SNVS): Secure real-time clock (RTC) • Secure JTAG controller (SJC)
ML accelerator	

Feature	Details
Edge TPU coprocessor	• ASIC designed by Google that provides high performance ML inferencing for TensorFlow Lite models • Uses PCIe and I2C/GPIO to interface with the iMX8M SoC • 4 trillion operations per second (TOPS) • 2 TOPS per watt
Memory and storage	
Random access memory (SDRAM)	• 1GB LPDDR4 SDRAM (4-channel, 32-bit bus width) • 1600MHz maximum DDR clock • Interfaces directly to the iMX8M build-in DDR controller
Flash memory (eMMC)	• 8GB NAND eMMC flash memory • 8-bits MMC mode • Conforms to JEDEC version 5.0 and 5.1
Expandable flash (MicroSD)	• Meets SD/SDIO 3.0 standard • Runs at 4-bits SDIO mode • Supports system boot from SD card
Network & wireless	
Ethernet	• 10/100/1000 Mbps Ethernet/IEEE 802.3 networks • Reduced gigabit media-independent interface (RGMII)
Wi-Fi	Murata LBEE5U91CQ module: • Wi-Fi 2x2 MIMO (802.11a/b/g/n/ac 2.4/5GHz) • Supports PCIe host interface for W-LAN
Bluetooth	Murata LBEE5U91CQ module: • Bluetooth 4.2 (supports Bluetooth low-energy) • Supports UART interface
Security	
Cryptographic coprocessor	Microchip ATECC608A cryptographic coprocessor: • Asymmetric (public/private) key cryptographic signature solution based on Elliptic Curve Cryptography and ECDSA signature protocols

Feature	Details
Hardware interface	
Baseboard connectors	3x 100-pin connectors (Hirose DF40C-100DP-0.4V)
Antenna connectors	2x coaxial cable connectors (Murata MM8930-2600)

Block diagrams

Figures 1 and 2 illustrate the core components on the SoM and SoC.

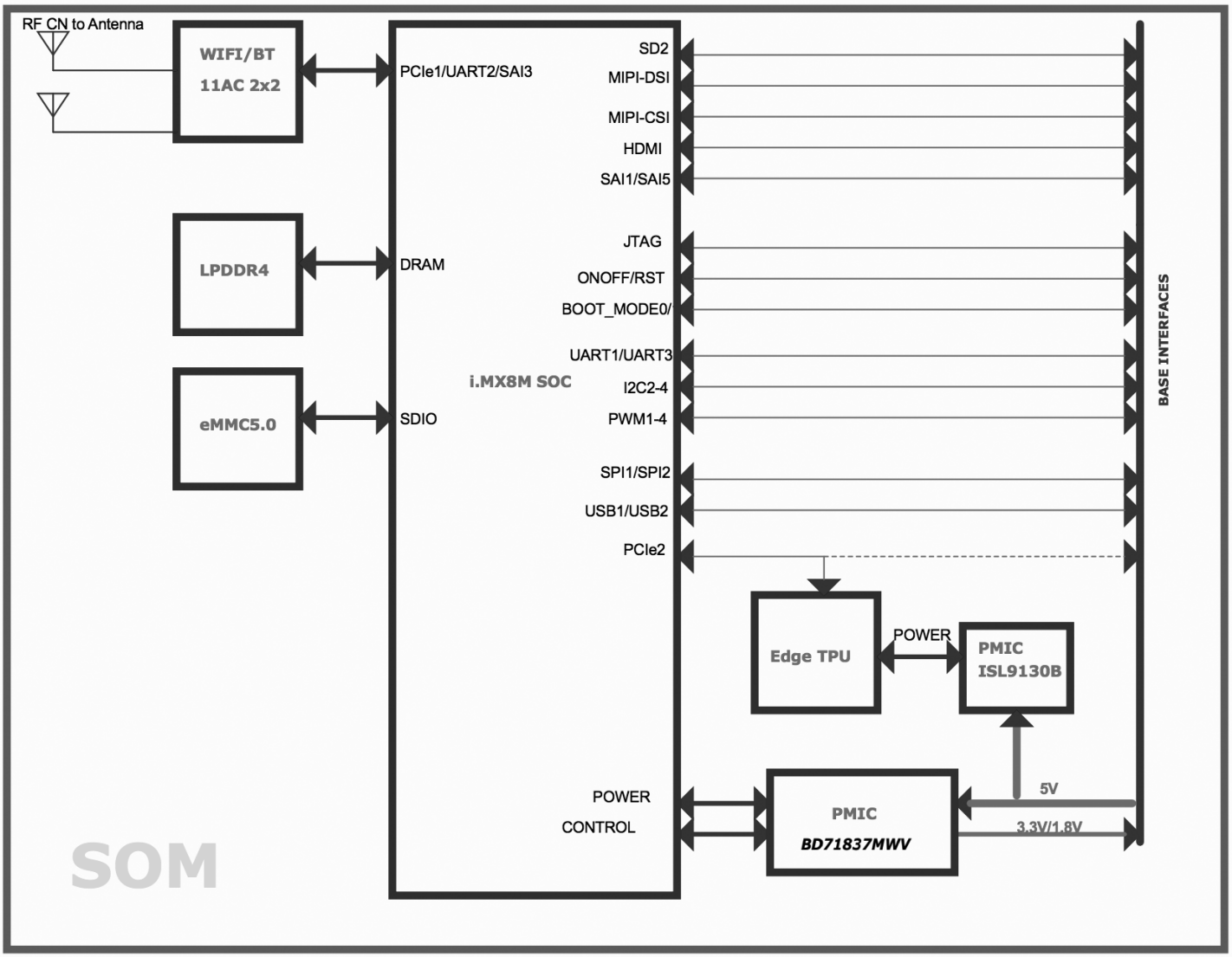


Figure 1. Block diagram of the SoM components

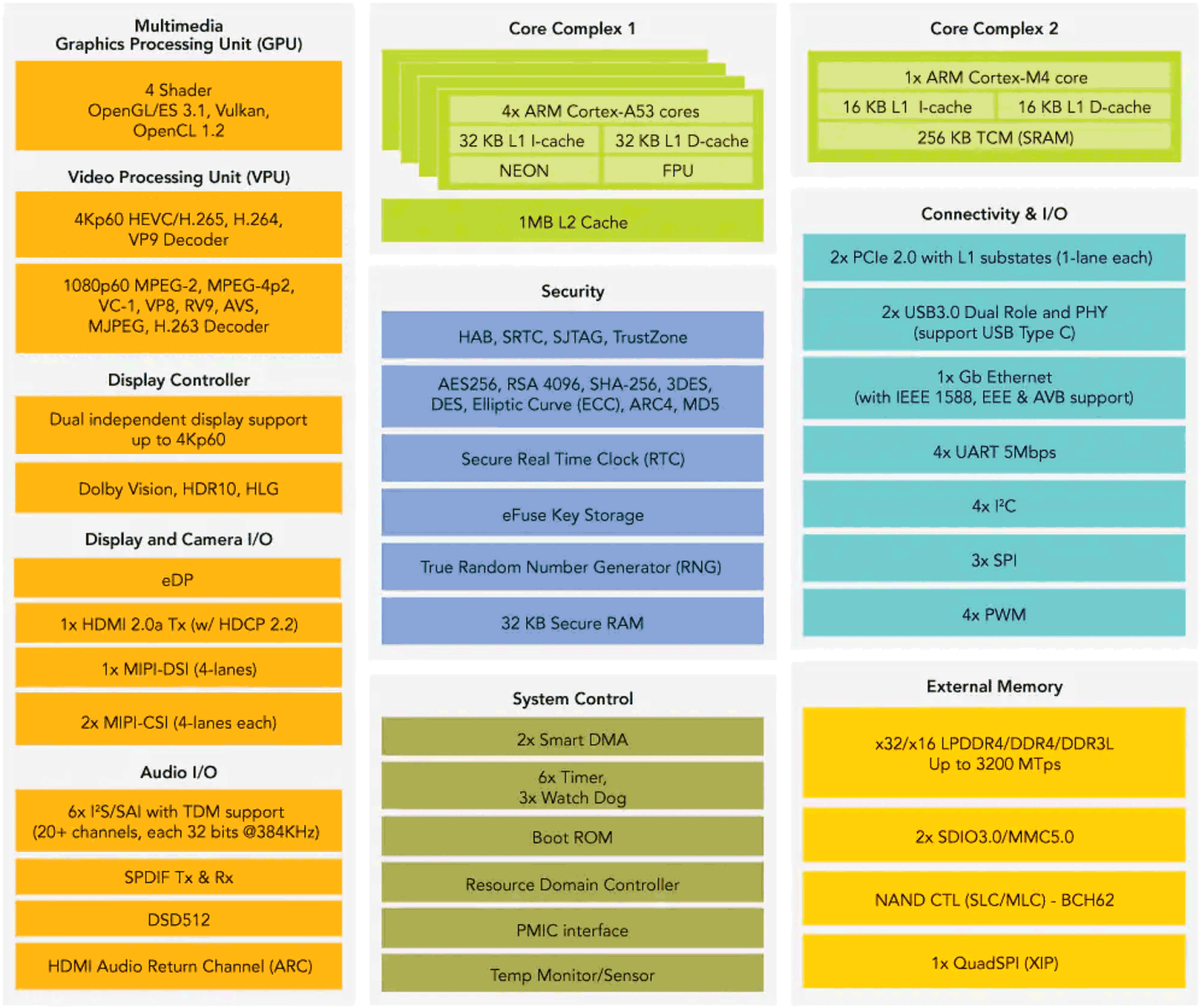


Figure 2. Block diagram of the i.MX8M SoC components, provided by NXP (some I/O signals on the SoC are consumed on the SoM, so refer to table 1 for availability)

Mechanical dimensions

Table 2. SoM mechanical dimensions

Measurement	Value
Size	48 x 40 x 5.11 mm
Weight	13 g

Figure 3 illustrates all of the SoM's dimensions. For a top-down view of the baseboard connector locations and component height restrictions, see the **Baseboard developer guide**.

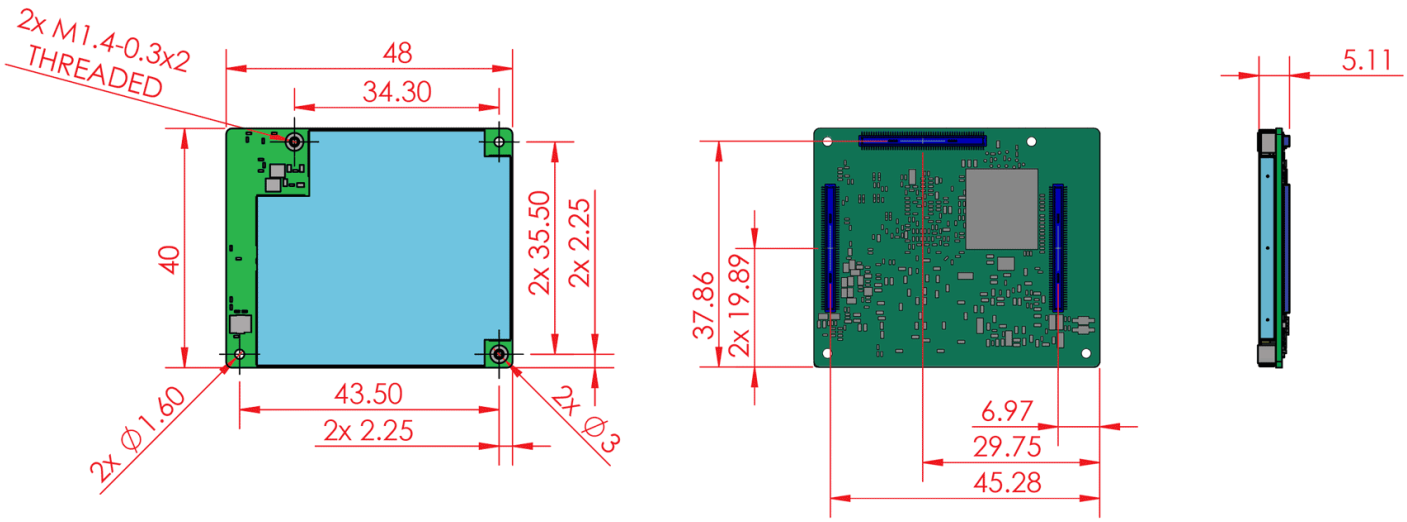


Figure 3. SoM dimensions (in millimeters)

Environmental reliability

Table 3. SoM environmental and mechanical limits

Measurement	Limits
Shock	50G/20ms
Vibration	20G/0-600Hz
MTTF	>200,000 hours
Operation temperature	0 to 50°C
Storage temperature	-40 to 85°C
Relative humidity	10% to 90% (operation) 5% to 95% (storage)

Certifications

Table 4. SoM certifications

Market	Certifications
USA	FCC
European Union	CE

System power

The SoM requires 5V as power input (at VSYS_5V). The SoM then generates the local voltage rails for all SoM components through on-board PMICs.

Table 5. SoM power requirements

Power input	Voltage
Main power supply (VSYS_5V)	5V +/-5%

Caution: Do not connect the 1.8V/3.3V power output pins to any high current devices or you might brownout the system. These power lines are shared with internal SoM circuits, so there is no safe limit for a high current device, but you can safely use them for low current tasks such as for a level shifter or pull-up/down.

Caution: Do not connect any of the 3.3V I/O pins to a device that draws more than ~ 82 mA of power or you will brownout the system.

Power signals

Even though there are multiple power signals defined in the board-to-board connectors, only the VSYS_5V and ground connections are required. All others are optional.

Note: Make sure to route *all* the VSYS_5V and GND pins, and add decoupling (bypass) capacitors between VSYS_5V and GND near the mating connector pins.

Table 6. Power and reset pin signals

Name	Type	Connector	Pins	Voltage	Description
VSYS_5V	Power	J1312	93, 94, 95, 96, 97, 98, 99, 100	5V	Main 5V power input to SoM. Must be connected.
GND	Power	J1312	9, 10, 65, 66, 71, 72, 77, 78, 83, 84		Common ground. Must be connected.
GND	Power	J1311	1, 2, 7, 8, 13, 14, 19, 20, 25, 26, 31, 33, 37, 38, 43, 44, 49, 50, 55, 56, 61, 62, 67, 68, 73, 74, 79, 80, 86, 89, 90, 94, 99, 100		Common ground. Must be connected.
GND	Power	J1310	1, 2, 7, 25, 39, 40, 42, 44, 45, 46, 50, 51, 56, 57, 62, 63, 64, 65, 66, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 80		Common ground. Must be connected.
DCDC_3V3	Power	J1310	84, 86, 88, 90	3.3V	3.3V output from SoM. Can be left floating if not used. Not for high-current usage; can be used to pull-up GPIO.

Name	Type	Connector	Pins	Voltage	Description
VDD_3V3	Power	J1310	94, 96, 98 100	3.3V	3.3V output from SoM. Can be left floating if not used. Not for high-current usage; can be used to pull-up GPIO.
VDDA_1V8	Power	J1310	91, 93, 95, 97, 99	1.8V	1.8V output from SoM. Can be left floating if not used. Not for high-current usage; can be used to pull-up GPIO.
POR_B	Output	J1310	79	3.3V	"Power_On_Reset" signal from IMX8M PMIC to reset the SoC (active-low open-drain output)
SYS_nRST	Input	J1312	63	3.3V	System reset (active-low input). Recommended for reset button on baseboard.

Power consumption

The following table lists the power draw for certain SoM components during different operational tests.

Table 7. SoM power draw measurements

Operational test	SoM power	System power (SoM + Dev Board baseboard)*
Idle	2.6W	4.0W
Idle with HDMI display on	3.0W	4.3W
High performance	6.2W	8.5W

* *Tested with **Coral Dev Board**—performance on your custom baseboard may vary*

During the high performance test, the top power-consuming components (top heat sources) are indicated in figure 4.

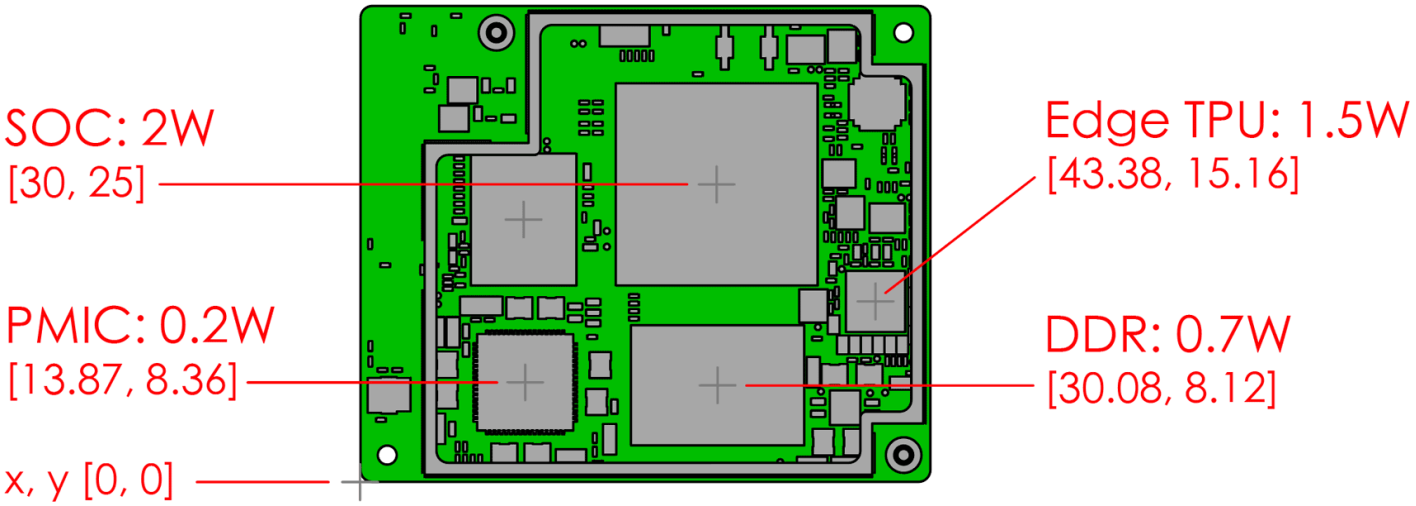


Figure 4. Power draw and ordinate locations (in millimeters) of top power components on the SoM while running the high performance test

The high performance test includes the following:

- GPU: 3D rendering
- CPU: 2 of 4 cores 100% loaded
- Active Wi-Fi download
- 7" HDMI display on
- DDR: 800 MHz
- Edge TPU running MobileNet V1 at 500 MHz
- Fan intermittently on

> **Caution:** You must provide a cooling solution to ensure the SoM surface maintains an operational temperature as specified in the Environmental reliability section. Unlike the Coral Dev Board, the standalone SoM does not include a cooling solution (the SoM components are covered only with an EMI shield).

Boot mode

Use the BOOT_MODE[1:0] pins to configure the SoM boot mode setting as indicated in the following tables.

Table 8. Boot mode pin signals

Name	Type	Connector	Pins	Voltage	Description
BOOT_MODE0	Input	J1312	64	3.3V	SoC BOOT_MODE0 signal (can be set by switch or pin-strap on baseboard)
BOOT_MODE1	Input	J1312	62	3.3V	SoC BOOT_MODE1 signal (can be set by switch or pin-strap on baseboard)

Table 9. Boot mode pin settings

BOOT_MODE[1:0] bits	Boot type
00	Boot from fuses (default behavior)
01	Serial downloader
10	Internal boot
11	Reserved

The boot configuration is specified by the iMX8M SoC, so for more details, refer to the **iMX8M SoC documentation**.

> **Note:** If BOOT_MODE[1:0] is "10" (internal boot), then GPIO pins SAI1_RX[7:0] and SAI1_TX[7:0] are used to enable boot configuration overrides by latching them to the BOOT_CFG[15:0] bits in the SoC. For details about these GPIO boot overrides, see the iMX8M SoC documentation.

Peripheral interfaces

The following interfaces are available from the SoM, through the three 100-pin board-to-board connectors.

This section is organized based on the default pin functions when running the Mendel operating system. For information about alternative pin functions you may enable with your own device tree overlay, see the **iMX8M SoC documentation**.

> **Note:** All I/O pins have a 90k pull-down resistor in the SoC that are used by default during bootup, which you can reconfigure with a device tree overlay after bootup. However, some pins (such as I2C, some SAI, and some SD2 pins) also have pull-up resistors inside the SoM, as noted in the following tables, which you cannot reconfigure with a device tree overlay.

> **Caution:** Do not connect any of the 3.3V I/O pins to a device that draws more than ~ 82 mA of power or you will brownout the system.

MIPI camera (CSI)

There are two channels for MIPI camera serial interface (CSI-2), each with four lanes and a maximum bit rate of 1.5 Gbps.

Table 10. CSI channel 1 pins

Name	Type	Connector	Pins	Voltage	Description
MIPI_CSI1_CLK_P/N	Input	J1311	18/16	0.2-1.2V	MIPI CSI1 clock (positive/negative)
MIPI_CSI1_D0_P/N	Input	J1311	12/10	0.2-1.2V	MIPI CSI1 data (positive/negative)
MIPI_CSI1_D1_P/N	Input	J1311	23/21	0.2-1.2V	MIPI CSI1 data (positive/negative)
MIPI_CSI1_D2_P/N	Input	J1311	6/4	0.2-1.2V	MIPI CSI1 data (positive/negative)
MIPI_CSI1_D3_P/N	Input	J1311	29/27	0.2-1.2V	MIPI CSI1 data (positive/negative)

Table 11. CSI channel 2 pins

Name	Type	Connector	Pins	Voltage	Description
MIPI_CSI2_CLK_P/N	Input	J1311	36/34	0.2-1.2V	MIPI CSI2 clock (positive/negative)
MIPI_CSI2_D0_P/N	Input	J1311	35/33	0.2-1.2V	MIPI CSI2 data (positive/negative)
MIPI_CSI2_D1_P/N	Input	J1311	30/28	0.2-1.2V	MIPI CSI2 data (positive/negative)
MIPI_CSI2_D2_P/N	Input	J1311	24/22	0.2-1.2V	MIPI CSI2 data (positive/negative)
MIPI_CSI2_D3_P/N	Input	J1311	41/39	0.2-1.2V	MIPI CSI2 data (positive/negative)

MIPI display (DSI)

The four-lane MIPI display serial interface (DSI) offers the following features:

- Resolution up to 1920 x 1080 at 60 Hz
- LCDIF display controller
- Maximum bit rate of 1.5 Gbps

Table 12. DSI pins

Name	Type	Connector	Pins	Voltage	Description
MIPI_DSI1_CLK_P/N	Output	J1311	59/57	0.2-1.2V	MIPI DSI clock (positive/negative)
MIPI_DSI1_D0_P/N	Output	J1311	47/45	0.2-1.2V	MIPI DSI data (positive/negative)
MIPI_DSI1_D1_P/N	Output	J1311	54/52	0.2-1.2V	MIPI DSI data (positive/negative)
MIPI_DSI1_D2_P/N	Output	J1311	42/30	0.2-1.2V	MIPI DSI data (positive/negative)
MIPI_DSI1_D3_P/N	Output	J1311	48/46	0.2-1.2V	MIPI DSI data (positive/negative)

HDMI

The High-Definition Multimedia Interface (HDMI) connection provides the following features:

- HDMI 2.0a supporting one display up to 1080p
- Upscale and downscale between 4K and HD video (requires full system resources)
- 20+ Audio interfaces 32-bit @ 384 kHz fs, with Time Division Multiplexing (TDM) support
- SPDIF input and output
- Audio Return Channel (ARC) on HDMI

Table 13. HDMI pins

Name	Type	Connector	Pins	Voltage	Description
HDMI_REFCLKP/N	Output	J1310	58/60	3.3V	HDMI reference clock (27Mhz) (positive/negative)
HDMI_CLKP/N	Output	J1312	68/70	3.3V	HDMI clock (positive/negative)
HDMI_TX0_P/N	Output	J1312	75/73	3.3V	HDMI transmit (positive/negative)
HDMI_TX1_P/N	Output	J1312	81/79	3.3V	HDMI transmit (positive/negative)
HDMI_TX2_P/N	Output	J1312	76/74	3.3V	HDMI transmit (positive/negative)
HDMI_AUX_P/N	Output	J1312	82/80	3.3V	HDMI AUX (positive/negative)
HDMI_HPD	Output	J1312	89	3.3V	HDMI Hot Plug Detect
HDMI_DDC_SDA	Output	J1312	85	3.3V	HDMI Display Data Channel data
HDMI_DDC_SCL	Output	J1312	87	3.3V	HDMI Display Data Channel clock
HDMI_CEC	Output	J1312	91	3.3V	HDMI Consumer Electronic Control

Ethernet

The Ethernet Media Access Controller (MAC) supports 10/100/1000 Mbps Ethernet/IEEE 802.3 networks with reduced gigabit media-independent interface (RGMII). Requires an Ethernet PHY on the baseboard.

Table 14. Ethernet pins

Name	Type	Connector	Pins	Voltage	Description
ENET_RD0	Input	J1310	33	1.8V	RGMII receive from PHY
ENET_RD1	Input	J1310	35	1.8V	RGMII receive from PHY
ENET_RD2	Input	J1310	31	1.8V	RGMII receive from PHY
ENET_RD3	Input	J1310	37	1.8V	RGMII receive from PHY
ENET_RX_CTL	Input	J1310	29	1.8V	RGMII receive from PHY
ENET_RXC	Input	J1310	27	1.8V	RGMII receive from PHY
ENET_TD0	Output	J1310	19	1.8V	RGMII transmit to PHY
ENET_TD1	Output	J1310	21	1.8V	RGMII transmit to PHY
ENET_TD2	Output	J1310	17	1.8V	RGMII transmit to PHY
ENET_TD3	Output	J1310	15	1.8V	RGMII transmit to PHY
ENET_TX_CTL	Output	J1310	13	1.8V	RGMII transmit to PHY
ENET_TXC	Output	J1310	23	1.8V	RGMII transmit to PHY
ENET_MDC	Output	J1310	11	1.8V	RGMII clock for PHY
ENET_MDIO	Output	J1310	9	1.8V	RGMII MDIO data for PHY
ENET_nRST (GPIO1_IO09)	Output	J1312	43	3.3V	PHY reset
ENET_nINT (GPIO1_IO11)	Input	J1312	39	3.3V	PHY interrupt
ENET_WoL (GPIO1_IO10)	Input	J1312	41	3.3V	PHY Wake-on-Lan
CLKO_25M (GPIO1_IO15)	Output	J1310	54	3.3V	Optional 25Mhz clock to PHY

PCIe

The SoC includes PCIE1 and PCIE2 lines that are routed to the baseboard connectors, but you should not need to connect these and **you should not remap these with your own device tree** because both are used on the SoM for Wi-Fi (PCIE1) and the Edge TPU (PCIE2).

USB

There are two USB controllers and corresponding PHYs on the SoM. Each USB instance contains USB 3.0 core, which can operate in both USB 3.0 and 2.0 mode.

Table 15. USB channel 1 pins

Name	Type	Connector	Pins	Voltage	Description
USB1_DP/N	I/O	J1311	51/53	3.3V	USB 2.0 (positive/negative)
USB1_TXP/N	Output	J1311	58/60	1.8V	USB 3.0 transmit (positive/negative)
USB1_RXP/N	Input	J1311	64/66	1.8V	USB 3.0 receive (positive/negative)
USB1_VBUS	Input	J1311	82/84	5V	VBUS detect (same at both pins)
USB1_ID	Input	J1311	76	3.3V	USB ID

Table 16. USB channel 2 pins

Name	Type	Connector	Pins	Voltage	Description
USB2_DP/N	I/O	J1311	63/65	3.3V	USB 2.0 (positive/negative)
USB2_TXP/N	Output	J1311	69/71	1.8V	USB 3.0 transmit (positive/negative)
USB2_RXP/N	Input	J1311	79/72	1.8V	USB 3.0 receive (positive/negative)
USB2_VBUS	Input	J1311	75/77	5V	VBUS detect (same at both pins)
USB2_ID	Input	J1311	88	3.3V	USB ID

Digital audio (SAI)

The SAI module provides a synchronous audio interface (SAI) that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

Note: If booting the SoM in eFUSE mode (default behavior), all SAI pins are available during boot. However, when using the other boot modes, pins SAI1_RX[7:0] and SAI1_TX[7:0] are used to enable boot configuration overrides by latching them to the BOOT_CFG[15:0] bits in the SoC—that is, only until boot completes. The SoM uses internal pin strap (pull-up and pull-down) resistors to select the different boot configuration, so you should be careful if you add any pull-up/down resistors for these pins on your baseboard. For details, see the IMX8M SoC documentation.

Table 17. SAI 1 signals

Name	Type	Connector	Pins	Voltage	Description
SAI1_MCLK	I/O	J1312	26	3.3V	Audio master clock
SAI1_RXC	Input	J1312	17	3.3V	Receive bit clock
SAI1_RXFS	Input	J1312	19	3.3V	Receive frame sync
SAI1_RXD0	Input	J1312	33	3.3V	Receive channel. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD1	Input	J1312	35	3.3V	Receive channel. Pull-up in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD2	Input	J1312	27	3.3V	Receive channel. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD3	Input	J1312	31	3.3V	Receive channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD4	Input	J1312	29	3.3V	Receive channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD5	Input	J1312	21	3.3V	Receive channel. Pull-up in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_RXD6	Input	J1312	25	3.3V	Receive channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.

Name	Type	Connector	Pins	Voltage	Description
SAI1_RXD7	Input	J1312	23	3.3V	Receive channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXC	Output	J1312	40	3.3V	Transmit bit clock.
SAI1_TXFS	Output	J1312	46	3.3V	Transmit frame sync.
SAI1_TXD0	Output	J1312	44	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD1	Output	J1312	42	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD2	Output	J1312	30	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD3	Output	J1312	36	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD4	Output	J1312	38	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD5	Output	J1312	34	3.3V	Transmit channel. Pull-up in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD6	Output	J1312	28	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.
SAI1_TXD7	Output	J1312	32	3.3V	Transmit channel. Pull-down in SoM: 10k Ohm. Reserved during boot, except in eFUSE mode. See note above.

Table 18. SAI 2 signals

Name	Type	Connector	Pins	Voltage	Description
SAI2_TXD	Output	J1312	14	3.3V	Transmit channel
SAI2_RXD	Input	J1312	20	3.3V	Receive channel
SAI2_TXC	Output	J1312	18	3.3V	Transmit bit clock
SAI2_TXFS	Output	J1312	16	3.3V	Transmit frame sync
SAI2_MCLK	I/O	J1312	12	3.3V	Audio master clock
SAI2_RXFS	Input	J1312	24	3.3V	Receive frame sync
SAI2_RXC	Input	J1312	23	3.3V	Receive bit clock

Note: The SoC includes SAI3 lines, but most of these are used by the SoM for Wi-Fi, so you should not remap these with your device tree.

The SoC also includes SAI5 lines but they are used as pin-strap for board identification purposes. Three of them (SAI5_RXD1, SAI5_RXD3, and SAI5_RXFS) are pin-strapped inside the SoM, and their level is latched by the U-Boot bootloader to determine the LPDDR4 memory size. **We recommend that you do not use those pins for any other purpose in your baseboard**.

The other unused SAI3 and SAI5 signals are available as **GPIO**.

Sony/Philips audio (SPDIF)

Sony/Philips Digital Interface (SPDIF) is a standard audio file transfer format that supports Transmitter and Receiver functionality. Refer to **NXP iMX8M documentation** for additional details.

Table 19. SPDIF pin signals

Name	Type	Connector	Pins	Voltage	Description
SPDIF_EXT_CLK	Output	J1311	92	3.3V	External clock signal
SPDIF_TX	Output	J1311	96	3.3V	Transmit data channel
SPDIF_RX	Input	J1311	98	3.3V	Receive data channel

Micro-SD card

An Ultra Secure Digital Host Controller (uSDHC) module provides the interface between the host and SD/SDIO/MMC cards, with the following features:

- SD/SDIO standard, up to version 3.0
- MMC standard, up to version 5.0
- 3.3V operation only
- 1- and 4-bit SD/SDIO/MMC modes

Table 20. SD/MMC pin signals

Name	Type	Connector	Pins	Voltage	Description
SD2_CLK	Output	J1310	48	3.3V	Serial clock
SD2_CMD	Output	J1310	26	3.3V	Command line Pull-up in SoM: 10k Ohm
SD2_nCD (SD2_CD_B)	Output	J1310	24	3.3V	Card detect
SD2_DAT0	I/O	J1310	28	3.3V	Data bit 0 Pull-up in SoM: 10k Ohm
SD2_DAT1	I/O	J1310	32	3.3V	Data bit 1
SD2_DAT2	I/O	J1310	34	3.3V	Data bit 2
SD2_DAT3	I/O	J1310	38	3.3V	Data bit 3
SD2_nRST (SD2_RESET_B)	Output	J1310	36	3.3V	Card reset
SDIO_WAKE (SD2_WP)	Output	J1310	30	3.3V	Write protect or GPIO

JTAG debugging

5-pin JTAG debugging with a Secure JTAG Controller (SJC) for secure debugging.

Table 21. JTAG pin signals

Name	Type	Connector	Pins	Voltage	Description
JTAG_TMS	Output	J1312	59	3.3V	Test mode select
JTAG_TDI	Input	J1312	61	3.3V	Test data in
JTAG_TDO	Output	J1312	57	3.3V	Test data out
JTAG_TCK	Output	J1312	53	3.3V	Test clock
JTAG_nTRST	Input	J1312	55	3.3V	Test reset

I2C

Two I2C bus interfaces are available.

Table 22. I2C pin signals

Name	Type	Connector	Pins	Voltage	Description
I2C2_SCL	Input	J1311	87	3.3V	Serial clock Pull-up in SoM: 4.7k Ohm
I2C2_SDA	Output	J1311	85	3.3V	Serial data Pull-up in SoM: 4.7k Ohm
I2C3_SCL	Input	J1311	83	3.3V	Serial clock Pull-up in SoM: 4.7k Ohm
I2C3_SDA	Output	J1311	81	3.3V	Serial data Pull-up in SoM: 4.7k Ohm

Note: The SoC also includes I2C1 and I2C4 lines, but these are used by the SoM for power management and wireless controls, so you should not remap these with your own device tree.

UART

Two UART v2 modules are available with the following features:

- 7- or 8-bit data words, 1 or 2 stop bits, programmable parity (even, odd, or none).
- Programmable baud rates up to 4 Mbps.
- 32-byte FIFO on Tx and 32 half-word FIFO on Rx supporting auto-baud.

> **Note:** By default, the Mendel operating system configures UART1 for use with the the serial console.

Table 23. UART pin signals

Name	Type	Connector	Pins	Voltage	Description
UART1_TXD	Output	J1311	93	3.3V	Transmit channel
UART1_RXD	Input	J1311	95	3.3V	Receive channel
UART3_TXD	Output	J1311	91	3.3V	Transmit chanel
UART3_RXD	Input	J1311	97	3.3V	Receive channel

> **Note:** The SoC also includes UART2 and UART4 lines, but these are used by the SoM for Bluetooth, so you should not remap these with your own device tree.

SPI

Two full-duplex eSPI interfaces are available, with data rates up to 52 Mbit/s and two chip select lines.

Table 24. SPI channel 1 pin signals

Name	Type	Connector	Pins	Voltage	Description
ECSPI1_MISO	Input	J1312	5	3.3V	Master input
ECSPI1_MOSI	Output	J1312	7	3.3V	Master output
ECSPI1_SCLK	Output	J1312	4	3.3V	Serial clock
ECSPI1_SS0	Output	J1312	8	3.3V	Chip select
ECSPI1_SS1	Output	J1310	6	3.3V	Chip select

Table 25. SPI channel 2 pin signals

Name	Type	Connector	Pins	Voltage	Description
ECSPI2_MISO	Input	J1312	3	3.3V	Master input
ECSPI2_MOSI	Output	J1312	6	3.3V	Master output
ECSPI2_SCLK	Output	J1312	2	3.3V	Serial clock
ECSPI2_SS0	Output	J1312	1	3.3V	Chip select
ECSPI2_SS1	Output	J1310	4	3.3V	Chip select

GPIO

The following pins are configured for general purpose input/output, by default. Additionally, you can reconfigure other pins (SAI, SPDIF, SDIO, I2C, UART, SPI, and PWM) to behave as GPIO, using a device tree overlay.

Table 26. GPIO pin signals

Name	Type	Connector	Pins	Voltage	Description
GPIO6	I/O	J1312	49	3.3V	GPIO
GPIO7	I/O	J1312	45	3.3V	GPIO
GPIO8	I/O	J1312	47	3.3V	GPIO
GPIO12	I/O	J1312	51	3.3V	GPIO
NAND_CLE	I/O	J1310	10	3.3V	GPIO
NAND_DATA02	I/O	J1310	12	3.3V	GPIO
NAND_ALE	I/O	J1310	16	3.3V	GPIO
NAND_DATA07	I/O	J1310	18	3.3V	GPIO
NAND_DATA06	I/O	J1310	20	3.3V	GPIO
NAND_DATA03	I/O	J1310	22	3.3V	GPIO
SAI3_RXC	I/O	J1312	13	3.3V	GPIO
SAI3_RXFS	I/O	J1312	15	3.3V	GPIO
SAI5_MCLK	I/O	J1312	50	3.3V	GPIO
SAI5_RXC	I/O	J1312	56	3.3V	GPIO

Name	Type	Connector	Pins	Voltage	Description
SAI5_RXD0	I/O	J1312	58	3.3V	GPIO
SAI5_RXD2	I/O	J1312	54	3.3V	GPIO

PWM

There are four PWM output pins available with 16-bit resolution and 4x16 data FIFO.

Table 27. PWM pin signals

Name	Type	Connector	Pins	Voltage	Description
PWM1 (GPIO1_IO01)	Output	J1312	88	3.3V	PWM or GPIO
PWM2 (GPIO1_IO013)	Output	J1312	90	3.3V	PWM or GPIO
PWM3 (GPIO1_IO014)	Output	J1312	92	3.3V	PWM or GPIO
PWM4 (SAI3_MCLK)	Output	J1312	11	3.3V	PWM or GPIO

Wi-Fi and Bluetooth

The SoM includes the **Murata LBEE5U91CQ module**, which provides Wi-Fi (IEEE 802.11 a/b/g/n/ac WLAN, 2.4/5 GHz) and Bluetooth 4.2 (with Bluetooth Low Energy support), using wireless antennas integrated into the board.

Baseboard developer guide

This section provides details to help you integrate the Coral SoM into your own baseboard (carrier board) hardware.

Reference design

If you'd like to see a reference baseboard design, download the following schematic and layout files for the Coral Dev Board.

File	Description
Coral-Dev-Board-baseboard-schematic.pdf	Baseboard schematic in PDF
Coral-Dev-Board-baseboard-schematic-Altium.zip	Baseboard schematic files in Altium format
Coral-Dev-Board-baseboard-layout-Allegro.brd	Baseboard CAD layout in BRD format

Baseboard connectors

The SoM connects to the host baseboard with three 100-pin connectors.

Table 28. SoM and baseboard connectors

SoM	Baseboard
3x 100-position plug Hirose Electric DF40C-100DP-0.4V(51)	3x 100-position receptacle Hirose Electric DF40HC(3.0)-100DS-0.4V(51)

The location of each connector plug on the SoM is illustrated in **figure 3**, and the corresponding position for each receptacle on your baseboard is illustrated in **figure 5**.

Connectors, keepouts, and component max heights

Figure 5 illustrates the area of your baseboard where the SoM connects. The measurements are relative to the standoff in the bottom-left corner, indicating the position for the three board-to-board (B2B) connectors (Hirose DF40C-100DP-0.4V), two standoffs, and the following component regions:

A. Antenna keepout: Place no components and no copper in this region. This area of your baseboard is directly below the SoM's Wi-Fi and Bluetooth antennas, so it must be kept clear of any metals to ensure strong radio signals.

B. Max height of baseboard components in this region is 2.8mm.

C. Max height of baseboard components in this region is 1.5mm.

Additionally, figure 5 indicates the location of pin 1 on your baseboard connectors. To see all the pin assignments, refer to the **pinout schematic**.

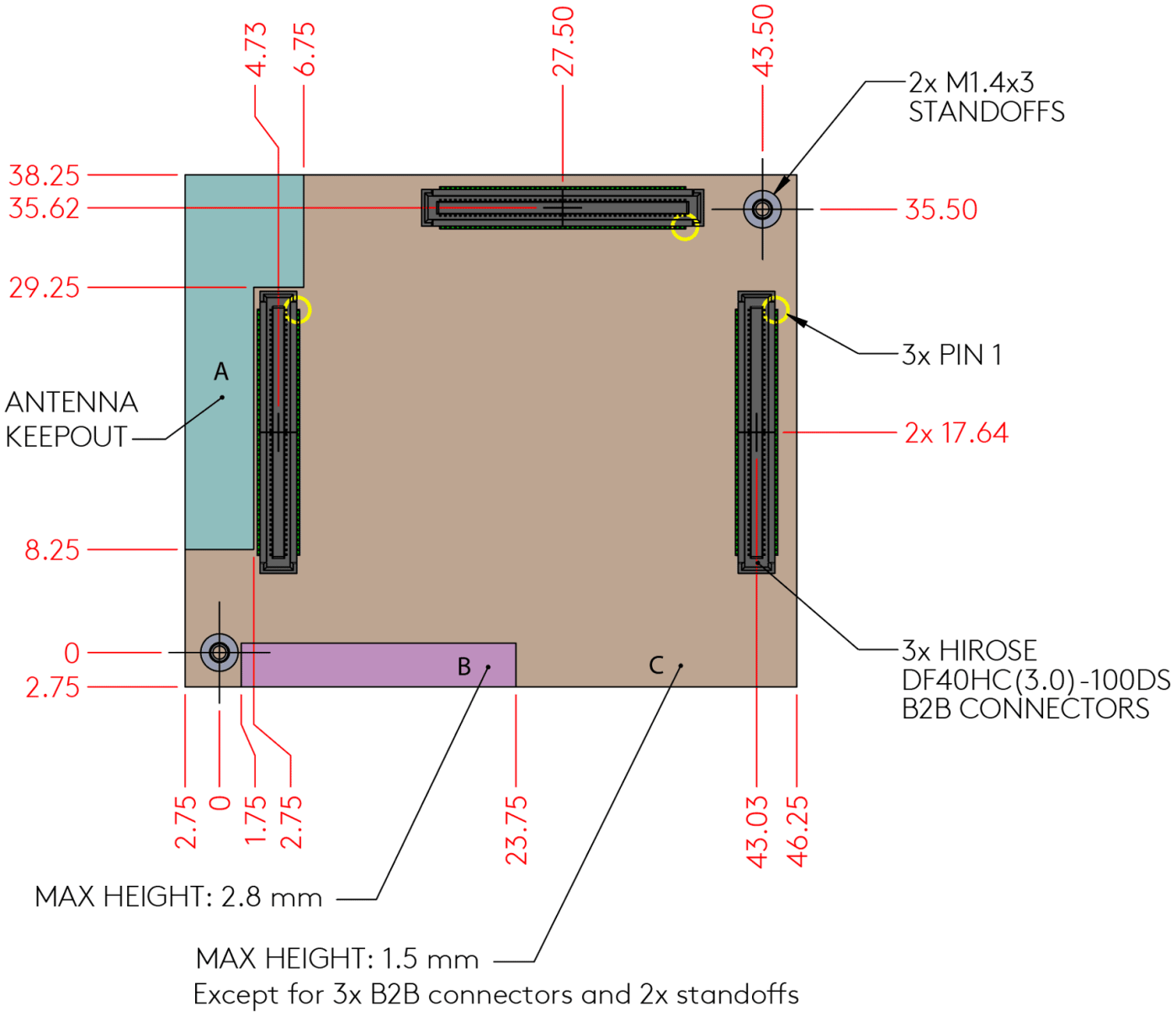


Figure 5. Top view of baseboard connectors and component restrictions (measured in millimeters)

Trace impedance recommendations

The following table lists the recommended impedance for high-speed signals on the baseboard.

Table 29. Trace impedance recommendation

Signal group	Impedance	PCB manufacture tolerance (+/-)
All single-ended signal, unless specified	50 Ohm single-ended	10%
PCIe TX/RX data pair	85 Ohm differential	10%
USB differential signals	90 Ohm differential	10%
Differential signals: including Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI)	100 Ohm differential	10%

MIPI trace length compensation

MIPI signals for the CSI/DSI interfaces are high-speed signals that require the total etched trace lengths for each line within a group (the paired clock lanes and four data lanes) be equal to each other. Due to space constraints on the SoM, the MIPI signal traces lengths currently are not equal (as indicated in the following tables). You must incorporate the length difference on your baseboard traces such that the trace lengths for each MIPI group match each other.

Table 30. CSI channel 1 signal trace length on SoM

Name	Etch length (mils)	Manhattan length (mils)
MIPI_CSI1_CLKN	306.1	287.89
MIPI_CSI1_CLKP	309.4	297.73
MIPI_CSI1_D0N	310.97	309.53
MIPI_CSI1_D0P	315.24	319.38
MIPI_CSI1_D1N	242.48	209.15
MIPI_CSI1_D1P	241.23	250.5
MIPI_CSI1_D2N	354.22	356.78
MIPI_CSI1_D2P	351.84	392.21
MIPI_CSI1_D3N	246.25	230.81
MIPI_CSI1_D3P	250.2	272.16

Table 31. CSI channel 2 signal trace length on SoM

Name	Etch length (mils)	Manhattan length (mils)
MIPI_CSI2_CLKN	299.51	282.39
MIPI_CSI2_CLKP	301.92	323.73
MIPI_CSI2_D0N	258.48	252.46
MIPI_CSI2_D0P	258.58	293.81
MIPI_CSI2_D1N	289.71	260.74
MIPI_CSI2_D1P	292.95	302.08
MIPI_CSI2_D2N	293.48	266.24
MIPI_CSI2_D2P	298.18	280.42
MIPI_CSI2_D3N	265.86	274.12
MIPI_CSI2_D3P	268.14	315.46

Table 32. DSI signal trace length on SoM

Name	Etch length (mils)	Manhattan length (mils)
MIPI_DSI_CLKN	296.45	339.08
MIPI_DSI_CLKP	297.41	380.43
MIPI_DSI_D0N	212.5	219
MIPI_DSI_D0P	211.9	260.34
MIPI_DSI_D1N	322.16	347.35
MIPI_DSI_D1P	326.95	388.69
MIPI_DSI_D2N	305.05	304.05
MIPI_DSI_D2P	309.08	345.38
MIPI_DSI_D3N	297.15	274.52
MIPI_DSI_D3P	298.16	315.86

Other recommendations

- Make sure to route *all* the VSYS_5V and GND pins, and add decoupling (bypass) capacitors between VSYS_5V and GND near the mating connector pins.
- When placing a pull-up or pull-down resistor on some of the SoM signals, such as I/O pins (especially SAI1_TXD[7:0] and SAI1_RXD[7:0]), review the signal description for each **peripheral interface**, because some of them already have pull-up/down resistor in the SoM for initialization purposes.

> Caution: You must provide a cooling solution to ensure the SoM surface maintains an operational temperature as specified in the Environmental reliability section. You can use the SoM's threaded standoffs (indicated in figure 3) to mount a passive or active cooling solution.

Pinout schematic

> Caution: The signal directions in figure 6 are not all accurate. Instead refer to the "type" of each pin in the tables from the Peripheral interfaces section.

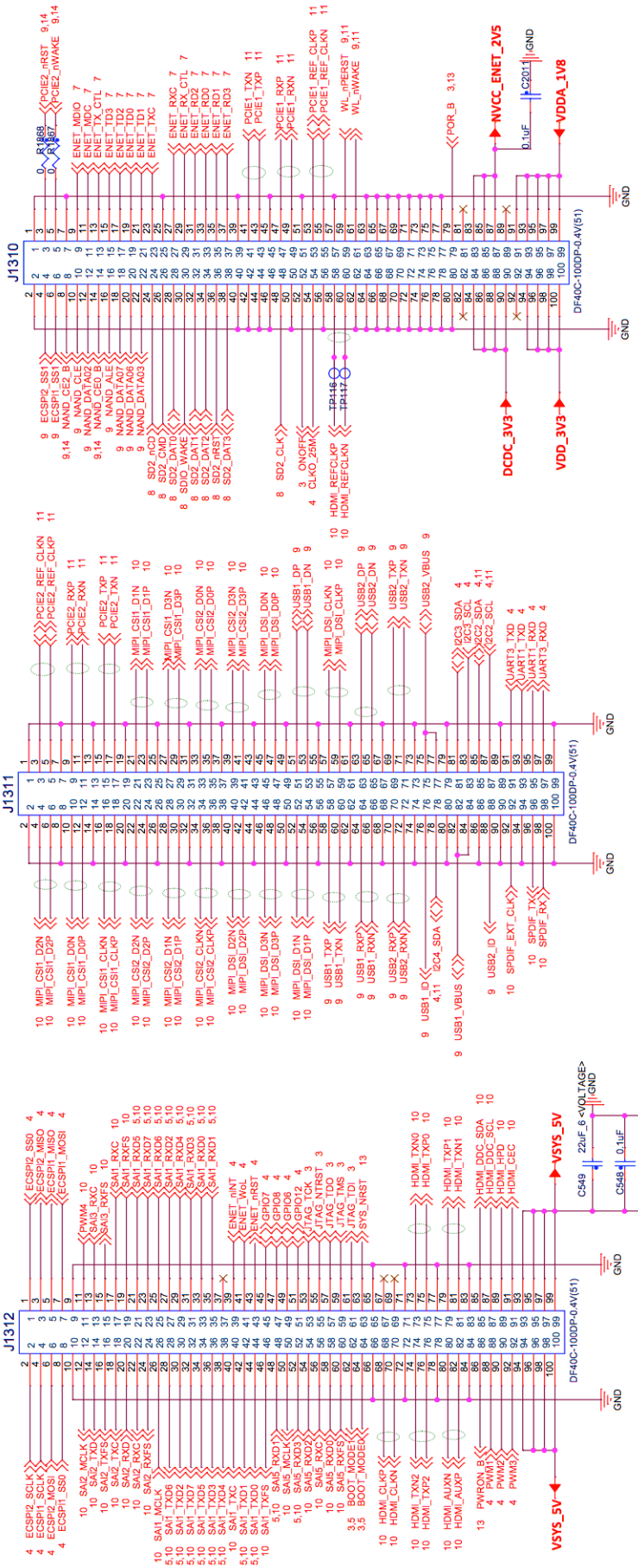


Figure 6. SoM connector schematic (click to enlarge)

Document revisions

Table 33. History of changes to this document

Version	Changes
1.2 (August 2019)	Add PDF download of this datasheet and the Dev Board baseboard schematic.
1.1 (July 2019)	Remove wireless antenna connector details.
1.0 (June 2019)	Initial release