Lake: A Framework for Designing and Automatically Configuring Physical Unified Buffers

Maxwell Strange

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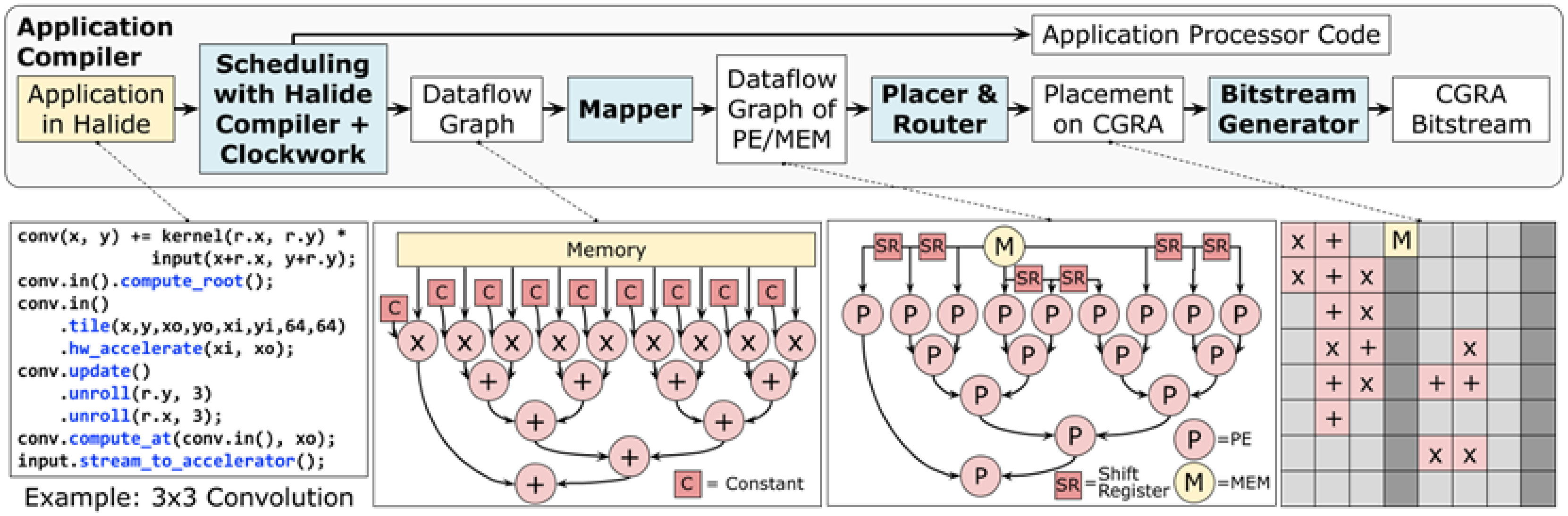
Lake – AHA Toolset Context

- Lake implements the **Memory (MEM)** portion of the dataflow graph



```
conv(x, y) += kernel(r.x, r.y) *
              input(x+r.x, y+r.y);
conv.in().compute_root();
conv.in()
    .tile(x,y,xo,yo,xi,yi,64,64)
    .hw_accelerate(xi, xo);
conv.update()
    .unroll(r.y, 3)
    .unroll(r.x, 3);
conv.compute_at(conv.in(), xo);
input.stream_to_accelerator();
```

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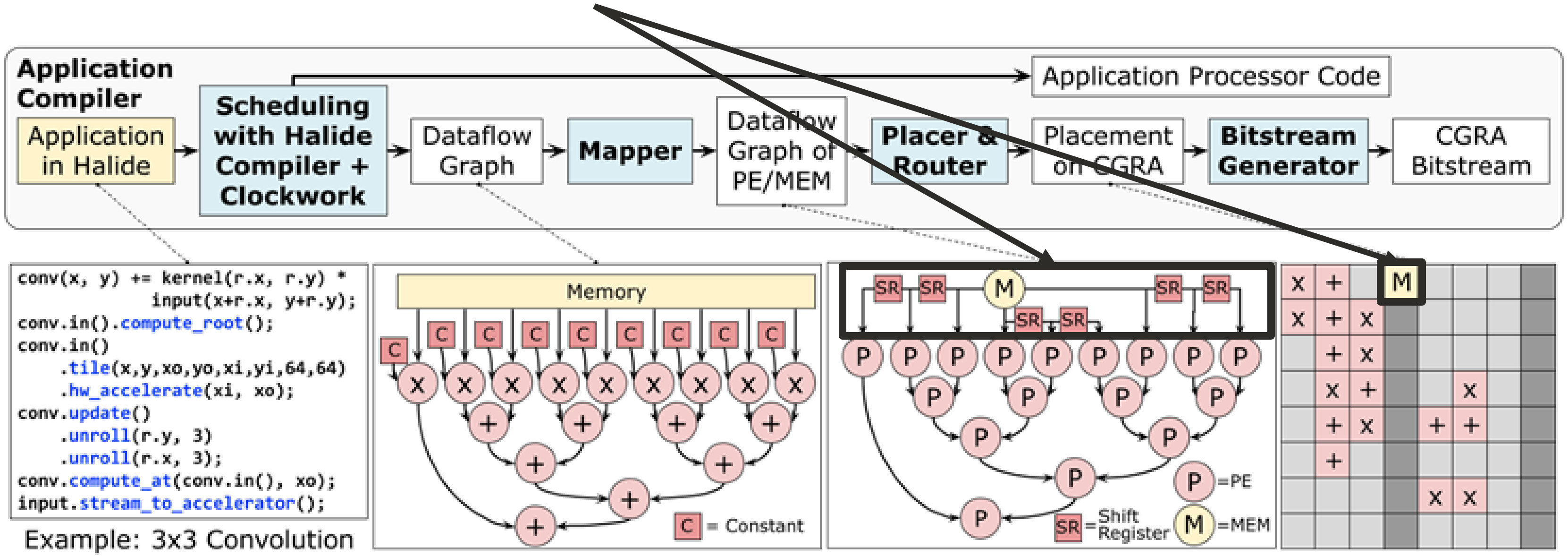

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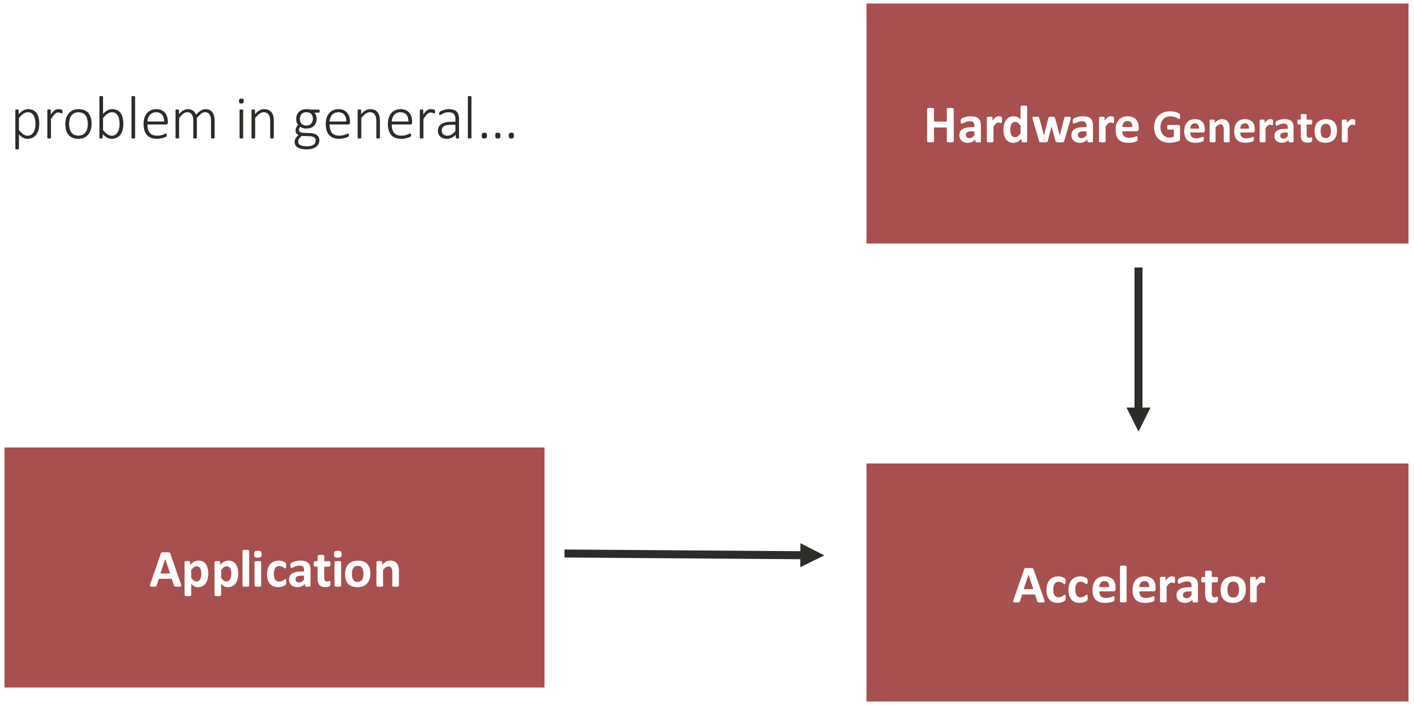
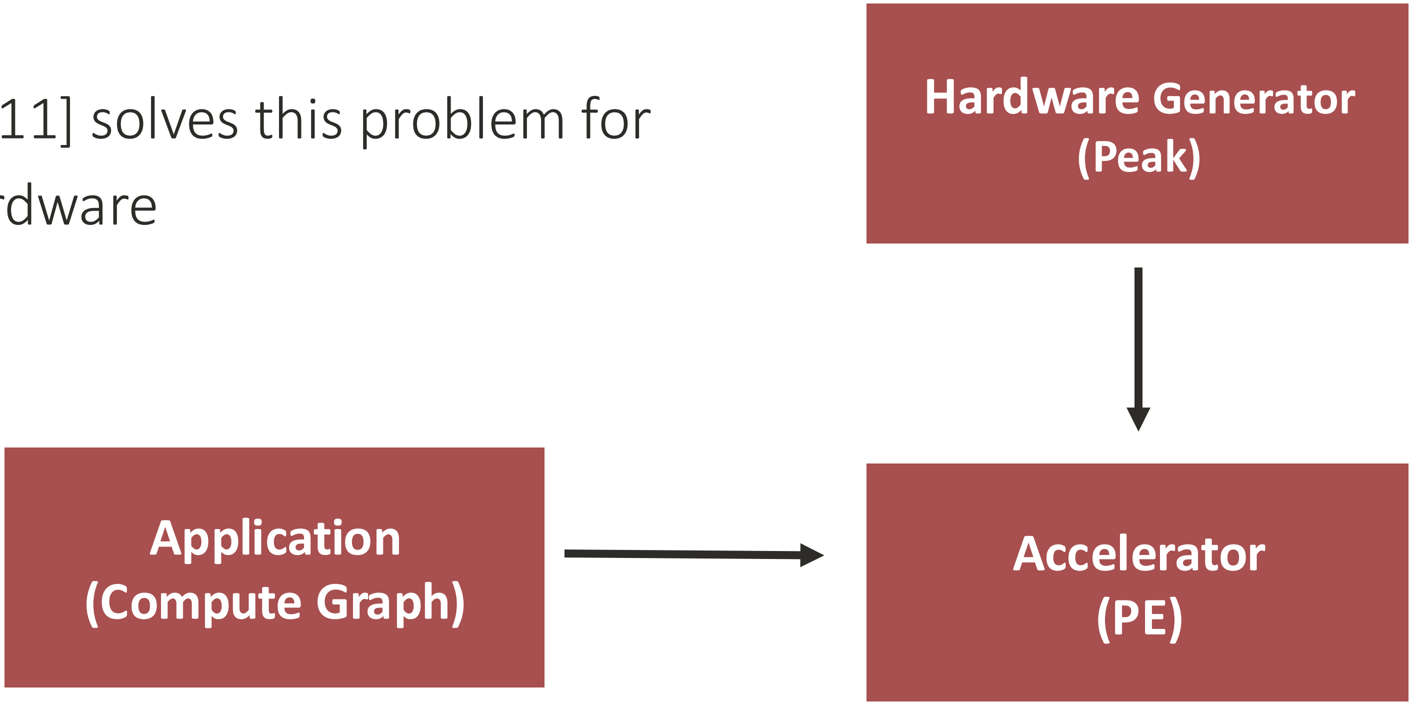
```

Tough problem in general…

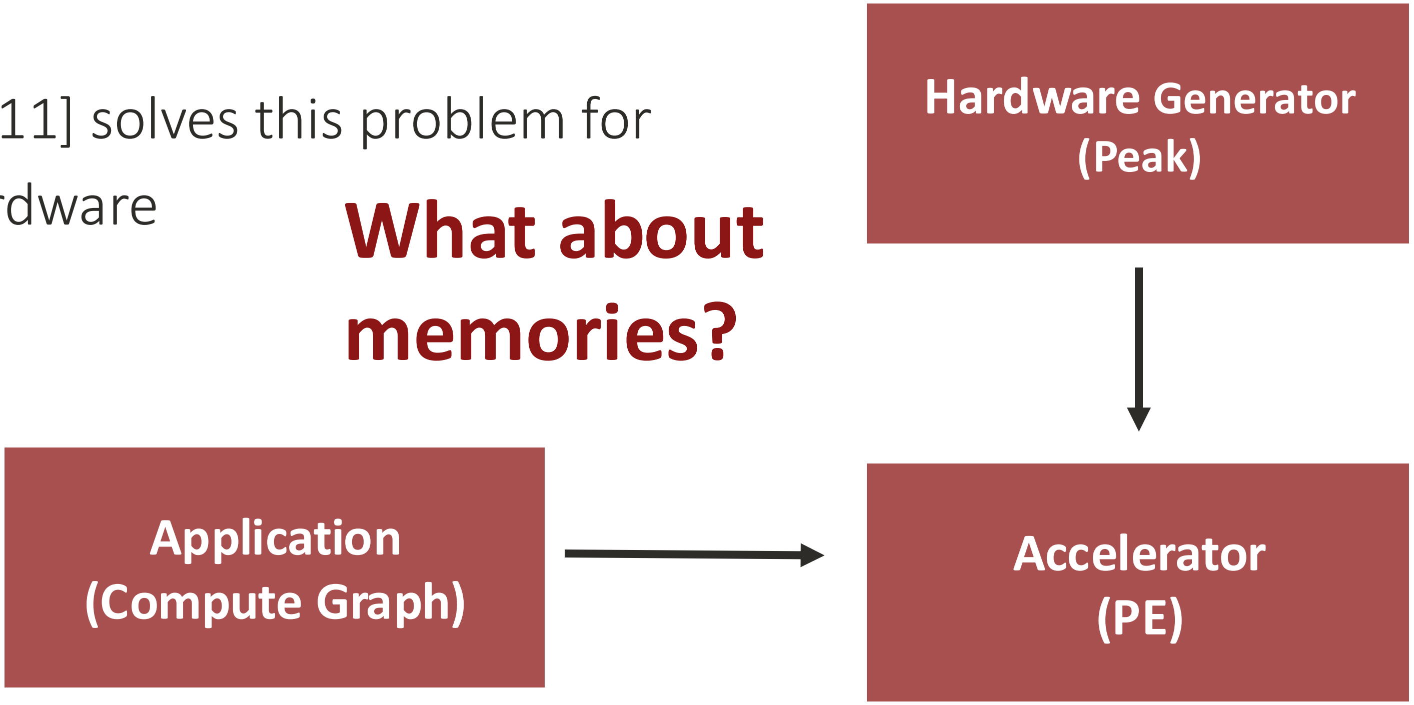


PEak [11] solves this problem for PE hardware



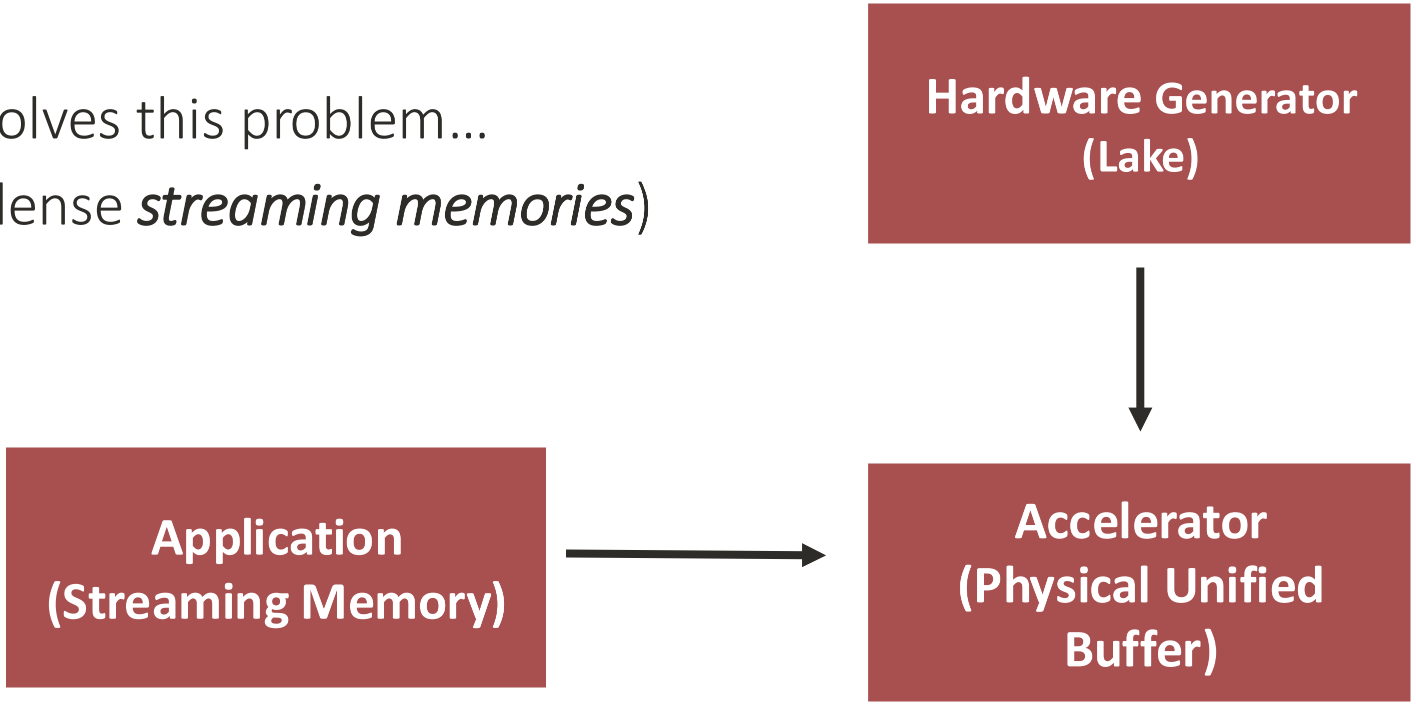
PEak [11] solves this problem for PE hardware

What about memories?



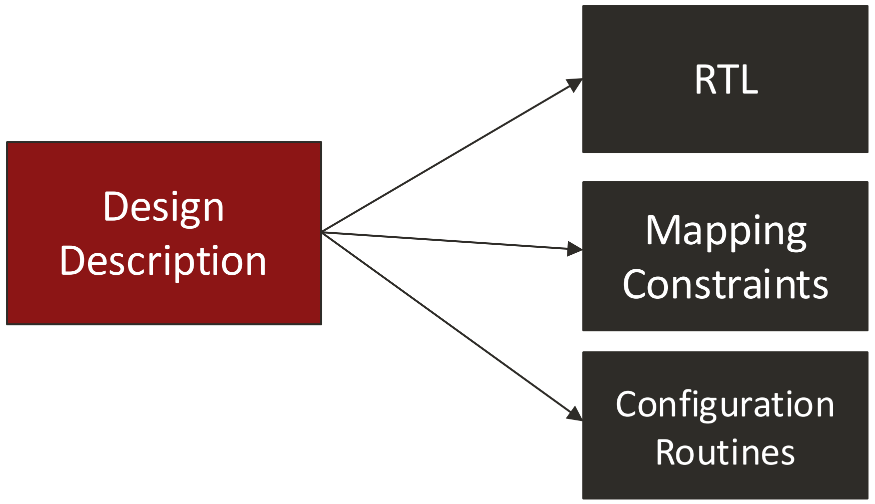
Lake solves this problem…

…for dense ***streaming memories***)


Hardware Generator (Lake)
Application (Streaming Memory)
Accelerator (Physical Unified Buffer)

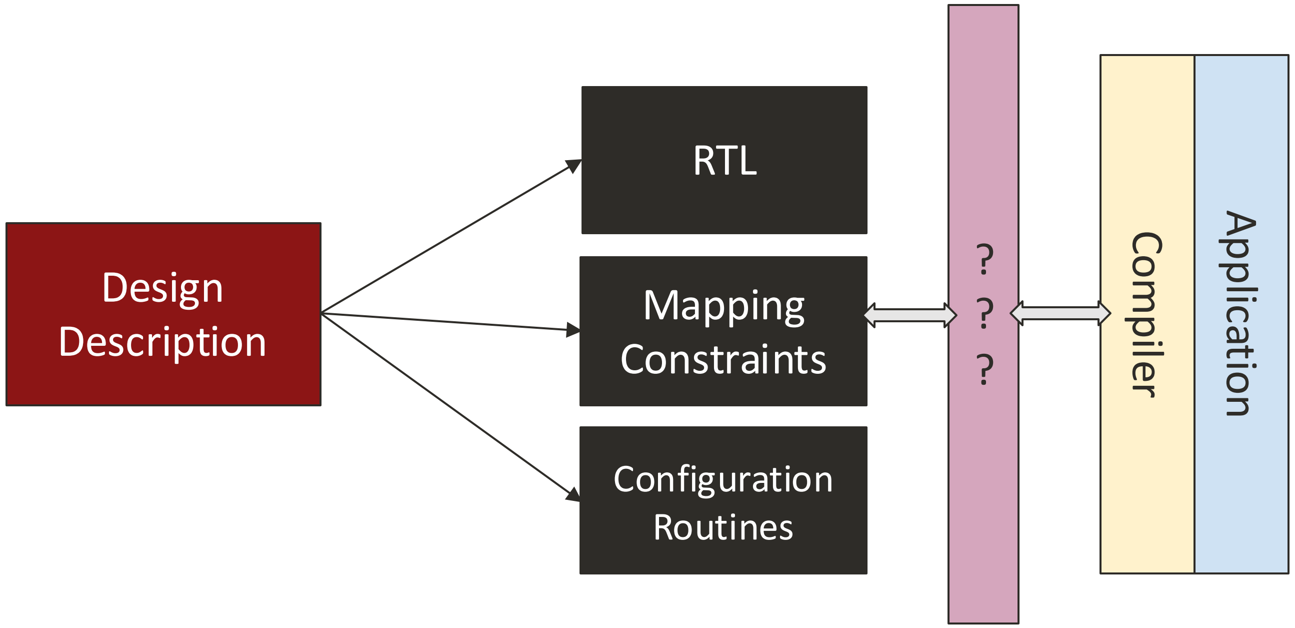
Single Source of Truth

- To enable automatic mapping and design-space exploration, it is crucial to generate mapping collateral from a single source of truth



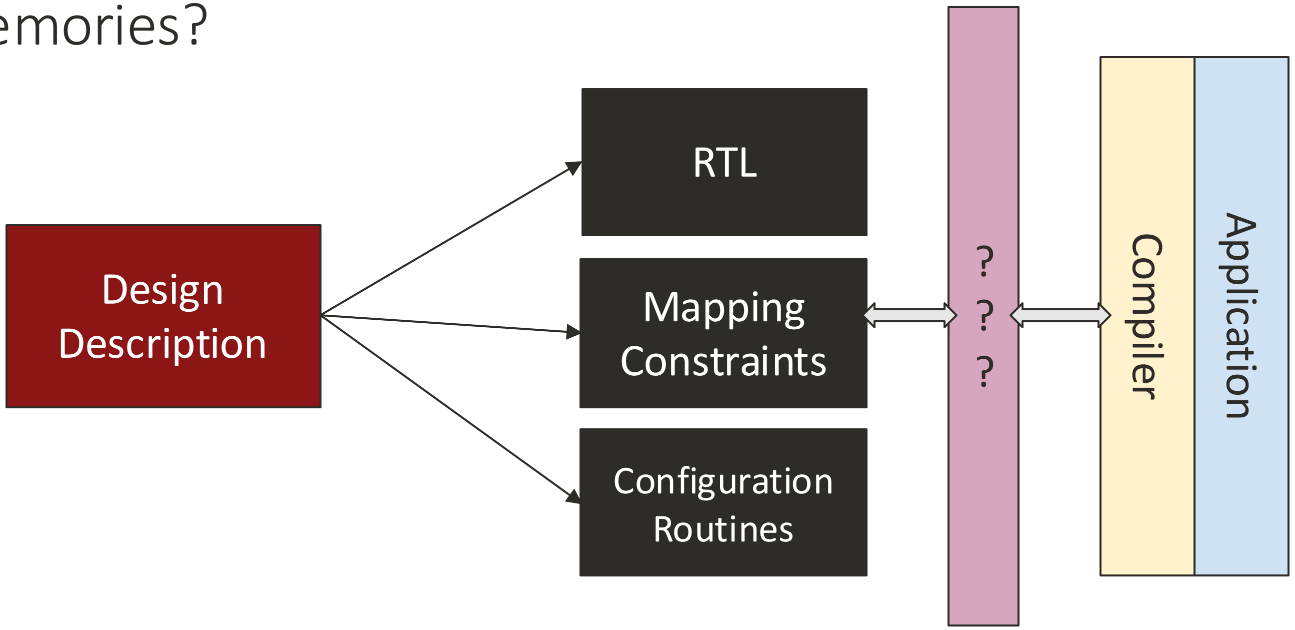
Need the Right Abstraction

- Maintaining compiler compatibility requires a stable HW/SW interface



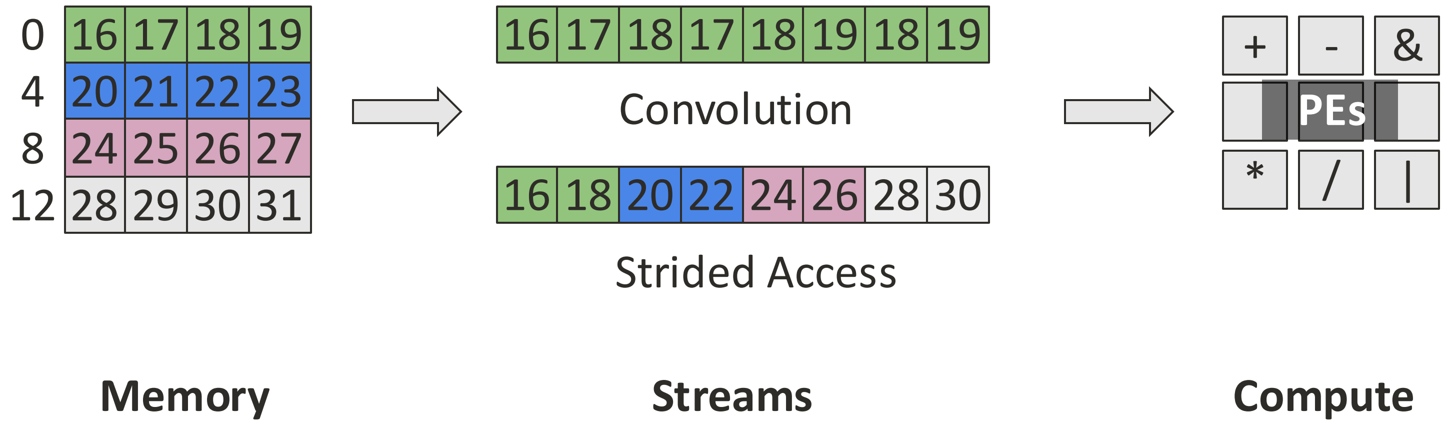
Need the Right Abstraction

- Maintaining compiler compatibility requires a stable HW/SW interface
- PEak used an ISA for PEs – what is analogous to an ISA for streaming memories?



Streaming Memories

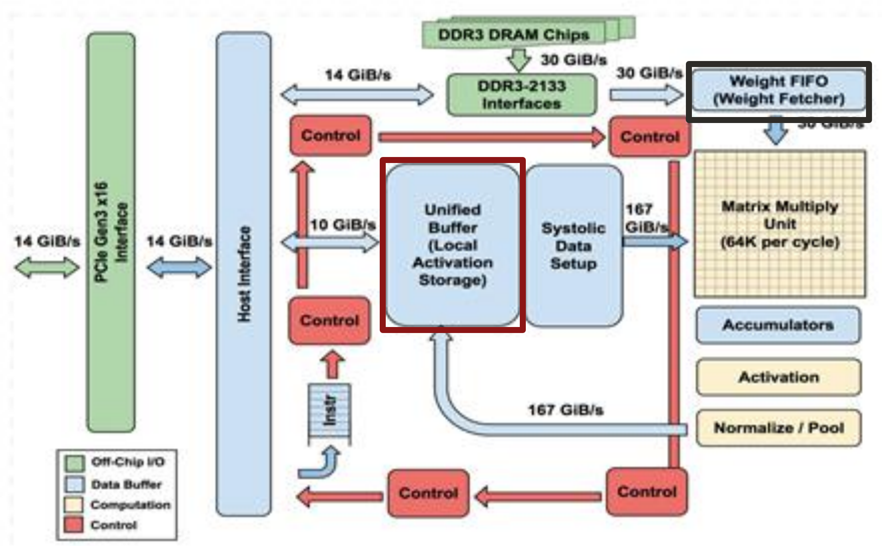
- Streaming memories ingest and emit (re)ordered streams of data to occupy large sets of compute units
  - Streaming memories have no data-dependent flow control



Streaming Memories

TPU [2]

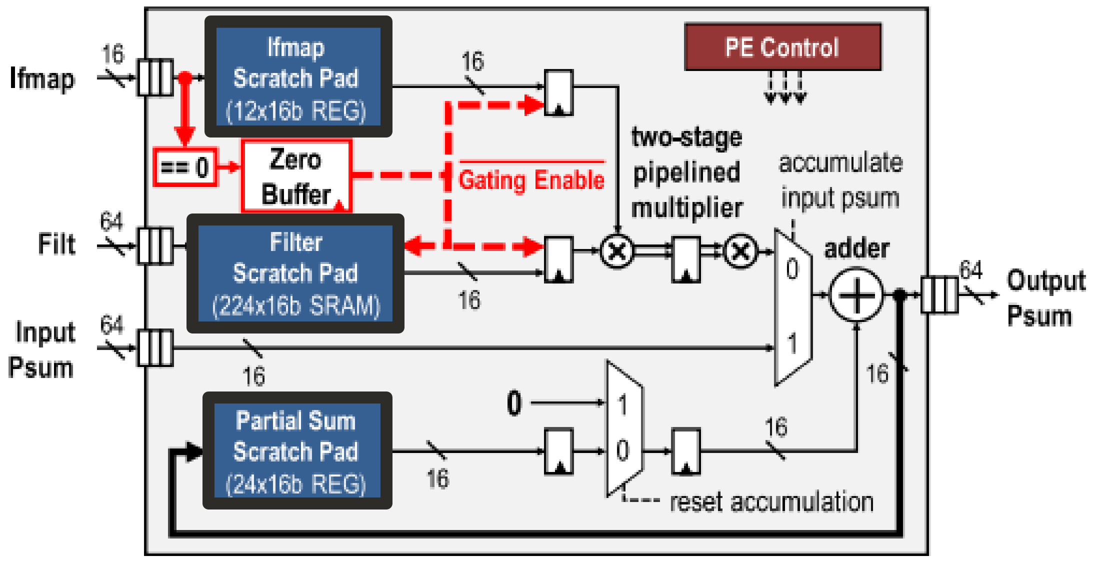
- Push memories used for activation storage, weight FIFO
- Custom compilation pathway (TensorFlow -> TPU Instructions)
- **Aggregate data and push through compute**



Streaming Memories

Eyeriss [5]

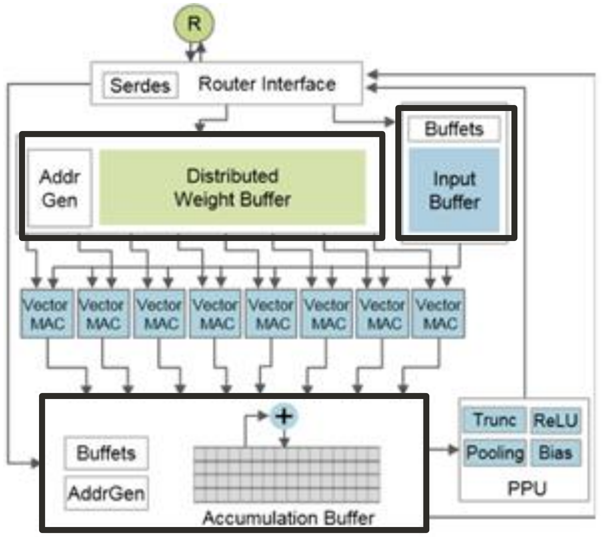
- Push memories for scratchpads
- Manual mapping to CNN parameters
- **Aggregate data and push through compute**



Streaming Memories

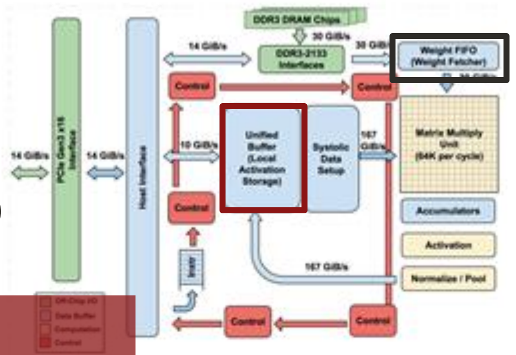
SIMBA PE [4]

- Push memories for inputs, weight buffer, accumulation buffer
- Caffe -> mapper + placer -> configuration binaries
- **Aggregate data and push through compute**



(c) Simba Processing Element

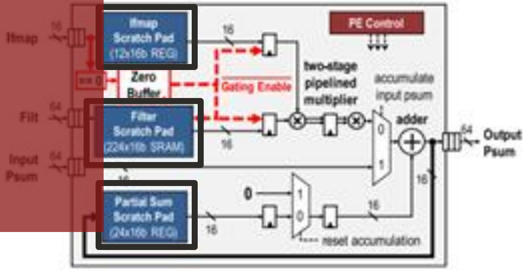
- TPU [2]
  - Push memories used for activation storage, weight FIFO
  - Custom compilation pathway (TensorFlow -> TPU Instructions)



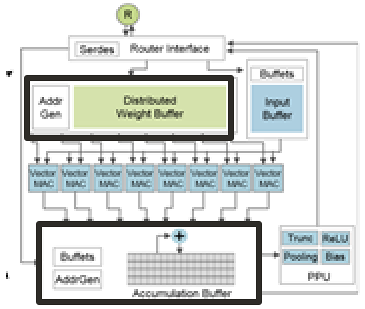
Three streaming memories

Three *different* compilers

- Eyeriss [5]
  - Push memories for scratchpads
  - Manual mapping to CNN parameters


Ifmap Scratch Pad (12x16b REG)
Filter Scratch Pad (224x16b SRAM)
Partial Sum Scratch Pad (24x16b REG)
PE Control
Zero Buffer
Gating Enable
two-stage pipelined multiplier
accumulate input psum
adder
Output Psum
reset accumulation

- SIMBA [4]
  - Push memories for inputs, weight buffer, accum buffer
  - Caffe -> mapper + placer -> configuration binaries



(c) Simba Processing Element

Unified Buffer [3] - Streaming Memory Abstraction

- Describes ***stream*** reorderings in space and time
  - Address sequences (space) to indicate reorderings
  - *Static schedule* sequences (time) to make sure all dependencies are obeyed

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
  for(x, 0, 64)
    blur(x, y) = (brighten(x, y) +
                  brighten(x, y+1)) / 2;
```

Example streaming memory application

- Easy to extract UB from IP/ML (streaming memory) applications

- Create a **Port** for each access statement in the original application
  - Iteration Domain
  - Address Sequence
  - Schedule Sequence

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Kernel Example

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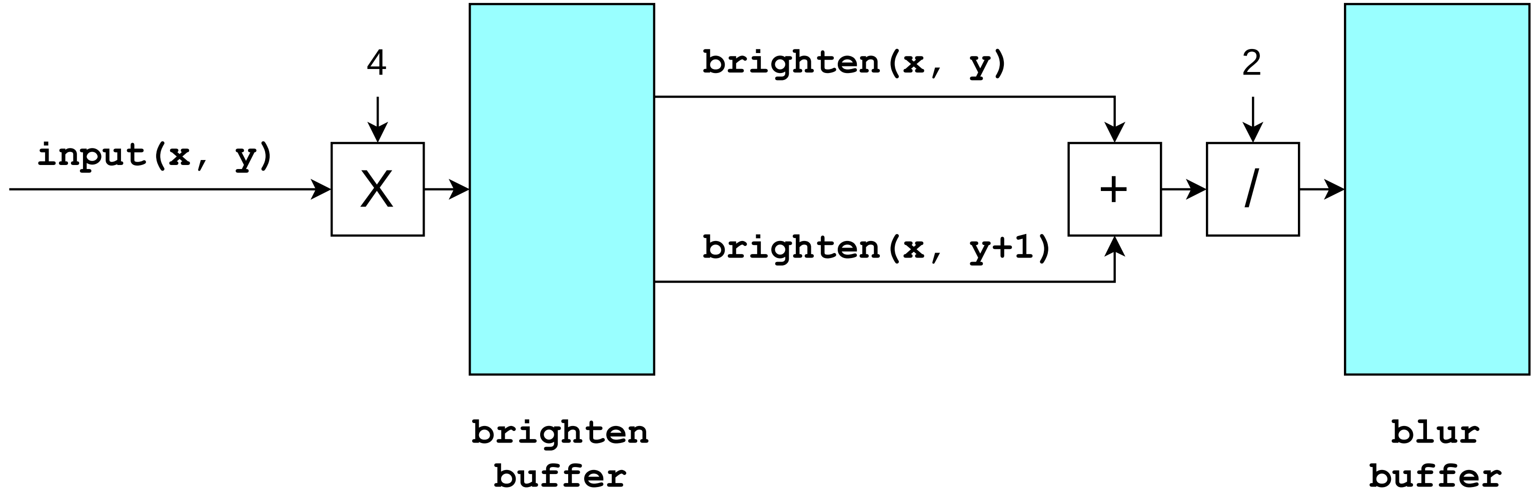

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```
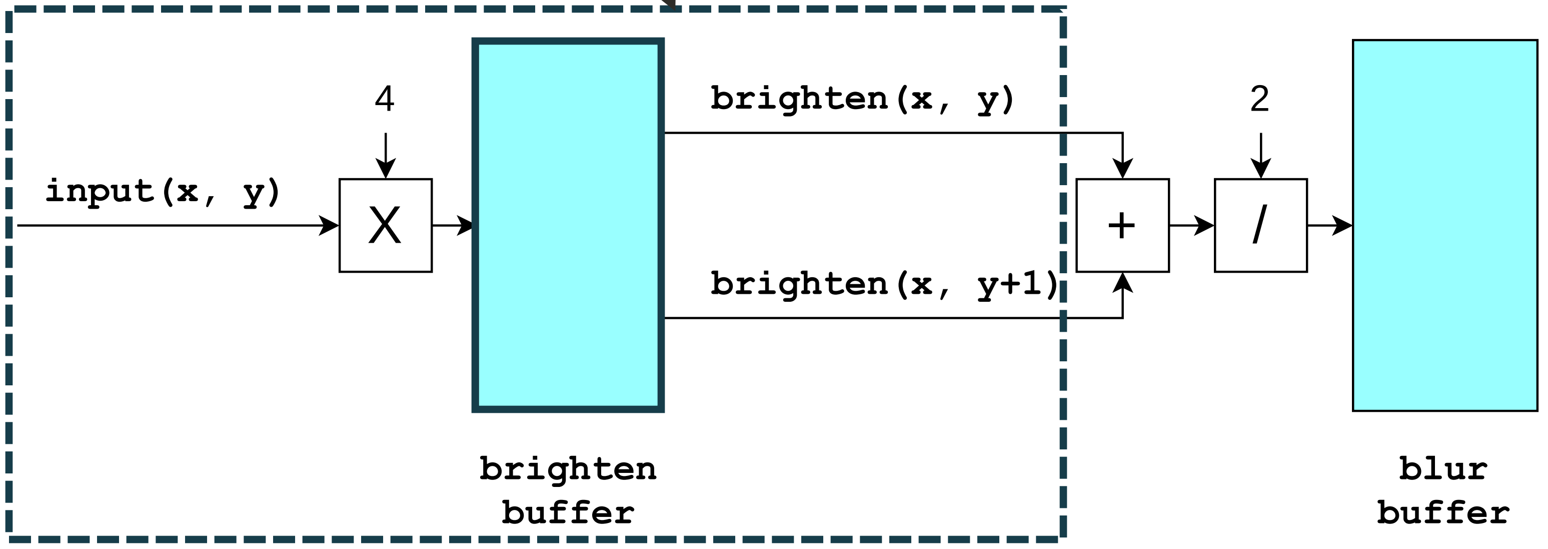

Extract the Unified Buffer for the **brighten** buffer



Kernel Example

One Port for each access statement

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
  for(x, 0, 64)
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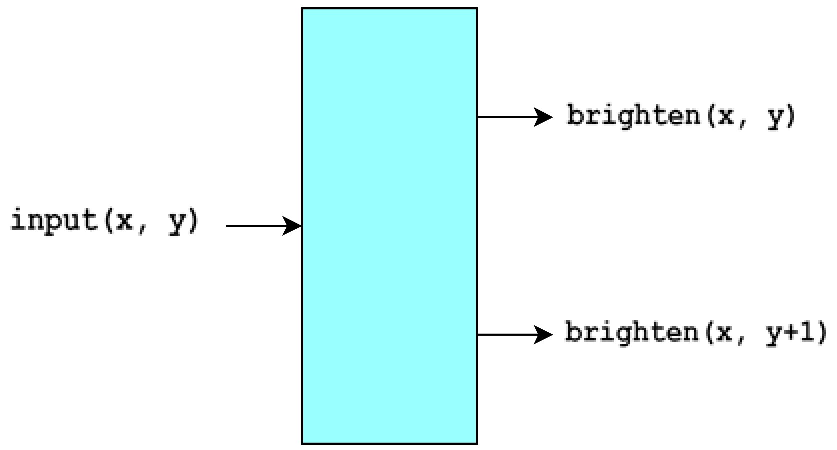

Unified Buffer Abstraction

Kernel Example

Assign each Port an Iteration Domain

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for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

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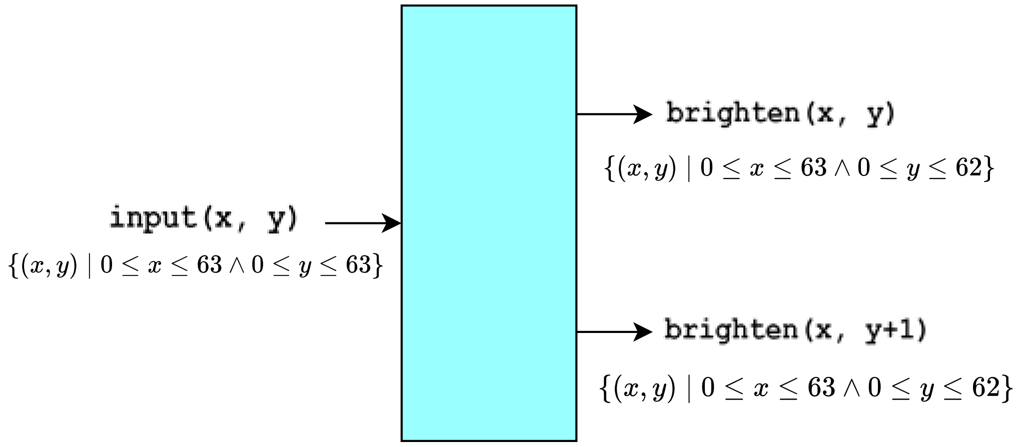
input(x, y)
$\{(x, y) \mid 0 \le x \le 63 \land 0 \le y \le 63\}$
brighten(x, y)
$\{(x, y) \mid 0 \le x \le 63 \land 0 \le y \le 62\}$
brighten(x, y+1)
$\{(x, y) \mid 0 \le x \le 63 \land 0 \le y \le 62\}$

Unified Buffer Abstraction

Kernel Example

Assign each Port an affine map from Iteration Domain to Address

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for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
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```

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten[64 * y + 1 * x + 0] = input * 4;
```

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Extents

```
for(y, 0, 64)
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    brighten[64 * y + 1 * x + 0] = input * 4;
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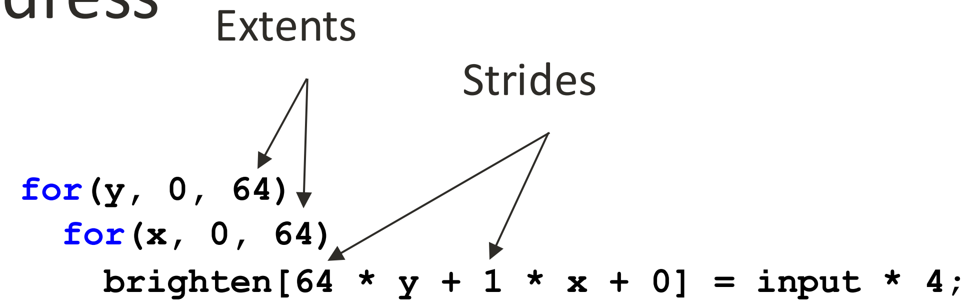

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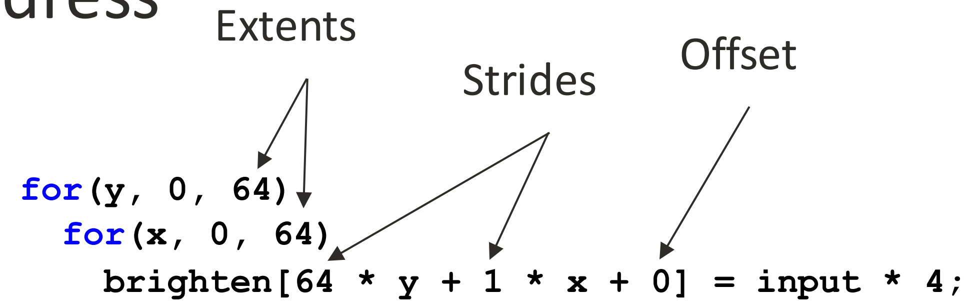

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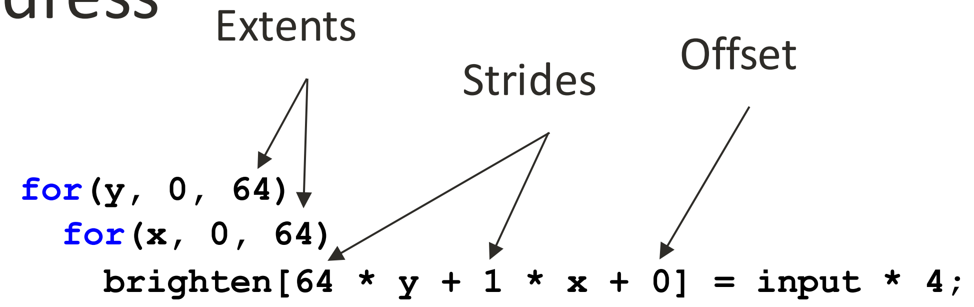

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for(y, 0, 64)
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Schedule:

As written (without optimizations), all reads occur after all writes

Kernel Example – Extracted UB

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

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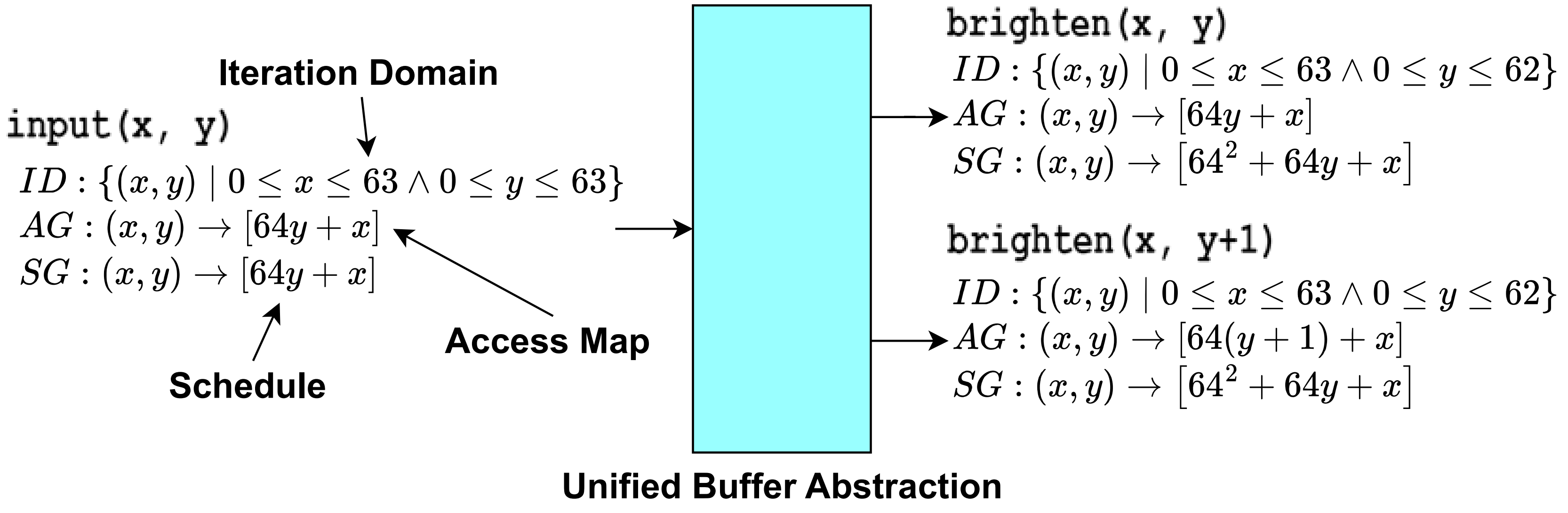

`input(x, y)`

$ID : \{(x, y) \mid 0 \leq x \leq 63 \wedge 0 \leq y \leq 63\}$

$AG : (x, y) \rightarrow [64y + x]$

$SG : (x, y) \rightarrow [64y + x]$

`brighten(x, y)`

$ID : \{(x, y) \mid 0 \leq x \leq 63 \wedge 0 \leq y \leq 62\}$

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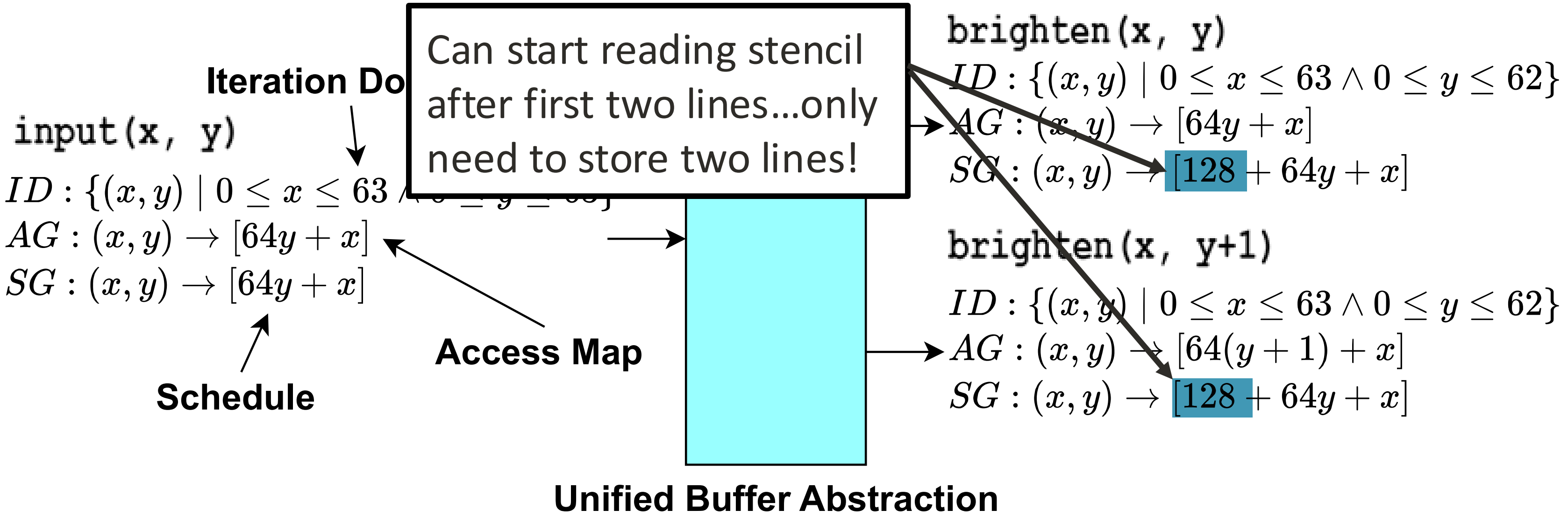

Can start reading stencil after first two lines…only need to store two lines!

`input(x, y)`

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$AG : (x,y) \to [64y + x]$
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`brighten(x, y)`

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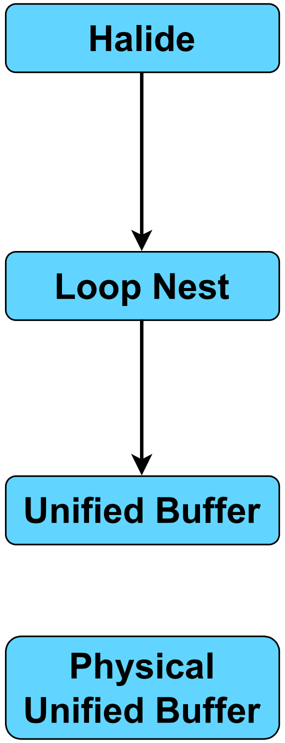
$AG : (x,y) \to [64y + x]$
$SG : (x,y) \to [128 + 64y + x]$

`brighten(x, y+1)`

$ID : \{(x,y) \mid 0 \le x \le 63 \wedge 0 \le y \le 62\}$
$AG : (x,y) \to [64(y+1) + x]$
$SG : (x,y) \to [128 + 64y + x]$

Compiler Flow



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blur.tile(x, y, xo, yo, xi, yi, 64, 63)
    .hw_accelerate(xi, xo);
brighten.store_at(blur, xo)
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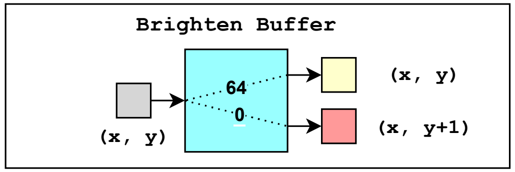
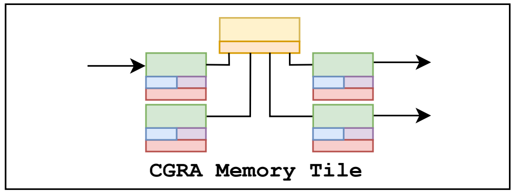
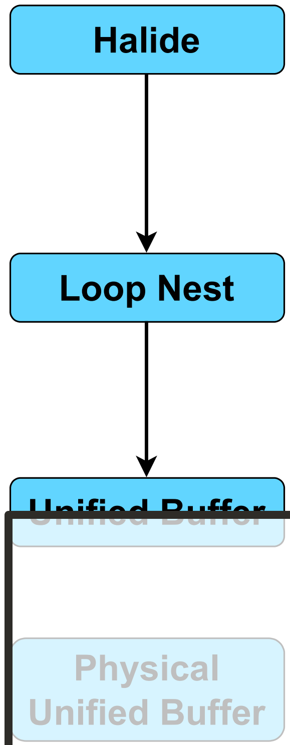
We know how to extract UBs!





Lake enables Unified Buffer mapping!



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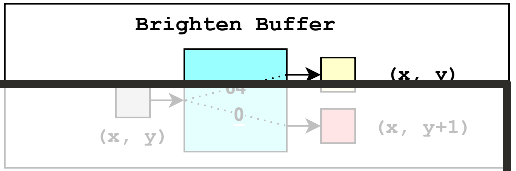
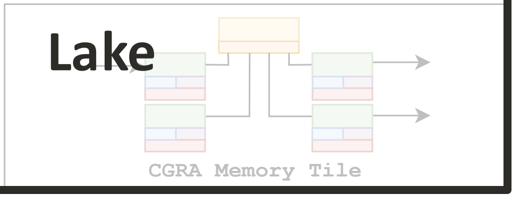
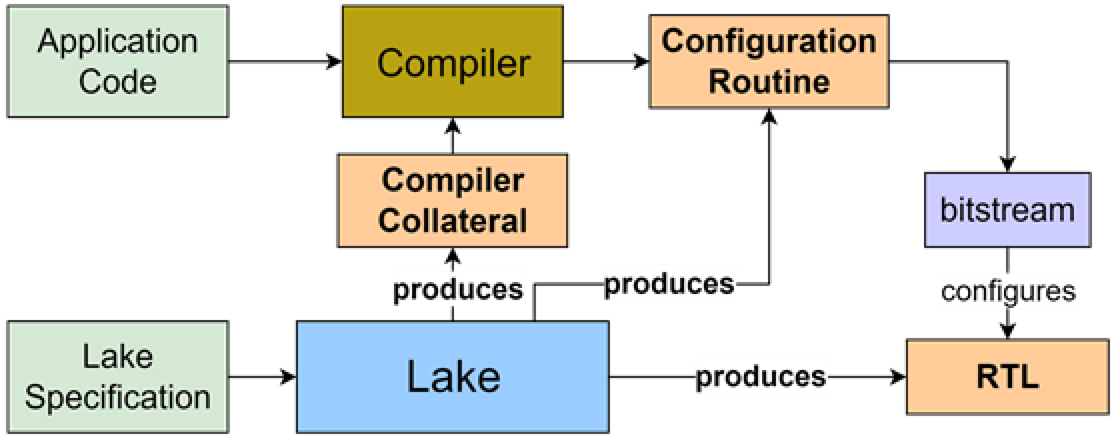




Use the UB abstraction to build RTL and program it

Lake System Overview

- Lake allows users to create physical implementations of Unified Buffers:
  - Hardware Generation (**RTL**)
  - Compiler Targetability (**Compiler Collateral**)
  - Bitstream Generation (**Configuration Routine**)



Lake Requirements

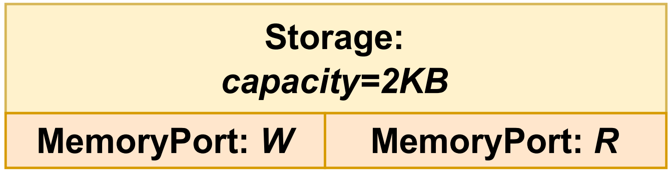
To create physical Unified Buffers (PUB) we need:

1. Type of Memory
   1. Capacity
   2. Memory Width
2. # and types of **Ports**
3. Capabilities of the controllers associated with each **Port**
4. Runtime paradigm (static or ready/valid)

Lake Components - 1

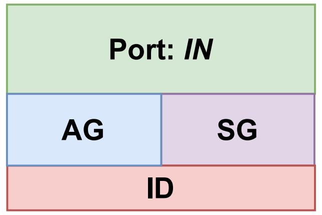
Define the memory system itself

- MemoryPort
  - Used to define physical interfaces to **Storage** element
  - Interface width
  - Type: R, W, R/W
- Storage
  - Actual storage (# bytes)
  - Real implementation will depend on attached **MemoryPorts**



Implied dual-port SRAM

Lake Components - 2



Define the **Ports**

1. Interface width
2. Type: IN, OUT
3. Buffering
   - Inserted when width mismatch with **MemoryPorts**

… and their associated capabilities

- **IterationDomain (ID)**
  1. Number of levels (nest depth)
  2. Maximum loop bounds

- **AddressGenerator (AG)**
  1. Maximum strides
  2. Maximum offset

- **ScheduleGenerator (SG)**
  1. Runtime
     1. Static
     2. Ready/Valid
  2. Maximum strides
  3. Maximum offset

Lake Specification

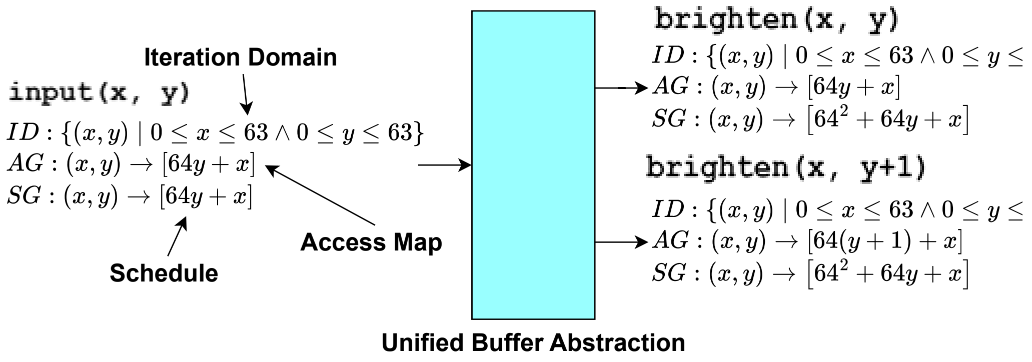
- Python library
  - Iterate over design space easily
  - Leverage OOP practices like inheritance
- Provide base static and ready/valid implementations
  - Users can write their own by overriding gen_hardware() and gen_bitstream()
  - Class interfaces guarantee proper interconnectivity
- Specify hardware topology through spec.connect()

Spec Example

- Consider applications when building the spec for the hardware
- Previous brighten kernel needed 3 **Ports**
  - Build a 4 **Port** memory design to map 2-4 **Port** applications
- Use wide, single-ported SRAM
  - Almost always use these for efficiency vs multi-ported SRAM

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
  for(x, 0, 64)
    blur(x, y) = (brighten(x, y) +
                  brighten(x, y+1)) / 2;
```


Iteration Domain
input(x, y)
$ID : \{(x,y) \mid 0 \leq x \leq 63 \wedge 0 \leq y \leq 63\}$
$AG : (x,y) \to [64y + x]$
$SG : (x,y) \to [64y + x]$
Schedule
Access Map
brighten(x, y)
$ID : \{(x,y) \mid 0 \leq x \leq 63 \wedge 0 \leq y \leq$
$AG : (x,y) \to [64y + x]$
$SG : (x,y) \to [64^2 + 64y + x]$
brighten(x, y+1)
$ID : \{(x,y) \mid 0 \leq x \leq 63 \wedge 0 \leq y \leq$
$AG : (x,y) \to [64(y+1) + x]$
$SG : (x,y) \to [64^2 + 64y + x]$
Unified Buffer Abstraction

Spec Example

- Consider applications when building the spec for the hardware
- Previous brighten kernel needed 3 **Ports**
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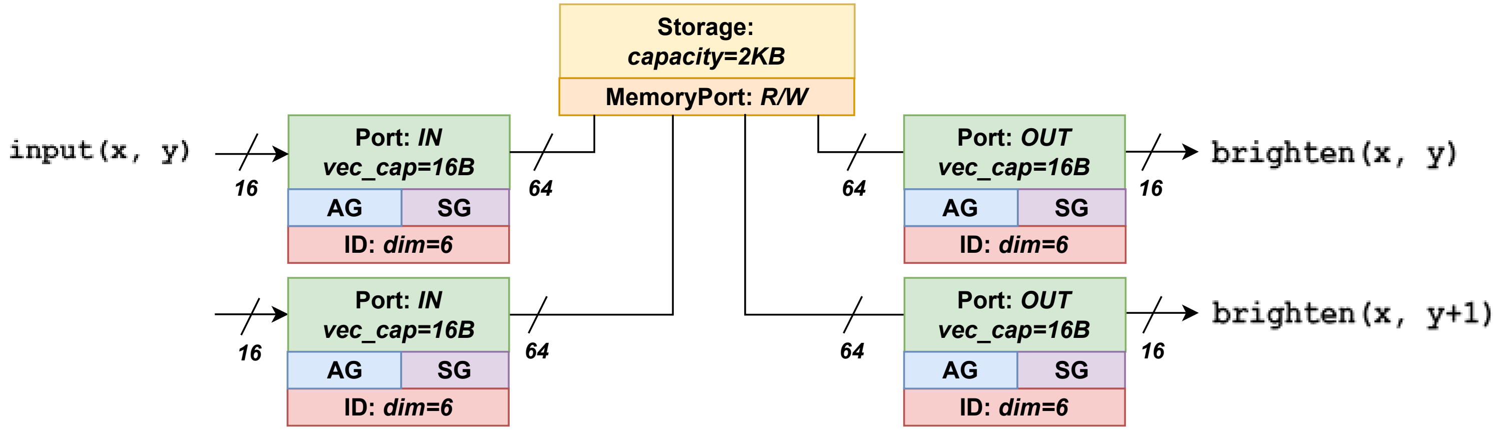
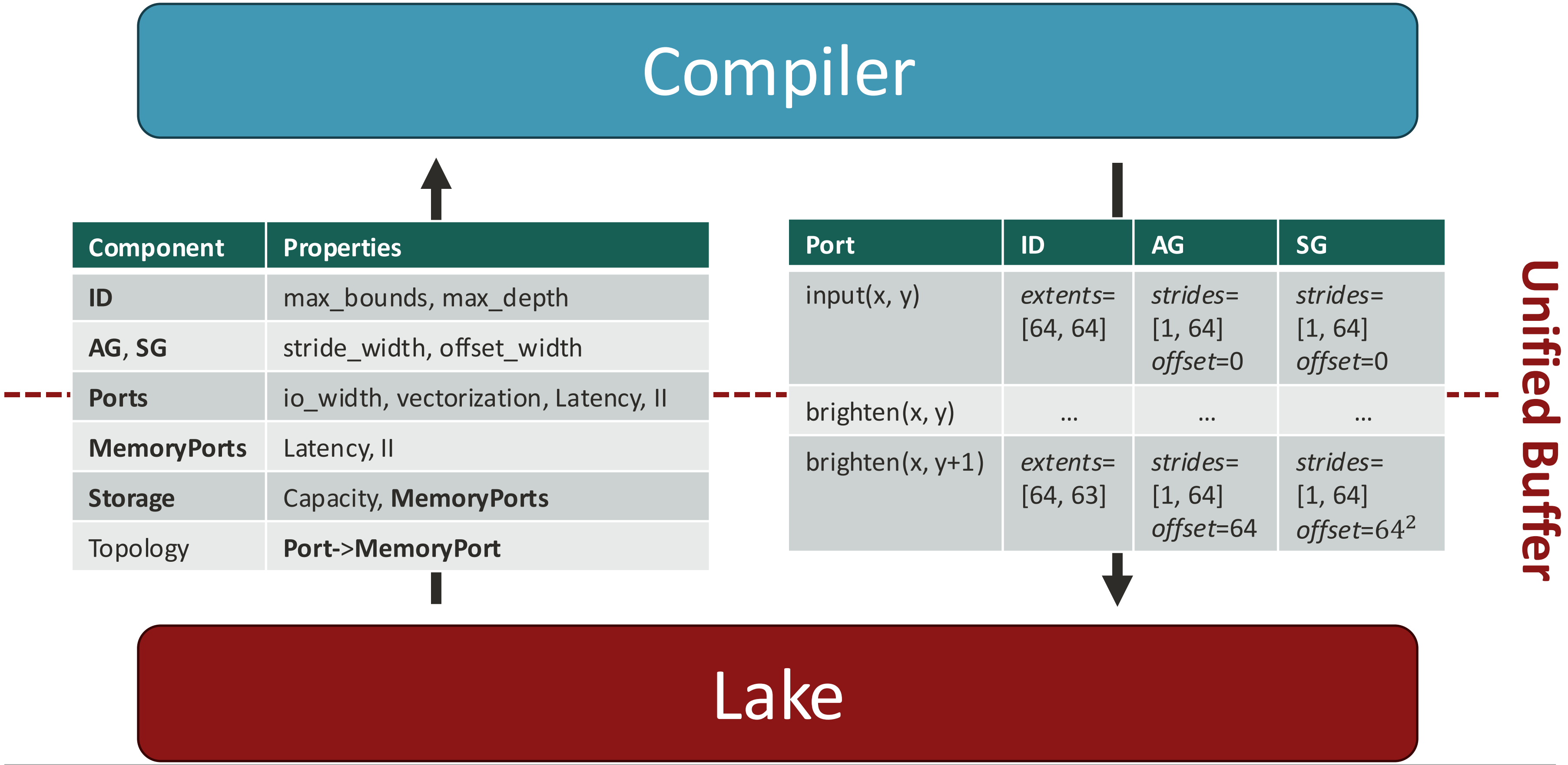


Compiler Collateral

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
  for(x, 0, 64)
    blur(x, y) = (brighten(x, y) +
                  brighten(x, y+1)) / 2;
```



Component	Properties
ID	max_bounds, max_depth
AG, **SG**	stride_width, offset_width
Ports	io_width, vectorization, Latency, II
MemoryPorts	Latency, II
Storage	Capacity, **MemoryPorts**
Topology	**Port->MemoryPort**

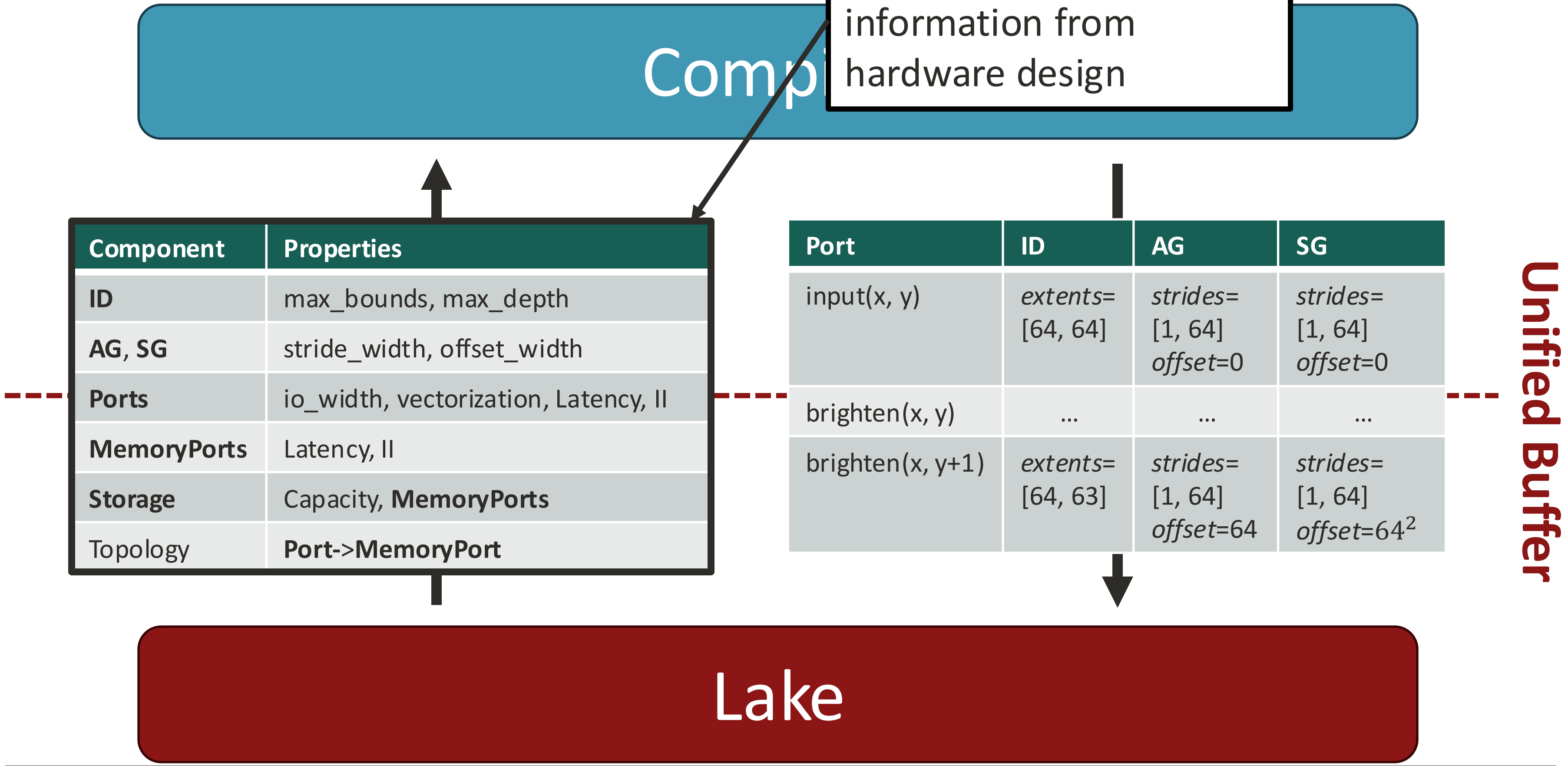
Port	ID	AG	SG
input(x, y)	*extents*= [64, 64]	*strides*= [1, 64] *offset*=0	*strides*= [1, 64] *offset*=0
brighten(x, y)	…	…	…
brighten(x, y+1)	*extents*= [64, 63]	*strides*= [1, 64] *offset*=64	*strides*= [1, 64] *offset*=64^2

Compiler Collateral

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

for(y, 0, 63)
  for(x, 0, 64)
                                   y) +
                                   y+1)) / 2;
```

Lake extracts UB-relevant information from hardware design



Component	Properties
ID	max_bounds, max_depth
AG, **SG**	stride_width, offset_width
Ports	io_width, vectorization, Latency, II
MemoryPorts	Latency, II
Storage	Capacity, **MemoryPorts**
Topology	**Port->MemoryPort**

Port	ID	AG	SG
input(x, y)	*extents*= [64, 64]	*strides*= [1, 64] *offset*=0	*strides*= [1, 64] *offset*=0
brighten(x, y)	…	…	…
brighten(x, y+1)	*extents*= [64, 63]	*strides*= [1, 64] *offset*=64	*strides*= [1, 64] *offset*=64^2

Compiler Collateral

```
for(y, 0, 64)
  for(x, 0, 64)
    brighten(x, y) = input(x, y) * 4;

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    blur(x, y) = (brighten(x, y) +
                  brighten(x, y+1)) / 2;
```
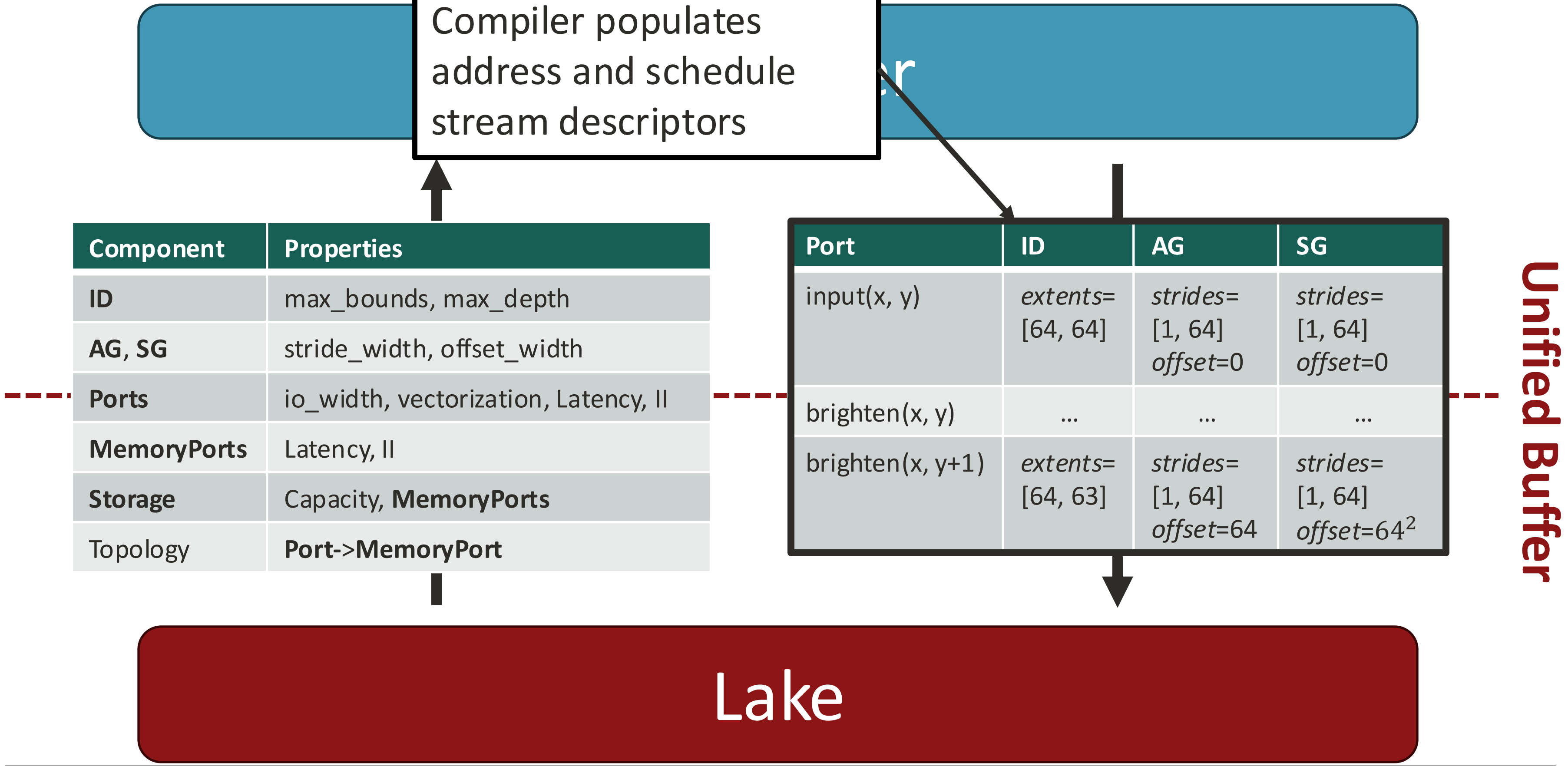



Compiler populates address and schedule stream descriptors

Component	Properties
ID	max_bounds, max_depth
AG, **SG**	stride_width, offset_width
Ports	io_width, vectorization, Latency, II
MemoryPorts	Latency, II
Storage	Capacity, **MemoryPorts**
Topology	**Port->MemoryPort**

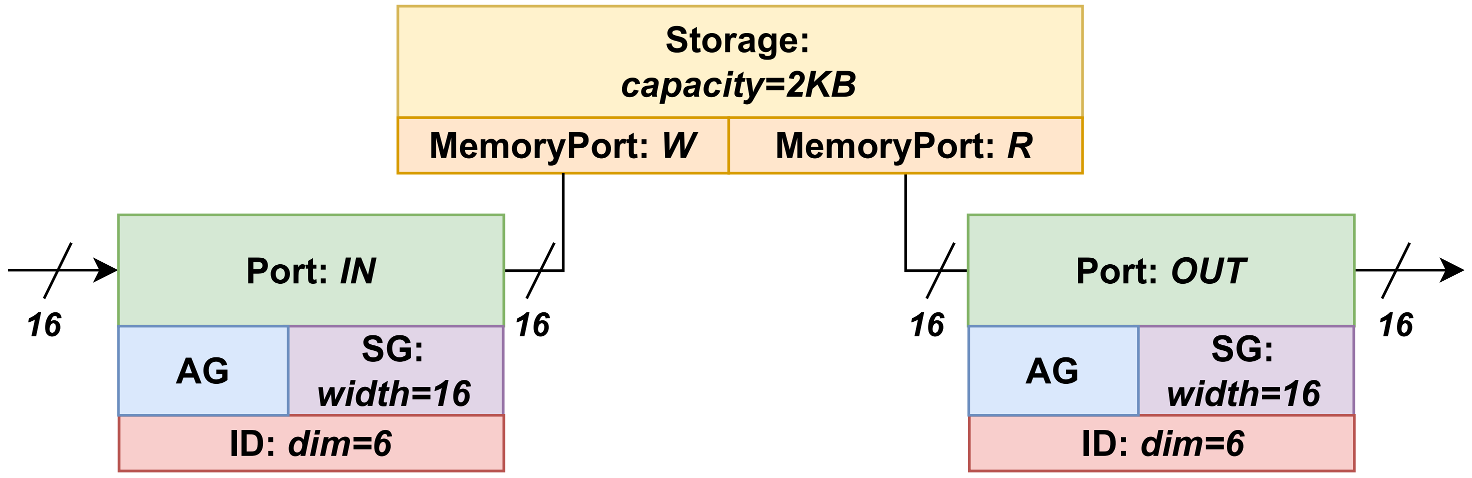
Port	ID	AG	SG
input(x, y)	*extents*= [64, 64]	*strides*= [1, 64] *offset*=0	*strides*= [1, 64] *offset*=0
brighten(x, y)	…	…	…
brighten(x, y+1)	*extents*= [64, 63]	*strides*= [1, 64] *offset*=64	*strides*= [1, 64] *offset*=64^2

Lake Summary

- Lake is a single-source-of-truth generator for ***streaming*** memories
    - RTL
    - Compiler Mapping Constraints
    - Configuration Routines
- Used Lake to build memories in multiple CGRAs
- Choosing the right abstraction (Unified Buffer) can be critical for automation

Demo - Overview

- Create a 1-input, 1-output memory tile with a dual-port SRAM



Demo – File Structure

/aha/lake

- MICRO24_WS
  - simple_dual_port.py
  - demo_driver.py

Use demo_driver.py to generate collateral

Specification already written in simple_dual_port.py

Demo - Specification

- First, we need to write the specification

```
# 1. Initialize the spec...
ls = Spec()
# 2. Define Ports (and register them)
in_port = Port(ext_data_width=data_width,
                            direction=Direction.IN)
out_port = Port(ext_data_width=data_width,
                             direction=Direction.OUT)
ls.register(in_port, out_port)
```

Demo - Specification

```
# 3. Define ID, AG, SG for each Port (and register them)
in_id = IterationDomain()
in_ag = AddressGenerator()
in_sg = ScheduleGenerator()
out_id = IterationDomain()
out_ag = AddressGenerator()
out_sg = ScheduleGenerator()
ls.register(in_id, in_ag, in_sg)
ls.register(out_id, out_ag, out_sg)
```

Demo - Specification

```
# 4. Define the Storage and its MemoryPorts
#    (and register them)

stg = SingleBankStorage(capacity=storage_capacity)

wr_mem_port = MemoryPort(data_width=data_width,
                         mptype=MemoryPortType.W, delay=1)

rd_mem_port = MemoryPort(data_width=data_width,
                         mptype=MemoryPortType.R, delay=1)

ls.register(stg, wr_mem_port, rd_mem_port)
```

Demo - Specification

```
# 5. Connect registered Components (Topology)
# In to In
ls.connect(in_port, in_id)
ls.connect(in_port, in_ag)
ls.connect(in_port, in_sg)
# Out to Out
ls.connect(out_port, out_id)
ls.connect(out_port, out_ag)
ls.connect(out_port, out_sg)
# In and Out to MemoryPorts
ls.connect(in_port, wr_mem_port)
ls.connect(out_port, rd_mem_port)
# MemoryPorts to Storage
ls.connect(wr_mem_port, stg)
ls.connect(rd_mem_port, stg)
```

Demo – Generate Collateral

- Once we've done that, we can generate the Verilog by calling its function

```
simple_dual_port_spec.get_verilog(output_dir=output_dir_verilog)
```

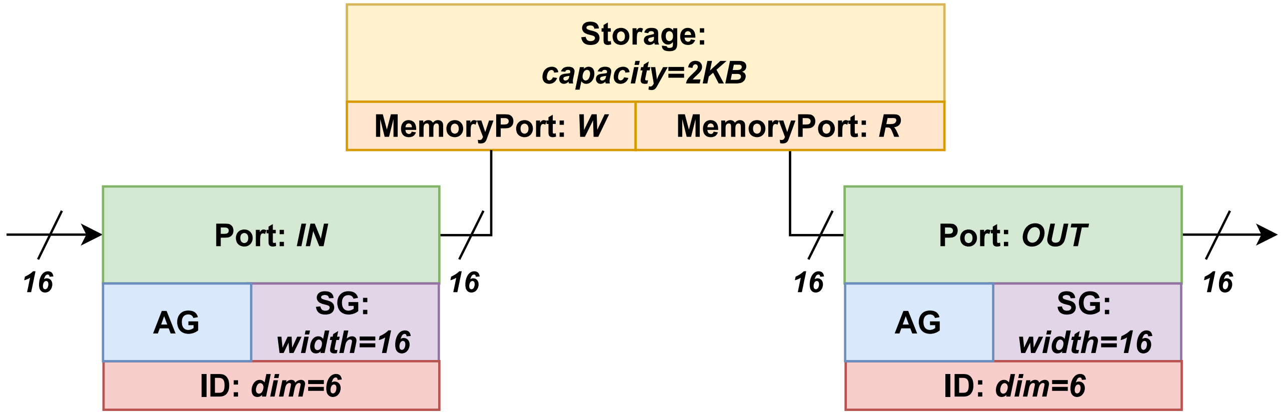
- We can also generate the bitstream for a test – given the schedule from the compiler (handwritten in this case)

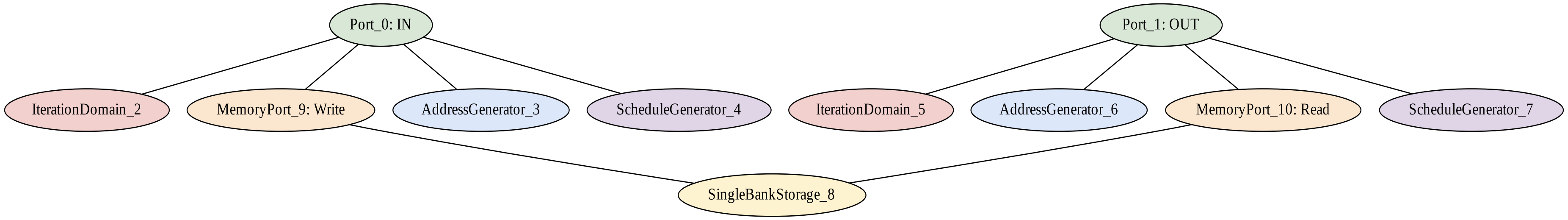
```
bs = simple_dual_port_spec.gen_bitstream(lt)
```

```
cd /aha/lake
python MICRO24_WS/demo_driver.py --outdir LAKE_TEST --visualize
```

- View graph representation in ./LAKE_TEST/simple_dual_port.png

Demo - Visualization



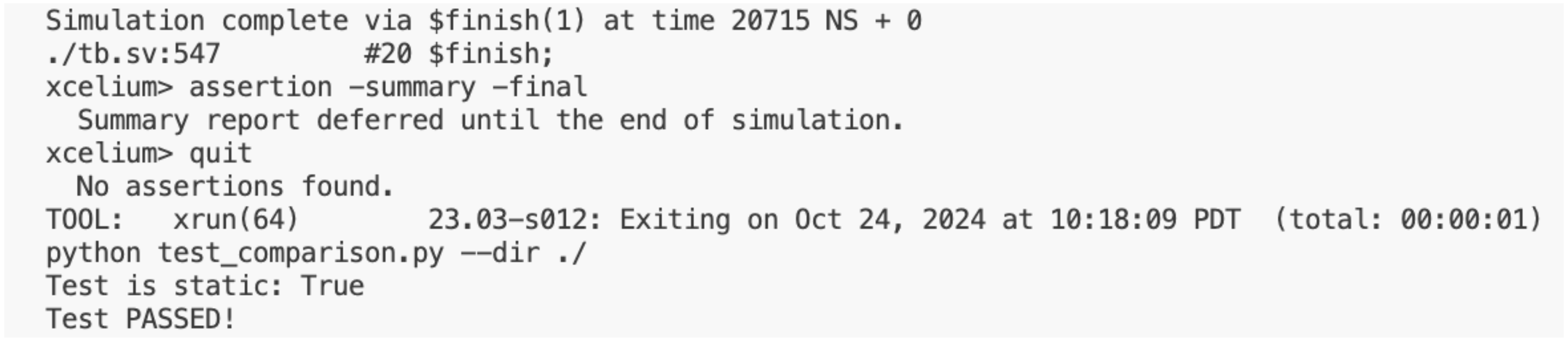


Demo – Run a Test

- Then we can run that test and verify our results!

```
cd LAKE_TEST
# optionally set WAVEFORM
export WAVEFORM=1
make sim
```

- The test passes against the gold schedule



```
Simulation complete via $finish(1) at time 20715 NS + 0
./tb.sv:547         #20 $finish;
xcelium> assertion -summary -final
  Summary report deferred until the end of simulation.
xcelium> quit
  No assertions found.
TOOL:   xrun(64)        23.03-s012: Exiting on Oct 24, 2024 at 10:18:09 PDT  (total: 00:00:01)
python test_comparison.py --dir ./
Test is static: True
Test PASSED!
```

Thank You

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Backup

Stanford University