XUANTIE 玄铁

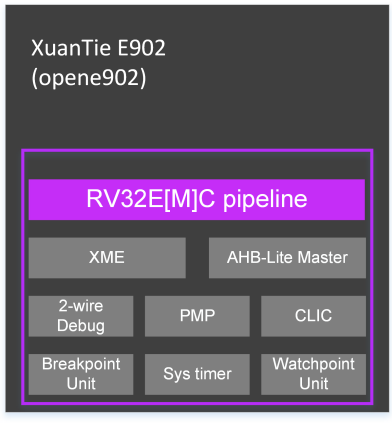
Ultra low power RISC-V processor



XuanTie E902 Datasheet

Overview

The XuanTie E902 (opene902) is a fully synthesizable, microcontroller-class processor compatible to the RISC-V RV32EMC ISA. It delivers ultra-low area and power aiming at entry-level MCUs and IoT applications.



Features

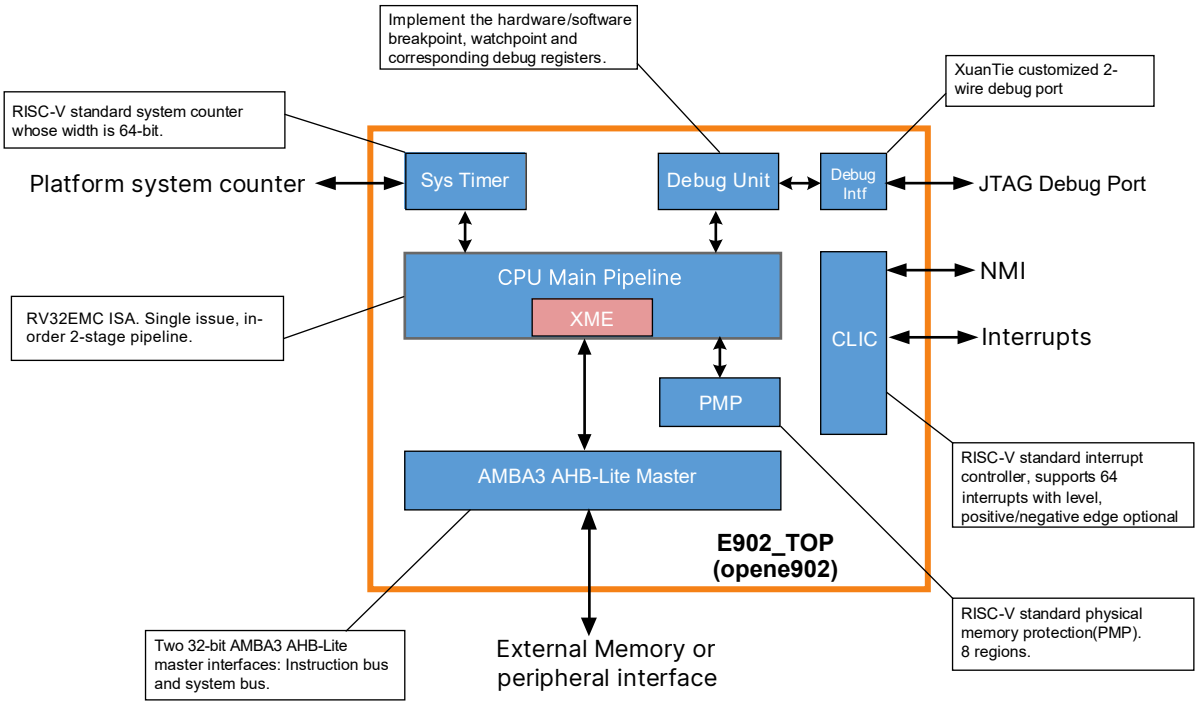
Feature	Description
Architecture	RV32EMC
Pipeline	2 stages
Bus Interface	AMBA3 AHB-Lite 32-bit master
Interrupts	64 interrupts + Non-maskable interrupt (NMI)
Sleep Modes	Sleep and deep sleep mode
Debug	2-wire/JTAG debug port, hardware and software breakpoints

XuanTie E902 Components

- Processor Overview

The E902 processor adopts a 16-/32-bit mixed instruction set and implements an energy-efficient 2-stage, single issue and in-order execution integer pipeline. Besides, E902 customizes four functional instructions and some extend CSRs to support the extensions.

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Physical Memory Protection (PMP)

The E902 processor has implemented RISC-V PMP, which allows machine and user privilege modes to access different address ranges. Only the machine mode has the authority to define the memory access permissions. The PMP has the following features:

- ◇ Supports 8 regions;
- ◇ Read/Write/Execution memory protection;
- ◇ Minimum 4KB address range.

Core Local Interrupt Controller (CLIC)

The E902 processor implements the RISC-V standard interrupt controller, CLIC and the CLINT. The CLIC has following features:

- ◇ Support 64 external interrupts;
- ◇ 8 priority settings;
- ◇ Support level or positive/negative edge interrupt types;
- ◇ Support hardware vector interrupt;
- ◇ The control registers are memory mapped.

Debug Components

The E902 processor adopts XuanTie customized 2-wire debug port to communicate between the host and the debug unit. The debug unit supports the following operations:

- ◇ Support hardware/software breakpoint;
- ◇ Support hardware watchpoint;
- ◇ Check and modify CPU register resource;
- ◇ Single step or multi step flexibly supported;
- ◇ Speed up program download through 2-wire debug port or standard JTAG port.

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- Interfaces

The E902 has two 32-bit AMBA3 AHB-Lite master interfaces to communicate with the external memory or peripheral IP which are instruction and system bus. The internal requests can be allocated to either bus according to the address.

- XuanTie MCU Enhanced Extensions (XME)

The E902 processor implements the XME to deliver more powerful features such as:

◇ Support NMI;
◇ Support Lockup;
◇ Support sleep and deep sleep;
◇ Support soft reset operation;
◇ Support configurable reset address through top port during integration;
◇ Extend four instructions to cover I-cache and sync operations.

Processor Configuration Options

The XuanTie E902 processor (opene902) has been configured as below:

Feature	Options
Architecture	RV32EMC
Hardware Multiplier	Shift-add multiplier (small area)
Interrupts	64
PMP	8 regions
Hardware Breakpoints	4
Debug Port	XuanTie 2-wire debug port

Software Ecosystems

◇ Compiler, assembler, linker, debugger and binary tools are contributed to GNU and supported officially;
◇ QEMU is contributed and supported officially;
◇ Code size optimized runtime lib
◇ Integrated Development Environment (CDK);
◇ High speed of program download (~1.1MB/s).

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