Allwinner Technology

A20

Datasheet

Revision 1.5
Apr 06, 2015

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Allwinner Technology Co., Ltd.

No.9 Technology Road 2,High-Tech Zone

Zhuhai, Guangdong Province, China

Contact Us: service@allwinnertech.com

Home Page: www.allwinnertech.com

Revision History

Revision	Date	Description
1.0	Feb 27, 2013	Initial version
1.1	March 21, 2013	Revize the logo
1.2	May 10, 2013	Revize VDD-RTC to 1.3V
1.3	Oct 16, 2013	Modify the recommended operating condition section
1.4	Dec 30, 2013	Add T_J and θ_{JC}
1.5	Apr 06, 2015	Modify the power up and down sequence

Table of Contents

1 OVERVIEW

Allwinner A20 processor is a dual-core ARM Cortex-A7 mobile application solution designed for tablet and smart TV applications.

A20 is based on a dual-core ARM Cortex-A7 CPU architecture, and integrates the powerful ARM Mali400 MP2 GPU, delivering a reliable system performance as well as good game compatibility. Besides,A20 supports 2160p video decoding and H.264 HP 1080p video encoding.

Additionally, A20 processor features a wide range of interfaces and connectivity, including 4-CH CVBS in, 4-CH CVBS out, HDMI with HDCP, VGA, LVDS/RGB LCD, SATA, USB, and GMAC, etc. More importantly, A20 processor is pin-compatible with its predecessor A10, which greatly simplifies the product design process and makes the upgrade of a design much easier.

2 FEATURES

Dual-Core CPU

- Dual Cortex-A7
  - –ARMv7 ISA standard ARM instruction set
  - –Thumb-2
  - –Jazeller RCT
  - –NEON Advanced SIMD
  - –VFPv4 floating point
  - –Hardware virtualization support
  - –Large Physical Address Extensions(LPAE)
  - –JTAG debug
  - –One general timer for individual CPU
  - –32KB Instruction and 32KB Data L1 Cache for individual CPU

Graphic Engine

- 3D
  - –Mali400 MP2 GPU
  - –Support OpenGL ES 2.0 / OpenVG 1.1 standard
- 2D
  - –Support BLT and ROP2/3/4
  - –Support 90° /180° /270° rotation
  - –Support mirror/ alpha (plane and pixel alpha) / color key
  - –Format conversion: ARGB 8888/4444/1555, RGB565, MONO 1/2/4/8bpp, Palette 1/2/4/8bpp (input only), YUV 444/422/420

Memory

- Internal BROM
  - –Support system boot from NAND Flash, SPI Nor Flash (SPI0), SD Card/TF card (SDC0/2)
  - –Support system code download through USB OTG (USB0)
- SDRAM
  - –Support DDR3/DDR3L/DDR2
  - –Support 32-bit bus width
  - –Support 2GB address space
- NAND Flash
  - –Comply to ONFI 2.3 and Toggle 1.0
  - –Support 64 bits ECC per 512 bytes or 1024 bytes
  - –Support 8bits data bus width
  - –Support 1K/2K/4K/8K/16K page size
  - –Support up to 8 CE and 2 RB
  - –Support system boot from NAND flash
  - –Support SLC/MLC NAND and EF-NAND
  - –Support SDR/DDR NAND interface
- SD/MMC Interface
  - –Comply with eMMC standard specification V4.3
  - –Comply with SD physical layer specification V2.0
  - –Comply with SDIO card specification V2.0
  - –Support 1/4/8 bits bus width
  - –Support HS/DS/SDR12/SDR25 bus mode
  - –Support eMMC mandatory and alternative boot operations
  - –Support four independent SD/MMC/SDIO controllers
  - –Support SDSC/SDHC/SDXC/MMC/ RS-MMC card
  - –Support eMMC/iNand Flash
  - –Support 1GB/2GB/4GB/8GB/16GB/32GB/64GB /128GB SD/MMC card
  - –Support SDIO interrupt detection
  - –Support descriptor-based internal DMA controller for efficient scatter and gather operations

System Resources

- **Timer**
  - 6 timers: clock source can be switched over 24M/32K for all timers, and external signals can be used as clock source for Timer4/5
  - Two 33-bit AVS counters
  - Watchdog to generate reset signal or interrupt
  - Real time counter for second, minute, hour, day, month, and year
- **High Speed Timer**
  - 4 channels
  - Clock source is fixed to AHB, and the pre-scale ranges from 1 to 16
  - 56-bit counter that can be separated to 24-bit high register and 32-bit low register
- **DMA**
  - 16 channels
  - Support data width of 8/32 bits
  - Support linear and IO address modes
- **CCU**
  - 8PLLs, a main 24MHz oscillator, an on-chip RC oscillator and a 32768Hz oscillator (optional)
- **GIC**
  - Support 16 SGIs, 16 PPIs, and 128 SPIs
  - Support ARM architecture security extensions
  - Support ARM architecture virtualization extensions
  - Support uniprocessor and multiprocessor environments

Video Engine (Phoenix 3.0)

- Video Decoding
  - Support picture size up to 3840x2160
  - Support decoding speed up to 1080p@60fps
  - Supported formats: Mpeg1/2, Mpeg4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP6/8, AVS jizun, Jpeg/Mjpeg, etc.
- Video Encoding
  - H.264 HP up to 1080p@30fps
  - Jpeg baseline: picture size up to 4080x4080
  - Alpha blending
  - Thumb generation
  - 4x2 scaling ratio from 1/16 to 64 arbitrary non-integer ratio

Display Engine

- Four moveable and size-adjustable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
  - 8-tap scale filter in horizontal and 4 tap in vertical
  - Source image size from 8x4 to 8192x8192 resolution and destination image size from 8x4 to 8192x8192 resolution
- Support multiple image input formats
  - mono 1/2/4/8 bpp
  - palette 1/2/4/8 bpp
  - 6/24/32 bpp color
  - YUV444/420/422/411
- Support alpha blending/color key/gamma/harware cursor/sprite
- Output color correction: luminance/hue/saturation, etc
- Support de-interlace
- Video enhancement: lum peaking/DCTi/black and white level extension
- 3D input/output format conversion and display

Video Output

- HDMI 1.4 transmitter with HDCP
- LVDS/Sync RGB/CPU LCD interface up to 1920x1200 resolution
- Support 4-channel CVBS, or 2-channel S-video, or 1-channel YPbPr/VGA (YPbPr/VGA up to 1080p)
- Support two-channel independent display

Video Input

- Support TV decoder: 4-ch analog CVBS or 1-ch YPbPr(480i/576i/480p/576p) signal input
- Dual CMOS sensor parallel interfaces that support YUV format only
  - CSI0 up to 1080p@30fps
  - CSI1 up to 720p@30fps
- Support BT656 interface
- Support 24-bit YUV444/RGB interface

Analog Audio Output

- Stereo audio DAC
- Stereo capless headphone drivers
  - –Up to 100dB SNR during DAC playback
  - –Support 8KHz~192KHz DAC sample rate
- One low-noise analog microphone bias
- Dedicated headphone outputs
- Two mixers to meet different requirements
  - –Output mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output
  - –ADC record mixer for LINEINL/R, FMINL/R, MIC1/2 and Stereo DAC output

Analog Audio Input

- Support four analog audio inputs
  - –Two microphone inputs
  - –Differential or stereo line-in input
  - –Stereo FM-in input
- Stereo audio ADC
  - –96dBA SNR
  - –Support 8KHz ~ 48KHz ADC sample rate

RTP

- 12-bit SAR ADC
- Dual touch detection
- Sampling frequency up to 2MHz

Connectivity

- **USB2.0 DRD**
  - –Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
  - –Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps) in Device mode
  - –Support up to 5 user-configurable endpoints for Bulk , Isochronous, Control and Interrupt
- **USB EHCI/OHCI**
  - –Two EHCI/OHCI-compliant hosts
- **EMAC**
  - –Support 10/100Mbps MII data transfer rate
- **GMAC**
  - –Comply with the IEEE 802.3-2002 standard
  - –Programmable frame length to support Standard or Jumbo Ethernet frames with size up to 16KB
  - –Support 10/100/1000Mbps data transfer rates RGMII interface to communicate with an external Gigabit PHY
  - –Support 10/100Mbps MII PHY interface
- **Digital Audio In/Out**
  - –One I2S compliant audio interface, supporting 8-channel and 2-channel input
  - –One PCM, supporting linear sample(8-bit or 16-bit), 8-bit u-law and A-law companded sample
  - –One AC97 audio codec, supporting 2-channel and 6-channel audio data output
- **Transport Stream Controller**
  - –Support both SPI and SSI
  - –Speed up to 150Mbps for both SPI and SSI
  - –Support 32-channel PID filter
  - –Support hardware PCR packet detect
- **Open-Drain TWI**
  - –Up to 5 TWIs compliant with TWI protocol
- **Smart Card Reader**
  - –One smart card reader controller supporting ISO/IEC 7816-3 and EMV2000 specifications
  - –Support synchronous and any other non-ISO 7816 and non-EMV cards
- **SPI**
  - –Master/Slave configurable
  - –Up to 4 independent SPI controllers: SPI0 with one CS signal for system boot, SPI1/2/3 each with two CS signals
- **UART**
  - –Up to 8 UART controllers:UART0 with two wires for debug tools, UART1 with 8 wires, UART2/3 each with 4 wires, and others each with 2 wires

- **PS2**
  - Two PS2 compliant to IBM PS2 and AT-compatible keyboard and mouse interface
  - Dual-role controller: a PS2 host or a PS2 device
- **IR**
  - Two IR controllers supporting CIR, MIR and FIR modes
- **SATA**
  - One SATA Host controller
  - Support SATA 1.5Gb/s and SATA 3.0Gb/s
  - Comply with SATA spec 2.6
  - Support external SATA(eSATA)
- **CAN**
  - One CAN bus controller
  - Support the CAN2.0 A/B protocol specification
  - Programmable data rate up to 1Mbps
- **Keypad**
  - One keypad matrix interface up to 8 rows and 8 colums
  - Interrupt for key press or key release
  - Internal debouncing filter to prevent switching noises
- **LRADC**
  - 6-bit resolution
  - Voltage input range between 0V to 2V
- **PWM**
  - 2 PWM outputs
  - Support cycle mode and pulse mode
  - The pre-scale is from 1 to 64

Security System

- Security System
  - Support AES, DES, 3DES, SHA-1, MD5
  - Support ECB/CBC modes for AES/DES/3DES
  - 128-bit, 192-bit and 256-bit key size for AES
  - 160-bit hardware PRNG with 192-bit seed
- Security JTAG

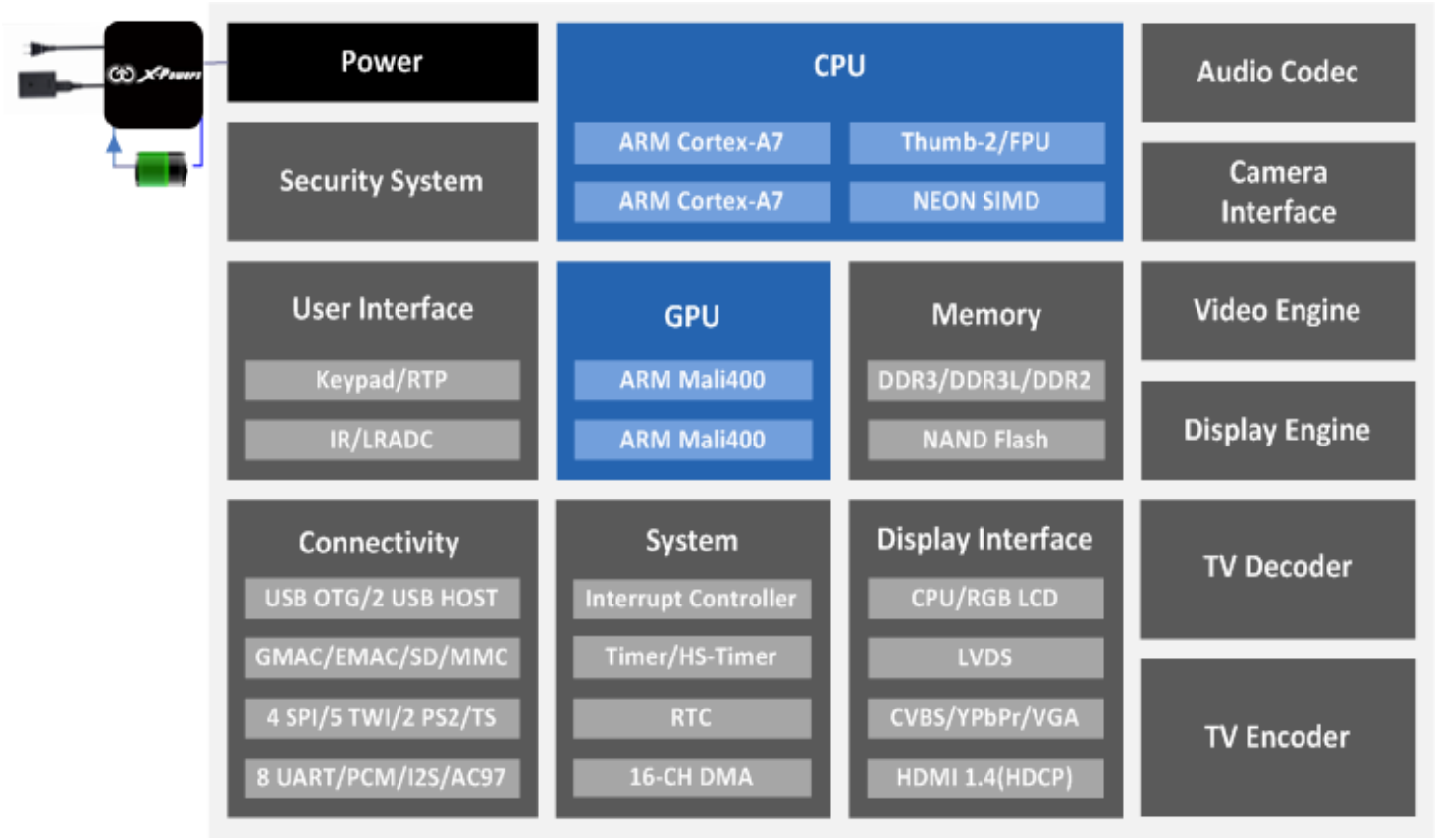
Power Management

- Flexible PLL clock generator and OSC for 32KHz
- Flexible clock gate
- Support DVFS for CPU frequency and voltage adjustment
- Support standby mode (only DDR+RTC-Domain power exist)

Package

- FBGA 441 balls,0.80mm ball pitch, 19x19x1.4mm

3 BLOCK DIAGRAM



4 PIN DESCRIPTION

4.1. PIN CHARACTERISTICS

Following table describes the A20 pin characteristics from seven aspects: ***BALL#, Pin Name, Default Function[1], Type[2], Reset State[3], Default Pull Up/Down[4], and Buffer Strength[5]***.

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
SDRAM						
AC7	SDQ0	DRAM	I/O	Z	-	-
AC4	SDQ1	DRAM	I/O	Z	-	-
AC8	SDQ2	DRAM	I/O	Z	-	-
AB5	SDQ3	DRAM	I/O	Z	-	-
AB7	SDQ4	DRAM	I/O	Z	-	-
AB8	SDQ5	DRAM	I/O	Z	-	-
AB4	SDQ6	DRAM	I/O	Z	-	-
AC3	SDQ7	DRAM	I/O	Z	-	-
AA1	SDQ8	DRAM	I/O	Z	-	-
AC1	SDQ9	DRAM	I/O	Z	-	-
Y1	SDQ10	DRAM	I/O	Z	-	-
AB2	SDQ11	DRAM	I/O	Z	-	-
AC2	SDQ12	DRAM	I/O	Z	-	-
W2	SDQ13	DRAM	I/O	Z	-	-
AB3	SDQ14	DRAM	I/O	Z	-	-
Y2	SDQ15	DRAM	I/O	Z	-	-
T2	SDQ16	DRAM	I/O	Z	-	-
N2	SDQ17	DRAM	I/O	Z	-	-
U2	SDQ18	DRAM	I/O	Z	-	-
P1	SDQ19	DRAM	I/O	Z	-	-
T1	SDQ20	DRAM	I/O	Z	-	-
U1	SDQ21	DRAM	I/O	Z	-	-
N1	SDQ22	DRAM	I/O	Z	-	-

Note:

1 ***Default function*** defines the default function of each pin, especially for pins with multiplexing functions;

2 There are five ***pin types*** here: O for output, I for input, I/O for input/output, A for analog,P for power and G for ground;

3 ***Reset state*** defines the state of the terminal at reset: Z for high-impedance.

4 ***Default Pull up/down*** defines the presence of an internal pull up or pull down resistor. Unless otherwise specified, the pin is default to be floating, and can be configured as pull up or pull down;

5 ***Buffer strength*** defines the driver strength of the associated output buffer. It is tested in the condition that VCC= 3.3V, strength=MAX;

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
M2	SDQ23	DRAM	I/O	Z	-	-
J1	SDQ24	DRAM	I/O	Z	-	-
L1	SDQ25	DRAM	I/O	Z	-	-
H1	SDQ26	DRAM	I/O	Z	-	-
K2	SDQ27	DRAM	I/O	Z	-	-
L2	SDQ28	DRAM	I/O	Z	-	-
G2	SDQ29	DRAM	I/O	Z	-	-
M1	SDQ30	DRAM	I/O	Z	-	-
H2	SDQ31	DRAM	I/O	Z	-	-
H3/H4/Y5/AA8	SVREF	DRAM	P		-	-
AB6	SDQS0	DRAM	I/O	Z	-	-
AC5	SDQS0B	DRAM	I/O	Z	-	-
AC6	SDQM0	DRAM	O	Z	-	-
AB1	SDQS1	DRAM	I/O	Z	-	-
AA2	SDQS1B	DRAM	I/O	Z	-	-
W1	SDQM1	DRAM	O	Z	-	-
R2	SDQM2	DRAM	O	Z	-	-
R1	SDQS2	DRAM	I/O	Z	-	-
P2	SDQS2B	DRAM	I/O	Z	-	-
K1	SDQS3	DRAM	I/O	Z	-	-
J2	SDQS3B	DRAM	I/O	Z	-	-
G1	SDQM3	DRAM	O	Z	-	-
V2	SCKB	DRAM	O	Z	-	-
V1	SCK	DRAM	O	Z	-	-
J4	SCK1	DRAM	O	Z	-	-
J3	SCK1B	DRAM	O	Z		
N3	SCKE	DRAM	O	Z	-	-
W4	SA0	DRAM	O	Z	-	-
R4	SA1	DRAM	O	Z	-	-
U4	SA2	DRAM	O	Z	-	-
M4	SA3	DRAM	O	Z	-	-
Y4	SA4	DRAM	O	Z	-	-
N4	SA5	DRAM	O	Z	-	-
V4	SA6	DRAM	O	Z	-	-
M3	SA7	DRAM	O	Z	-	-
AA3	SA8	DRAM	O	Z	-	-
P4	SA9	DRAM	O	Z	-	-
L3	SA10	DRAM	O	Z	-	-
W3	SA11	DRAM	O	Z	-	-
P3	SA12	DRAM	O	Z	-	-
Y3	SA13	DRAM	O	Z	-	-
R3	SA14	DRAM	O	Z	-	-
AA4	SA15	DRAM	O	Z		
K3	SBA0	DRAM	O	Z	-	-
L4	SBA1	DRAM	O	Z	-	-
K4	SBA2	DRAM	O	Z	-	-
T3	SWE	DRAM	O	Z	-	-
U3	SCAS	DRAM	O	Z	-	-
T4	SRAS	DRAM	O	Z	-	-
V3	SCS	DRAM	O	Z	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
AA5	SODT	DRAM	O	Z	-	-
AA7	SZQ	DRAM	A	Z	-	-
AA6	SRST	DRAM	O	Z	-	-
N8	SADBG	DRAM	A	Z	-	-
P8	SDDBG0	DRAM	A	Z	-	-
R8	SADBG1	DRAM	A	Z	-	-
M8/N9/P9	VDD-DLL	POWER	P	-	-	-
G5/H5/L5/W5/ W6/W7/M5/R5/ T5/Y6	VCC-DRAM	POWER	P	-	-	-
GPIO A						
D5	PA0	GPIO	I/O	Z	NO PULL	20
E5	PA1	GPIO	I/O	Z	NO PULL	20
D6	PA2	GPIO	I/O	Z	NO PULL	20
E6	PA3	GPIO	I/O	Z	NO PULL	20
D7	PA4	GPIO	I/O	Z	NO PULL	20
E7	PA5	GPIO	I/O	Z	NO PULL	20
D8	PA6	GPIO	I/O	Z	NO PULL	20
E8	PA7	GPIO	I/O	Z	NO PULL	20
D9	PA8	GPIO	I/O	Z	NO PULL	20
E9	PA9	GPIO	I/O	Z	NO PULL	20
D10	PA10	GPIO	I/O	Z	NO PULL	20
E10	PA11	GPIO	I/O	Z	NO PULL	20
D11	PA12	GPIO	I/O	Z	NO PULL	20
E11	PA13	GPIO	I/O	Z	NO PULL	20
D12	PA14	GPIO	I/O	Z	NO PULL	20
E12	PA15	GPIO	I/O	Z	NO PULL	20
D13	PA16	GPIO	I/O	Z	NO PULL	20
C13	PA17	GPIO	I/O	Z	NO PULL	20
H10/J10	VCC-PA	POWER	P	-	-	-
GPIO B						
A15	PB0	GPIO	I/O	Z	NO PULL	20
B15	PB1	GPIO	I/O	Z	NO PULL	20
A14	PB2	GPIO	I/O	Z	NO PULL	20
B14	PB3	GPIO	I/O	Z	NO PULL	20
A13	PB4	GPIO	I/O	Z	NO PULL	20
B13	PB5	GPIO	I/O	Z	NO PULL	20
A12	PB6	GPIO	I/O	Z	NO PULL	20
B12	PB7	GPIO	I/O	Z	NO PULL	20
A11	PB8	GPIO	I/O	Z	NO PULL	20
C12	PB9	GPIO	I/O	Z	NO PULL	20
C11	PB10	GPIO	I/O	Z	NO PULL	20
C10	PB11	GPIO	I/O	Z	NO PULL	20
C9	PB12	GPIO	I/O	Z	NO PULL	20
B11	PB13	GPIO	I/O	Z	NO PULL	20
A10	PB14	GPIO	I/O	Z	NO PULL	20
B10	PB15	GPIO	I/O	Z	NO PULL	20
A9	PB16	GPIO	I/O	Z	NO PULL	20
B9	PB17	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
A8	PB18	GPIO	I/O	Z	NO PULL	20
B8	PB19	GPIO	I/O	Z	NO PULL	20
C8	PB20	GPIO	I/O	Z	NO PULL	20
C7	PB21	GPIO	I/O	Z	NO PULL	20
A7	PB22	GPIO	I/O	Z	NO PULL	20
B7	PB23	GPIO	I/O	Z	NO PULL	20
GPIO C						
M23	PC0	GPIO	I/O	Z	NO PULL	20
M22	PC1	GPIO	I/O	Z	NO PULL	20
L23	PC2	GPIO	I/O	Z	NO PULL	20
L22	PC3	GPIO	I/O	Z	PULL UP	20
K23	PC4	GPIO	I/O	Z	PULL UP	20
K22	PC5	GPIO	I/O	Z	NO PULL	20
J23	PC6	GPIO	I/O	Z	PULL UP	20
J22	PC7	GPIO	I/O	Z	PULL UP	20
H23	PC8	GPIO	I/O	Z	NO PULL	20
H22	PC9	GPIO	I/O	Z	NO PULL	20
G23	PC10	GPIO	I/O	Z	NO PULL	20
G22	PC11	GPIO	I/O	Z	NO PULL	20
H21	PC12	GPIO	I/O	Z	NO PULL	20
H20	PC13	GPIO	I/O	Z	NO PULL	20
G21	PC14	GPIO	I/O	Z	NO PULL	20
G20	PC15	GPIO	I/O	Z	NO PULL	20
M21	PC16	GPIO	I/O	Z	PULL DOWN	20
F23	PC17	GPIO	I/O	Z	PULL UP	20
F22	PC18	GPIO	I/O	Z	PULL UP	20
L21	PC19	GPIO	I/O	Z	NO PULL	20
K21	PC20	GPIO	I/O	Z	NO PULL	20
J21	PC21	GPIO	I/O	Z	NO PULL	20
J20	PC22	GPIO	I/O	Z	NO PULL	20
G19	PC23	GPIO	I/O	Z	PULL UP	20
F21	PC24	GPIO	I/O	Z	NO PULL	20
H19/J19	VCC-PC	POWER	P	-	-	-
GPIO D						
AB15	PD0	GPIO	I/O	Z	NO PULL	20
AC15	PD1	GPIO	I/O	Z	NO PULL	20
AB14	PD2	GPIO	I/O	Z	NO PULL	20
AC14	PD3	GPIO	I/O	Z	NO PULL	20
AB13	PD4	GPIO	I/O	Z	NO PULL	20
AC13	PD5	GPIO	I/O	Z	NO PULL	20
AB12	PD6	GPIO	I/O	Z	NO PULL	20
AC12	PD7	GPIO	I/O	Z	NO PULL	20
AB11	PD8	GPIO	I/O	Z	NO PULL	20
AC11	PD9	GPIO	I/O	Z	NO PULL	20
Y15	PD10	GPIO	I/O	Z	NO PULL	20
AA15	PD11	GPIO	I/O	Z	NO PULL	20
Y14	PD12	GPIO	I/O	Z	NO PULL	20
AA14	PD13	GPIO	I/O	Z	NO PULL	20
Y13	PD14	GPIO	I/O	Z	NO PULL	20
AA13	PD15	GPIO	I/O	Z	NO PULL	20
Y12	PD16	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
AA12	PD17	GPIO	I/O	Z	NO PULL	20
Y11	PD18	GPIO	I/O	Z	NO PULL	20
AA11	PD19	GPIO	I/O	Z	NO PULL	20
Y10	PD20	GPIO	I/O	Z	NO PULL	20
AA10	PD21	GPIO	I/O	Z	NO PULL	20
AB10	PD22	GPIO	I/O	Z	NO PULL	20
AC10	PD23	GPIO	I/O	Z	NO PULL	20
Y9	PD24	GPIO	I/O	Z	NO PULL	20
AA9	PD25	GPIO	I/O	Z	NO PULL	20
AB9	PD26	GPIO	I/O	Z	NO PULL	20
AC9	PD27	GPIO	I/O	Z	NO PULL	20
GPIO E						
E23	PE0	GPIO	I/O	Z	NO PULL	20
E22	PE1	GPIO	I/O	Z	NO PULL	20
D23	PE2	GPIO	I/O	Z	NO PULL	20
D22	PE3	GPIO	I/O	Z	NO PULL	20
C23	PE4	GPIO	I/O	Z	NO PULL	20
C22	PE5	GPIO	I/O	Z	NO PULL	20
B23	PE6	GPIO	I/O	Z	NO PULL	20
B22	PE7	GPIO	I/O	Z	NO PULL	20
A23	PE8	GPIO	I/O	Z	NO PULL	20
A22	PE9	GPIO	I/O	Z	NO PULL	20
B21	PE10	GPIO	I/O	Z	NO PULL	20
A21	PE11	GPIO	I/O	Z	NO PULL	20
F19	VCC-PE	POWER	P	-	-	-
GPIO F						
M20	PF0	GPIO	I/O	Z	NO PULL	20
M19	PF1	GPIO	I/O	Z	NO PULL	20
L20	PF2	GPIO	I/O	Z	NO PULL	20
L19	PF3	GPIO	I/O	Z	NO PULL	20
K20	PF4	GPIO	I/O	Z	NO PULL	20
K19	PF5	GPIO	I/O	Z	NO PULL	20
N19	VCC-PF	POWER	P	-	-	-
GPIO G						
F20	PG0	GPIO	I/O	Z	NO PULL	20
E21	PG1	GPIO	I/O	Z	NO PULL	20
E20	PG2	GPIO	I/O	Z	NO PULL	20
D21	PG3	GPIO	I/O	Z	NO PULL	20
D20	PG4	GPIO	I/O	Z	NO PULL	20
C21	PG5	GPIO	I/O	Z	NO PULL	20
E19	PG6	GPIO	I/O	Z	NO PULL	20
C20	PG7	GPIO	I/O	Z	NO PULL	20
D19	PG8	GPIO	I/O	Z	NO PULL	20
C19	PG9	GPIO	I/O	Z	NO PULL	20
D18	PG10	GPIO	I/O	Z	NO PULL	20
C18	PG11	GPIO	I/O	Z	NO PULL	20
E18	VCC-PG	POWER	P	-	-	-
GPIO H						
A6	PH0	GPIO	I/O	Z	NO PULL	20
B6	PH1	GPIO	I/O	Z	NO PULL	20
C6	PH2	GPIO	I/O	Z	NO PULL	20

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
A5	PH3	GPIO	I/O	Z	NO PULL	20
B5	PH4	GPIO	I/O	Z	NO PULL	20
C5	PH5	GPIO	I/O	Z	NO PULL	20
A4	PH6	GPIO	I/O	Z	NO PULL	20
B4	PH7	GPIO	I/O	Z	NO PULL	20
C4	PH8	GPIO	I/O	Z	NO PULL	20
D4	PH9	GPIO	I/O	Z	NO PULL	20
A3	PH10	GPIO	I/O	Z	NO PULL	20
B3	PH11	GPIO	I/O	Z	NO PULL	20
C3	PH12	GPIO	I/O	Z	NO PULL	20
A2	PH13	GPIO	I/O	Z	NO PULL	20
B2	PH14	GPIO	I/O	Z	NO PULL	20
A1	PH15	GPIO	I/O	Z	NO PULL	20
B1	PH16	GPIO	I/O	Z	NO PULL	20
C1	PH17	GPIO	I/O	Z	NO PULL	20
C2	PH18	GPIO	I/O	Z	NO PULL	20
D1	PH19	GPIO	I/O	Z	NO PULL	20
D2	PH20	GPIO	I/O	Z	NO PULL	20
D3	PH21	GPIO	I/O	Z	NO PULL	20
E1	PH22	GPIO	I/O	Z	NO PULL	20
E2	PH23	GPIO	I/O	Z	NO PULL	20
E3	PH24	GPIO	I/O	Z	NO PULL	20
E4	PH25	GPIO	I/O	Z	NO PULL	20
F3	PH26	GPIO	I/O	Z	NO PULL	20
F4	PH27	GPIO	I/O	Z	NO PULL	20
GPIO I						
A20	PI0	GPIO	I/O	Z	NO PULL	20
B20	PI1	GPIO	I/O	Z	NO PULL	20
A19	PI2	GPIO	I/O	Z	NO PULL	20
B19	PI3	GPIO	I/O	Z	NO PULL	20
A18	PI4	GPIO	I/O	Z	NO PULL	20
B18	PI5	GPIO	I/O	Z	NO PULL	20
A17	PI6	GPIO	I/O	Z	NO PULL	20
B17	PI7	GPIO	I/O	Z	NO PULL	20
A16	PI8	GPIO	I/O	Z	NO PULL	20
B16	PI9	GPIO	I/O	Z	NO PULL	20
C17	PI10	GPIO	I/O	Z	NO PULL	20
D17	PI11	GPIO	I/O	Z	NO PULL	20
C16	PI12	GPIO	I/O	Z	NO PULL	20
D16	PI13	GPIO	I/O	Z	NO PULL	20
C15	PI14	GPIO	I/O	Z	NO PULL	20
D15	PI15	GPIO	I/O	Z	NO PULL	20
E17	PI16	GPIO	I/O	Z	NO PULL	20
E16	PI17	GPIO	I/O	Z	NO PULL	20
E15	PI18	GPIO	I/O	Z	NO PULL	20
D14	PI19	GPIO	I/O	Z	NO PULL	20
E14	PI20	GPIO	I/O	Z	NO PULL	20
E13	PI21	GPIO	I/O	Z	NO PULL	20
SYSTEM CONTROL						
W8	BOOTSEL	-	I	H	PULL UP	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
T10	JTAGSEL	-	I	H	PULL UP	-
H16	TEST	-	I	L	PULL DOWN	-
F5	NMI#	-	I	Z	NO PULL	
C14	RESET#	-	I	Z	NO PULL	
USB						
N20	DM0	-	A	-	-	-
N21	DP0	-	A	-	-	-
P20	DM1	-	A	-	-	-
P21	DP1	-	A	-	-	-
L16/L15	VCC-USB	-	P	-	-	-
K16	VDD-USB	-	P	-	-	-
R20	DM2	-	A	-	-	-
R21	DP2	-	A	-	-	-
SATA						
T20	SATA-TXP	-	A	-	-	-
T21	SATA-TXM	-	A	-	-	-
U20	SATA-RXM	-	A	-	-	-
U21	SATA-RXP	-	A	-	-	-
V21	REXT-SATA	-	A	-	-	-
M15/M16	VDD-SATA	-	P	-	-	-
N15/N16	VDD25-SATA	-	P	-	-	-
P19	SATA-CLKM	-	A	-	-	-
R19	SATA-CLKP	-	A	-	-	-
TP						
Y22	TPX1	-	A	-	-	-
AA22	TPX2	-	A	-	-	-
Y23	TPY1	-	A	-	-	-
AA23	TPY2	-	A	-	-	-
AUDIO CODEC						
AC23	MICOUTN	-	A	-	-	-
AC22	MICOUTP	-	A	-	-	-
Y21	FMINR	-	A	-	-	-
Y20	FMINL	-	A	-	-	-
AA21	VMIC	-	P	-	-	-
AC21	MICIN2	-	A	-	-	-
AC20	MICIN1	-	A	-	-	-
W20	VRA1	-	A	-	-	-
V20	VRA2	-	A	-	-	-
T19	AVCC	-	P	-	-	-
W21	VRP	-	A	-	-	-
AB21	LINEINR	-	A	-	-	-
AB20	LINEINL	-	A	-	-	-
U19	AGND	-	G	-	-	-
W19	HPR	-	A	-	-	-
Y19	HPL	-	A	-	-	-
V19	GND-HP	-	G	-	-	-
AA19	HPCOM	-	A			
AA20	HPCOMFB	-	A	-	-	-
AC19	HPBP	-	P	-	-	-
AB19	VCCHP	-	P	-	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
LRADC						
AB23	LRADC0	-	A	-	-	-
AB22	LRADC1	-	A	-	-	-
TV-OUT						
AC16	TVOUT0	-	A	-	-	-
AB16	TVOUT1	-	A	-	-	-
AC17	TVOUT2	-	A	-	-	-
AB17	TVOUT3	-	A	-	-	-
W15	VCC-TVOUT	-	P	-	-	-
TV-IN						
AC18	TVIN0	-	A	-	-	-
AB18	TVIN1	-	A	-	-	-
AA17	TVIN2	-	A	-	-	-
Y17	TVIN3	-	A	-	-	-
W16	VCC-TVIN	-	P	-	-	-
W17	VCC25-TVIN	-	P	-	-	-
AA16	VRP-TVIN	-	A	-	-	-
Y16	VRN-TVIN	-	A	-	-	-
HDMI						
V23	HTX0P	-	A	-	-	-
V22	HTX0N	-	A	-	-	-
U23	HTX1P	-	A	-	-	-
U22	HTX1N	-	A	-	-	-
T23	HTX2P	-	A	-	-	-
T22	HTX2N	-	A	-	-	-
W23	HTXCP	-	A	-	-	-
W22	HTXCN	-	A	-	-	-
T13	VCC-HDMI	-	P	-	-	-
R23	HSCL	-	I/O	-	-	-
R22	HSDA	-	I/O	-	-	-
P22	HHPD	-	I/O	-	-	-
P23	HCEC	-	I/O	-	-	-
T14	HVREG1	-	A	-	-	-
CLOCK						
F1	X32KI	-	A	-	-	-
F2	X32KO	-	A	-	-	-
K8	VDD-RTC	-	P	-	-	-
N23	X24MI	-	A	-	-	-
N22	X24MO	-	A			
R15	PLLVREG		A			
P16	VCC-PLL	-	P			
T15	PLLTEST	-	A			
T16	PLLDV	-	A			
POWER						
J12/J13/H11/ H12/H13/H14	VDD-CPU	-	P	-	-	-
T8/R9/R10/L8/ L9/K9/K10/K15/ J15/J16	VDD-SYS	-	P	-	-	-

BALL#	Pin Name	Default Function	Type	Reset State	Default Pull Up/Down	Buffer Strength (mA)
J5/K5/N5/P5/U5/ V5/Y7/Y8/G3/G4/ L10/L11/L12/L13/ L14/K11/K12/ K13/K14J11/M9/ M10/M11/M12/ M13/M14/N10/ N11/N12/N13/ N14/P10/P11/ P12/P13/P14/ P15/R11/R12/ R13/T11/T12/ W9/W10/W11/ V19/W18/Y18/ AA18	GND	-	G	-	-	-
H8/H9/J8/J9/J14/ H15	VCC	-	P	-	-	-
W12/W13/W14	VCC-LVDS	-	P	-	-	-
R14/R16	NC	-	-	-	-	-
EFUSE						
T9	VDDQE		P	-	-	-

4.2. GPIO MULTIPLEXING FUNCTIONS

Following table provides a description of the GPIO multiplexing functions of A20.

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PA0	GPIO	I/O	I	Z	ERXD3	SPI1-CS0	UART2-RTS	GRXD3	-	-
PA1	GPIO	I/O	I	Z	ERXD2	SPI1-CLK	UART2-CTS	GRXD2	-	-
PA2	GPIO	I/O	I	Z	ERXD1	SPI1-MOSI	UART2-TX	GRXD1	-	-
PA3	GPIO	I/O	I	Z	ERXD0	SPI1-MISO	UART2-RX	GRXD0	-	-
PA4	GPIO	I/O	I	Z	ETXD3	SPI1-CS1	-	GTXD3	-	-
PA5	GPIO	I/O	I	Z	ETXD2	SPI3-CS0	-	GTXD2	-	-
PA6	GPIO	I/O	I	Z	ETXD1	SPI3-CLK	-	GTXD1	-	-
PA7	GPIO	I/O	I	Z	ETXD0	SPI3-MOSI	-	GTXD0	-	-
PA8	GPIO	I/O	I	Z	ERXCK	SPI3-MISO	-	GRXCK	-	-
PA9	GPIO	I/O	I	Z	ERXERR	SPI3-CS1	-	GNULL/ERX-ERR	I2S1-MCLK	-
PA10	GPIO	I/O	I	Z	ERXDV	-	UART1-TX	GRXCTL/ RXDV	-	-
PA11	GPIO	I/O	I	Z	EMDC	-	UART1-RX	GMDC	-	-
PA12	GPIO	I/O	I	Z	EMDIO	UART6-TX	UART1-RTS	GMDIO	-	-
PA13	GPIO	I/O	I	Z	ETXEN	UART6-RX	UART1-CTS	GTXCTL/ ETXEN	-	-
PA14	GPIO	I/O	I	Z	ETXCK	UART7-TX	UART1-DTR	GNULL/ ETXCK	I2S1-BCLK	-
PA15	GPIO	I/O	I	Z	ECRS	UART7-RX	UART1-DSR	GTXCK/ ECRS	I2S1-LRCK	-
PA16	GPIO	I/O	I	Z	ECOL	CAN-TX	UART1-DCD	GCLKIN/ ECOL	I2S1-DO	-
PA17	GPIO	I/O	I	Z	ETXERR	CAN-RX	UART1-RING	GNULL/ETX-ERR	I2S1-DI	-
PB0	GPIO	I/O	I	Z	TWI0-SCK	-	-	-	-	-
PB1	GPIO	I/O	I	Z	TWI0-SDA	-	-	-	-	-
PB2	GPIO	I/O	I	Z	PWM0	-	-	-	-	-
PB3	GPIO	I/O	I	Z	IR0-TX	-	OWA-MCLK	-		-
PB4	GPIO	I/O	I	Z	IR0-RX	-	-	-	-	-
PB5	GPIO	I/O	I	Z	I2S-MCLK	AC97-MCLK	-	-	-	-
PB6	GPIO	I/O	I	Z	I2S-BCLK	AC97-BCLK	-	-	-	-
PB7	GPIO	I/O	I	Z	I2S-LRCK	AC97-SYNC	-	-	-	-
PB8	GPIO	I/O	I	Z	I2S-DO0	AC97-DO	-	-	-	-
PB9	GPIO	I/O	I	Z	I2S-DO1	-	-	-	-	-
PB10	GPIO	I/O	I	Z	I2S-DO2	-	-	-	-	-
PB11	GPIO	I/O	I	Z	I2S-DO3	-	-	-	-	-
PB12	GPIO	I/O	I	Z	I2S-DI	AC97-DI	OWA-DI	-	-	-
PB13	GPIO	I/O	I	Z	SPI2-CS1	-	OWA-DO	-	-	-
PB14	GPIO	I/O	I	Z	SPI2-CS0	JTAG-MS0	-	-	-	-
PB15	GPIO	I/O	I	Z	SPI2-CLK	JTAG-CK0	-	-	-	-
PB16	GPIO	I/O	I	Z	SPI2-MOSI	JTAG-DO0	-	-	-	-
PB17	GPIO	I/O	I	Z	SPI2-MISO	JTAG-DI0	-	-	-	-
PB18	GPIO	I/O	I	Z	TWI1-SCK	-	-	-	-	-
PB19	GPIO	I/O	I	Z	TWI1-SDA	-	-	-	-	-
PB20	GPIO	I/O	I	Z	TWI2-SCK	-	-	-	-	-

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PB21	GPIO	I/O	I	Z	TWI2-SDA	-	-	-	-	-
PB22	GPIO	I/O	I	Z	UART0-TX	IR1-TX	-	-	-	-
PB23	GPIO	I/O	I	Z	UART0-RX	IR1-RX	-	-	-	-
PC0	GPIO	I/O	I	Z	NWE#	SPI0-MOSI	-	-	-	-
PC1	GPIO	I/O	I	Z	NALE	SPI0-MISO	-	-	-	-
PC2	GPIO	I/O	I	Z	NCLE	SPI0-CLK	-	-	-	-
PC3	GPIO	I/O	I	Pull-Up	NCE1	-	-	-	-	-
PC4	GPIO	I/O	I	Pull-Up	NCE0	-	-	-	-	-
PC5	GPIO	I/O	I	Z	NRE#	-	-	-	-	-
PC6	GPIO	I/O	I	Pull-Up	NRB0	SDC2-CMD	-	-	-	-
PC7	GPIO	I/O	I	Pull-Up	NRB1	SDC2-CLK	-	-	-	-
PC8	GPIO	I/O	I	Z	NDQ0	SDC2-D0	-	-	-	-
PC9	GPIO	I/O	I	Z	NDQ1	SDC2-D1	-	-	-	-
PC10	GPIO	I/O	I	Z	NDQ2	SDC2-D2	-	-	-	-
PC11	GPIO	I/O	I	Z	NDQ3	SDC2-D3	-	-	-	-
PC12	GPIO	I/O	I	Z	NDQ4	-	-	-	-	-
PC13	GPIO	I/O	I	Z	NDQ5	-	-	-	-	-
PC14	GPIO	I/O	I	Z	NDQ6	-	-	-	-	-
PC15	GPIO	I/O	I	Z	NDQ7	-	-	-	-	-
PC16	GPIO	I/O	I	Pull-Down	NWP	-	-	-	-	-
PC17	GPIO	I/O	I	Pull-Up	NCE2	-	-	-	-	-
PC18	GPIO	I/O	I	Pull-Up	NCE3	-	-	-	-	-
PC19	GPIO	I/O	I	Z	NCE4	SPI2-CS0	-	-	-	-
PC20	GPIO	I/O	I	Z	NCE5	SPI2-CLK	-	-	-	-
PC21	GPIO	I/O	I	Z	NCE6	SPI2-MOSI	-	-	-	-
PC22	GPIO	I/O	I	Z	NCE7	SPI2-MISO	-	-	-	-
PC23	GPIO	I/O	I	Pull-Up	-	SPI0-CS0	-	-	-	-
PC24	GPIO	I/O	I	Z	NDQS	-	-	-	-	-
PD0	GPIO	I/O	I	Z	LCD0-D0	LVDS0-VP0	-	-	-	-
PD1	GPIO	I/O	I	Z	LCD0-D1	LVDS0-VN0	-	-	-	-
PD2	GPIO	I/O	I	Z	LCD0-D2	LVDS0-VP1	-	-	-	-
PD3	GPIO	I/O	I	Z	LCD0-D3	LVDS0-VN1	-	-	-	-
PD4	GPIO	I/O	I	Z	LCD0-D4	LVDS0-VP2	-	-	-	-
PD5	GPIO	I/O	I	Z	LCD0-D5	LVDS0-VN2	-	-	-	-
PD6	GPIO	I/O	I	Z	LCD0-D6	LVDS0-VPC	-	-	-	-
PD7	GPIO	I/O	I	Z	LCD0-D7	LVDS0-VNC	-	-	-	-
PD8	GPIO	I/O	I	Z	LCD0-D8	LVDS0-VP3	-	-	-	-
PD9	GPIO	I/O	I	Z	LCD0-D9	LVDS0-VN3	-	-	-	-
PD10	GPIO	I/O	I	Z	LCD0-D10	LVDS1-VP0	-	-	-	-
PD11	GPIO	I/O	I	Z	LCD0-D11	LVDS1-VN0	-	-	-	-
PD12	GPIO	I/O	I	Z	LCD0-D12	LVDS1-VP1	-	-	-	-
PD13	GPIO	I/O	I	Z	LCD0-D13	LVDS1-VN1	-	-	-	-
PD14	GPIO	I/O	I	Z	LCD0-D14	LVDS1-VP2	-	-	-	-
PD15	GPIO	I/O	I	Z	LCD0-D15	LVDS1-VN2	-	-	-	-
PD16	GPIO	I/O	I	Z	LCD0-D16	LVDS1-VPC	-	-	-	-
PD17	GPIO	I/O	I	Z	LCD0-D17	LVDS1-VNC	-	-	-	-
PD18	GPIO	I/O	I	Z	LCD0-D18	LVDS1-VP3	-	-	-	-
PD19	GPIO	I/O	I	Z	LCD0-D19	LVDS1-VN3	-	-	-	-
PD20	GPIO	I/O	I	Z	LCD0-D20	CSI1-MCLK	-	-	-	-
PD21	GPIO	I/O	I	Z	LCD0-D21	SMC-VPPEN	-	-	-	-
PD22	GPIO	I/O	I	Z	LCD0-D22	SMC-VPPPP	-	-	-	-
PD23	GPIO	I/O	I	Z	LCD0-D23	SMC-DET	-	-	-	-
PD24	GPIO	I/O	I	Z	LCD0-CLK	SMC-VCCEN	-	-	-	-
PD25	GPIO	I/O	I	Z	LCD0-DE	SMC-RST	-	-	-	-
PD26	GPIO	I/O	I	Z	LCD0-HSYNC	SMC-SLK	-	-	-	-
PD27	GPIO	I/O	I	Z	LCD0-VSYNC	SMC-SDA	-	-	-	-

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PE0	GPIO	I/O	I	Z	TS0-CLK	CSI0-PCLK	-	-	-	-
PE1	GPIO	I/O	I	Z	TS0-ERR	CSI0-MCLK	-	-	-	-
PE2	GPIO	I/O	I	Z	TS0-SYNC	CSI0-HSYNC	-	-	-	-
PE3	GPIO	I/O	I	Z	TS0-DVLD	CSI0-VSYNC	-	-	-	-
PE4	GPIO	I/O	I	Z	TS0-D0	CSI0-D0	-	-	-	-
PE5	GPIO	I/O	I	Z	TS0-D1	CSI0-D1	-	-	-	-
PE6	GPIO	I/O	I	Z	TS0-D2	CSI0-D2	-	-	-	-
PE7	GPIO	I/O	I	Z	TS0-D3	CSI0-D3	-	-	-	-
PE8	GPIO	I/O	I	Z	TS0-D4	CSI0-D4	-	-	-	-
PE9	GPIO	I/O	I	Z	TS0-D5	CSI0-D5	-	-	-	-
PE10	GPIO	I/O	I	Z	TS0-D6	CSI0-D6	-	-	-	-
PE11	GPIO	I/O	I	Z	TS0-D7	CSI0-D7	-	-	-	-
PF0	GPIO	I/O	I	Z	SDC0-D1	-	JTAG-MS1	-	-	-
PF1	GPIO	I/O	I	Z	SDC0-D0	-	JTAG-DI1	-	-	-
PF2	GPIO	I/O	I	Z	SDC0-CLK	-	UART0-TX	-	-	-
PF3	GPIO	I/O	I	Z	SDC0-CMD	-	JTAG-DO1	-	-	-
PF4	GPIO	I/O	I	Z	SDC0-D3	-	UART0-RX	-	-	-
PF5	GPIO	I/O	I	Z	SDC0-D2	-	JTAG-CK1	-	-	-
PG0	GPIO	I/O	I	Z	TS1-CLK	CSI1-PCLK	SDC1-CMD	-	-	-
PG1	GPIO	I/O	I	Z	TS1-ERR	CSI1-MLCK	SDC1-CLK	-	-	-
PG2	GPIO	I/O	I	Z	TS1-SYNC	CSI1-HSYNC	SDC1-D0	-	-	-
PG3	GPIO	I/O	I	Z	TS1-DVLD	CSI1-VSYNC	SDC1-D1	-	-	-
PG4	GPIO	I/O	I	Z	TS1-D0	CSI1-D0	SDC1-D2	CSI0-D8	-	-
PG5	GPIO	I/O	I	Z	TS1-D1	CSI1-D1	SDC1-D3	CSI0-D9	-	-
PG6	GPIO	I/O	I	Z	TS1-D2	CSI1-D2	UART3-TX	CSI0-D10	-	-
PG7	GPIO	I/O	I	Z	TS1-D3	CSI1-D3	UART3-RX	CSI0-D11	-	-
PG8	GPIO	I/O	I	Z	TS1-D4	CSI1-D4	UART3-RTS	CSI0-D12	-	-
PG9	GPIO	I/O	I	Z	TS1-D5	CSI1-D5	UART3-CTS	CSI0-D13	-	-
PG10	GPIO	I/O	I	Z	TS1-D6	CSI1-D6	UART4-TX	CSI0-D14	-	-
PG11	GPIO	I/O	I	Z	TS1-D7	CSI1-D7	UART4-RX	CSI0-D15	-	-
PH0	GPIO	I/O	I	Z	LCD1-D0	-	UART3-TX	-	EINT0	CSI1-D0
PH1	GPIO	I/O	I	Z	LCD1-D1	-	UART3-RX	-	EINT1	CSI1-D1
PH2	GPIO	I/O	I	Z	LCD1-D2	-	UART3-RTS	-	EINT2	CSI1-D2
PH3	GPIO	I/O	I	Z	LCD1-D3	-	UART3-CTS	-	EINT3	CSI1-D3
PH4	GPIO	I/O	I	Z	LCD1-D4	-	UART4-TX	-	EINT4	CSI1-D4
PH5	GPIO	I/O	I	Z	LCD1-D5	-	UART4-RX	-	EINT5	CSI1-D5
PH6	GPIO	I/O	I	Z	LCD1-D6	-	UART5-TX	-	EINT6	CSI1-D6
PH7	GPIO	I/O	I	Z	LCD1-D7	-	UART5-RX	-	EINT7	CSI1-D7
PH8	GPIO	I/O	I	Z	LCD1-D8	ERXD3	KP-IN0	-	EINT8	CSI1-D8
PH9	GPIO	I/O	I	Z	LCD1-D9	ERXD2	KP-IN1	-	EINT9	CSI1-D9
PH10	GPIO	I/O	I	Z	LCD1-D10	ERXD1	KP-IN2	-	EINT10	CSI1-D10
PH11	GPIO	I/O	I	Z	LCD1-D11	ERXD0	KP-IN3	-	EINT11	CSI1-D11
PH12	GPIO	I/O	I	Z	LCD1-D12	-	PS2-SCK1	-	EINT12	CSI1-D12
PH13	GPIO	I/O	I	Z	LCD1-D13	-	PS2-SDA1	SMC-RST	EINT13	CSI1-D13
PH14	GPIO	I/O	I	Z	LCD1-D14	ETXD3	KP-IN4	SMC-VPPEN	EINT14	CSI1-D14
PH15	GPIO	I/O	I	Z	LCD1-D15	ETXD2	KP-IN5	SMC-VPPPP	EINT15	CSI1-D15
PH16	GPIO	I/O	I	Z	LCD1-D16	ETXD1	KP-IN6	SMC-DET	EINT16	CSI1-D16
PH17	GPIO	I/O	I	Z	LCD1-D17	ETXD0	KP-IN7	SMC-VCCEN	EINT17	CSI1-D17
PH18	GPIO	I/O	I	Z	LCD1-D18	ERXCK	KP-OUT0	SMC-SLK	EINT18	CSI1-D18
PH19	GPIO	I/O	I	Z	LCD1-D19	ERXERR	KP-OUT1	SMC-SDA	EINT19	CSI1-D19

Port	Default Function	IO Type	Default IO State	Default Pull-up/ down	Multi2	Multi3	Multi4	Multi5	Multi6	Multi7
PH20	GPIO	I/O	I	Z	LCD1-D20	ERXDV	CAN-TX	-	EINT20	CSI1-D20
PH21	GPIO	I/O	I	Z	LCD1-D21	EMDC	CAN-RX	-	EINT21	CSI1-D21
PH22	GPIO	I/O	I	Z	LCD1-D22	EMDIO	KP-OUT2	SDC1-CMD	-	CSI1-D22
PH23	GPIO	I/O	I	Z	LCD1-D23	ETXEN	KP-OUT3	SDC1-CLK	-	CSI1-D23
PH24	GPIO	I/O	I	Z	LCD1-CLK	ETXCK	KP-OUT4	SDC1-D0	-	CSI1-PCLK
PH25	GPIO	I/O	I	Z	LCD1-DE	ECRS	KP-OUT5	SDC1-D1	-	CSI1-FIELD
PH26	GPIO	I/O	I	Z	LCD1-HSYNC	ECOL	KP-OUT6	SDC1-D2	-	CSI1-HSYNC
PH27	GPIO	I/O	I	Z	LCD1-VSYNC	ETXERR	KP-OUT7	SDC1-D3	-	CSI1-VSYNC
PI0	GPIO	I/O	I	Z	-	TWI3-SCK	-	-	-	-
PI1	GPIO	I/O	I	Z	-	TWI3-SDA	-	-	-	-
PI2	GPIO	I/O	I	Z	-	TWI4-SCK	-	-	-	-
PI3	GPIO	I/O	I	Z	PWM1	TWI4-SDA	-	-	-	-
PI4	GPIO	I/O	I	Z	SDC3-CMD	-	-	-	-	-
PI5	GPIO	I/O	I	Z	SDC3-CLK	-	-	-	-	-
PI6	GPIO	I/O	I	Z	SDC3-D0	-	-	-	-	-
PI7	GPIO	I/O	I	Z	SDC3-D1	-	-	-	-	-
PI8	GPIO	I/O	I	Z	SDC3-D2	-	-	-	-	-
PI9	GPIO	I/O	I	Z	SDC3-D3	-	-	-	-	-
PI10	GPIO	I/O	I	Z	SPI0-CS0	UART5-TX	-	-	EINT22	-
PI11	GPIO	I/O	I	Z	SPI0-CLK	UART5-RX	-	-	EINT23	-
PI12	GPIO	I/O	I	Z	SPI0-MOSI	UART6-TX	CLK-OUT-A	-	EINT24	-
PI13	GPIO	I/O	I	Z	SPI0-MISO	UART6-RX	CLK-OUT-B	-	EINT25	-
PI14	GPIO	I/O	I	Z	SPI0-CS1	PS2-SCK1	TCLKIN0	-	EINT26	-
PI15	GPIO	I/O	I	Z	SPI1-CS1	PS2-SDA1	TCLKIN1	-	EINT27	-
PI16	GPIO	I/O	I	Z	SPI1-CS0	UART2-RTS	-	-	EINT28	-
PI17	GPIO	I/O	I	Z	SPI1-CLK	UART2-CTS	-	-	EINT29	-
PI18	GPIO	I/O	I	Z	SPI1-MOSI	UART2-TX	-	-	EINT30	-
PI19	GPIO	I/O	I	Z	SPI1-MISO	UART2-RX	-	-	EINT31	-
PI20	GPIO	I/O	I	Z	PS2-SCK0	UART7-TX	HSCL	-	-	-
PI21	GPIO	I/O	I	Z	PS2-SDA0	UART7-RX	HSDA	-	-	-

4.3. DETAILED PIN/SIGNAL DESCRIPTION

Pin/Signal	Description	Type
DRAM		
SDQ[31:0]	DRAM DQ[31:0]	I/O
SVREF	DRAM Reference Input	P
SDQS[3:0]	DRAM Data Strobe DQS[3:0]	I/O
SDQSB[3:0]	DRAM Data Strobe DQSB[3:0]	I/O
SDQM[3:0]	DRAM DQ Mask[3:0]	O
SCK	DRAM Clock	O
SCKB	DRAM CKB	O
SCK1	DRAM Clock	O
SCK1B	DRAM CKB	O
SCKE	DRAM Clock Enable	O
SA[15:0]	DRAM Data Address[15:0]	O

Pin/Signal	Description	Type
SBA[2:0]	DRAM Bank Address[2:0]	O
SWE	DRAM Write Enable	O
SCAS	DRAM Column Address Strobe	O
SRAS	DRAM Row Address Strobe	O
SCS	DRAM Chip Select	O
SODT	DRAM ODT Control	O
SZQ	DRAM ZQ Calibration	A
SRST	DRAM Reset	O
SADBG	DRAM Analog Debug	A
SDDBG0	DRAM Digital Debug	A
SADBG1	DRAM Analog Debug	A
VDD-DLL	DLL Power Supply	P
VCC-DRAM	DRAM Power Supply	P
GPIO		
PA[17:0]	Port A Bit[17:0]	I/O
VCC-PA	Port A Power Supply	P
PB[23:0]	Port B Bit[23:0]	I/O
PC[24:0]	Port C Bit[23:0]	I/O
VCC-PC	Port C Power Supply	P
PD[27:0]	Port D Bit[27:0]	I/O
PE[11:0]	Port E Bit[11:0]	I/O
VCC-PE	Port E Power Supply	P
PF[5:0]	Port F Bit[5:0]	I/O
VCC-PF	Port F Power Supply	P
PG[11:0]	Port G Bit[11:0]	I/O
VCC-PG	Port G Power Supply	P
PH[27:0]	Port H Bit[27:0]	I/O
PI[21:0]	Port I Bit[21:0]	I/O
SYSTEM CONTROL		
BOOTSEL	Boot Mode Select	I
JTAGSEL	JTAG Mode Select	I
TEST	Test Signal	I
NMI#	Non-Maskable Interrupt	I
RESET#	Reset Signal	I
INTERRUPT		
EINT[31:0]	External Interrupt	I
JTAG		
JTAG-DO[1:0]	JTAG Data Output	O
JTAG-DI[1:0]	JTAG Data Input	I
JTAG-MS[1:0]	JTAG Mode Select	I
JTAG-CK[1:0]	JTAG Clock Signal	I
PWM		
PWM[1:0]	PWM	O
CLOCK		
X32KI	Clock Input of 32768Hz Crystal	A
X32KO	Clock Output of 32768Hz Crystal	A
VDD-RTC	RTC Power Supply	P
X24MI	Clock Input of 24MHz Crystal	A
X24MO	Clock Output of 24MHz Crystal	A
PLLVREG	PLL Power	P
VCC-PLL	PLL Power	P
PLLDV	PLL Power	P
PLLTEST	PLL Test Signal	A

Pin/Signal	Description	Type
CLK-OUT-A	Clock OUT A	I/O
CLK-OUT-B	Clock OUT B	I/O
TCLKIN[1:0]	Clock	I/O
NAND FLASH		
NDQ[7:0]	NAND Flash Data Bit[7:0]	I/O
NCE[7:0]	NAND Flash Chip Select[7:0]	O
NWE#	NAND Flash Write Enable	O
NALE	NAND Flash Address Latch Enable	O
NCLE	NAND Flash Command Latch Enable	O
NRE#	NAND Flash Read Enable	O
NRB[1:0]	NAND Flash Ready/Busy Bit	I
NWP	NAND Flash Write Protection	O
NDQS	NAND Flash Data Strobe	I/O
LCD (x=[1:0])		
LCDx-D[23:0]	LCD Data Bit[23:0]	O
LCDx-CLK	LCD Clock Signal	O
LCDx-DE	LCD Data Enable	O
LCDx-HSYNC	LCD Horizontal SYNC	O
LCDx-VSYNC	LCD Vertical SYNC	O
LVDS (x=[1:0])		
LVDS0-VP[3:0]	LVDS Channel0 Data Positive Signal Output[3:0]	A
LVDS0-VN[3:0]	LVDS Channel0 Data Negative Signal Output[3:0]	A
LVDS0-VPC	LVDS Channel0 Clock Positive Output	A
LVDS0-VNC	LVDS Channel0 Clock Negative Output	A
LVDS1-VP[3:0]	LVDS Channel1 Data Positive Signal Output[3:0]	A
LVDS1-VN[3:0]	LVDS Channel1 Data Negative Signal Output[3:0]	A
LVDS1-VPC	LVDS Channel1 Clock Positive Output	A
LVDS1-VNC	LVDS Channel1 Clock Negative Output	A
VCC- LVDS	LVDS Power Supply	P
HDMI		
HTX0P	HDMI Data0 Positive	A
HTX0N	HDMI Data0 Negative	A
HTX1P	HDMI Data1 Positive	A
HTX1N	HDMI Data1 Negative	A
HTX2P	HDMI Data2 Positive	A
HTX2N	HDMI Data2 Negative	A
HTXCP	HDMI Clock Positive	A
HTXCN	HDMI Clock Negative	A
VCC-HDMI	HDMI Power Supply	P
HSCL	HDMI DDC Clock	I/O
HSDA	HDMI DDC Data	I/O
HHPD	HDMI Hot Plug Detection	I/O
HCEC	HDMI CEC	I/O
TV-OUT		
TVOUT[3:0]	TV-out Output[3:0]	A
VCC-TVOUT	TV-out Power Supply	P
CSI (x=[1:0])		
CSI0-D[15:0]	CSI0 Data Bit[15:0]	I
CSI1-D[23:0]	CSI1 Data Bit[23:0]	I
CSIx-PCLK	CSI Pixel Clock	I
CSIx-MCLK	CSI Master Clock	O

Pin/Signal	Description	Type
CSIx-HSYNC	CSI Horizontal SYNC	I
CSIx-VSYNC	CSI Vertical SYNC	I
TV-IN		
TVIN[3:0]	TV-in Input[3:0]	A
VCC-TVIN	TV-in Power Supply	P
VCC25-TVIN	TV-in Power Supply	P
VRP-TVIN	TV-in Reference	A
VRN-TVIN	TV-in Reference	A
USB		
DM[2:0]	USB DM[2:0] Signal	A
DP[2:0]	USB DP[2:0] Signal	A
VCC-USB	USB Power Supply	P
VDD-USB	USB Power	P
TP		
TPX[2:1]	TP ADC Input	A
TPY[2:1]	TP ADC Input	A
AUDIO CODEC		
MICOUTN	MIC Negative Output	A
MICOUTP	MIC Positive Ouput	A
FMINR	FM Right Channel Input	A
FMINL	FM Left Channel Input	A
VMIC	MIC Power Supply	A
MICIN[2:1]	MIC Input	A
VRA1	Reference (1.5V)	A
VRA2	Reference (1.5V)	A
AVCC	Analog Power Supply	P
VRP	Reference (3.0V)	A
LINEINR	Linein Right Channel Input	A
LINEINL	Linein Left Channel Input	A
AGND	Analog Ground	G
HPR	Headphone Right Channel Output	A
HPL	Headphone Left Channel Output	A
GND-HP	Headphone Ground	G
HPCOM	Headphone Common Referene	A
HPCOMFB	Headphone Common Reference Feedback	A
HPBP	Headphone Bypass Output	A
LRADC		
LRADC[1:0]	LRADC Input [1:0]	A
EMAC		
ERXD[3:0]	EMAC MII Receive Data Nibble Data Bit[3:0]	I
ETXD[3:0]	EMAC MII Transmit Data Nibble Data Bit[3:0]	O
ERXCK	EMAC MII Receive Clock	I
ERXERR	EMAC MII Receive Error	I
ERXDV	EMAC Receive Data Valid	I
EMDC	EMAC MII Management Data Clock	O
EMDIO	EMAC MII Management Data Input/Output	I/O
ETXEN	EMAC MII Transmit Enable	O
ETXCK	EMAC MII Transmit Clock	I
ECRS	EMAC MII Carrier Sense	I
ECOL	EMAC MII Collision Detect	I
ETXERR	EMAC MII Transmit Error	O
GMAC		
GRXD[3:0]	GMAC Receive Data[3:0]	I

Pin/Signal	Description	Type
GTXD[3:0]	GMAC Transmit Data[3:0]	O
GNULL/ERXERR	RGMII Null / MII Receive Error	I
GRXCTL/RXDV	RGMII Receive Control / MII Receive Data Valid	I, I
GMDC	GMAC Management Data Clock	O
GMDIO	GMAC Management Data Input/Output	I/O
GTXCTL/ETXEN	RGMII Transmit Control/ MII Transmit Enable	O,O
GNULL/ETXCK	RGMII Null / MII Transmit Clock	I
GTXCK/ECRS	RGMII Transmit Clock / MII Carrier Sense	O,I
GCLKIN/ECOL	RGMII Clock in / MII Collision Detect	I,I
GNULL/ETXERR	RGMII Null / MII Transmit Error	O
SPI (x=[3:0])		
SPIx-CS[1:0]	SPI Chip Select Signal	I/O
SPIx-CLK	SPI Clock Signal	I/O
SPIx-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIx-MISO	SPI Master Data In, Slave Data Out	I/O
UART (x=[7:0])		
UARTx-TX	UART Data Transmit	O
UARTx-RX	UART Data Receive	I
UARTx-RTS	UART Data Request to Send	O
UARTx-CTS	UART Data Clear to Send	I
UARTx-DTR	UART Data Terminal Ready	O
UARTx-DSR	UART Data Set Ready	I
UARTx-DCD	UART Data Carrier Detect	I
UARTx-RING	UART Data Ring Indicator	I
TWI (x=[4:0])(Open-Drain)		
TWIx-SCK	TWI Clock Signal	I/O
TWIx-SDA	TWI Data Signal	I/O
SD/MMC (x=[3:0])		
SDCx-D[3:0]	SD/MMC/SDIO Data Bit[3:0]	I/O
SDCx-CLK	SD/MMC/SDIO Clock	O
SDCx-CMD	SD/MMC/SDIO Command Signa	I/O
KEYPAD		
KP-IN[7:0]	Keypad Data Input	I
KP-OUT[7:0]	Keypad Data Output	O
IR(x=[1:0])		
IRx-TX	IR Data Transmit	I/O
IRx-RX	IR Data Receive	I/O
PS2		
PS2-SCK[1:0]	PS2 Clock Signal	I/O
PS2-SDA[1:0]	PS2 Data Signal	I/O
I2S		
I2S-DO[3:0]	I2S Data Output	O
I2S-DI	I2S Data Input	I
I2S-MCLK	I2S Mater Clock	O
I2S-BCLK	I2S Bit Clock	I/O
I2S-LRCK	I2S Left/Right Select Clock	I/O
I2S1-DO	I2S1 Data Output	O
I2S1-DI	I2S1 Data Input	I
I2S1-BCLK	I2S1 Bit Clock	I/O
I2S1-LRCK	I2S1 Left/Right Select Clock	I/O
I2S1-MCLK	I2S1 Mater Clock	O
AC97		

Pin/Signal	Description	Type
AC97-DO	AC97 Data Output	O
AC97-DI	AC97 Data Input	I
AC97-MCLK	AC97 Master Clock	O
AC97-BCLK	AC97 Bit Clock	I/O
AC97-SYNC	AC97 SYNC Signal	I/O
TS (x=[1:0])		
TSx-D[7:0]	Transport Stream Data Bit[7:0]	I
TSx-CLK	Transport Stream Clock	I
TSx-ERR	Transport Stream Error Indicate	I
TSx-SYNC	Transport Stream SYNC	I
TSx-DVLD	Transport Stream Data Valid	I
CAN		
CAN-TX	CAN Data Transmit	O
CAN-RX	CAN Data Receive	I
SMC		
SMC-RST	Smart Card Reset	O
SMC-VPPEN	Smart Card Program Voltage Enable	O
SMC-VPPPP	Smart Card Program Control	O
SMC-DET	Smart Card Detect	I
SMC-VCCEN	Smart Card Power Enable	O
SMC-SLK	Smart Card Clock	O
SMC-SDA	Smart Card Data	I/O
SATA		
SATA-TXP	SATA Positive Transmit	A
SATA-TXM	SATA Negative Transmit	A
SATA-RXP	SATA Positive Receive	A
SATA-RXM	SATA Negative Receive	A
REXT-SATA	Reference	A
VDD-SATA	SATA Power Supply	P
VDD25-SATA	SATA Power Supply	P
SATA-CLKM	SATA Negative Clock	A
SATA-CLKP	SATA Positve Clock	A
eFUSE		
VDDQE	eFuse Power Supply	P
POWER		
VDD-CPU	CPU Power Supply	P
VDD-SYS	System Power Supply	P
GND	Ground	G
VCC	IO Power Supply	P

4.4. POWER SIGNAL DESCRIPTION

SIGNAL	DESCRIPTION	BALL#
DRAM		
VCC-DRAM	DRAM Power Supply	G5/H5/L5/W5/W6/W7/M5/R5/T5/Y6
VDD-DLL	DLL Power Supply	M8/N9/P9
GPIO		
VCC-PA	Port A Power Supply	H10/J10
VCC-PC	Port C Power Supply	H19/J19

SIGNAL	DESCRIPTION	BALL#
VCC-PE	Port E Power Supply	F19
VCC-PF	Port F Power Supply	N19
VCC-PG	Port G Power Supply	E18
USB		
VCC-USB	USB Power Supply	L16/L15
VDD-USB	USB Power Supply	K16
AUDIO CODEC		
VMIC	MIC Power Supply	AA21
VRA1	Reference(1.5V)	W20
VRA2	Reference (1.5V)	V20
AVCC	Analog Power Supply	T19
VRP	Reference (3.0V)	W21
AGND	Analog Ground	U19
TV-OUT		
VCC-TVOUT	TVOUT power supply	W15
TV-IN		
VCC-TVIN	TVIN Power Supply	W16
VCC25-TVIN	TVIN Power Supply	W17
VRP-TVIN	TVIN BIAS	AA16
VRN-TVIN	TVIN BIAS	Y16
HDMI		
VCC-HDMI	HDMI Power Supply	T13
LVDS		
VCC- LVDS	LVDS Power Supply	W12/W13/W14
RTC		
VDD-RTC	RTC Power Supply	K8
CLOCK		
VCC-PLL	PLL Power Supply	P16
EFUSE		
VDDQE	eFUSE Power Supply	T9
CPU		
VDD-CPU	CPU Power Supply	J12/J13/H11/H12/H13/H14
SYSTEM		
VDD-SYS	System Power Supply	T8/R9/R10/L8/L9/K9/K10/K15/J15/J16
CORE POWER		
GND	Ground	J5/K5/N5/P5/U5/V5/Y7/Y8/G3/G4/L10/L11/ L12/L13/L14/K11/K12/K13/K14J11/M9/M10/ M11/M12/M13/M14/N10/N11/N12/N13/N14/ P10/P11/P12/P13/P14/P15/R11/R12/R13/ T11/T12/W9/W10/W11/W18/Y18/AA18
VCC	IO power supply	H8/H9/J8/J9/J14/H15

5 ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

SYMBOL	PARAMETER		MIN	MAX	UNIT
T_g	Storage Temperature		-40	125	°C
$I_{I/O}$	In/Out current for input and output		-40	40	mA
V_{ESD}	ESD stress voltage	HBM(human body model)	-4K	4K	V_{ESD}
		CDM(charged device model)	-250	250	
VCC	DC Supply Voltage for I/O		-0.3	3.6	V
VDD	DC Supply Voltage for Internal Digital Logic		-0.3	1.4	V
AVCC	DC Supply Voltage for Analog Part		-0.3	3.6	V
VCC-DRAM	Power Supply for DRAM		-0.3	1.98	V
VCC-USB	Power Supply for USB PHY		-0.3	3.6	V
VCC-TVOUT	Power Supply for TV-OUT DAC		-0.3	3.6	V
VCC-PLL	Power Supply for PLL		-0.3	3.6	V
VDD-RTC	Power Supply for RTC		-0.3	1.4	V
VDD-CPU	Power Supply for CPU		-0.3	1.4	V
VDD-SYS	Power Supply for System		-0.3	1.4	V

5.2. RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_a	Ambient Operating Temperature[Commercial]	-20	-	+70	°C
VCC	DC Supply Voltage for I/O	1.7	1.8~3.3	3.6	V
VDD	DC Supply Voltage for Internal Digital Logic	1.0	-	1.4	V
AVCC	DC Supply Voltage for Analog Part	2.7	3.0	3.3	V
VCC-DRAM	Power Supply for DRAM	1.28	-	1.98	V
VCC-USB	Power Supply for USB PHY	3.0	3.3	3.45	V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VCC-TVOUT	Power Supply for TV-OUT DAC	3.0	3.3	3.6	V
VCC-TVIN	Power Supply for TV-in	3.0	3.3	3.6	V
VCC25-TVIN	Power Supply for TV-in	-	2.5	-	V
VCC-PLL	Power Supply for PLL	2.7	3.0	3.3	V
VCC-LVDS	Power Supply for LVDS	-	3.3	-	V
VDD-RTC	Power Supply for RTC	1.2	1.3	1.4	V
VDD-CPU	Power Supply for CPU	1.0	-	1.4	V
VDD-SYS	Power Supply for System	1.0	-	1.4	V

5.3. DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage	VCC=3.3V	0.7*VCC	-	VCC+0.3	V
V_{IL}	Low-Level Input Voltage	VCC=3.3V	-0.3	-	0.3*VCC	V
V_{HYS}	Hysteresis Voltage	-	-	-	-	mV
I_{IH}	High-Level Input Current	VCC=3.3V, VI=3.3V	-	-	10	uA
I_{IL}	Low-Level Input Current	VCC=3.3V, VI=0V	-	-	10	uA
V_{OH}	High-Level Output Voltage	VCC=3.3V	VCC-0.2	-	-	V
V_{OL}	Low-Level Output Voltage	VCC=3.3V	-	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current	VCC=3.3V	-10	-	10	uA
C_{IN}	Input Capacitance	-	-	-	5	pF
C_{OUT}	Output Capacitance	-	-	-	5	pF

5.4. OSCILLATOR ELECTRICAL CHARACTERISTICS

The A20 contains two oscillators: a 24MHz oscillator and a 32768Hz oscillator. Each oscillator requires a specific crystal.

The A20 device operation requires following two input clocks:

- The 32768Hz frequency is used for low frequency operation.
- The 24MHz frequency is used to generate the main source clock of the A20 device.

5.4.1. 24MHz OSCILLATOR CHARACTERISTICS

The 24.0MHz crystal is connected between the HOSCI (amplifier input) and HOSCO (amplifier output).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	24	-	MHz
t_{ST}	Startup Time	-	-	-	ms

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
	Frequency Tolerance at 25°C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

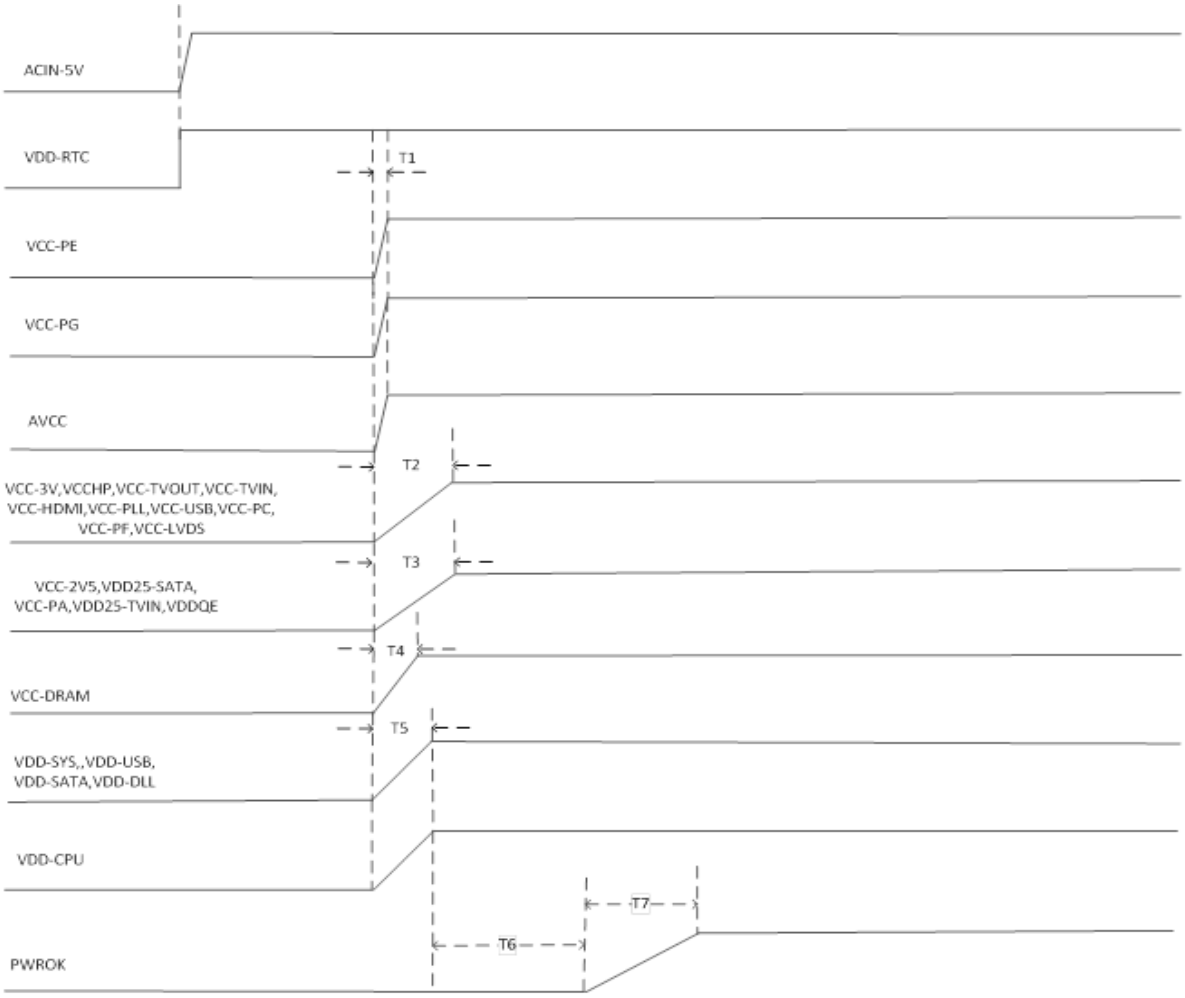
5.4.2. 32768HZ OSCILLATOR CHARACTERISTICS

The 32768Hz crystal is connected between the LOSCI (amplifier input) and LOSCO (amplifier output).

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
1/(tCPMAIN)	Crystal Oscillator Frequency Range	-	32768	-	Hz
t_{ST}	Startup Time	-	-	-	ms
	Frequency Tolerance at 25°C	-50	-	+50	ppm
	Oscillation Mode	Fundamental			-
	Maximum Change Over Temperature Range	-50	-	+50	ppm
PON	Drive Level	-	-	50	uW
CL	Equivalent Load Capacitance	-	-	-	pF
CL1,CL2	Internal Load Capacitance(CL1=CL2)	-	-	-	pF
RS	Series Resistance(ESR)	-	-	-	Ω
	Duty Cycle	30	50	70	%
CM	Motional Capacitance	-	-	-	pF
C_{SHUT}	Shunt Capacitance	-	-	-	pF
R_{BIAS}	Internal Bias Resistor	-	-	-	MΩ

5.5. POWER UP/DOWN SEQUENCE

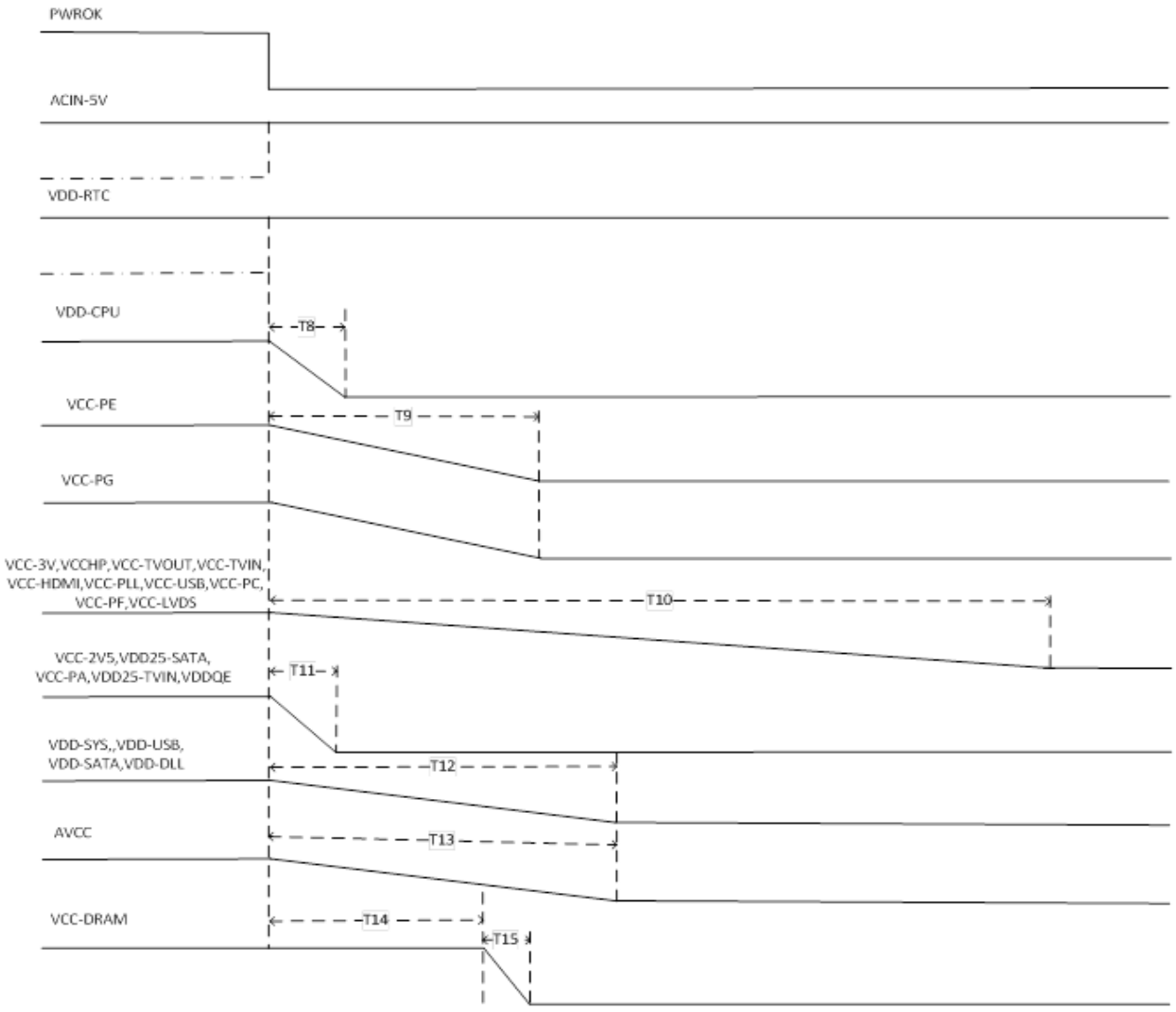
The following figure shows an example of the power-up sequence for A20 device.During the entire power-up sequence,the PWROK pin must be held low until all power domains are stable.



Parameter	Symbol	Min	Typ	Max	Unit
AXP209 LDO2/3/4 Ramp Up Rate	T1	50	100	200	us
SY8021L DCDC1(VCC-3V) Ramp Up Rate	T2	500	1200	2000	us
AP1231(VCC-2V5) Ramp Up Rate	T3	500	1200	2000	us
SY8021L DCDC1(VCC-DRAM) Ramp Up Rate	T4	500	800	2000	us
AXP209 DCDC3(VDD-SYS) Ramp Up Rate	T5	500	1000	2000	us
AXP209 DCDC2(VDD-CPU) Ramp Up Rate	T5	500	1000	2000	us

AXP209 PWROK Start Up after All Domains are Stable	T6	50	64	80	ms
PWROK Ramp Up Rate	T7	35	50	80	ms

The following figure shows an example of the power-down sequence for A20 device.Power-down is achieved by setting PWRON input to 0.When this occurs,except VCC-DRAM,other voltages ramp down at the same time.The ramp down rate of each voltage is generally determined by the load on that voltage.Depending on the different application solution,the ramp down rate of each voltage is different.

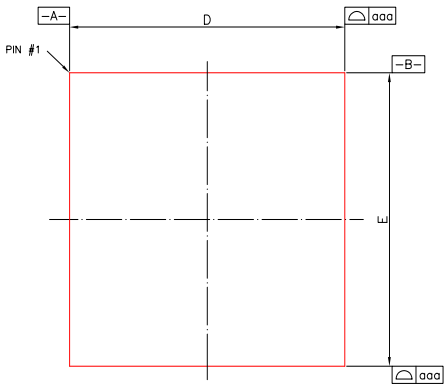


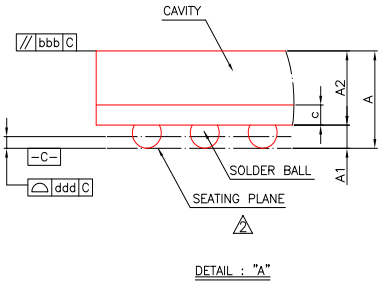
6 PIN ASSIGNMENT

6.1. PIN MAP

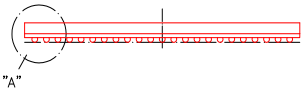
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	PH15	PH13	PH10	PH6	PH3	PH0	PB22	PB18	PB16	PB14	PB8	PB6	PB4	PB2	PB0	PI8	PI6	PI4	PI2	PI0	PE11	PE9	PE8	A
B	PH16	PH14	PH11	PH7	PH4	PH1	PB23	PB19	PB17	PB15	PB13	PB7	PB5	PB3	PB1	PI9	PI7	PI5	PI3	PI1	PE10	PE7	PE6	B
C	PH17	PH18	PH12	PH8	PH5	PH2	PB21	PB20	PB12	PB11	PB10	PB9	PA17	RESET#	PI14	PI12	PI10	PG11	PG9	PG7	PG5	PE5	PE4	C
D	PH19	PH20	PH21	PH9	PA0	PA2	PA4	PA6	PA8	PA10	PA12	PA14	PA16	PI19	PI15	PI13	PI11	PG10	PG8	PG4	PG3	PE3	PE2	D
E	PH22	PH23	PH24	PH25	PA1	PA3	PA5	PA7	PA9	PA11	PA13	PA15	PI21	PI20	PI18	PI17	PI16	VCC-PG	PG6	PG2	PG1	PE1	PE0	E
F	X32KI	X32KO	PH26	PH27	NMI#														VCC-PE	PG0	PC24	PC18	PC17	F
G	SDQM3	SDQ29	GND	GND	VCC-DRAM														PC23	PC15	PC14	PC11	PC10	G
H	SDQ26	SDQ31	SVREF	SVREF	VCC-DRAM			VCC	VCC	VCC-PA	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	VCC	TEST			VCC-PC	PC13	PC12	PC9	PC8	H
J	SDQ24	SDQS3B	SCK1B	SCK1	GND			VCC	VCC	VCC-PA	GND	VDD-CPU	VDD-CPU	VCC	VDD-SYS	VDD-SYS			VCC-PC	PC22	PC21	PC7	PC6	J
K	SDQS3	SDQ27	SBA0	SBA2	GND			VDD-RTC	VDD-SYS	VDD-SYS	GND	GND	GND	GND	VDD-SYS	VDD-USB			PF5	PF4	PC20	PC5	PC4	K
L	SDQ25	SDQ28	SA10	SBA1	VCC-DRAM			VDD-SYS	VDD-SYS	GND	GND	GND	GND	GND	VCC-USB	VCC-USB			PF3	PF2	PC19	PC3	PC2	L
M	SDQ30	SDQ23	SA7	SA3	VCC-DRAM			VDD-DLL	GND	GND	GND	GND	GND	GND	VDD-SATA	VDD-SATA			PF1	PF0	PC16	PC1	PC0	M
N	SDQ22	SDQ17	SCKE	SA5	GND			SADBG	VDD-DLL	GND	GND	GND	GND	GND	VDD25-SATA	VDD25-SATA			VCC-PF	DM0	DP0	X24MO	X24MI	N
P	SDQ19	SDQS2B	SA12	SA9	GND			SDDBG0	VDD-DLL	GND	GND	GND	GND	GND	GND	VCC-PLL			SATA-CLKM	DM1	DP1	HHPD	HCEC	P
R	SDQS2	SDQM2	SA14	SA1	VCC-DRAM			SDDBG1	VDD-SYS	VDD-SYS	GND	GND	GND	NC	PLLVREG	NC			SATA-CLKP	DM2	DP2	HSDA	HSCL	R
T	SDQ20	SDQ16	SWE	SRAS	VCC-DRAM			VDD-SYS	VDDQE	JTAG-SEL	GND	GND	VCC-HMDI	HVREG1	PLLTEST	PLLDV			AVCC	SATA-TXP	SATA-TXM	HTX2N	HTX2P	T
U	SDQ21	SDQ18	SCAS	SA2	GND														AGND	SATA-RXM	SATA-RXP	HTX1N	HTX1P	U
V	SCK	SCKB	SCS	SA6	GND														GND-HP	VRA2	REXT-SATA	HTX0N	HTX0P	V
W	SDQM1	SDQ13	SA11	SA0	VCC-DRAM	VCC-DRAM	VCC-DRAM	BOOTSEL	GND	GND	GND	VCC-LVDS	VCC-LVDS	VCC-LVDS	VCC-TVOUT	VCC-TVIN	VCC25-TVIN	GND	HPR	VRA1	VRP	HTXCN	HTXCP	W
Y	SDQ10	SDQ15	SA13	SA4	SVREF	VCC-DRAM	GND	GND	PD24	PD20	PD18	PD16	PD14	PD12	PD10	VRN-TVIN	TVIN3	GND	HPL	FMINL	FMINR	TPX1	TPY1	Y
AA	SDQ8	SDQS1B	SA8	SA15	SODT	SRST	SZQ	SVREF	PD25	PD21	PD19	PD17	PD15	PD13	PD11	VRP-TVIN	TVIN2	GND	HPCOM	HPCOMFB	VMIC	TPX2	TPY2	AA
AB	SDQS1	SDQ11	SDQ14	SDQ6	SDQ3	SDQS0	SDQ4	SDQ5	PD26	PD22	PD8	PD6	PD4	PD2	PD0	TVOUT1	TVOUT3	TVIN1	VCC-HP	LINEINL	LINEINR	LRADC1	LRADC0	AB
AC	SDQ9	SDQ12	SDQ7	SDQ1	SDQS0B	SDQM0	SDQ0	SDQ2	PD27	PD23	PD9	PD7	PD5	PD3	PD1	TVOUT0	TVOUT2	TVIN0	HPBP	MICIN1	MICIN2	MICOUTP	MICOUTN	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

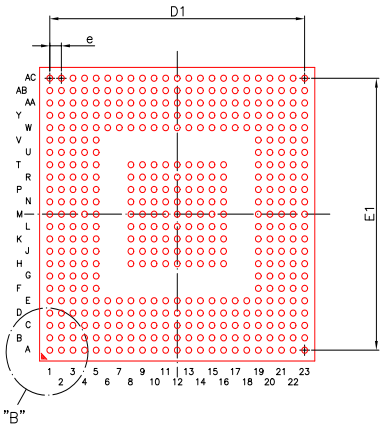
6.2. PACKAGE DIMENSION

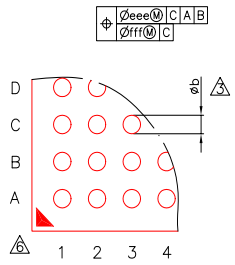




DETAIL : "A"







DETAIL : "B"

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.40	---	---	0.055
A1	0.25	0.30	0.35	0.010	0.012	0.014
A2	0.91	0.96	1.01	0.036	0.038	0.040
b	0.35	0.40	0.45	0.014	0.016	0.018
c	0.22	0.26	0.30	0.009	0.010	0.012
D	18.90	19.00	19.10	0.744	0.748	0.752
E	18.90	19.00	19.10	0.744	0.748	0.752
D1	---	17.60	---	---	0.693	---
E1	---	17.60	---	---	0.693	---
e	---	0.80	---	---	0.031	---
aaa	0.15			0.006		
bbb	0.20			0.008		
ddd	0.20			0.008		
eee	0.15			0.006		
fff	0.08			0.003		
MD/ME	23/23			23/23		