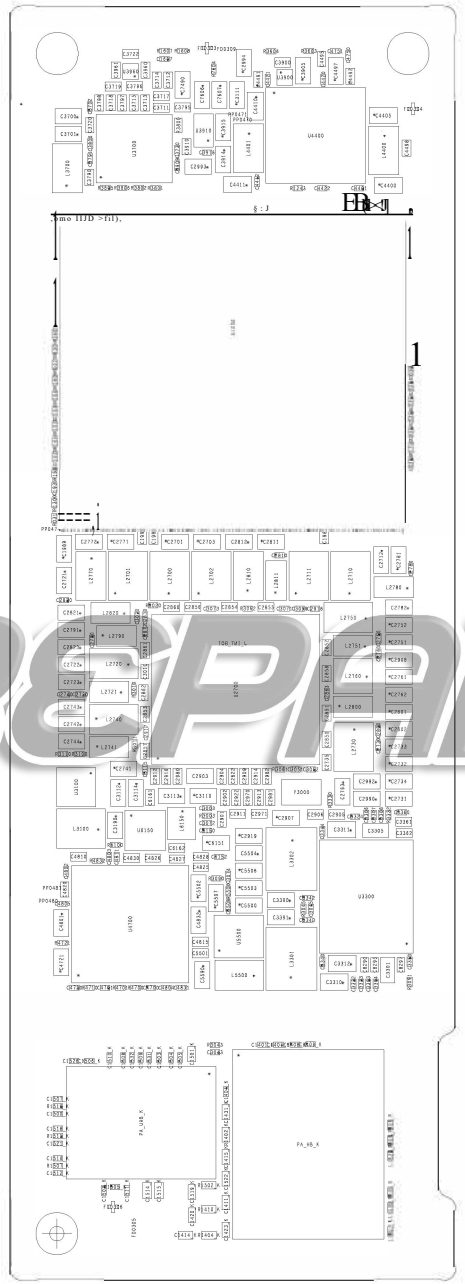
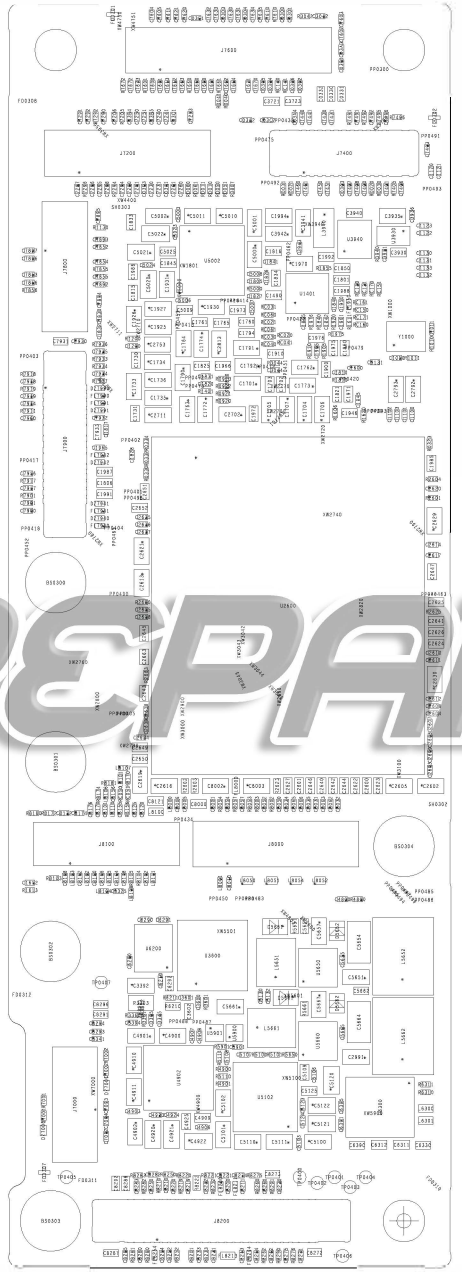


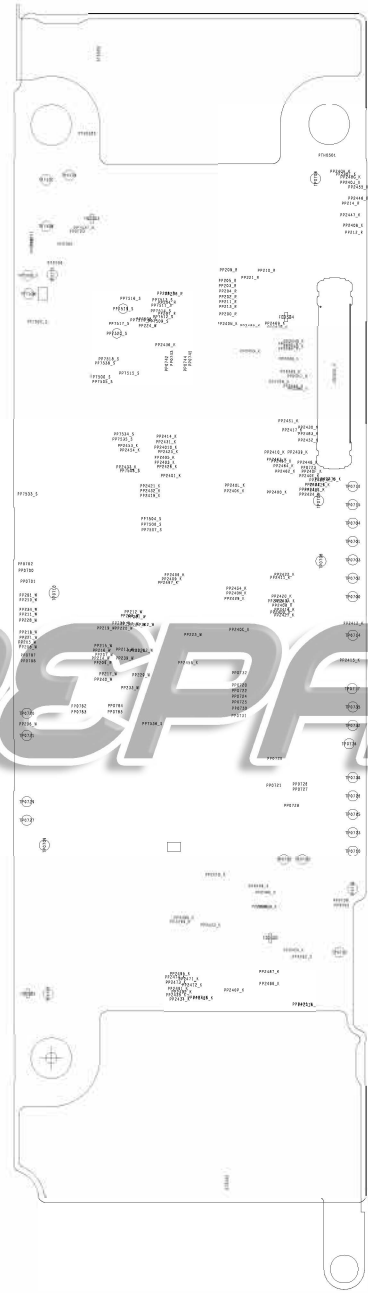
BOTTOM SIDE ASSEMBLY



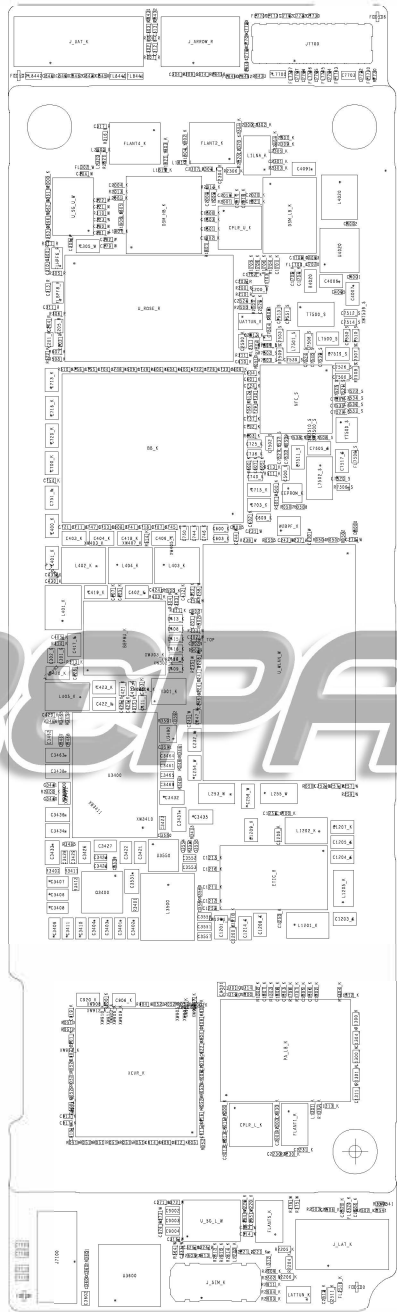
TOP SIDE ASSEMBLY

BOTTOM SIDE ASSEMBLY

TOP SIDE ASSEMBLY



BOTTOM SIDE ASSEMBLY



TOP SIDE ASSEMBLY

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

N104 TOP MLB - CRB

LAST_MODIFICATION=Sun Apr 14 18:20:31 2019

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0017191502	ENGINEERING RELEASED	2019-04-14

Sub Designs

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/SOFT	SYNC_DATE/TIME
N104	RADIO_MLB_ICE_LOFT	0.46.0	S	2019_02_05_16:59:54

051-04047	1	SCH,MLB_TOP,N104	SCH	CRITICAL	?
820-01523	1	PCB,MLB_TOP,N104	PCB	CRITICAL	?

NAND

Ultimate

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00377	1	HYNIX, 3DV4, ULTIMATE	U2600	CRITICAL	ULTIMATE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00393	335S00377	ALT_PARTS	U2600	TOSHIBA, BICS4, ULTIMATE
335S00388	335S00377	ALT_PARTS	U2600	WD, BICS4, ULTIMATE
335S00416	335S00377	ALT_PARTS	U2600	SAMSUNG, 3DV5, ULTIMATE

Supreme

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00394	1	TOSHIBA, BICS4, SUPREME	U2600	CRITICAL	SUPREME

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00389	335S00394	ALT_PARTS	U2600	WD, BICS4, SUPREME
335S00378	335S00394	ALT_PARTS	U2600	HYNIX, 3DV4, SUPREME

Extreme

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00379	1	HYNIX, 3DV4, EXTREME	U2600	CRITICAL	EXTREME

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00358	335S00379	ALT_PARTS	U2600	TOSHIBA, BICS3, EXTREME
335S00390	335S00379	ALT_PARTS	U2600	WD, BICS4, EXTREME
335S00247	335S00379	ALT_PARTS	U2600	WD, BICS3, EXTREME
335S00415	335S00379	ALT_PARTS	U2600	SAMSUNG, 3DV5, EXTREME

Global Ferrites

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00194	155S00610	ALT_PARTS	ALL	FERR BD, 150OHM, TDK
155S00200	155S00610	ALT_PARTS	ALL	FERR BD, 150OHM, TY

AVUS INDUCTORS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00721	152S00876	ALT_PARTS	ALL	Taiyo,IND,WLD,33M,3.6A,60MΩ,2016
152S00930	152S00897	ALT_PARTS	ALL	Cyntec,IND,CPLD,0.33M,6.1A,27MΩ,2016
152S00826	152S00821	ALT_PARTS	ALL	Taiyo,IND,WLD,33M,2.2A,68MΩ,2012
152S00831	152S00818	ALT_PARTS	ALL	Taiyo,IND,WLD,0.22UH,5.3A,49MΩ,1608
152S00994	152S00987	ALT_PARTS	ALL	Taiyo,IND,WLD,33M,1.5A,67MΩ,2012
152S00991	152S00984	ALT_PARTS	ALL	Taiyo,IND,WLD,0.47UH,3.5A,34MΩ,1614
152S00992	152S00985	ALT_PARTS	ALL	Taiyo,IND,WLD,0.47UH,4.6A,45MΩ,2012
152S00989	152S00982	ALT_PARTS	ALL	Taiyo,IND,WLT,0.47UH,2.5A,79MΩ,1608
152S00826	152S00981	ALT_PARTS	ALL	Taiyo,IND,WLD,33M,2.5A,52MΩ,2012

CRITICAL PART#	COMMENT
152S00876	Cyntec,IND
152S00897	Taiyo,IND
152S00821	Cyntec,IND
152S00818	Cyntec,IND
152S00987	Cyntec,IND
152S00984	Cyntec.IND
152S00985	Cyntec,IND
152S00982	Cyntec,IND
152S00981	Cyntec,IND

Global Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	ALT_PARTS	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005
138S0648	138S0652	ALT_PARTS	ALL	CAP,X5R,4.7UF,6.3V,0.65MM,0402,TAIYO
138S0739	138S0706	ALT_PARTS	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S00049	138S0831	ALT_PARTS	ALL	CAP,CER,X5R,2.2UF,20%,6.3V,0201,KYOCERA
138S0945	138S0706	ALT_PARTS	ALL	CAP,CER,X5R,1UF,20%,10V,0201,KYOCERA
155S00200	155S00400	ALT_PARTS	ALL	FERR BD,150 OHM,25%,200MA,0.7 DCR,01005
155S00414	155S0876	ALT_PARTS	ALL	FERR BD,10 OHM,50%,1.1A,0.05 DCR,01005
132S00199	132S00200	ALT_PARTS	ALL	CAP,CER,X5R,0.1UF,20%,10V,01005
132S00204	132S00200	ALT_PARTS	ALL	CAP,CER,X5R,0.1UF,20%,10V,01005
155S0755	155S00341	ALT_PARTS	ALL	FERR BD,240 OHM,25%,200MA,1.0 DCR,01005
132S0400	132S0436	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,20%,6.3V,01005
138S00264	138S00008	ALT_PARTS	ALL	CAP,CER,X5R,1.5UF,20%,6.3V,0201
132S00232	132S00014	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,10%,6.3V,01005
132S00233	132S00014	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,10%,6.3V,01005
371S00062	371S00101	ALT_PARTS	ALL	DIODE,SCHOTTKY,30V,250MW,0201
377S00061	377S0183	ALT_PARTS	ALL	TVS,0201R,5.0V,0201
377S00070	377S00001	ALT_PARTS	ALL	TVS,0201R,5.0V,6PF,01005,STM
377S00140	377S00001	ALT_PARTS	ALL	TVS,0201R,5V,6PF,01005,SEMTECH
377S0168	377S00129	ALT_PARTS	ALL	SUPPRESS,TRANS,6.0V,180PF,AMOTECH,01005
118S00144	118S00012	ALT_PARTS	ALL	RES,TK,2490HM,1%,200PPM,1/32W,01005,CYN
138S00284	138S00136	ALT_PARTS	ALL	CAP,CER,X5R,2.2UF,20%,10V,0201,KYO
131S00329	131S00025	ALT_PARTS	ALL	CAP,CER,1000PF,2%,25V,0201,TAIYO
132S00088	132S0639	ALT_PARTS	ALL	CAP,CER,0.47UF,20%,25V,0201,TAIYO
138S0719	138S1103	ALT_PARTS	ALL	CAP,CER,4.7UF,20%,10V,0402,MURATA
152S00655	152S00656	ALT_PARTS	ALL	IND,WLD,1.0UH,20%,3A,2016,TAIYO
131S00118	138100299	ALT_PARTS	ALL	CAP,CER,100PF,2%,50V,0201,MURATA
155S00437	155S00402	ALT_PARTS	ALL	FERR BD,330HM,25%,1.6A,0201,TDK
155S00339	155S0660	ALT_PARTS	ALL	FERR BD,220HM,25%,1.6A,0201,TAIYO

Global Capacitors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00116	138S00071	ALT_PARTS	ALL	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55,TY
138S00117	138S00071	ALT_PARTS	ALL	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55,KYO

CRITICAL PART#	COMMENT
138S00071	CAP,CER,X5R,4UF,20%,6.3V,0201,H=0.55

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00140	138S00141	ALT_PARTS	ALL	CAP,3.9UF,20%,6.3V,KYO,0201
138S00268	138S00141	ALT_PARTS	ALL	CAP,3.0UF,20%,6.3V,SAM,0201

CRITICAL PART#	COMMENT
138S00141	CAP,X5R,4.0UF,20%,6.3V,MUR,0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00148	138S00149	ALT_PARTS	ALL	CAP,15UF,20%,4V,KYO,0402
138S00150	138S00149	ALT_PARTS	ALL	CAP,15UF,20%,4V,SAM,0402
138S00151	138S00149	ALT_PARTS	ALL	CAP,15UF,20%,4V,TY,0402

CRITICAL PART#	COMMENT
138S00149	CAP,X5R,14UF,20%,4V,MUR,0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00144	138S00279	ALT_PARTS	ALL	CAP,26UF,20%,4V,MUR,0402

CRITICAL PART#	COMMENT
138S00144	CAP,X5R,26UF,20%,4V,MUR,0402
138S00279	CAP,X5R,20UF,20%,4V,SAM,0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	ALT_PARTS	ALL	CAP,4.7UF,20%,4V,KYO,0201
138S00164	138S00139	ALT_PARTS	ALL	CAP,4UF,20%,4V,TY,0201
138S00280	138S00139	ALT_PARTS	ALL	CAP,4UF,20%,4V,SAM,0201

CRITICAL PART#	COMMENT
138S00139	CAP,X5R,4.0UF,20%,4V,MUR,0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00221	138S00146	ALT_PARTS	ALL	CAP,18UF,20%,6.3V,KYO,0402

CRITICAL PART#	COMMENT
138S00146	CAP,X5R,18UF,20%,6.3V,MUR,0402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00003	138S00048	ALT_PARTS	ALL	0402,15uF,6.3V, Murata

CRITICAL PART#	COMMENT
138S00003	0402,15uF,6.3

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00128	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,TY

CRITICAL PART#	COMMENT
138S00133	01005,0.47uF, 6.3V

Display CMC's

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S00391	155S00415	ALT_PARTS	ALL	CMC,350SM,7GHz,TDK

XTAL Alternate

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0612	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612
197S00120	197S00118	ALT_PARTS	Y1000	XTAL, 24M, 1612

CEBU DEFAULT

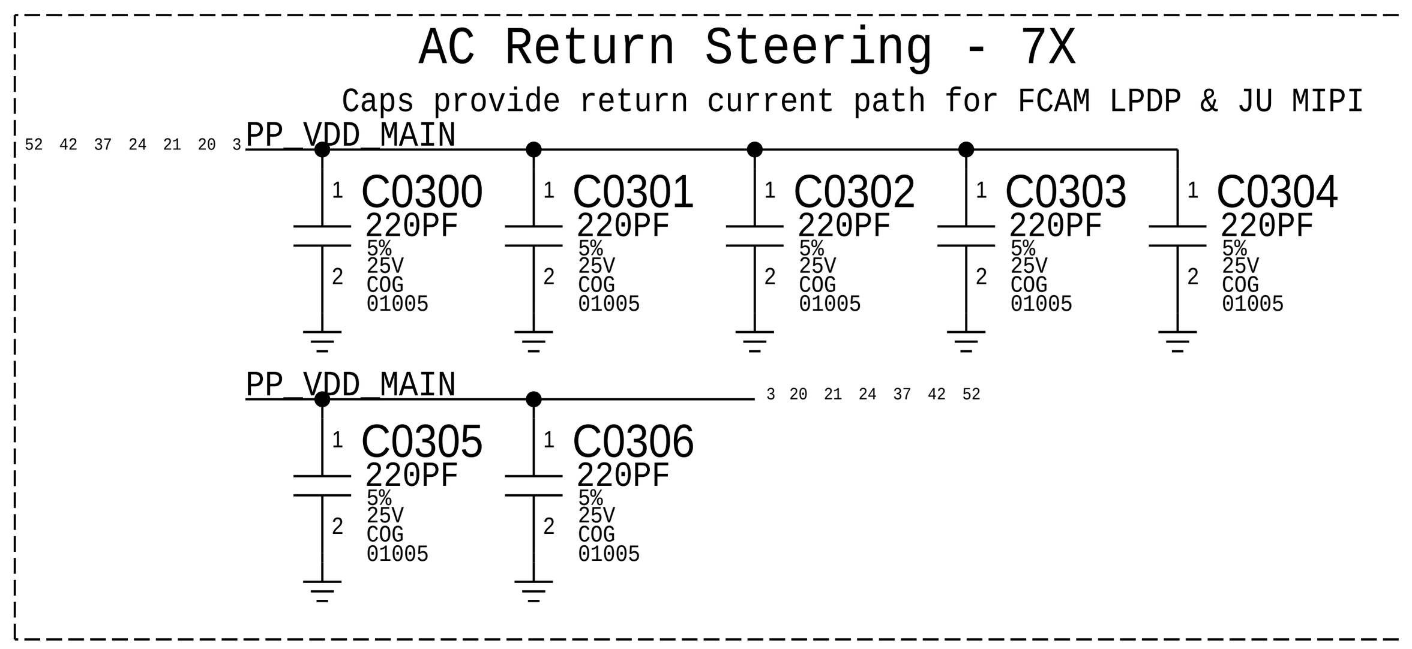
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00623	1	CEBU B0 4GB HYNIX 18NM	U1000	CRITICAL	ALL

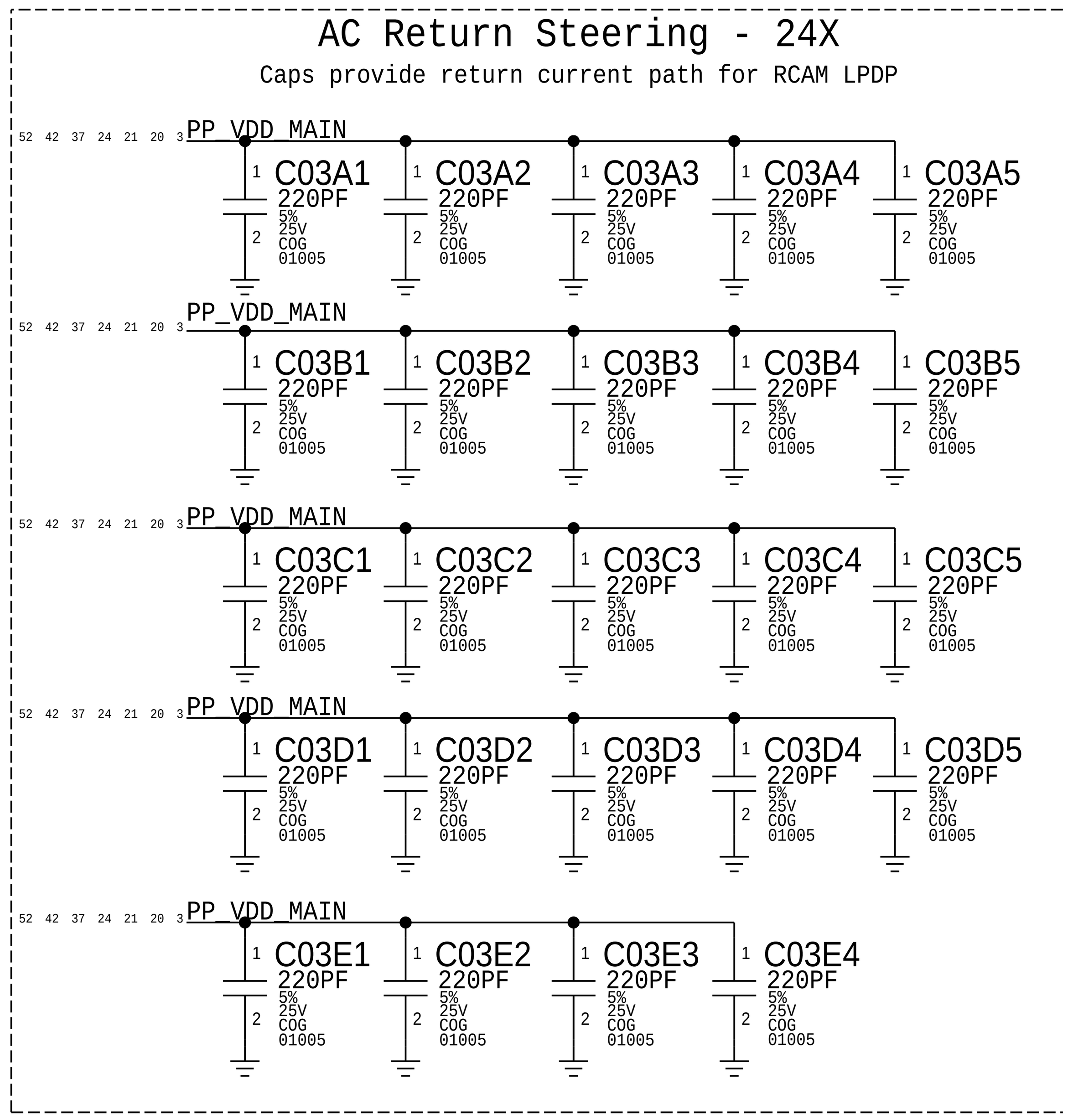
CEBU ALTS

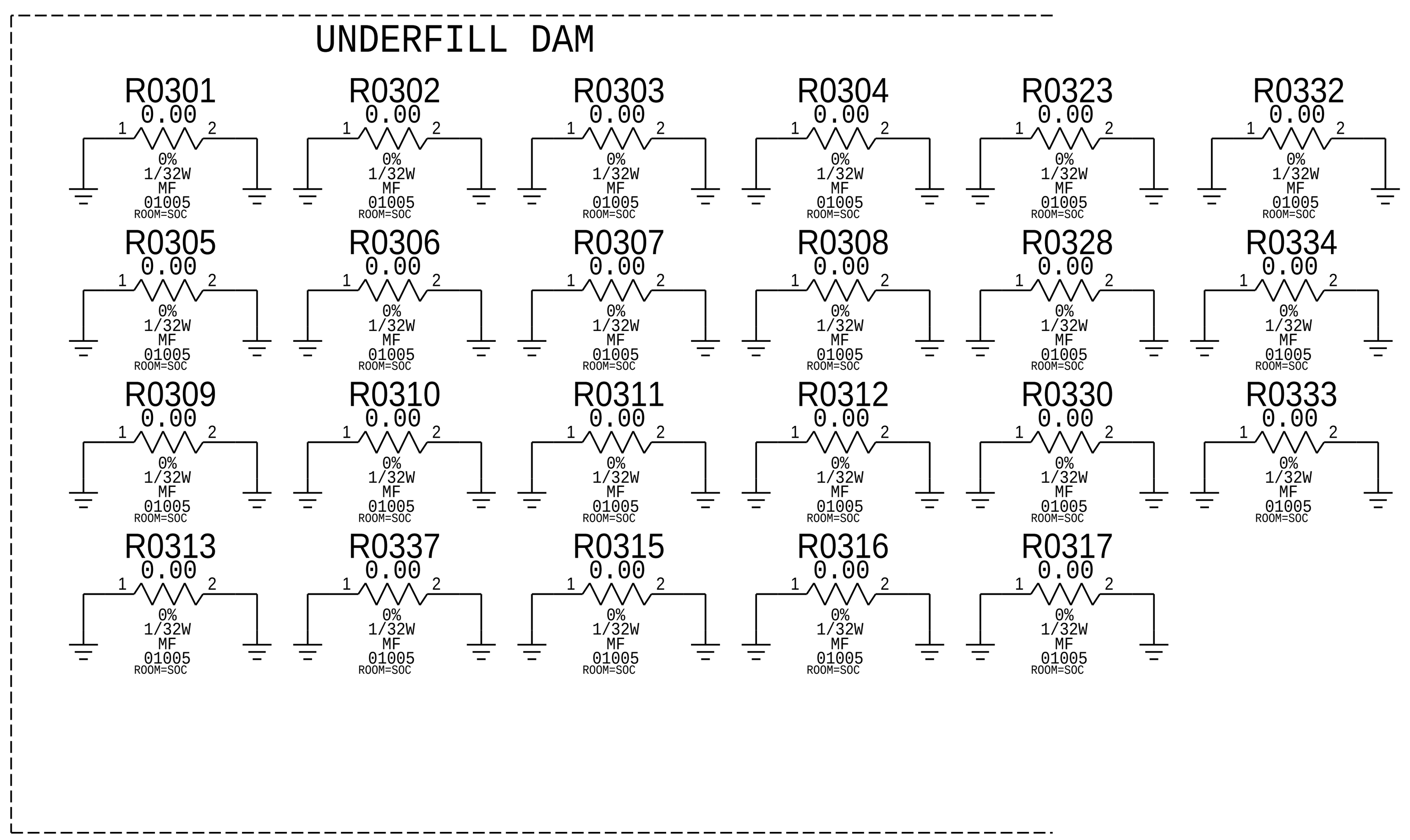
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00624	339S00623	ALT_PARTS	U1000	CEBU B0 4GB MICRON 18NM
339S00625	339S00623	ALT_PARTS	U1000	CEBU B0 4GB SAMSUNG 16NM

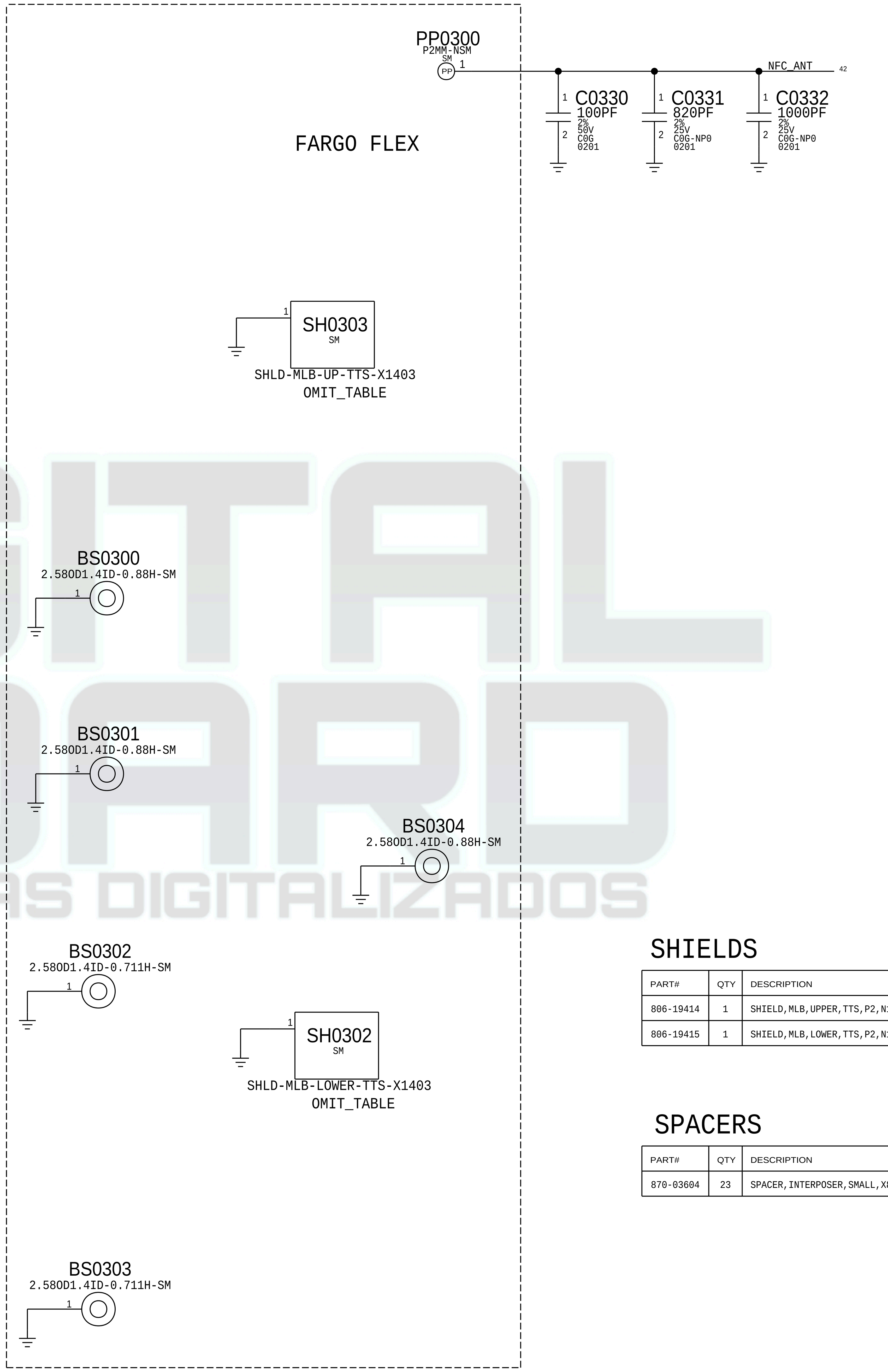
EEEE Codes

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7691	1	EEEE FOR (MLB_TOP,639-06358,ULTIMATE)	EEEE_KF2F	CRITICAL	ULTIMATE
825-7691	1	EEEE FOR (MLB_TOP,639-06359,SUPREME)	EEEE_KF2R	CRITICAL	SUPREME
825-7691	1	EEEE FOR (MLB_TOP,639-06360,EXTREME)	EEEE_KF34	CRITICAL	EXTREME
825-7691	1	EEEE FOR (MLB_TOP,639-06949,ULTIMATE)	EEEE_L6R1	CRITICAL	ULTIMATE
825-7691	1	EEEE FOR (MLB_TOP,639-06951,SUPREME)	EEEE_L6RQ	CRITICAL	SUPREME
825-7691	1	EEEE FOR (MLB_TOP,639-06952,EXTREME)	EEEE_L6T3	CRITICAL	EXTREME

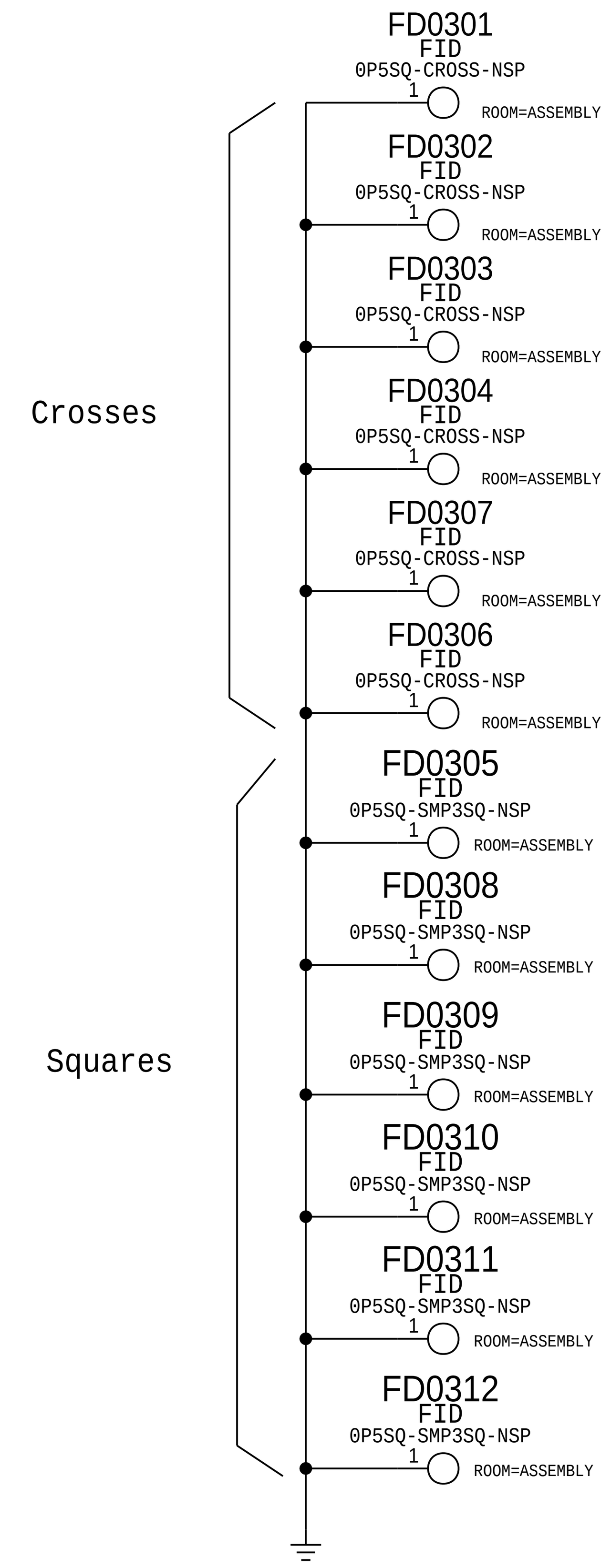








FIDUCIALS



SHIELDS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-19414	1	SHIELD,MLB,UPPER,TTS,P2,N104	SH0303	CRITICAL	?
806-19415	1	SHIELD,MLB,LOWER,TTS,P2,N104	SH0302	CRITICAL	?

SPACERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
870-03604	23	SPACER,INTERPOSER,SMALL,X891	SP1-SP26	CRITICAL	?

TEST POINTS

41 36	IN	PP_HYDRA_ACC1	TP0400 TP TP-P55
51 41	IN	90_HYDRA_DP1_CONN_P	TP0401 TP TP-P55
51 41	IN	90_HYDRA_DP1_CONN_N	TP0402 TP TP-P55
51 41	IN	90_HYDRA_DP2_CONN_P	TP0403 TP TP-P55
51 41	IN	90_HYDRA_DP2_CONN_N	TP0404 TP TP-P55
51	IN	CON_DETECT_E75_TO_HYDRA_CONN_L	TP0405 TP TP-P55
51 41	IN	PP_HYDRA_ACC2	TP0406 TP TP-P55
42 24	IN	PP_VBUS1_E75	TP0407 TP TP-P55

BUMP SENSE

17	IN	ANALOG_GPU_SENSEN	PP0453 P2MM-NSM SM 1 PP ROOM=TEST
14	IN	ANALOG_GPU_SENSEP	PP0413 P2MM-NSM SM 1 PP ROOM=TEST
17	IN	ANALOG_CPU_PCORE_SENSEN	PP0451 P2MM-NSM SM 1 PP ROOM=TEST
14	IN	ANALOG_CPU_PCORE_SENSEP	PP0412 P2MM-NSM SM 1 PP ROOM=TEST
17	IN	ANALOG_SOC_SENSEN	PP0416 P2MM-NSM SM 1 PP ROOM=TEST
14	IN	ANALOG_SOC_SENSEP	PP0414 P2MM-NSM SM 1 PP ROOM=TEST
16	IN	ANALOG_DCS_SENSEP	PP0417 P2MM-NSM SM 1 PP ROOM=TEST
17	IN	ANALOG_VDDQL_DCS_SENSEN	PP0452 P2MM-NSM SM 1 PP ROOM=TEST
16	IN	ANALOG_VDDQL_SENSEP	PP0418 P2MM-NSM SM 1 PP ROOM=TEST

SOC Debug

22 7	IN	CLK_AP_TO_PMU_TST_CLKOUT	PP0400 P2MM-NSM SM 1 PP ROOM=TEST
7 6	IN	GPIO_BOARD_ID0	PP0401 P2MM-NSM SM 1 PP ROOM=TEST
37 9	IN	GPIO_ISP_TO_DISPLAY_FLASH_INT	PP0402 P2MM-NSM SM 1 PP ROOM=TEST
42 41 9 45 44	IN	GPIO_ISP_RCAM_TO_STROBE_TRIGGER	PP0403 P2MM-NSM SM 1 PP ROOM=TEST
7	IN	PROBE_DFU_STATUS	PP0404 P2MM-NSM SM 1 PP ROOM=TEST
22 7	IN	IO_PMU_TO_AP_PRE_UVLO_L	PP0405 P2MM-NSM SM 1 PP ROOM=TEST

PMU

13	IN	PROBE_AOP_TO_DDR_SLEEP1	PP0420 P2MM-NSM SM 1 PP ROOM=TEST
41 22 7	IN	IO_PMU_TO_AP_HYDRA_ACTIVE_READY	PP0422 P2MM-NSM SM 1 PP ROOM=TEST

NAND

18 11 6	IN	SPI0_AP_FROM_S4E_MISO_BOOT_CONFIG2	PP0462 P2MM-NSM SM 1 PP ROOM=TEST
18	IN	ANALOG_NAND_ANI0_VREF	PP0463 P2MM-NSM SM 1 PP ROOM=TEST
18	IN	ANALOG_NAND_ANI1_VREF	PP0464 P2MM-NSM SM 1 PP ROOM=TEST
18 7	IN	IO_AP_TO_NAND_RESET_L	PP0465 P2MM-NSM SM 1 PP ROOM=TEST

PCIE Refclk

18 8	IN	90_PCIE0_AP_TO_NAND_REFCLK_P	PP0430 P2MM-NSM SM 1 PP ROOM=TEST
18 8	IN	90_PCIE0_AP_TO_NAND_REFCLK_N	PP0431 P2MM-NSM SM 1 PP ROOM=TEST

Hydra VBUS

41 24	IN	IO_HYDRA_TO_CHARGER_VBUS1_VALID_L	PP0450 P2MM-NSM SM 1 PP ROOM=TEST

Rigel

30 28	IN	GPIO_CAM_PMU1_TO_RIGEL_ENABLE	PP0470 P2MM-NSM SM 1 PP ROOM=TEST
30 28 22	IN	GPIO_CAM_PMU1_FROM_RIGEL_INT	PP0471 P2MM-NSM SM 1 PP ROOM=TEST

DISPLAY

49	IN	DISPLAY_TEST	PP0434 P2MM-NSM SM 1 PP ROOM=TEST

SPMI DATA

28 9	IN	SPMI_ISP_BI_CAM_PMU1_DATA	PP0432 P2MM-NSM SM 1 PP ROOM=TEST

SWD

41 13	IN	SWD_DOCK_TO_AP_SWCLK	PP0480 P2MM-NSM SM 1 PP ROOM=TEST
41 13	IN	SWD_DOCK_BI_AP_SWDIO	PP0481 P2MM-NSM SM 1 PP ROOM=TEST
56 13	IN	SWD_NUB_BI_PMU_SWDIO	PP0482 P2MM-NSM SM 1 PP ROOM=TEST
56 40	IN	GPIO_AP_TO_CCG2_SWCLK	PP0483 P2MM-NSM SM 1 PP ROOM=TEST
56 40	IN	GPIO_AP_BI_CCG2_SWDIO	PP0484 P2MM-NSM SM 1 PP ROOM=TEST

VALIDATION

32 11	IN	SPI3_AP_FROM_CODEC_MISO	PP0472 P2MM-NSM SM 1 PP ROOM=TEST
32 11	IN	SPI3_AP_TO_CODEC_MOSI	PP0473 P2MM-NSM SM 1 PP ROOM=TEST
22 13	IN	CLK_PMU_TO_AOP_32K	PP0474 P2MM-NSM SM 1 PP ROOM=TEST
28	IN	IO_CAM_PMU1_CRASH	PP0475 P2MM-NSM SM 1 PP ROOM=TEST
42 26 13	IN	SPI0_AOP_FROM_IMU_R1_MISO	PP0479 P2MM-NSM SM 1 PP ROOM=TEST
56 42 26	IN	GPIO_AOP_FROM_IMU_DATARDY	PP0490 P2MM-NSM SM 1 PP ROOM=TEST
56 42	IN	GPIO_AOP_FROM_COMPASS_INT	PP0491 P2MM-NSM SM 1 PP ROOM=TEST
29 28	IN	GPIO_CAM_PMU1_TO_WIDE_LDO_EN	PP0492 P2MM-NSM SM 1 PP ROOM=TEST
29 28	IN	GPIO_CAM_PMU1_TO_SWIDE_LDO_EN	PP0493 P2MM-NSM SM 1 PP ROOM=TEST
41 11	IN	UART0_AP_DEBUG_RXD	PP0494 P2MM-NSM SM 1 PP ROOM=TEST
41 11	IN	UART0_AP_DEBUG_TXD	PP0495 P2MM-NSM SM 1 PP ROOM=TEST
41 11	IN	UART7_AP_FROM_ACCESSORY_RXD	PP0496 P2MM-NSM SM 1 PP ROOM=TEST
41 11	IN	UART7_AP_TO_ACCESSORY_TXD	PP0497 P2MM-NSM SM 1 PP ROOM=TEST
37 10	IN	DWI_PMGR_TO_BACKLIGHT_DATA	PP0498 P2MM-NSM SM 1 PP ROOM=TEST
54 13	IN	I2C0_AOP_SCL	PP0485 P2MM-NSM SM 1 PP ROOM=CODEC
54 13	IN	I2C0_AOP_SDA	PP0486 P2MM-NSM SM 1 PP ROOM=CODEC
38 22 7	IN	IO_AP_FROM_PMU_CPU_TRIGGER0_L	PP0487 P2MM-NSM SM 1 PP ROOM=TEST
35 34 33	IN	IO_SPKAMP_TO_SPKAMP_SYNC	PP0488 P2MM-NSM SM 1 PP ROOM=TEST

RADIOS

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from startup, skipping any layers in between.	EXAMPLE: 1.5/1.5,IN: 3IN. 2
A_DIELECTRIC_(N)XD XV_XVL_X Calculates dielectric distance from Hybrid Table and startup. Inverted distance is used unless 'L' defined	EXAMPLE: 2.2DL,3V,5D,7V,8VL-10DL 2,2D,4D,4V
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from startup, Inverted distance is used unless 'L' is defined	EXAMPLE: 2_4_IN_3L ?

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_WIDE_L1_THIN		ZONE NAME= PRIMARY	
ISL7	ISL5,ISL9	50	0.102
BOTTOM	ISL9	50	0.061

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
ISL7	ISL5,ISL9	50	0.102
BOTTOM	ISL8	50	0.175

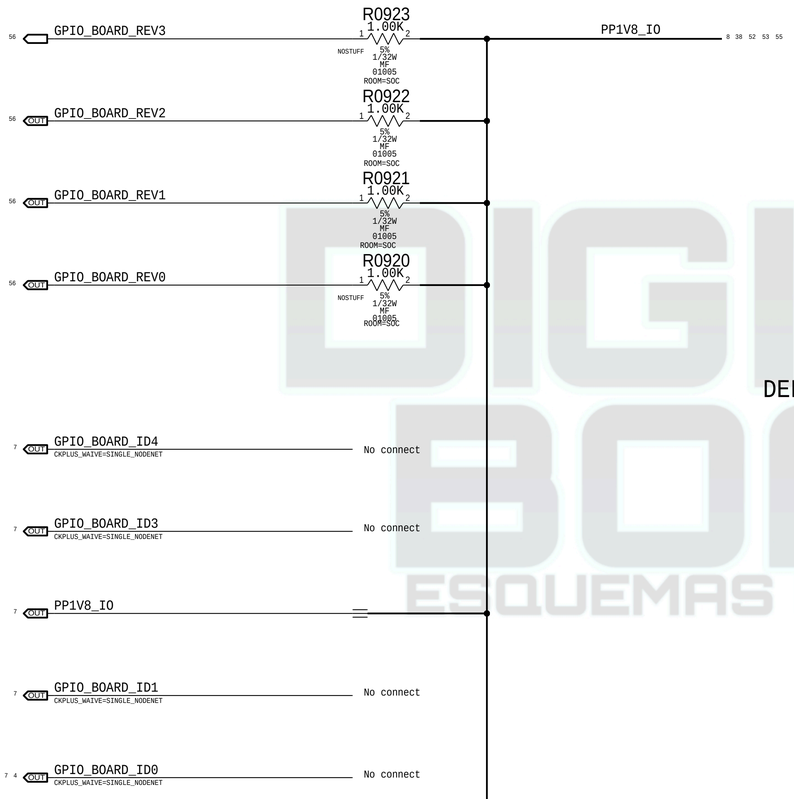
HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
ISL6	ISL7,ISL5	50	0.041
ISL8	ISL9,ISL7	50	0.030
ISL9	BOTTOM,ISL8	50	0.030
BOTTOM	ISL9	50	0.061

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	NET TYPE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND	S	DEFAULT	GND ?	
90_OHM	P	A_90_OHM_DIFF	DP:DP_*90* ?	

CAPPED RULE EXAMPLE:SMD2ALL,SMD_TO_SMD,MVIA2ALL,SHAPE2ALL	LAYER BOTH,TOP,BOT,L1,L2,L3,L4,L5,L6,L7,L8,L9,L10,L11,L12,L13,L14	VALUE (MM)	RULE NAME(S) EXAMPLE: 2D,2V,3DL-5DL,3VL
LINE2SMD	?	0.070	2,2D,4D,4V
MVIA2MVIA	?	=0.065	2,2D,4D,4V
MVIA2SMD	?	=0.070	2,2D,4D,4V
MVIA2SHAPE	?	=0.070	2,2D,4D,4V
SMD2SMD	?	0.070	2,2D,4D,4V
SMD2SHAPE	?	0.070	2,2D,4D,4V
LINE2SHAPE	?	0.165	2
LINE2MVIA	?	0.165	2

BOOTSTRAPPING:

BOARD REV



SELECTED -->

Board Rev[3:0] Float=Low | PU=High	3	2	1	0
PreProto	**1**	**1**	**1**	**1**
Proto 1	**1**	**1**	**1**	0
(Spare)	**1**	**1**	0	**1**
Proto 2	**1**	**1**	0	0
P2+ B0/B0 4G	**1**	0	**1**	**1**
EVT	**1**	0	**1**	0
(Spare)	0	**1**	**1**	**1**
Carrier	0	**1**	**1**	0
(Spare)	0	0	**1**	**1**
DVT	0	0	**1**	0
(Spare)	0	0	0	**1**
PVT	0	0	0	0

BOARD ID

DEFAULT -->

		Board ID[4:0] Float=Low I PU=High				
		4	3	2	1	0
	BoardID[4:0]	**Unused**	**0** = ICE, **1** = MAV	**00** = None **01** = x1367/9 **11** = x1364/8 **10** = x1403		**0** = MLB, **1** = DEV
MLB x1403	**5'b00100**	0	0	**1**	0	0
DEV x1403	**5'b00101**	0	0	**1**	0	**1**
MLB x1364	**5'b01110**	0	**1**	**1**	**1**	0
DEV x1364	**5'b01111**	0	**1**	**1**	**1**	**1**
MLB X1368	**5'b00110**	0	0	**1**	**1**	0
DEV X1368	**5'b00111**	0	0	**1**	**1**	**1**
MLB x1367	**5'b01010**	0	**1**	0	**1**	0
DEV x1367	**5'b01011**	0	**1**	0	**1**	**1**
MLB x1369	**5'b00010**	0	0	0	**1**	0
DEV x1369	**5'b00011**	0	0	0	**1**	**1**

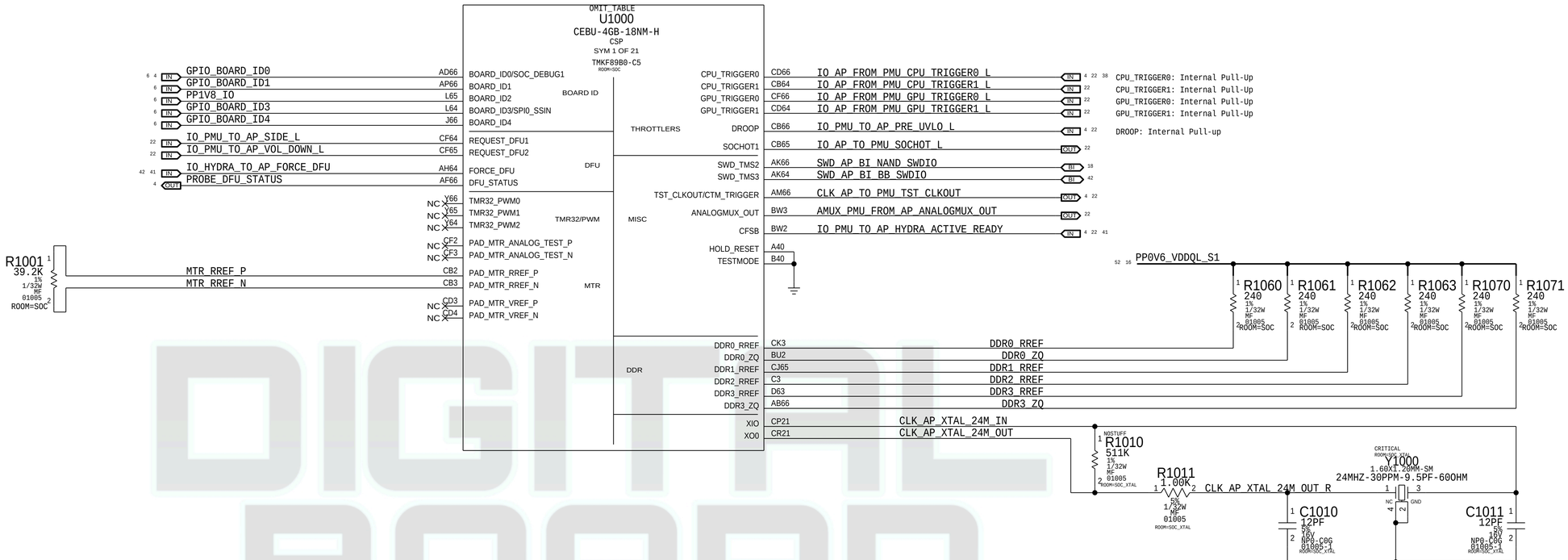
BOOT CONFIG

POR -->

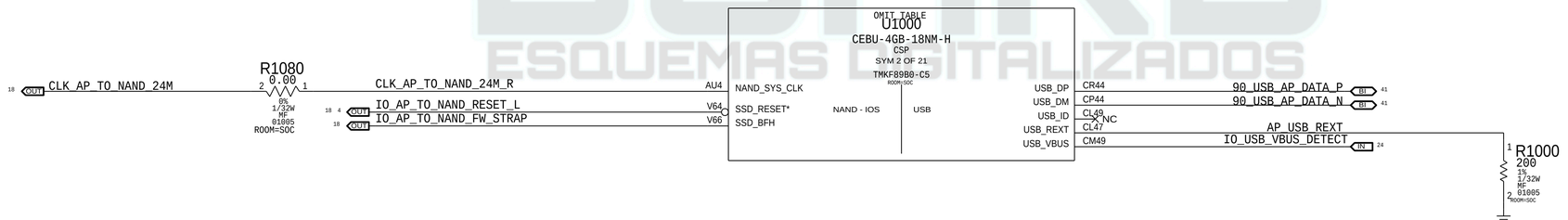
Proto Builds -->

Boot Config [2:0] Float = Low PU = High	2	1	0
SPI NOR on SPI0 12 MHz	0	0	0
SPI NOR on SPI0 12 MHz Test	0	0	**1**
SPI NAND on SPI0 12 MHz	0	**1**	0
SPI NAND on SPI0 12 MHz Test	0	**1**	**1**
SPI NOR on SPI0 40 MHz	**1**	0	0
SPI NOR on SPI0 40 MHz Test	**1**	0	**1**
SPI NOR on SPI0 6 MHz	**1**	**1**	0
SPI NOR on SPI0 6 MHz Test	**1**	**1**	**1**

SOC: Misc



SOC: NAND + USB



SOC: PCIe

OMIT_TABLE

U1000

CEBU-4GB-18NM-H

CSP

SYM 3 OF 21

TMKF89B0-C5

ROOM=SOC

PCIE LINK 0

PCIE LINK 3

PCIE LINK 4

NAND LINK

LINK1 LINK2 LINK3 LINK4

		PCIE0_AP_BI_NAND_CLKREQ_L	BJ65	PCIE_CLKREQ0*		PCIE_CLKREQ3*	E2 PCIE3_AP_BI_WLAN_CLKREQ_1V2_L
		90_PCIE0_AP_TO_NAND_REFCLK_P	CP32	PCIE_REF_CLK0_P		PCIE_REF_CLK3_P	CR26 90_PCIE3_AP_TO_WLAN_REFCLK_P
		90_PCIE0_AP_TO_NAND_REFCLK_N	CR32	PCIE_REF_CLK0_N		PCIE_REF_CLK3_N	CP26 90_PCIE3_AP_TO_WLAN_REFCLK_N
90_PCIE0_AP_FROM_NAND_RX_P	C1100 0.22UF	90_PCIE0_AP_FROM_NAND_C_RX_P	CR17	PCIE_RX0_P		PCIE_RX3_P	CR6 90_PCIE3_AP_FROM_WLAN_C_RX_P
90_PCIE0_AP_FROM_NAND_RX_N	C1101 0.22UF	90_PCIE0_AP_FROM_NAND_C_RX_N	CP17	PCIE_RX0_N		PCIE_RX3_N	CP6 90_PCIE3_AP_FROM_WLAN_C_RX_N
90_PCIE0_AP_TO_NAND_TX_P	C1102 0.22UF	90_PCIE0_AP_TO_NAND_C_TX_P	CM19	PCIE_TX0_P		PCIE_TX3_P	CM7 90_PCIE3_AP_TO_WLAN_C_TX_P
90_PCIE0_AP_TO_NAND_TX_N	C1103 0.22UF	90_PCIE0_AP_TO_NAND_C_TX_N	CN19	PCIE_TX0_N		PCIE_TX3_N	CN7 90_PCIE3_AP_TO_WLAN_C_TX_N
		PCIE0_AP_TO_NAND_PERST_L	BE64	PCIE_PERST0*		PCIE_PERST3*	G4 PCIE3_AP_TO_WLAN_PERST_1V2_L
			BJ66	PCIE_CLKREQ1*		PCIE_CLKREQ2*	BG64
			CP30	PCIE_REF_CLK1_P		PCIE_REF_CLK2_P	CR28
			CR30	PCIE_REF_CLK1_N		PCIE_REF_CLK2_N	CP28
			CR13	PCIE_RX1_P		PCIE_RX2_P	CR9
			CP13	PCIE_RX1_N		PCIE_RX2_N	CP9
			CM15	PCIE_TX1_P		PCIE_TX2_P	CM11
			CN15	PCIE_TX1_N		PCIE_TX2_N	CN11
			BG66	PCIE_PERST1*		PCIE_PERST2*	BE65
		PCIE_RCAL_POS	CK13	PCIE_RCAL_P		PCIE_CLKREQ4*	E3 PCIE4_AP_BI_BB_CLKREQ_1V2_L
	R1140 200 1% 1/32W MF 01005					PCIE_REF_CLK4_P	CR24 90_PCIE4_AP_TO_BB_REFCLK_P
						PCIE_REF_CLK4_N	CP24 90_PCIE4_AP_TO_BB_REFCLK_N
		PCIE_RCAL_NEG	CL13	PCIE_RCAL_N		PCIE_RX4_P	CR4 90_PCIE4_AP_FROM_BB_C_RX_P
	C1140 10PF 5% 16V NP0/C0G 01005					PCIE_RX4_N	CP4 90_PCIE4_AP_FROM_BB_C_RX_N
						PCIE_TX4_P	CM5 90_PCIE4_AP_TO_BB_C_TX_P
						PCIE_TX4_N	CN5 90_PCIE4_AP_TO_BB_C_TX_N
						PCIE_PERST4*	G3 PCIE4_AP_TO_BB_PERST_1V2_L

C1130 0.1UF — 90_PCIE3_AP_FROM_WLAN_RX_P / 90_PCIE3_AP_FROM_WLAN_RX_N

C1131 0.1UF

C1132 0.1UF — 90_PCIE3_AP_TO_WLAN_TX_P / 90_PCIE3_AP_TO_WLAN_TX_N

C1133 0.1UF

C1120 0.1UF — 90_PCIE4_AP_FROM_BB_RX_P / 90_PCIE4_AP_FROM_BB_RX_N

C1121 0.1UF

C1122 0.1UF — 90_PCIE4_AP_TO_BB_TX_P / 90_PCIE4_AP_TO_BB_TX_N

C1123 0.1UF

PCIe BB CLKREQ PU on BB domain

PCIe Clock Request Pull-Ups

PP1V2_SOC

PP1V8_IO

R1100 100K 5% 1/32W MF 01005 ROOM=SOC

R1130 100K 5% 1/32W MF 01005 ROOM=SOC

PCIE0_AP_BI_NAND_CLKREQ_L

PCIE3_AP_BI_WLAN_CLKREQ_1V2_L

PCIe Reset Pull-Downs

PCIE3_AP_TO_WLAN_PERST_1V2_L

PCIE4_AP_TO_BB_PERST_1V2_L

PCIE0_AP_TO_NAND_PERST_L

R1101 100K 5% 1/32W MF 01005 ROOM=SOC

R1121 100K 5% 1/32W MF 01005 ROOM=SOC

R1131 100K 5% 1/32W MF 01005 ROOM=SOC

SOC: ISP

LPDP LANE SWAPPING
OPTIMIZES ROUTING

MIPI LANE SWAPPING
OPTIMIZES ROUTING

OMIT_TABLE
U1000
CEBU-4GB-18NM-H
CSP
SYM 4 OF 21
TMKF89B0-C5
ROOM=SOC

LPDP-RX
MIPI-C
I2C
GPIO
SENSOR CLK

46	90_LPDP_ISP_FROM_FCAM_RX_D1_P	A32	LPDPRX_RX_D0_P
46	90_LPDP_ISP_FROM_FCAM_RX_D1_N	B32	LPDPRX_RX_D0_N
46	90_LPDP_ISP_FROM_FCAM_RX_D0_P	B30	LPDPRX_RX_D1_P
46	90_LPDP_ISP_FROM_FCAM_RX_D0_N	C30	LPDPRX_RX_D1_N
	NC	A28	LPDPRX_RX_D2_P
	NC	B28	LPDPRX_RX_D2_N
45	90_LPDP_ISP_FROM_SWIDE_RX_D0_N	B26	LPDPRX_RX_D3_P
45	90_LPDP_ISP_FROM_SWIDE_RX_D0_P	C26	LPDPRX_RX_D3_N
45	90_LPDP_ISP_FROM_SWIDE_RX_D1_N	B23	LPDPRX_RX_D4_P
45	90_LPDP_ISP_FROM_SWIDE_RX_D1_P	C23	LPDPRX_RX_D4_N
45	90_LPDP_ISP_FROM_SWIDE_RX_D2_N	A21	LPDPRX_RX_D5_P
45	90_LPDP_ISP_FROM_SWIDE_RX_D2_P	B21	LPDPRX_RX_D5_N
	NC	A17	LPDPRX_RX_D6_P
	NC	B17	LPDPRX_RX_D6_N
44	90_LPDP_ISP_FROM_WIDE_RX_D0_N	B15	LPDPRX_RX_D7_P
44	90_LPDP_ISP_FROM_WIDE_RX_D0_P	C15	LPDPRX_RX_D7_N
	NC	A13	LPDPRX_RX_D8_P
	NC	B13	LPDPRX_RX_D8_N
44	90_LPDP_ISP_FROM_WIDE_RX_D2_N	B11	LPDPRX_RX_D9_P
44	90_LPDP_ISP_FROM_WIDE_RX_D2_P	C11	LPDPRX_RX_D9_N
44	90_LPDP_ISP_FROM_WIDE_RX_D1_N	B7	LPDPRX_RX_D10_P
44	90_LPDP_ISP_FROM_WIDE_RX_D1_P	C7	LPDPRX_RX_D10_N
	NC	A6	LPDPRX_RX_D11_P
	NC	B6	LPDPRX_RX_D11_N
	LPDP_ISP_RX0_RCAL_POS	A24	LPDPRX0_RCAL_P
	LPDP_ISP_RX0_RCAL_NEG	B24	LPDPRX0_RCAL_N
	LPDP_ISP_RX1_RCAL_POS	A9	LPDPRX1_RCAL_P
	LPDP_ISP_RX1_RCAL_NEG	B9	LPDPRX1_RCAL_N
46	LPDP_ISP_BI_FCAM_AUX_RX_D0P	D34	LPDPRX_AUX_D0_P
	NC	C34	LPDPRX_AUX_D1_P
45	LPDP_ISP_BI_SWIDE_AUX_RX_D2P	D32	LPDPRX_AUX_D2_P
	NC	D28	LPDPRX_AUX_D3_P
	NC	C24	LPDPRX_AUX_D4_P
	NC	D21	LPDPRX_AUX_D5_P
	NC	D19	LPDPRX_AUX_D6_P
	NC	C19	LPDPRX_AUX_D7_P
	NC	D17	LPDPRX_AUX_D8_P
44	LPDP_ISP_BI_WIDE_AUX_RX_D9P	D13	LPDPRX_AUX_D9_P
	NC	D9	LPDPRX_AUX_D10_P
	NC	D6	LPDPRX_AUX_D11_P

	MIPI0C_DPCLK	A57	90_MIPI_ISP_FROM_IRCAM_CLK_P (IN 46)
	MIPI0C_DNCLK	B57	90_MIPI_ISP_FROM_IRCAM_CLK_N (IN 46)
	MIPI0C_DPDATA0	A55	90_MIPI_ISP_FROM_IRCAM_D0_N (BI 46)
	MIPI0C_DNDATA0	B55	90_MIPI_ISP_FROM_IRCAM_D0_P (BI 46)
	MIPI0C_DPDATA1	B59	90_MIPI_ISP_FROM_IRCAM_D1_N (IN 46)
	MIPI0C_DNDATA1	A59	90_MIPI_ISP_FROM_IRCAM_D1_P (IN 46)
	MIPI0C_REXT	D55	MIPI0C_ISP_REXT
	ISP_I2C0_SCL/ISP_GPIO_15	C40	I2C0_ISP_SCL (OUT 55)
	ISP_I2C0_SDA/ISP_GPIO_14	A44	I2C0_ISP_SDA (BI 55)
	ISP_I2C1_SCL/ISP_GPIO_13	A42	NC
	ISP_I2C1_SDA/ISP_GPIO_12	D40	NC
	ISP_I2C2_SCL/ISP_GPIO_11	B41	NC
	ISP_I2C2_SDA/ISP_GPIO_10	A43	NC
	ISP_I2C3_SCL/ISP_GPIO_9	C42	I2C3_ISP_SCL (OUT 55)
	ISP_I2C3_SDA/ISP_GPIO_8	A49	I2C3_ISP_SDA (BI 55)
	ISP_GPIO0/SIO_LEAP_MADI_IN/AOP_LEAP_MADI_IN	C47	GPIO_ISP_TO_CAM_PMU1_RESET_L (OUT 28 42)
	ISP_GPIO1/ISIO_LEAP_MADI_OUT/AOP_LEAP_MADI_OUT	D47	NC
	ISP_GPIO2/SOC_DEBUG2/MTR_ADC_DOUT	D44	GPIO_ISP_TO_DISPLAY_FLASH_INT (OUT 4 37)
	ISP_GPIO3/SOC_DEBUG3	C45	GPIO_ISP_RCAM_TO_STROBE_TRIGGER (OUT 4 41 42 44 45)
	ISP_GPIO4/ISP_SPMI_SDATA/MTR_ADC_CLKOUT	AB4	SPMI_ISP_BI_CAM_PMU1_DATA (BI 4 28)
	ISP_GPIO5/ISP_SPMI_SCLK	AB2	SPMI_ISP_TO_CAM_PMU1_CLK_R
	ISP_GPIO6/ISP_FCAM_SPMI_SDATA/PLL_DIGOBS_0	AB3	NC
	ISP_GPIO7/ISP_FCAM_SPMI_SCLK/PLL_DIGOBS_1	AC3	NC
	SENSOR0_CLK	T2	CLK_ISP_TO_CAM_PMU1_24M_R
	SENSOR1_CLK	V3	NC
	SENSOR2_CLK	V4	NC
	SENSOR3_CLK	V2	CLK_ISP_TO_RIGEL_12M_R

R1250 200 1% 1/32W MF 01005 ROOM=SOC (1–2)

R1230 33.2 1% 1/32W MF 01005 ROOM=SOC (1–2) SPMI_ISP_TO_CAM_PMU1_CLK (OUT 28)

R1240 33.2 1% 1/32W MF 01005 ROOM=SOC (1–2) CLK_ISP_TO_CAM_PMU1_24M (OUT 28)

R1243 0.00 0% 1/32W MF 01005 ROOM=SOC (1–2) CLK_ISP_TO_RIGEL_12M (OUT 30)

R1200 200 1% 1/32W MF 01005 ROOM=SOC (1–2)

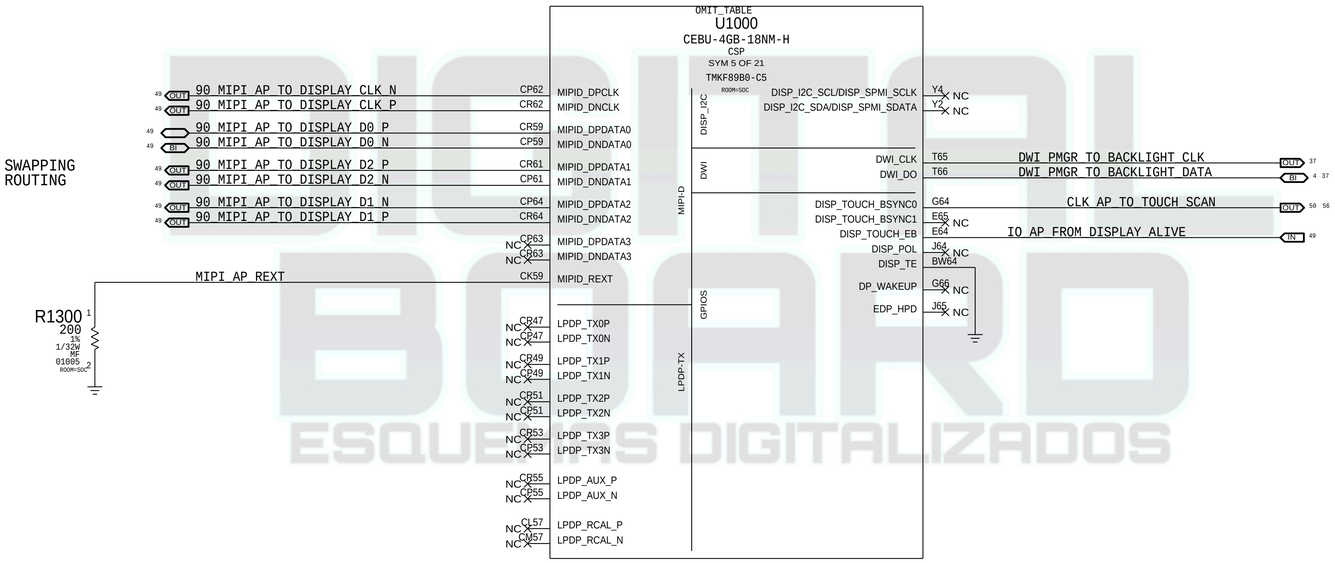
C1200 10PF 5% 16V NP0/C0G 01005 ROOM=SOC (1–2)

R1210 200 1% 1/32W MF 01005 ROOM=SOC (1–2)

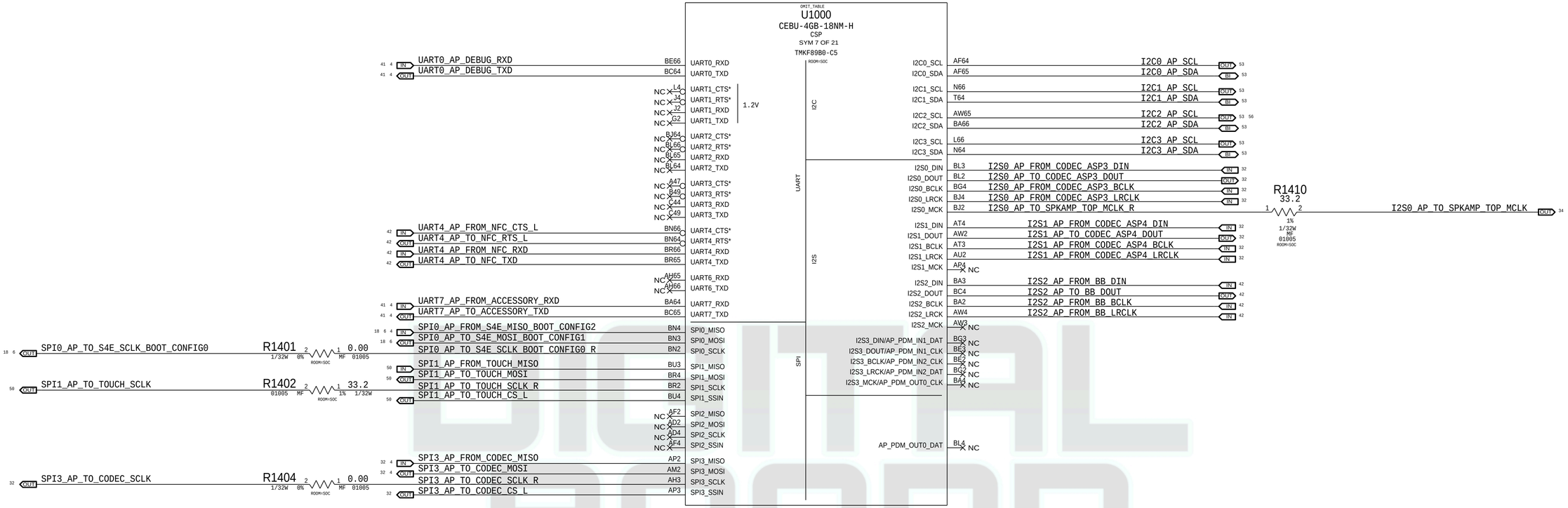
C1210 10PF 5% 16V NP0/C0G 01005 ROOM=SOC (1–2)

SOC: Display

MIPI LANE SWAPPING
OPTIMIZES ROUTING

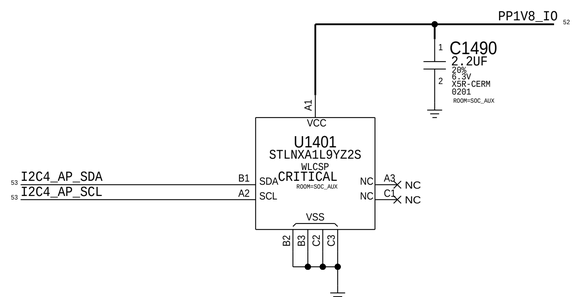


SOC: AP Serial



SPI: Route as Daisy-Chain. No T's Allowed

Place series terminations close to SoC Pins



SOC: AP GPIO

GPIO[0-8]: 1.2V

OMIT_TABLE

U1000
CEBU-4GB-18NM-H
CSP
SYM 6 OF 21
TMKF89B0-C5
GPIO ROOM=SOC

56	GPIO_AP_CANARY2_1V2	L3	GPIO0/I2C5_SCL	GPIO16	AU64	NC_AP_GPIO16	56
56	NC_AP_GPIO1	L2	GPIO1/I2C5_SDA	GPIO17	AU65	NC_AP_GPIO17	56
56	NC_AP_GPIO2	N4	GPIO2	GPIO18	BY66	NC_AP_GPIO18	56
56	GPIO_AP_FROM_WLAN_TIME_SYNC_1V2	N3	GPIO3	GPIO19	AD64	PP1V8_IO	56
56	GPIO_AP_TO_BB_COREDUMP_1V2	N2	GPIO4	GPIO20	AB65	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	56
56	GPIO_AP_FROM_BB_RESET_DETECT_1V2_L	P4	GPIO5	GPIO21	BY64	GPIO_AP_CANARY1	56
56	GPIO_AP_FROM_SPKRAMP_TOP_INT_1V2_L	P2	GPIO6	GPIO22	BY65	GPIO_AP_TO_NFC_DEV_WAKE	56
56	NC_AP_GPIO7	T4	GPIO7	GPIO23	AU66	NC_AP_GPIO23	56
56	NC_AP_GPIO8	T3	GPIO8	GPIO24	AT64	GPIO_AP_FROM_CODEC_INT_L	56
56	GPIO_BOARD_REV3	P64	GPIO9	GPIO25	BW66	GPIO_AP_FROM_BT_AUDIO_SYNC	56
56	GPIO_BOARD_REV2	AP65	GPIO10	GPIO26	BU64	NC_AP_GPIO26	56
56	GPIO_BOARD_REV1	AP64	GPIO11	GPIO27	BU65	NC_AP_GPIO27	56
56	GPIO_BOARD_REV0	B47	GPIO12	GPIO28	BU66	GPIO_AP_TO_AMUX_PMU_SYNC	56
56	NC_AP_GPIO13	AW64	GPIO13	GPIO29	P66	GPIO_AP_TO_TOUCH_RESET_L	56
56	NC_AP_GPIO14	AW66	GPIO14	GPIO30	P65	NC_AP_GPIO30	56
56	GPIO_AP_BI_CCG2_SWDIO	AM65	GPIO15	GPIO31	AM64	GPIO_AP_TO_CCG2_SWCLK	56

SOC: AOP

OMIT_TABLE
U1000
CEBU-4GB-18NM-H
CSP
SYM 9 OF 21
TMKF89B0-C5
ROOM=SOC

I2C0_AOP_SCL — C1600 10PF 5% 16V NP0/C0G 01005 ROOM=SOC
SPI0_AOP_TO_IMU_R1_SCLK — R1601 33.2 1% 1/32W 01005 MF ROOM=SOC → SPI0_AOP_TO_IMU_R1_SCLK_R

I2C0_AOP_SDA	CP36	AOP_I2CM0_SCL
	CJ32	AOP_I2CM0_SDA
I2C1_AOP_SCL	CM34	AOP_I2CM1_SCL
I2C1_AOP_SDA	CM26	AOP_I2CM1_SDA
SPI0_AOP_FROM_IMU_R1_MISO	CJ30	AOP_SPI0_MISO
SPI0_AOP_TO_IMU_R1_MOSI	CK23	AOP_SPI0_MOSI
SPI0_AOP_TO_IMU_R1_SCLK_R	CK30	AOP_SPI0_SCLK
	CJ42	AOP_SPI1_MISO
	CL42	AOP_SPI1_MOSI
	CL55	AOP_SPI1_SCLK
I2S0_AOP_FROM_CODEC_ASP1_DIN	CK53	AOP_I2S0_DIN
I2S0_AOP_TO_CODEC_ASP1_DOUT	CL53	AOP_I2S0_DOUT
I2S0_AOP_FROM_CODEC_ASP1_BCLK	CK40	AOP_I2S0_BCLK
I2S0_AOP_FROM_CODEC_ASP1_LRCLK	CK51	AOP_I2S0_LRCK
I2S0_AOP_TO_CODEC_MCLK1_R	CM42	AOP_I2S0_MCK/AOP_PDM_CLK2
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_SOC_R	CL40	AOP_I2S1_DIN
I2S1_AOP_TO_AMPS_CODEC_ASP2_DOUT	CM61	AOP_I2S1_DOUT/AOP_PDM_IN2_DAT
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK_R	CM40	AOP_I2S1_BCLK/AOP_PDM_IN1_CLK
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK_R	CM62	AOP_I2S1_LRCK/AOP_PDM_IN2_CLK
I2S1_AOP_TO_SPKRAMP_BOT_ARC_MCLK_R	CJ40	AOP_I2S1_MCK
SPMI1_AOP_BI_RF_DATA_R	CM24	AOP_UART0_RXD/NUB_SPMI1_SDATA
SPMI1_AOP_TO_RF_CLK_R	CM32	AOP_UART0_TXD/NUB_SPMI1_SCLK
UART1_AOP_FROM_TOUCH_RXD	CK7	AOP_UART1_RXD/NUB_SPMI2_SDATA
UART1_AOP_TO_TOUCH_TXD	CL32	AOP_UART1_TXD/NUB_SPMI2_SCLK
UART2_AOP_FROM_BB_RXD	CL61	AOP_UART2_RXD
UART2_AOP_TO_BB_TXD	CR36	AOP_UART2_TXD

I2S0_AOP_TO_CODEC_MCLK1 — R1603 33.2 1% 1/32W 01005 MF ROOM=SOC
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN — R1609 300 1% 1/32W 01005-1 MF ROOM=SOC
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK — R1604 49.9 1% 1/32W 01005 MF ROOM=SOC
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK — R1605 49.9 1% 1/32W 01005 MF ROOM=SOC
I2S1_AOP_TO_SPKRAMP_BOT_ARC_MCLK — R1606 0.00 MF 01005 1/32W 0% ROOM=SOC
SPMI1_AOP_BI_RF_DATA — R1607 0.00 MF 01005 1/32W 0% ROOM=SOC
SPMI1_AOP_TO_RF_CLK — R1608 33.2 1% 1/32W 01005 MF ROOM=SOC
C1607 15PF 5% 16V NP0-C0G 01005-1 ROOM=SOC NOSTUFF

AOP_FUNC0	CL62	GPIO_AOP_FROM_IMU_DATARDY
AOP_FUNC1	CL34	GPIO_AOP_TO_R1_COREDUMP_TRIGGER
AOP_FUNC2	CM63	GPIO_AOP_TO_CODEC_CLP_EN
AOP_FUNC3	CJ34	GPIO_AOP_TO_R1_SPI_CS_L
AOP_FUNC4	CK34	GPIO_AOP_FROM_R1_INT
AOP_FUNC5	CM55	GPIO_AOP_TO_CODEC_RESET_L
AOP_FUNC6	CR38	GPIO_AOP_FROM_NFC_HOST_WAKE
AOP_FUNC7	CM53	GPIO_AOP_FROM_SPKAMP_BOT_ARC_INT_L
AOP_FUNC8	CP38	GPIO_AOP_TO_WLAN_CONTEXT_A
AOP_FUNC9/AOP_LPPLL	CM51	GPIO_AOP_TO_IMU_SPI_CS_L
AOP_FUNC10	CM36	GPIO_AOP_TO_R1_TIME_SYNC
AOP_FUNC11	CM47	NC_AOP_GPIO11
AOP_FUNC12	CL36	GPIO_AOP_FROM_ROMEO_B2B_DETECT
AOP_FUNC13	CL64	CLK_AP_TO_TOUCH_SCAN
AOP_FUNC14	CJ36	NC_AOP_GPIO14
AOP_FUNC15/AOP_PDM_CLK4	CK57	GPIO_AOP_BI_PROX_INT_L
AOP_FUNC16/AOP_PDM_CLK3	CK36	GPIO_AOP_FROM_ALS_INT_L
AOP_FUNC17	CM64	GPIO_AOP_FROM_K2_INT_L
AOP_FUNC18	CM38	GPIO_AOP_FROM_COMPASS_INT
AOP_FUNC19	CM59	NC_AOP_GPIO19
AOP_FUNC20	CL38	GPIO_AOP_FROM_TOUCH_CTS
AOP_FUNC21	CJ61	GPIO_AOP_FROM_TOUCH_INT_L
AOP_FUNC22	CJ38	GPIO_AOP_TO_WLAN_CONTEXT_B

SOC: SMC

OMIT_TABLE
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CSP
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ROOM=SOC

I2C0_SMC_SCL	CL23	SMC_I2CM0_SCL
I2C0_SMC_SDA	CM30	SMC_I2CM0_SDA
I2C1_SMC_SCL	CL30	SMC_I2CM1_SCL/SMC_UART1_TXD
I2C1_SMC_SDA	CJ6	SMC_I2CM1_SDA/SMC_UART1_RXD
	CJ28	SMC_UART0_RXD/SMC_I2CM2_SDA
I2C2_SMC_SDA	CL24	SMC_UART0_TXD/SMC_I2CM2_SCL

SOC: NUB

OMIT_TABLE
U1000
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CSP
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ROOM=SOC

SPMI0_NUB_TO_PMU_DOTARA_CLK — R1610 33.2 1% 1/32W 01005 MF ROOM=SOC
SPMI0_NUB_BI_PMU_DOTARA_DATA — R1613 33.2 1% 1/32W 01005 MF ROOM=INT
SWD_NUB_TO_MANY_SWCLK — R1611 0.00 MF 01005 1/32W 0% ROOM=SOC
C1612 15PF 5% 16V NP0-C0G 01005-1 ROOM=SOC NOSTUFF
R1620 200 1% 1/32W MF 01005 ROOM=SOC

SPMI0_NUB_TO_PMU_DOTARA_CLK_R	CJ9	NUB_SPMI0_SCLK
SPMI0_NUB_BI_PMU_DOTARA_DATA_R	CL26	NUB_SPMI0_SDATA
SWD_NUB_TO_MANY_SWCLK_R	CJ21	NUB_SWD_TCK_OUT
SWD_NUB_BI_PMU_SWDIO	CJ24	NUB_SWD_TMS0
SWD_NUB_BI_R1_SWDIO	CJ19	NUB_SWD_TMS1
IO_HYDRA_TO_NUB_PMU_DOCK_CONNECT	CK24	NUB_DOCK_CONNECT
IO_HYDRA_TO_NUB_DOCK_ATTENTION	CJ15	NUB_DOCK_ATTENTION/NUB_PDM_CLK1
GPIO_NUB_FROM_CCG2_INT_L	CJ26	NUB_GPIO_0/AOP_PDM_CLK0
GPIO_NUB_FROM_GECKO_IRQ_L	CK9	NUB_GPIO_1/AOP_PDM_DATA0
GPIO_NUB_TO_GECKO_RESET_L	CM28	NUB_GPIO_2/AOP_FUNC_23
	CJ7	NUB_GPIO_3
	CL28	NUB_GPIO_4/AOP_PDM_DATA1
	CJ11	NUB_GPIO_5/AOP_PDM_DATAOUT
GPIO_NUB_FROM_IRCAM_B2B_DETECT	CK28	NUB_GPIO_6/AOP_PDM_OUT0_CLK
SWD_DOCK_TO_AP_SWCLK	CJ55	JTAG_TCK
SWD_DOCK_BI_AP_SWDIO	CJ44	JTAG_TMS
	CL44	JTAG_SEL
	CJ62	JTAG_TDI
	CK62	JTAG_TDO
	CL51	JTAG_TRST*
90_USB_DBG_DATA_N	CR42	DBG_USB_DM
90_USB_DBG_DATA_P	CP42	DBG_USB_DP
	CK45	DBG_USB_ID
DBG_USB_VBUS_REXT	CM45	DBG_USB_REXT
PP3V3_USB_DEBUG_FILT	CL45	DBG_USB_VBUS
	CJ23	CLK24M_OUT
IO_PMU_TO_SYSTEM_RESET_L	CK42	COLD_RESET*
	CJ57	CFSB_AON
CLK_PMU_TO_AOP_32K	CL63	RT_CLK32768
IO_AP_TO_PMU_RESET	CL59	WDOG
PROBE_AOP_TO_DDR_SLEEP1	CM44	AON_SLEEP1_RESET*
	CJ3	LP4_IN_RESET*

SOC: CPU/GPU

1.029V @ 15.2A MAX
0.909V @ 15.2A MAX
0.540V @ 3.8A MAX
PP_CPU_PCORE

C1702 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1703 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1701 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1704 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1705 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1706 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1707 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

OMIT_TABLE
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ROOM=SOC
CPU/GPU

AN46	VDD_PCPU	VDD_GPU	AA29
AN50	VDD_PCPU	VDD_GPU	AA37
AN54	VDD_PCPU	VDD_GPU	AA46
AN58	VDD_PCPU	VDD_GPU	AA54
AR43	VDD_PCPU	VDD_GPU	AC27
AR48	VDD_PCPU	VDD_GPU	AC31
AR56	VDD_PCPU	VDD_GPU	AC35
AV41	VDD_PCPU	VDD_GPU	W56
AV58	VDD_PCPU	VDD_GPU	AC39
BB58	VDD_PCPU	VDD_GPU	F27
BF41	VDD_PCPU	VDD_GPU	F31
BK41	VDD_PCPU	VDD_GPU	F35
BK54	VDD_PCPU	VDD_GPU	F48
BK58	VDD_PCPU	VDD_GPU	F52
BM43	VDD_PCPU	VDD_GPU	H33
BM48	VDD_PCPU	VDD_GPU	H41
BM52	VDD_PCPU	VDD_GPU	H50
BM56	VDD_PCPU	VDD_GPU	K27
BP46	VDD_PCPU	VDD_GPU	K31
BP50	VDD_PCPU	VDD_GPU	K35
BT56	VDD_PCPU	VDD_GPU	K39
CC46	VDD_PCPU	VDD_GPU	K43
CC50	VDD_PCPU	VDD_GPU	K48
CC56	VDD_PCPU	VDD_GPU	K52
BM39	VDD_PCPU_SENSE	VDD_GPU	K56
AN29	VDD_ECPU	VDD_GPU	M29
AN33	VDD_ECPU	VDD_GPU	M46
AN37	VDD_ECPU	VDD_GPU	M54
AR27	VDD_ECPU	VDD_GPU	R27
AR31	VDD_ECPU	VDD_GPU	R31
AR35	VDD_ECPU	VDD_GPU	R35
AR39	VDD_ECPU	VDD_GPU	R48
AV33	VDD_ECPU	VDD_GPU	R52
AV37	VDD_ECPU	VDD_GPU	R56
AY27	VDD_ECPU	VDD_GPU	U33
AY39	VDD_ECPU	VDD_GPU	U50
BB29	VDD_ECPU	VDD_GPU	W27
BD27	VDD_ECPU	VDD_GPU	W31
BF29	VDD_ECPU	VDD_GPU	W35
BF37	VDD_ECPU	VDD_GPU	W39
BH27	VDD_ECPU	VDD_GPU	W43
BH35	VDD_ECPU	VDD_GPU	W48
BK29	VDD_ECPU	VDD_GPU	W52
BK33	VDD_ECPU	VDD_GPU_SENSE	AE27
BK37	VDD_ECPU		

0.985V @ 12.6A MAX
0.686V @ 5.80A MAX
0.562V @ 3.20A MAX
PP_GPU

C1730 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1731 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1733 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
C1734 20UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT
C1735 20UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT
C1736 20UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT

0.970V @ 3.6A MAX
0.650V @ 2.1A MAX
0.530V @ 1.2A MAX
PP_CPU_ECORE

C1791 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1792 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1790 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1794 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

ANALOG_CPU_PCORE_SENSESP

ANALOG_GPU_SENSESP

SOC: SRAM

OMIT_TABLE
U1000
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ROOM=SOC
SRAM

AR52	VDD_SRAM_PCPU	VDD_SRAM_SOC	AA18
BB41	VDD_SRAM_PCPU	VDD_SRAM_SOC	AA58
BF58	VDD_SRAM_PCPU	VDD_SRAM_SOC	AC12
BK46	VDD_SRAM_PCPU	VDD_SRAM_SOC	AC48
		VDD_SRAM_SOC	AE18
AV29	VDD_SRAM_ECPU	VDD_SRAM_SOC	AE41
BB37	VDD_SRAM_ECPU	VDD_SRAM_SOC	AE54
BH31	VDD_SRAM_ECPU	VDD_SRAM_SOC	AG12
		VDD_SRAM_SOC	AG25
		VDD_SRAM_SOC	AG35
AA33	VDD_SRAM_GPU	VDD_SRAM_SOC	AG48
AA50	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ18
H29	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ29
H37	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ41
H46	VDD_SRAM_GPU	VDD_SRAM_SOC	AJ54
H54	VDD_SRAM_GPU	VDD_SRAM_SOC	AL12
M33	VDD_SRAM_GPU	VDD_SRAM_SOC	AL25
M50	VDD_SRAM_GPU	VDD_SRAM_SOC	AL35
U29	VDD_SRAM_GPU	VDD_SRAM_SOC	AN18
U46	VDD_SRAM_GPU	VDD_SRAM_SOC	AR12
U54	VDD_SRAM_GPU	VDD_SRAM_SOC	AR25
		VDD_SRAM_SOC	AV18
		VDD_SRAM_SOC	AY12
		VDD_SRAM_SOC	AY25
		VDD_SRAM_SOC	BB18
BP54	VDD_SRAM_ANE	VDD_SRAM_SOC	BD25
BV46	VDD_SRAM_ANE	VDD_SRAM_SOC	BF18
CC54	VDD_SRAM_ANE	VDD_SRAM_SOC	BK18
		VDD_SRAM_SOC	BM12
		VDD_SRAM_SOC	BM25
		VDD_SRAM_SOC	BM35
		VDD_SRAM_SOC	BP18
		VDD_SRAM_SOC	BP29
		VDD_SRAM_SOC	BP41
		VDD_SRAM_SOC	BT12
		VDD_SRAM_SOC	BT25
		VDD_SRAM_SOC	BT35
		VDD_SRAM_SOC	BV18
		VDD_SRAM_SOC	BV29
		VDD_SRAM_SOC	BV41
		VDD_SRAM_SOC	CA35
		VDD_SRAM_SOC	CE25
		VDD_SRAM_SOC	CE56
		VDD_SRAM_SOC	K20
		VDD_SRAM_SOC	R12
		VDD_SRAM_SOC	W20

0.752V @ 2.7A MAX
PP_SRAM_S1

C1772 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1773 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT
C1774 14UF 20% 4V X5R 0402-D2X-1 ROOM=SOC_FILT

SOC: SOC

0.770V @ 4.9A MAX
0.651V @ 3.4A MAX
0.590V @ 2.7A MAX
PP_SOC_S1

C1760 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1761 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1765 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1762 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
C1763 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
C1764 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT

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ROOM=SOC
SOC

AA41	VDD_SOC	VDD_SOC	H25
AC43	VDD_SOC	VDD_SOC	BH25
AC52	VDD_SOC	VDD_SOC	BH39
AC56	VDD_SOC	VDD_SOC	BK10
AE8	VDD_SOC	VDD_SOC	BK14
AE22	VDD_SOC	VDD_SOC	BK22
AE33	VDD_SOC	VDD_SOC	BM16
AE37	VDD_SOC	VDD_SOC	BM20
AE46	VDD_SOC	VDD_SOC	BM27
AE50	VDD_SOC	VDD_SOC	BM31
AE58	VDD_SOC	VDD_SOC	BP14
AG20	VDD_SOC	VDD_SOC	BP22
AG27	VDD_SOC	VDD_SOC	BP33
AG31	VDD_SOC	VDD_SOC	BP37
AG39	VDD_SOC	VDD_SOC	BT16
AG43	VDD_SOC	VDD_SOC	BT20
AG52	VDD_SOC	VDD_SOC	BT27
AG56	VDD_SOC	VDD_SOC	BT31
AJ22	VDD_SOC	VDD_SOC	BT39
AJ33	VDD_SOC	VDD_SOC	BT43
AJ37	VDD_SOC	VDD_SOC	M56
AJ50	VDD_SOC	VDD_SOC	BV14
AJ58	VDD_SOC	VDD_SOC	BV22
AL20	VDD_SOC	VDD_SOC	BV33
AL27	VDD_SOC	VDD_SOC	BV37
AL31	VDD_SOC	VDD_SOC	BV56
AL39	VDD_SOC	VDD_SOC	CA16
AC20	VDD_SOC	VDD_SOC	CA20
AL43	VDD_SOC	VDD_SOC	CA27
AL52	VDD_SOC	VDD_SOC	CA31
AL56	VDD_SOC	VDD_SOC	CA39
AN10	VDD_SOC	VDD_SOC	CA43
AN14	VDD_SOC	VDD_SOC	CC14
AN22	VDD_SOC	VDD_SOC	CC22
AR16	VDD_SOC	VDD_SOC	CE20
AR20	VDD_SOC	VDD_SOC	CE27
AV10	VDD_SOC	VDD_SOC	AY16
AV14	VDD_SOC	VDD_SOC	CE52
AV22	VDD_SOC	VDD_SOC	CG22
BB10	VDD_SOC	VDD_SOC	F41
BB14	VDD_SOC	VDD_SOC	U12
BB22	VDD_SOC		
BB60	VDD_SOC		
BD16	VDD_SOC		
BD20	VDD_SOC		
BD39	VDD_SOC		
BF22	VDD_SOC		
BF8	VDD_SOC		
BF14	VDD_SOC		
BH16	VDD_SOC		
BH20	VDD_SOC		
		VDD_SOC_SENSE	AY20

ANALOG_SOC_SENSESP

SOC: FIXED

OMIT_TABLE
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ROOM=SOC

VDD_FIXED: 0.8V @ 15mA MAX
PP0V8_SOC_FIXED_S1

C1801 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

(Analog)
VDD_FIXED_MIPID: 0.8V @ 40mA MAX
VDD_FIXED_MIPIC: 0.8V @ 15mA MAX
VDD_FIXED_MIPID_PLL: 0.8V @ 10mA MAX
PP0V8_SOC_FIXED_S1

C1806 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1805 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

(Analog)
VDD_FIXED_USB: 0.8V @ 5mA MAX
PP0V8_SOC_FIXED_S1

R1810 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT
PP0V8_USB_DEBUG
C1810 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT NOSTUFF

(Analog)
VDD_FIXED_LPDP_RX: 0.8V @ 80mA MAX
PP0V8_SOC_FIXED_S1

C1817 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1816 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1815 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT

VDD_FIXED_PCIE:0.8V @ 105mA MAX
PP0V8_SOC_FIXED_S1

C1821 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1820 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

CC16	VDD_FIXED	CG16	VDD_FIXED_PCIE_REFBUF
AC10	VDD_FIXED		
AC58	VDD_FIXED		FIXED
BD8	VDD_FIXED		
AR60	VDD_FIXED		
M12	VDD_FIXED		
BD60	VDD_FIXED	CA12	VDD_FIXED_PLL_DDR0
CG56	VDD_FIXED	BM60	VDD_FIXED_PLL_DDR1
F37	VDD_FIXED	W12	VDD_FIXED_PLL_DDR2
F56	VDD_FIXED	D59	VDD_FIXED_PLL_DDR3
CG60	VDD_FIXED_MIPID		
F60	VDD_FIXED_MIPIC	CG50	VDD_FIXED_PLL_LPDP
CJ59	VDD_FIXED_MIPID_PLL	BH12	VDD_FIXED_PLL_SOC
CG48	VDD_FIXED_USB	BD10	VDD_FIXED_PLL_ANE
		BF12	VDD_FIXED_PLL_GPU
CG54	VDD_FIXED_LPDP_TX	AL48	VDD_FIXED_PCPU
H10	VDD_FIXED_LPDP_RX	AN41	VDD_FIXED_ECPU
H14	VDD_FIXED_LPDP_RX		
H18	VDD_FIXED_LPDP_RX		
H22	VDD_FIXED_LPDP_RX	BH8	VDD_FIXED_MTR
CE12	VDD_FIXED_PCIE0		
CE8	VDD_FIXED_PCIE1		

PP0V8_SOC_FIXED_PCIE_REFBUF

R1840 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT
C1840 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

VDD_FIXED_PCIE_REFBUF:0.8V @ 50mA MAX
PP0V8_SOC_FIXED_S1

PP0V8_SOC_FIXED_S1

C1841 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1842 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

VDD_FIXED_PLL_DDR0: 0.8V @ 8mA
VDD_FIXED_PLL_DDR1: 0.8V @ 8mA
VDD_FIXED_PLL_DDR2: 0.8V @ 8mA
VDD_FIXED_PLL_DDR3: 0.8V @ 8mA
VDD_FIXED_PLL_LPDP: 0.8V @ 3mA
VDD_FIXED_PLL_SOC: 0.8V @ 9mA
VDD_FIXED_PLL_ANE: 0.8V @ 5mA
VDD_FIXED_PLL_GPU: 0.8V @ 5mA
VDD_FIXED_PCPU: 0.8V @ 5mA
VDD_FIXED_ECPU: 0.8V @ 5mA

VDD_FIXED_MTR 0.8V @ 5mA
PP0V8_SOC_FIXED_S1

SOC: VDD12

OMIT_TABLE
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ROOM=SOC

VDD12_PLL_SOC: 1.2V @ 8mA MAX
VDD12_PLL_PCPU: 1.2V @ 7mA MAX
VDD12_PLL_ECPU: 1.2V @ 7mA MAX
VDD12_PLL_GPU: 1.2V @ 7mA MAX
VDD12_PLL_ANE: 1.2V @ 7mA MAX
PP1V2_SOC

C1828 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1827 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1826 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1825 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDDIO12_PLL_DDRx: 1.2V @ 8mA MAX
PP1V2_SOC

BF10	VDD12_PLL_SOC	AC8	VDDIO12_GRP5
	VDD12	AG8	VDDIO12_GRP5
AJ46	VDD12_PLL_PCPU		
AN39	VDD12_PLL_ECPU		
BD12	VDD12_PLL_GPU		
BD14	VDD12_PLL_ANE		
CC12	VDDIO12_PLL_DDR0	CG14	VDD12_PCIE0
BK60	VDDIO12_PLL_DDR1	CG8	VDD12_PCIE1
AA12	VDDIO12_PLL_DDR2	CC18	VDD12_PCIE_REFBUF
D61	VDDIO12_PLL_DDR3	CE18	VDD12_PCIE_REFBUF
		CG52	VDD12_LPDP_TX
		CE48	VDD12_PLL_LPDP
		F25	VDD12_LPDP_RX
		F8	VDD12_LPDP_RX
		F12	VDD12_LPDP_RX
		F16	VDD12_LPDP_RX
		F20	VDD12_LPDP_RX

PP_VDDIO12_GRP5

XW1801 OMIT SHORT-20L-0.05MM-SM ROOM=SOC_FILT CONTROL_INDUCTANCE

VDDIO12_GRP5:1.2V @ 15mA MAX
PP1V2_SOC

C1845 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

VDD12_PCIE:1.2V @ 95mA MAX
VDD12_PCIE_REFBUF:1.2V @ 20mA MAX
PP1V2_SOC

C1850 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

PP1V2_SOC_PCIE_REFBUF

R1855 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT

C1855 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT

VDD12_LPDP_RX: 1.2V @ 9mA MAX
VDD12_LPDP_RX: 1.2V @ 200mA MAX
PP1V2_SOC

C1830 15PF 5% 16V NP0-C0G 01005-1 ROOM=SOC_FILT
C1831 0.01UF 10% 6.3V X5R 01005 ROOM=SOC_FILT
C1832 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1833 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1834 4UF 20% 4V X5R 0201 ROOM=SOC_FILT

SOC: DDR

SOC: AOP/AVE/ISP/USB

OMIT_TABLE

U1000
CEBU-4GB-18NM-H
CSP
SYM 15 OF 21
TMKF89B0-C5
ROOM=SOC

U1000
CEBU-4GB-18NM-H
CSP
SYM 16 OF 21
TMKF89B0-C5
ROOM=SOC
DDR

AOP/AVE/DISP/USB

PP_DCS_S1
0.895V @ 910mA MAX
0.735V @ 550mA MAX
0.614V @ 300mA MAX
Place caps on SoC Corners
C1989 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT
C1988 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1987 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1986 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1985 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
BP10 VDD_DCS_DDR0
CC10 VDD_DCS_DDR0
BP58 VDD_DCS_DDR1
CC58 VDD_DCS_DDR1
AA10 VDD_DCS_DDR2
K10 VDD_DCS_DDR2
H58 VDD_DCS_DDR3
W58 VDD_DCS_DDR3
ANALOG_DCS_SENSEP (OUT)
A62 VDD_DCS_SENSE

VDDQL* TOTAL: 0.573V - 0.63V @ 620mA MAX
Place caps on SoC Corners
PP0V6_VDDQL_S1
C1994 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1993 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1992 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1991 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1990 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
BG1 VDDQL_DDR0
BL1 VDDQL_DDR0
BM8 VDDQL_DDR0
BR1 VDDQL_DDR0
CC8 VDDQL_DDR0
CH1 VDDQL_DDR0
CK1 VDDQL_DDR0
CM1 VDDQL_DDR0
BE67 VDDQL_DDR1
BJ67 VDDQL_DDR1
BN67 VDDQL_DDR1
BP60 VDDQL_DDR1
CE60 VDDQL_DDR1
CF67 VDDQL_DDR1
CJ67 VDDQL_DDR1
CL67 VDDQL_DDR1
AF1 VDDQL_DDR2
AK1 VDDQL_DDR2
AP1 VDDQL_DDR2
E1 VDDQL_DDR2
J1 VDDQL_DDR2
K8 VDDQL_DDR2
N1 VDDQL_DDR2
W8 VDDQL_DDR2
AD67 VDDQL_DDR3
AH67 VDDQL_DDR3
AM67 VDDQL_DDR3
D67 VDDQL_DDR3
G67 VDDQL_DDR3
K60 VDDQL_DDR3
L67 VDDQL_DDR3
W60 VDDQL_DDR3
A64 VDDQL_SENSE
ANALOG_VDDQL_SENSEP (OUT)

VDD2_DDR*: 1.06V - 1.17V @ 2.2A MAX
PP1V1_S2
C1980 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1981 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1982 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
C1983 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
Added C1982, C1983 (2.2uF for each VDD2_DDRx Channel)
BC2 VDD2_DDR0
BU1 VDD2_DDR0
BY1 VDD2_DDR0
CD1 VDD2_DDR0
CM3 VDD2_DDR0
BC66 VDD2_DDR1
BU67 VDD2_DDR1
BY67 VDD2_DDR1
CD67 VDD2_DDR1
CM65 VDD2_DDR1
AB1 VDD2_DDR2
AT2 VDD2_DDR2
D3 VDD2_DDR2
P1 VDD2_DDR2
V1 VDD2_DDR2
AB67 VDD2_DDR3
AT66 VDD2_DDR3
D65 VDD2_DDR3
P67 VDD2_DDR3
V67 VDD2_DDR3

PP1V1_S2
Current included in VDD2
CJ4 VDDIO11_RET_DDR0
CJ64 VDDIO11_RET_DDR1
D4 VDDIO11_RET_DDR2
D62 VDDIO11_RET_DDR3

VDD1_DDR*: 1.70V - 1.95V @ 220mA MAX
PP1V8_S2
C1996 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1997 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1998 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
C1999 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
BC1 VDD1_DDR0
CN2 VDD1_DDR0
BC67 VDD1_DDR1
CN66 VDD1_DDR1
AT1 VDD1_DDR2
C2 VDD1_DDR2
AT67 VDD1_DDR3
C66 VDD1_DDR3

VDD_LOW: 0.71V @ 220mA MAX
VDD_LOW_FLPPLL: 0.71V @ 0.3mA MAX
VDD_LOW_ULPPLL: 0.71V @ 0.03mA MAX
VDD_LOW_USB_DEBUGL: 0.71V @ 5mA MAX
PP0V7_VDD_LOW_S2
C1900 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
CC29 VDD_LOW
CC33 VDD_LOW
CC37 VDD_LOW
CC41 VDD_LOW
CE35 VDD_LOW
CE39 VDD_LOW
CE43 VDD_LOW
CG25 VDD_LOW

R1905 10 5% 1/32W MF 01005 ROOM=SOC_FILT
PP0V7_VDD_LOW_FLPPLL_R
C1905 0.47UF 20% 6.3V X5R 01005-1 ROOM=SOC_FILT
CE33 VDD_LOW_FLPPLL

R1910 100 5% 1/32W MF 01005 ROOM=SOC_FILT
PP0V7_VDD_LOW_ULPPLL_R
C1910 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
CE31 VDD_LOW_ULPPLL

R1920 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT
PP_VDD_LOW_USB_DEBUG
C1920 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
CG46 VDD_LOW_USB_DEBUG

PP_AVE_S1
C1927 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
C1926 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
C1925 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=SOC_FILT
AA22 VDD_AVE
AC25 VDD_AVE
K12 VDD_AVE
K16 VDD_AVE
K25 VDD_AVE
M14 VDD_AVE
R25 VDD_AVE
U14 VDD_AVE
W16 VDD_AVE
W25 VDD_AVE
VDD_AVE: 0.59V - 0.801V @ 3.2A MAX

VDD_DISP: 0.56V - 0.718V @ 1.5A MAX
PP_DISP_S1
C1931 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
C1930 15UF 20% 6.3V X5R-CERM 0402-0.1MM ROOM=SOC_FILT
AA14 VDD_DISP
AC16 VDD_DISP
AE10 VDD_DISP
AE14 VDD_DISP
AG16 VDD_DISP
AJ10 VDD_DISP
AJ14 VDD_DISP
AL16 VDD_DISP

VDD33_USB*: 3.3V @ 15mA MAX
PP3V3_USB
CK47 VDD33_USB

R1940 0.00 0% 1/32W MF 01005 ROOM=SOC_FILT
PP3V3_USB_DEBUG
PP3V3_USB_DEBUG_FILT
C1935 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1940 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
CJ47 VDD33_USB_DEBUG

VDD18_TSADC_SOC: 1.8V @ 3mA MAX
VDD18_TSADC_CPU: 1.8V @ 5mA MAX
VDD18_TSADC_CPU: 1.8V @ 3mA MAX
VDD18_AMUX: 1.8V @ 0.3mA MAX
PP1V8_IO
VDD18_TSADC_SOC0 BP25
VDD18_TSADC_SOC1 CJ51
VDD18_TSADC_SOC2 C4
VDD18_TSADC_CPU0 AV39
VDD18_TSADC_CPU1 AR41
VDD18_TSADC_CPU2 BK50
VDD18_TSADC_CPU3 BK52
VDD18_TSADC_CPU4 AL46
VDD18_TSADC_GPU0 F46
VDD18_AMUX BW4

VDD18_USB: 1.8V @ 20mA MAX
VDD18_XTAL: 1.8V @ 1mA MAX
PP1V8_IO
FL1950 240OHM-25%-0.2A-0.9OHM 01005 ROOM=SOC_FILT
PP1V8_XTAL
C1945 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1950 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1946 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
VDD18_USB CJ49
VDD18_XTAL CJ17

VDDIO18_AOP: 1.8 @ 20mA MAX
PP1V8_S2
C1960 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1961 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
VDDIO18_AOP CG29
VDDIO18_AOP CG33
VDDIO18_AOP CG37
VDDIO18_AOP CG39
VDDIO18_AOP CG41

VDD18_MIPIC:1.8 @ 2mA MAX
VDD18_MIPID:1.8 @ 20mA MAX
PP1V8_IO
C1965 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=SOC_FILT
C1966 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
VDD18_MIPIC F58
VDD18_MIPID CG58

VDD18_EFUSE1 AC60
VDD18_EFUSE2 CA25

VDDIO18_GPR*: 1.8V @ 75mA MAX
VDDIO18_MTR: 1.8V @ 28mA MAX
PP1V8_IO
C1970 26UF 20% 4V X5R 0402-0.1MM ROOM=SOC_FILT
C1971 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1972 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
C1973 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
VDDIO18_GRP1 AL8
VDDIO18_GRP1 AR8
VDDIO18_GRP1 AY8
VDDIO18_GRP3 AG60
VDDIO18_GRP3 AL60
VDDIO18_GRP3 AN60
VDDIO18_GRP3 AY60
VDDIO18_GRP3 BH60
VDDIO18_GRP4 F39
VDDIO18_GRP4 F43
VDDIO18_MTR BK8

VDDIO18_ULPLL: 1.8V @ 0.03mA MAX
PP1V8_S2
R1975 100 5% 1/32W MF 01005 ROOM=SOC_FILT
PP1V8_ULPPLL_R
C1975 4UF 20% 4V X5R 0201 ROOM=SOC_FILT
VDD18_ULPPLL CE29

VDDIO18_FMON: 1.8V @ 0.1mA MAX
PP1V8_IO
R1976 49.9 1% 1/32W MF 01005
PP1V8_FMON_R
C1976 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=SOC_FILT
VDD18_FMON BV25

SOC: GND

OMIT_TABLE
U1000
CEBU-4GB-18NM-H
CSP
SYM 19 OF 21
TMKF89B0-C5
ROOM=SOC

A11	VSS	VSS	AL54
A15	VSS	VSS	AL58
A19	VSS	VSS	AM1
A2	VSS	VSS	AM3
A23	VSS	VSS	AN12
A26	VSS	VSS	AN16
A3	VSS	VSS	AN20
A30	VSS	VSS	AN25
A34	VSS	VSS	AN27
A36	VSS	VSS	AN31
A38	VSS	VSS	AN35
A4	VSS	VSS	AN43
A5	VSS	VSS	AN48
A51	VSS	VSS	AN52
A53	VSS	VSS	AN56
A61	VSS	VSS	AN8
A65	VSS	VSS	AP67
A66	VSS	VSS	AR10
A7	VSS	VSS	AR14
AA16	VSS	VSS	AR18
AA20	VSS	VSS	AR22
AA25	VSS	VSS	AR29
AA27	VSS	VSS	AR33
AA31	VSS	VSS	AR37
AA35	VSS	VSS	AR46
AA39	VSS	VSS	AR50
AA43	VSS	VSS	AR54
AA48	VSS	VSS	AR58
AA52	VSS	VSS	AT65
AA56	VSS	VSS	AU1
AA60	VSS	VSS	AU3
AA8	VSS	VSS	AU67
AB64	VSS	VSS	AV12
AC14	VSS	VSS	AV16
AC18	VSS	VSS	AV20
AC22	VSS	VSS	AV25
AC29	VSS	VSS	AV27
AC33	VSS	VSS	AV31
AC37	VSS	VSS	AV35
AC41	VSS	VSS	AV60
AC46	VSS	VSS	AV8
AC50	VSS	VSS	AW1
AC54	VSS	VSS	AW67
AD1	VSS	VSS	AY10
AD65	VSS	VSS	AY14
AE12	VSS	VSS	AY22
AE16	VSS	VSS	AY29
AE20	VSS	VSS	AY37
AE25	VSS	VSS	AY41
AE31	VSS	VSS	AY58
AE35	VSS	VSS	B1
AE39	VSS	VSS	B19
AE43	VSS	VSS	B2
AE48	VSS	VSS	B3
AE52	VSS	VSS	B34
AE56	VSS	VSS	B36
AE60	VSS	VSS	B38
AF3	VSS	VSS	B4
AF67	VSS	VSS	B42
AG10	VSS	VSS	B45
AG14	VSS	VSS	B5
AG18	VSS	VSS	B51
AG22	VSS	VSS	B53
AG29	VSS	VSS	B61
AG33	VSS	VSS	B62
AG37	VSS	VSS	B63
AG41	VSS	VSS	B64
AG46	VSS	VSS	B65
AG50	VSS	VSS	B66
AG54	VSS	VSS	B67
AG58	VSS	VSS	BA1
AH1	VSS	VSS	BA65
AH4	VSS	VSS	BA67
AJ12	VSS	VSS	BB12
AJ16	VSS	VSS	BB16
AJ20	VSS	VSS	BB20
AJ25	VSS	VSS	BB25
AJ27	VSS	VSS	BB27
AJ31	VSS	VSS	BB39
AJ35	VSS	VSS	BB8
AJ39	VSS	VSS	BC3
AJ43	VSS	VSS	BD18
AJ48	VSS	VSS	BD22
AJ52	VSS	VSS	BD29
AJ56	VSS	VSS	BD37
AJ60	VSS	VSS	BD41
AJ8	VSS	VSS	BD58
AK65	VSS	VSS	BE1
AK67	VSS	VSS	BE4
AL10	VSS	VSS	BF16
AL14	VSS	VSS	BF20
AL18	VSS	VSS	BF25
AL22	VSS	VSS	BF27
AL29	VSS	VSS	BF39
AL33	VSS	VSS	BF60
AL37	VSS	VSS	BG65
AL41	VSS	VSS	BG67
AL50	VSS	VSS	BH10

OMIT_TABLE
U1000
CEBU-4GB-18NM-H
CSP
SYM 20 OF 21
TMKF89B0-C5
ROOM=SOC

BH14	VSS	VSS	CA29
BH18	VSS	VSS	CA33
BH22	VSS	VSS	CA37
BH29	VSS	VSS	CA41
BH33	VSS	VSS	CA46
BH37	VSS	VSS	CA56
BH41	VSS	VSS	CB1
BH58	VSS	VSS	CB4
BJ1	VSS	VSS	CB67
BJ3	VSS	VSS	CC20
BK12	VSS	VSS	CC25
BK16	VSS	VSS	CC27
BK20	VSS	VSS	CC31
BK25	VSS	VSS	CC35
BK27	VSS	VSS	CC39
BK31	VSS	VSS	CC43
BK35	VSS	VSS	CC48
BK39	VSS	VSS	CC52
BK43	VSS	VSS	CC60
BK48	VSS	VSS	CD2
BK56	VSS	VSS	CD65
BL67	VSS	VSS	CE10
BM10	VSS	VSS	CE14
BM14	VSS	VSS	CE22
BM18	VSS	VSS	CE37
BM22	VSS	VSS	CE41
BM29	VSS	VSS	CE46
BM33	VSS	VSS	CE50
BM37	VSS	VSS	CE54
BM41	VSS	VSS	CE58
BM46	VSS	VSS	CF1
BM50	VSS	VSS	CF4
BM54	VSS	VSS	CG12
BM58	VSS	VSS	CG16
BN1	VSS	VSS	CG20
BN65	VSS	VSS	CG27
BP12	VSS	VSS	CG31
BP16	VSS	VSS	CG35
BP20	VSS	VSS	CG43
BP27	VSS	VSS	CH2
BP31	VSS	VSS	CH3
BP35	VSS	VSS	CH4
BP43	VSS	VSS	CH64
BP48	VSS	VSS	CH65
BP52	VSS	VSS	CH66
BP56	VSS	VSS	CH67
BP8	VSS	VSS	CJ1
BR3	VSS	VSS	CJ13
BR64	VSS	VSS	CJ2
BR67	VSS	VSS	CJ45
BT14	VSS	VSS	CJ5
BT18	VSS	VSS	CJ53
BT22	VSS	VSS	CJ63
BT29	VSS	VSS	CJ66
BT33	VSS	VSS	CK11
BT37	VSS	VSS	CK15
BT41	VSS	VSS	CK17
BT46	VSS	VSS	CK19
BV12	VSS	VSS	CK2
BV16	VSS	VSS	CK21
BV20	VSS	VSS	CK26
BV27	VSS	VSS	CK32
BV31	VSS	VSS	CK38
BV35	VSS	VSS	CK4
BV39	VSS	VSS	CK44
BV43	VSS	VSS	CK49
BW1	VSS	VSS	CK5
BW65	VSS	VSS	CK55
BW67	VSS	VSS	CK6
BY2	VSS	VSS	CK61
BY3	VSS	VSS	CK63
BY4	VSS	VSS	CK64
C1	VSS	VSS	CK65
C13	VSS	VSS	CK66
C17	VSS	VSS	CK67
C21	VSS	VSS	CL1
C24	VSS	VSS	CL11
C28	VSS	VSS	CL15
C32	VSS	VSS	CL17
C36	VSS	VSS	CL19
C38	VSS	VSS	CL2
C5	VSS	VSS	CL21
C51	VSS	VSS	CL3
C53	VSS	VSS	CL4
C55	VSS	VSS	CL5
C57	VSS	VSS	CL6
C59	VSS	VSS	CL65
C6	VSS	VSS	CL66
C61	VSS	VSS	CL7
C62	VSS	VSS	CL9
C63	VSS	VSS	CM13
C64	VSS	VSS	CM17
C65	VSS	VSS	CM2
C67	VSS	VSS	CM21
C9	VSS	VSS	CM23
CA14	VSS	VSS	CM4
CA18	VSS	VSS	CM6
CA22	VSS	VSS	CM66

OMIT_TABLE
U1000
CEBU-4GB-18NM-H
CSP
SYM 21 OF 21
TMKF89B0-C5
ROOM=SOC

CM67	VSS	VSS	F10
CM9	VSS	VSS	F14
CN1	VSS	VSS	F18
CN13	VSS	VSS	F22
CN17	VSS	VSS	F29
CN21	VSS	VSS	F33
CN23	VSS	VSS	F50
CN24	VSS	VSS	F54
CN26	VSS	VSS	G1
CN28	VSS	VSS	G65
CN3	VSS	VSS	H12
CN30	VSS	VSS	H16
CN32	VSS	VSS	H20
CN34	VSS	VSS	H27
CN36	VSS	VSS	H31
CN38	VSS	VSS	H35
CN4	VSS	VSS	H39
CN40	VSS	VSS	H43
CN42	VSS	VSS	H48
CN44	VSS	VSS	H52
CN45	VSS	VSS	H56
CN47	VSS	VSS	H60
CN49	VSS	VSS	H8
CN51	VSS	VSS	J3
CN53	VSS	VSS	J67
CN55	VSS	VSS	K14
CN57	VSS	VSS	K18
CN59	VSS	VSS	K22
CN6	VSS	VSS	K29
CN61	VSS	VSS	K33
CN62	VSS	VSS	K37
CN63	VSS	VSS	K41
CN64	VSS	VSS	K46
CN65	VSS	VSS	K50
CN67	VSS	VSS	K54
CN9	VSS	VSS	K58
CP1	VSS	VSS	L1
CP11	VSS	VSS	M25
CP15	VSS	VSS	M27
CP19	VSS	VSS	M31
CP2	VSS	VSS	M35
CP23	VSS	VSS	M48
CP3	VSS	VSS	M52
CP34	VSS	VSS	N65
CP40	VSS	VSS	N67
CP45	VSS	VSS	P3
CP5	VSS	VSS	R14
CP57	VSS	VSS	R29
CP65	VSS	VSS	R33
CP66	VSS	VSS	R46
CP67	VSS	VSS	R50
CP7	VSS	VSS	R54
CR11	VSS	VSS	T1
CR15	VSS	VSS	T67
CR19	VSS	VSS	U25
CR2	VSS	VSS	U27
CR23	VSS	VSS	U31
CR3	VSS	VSS	U35
CR34	VSS	VSS	U48
CR40	VSS	VSS	U52
CR45	VSS	VSS	U56
CR5	VSS	VSS	V65
CR57	VSS	VSS	W10
CR65	VSS	VSS	W14
CR66	VSS	VSS	W18
CR7	VSS	VSS	W22
D1	VSS	VSS	W29
D11	VSS	VSS	W33
D15	VSS	VSS	W37
D2	VSS	VSS	W41
D23	VSS	VSS	W46
D26	VSS	VSS	W50
D30	VSS	VSS	W54
D36	VSS	VSS	Y1
D38	VSS	VSS	Y3
D42	VSS	VSS	Y67
D45	VSS		
D49	VSS		
D5	VSS	VSS_1	CR1
D51	VSS	VSS_2	CR67
D53	VSS	VSS_3	A1
D57	VSS	VSS_4	A67
D64	VSS	VSS_DDR_SENSE	A63
D66	VSS	VSS_GPU_SENSE	AE29
D7	VSS	VSS_PCPU_SENSE	BP39
E4	VSS	VSS_SENSE	AY18
E66	VSS		
E67	VSS		

<-- Corner Ball Test Pins. System connects to GND.

ANALOG_VDDQL_DCS_SENSEN OUT 4
ANALOG_GPU_SENSEN OUT 4
ANALOG_CPU_PCORE_SENSEN OUT 4
ANALOG_SOC_SENSEN OUT 4

S4E NAND

FUTURE COMPATABILITY: R2602 50mohm Max
Default R2602: NO STUFF

196mA MAX
PP1V2_IO_NAND

R2602 0 5% 1/20W MF 0201 ROOM=NAND NOSTUFF

C2630 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2629 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2643 4UF 20% 6.3V X5R 0201 ROOM=NAND
C2645 4UF 20% 6.3V X5R 0201 ROOM=NAND
C2647 4UF 20% 6.3V X5R 0201 ROOM=NAND
C2612 220PF 5% 25V C0G 01005 ROOM=NAND
C2618 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2614 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2615 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2617 22PF 5% 16V C0G 01005 ROOM=NAND

PP_VDDIO_2_NAND_R

R2603 0 5% 1/20W MF 0201 ROOM=NAND

267mA MAX S4E (8 dies)
50mA MAX S4E COMPATABILITY MODE
PP1V8_IO

C2641 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2624 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2626 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2610 0.1UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2611 220PF 5% 25V C0G 01005 ROOM=NAND

700mA MAX S4E
578mA MAX S4E COMPATABILITY MODE
PP0V9_NAND

C2602 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=NAND
C2605 15UF 20% 6.3V X6R 0402-0.1MM-1 ROOM=NAND
C2600 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2601 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2622 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2627 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2640 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2642 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2644 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2646 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2603 220PF 5% 25V C0G 01005 ROOM=NAND
C2606 220PF 5% 25V C0G 01005 ROOM=NAND
C2609 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2607 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2608 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2604 22PF 5% 16V C0G 01005 ROOM=NAND

FUTURE COMPATABILITY
R2625 -> Ferrite Bead (APN: 155S00340)

C2625 4UF 20% 4V X5R 0201 ROOM=NAND
PP1V8_IO_NAND_F
R2625 0.00 0% 1/32W MF 01005 ROOM=NAND

FUTURE COMPATABILITY:
R2663 -> 2 Ohm

PP1V8_IO_NAND_R
R2663 0.00 0% 1/32W MF 01005 ROOM=NAND
C2663 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

1150mA MAX (1us peak power)
PP2V63_NAND

C2613 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2616 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2619 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND
C2621 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=NAND

C2649 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2650 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2651 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND
C2652 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

C2638 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND
C2639 68PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2634 47PF 5% 16V NP0-C0G 01005 ROOM=NAND
C2635 22PF 5% 16V C0G 01005 ROOM=NAND
C2636 220PF 5% 25V C0G 01005 ROOM=NAND
C2637 100PF 5% 16V NP0-C0G 01005-1 ROOM=NAND

FUTURE COMPATABILITY
R2623 -> Ferrite Bead (APN: 155S00161)

PP0V9_NAND_F
R2623 0 5% 1/20W MF 0201 ROOM=NAND
PP0V9_NAND
C2623 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=NAND

ANALOG_NAND_ANI1_VREF
ANALOG_NAND_ANI0_VREF

U2600
NAND-S4E-S5E-MCP-STUDY
LGA
ROOM=NAND
OMIT_TABLE

N6	PCI_AVDD_CLK_1	
M9	PCI_AVDD_CLK_2	
J6	PCI_AVDD_H	
N8	PCI_VDD_1	
J8	PCI_VDD_2	
L2	AVDD18_PLL	
G12	ANIO_VREF	
J4	ANI1_VREF	
G6	VDD	
G8	VDD	
L6	VDD	
L8	VDD	
R6	VDD	
R8	VDD	
J2	VDDIO_1(GPIO)	
K9	VDDIO_1(GPIO)	
T5	VDDIO_1(GPIO)	
E2	VDDIO_2(NAND)	
E10	VDDIO_2(NAND)	
N2	VDDIO_2(NAND)	
P9	VDDIO_2(NAND)	
D3	VCC	
E12	VCC	
G4	VCC	
L12	VCC	
P2	VCC	
R4	VDD_PLL	
F3	VPP	NC
A2, A4, A6, A8, A10, A12, B1, B13, C2, C12, D1, D11, D13, F1, F5, F7, F9, F11, F13, H1, H3, H5, H9, H11, H13, J10, K1, K5, K7, K13, L10, M1, M5, M7, M13, N4, N10, P1, P3, P7, P11, P13, R10, T1, T7, T9, T13, U2, U4, U6, U8, U10, U12	VSS	

CLK_AP_TO_NAND_24M	M3	CLK_IN
90_PCIE0_AP_TO_NAND_REFCLK_P	K11	PCIE_REFCLK_P
90_PCIE0_AP_TO_NAND_REFCLK_N	J12	PCIE_REFCLK_M
PCIE0_AP_BI_NAND_CLKREQ_L	P5	PCIE_CLKREQ_N
ANALOG_PCIE_NAND_RESREF	H7	PCI_RESREF
90_PCIE0_AP_TO_NAND_TX_P	M11	PCIE_RX0_P
90_PCIE0_AP_TO_NAND_TX_N	N12	PCIE_RX0_M
90_PCIE0_AP_FROM_NAND_RX_P	R12	PCIE_TX0_P
90_PCIE0_AP_FROM_NAND_RX_N	T11	PCIE_TX0_M
IO_AP_TO_NAND_RESET_L	L4	RESET*
	G10	TRST*
ANALOG_NAND_ZQ_C	K3	ZQ_C
ANALOG_NAND_ZQ_NEG	C10	ZQ_N

EXT_D0/BOOT0	B3	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
EXT_D1/BOOT1	C4	IO_AP_TO_NAND_FW_STRAP
EXT_D2/BOOT2/SPINAND_SCLK	B5	SPIO_AP_TO_S4E_SCLK_BOOT_CONFIG0
EXT_D3/SWD_UID0/SPINAND_MISO	C6	SPIO_AP_FROM_S4E_MISO_BOOT_CONFIG2
EXT_D4/UART_RX	B7	NC
EXT_D5/SWD_UID1/SPINAND_MOSI	C8	SPIO_AP_TO_S4E_MOSI_BOOT_CONFIG1
EXT_D6/UART_TX	B9	NC
EXT_D7/SPF	B11	IO_PMU_TO_MANY_SYSTEM_ALIVE
EXT_NCE/PERST*	E8	PCIE0_AP_TO_NAND_PERST_L
EXT_NRE/JTAG_TMS	D7	SWD_AP_BI_NAND_SWDIO
EXT_NWE/JTAG_TCK	E6	SWD_NUB_TO_MANY_SWCLK
EXT_RNB/JTAG_TDO	E4	
EXT_CLE/JTAG_TDI	D5	NC
EXT_ALE/JTAG_SEL	D9	
DROOP_N	T3	
WP_N	G2	PP_VDDIO_2_NAND_R

Default C2620: No Stuff

FUTURE COMPATABILITY:
R2604 -> 200 Ohm
C2620 -> 10pF

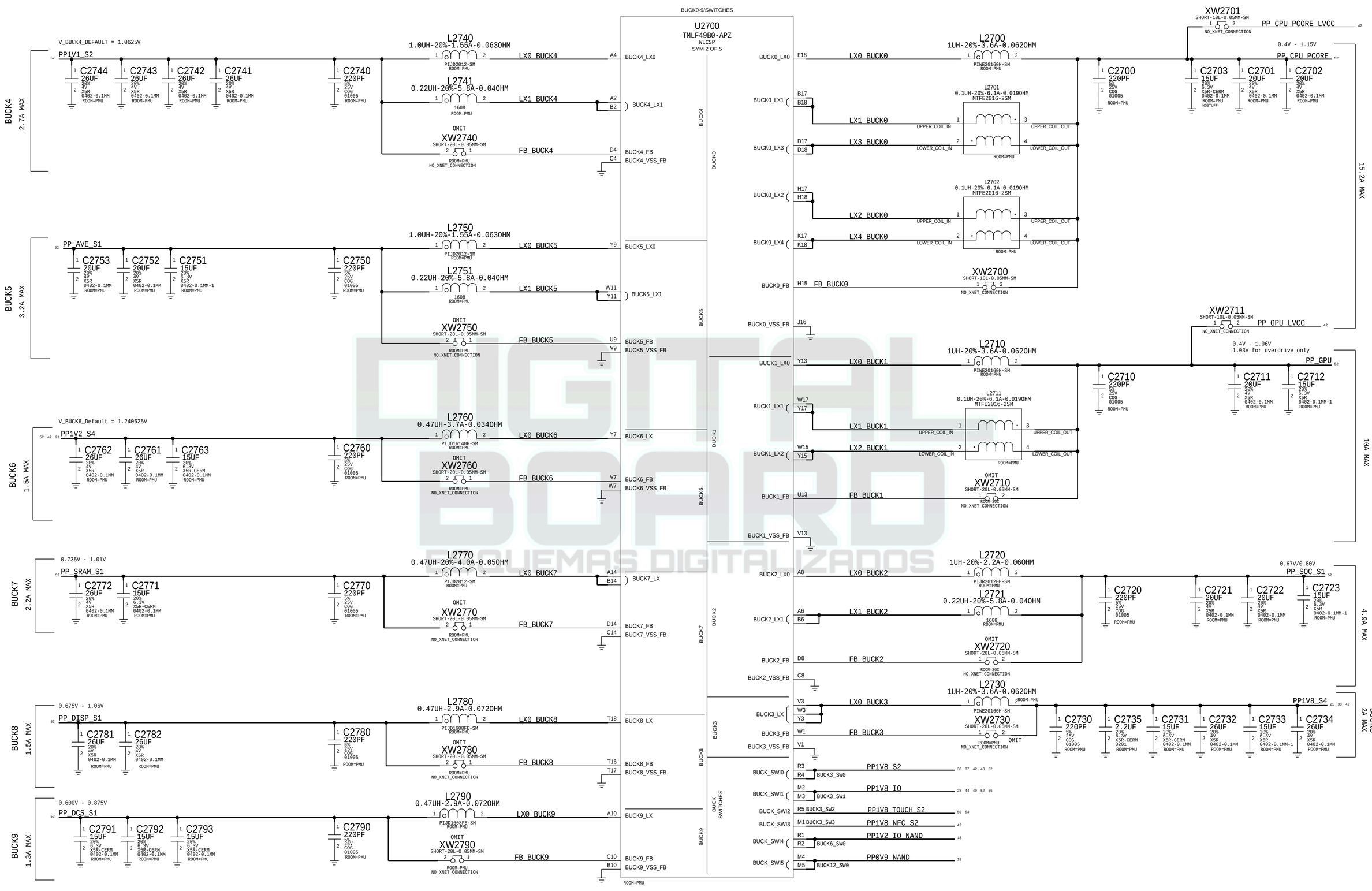
C2620 10PF 5% 16V NP0/C0G 01005 ROOM=NAND NOSTUFF
R2604 3.01K 1% 1/32W MF 01005 ROOM=NAND

Board trace <= 0.2Ohm

R2600 100 0.1% 1/32W MF 01005 ROOM=NAND
R2601 300 0.1% 1/32 MF 01005 ROOM=NAND

FUTURE COMPATABILITY: R2600 -> 300 Ohm

FUTURE COMPATABILITY
PP_VDDIO_2_NAND_R


BUCK0-9/SWITCHES
U2700
TMLF49B0-APZ
WLCSP
SYM 2 OF 5
BUCK4
2.7A MAX
V_BUCK4_DEFAULT = 1.0625V
PP1V1_S2
L2740
1.0UH-20%-1.55A-0.063OHM
PIJD2012-SM
LX0_BUCK4
BUCK4_LX0
L2741
0.22UH-20%-5.8A-0.04OHM
1608
LX1_BUCK4
BUCK4_LX1
OMIT
XW2740
SHORT-20L-0.05MM-SM
FB_BUCK4
BUCK4_FB
BUCK4_VSS_FB
C2744 26UF 20% 4V X5R 0402-0.1MM
C2743 26UF 20% 4V X5R 0402-0.1MM
C2742 26UF 20% 4V X5R 0402-0.1MM
C2741 26UF 20% 4V X5R 0402-0.1MM
C2740 220PF 5% 25V C0G 01005
BUCK5
3.2A MAX
PP_AVE_S1
L2750
1.0UH-20%-1.55A-0.063OHM
LX0_BUCK5
BUCK5_LX0
L2751
0.22UH-20%-5.8A-0.04OHM
LX1_BUCK5
BUCK5_LX1
XW2750
FB_BUCK5
BUCK5_FB
BUCK5_VSS_FB
C2753 20UF 20% 4V X5R 0402-0.1MM
C2752 20UF 20% 4V X5R 0402-0.1MM
C2751 15UF 20% 6.3V X5R 0402-0.1MM-1
C2750 220PF 5% 25V C0G 01005
BUCK6
1.5A MAX
V_BUCK6_Default = 1.240625V
PP1V2_S4
L2760
0.47UH-3.7A-0.034OHM
PIJD16140H-SM
LX0_BUCK6
BUCK6_LX
XW2760
FB_BUCK6
BUCK6_FB
BUCK6_VSS_FB
C2762 26UF 20% 4V X5R 0402-0.1MM
C2761 26UF 20% 4V X5R 0402-0.1MM
C2763 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2760 220PF 5% 25V C0G 01005
BUCK7
2.2A MAX
0.735V - 1.01V
PP_SRAM_S1
L2770
0.47UH-20%-4.0A-0.05OHM
PIJD2012-SM
LX0_BUCK7
BUCK7_LX
XW2770
FB_BUCK7
BUCK7_FB
BUCK7_VSS_FB
C2772 26UF 20% 4V X5R 0402-0.1MM
C2771 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2770 220PF 5% 25V C0G 01005
BUCK8
1.5A MAX
0.675V - 1.06V
PP_DISP_S1
L2780
0.47UH-2.9A-0.072OHM
PIJD1608FE-SM
LX0_BUCK8
BUCK8_LX
XW2780
FB_BUCK8
BUCK8_FB
BUCK8_VSS_FB
C2781 26UF 20% 4V X5R 0402-0.1MM
C2782 26UF 20% 4V X5R 0402-0.1MM
C2780 220PF 5% 25V C0G 01005
BUCK9
1.3A MAX
0.600V - 0.875V
PP_DCS_S1
L2790
0.47UH-2.9A-0.072OHM
PIJD1608FE-SM
LX0_BUCK9
BUCK9_LX
XW2790
FB_BUCK9
BUCK9_FB
BUCK9_VSS_FB
C2791 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2792 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2793 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2790 220PF 5% 25V C0G 01005
BUCK0
15.2A MAX
L2700
1UH-20%-3.6A-0.062OHM
PIWE20160H-SM
BUCK0_LX0
LX0_BUCK0
L2701
0.1UH-20%-6.1A-0.019OHM
MTFE2016-2SM
BUCK0_LX1
LX1_BUCK0
BUCK0_LX3
LX3_BUCK0
L2702
BUCK0_LX2
LX2_BUCK0
BUCK0_LX4
LX4_BUCK0
XW2700
SHORT-10L-0.05MM-SM
BUCK0_FB
FB_BUCK0
BUCK0_VSS_FB
XW2701
PP_CPU_PCORE_LVCC
0.4V - 1.15V
PP_CPU_PCORE
C2700 220PF 5% 25V C0G 01005
C2703 15UF 20% 6.3V X5R-CERM 0402-0.1MM NOSTUFF
C2701 20UF 20% 4V X5R 0402-0.1MM
C2702 20UF 20% 4V X5R 0402-0.1MM
BUCK1
10A MAX
L2710
1UH-20%-3.6A-0.062OHM
BUCK1_LX0
LX0_BUCK1
L2711
0.1UH-20%-6.1A-0.019OHM
MTFE2016-2SM
BUCK1_LX1
LX1_BUCK1
BUCK1_LX2
LX2_BUCK1
XW2710
BUCK1_FB
FB_BUCK1
BUCK1_VSS_FB
XW2711
PP_GPU_LVCC
0.4V - 1.06V
1.03V for overdrive only
PP_GPU
C2710 220PF 5% 25V C0G 01005
C2711 20UF 20% 4V X5R 0402-0.1MM
C2712 15UF 20% 6.3V X5R 0402-0.1MM-1
BUCK2
4.9A MAX
L2720
1UH-20%-2.2A-0.060HM
BUCK2_LX0
LX0_BUCK2
L2721
0.22UH-20%-5.8A-0.04OHM
BUCK2_LX1
LX1_BUCK2
XW2720
BUCK2_FB
FB_BUCK2
BUCK2_VSS_FB
0.67V/0.80V
PP_SOC_S1
C2720 220PF 5% 25V C0G 01005
C2721 20UF 20% 4V X5R 0402-0.1MM
C2722 20UF 20% 4V X5R 0402-0.1MM
C2723 15UF 20% 6.3V X5R 0402-0.1MM-1
BUCK3
2A MAX
L2730
1UH-20%-3.6A-0.062OHM
BUCK3_LX
LX0_BUCK3
XW2730
BUCK3_FB
FB_BUCK3
BUCK3_VSS_FB
PP1V8_S4
C2730 220PF 5% 25V C0G 01005
C2735 2.2UF 20% 6.3V X5R-CERM 0201
C2731 15UF 20% 6.3V X5R-CERM 0402-0.1MM
C2732 26UF 20% 4V X5R 0402-0.1MM
C2733 15UF 20% 6.3V X5R 0402-0.1MM-1
C2734 26UF 20% 4V X5R 0402-0.1MM
BUCK SWITCHES
BUCK_SWI0
BUCK3_SW0
PP1V8_S2
BUCK_SWI1
BUCK3_SW1
PP1V8_IO
BUCK_SWI2
BUCK3_SW2
PP1V8_TOUCH_S2
BUCK_SWI3
BUCK3_SW3
PP1V8_NFC_S2
BUCK_SWI4
BUCK6_SW0
PP1V2_IO_NAND
BUCK_SWI5
BUCK12_SW0
PP0V9_NAND
UPPER_COIL_IN
UPPER_COIL_OUT
LOWER_COIL_IN
LOWER_COIL_OUT
NO_XNET_CONNECTION
ROOM=PMU

BUCK10-12/BUCK-ANALOG-DIGITAL VDD

U2700
TMLF49B0-APZ
WLCSP
SYM 3 OF 5

52 42 37 37 24 21 20 3 PP_VDD_MAIN

C2852 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2851 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2850 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2855 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2854 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2853 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2863 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU
C2858 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2857 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2856 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2862 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2861 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2860 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU

C17 C18 G17 G18 L17 L18 R17 R18 — VDD_BUCK0_8_11
W8 W12 W16 Y8 Y12 Y16 — VDD_BUCK1_5_6
A1 A5 A9 B1 B5 B9 — VDD_BUCK2_4_9
V4 W4 Y4 — VDD_BUCK3_10
A13 B13 — VDD_BUCK12_7

BUCK VDD

BUCK10_LX Y5 LX0 BUCK10
L2800 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU
PP0V6_VDDQL_S1 52
C2800 220PF 5% 25V C0G 01005 ROOM=PMU
C2802 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C2801 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU

BUCK10_FB V5 FB_BUCK10
OMIT XW2800 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

BUCK10_VSS_FB W5

BUCK10
1.3A MAX

BUCK11_LX0 M18 LX0 BUCK11
L2810 1UH-20%-2.2A-0.06OHM PIJR20120H-SM ROOM=PMU
0.415V - 1.06V
PP_CPU_ECORE 52
C2810 220PF 5% 25V C0G 01005 ROOM=PMU
C2811 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C2812 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C2813 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU

BUCK11_LX1 P17 P18 LX1 BUCK11
L2811 0.22UH-20%-5.8A-0.04OHM 1608 ROOM=PMU

BUCK11_FB M15 FB_BUCK11
OMIT XW2810 SHORT-20L-0.05MM-SM ROOM=SOC NO_XNET_CONNECTION

BUCK11_VSS_FB M16

BUCK11
3.6A MAX

21 PP1V5_VLDOINT
C2872 220PF 5% 25V C0G 01005 ROOM=PMU

C1 C5 C9 C13 C16 E6 F6 F7 F17 G16 K6 L16 R16 U2 U4 V8 V12 V16 W13 K11 — VDD_ANA

ANALOG VDD

52 42 37 37 24 21 20 3 PP_VDD_MAIN
C2830 0.1UF 20% 6.3V X5R-CERM 01005 ROOM=PMU

F9 — VDD_MAIN

BUCK12_LX A12 LX0 BUCK12
L2820 0.47UH-2.9A-0.072OHM PIJD1608FE-SM ROOM=PMU
PP0V9_S1 21
C2820 220PF 5% 25V C0G 01005 ROOM=PMU
C2822 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=PMU
C2823 15UF 20% 6.3V X5R 0402-0.1MM-1 ROOM=PMU
C2821 26UF 20% 4V X5R 0402-0.1MM ROOM=PMU

BUCK12_FB C12 FB_BUCK12
OMIT XW2820 SHORT-20L-0.05MM-SM ROOM=PMU NO_XNET_CONNECTION

BUCK12_VSS_FB B12

BUCK12
1.5A MAX

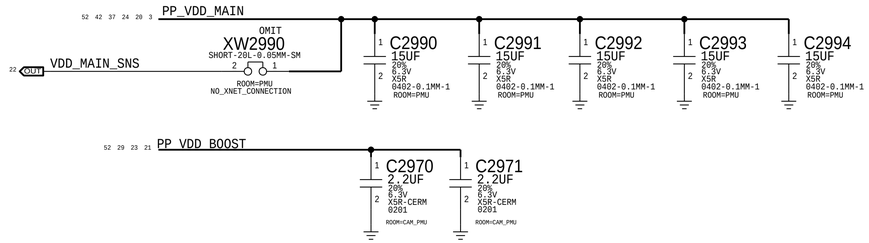
D6 E15 T6 T11 — VDD_DIG

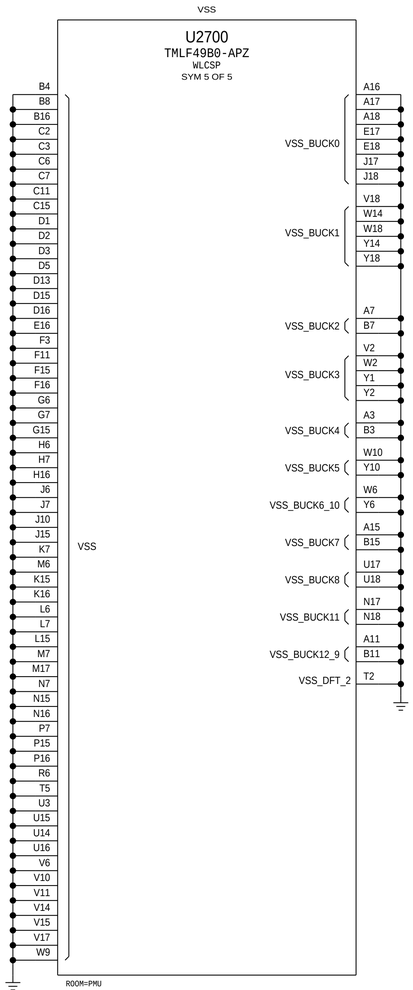
DIGITAL VDD

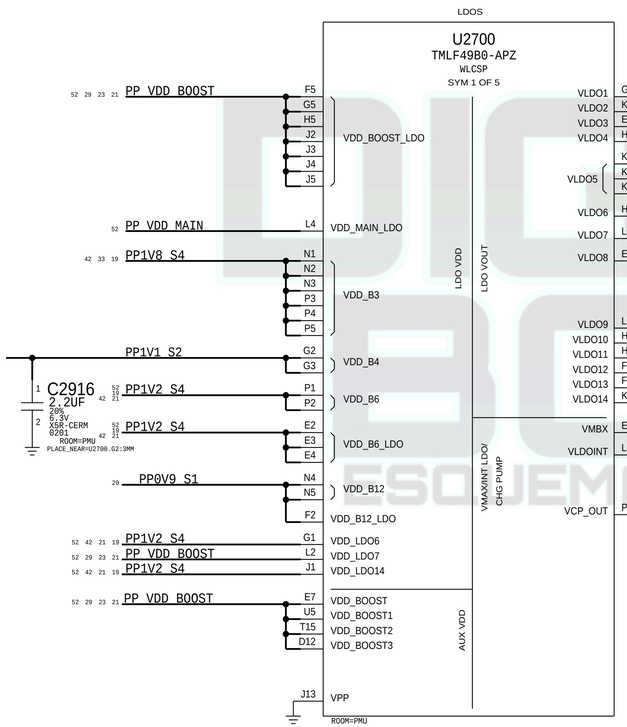
52 PP1V2_S2 N6 VDDIO1V2

ROOM=PMU

PMU - LDOs



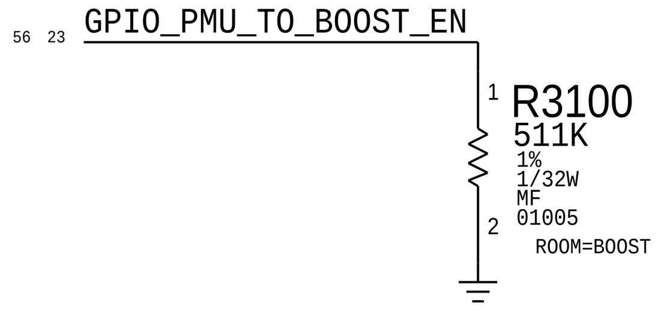




PMU - GPIOs

TODO: Update
CONTROL PIN NOTES:
NOTE (1):INPUT PULL-DOWN 100-300k
NOTE (2):INPUT PULL-DOWN 1M
NOTE (3):INPUT PULL-UP OR DOWN 100k-300k
NOTE (4):OUTPUT OPEN-DRAIN, REQUIRES PULL-UP
AMUX CAPS
AMUX_PMU_FROM_CAM_PMU1
AMUX_PMU_FROM_GECKO
AMUX_WIDE_PVDD
CHESTNUT_TO_PMU_AMUX
C3071
C3072
C3073
C3074
1000PF
ROOM=PMU
COLD_RESET & SYSTEM_ALIVE
PP1V8_S2
R3061
R3062
100K
IO_PMU_TO_MANY_SYSTEM_ALIVE
IO_PMU_TO_SYSTEM_RESET_L
NTCs
CHARGER NTC
C3045
100PF
R3045
10KOHM-1%
CHARGER_NTC
NTC_CHARGER_RETURN
OMIT
XW3045
NO_XNET_CONNECTION
REAR CAMERA NTC
C3042
R3042
REAR_CAMERA_NTC
RCAM_NTC_RETURN
XW3042
RADIO PA NTC
C3043
R3043
RADIO_PA_NTC
PA_NTC_RETURN
XW3043
AP NTC
C3044
R3044
AP_NTC
AP_NTC_RETURN
XW3044
LAT NTC ON BOTTOM BOARD
Only has DS control when powered by VBUCK3
SYSTEM INTERFACE/AUX
U2700
TMLF49B0-APZ
WLCSP
SYM 4 OF 5
IO_AP_TO_PMU_RESET
IO_HYDRA_TO_PMU_RESET
IO_AP_TO_PMU_SOCHOT_L
IO_PMU_TO_SYSTEM_RESET_L
IO_PMU_TO_AP_HYDRA_ACTIVE_READY
CLK_PMU_TO_AOP_32K
CLK_PMU_TO_TOUCH_32K
IO_PMU_TO_MANY_SYSTEM_ALIVE
IO_TOUCH_TO_MANY_SCAN_ACTIVE
GPIO_PMU_TO_AP_DOUBLE_CLICK_DET_L
IO_PMU_TO_DOTARA_RESET_L
IO_HYDRA_TO_NUB_PMU_DOCK_CONNECT
SPMI0_NUB_TO_PMU_DOTARA_CLK
SPMI0_NUB_BI_PMU_DOTARA_DATA
AMUX_PMU_FROM_AP_ANALOGMUX_OUT
CHESTNUT_FROM_DISPLAY_PWR_EN
AMUX_WIDE_PVDD
IO_HYDRA_TO_PMU_USB_BRICK_ID_TIA
AMUX_PMU_FROM_GECKO
AMUX_PMU_TO_ADC_IN
AMUX_PMU_AY
R3011
200K
ROOM=PMU
NOSTUFF
GPIO_AP_TO_AMUX_PMU_SYNC
CHESTNUT_TO_PMU_AMUX
AMUX_PMU_FROM_CAM_PMU1
GPIO_CAM_PMU1_FROM_RIGEL_INT
GPIO_PMU_TO_AMUX_PMU_SUPER_TP
CLK_AP_TO_PMU_TST_CLKOUT
GPIO_PMU_TO_WLAN_R1_32K_CLK
AMUX_PMU_BY
SIM_NTC
REAR_CAMERA_NTC
RADIO_PA_NTC
AP_NTC
CHARGER_NTC
PMU_TCAL
C3020
R3020
3.92K
PMU_XTAL1
PMU_XTAL2
PMU_VSS_RTC
CRITICAL
Y3000
32.768KHZ-20PPM-12.5PF
C3051
C3052
22PF
XW3000
SWD_NUB_TO_MANY_SWCLK
RESET_IN1
RESET_IN2
RESET_IN3
RESET*
SHDN
ACTIVE_READY
SLEEP_32K
OUT_32K
SYS_ALIVE
FORCE_SYNC
DBLCLICK_DET
CRASH*
FAULT_OUT*
LDO13_EN
SPMI_SCLK
SPMI_SDATA
AMUX_AY
AMUX_BY
TDEV1
TDEV2
TDEV3
TDEV4
TDEV5
TCAL
XIN
XOUT
VSS
NXTAL_MEMS
DFT_CTRL<0>
DFT_CTRL<1>
IREF
VREF
VSS_REF
VREF_ADC
VDD_MAIN_SNS
UVWARN*
VDD_BOOST_UVLO_L
CPU_TRIGGER0*
CPU_TRIGGER1*
GPU_TRIGGER0*
GPU_TRIGGER1*
BRICK_ID1
BRICK_ID2
ADC_IN
IBAT
VBAT
BUTTON1
BUTTON2
BUTTON3
BUTTON4
BUTTONO1
BUTTONO2
BUTTONO3
R3010
200K
C3010
1.5UF
OMIT
XW3046
C3099
0.1UF
PMU_IREF
PMU_VREF
PMU_VSS_REF
PMU_VREF_ADC
VDD_MAIN_SNS
IO_PMU_TO_AP_PRE_UVLO_L
IO_AP_FROM_PMU_CPU_TRIGGER0_L
IO_AP_FROM_PMU_CPU_TRIGGER1_L
IO_AP_FROM_PMU_GPU_TRIGGER0_L
IO_AP_FROM_PMU_GPU_TRIGGER1_L
IO_HYDRA_TO_PMU_USB_BRICK_ID_TIA
ANALOG_PMU_VDD_MAIN_SENSE_FILT
AMUX_PMU_TO_ADC_IN
PMU_VDD_MAIN_ISENSE
PMU_VDD_MAIN_VSENSE
IO_BUTTON_VOL_DOWN_L
IO_BUTTON_SIDE_L
IO_BUTTON_VOL_UP_L
IO_BUTTON_RINGER_A
IO_PMU_TO_AP_VOL_DOWN_L
IO_PMU_TO_AP_SIDE_L
GPIO_PMU_TO_CCG2_RESET_L
GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L
SWD_NUB_BI_PMU_SWDIO
NC_PMU_GPIO_4
GPIO_PMU_NFC_TO_ARC_TRIG
GPIO_PMU_NFC_TO_ARC_RESET_L
GPIO_PMU_TO_BBPMU_RESET_L
NC_PMU_GPIO8
GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L
NC_PMU_GPIO10
NC_PMU_GPIO11
GPIO_PMU_FROM_CODEC_WAKE_L
GPIO_PMU_FROM_YANGTZE_INT_L
GPIO_PMU_TO_R1_RESET_L
GPIO_PMU_TO_AMUX_PMU_SUPER_TP
GPIO_PMU_FROM_WLAN_HOST_WAKE
GPIO_PMU_TO_WLAN_REG_ON
GPIO_PMU_TO_WLAN_R1_32K_CLK
GPIO_PMU_TO_SPKAMP_BOT_RESET_L
GPIO_PMU_TO_NFC_EN
GPIO_PMU_TO_BOOST_EN
I2C2_AP_SCL
GPIO_PMU_TO_DISPLAY_RESET_L
GPIO_PMU_TO_DISPLAY_PANICB
GPIO_PMU_TO_DOTARA_EN_EXT_1V8
R3090
200K
REQUIRED TO PREVENT STARTUP GLITCH
R3091
200K
SEQUENCED
PMU_VDD_RTC_DIG cap tracker rdar#: 29938782
R3003
9.53K
ANALOG_PMU_VDD_MAIN_SENSE
ANALOG_PMU_VDD_MAIN_SENSE_FILT
C3003
0.1UF

Boost Enable Pull



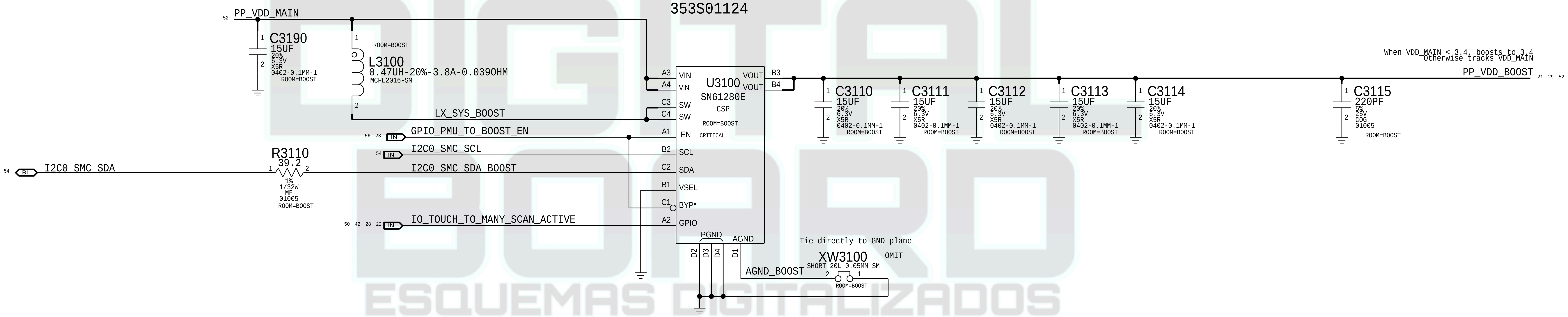
L3100

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00871	152S00869	ALT_PARTS	ALL	IND,PWR,0.47UH,20%,CYNTEC,2016
152S00873	152S00869	ALT_PARTS	ALL	IND,PWR,0.47UH,20%,TDK,2016

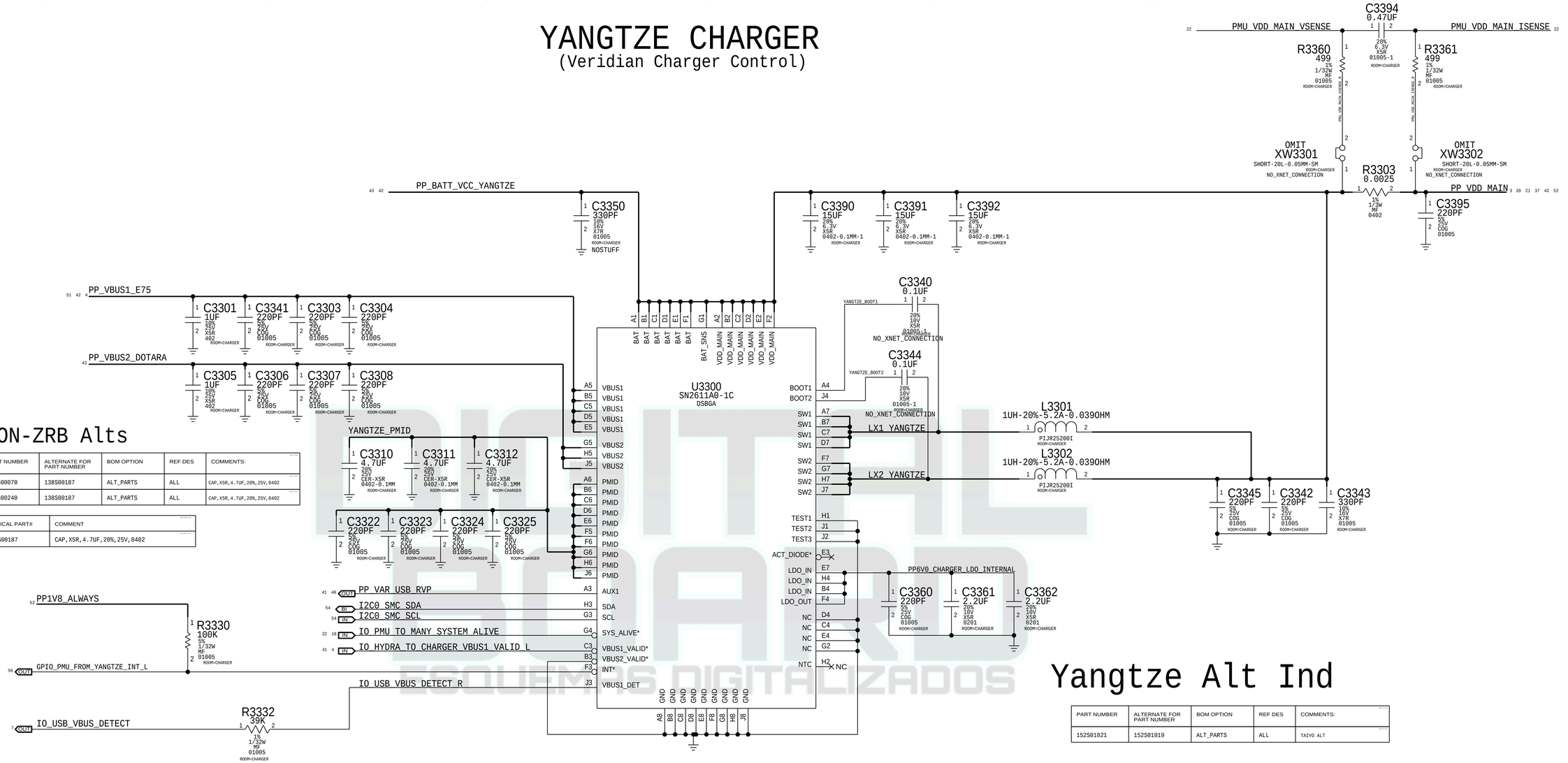
CRITICAL PART#	COMMENT
152S00869	IND,PWR,0.47UH,20%,3.8A,39MOHM,TAIYO,2016

BOOST

353S01124



YANGTZE CHARGER
(Veridian Charger Control)



NON-ZRB Alts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00070	138S00187	ALT_PARTS	ALL	CAP,X5R,4.7UF,20%,25V,0402
138S00240	138S00187	ALT_PARTS	ALL	CAP,X5R,4.7UF,20%,25V,0402

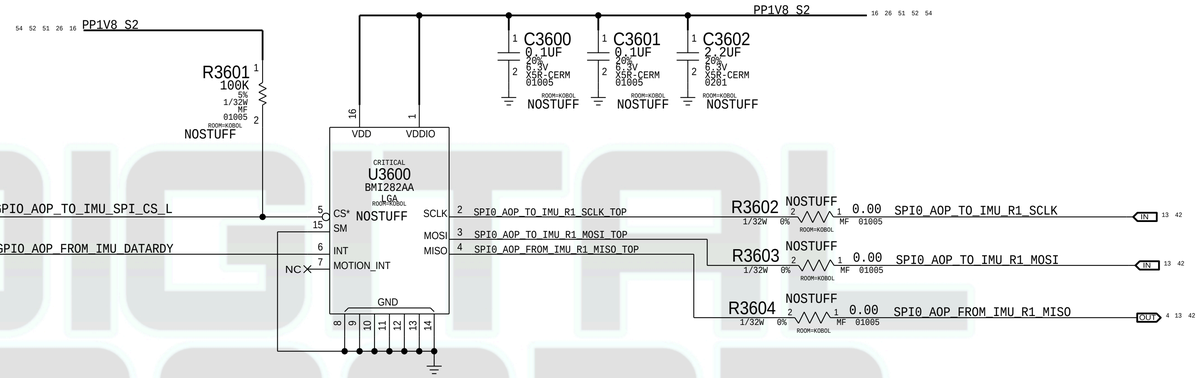
CRITICAL PART#	COMMENT
138S00187	CAP,X5R,4.7UF,20%,25V,0402

Yangtze Alt Ind

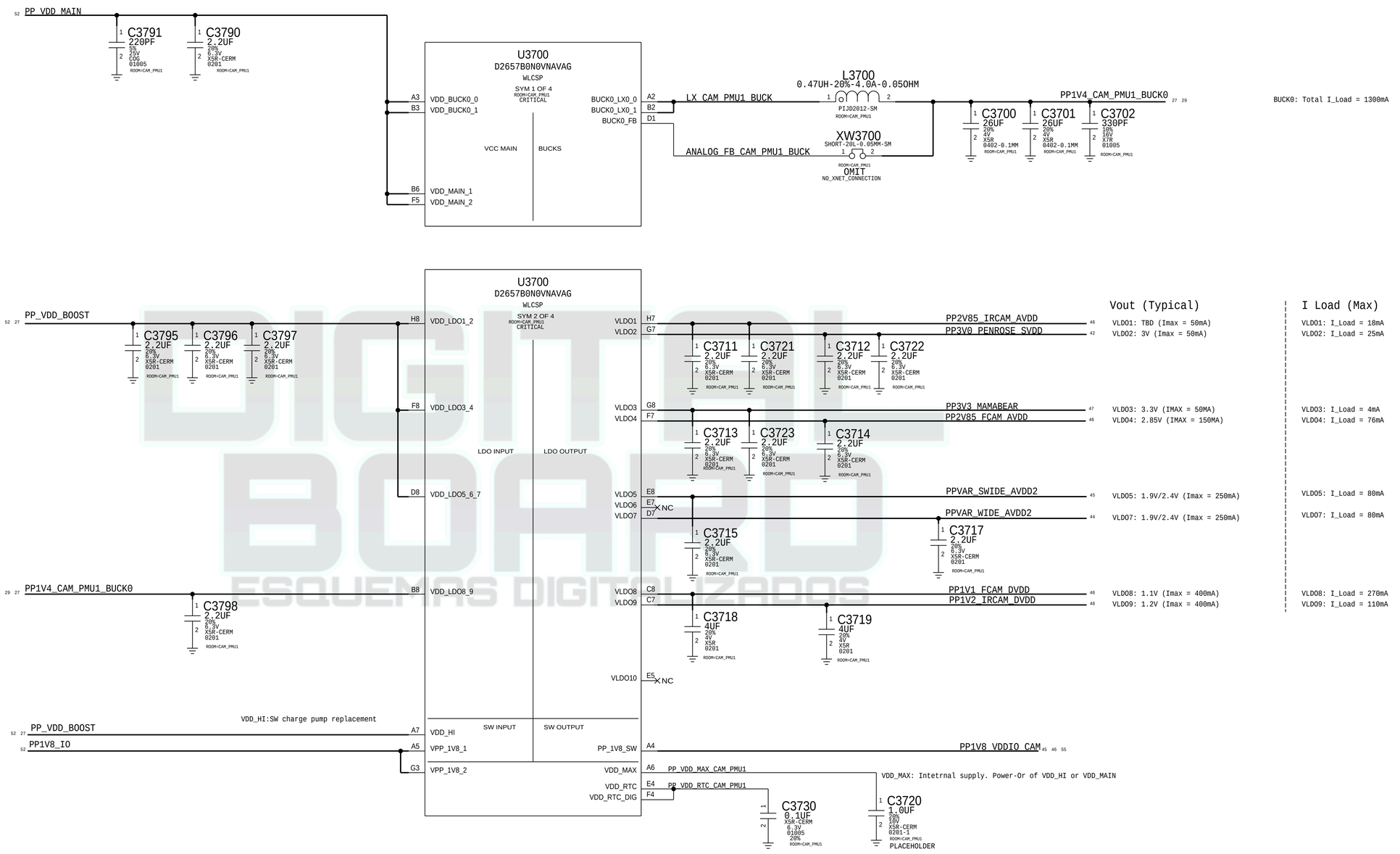
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01021	152S01019	ALT_PARTS	ALL	TAIYO ALT

Kobol - Accel & Gyro

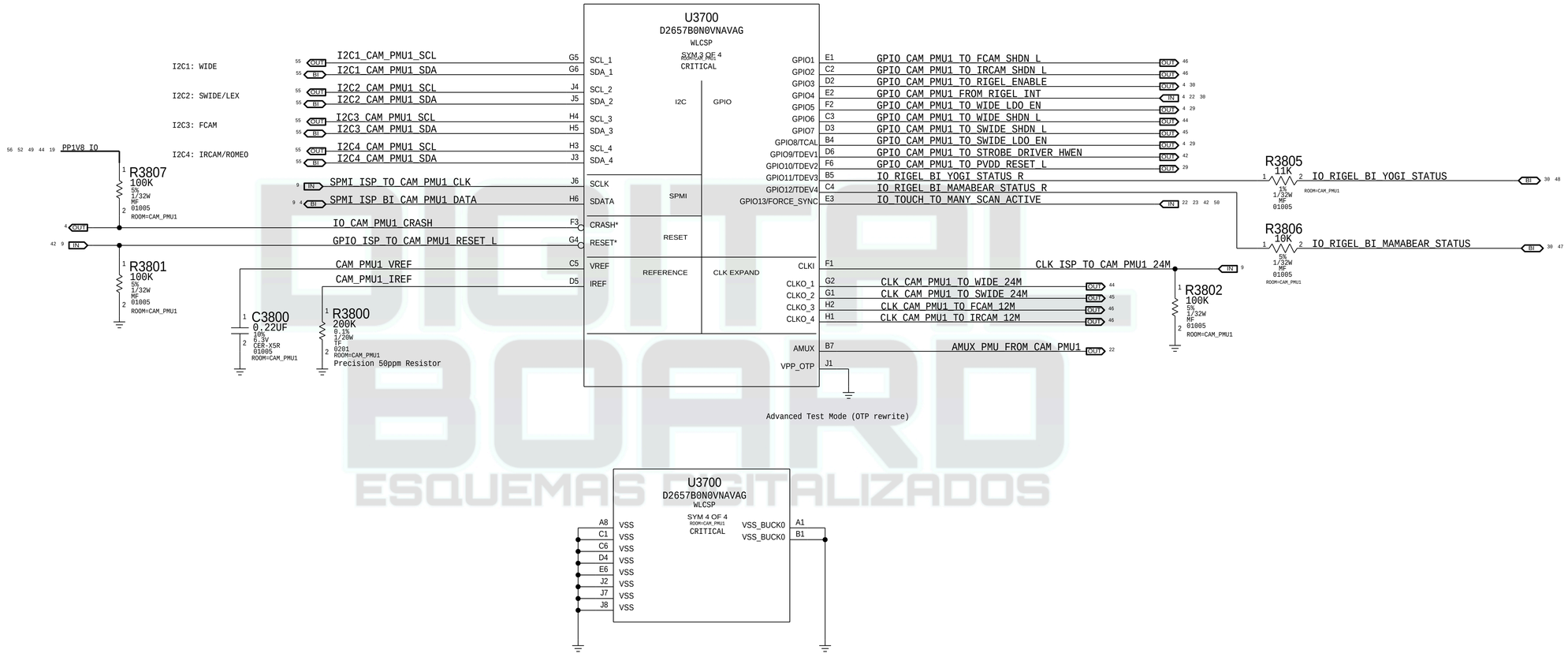
APN: 338S00367



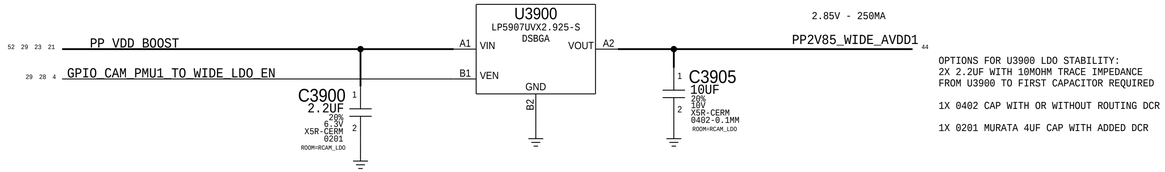
CAMERA PMU1



CAMERA PMU1



WIDE AVDD_ADC LDO



OPTIONS FOR U3900 LDO STABILITY:
2X 2.2UF WITH 10MOHM TRACE IMPEDANCE FROM U3900 TO FIRST CAPACITOR REQUIRED

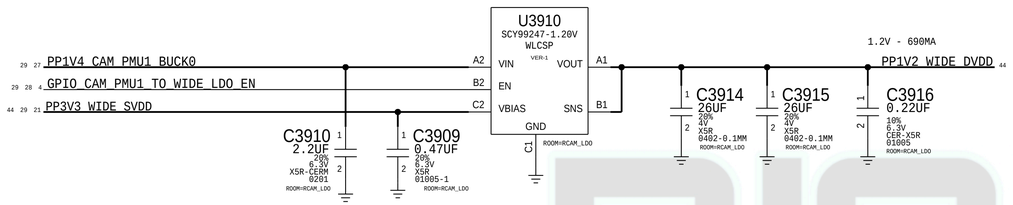
1X 0402 CAP WITH OR WITHOUT ROUTING DCR

1X 0201 MURATA 4UF CAP WITH ADDED DCR

Camera LDO Alts

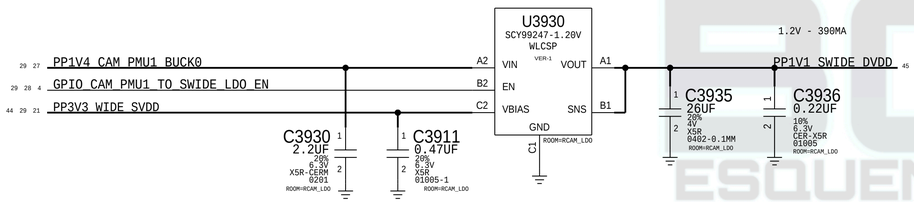
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01728	353S00015	ALT_PARTS	U3900,U3960	ONSEMI ALTERNATE
353S01690	353S01904	ALT_PARTS	U3910,U3930	OLDER ALTERNATE

WIDE DVDD LDO



Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

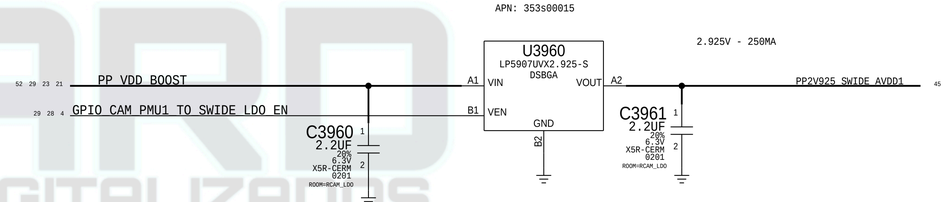
SUPERWIDE VDDL LDO



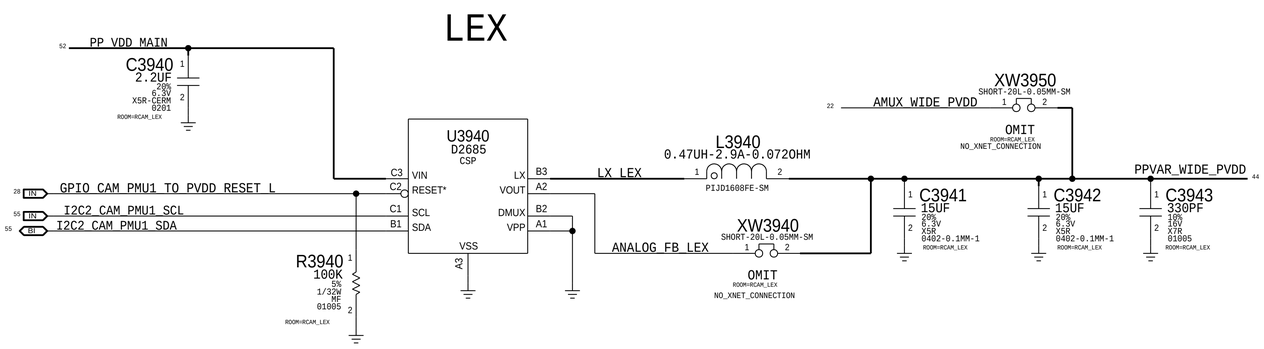
Enable operation: Assert EN after VIN and VBIAS rails reach nominal levels

SUPERWIDE AVDD LDO

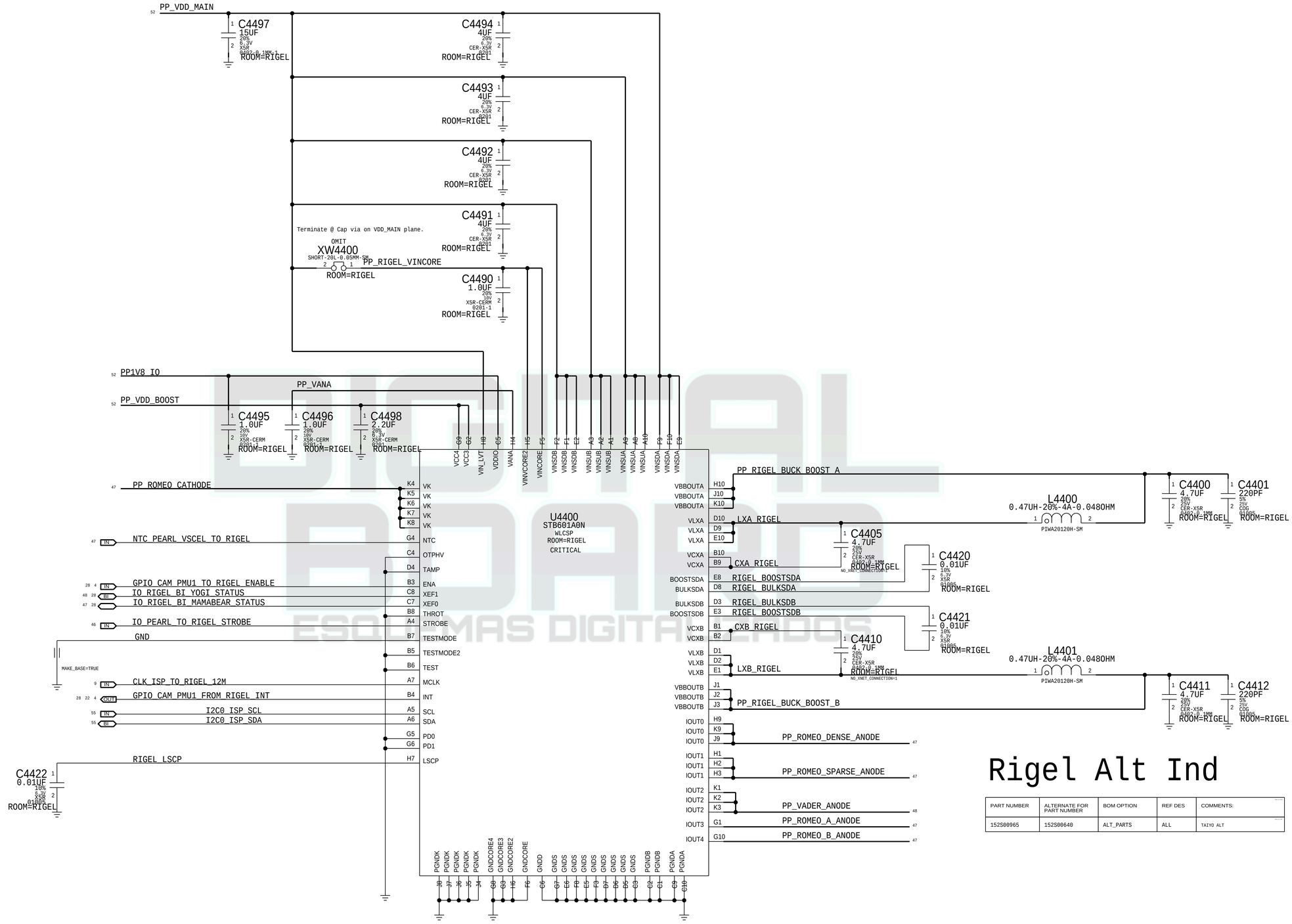
APN: 353s00015



LEX



Rigel Driver



Rigel Alt Ind

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00965	152S00640	ALT_PARTS	ALL	TAIYO ALT

BRIGHTON AUDIO CODEC (ANALOG INPUTS & OUTPUTS)

U4700
CS42L77A1
WLCSP
SYM 1 OF 4
CRITICAL
ROOM=CODEC

51 IN MIC1_LOWER_TO_CODEC_AIN1_P → M8 AIN1+
51 IN MIC1_LOWER_TO_CODEC_AIN1_N → L8 AIN1-
42 IN MIC2_REAR_TO_CODEC_AIN2_P → M11 AIN2+
42 IN MIC2_REAR_TO_CODEC_AIN2_N → L11 AIN2-
48 IN MIC3_FRONT_TO_CODEC_AIN3_P → M9 AIN3+
48 IN MIC3_FRONT_TO_CODEC_AIN3_N → L9 AIN3-
51 IN MIC4_LOWER_TO_CODEC_AIN4_P → M10 AIN4+
51 IN MIC4_LOWER_TO_CODEC_AIN4_N → L10 AIN4-

42 IN PENROSE_IR_TO_CODEC_AIN5_POS → XW4750 SHORT-20L-0.05MM-SM (OMIT, NO_XNET_CONNECTION) → PENROSE_IR_TO_CODEC_AIN5_P → M3 AIN5A+
42 31 IN PENROSE_IR_VIS_TO_CODEC_RTN → C4750 0.22UF 10% 6.3V CER-X5R 01005 NO_XNET_CONNECTION (PLACE_NEAR=J_INT_BOT.387:3MM) → PENROSE_IR_TO_CODEC_AIN5_N → L3 AIN5A-

L4 AIN5B+
L5 AIN5B-

42 IN PENROSE_VIS_TO_CODEC_AIN6_POS → XW4751 SHORT-20L-0.05MM-SM (OMIT, NO_XNET_CONNECTION) → PENROSE_VIS_TO_CODEC_AIN6_P → K5 AIN6A+
42 31 IN PENROSE_IR_VIS_TO_CODEC_RTN → C4751 0.22UF 10% 6.3V CER-X5R 01005 NO_XNET_CONNECTION → PENROSE_VIS_TO_CODEC_AIN6_N → K4 AIN6A-

L2 AIN6B+
M2 AIN6B-

J2 AIN7+
K2 AIN7-

J3 AIN8+
K3 AIN8-

H3 AIN9+
H2 AIN9-

J4 AIN10+
J5 AIN10-

L6 AIN11+
L7 AIN11-

K7 AIN12+
K6 AIN12-

34 OUT PDM_OUT1_CODEC_TO_SPKAMP_TOP_CLK → A6 PDMOUT1_CLK
34 OUT PDM_OUT1_CODEC_TO_SPKRAMP_TOP_DATA → D6 PDMOUT1_DATA
B6 PDMOUT2_CLK
C6 PDMOUT2_DATA

AOUT+ F11 → CODEC_AOUT_TO_HAC_POS 48
AOUT- G11 → CODEC_AOUT_TO_HAC_NEG 48

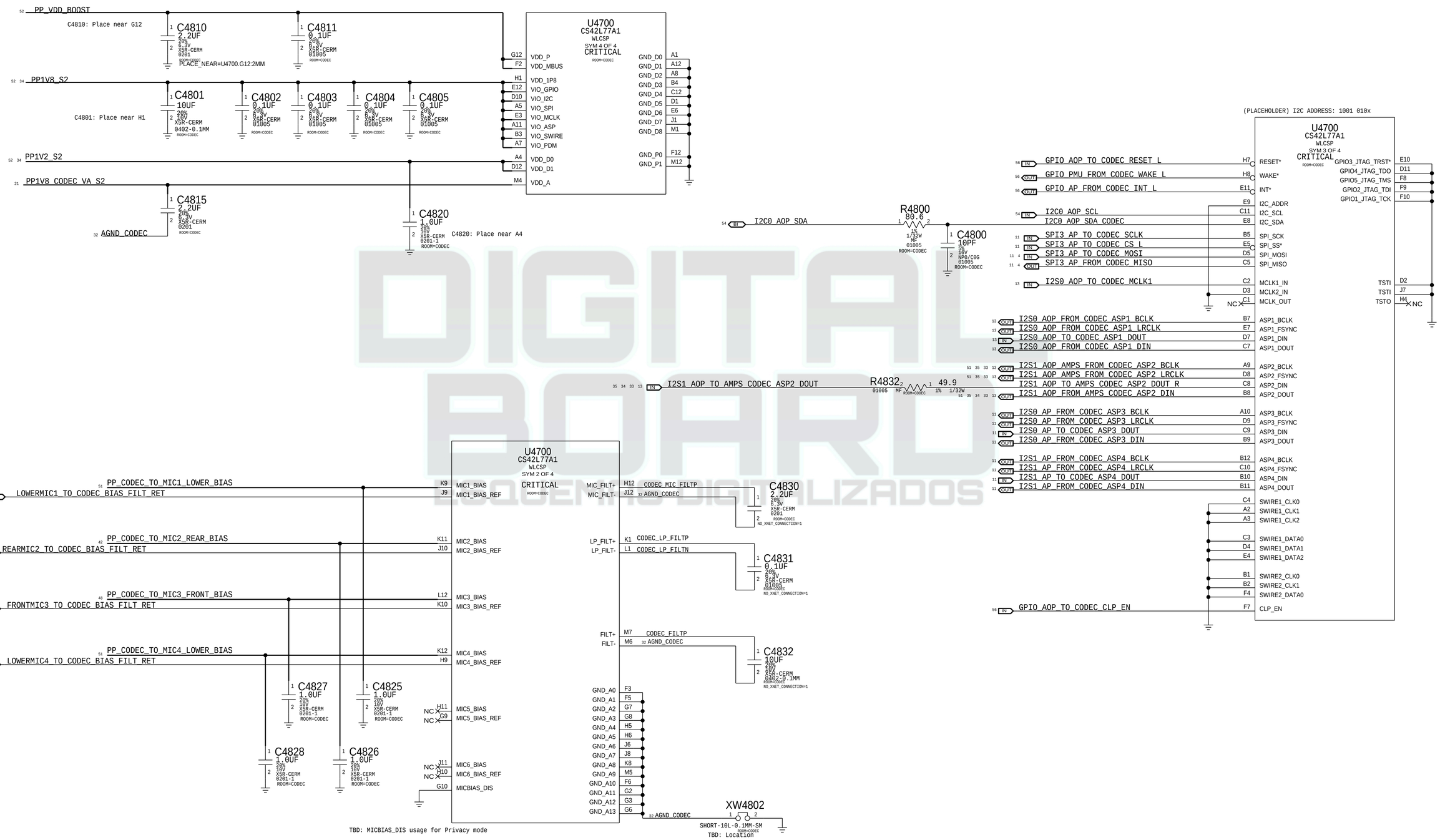
DP F1 ← 90_MIKEYBUS_CODEC_DATA_P
DN E1 ← 90_MIKEYBUS_CODEC_DATA_N
MBUS_REF E2 ← MIKEYBUS_REFERENCE IN 51
R4710 100 5% 1/32W MF 01005 ROOM=CODEC (Can be placed near Dock Connector)

C4700 100PF 5% 16V NP0-C0G 01005-1 ROOM=CODEC
R4700 20.0 5% 1/32W MF 01005 ROOM=CODEC
90_MIKEYBUS_DATA_P BI 41
R4701 20.0 5% 1/32W MF 01005 ROOM=CODEC
90_MIKEYBUS_DATA_N BI 41
C4701 100PF 5% 16V NP0-C0G 01005-1 ROOM=CODEC

LDCM

TIA_EXOUT G4 NC
TIA_OUT G5 → HALOGEN_TIA_IOUT → C4720 220PF 5% 25V C0G 01005 ROOM=CODEC
TIA_SENSE G1 → HALOGEN_TIA_IN → R4721 200K 1% 1/32W MF 01005 ROOM=CODEC → IO_HYDRA_TO_PMU_USB_BRICK_ID_TIA IN 22 41
C4721 10UF 20% 10V X5R-CERM 0402-0.1MM ROOM=CODEC NO_XNET_CONNECTION

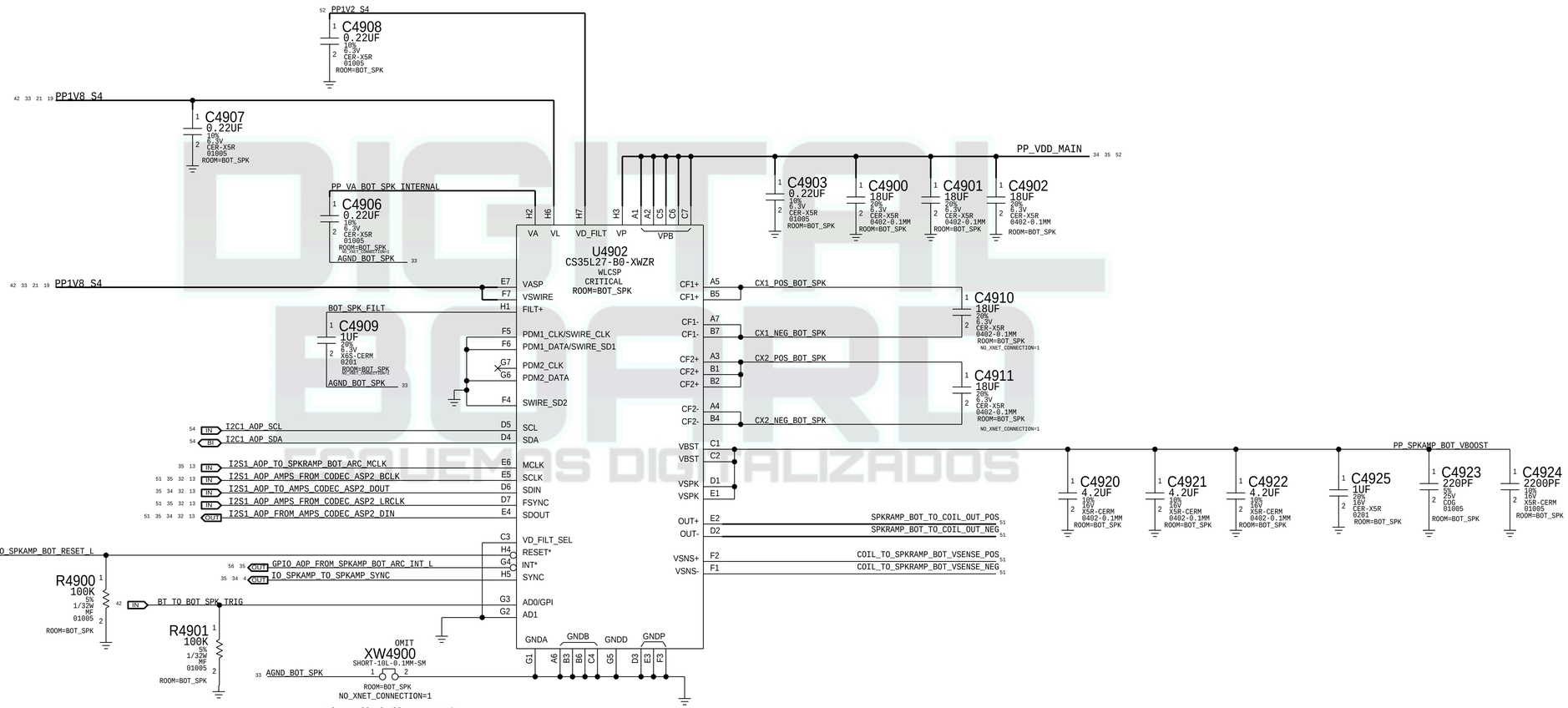
BRIGHTON AUDIO CODEC (POWER & I/O)



Amp: South Speaker

AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	AOP I2C1
ARC	0	1	TBD2	

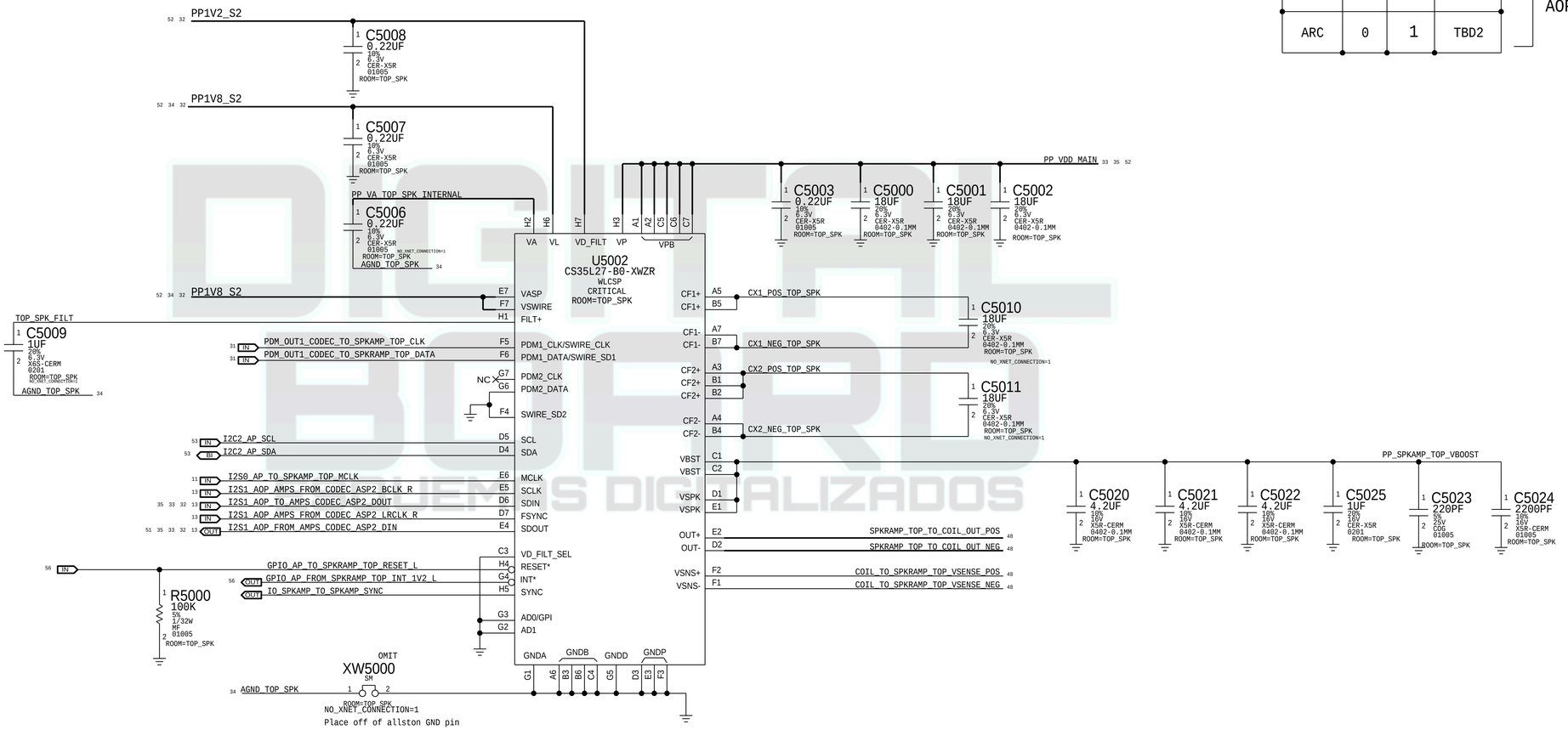
-----> BOT



Amp: North Speaker

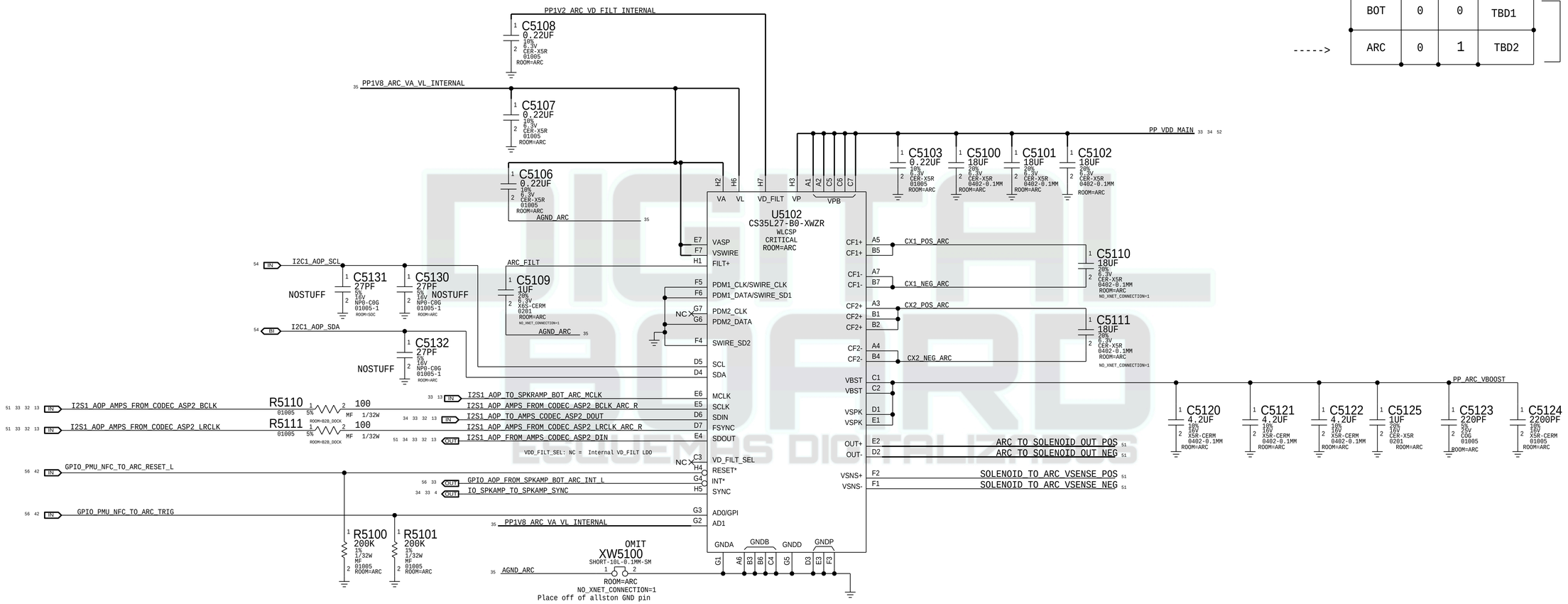
TODO: Verify I2C Table

AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	A0P I2C1
ARC	0	1	TBD2	

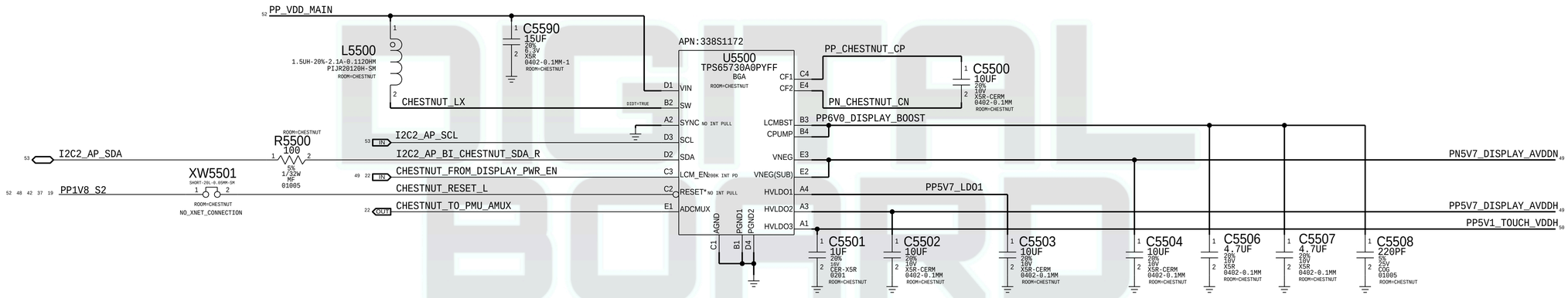


Amp: Arc

AMP	AD0	AD1	I2C_ADR	
TOP	0	0	TBD1	AP I2C2
BOT	0	0	TBD1	AOP I2C1
ARC	0	1	TBD2	



CHESTNUT DISPLAY PMU

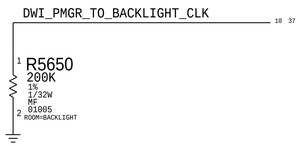


Chestnut Alt Ind

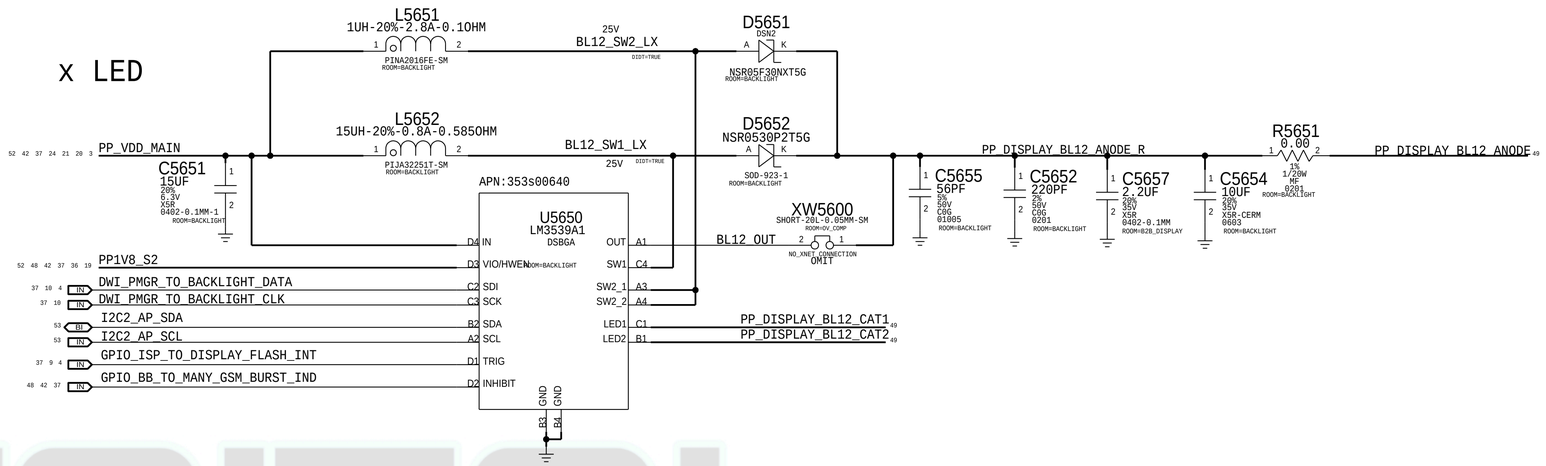
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00913	152S00938	ALT_PARTS	L5500	XTAL, 24M, 1612

MUON - LED BACKLIGHT DRIVERS

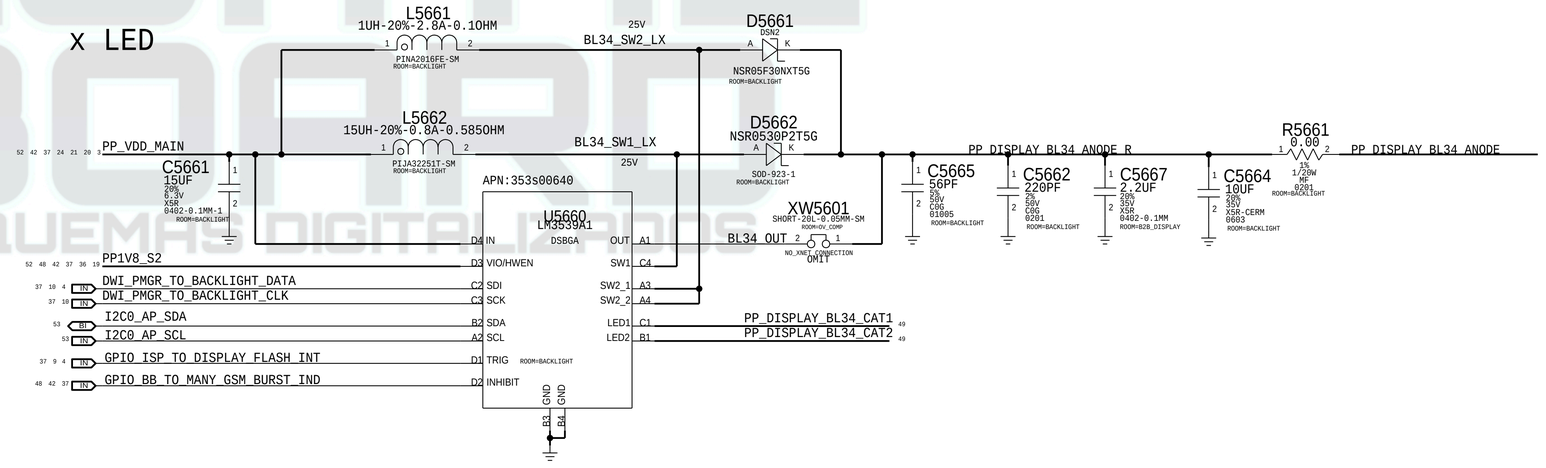
DWI Clock Pull



x LED



x LED

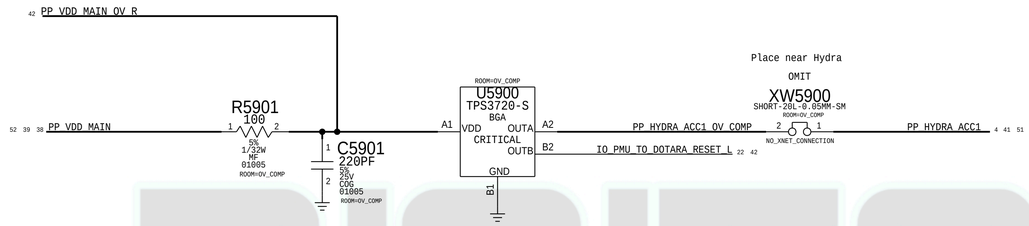


Muon Inductor Alt

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00940	152S00939	ALT_PARTS	L5652,L5662	IND, TAIYO,15UH,0.8A,3225

VDD_MAIN COMPARATORS

VDD_MAIN OV CUT-OFF CIRCUIT

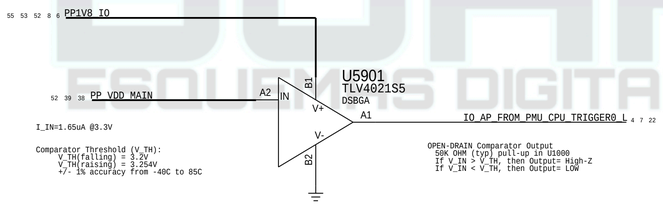


Voltage Threshold = 5.2V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S01375	353S01398	ALT_PARTS	U5900	ON SEMI

VDD_MAIN PRE-UPO COMPARATOR

APN:353S01976



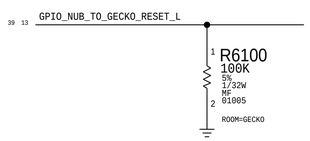
I_IN=1.65uA @3.3V

Comparator Threshold (V_TH):
V_TH(falling) = 3.2V
V_TH(raising) = 3.254V
+/- 1% accuracy from -40C to 85C

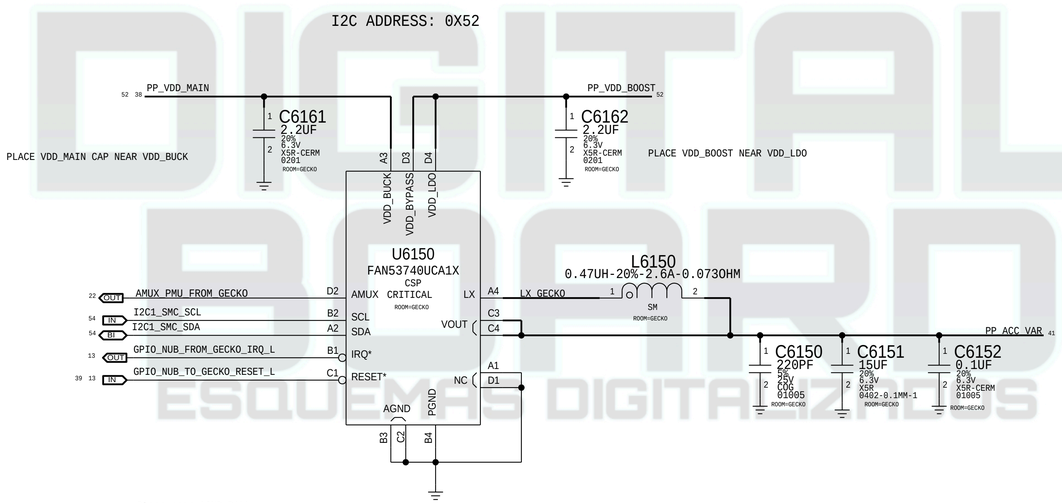
OPEN-DRAIN Comparator Output
50K OHM (typ) pull-up in U1000
If V_IN > V_TH, then Output= High-Z
If V_IN < V_TH, then Output= LOW

Gecko

GECKO Reset Pull Down



I2C ADDRESS: 0X52

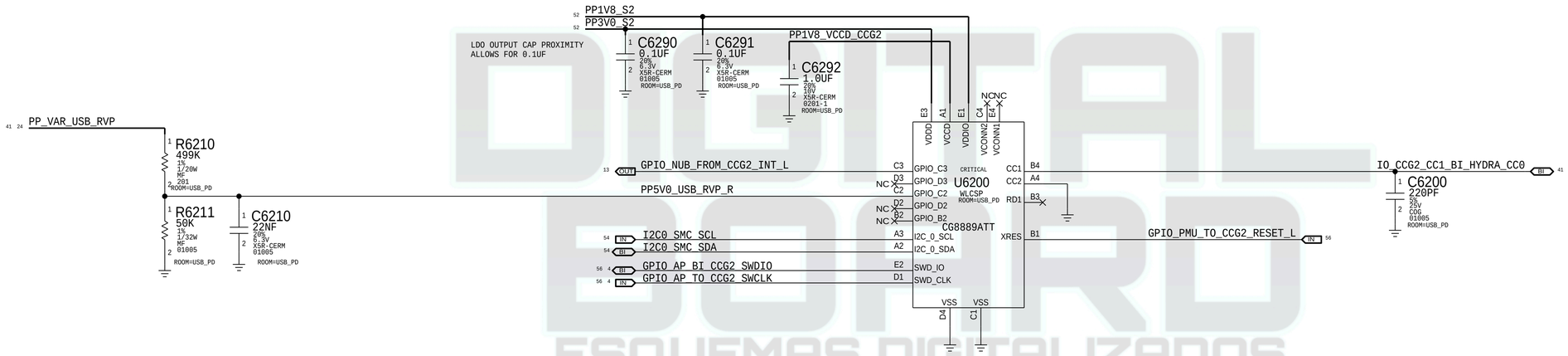


Place near AGND BALL

IND Alternate

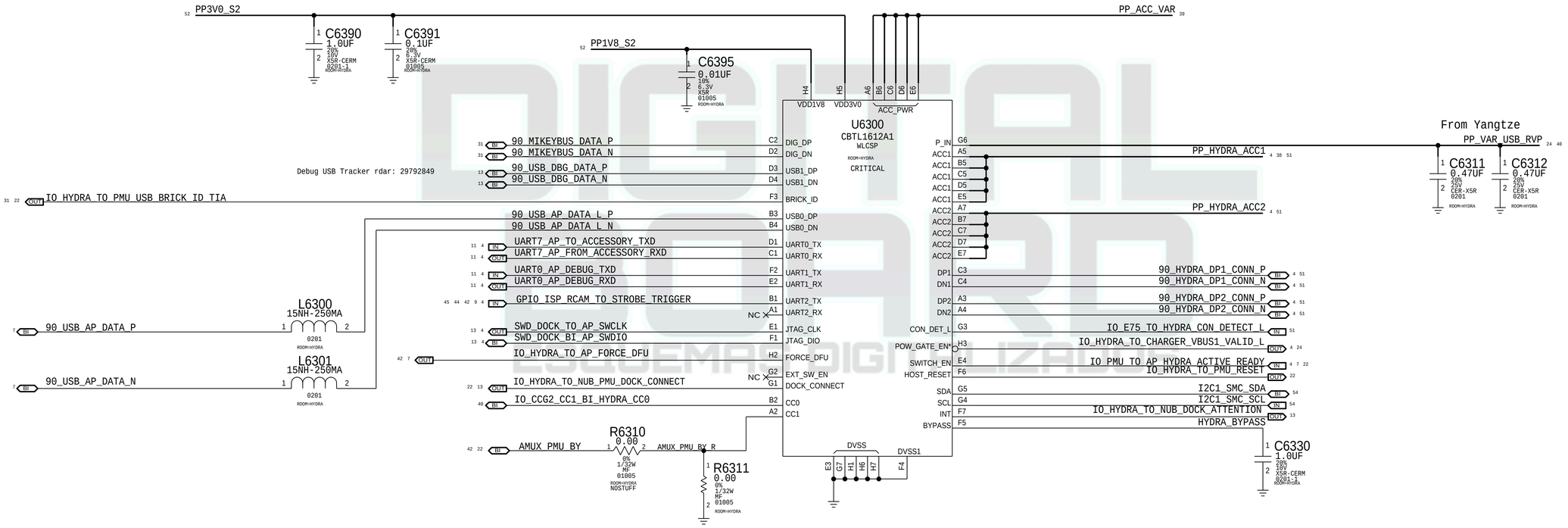
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00853	152S00759	ALT_PARTS	L6150	IND,PWR,0.47UH,20%,2.7A,TY

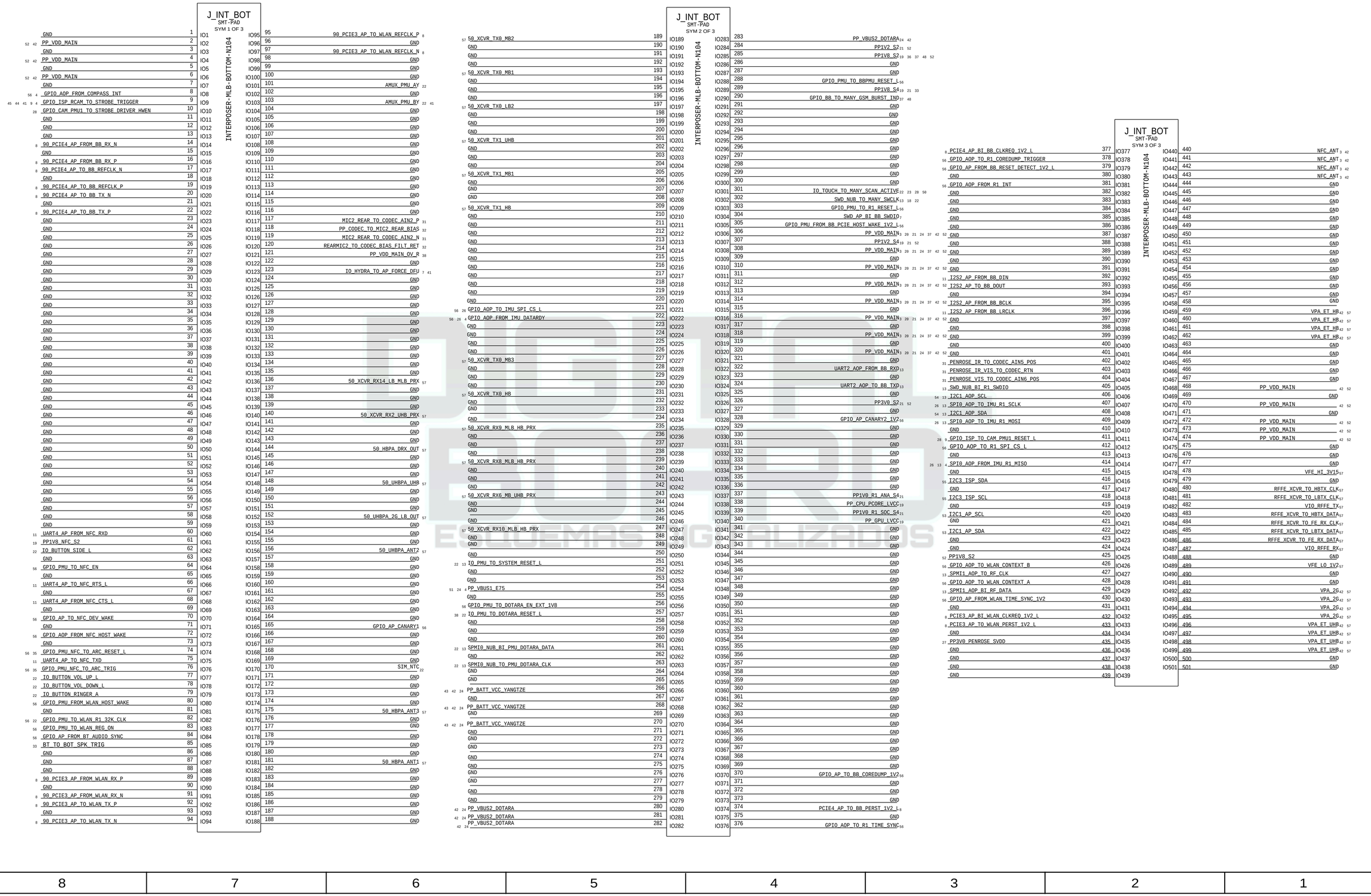
USB-PD



Hydra

I2C Address: 0011010X




J_INT_BOT
SMT-PAD
SYM 1 OF 3
INTERPOSER-MLB-BOTTOM-N104
GND 1
PP_VDD_MAIN 2
GND 3
PP_VDD_MAIN 4
GND 5
PP_VDD_MAIN 6
GND 7
GPIO_AOP_FROM_COMPASS_INT 8
GPIO_ISP_RCAM_TO_STROBE_TRIGGER 9
GPIO_CAM_PMU1_TO_STROBE_DRIVER_HWEN 10
GND 11
GND 12
GND 13
90_PCIE4_AP_FROM_BB_RX_N 14
GND 15
90_PCIE4_AP_FROM_BB_RX_P 16
90_PCIE4_AP_TO_BB_REFCLK_N 17
GND 18
90_PCIE4_AP_TO_BB_REFCLK_P 19
90_PCIE4_AP_TO_BB_TX_N 20
GND 21
90_PCIE4_AP_TO_BB_TX_P 22
GND 23
GND 24
GND 25
GND 26
GND 27
GND 28
GND 29
GND 30
GND 31
GND 32
GND 33
GND 34
GND 35
GND 36
GND 37
GND 38
GND 39
GND 40
GND 41
GND 42
GND 43
GND 44
GND 45
GND 46
GND 47
GND 48
GND 49
GND 50
GND 51
GND 52
GND 53
GND 54
GND 55
GND 56
GND 57
GND 58
GND 59
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102 GND
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105 GND
106 GND
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108 GND
109 GND
110 GND
111 GND
112 GND
113 GND
114 GND
115 GND
116 GND
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118 PP_CODEC_TO_MIC2_REAR_BIAS
119 MIC2_REAR_TO_CODEC_AIN2_N
120 REARMIC2_TO_CODEC_BIAS_FILT_RET
121 PP_VDD_MAIN_OV_R
122 GND
123 IO_HYDRA_TO_AP_FORCE_DFU
124 GND
125 GND
126 GND
127 GND
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130 GND
131 GND
132 GND
133 GND
134 GND
135 GND
136 50_XCVR_RX14_LB_MLB_PRX
137 GND
138 GND
139 GND
140 50_XCVR_RX2_UHB_PRX
141 GND
142 GND
143 GND
144 50_HBPA_DRX_OUT
145 GND
146 GND
147 GND
148 50_UHBPA_UHB
149 GND
150 GND
151 GND
152 50_UHBPA_2G_LB_OUT
153 GND
154 GND
155 GND
156 50_UHBPA_ANT2
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164 GND
165 GPIO_AP_CANARY1
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168 GND
169 GND
170 SIM_NTC
171 GND
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174 GND
175 50_HBPA_ANT3
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177 GND
178 GND
179 GND
180 GND
181 50_HBPA_ANT1
182 GND
183 GND
184 GND
185 GND
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IO284 PP1V2_S2
IO285 PP1V8_S2
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IO287 GND
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IO289 PP1V8_S4
IO290 GPIO_BB_TO_MANY_GSM_BURST_IND
IO291 GND
IO292 GND
IO293 GND
IO294 GND
IO295 GND
IO296 GND
IO297 GND
IO298 GND
IO299 GND
IO300 GND
IO301 IO_TOUCH_TO_MANY_SCAN_ACTIVE
IO302 SWD_NUB_TO_MANY_SWCLK
IO303 GPIO_PMU_TO_R1_RESET_L
IO304 SWD_AP_BI_BB_SWDIO
IO305 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L
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IO307 PP1V2_S4
IO308 PP_VDD_MAIN
IO309 GND
IO310 PP_VDD_MAIN
IO311 GND
IO312 PP_VDD_MAIN
IO313 GND
IO314 PP_VDD_MAIN
IO315 GND
IO316 PP_VDD_MAIN
IO317 GND
IO318 PP_VDD_MAIN
IO319 GND
IO320 PP_VDD_MAIN
IO321 GND
IO322 UART2_AOP_FROM_BB_RXD
IO323 GND
IO324 UART2_AOP_TO_BB_TXD
IO325 GND
IO326 PP3V0_S2
IO327 GND
IO328 GPIO_AP_CANARY2_1V2
IO329 GND
IO330 GND
IO331 GND
IO332 GND
IO333 GND
IO334 GND
IO335 GND
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IO343 GND
IO344 GND
IO345 GND
IO346 GND
IO347 GND
IO348 GND
IO349 GND
IO350 GND
IO351 GND
IO352 GND
IO353 GND
IO354 GND
IO355 GND
IO356 GND
IO357 GND
IO358 GND
IO359 GND
IO360 GND
IO361 GND
IO362 GND
IO363 GND
IO364 GND
IO365 GND
IO366 GND
IO367 GND
IO368 GND
IO369 GND
IO370 GPIO_AP_TO_BB_COREDUMP_1V2
IO371 GND
IO372 GND
IO373 GND
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IO375 GND
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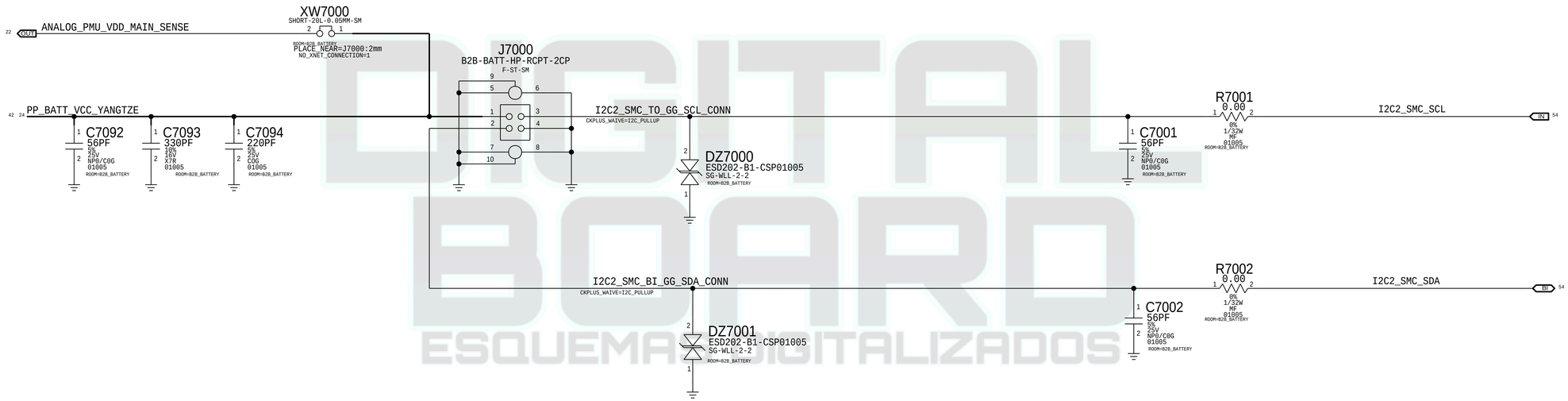
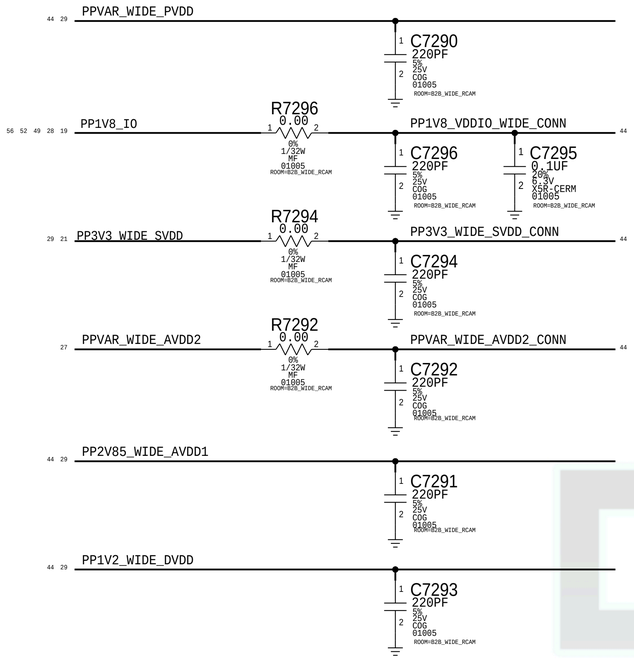
441 NFC_ANT3
442 NFC_ANT3
443 NFC_ANT3
444 GND
445 GND
446 GND
447 GND
448 GND
449 GND
450 GND
451 GND
452 GND
453 GND
454 GND
455 GND
456 GND
457 GND
458 GND
459 VPA_ET_HB
460 VPA_ET_HB
461 VPA_ET_HB
462 VPA_ET_HB
463 GND
464 GND
465 GND
466 GND
467 GND
468 PP_VDD_MAIN
469 GND
470 PP_VDD_MAIN
471 GND
472 PP_VDD_MAIN
473 PP_VDD_MAIN
474 PP_VDD_MAIN
475 GND
476 GND
477 GND
478 VFE_HI_3V15
479 GND
480 RFFE_XCVR_TO_HBTX_CLK
481 RFFE_XCVR_TO_LBTX_CLK
482 VIO_RFFE_TX
483 RFFE_XCVR_TO_HBTX_DATA
484 RFFE_XCVR_TO_FE_RX_CLK
485 RFFE_XCVR_TO_LBTX_DATA
486 RFFE_XCVR_TO_FE_RX_DATA
487 VIO_RFFE_RX
488 GND
489 VFE_LO_1V2
490 GND
491 GND
492 VPA_2G
493 VPA_2G
494 VPA_2G
495 VPA_2G
496 VPA_ET_UHB
497 VPA_ET_UHB
498 VPA_ET_UHB
499 VPA_ET_UHB
500 GND
501 GND

BATTERY CONNECTOR

RCPT: 516S00505 <-- This one on MLB
PLUG: 516S00506

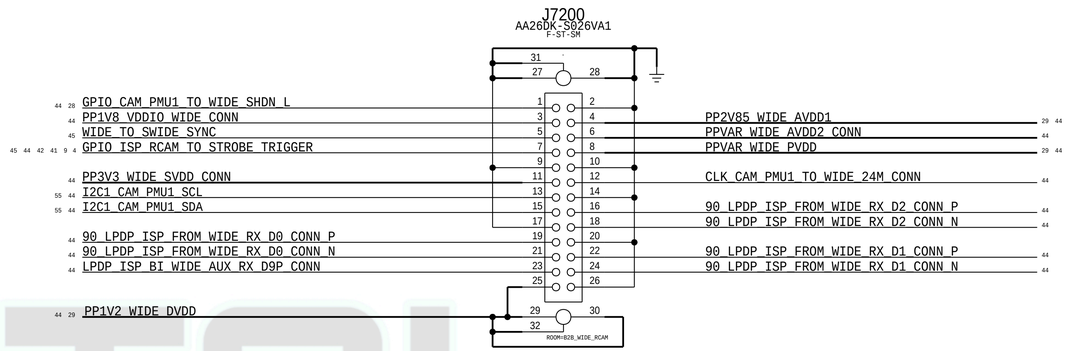


Power Filtering

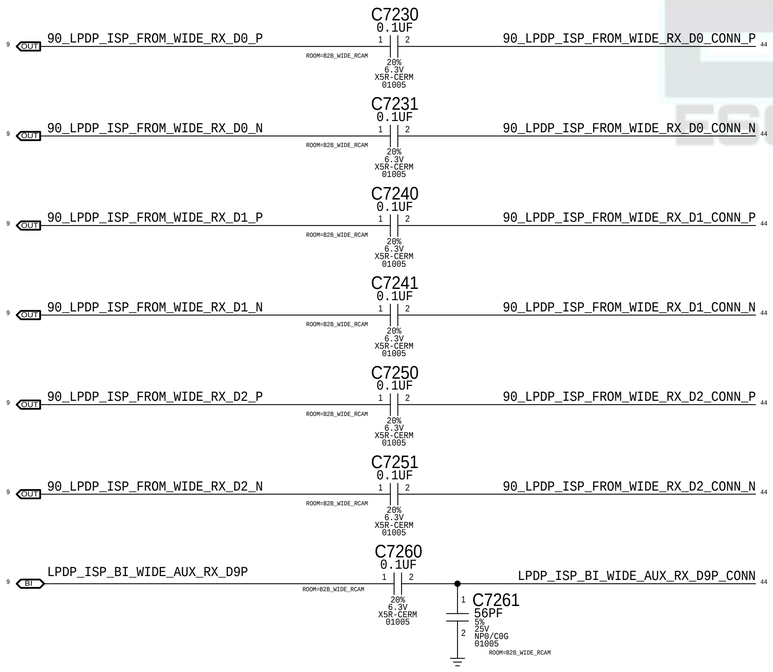


Wide Camera Connector

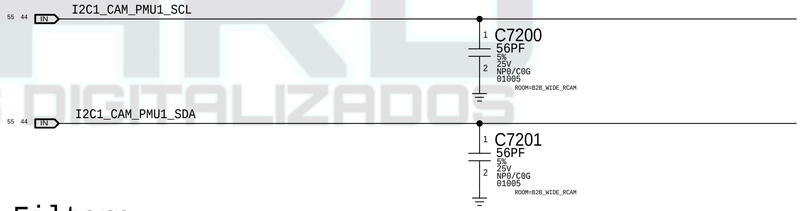
Rcpt: 516S00313 <-- This one on MLB
Plug: 516S00314



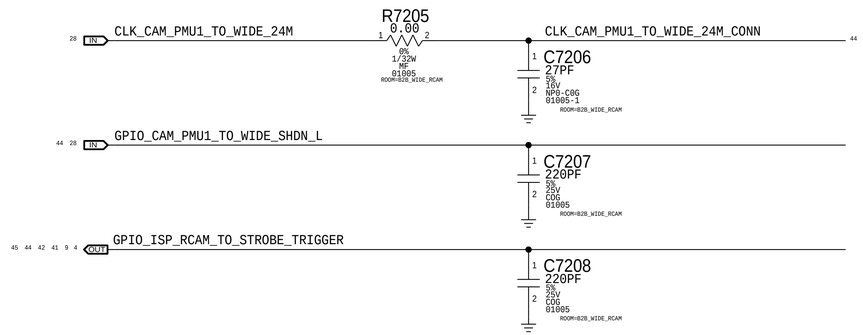
LPDP Filters



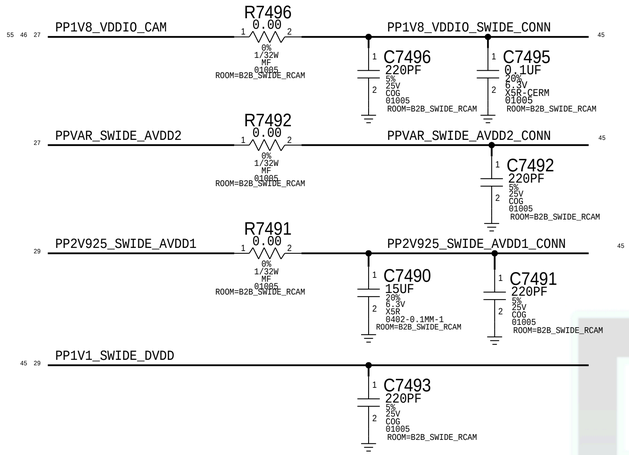
RCAM I2C



IO Filters

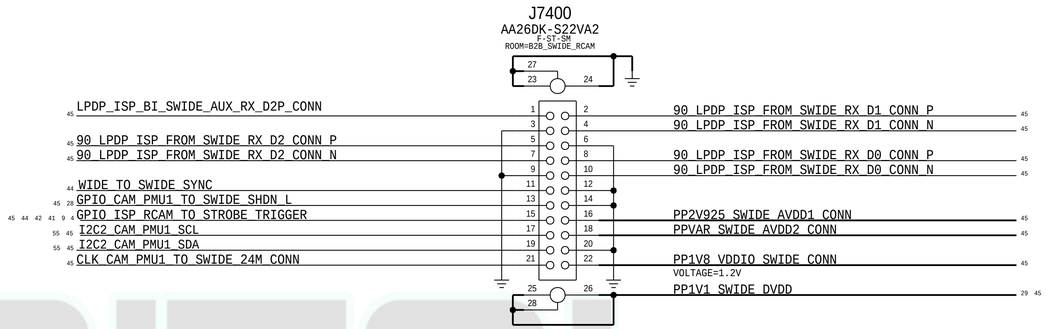


Power Filtering

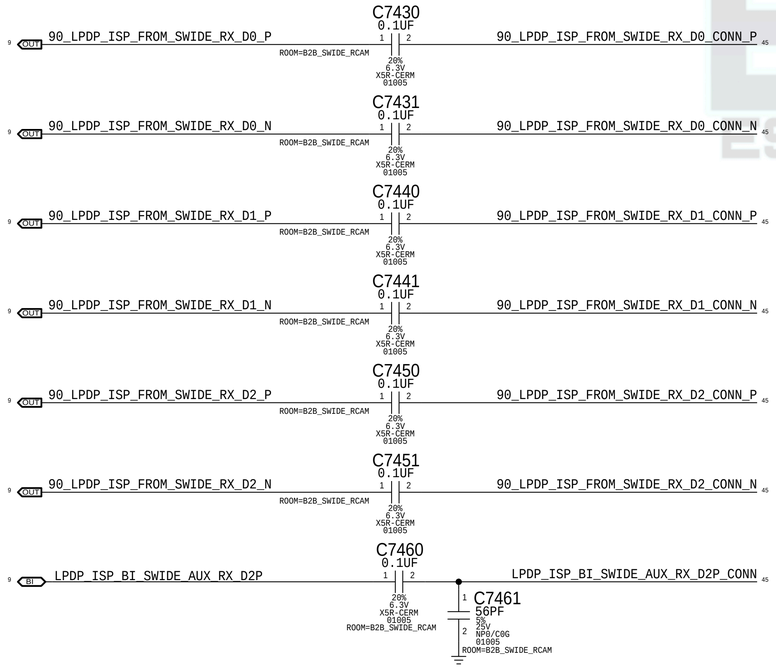


Super Wide Camera Connector

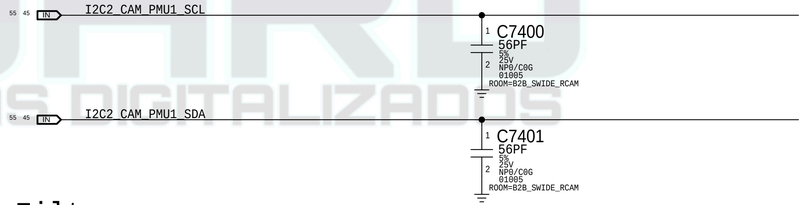
RCPT: 516S00458 <-- This one on MLB
PLUG: 516S00459



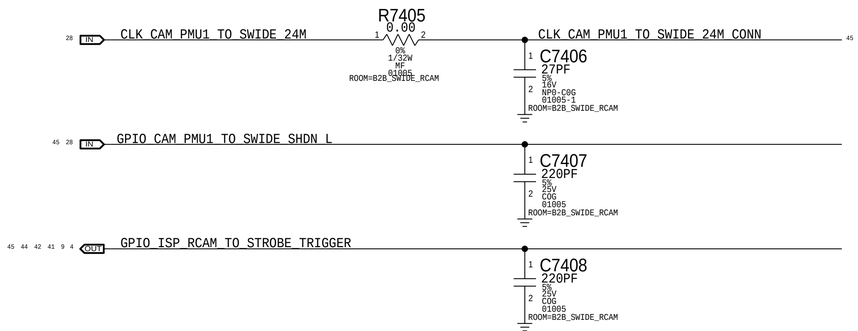
LPDP Filters



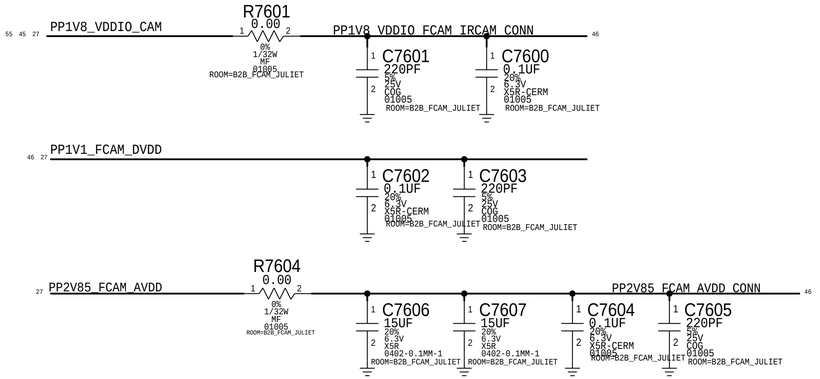
RCAM I2C



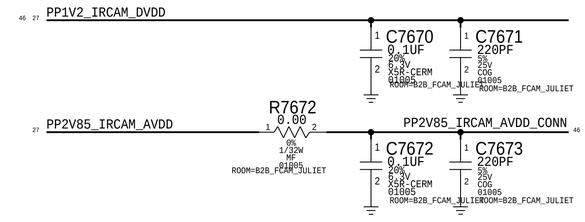
IO Filters



FCAM PO

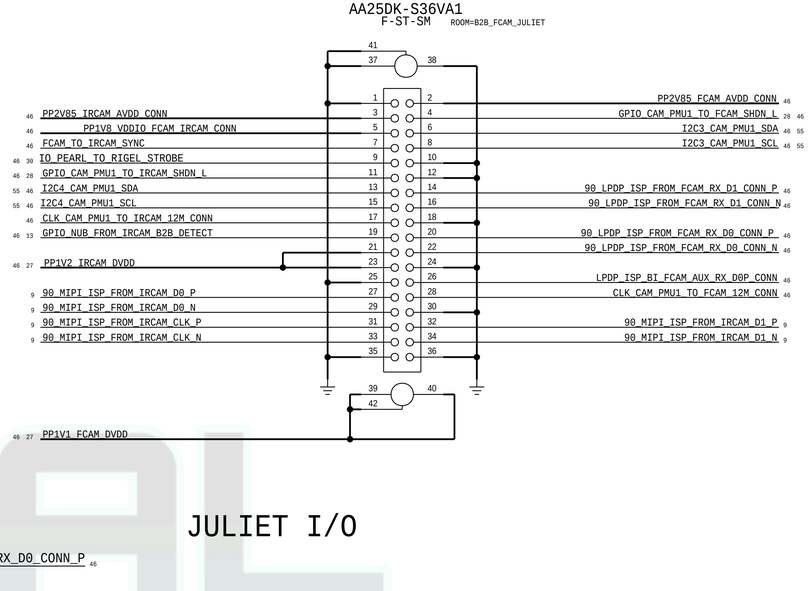


Juliet Power and I/O

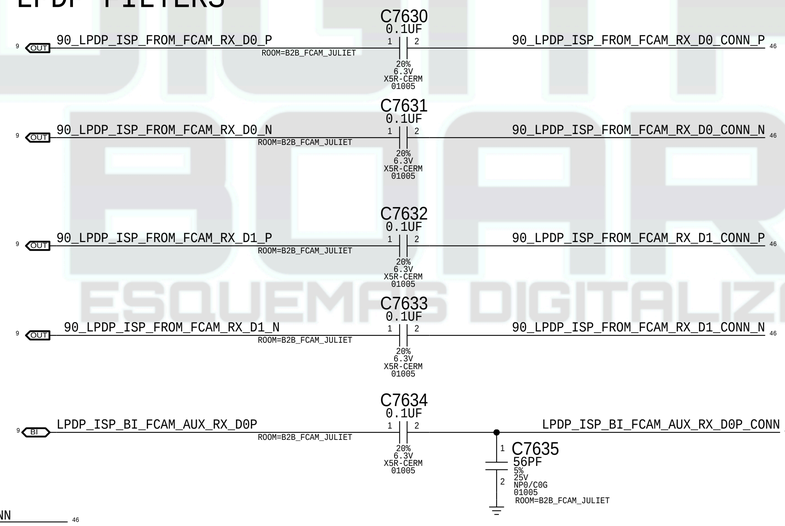


FCAM/Juliet Connector

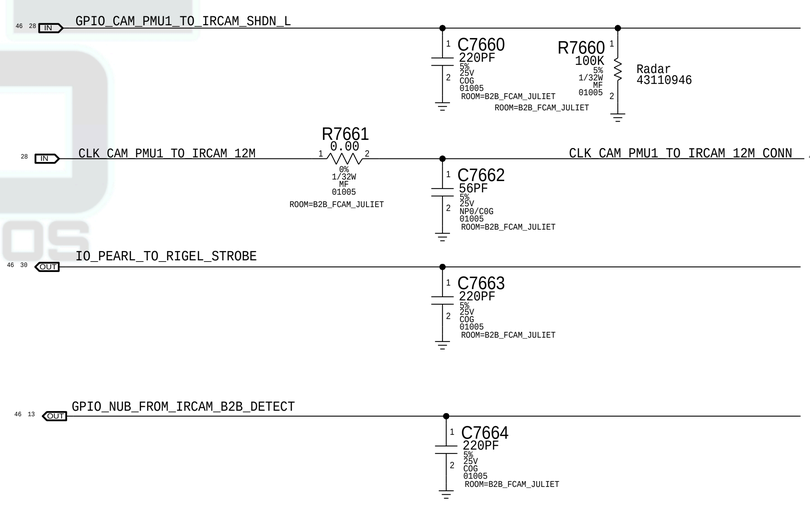
Rcpt: 516S00521 <-- This one on MLB
Plug: 516S00522



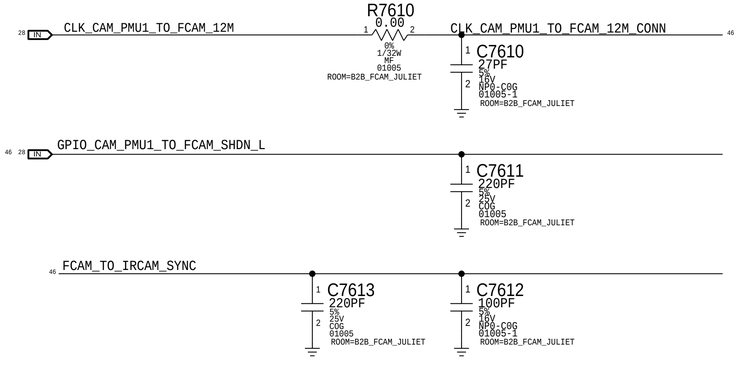
LPDP FILTERS



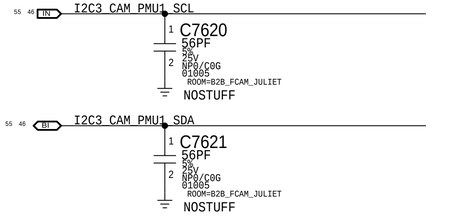
JULIET I/O



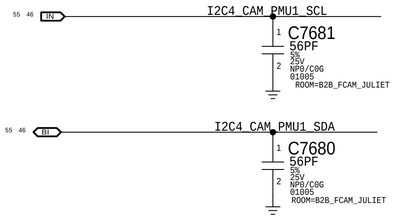
FCAM I/O



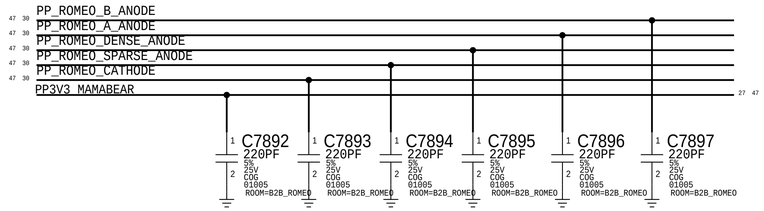
FCAM I2C



Juliet I2C

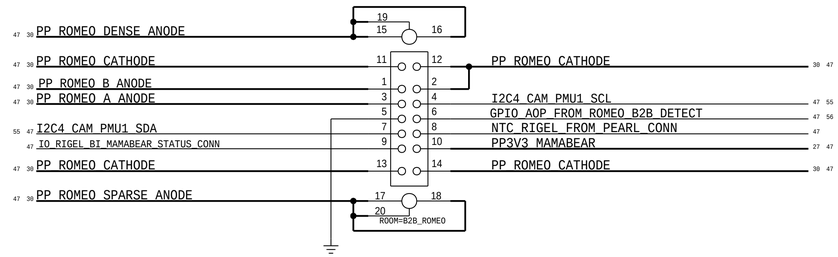


Romeo Power Filtering

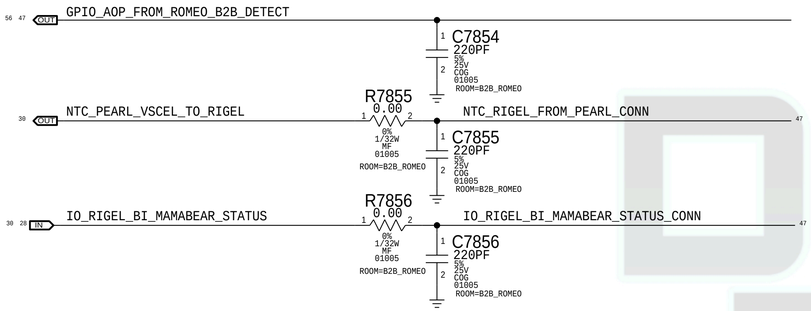


Romeo Connector

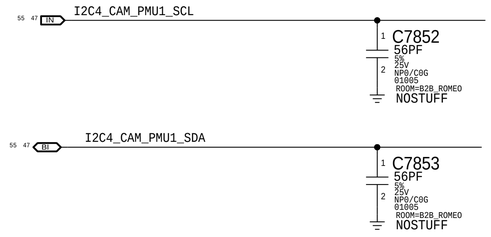
RCPT: 516S00453 <-- This one on MLB
PLUG: 516S00454



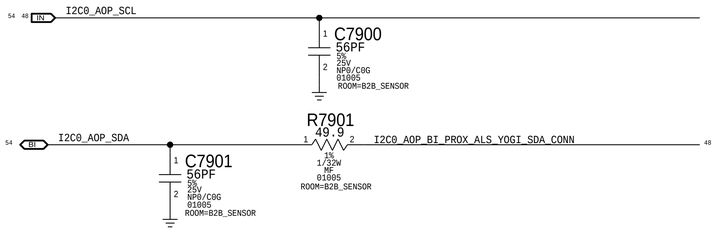
Romeo I/O



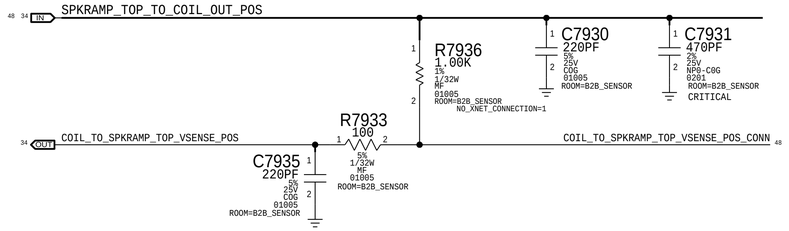
Romeo I2C

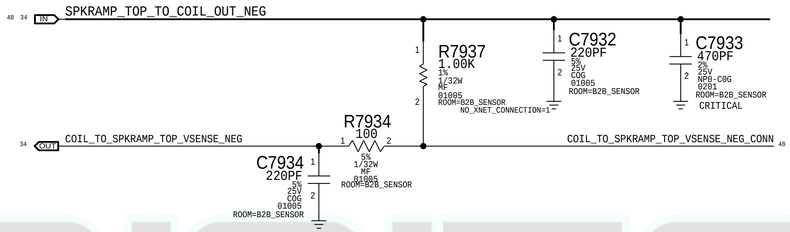


AOP I2C



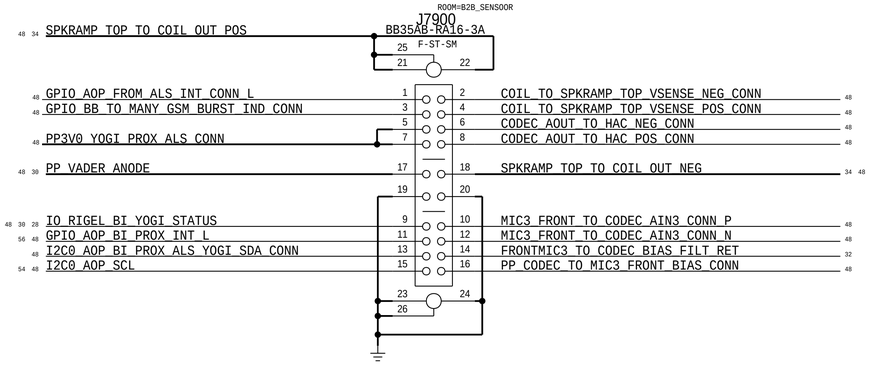
SPEAKER2



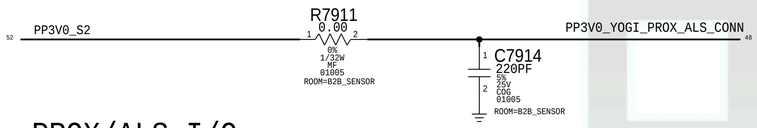


Vader + Sensor Connector

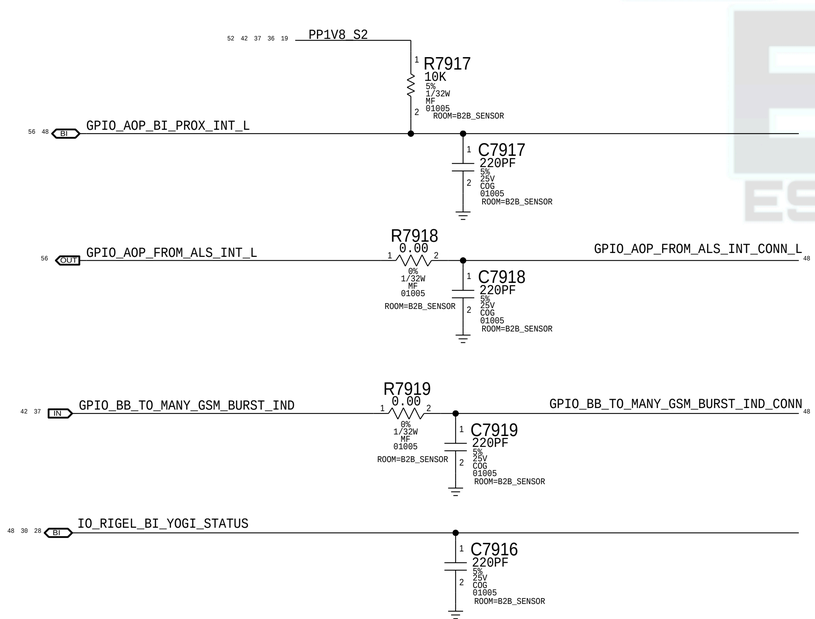
RCPT: 516S00449 <-- This one on MLB
PLUG: 516S00450



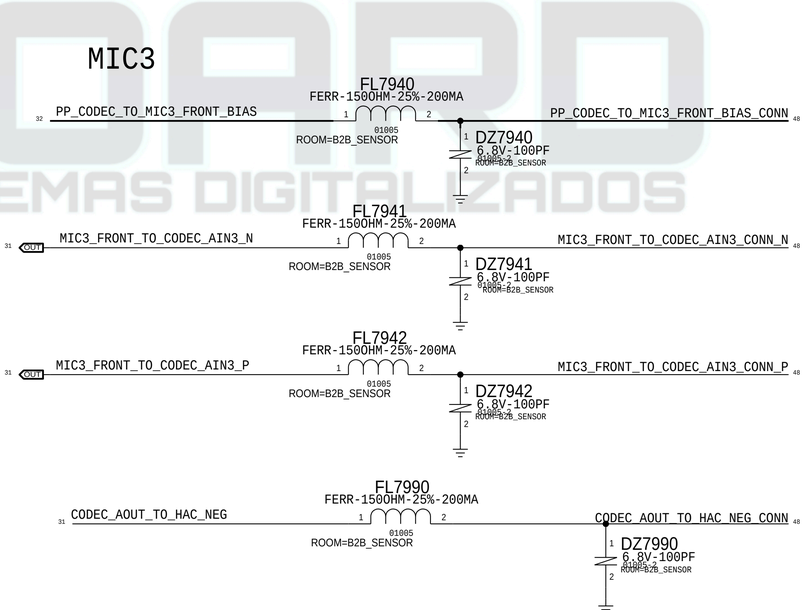
PROX & ALS POWER



PROX/ALS I/O



MIC3



DISPLAY CONNECTOR

RCPT: 516S00313 <-- This one on MLB
PLUG: 516S00314

J8000
AA26DK-S026VA1
F-ST-SM

49	PN5V7_DISPLAY_AVDDN_CONN	1 / 2	PP1V8_DISPLAY_DVDD_CONN	49
		3 / 4	PP5V7_DISPLAY_AVDDH_CONN	49
49	90_MIPI_AP_TO_DISPLAY_DATA0_CONN_P	5 / 6	PMU_TO_DISPLAY_PANICB_CONN	49
49	90_MIPI_AP_TO_DISPLAY_DATA0_CONN_N	7 / 8	DISPLAY_TEST	4
		9 / 10	IO_AP_FROM_DISPLAY_ALIVE_CONN	49
49	90_MIPI_AP_TO_DISPLAY_DATA1_CONN_P	11 / 12	GPIO_PMU_TO_DISPLAY_RESET_CONN_L	49
49	90_MIPI_AP_TO_DISPLAY_DATA1_CONN_N	13 / 14	CHESTNUT_FROM_DISPLAY_PWR_EN_CONN	49
		15 / 16	PP_DISPLAY_BL34_CAT1	37 49
49	90_MIPI_AP_TO_DISPLAY_CLK_CONN_P	17 / 18	PP_DISPLAY_BL34_ANODE	37 49
49	90_MIPI_AP_TO_DISPLAY_CLK_CONN_N	19 / 20	PP_DISPLAY_BL34_CAT2	37 49
		21 / 22	PP_DISPLAY_BL12_CAT1	37 49
49	90_MIPI_AP_TO_DISPLAY_DATA2_CONN_P	23 / 24	PP_DISPLAY_BL12_ANODE	37 49
49	90_MIPI_AP_TO_DISPLAY_DATA2_CONN_N	25 / 26	PP_DISPLAY_BL12_CAT2	37 49
		27 / 28		
		29 / 30		
		31 / 32		

DISPLAY POWER FILTERS

FL8000
240-OHM-25%-0.42A-0.31DCR
0201
ROOM=B2B_DISPLAY

36 PP5V7_DISPLAY_AVDDH — PP5V7_DISPLAY_AVDDH_CONN 49

- C8002 10UF 20% 16V X5R-CERM 0402-0.1MM ROOM=B2B_DISPLAY
- C8003 10UF 20% 16V X5R-CERM 0402-0.1MM ROOM=B2B_DISPLAY
- C8000 2.2UF 20% 10V X5R 0201 ROOM=B2B_DISPLAY
- C8001 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

L8001
FERR-150OHM-25%-200MA
01005
ROOM=B2B_DISPLAY

36 PN5V7_DISPLAY_AVDDN — PN5V7_DISPLAY_AVDDN_CONN 49

- C8010 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

L8000
FERR-1500HM-25%-200MA
01005
ROOM=B2B_DISPLAY

56 52 44 28 19 PP1V8_IO — PP1V8_DISPLAY_DVDD_CONN 49

- C8005 0.47UF 20% 6.3V X5R 01005-1 ROOM=B2B_DISPLAY
- C8006 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

DISPLAY MIPI CHOKES

L8054
350HM-0.05A-7GHZ-3OHM
NFP0R-SM
SYM_VER-1
ROOM=B2B_DISPLAY
CRITICAL

10 IN 90_MIPI_AP_TO_DISPLAY_CLK_P — 90_MIPI_AP_TO_DISPLAY_CLK_CONN_P 49
10 IN 90_MIPI_AP_TO_DISPLAY_CLK_N — 90_MIPI_AP_TO_DISPLAY_CLK_CONN_N 49

L8050
350HM-0.05A-7GHZ-3OHM
NFP0R-SM
SYM_VER-1
ROOM=B2B_DISPLAY
CRITICAL

10 BI 90_MIPI_AP_TO_DISPLAY_D0_P — 90_MIPI_AP_TO_DISPLAY_DATA0_CONN_P 49
10 BI 90_MIPI_AP_TO_DISPLAY_D0_N — 90_MIPI_AP_TO_DISPLAY_DATA0_CONN_N 49

L8051
350HM-0.05A-7GHZ-3OHM
NFP0R-SM
SYM_VER-1
ROOM=B2B_DISPLAY
CRITICAL

10 IN 90_MIPI_AP_TO_DISPLAY_D1_P — 90_MIPI_AP_TO_DISPLAY_DATA1_CONN_P 49
10 IN 90_MIPI_AP_TO_DISPLAY_D1_N — 90_MIPI_AP_TO_DISPLAY_DATA1_CONN_N 49

L8052
350HM-0.05A-7GHZ-3OHM
NFP0R-SM
SYM_VER-1
ROOM=B2B_DISPLAY
CRITICAL

10 IN 90_MIPI_AP_TO_DISPLAY_D2_P — 90_MIPI_AP_TO_DISPLAY_DATA2_CONN_P 49
10 90_MIPI_AP_TO_DISPLAY_D2_N — 90_MIPI_AP_TO_DISPLAY_DATA2_CONN_N 49

DISPLAY CONTROL SIGNAL FILTERS

36 22 OUT CHESTNUT_FROM_DISPLAY_PWR_EN — R8002 0.00 0% 1/32W MF 01005 ROOM=B2B_DISPLAY — CHESTNUT_FROM_DISPLAY_PWR_EN_CONN 49

- C8050 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

56 IN GPIO_PMU_TO_DISPLAY_RESET_L — R8003 0.00 0% 1/32W MF 01005 ROOM=B2B_DISPLAY — GPIO_PMU_TO_DISPLAY_RESET_CONN_L 49

- R8053 100K 5% 1/32W MF 01005 ROOM=B2B_DISPLAY
- C8052 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

56 IN GPIO_PMU_TO_DISPLAY_PANICB — R8054 10 5% 1/32W MF 01005 ROOM=B2B_DISPLAY — PMU_TO_DISPLAY_PANICB_CONN 49

- C8054 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

10 IN IO_AP_FROM_DISPLAY_ALIVE — R8057 0.00 0% 1/32W MF 01005 ROOM=B2B_DISPLAY — IO_AP_FROM_DISPLAY_ALIVE_CONN 49

- C8057 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DISPLAY

BACKLIGHT FILTERS

BL12

49 37 PP_DISPLAY_BL12_ANODE

- C8062 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY
- C8063 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

49 37 PP_DISPLAY_BL12_CAT1

- C8031 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

49 37 PP_DISPLAY_BL12_CAT2

- C8032 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

BL34

49 37 PP_DISPLAY_BL34_ANODE

- C8065 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY
- C8066 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

49 37 PP_DISPLAY_BL34_CAT1

- C8034 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

49 37 PP_DISPLAY_BL34_CAT2

- C8035 220PF 5% 25V C0G 01005 ROOM=B2B_DISPLAY

RCPT: 516S00473 <-- This one on MLB
PLUG: 516S00474

TOUCH B2B

J8100
BB35K-RA20-3A
F-ST-SM
ROOM=B2B_TOUCH

50	CLK_PMU_TO_TOUCH_32K_CONN	1	2	SPI1_AP_TO_TOUCH_SCLK_CONN	50
		3	4	SPI1_AP_TO_TOUCH_MOSI_CONN	50
50	GPIO_AOP_FROM_TOUCH_CTS_CONN	5	6	SPI1_AP_FROM_TOUCH_MISO_CONN	50
50	CLK_AP_TO_TOUCH_SCAN_CONN	7	8	SPI1_AP_TO_TOUCH_CS_CONN_L	50
50	GPIO_AOP_FROM_TOUCH_INT_CONN_L	9	10	UART1_AOP_FROM_TOUCH_RXD_CONN	50
50	IO_TOUCH_TO_MANY_SCAN_ACTIVE_CONN	11	12	I2C3_AP_SCL	50 53
50	GPIO_AP_TO_TOUCH_RESET_CONN_L	13	14	I2C3_AP_BI_TOUCH_SDA_CONN	50
50	I2C_CUMULUS_SDA_CONN	15	16		
50	I2C_CUMULUS_SCL_CONN	17	18	PP5V1_TOUCH_VDDH_CONN	50
50	UART1_AOP_TO_TOUCH_TXD_CONN	19	20	PP1V8_TOUCH_S2_CONN	50
		21	22		
		23	24		
		25	26		

TOUCH POWER

53 50 19 PP1V8_TOUCH_S2 — L8100 FERR-33OHM-25%-1.5A (0201, ROOM=B2B_TOUCH) — PP1V8_TOUCH_S2_CONN 50

- C8121 2.2UF 20% 6.3V X5R-CERM 0201 ROOM=B2B_TOUCH
- C8120 220PF 5% 25V C0G 01005 ROOM=B2B_TOUCH

36 PP5V1_TOUCH_VDDH — L8101 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — PP5V1_TOUCH_VDDH_CONN 50

- C8125 220PF 5% 25V C0G 01005 ROOM=B2B_TOUCH

CUMULUS I2C

I2C_CUMULUS_SCL_CONN 50 (CKPLUS_WAIVE=I2C_PULLUP)

- R8104 1.00K 5% 1/32W MF 01005 ROOM=B2B_TOUCH

I2C_CUMULUS_SDA_CONN 50 (CKPLUS_WAIVE=I2C_PULLUP)

- R8105 1.00K 5% 1/32W MF 01005 ROOM=B2B_TOUCH

TOUCH RESET

56 GPIO_AP_TO_TOUCH_RESET_L — L8108 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — GPIO_AP_TO_TOUCH_RESET_CONN_L 50

- C8178 220PF 5% 25V C0G 01005 ROOM=B2B_TOUCH

AOP/TOUCH INTERFACE

56 10 IN CLK_AP_TO_TOUCH_SCAN — L8102 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — CLK_AP_TO_TOUCH_SCAN_CONN 50

- C8160 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

50 OUT GPIO_AOP_FROM_TOUCH_CTS — L8103 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — GPIO_AOP_FROM_TOUCH_CTS_CONN 50

- C8162 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

42 28 23 22 OUT IO_TOUCH_TO_MANY_SCAN_ACTIVE — L8104 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — IO_TOUCH_TO_MANY_SCAN_ACTIVE_CONN 50

- C8164 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

56 OUT GPIO_AOP_FROM_TOUCH_INT_L — L8105 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — GPIO_AOP_FROM_TOUCH_INT_CONN_L 50

- C8166 220PF 5% 25V C0G 01005 ROOM=B2B_TOUCH

22 IN CLK_PMU_TO_TOUCH_32K — R8103 33.2 1% 1/32W MF 01005 ROOM=B2B_TOUCH — CLK_PMU_TO_TOUCH_32K_CONN 50

- C8168 100PF 5% 25V C0G-CERM 01005 ROOM=B2B_TOUCH

13 OUT UART1_AOP_FROM_TOUCH_RXD — L8110 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — UART1_AOP_FROM_TOUCH_RXD_CONN 50

- C8101 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

13 IN UART1_AOP_TO_TOUCH_TXD — L8111 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — UART1_AOP_TO_TOUCH_TXD_CONN 50

- C8102 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

AP/TOUCH INTERFACE

53 50 19 PP1V8_TOUCH_S2

- R8170 100K 5% 1/32W MF 01005

31 IN SPI1_AP_TO_TOUCH_CS_L — L8106 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — SPI1_AP_TO_TOUCH_CS_CONN_L 50

- C8170 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

31 IN SPI1_AP_TO_TOUCH_SCLK — R8172 0.00 0% 1/32W MF 01005 ROOM=B2B_TOUCH — SPI1_AP_TO_TOUCH_SCLK_CONN 50

- R8180 511K 1% 1/32W MF 01005 ROOM=B2B_TOUCH
- C8172 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

11 IN SPI1_AP_TO_TOUCH_MOSI — R8174 0.00 0% 1/32W MF 01005 ROOM=B2B_TOUCH — SPI1_AP_TO_TOUCH_MOSI_CONN 50

- R8181 511K 1% 1/32W MF 01005 ROOM=B2B_TOUCH
- C8174 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

11 OUT SPI1_AP_FROM_TOUCH_MISO — L8107 FERR-1500HM-25%-200MA (01005, ROOM=B2B_TOUCH) — SPI1_AP_FROM_TOUCH_MISO_CONN 50

- C8176 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

53 50 IN I2C3_AP_SCL

- C8155 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

53 BI I2C3_AP_SDA — R8156 0.00 0% 1/32W MF 01005 ROOM=B2B_TOUCH — I2C3_AP_BI_TOUCH_SDA_CONN 50

- C8156 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_TOUCH

ARC

ARC_TO_SOLENOID_OUT_POS
R8276 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C8271 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C8272 470PF 20% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
R8290 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARC_VSENSE_POS
C8275 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARC_VSENSE_POS_CONN

ARC_TO_SOLENOID_OUT_NEG
R8275 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C8270 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C8273 470PF 20% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
R8291 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARC_VSENSE_NEG
C8274 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
SOLENOID_TO_ARC_VSENSE_NEG_CONN

SOUTH SPEAKER

SPKRAMP_BOT_TO_COIL_OUT_POS
R8283 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C8283 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C8286 470PF 20% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
R8282 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_POS
C8282 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN

SPKRAMP_BOT_TO_COIL_OUT_NEG
R8281 1.00K 1% 1/32W MF 01005 ROOM=B2B_DOCK NO_XNET_CONNECTION=1
C8285 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C8287 470PF 20% 25V NP0-C0G 0201 ROOM=B2B_DOCK CRITICAL
R8280 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_NEG
C8280 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN

I2S

I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK
R8219 49.9 1% 1/32W MF 01005 ROOM=B2B_DOCK
C8219 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK_CONN

I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK
R8220 49.9 1% 1/32W MF 01005 ROOM=B2B_DOCK
C8220 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK_CONN

I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN
C8221 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
R8221 49.9 1% 1/32W MF 01005 ROOM=B2B_DOCK
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_R
R8222 0.00 1% 1/20W MF 0201 ROOM=B2B_DOCK
I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_CONN

Hydra

IO_E75_TO_HYDRA_CON_DETECT_L
R8210 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
C8210 27PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK
CON_DETECT_E75_TO_HYDRA_CONN_L

FL8211 10-OHM-1.1A 01005 ROOM=B2B_DOCK
PP_HYDRA_ACC1
C8211 100PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK
PP_HYDRA_ACC1_CONN

FL8213 22-OHM-25%-1800MA 0201 ROOM=B2B_DOCK
PP_HYDRA_ACC2
C8213 100PF 5% 16V NP0-C0G 01005-1 ROOM=B2B_DOCK
PP_HYDRA_ACC2_CONN

FL8200 FERR-1500HM-25%-200MA 01005 ROOM=B2B_DOCK
PP1V8_S2
C8200 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
PP1V8_SAK_K2_S2_CONN

Potassium Interrupt PU
PP1V8_S2
R8201 10K 5% 1/32W MF 01005 ROOM=B2B_DOCK
GPIO_AOP_FROM_K2_INT_L
C8233 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
R8233 0.00 0% 1/32W MF 01005 ROOM=B2B_DOCK
GPIO_K2_TO_AOP_INT_CONN_L

LOWER MIC1 + LOWER MIC4

FL8254 FERR-1500HM-25%-200MA 01005 ROOM=B2B_DOCK
PP_CODEC_TO_MIC1_LOWER_BIAS
C8254 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
PP_CODEC_TO_MIC1_LOWER_BIAS_CONN

MIC1_LOWER_TO_CODEC_AIN1_P
R8250 0.00 0% 1/32W MF 01005 ROOM=B2B_DOCK
C8250 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
MIC1_LOWER_TO_CODEC_AIN1_CONN_P

MIC1_LOWER_TO_CODEC_AIN1_N
R8252 0.00 0% 1/32W MF 01005 ROOM=B2B_DOCK
C8252 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
MIC1_LOWER_TO_CODEC_AIN1_CONN_N

FL8264 FERR-1500HM-25%-200MA 01005 ROOM=B2B_DOCK
PP_CODEC_TO_MIC4_LOWER_BIAS
C8264 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
PP_CODEC_TO_MIC4_LOWER_BIAS_CONN

MIC4_LOWER_TO_CODEC_AIN4_P
R8260 0.00 0% 1/32W MF 01005 ROOM=B2B_DOCK
C8260 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
MIC4_LOWER_TO_CODEC_AIN4_CONN_P

MIC4_LOWER_TO_CODEC_AIN4_N
R8262 0.00 0% 1/32W MF 01005 ROOM=B2B_DOCK
C8262 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
MIC4_LOWER_TO_CODEC_AIN4_CONN_N

DOCK FLEX CONNECTOR

RCPT: 516S00467 <-- This one on MLB
PLUG: 516S00468

PP_VBUS1_E75
C8290 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C8291 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C8292 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C8293 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
J8200 BB35AF-RA34-3A F-ST-SM
C8294 220PF 5% 25V C0G 01005 ROOM=B2B_DOCK
C8295 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C8296 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK
C8297 0.1UF 10% 25V X5R 0201 ROOM=B2B_DOCK

SPKRAMP_BOT_TO_COIL_OUT_NEG	35	36	SPKRAMP_BOT_TO_COIL_OUT_POS
COIL_TO_SPKRAMP_BOT_VSENSE_NEG_CONN	1	2	COIL_TO_SPKRAMP_BOT_VSENSE_POS_CONN
PP_CODEC_TO_MIC1_LOWER_BIAS_CONN	3	4	LOWERMIC1_TO_CODEC_BIAS_FILT_RET
MIC1_LOWER_TO_CODEC_AIN1_CONN_N	5	6	MIC1_LOWER_TO_CODEC_AIN1_CONN_P
	7	8	MIKEYBUS_REFERENCE
	9	10	CON_DETECT_E75_TO_HYDRA_CONN_L
90_HYDRA_DP2_CONN_P	11	12	
90_HYDRA_DP2_CONN_N	13	14	I2S1_AOP_AMPS_FROM_CODEC_ASP2_LRCLK_CONN
90_HYDRA_DP1_CONN_N	15	16	I2S1_AOP_AMPS_FROM_CODEC_ASP2_BCLK_CONN
90_HYDRA_DP1_CONN_P	17	18	I2S1_AOP_FROM_AMPS_CODEC_ASP2_DIN_CONN
	19	20	
GPIO_K2_TO_AOP_INT_CONN_L	21	22	I2C1_AOP_BI_SAK_K2_SDA_CONN
I2C1_AOP_SCL	23	24	PP1V8_SAK_K2_S2_CONN
PP_HYDRA_ACC2_CONN	25	26	PP_HYDRA_ACC1_CONN
	27	28	
MIC4_LOWER_TO_CODEC_AIN4_CONN_N	29	30	MIC4_LOWER_TO_CODEC_AIN4_CONN_P
PP_CODEC_TO_MIC4_LOWER_BIAS_CONN	31	32	LOWERMIC4_TO_CODEC_BIAS_FILT_RET
SOLENOID_TO_ARC_VSENSE_POS_CONN	33	34	SOLENOID_TO_ARC_VSENSE_NEG_CONN
ARC_TO_SOLENOID_OUT_POS	37	38	ARC_TO_SOLENOID_OUT_NEG
	41	42	
	44		

I2C

I2C1_AOP_SCL
C8231 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK
I2C1_AOP_SDA
R8232 100 5% 1/32W MF 01005 ROOM=B2B_DOCK
I2C1_AOP_BI_SAK_K2_SDA_CONN CKPLUS_WAIVE=I2C_PULLUP
C8232 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_DOCK

Medusa Compatibility

42 37 24 21 20 3	PP_VDD_MAIN	MAKE_BASE=TRUE	PP_VDD_MAIN 21
			PP_VDD_MAIN 23
			PP_VDD_MAIN 30 52
			PP_VDD_MAIN 27 52
			PP_VDD_MAIN 33 34 35 52
			PP_VDD_MAIN 38 39
			PP_VDD_MAIN 29
			PP_VDD_MAIN 36
			PP_VDD_MAIN 30 52
			PP_VDD_MAIN 27 52
			PP_VDD_MAIN 33 34 35 52
			PP_VDD_MAIN 42
			PP_VDD_MAIN 42
42 21 19	PP1V2_S4	MAKE_BASE=TRUE	PP1V2_S4 33
42 21	PP3V0_S2	MAKE_BASE=TRUE	PP3V0_S2 48
			PP3V0_S2 41
			PP3V0_S2 40
42 21	PP1V2_S2	MAKE_BASE=TRUE	PP1V2_S2 32 34
			PP1V2_S2 20
29 23 21	PP_VDD_BOOST	MAKE_BASE=TRUE	PP_VDD_BOOST 39
			PP_VDD_BOOST 30
			PP_VDD_BOOST 32
			PP_VDD_BOOST 27
19	PP_CPU_PCORE	MAKE_BASE=TRUE	PP_CPU_PCORE 14
20	PP_CPU_ECORE	MAKE_BASE=TRUE	PP_CPU_ECORE 14
19	PP_GPU	MAKE_BASE=TRUE	PP_GPU 14
19	PP_AVE_S1	MAKE_BASE=TRUE	PP_AVE_S1 16
19	PP_SRAM_S1	MAKE_BASE=TRUE	PP_SRAM_S1 14
19	PP_DISP_S1	MAKE_BASE=TRUE	PP_DISP_S1 16
19	PP_DCS_S1	MAKE_BASE=TRUE	PP_DCS_S1 16
20	PP0V6_VDDQL_S1	MAKE_BASE=TRUE	PP0V6_VDDQL_S1 7 16
19	PP_SOC_S1	MAKE_BASE=TRUE	PP_SOC_S1 14
21	PP0V7_VDD_LOW_S2	MAKE_BASE=TRUE	PP0V7_VDD_LOW_S2 16
21	PP3V3_USB	MAKE_BASE=TRUE	PP3V3_USB 16
19	PP1V1_S2	MAKE_BASE=TRUE	PP1V1_S2 21
			PP1V1_S2 16
21	PP1V2_SOC	MAKE_BASE=TRUE	PP1V2_SOC 15
			PP1V2_SOC 15
			PP1V2_SOC 8 15
21	PP1V8_ALWAYS	MAKE_BASE=TRUE	PP1V8_ALWAYS 24
48 42 37 36 19	PP1V8_S2	MAKE_BASE=TRUE	PP1V8_S2 16 26 51 54
			PP1V8_S2 16
			PP1V8_S2 40
			PP1V8_S2 32 34
			PP1V8_S2 41
			PP1V8_S2 22
			PP1V8_S2 42
56 49 44 28 19	PP1V8_IO	MAKE_BASE=TRUE	PP1V8_IO 16
			PP1V8_IO 11
			PP1V8_IO 30
			PP1V8_IO 16
			PP1V8_IO 16
			PP1V8_IO 27
			PP1V8_IO 18
			PP1V8_IO 6 8 38 53 55
21	PP0V8_SOC_FIXED_S1	MAKE_BASE=TRUE	PP0V8_SOC_FIXED_S1 15
			PP0V8_SOC_FIXED_S1 15
			PP0V8_SOC_FIXED_S1 15

AP I2C

AP I2C0

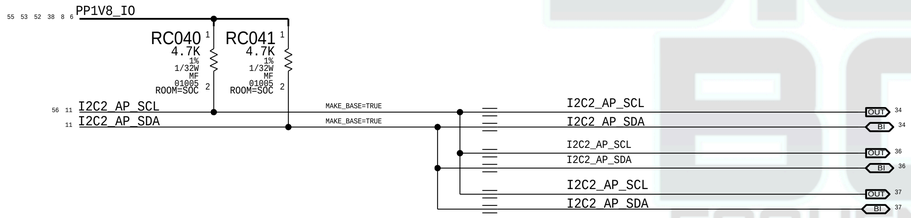
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C0	PP1V8_IO	1 MHz	Muon	0x62	1100 010X	0xC4, 0xC5	-	1 MHz	TOP MLB

AP I2C1

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C1	PP1V8_IO	100 kHz	MIC2	0x56	1010 110X	0xAC, 0xAD	-	1 MHz	Strobe Flex

MIC2 ON STROBE FLEX
STROBE FLEX B2B ON BOTTOM BOARD

AP I2C2

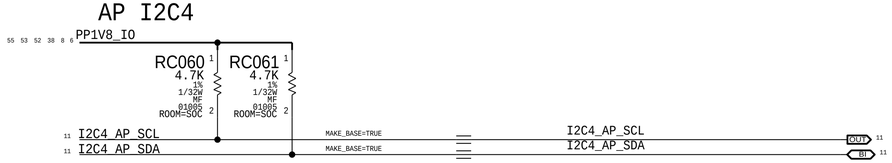


Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C2	PP1V8_IO	400 kHz	Top Speaker Amp	0x40	1000 000X	0x80, 0x81	-	1 MHz	Top MLB
			Chestnut	0x27	0100 111X	0x4E, 0x4F	-	400 kHz	Top MLB
			Muon	0x62	1100 010X	0xC4, 0xC5	-	1 MHz	Top MLB

AP I2C3

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AP I2C3	PP1V8_IO	400 kHz	Touch EEPROM	0x51	1010 001X	0xA2, 0xA3	-	1 MHz	Touch Flex
			Roswell	0X10	0010 000X	0X20, 0X21	-	400 kHz	Touch Flex

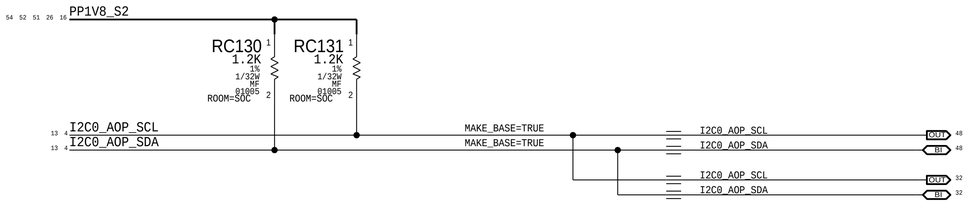
AP I2C4



Bus Name	Bus Voltage	Bus Speed	Device	Max Speed	Location
AP I2C4	PP1V8_IO	400 kHz	LYNX	1 MHz	Top MLB

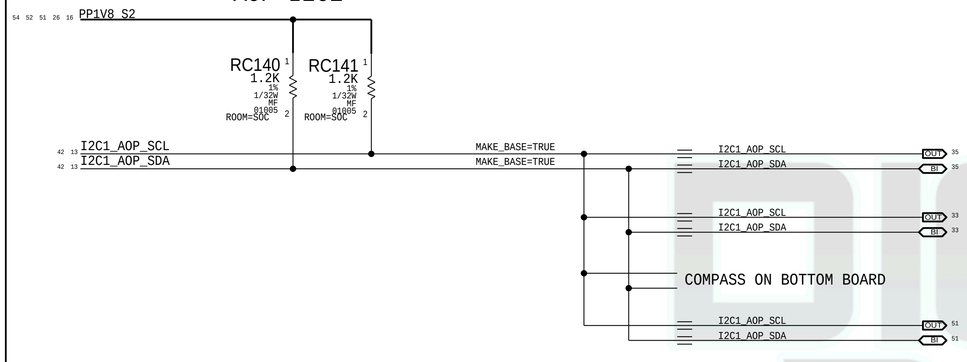
AOP/SMC I2C

AOP I2C0



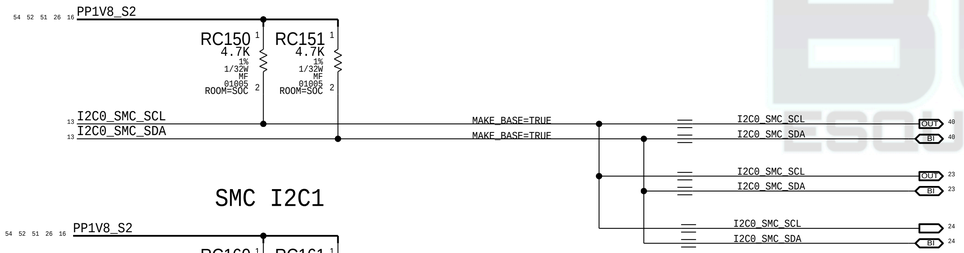
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AOP I2C0	PP1V8_S2	750 kHz	Doppler	0x58	1011 000X	0xB0, 0xB1	-	1 MHz	Sensor Flex
			Foxhound	0x29	0101 001X	0x52, 0x53	-	1 MHz	Sensor Flex
			Yogi	0x33	0110 011X	0x66, 0x67	-	1 MHz	Sensor Flex
			Brighton	0x4A	1001 010X	0x94, 0x95	-	1 MHz	Top MLB

AOP I2C1



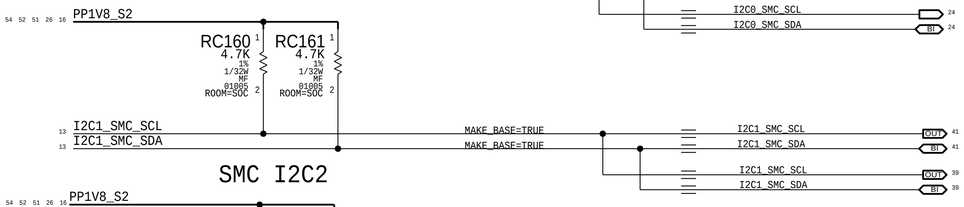
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
AOP I2C1	PP1V8_S2	400 kHz	Arc Speaker Amp	0x42	1000 010X	0x84, 0x85	-	1 MHz	Top MLB
			Bot Speaker Amp	0x40	1000 000X	0x80, 0x81	-	1 MHz	Top MLB
			K2	0x76	1110 110X	0xEC, 0xED	-	1 MHz	Dock Flex
			Sakonnet	0x08	0001 000X	0x10, 0x11	-	1 MHz	Arc Flex
			Moly	0x0E	0001 110X	0x1C, 0x1D	-	1 MHz	BTN Combine Flex
			Arc EEPROM	0x50	1010 000X	0xA0, 0xA1	-	1 MHz	Arc Flex

SMC I2C0



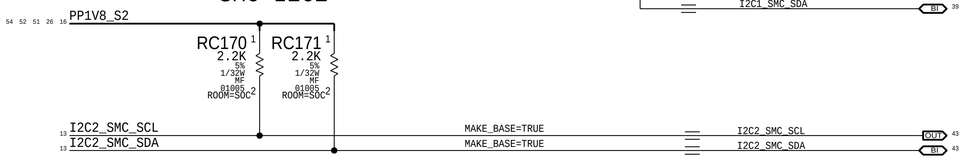
Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
SMC I2C0	PP1V8_S2	400 kHz	CCG2	0x12	0010 010X	0x24, 0x25	-	1 MHz	Top Board
			Boost	0x75	1110 101X	0xEA, 0xEB	-	1 MHz	Top Board
			Yangtze	0x71	1110 001X	0xE2, 0xE3	-	400 KHz	Top Board

SMC I2C1

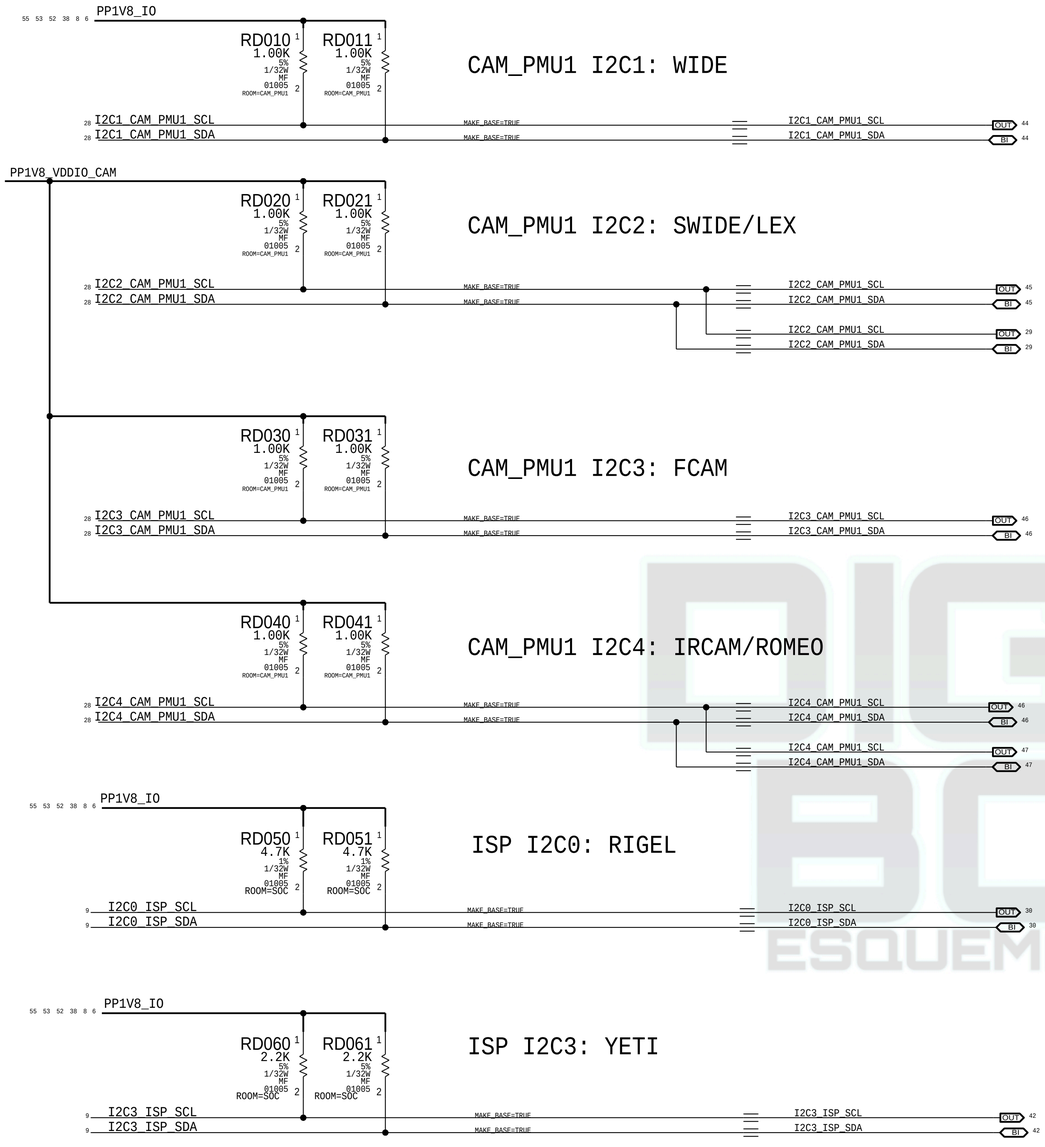


Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
SMC I2C1	PP1V8_S2	400 kHz	Hydra	0x1A	0011 010X	0x34, 0x35	-	400 KHz	Top Board
			Gecko	0x52	1010 010X	0xA4, 0xA5	-	400 KHz	Top Board

SMC I2C2



Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Location
SMC i2c2	PP1V8_S2	400 kHz	Veridian	0X0B	BMU Flex



CAM_PMU1 I2C1: WIDE

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
I2C1	PP1V8_IO	1 MHz	Toronto	0X10	0010 000X	0x20, 0x21	-	1 MHz	Wide Cam
			Raman	0X3C	0111 100X	0x78, 0x79	-	1 MHz	Wide Cam

CAM_PMU1 I2C2: SWIDE/LEX

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
I2C2	PP1V8_IO_CAM	1 MHz	Manitoba	0x20	0100 000X	0x40, 0x41	-	1 MHz	SWIDE Cam
			Lex	0X75	1110 101X	0xEA, 0xEB	-	1 MHz	MLB_TOP

CAM_PMU1 I2C3: FCAM

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
I2C3	PP1V8_IO_CAM	1 MHz	Maryland	0x10	0010 000X	0x20, 0x21	-	1 MHz	Front Cam

CAM_PMU1 I2C4: IRCAM/ROMEO

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
I2C4	PP1V8_IO_CAM	1 MHz	Juliet	0x18	0011 000X	0x30, 0x31	-	1 MHz	Top Board
			Romeo	0x66	1100 110X	0xCC, 0xCD		1 MHz	Top Board

ISP I2C0: RIGEL

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C0	PP1V8_IO	1 MHz	Rigel	0x55	1010 101X	0xAA, 0xAB	-	1 MHz	Top Board

ISP I2C3: YETI

Bus Name	Bus Voltage	Bus Speed	Device	7-Bit Addr.	Binary	8-Bit Addr.	Min Speed	Max Speed	Location
ISP I2C3	PP1V8_IO	1 MHz	Yeti	0x65	1100 101X	0xCA, 0xCB	-	1 MHz	Bot Board

AOP

SCM_SPI TRIGGER & CS >

SCM_I2CM0 TRIGGER --->

SCM_I2CM1 TRIGGER >

AOP_FUNC_0	13	GPIO_AOP_FROM_IMU_DATARDY	GPIO_AOP_FROM_IMU_DATARDY	IN	4 26 42
AOP_FUNC_1	13	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	GPIO_AOP_TO_R1_COREDUMP_TRIGGER	OUT	42
AOP_FUNC_2	13	GPIO_AOP_TO_CODEC_CLP_EN	GPIO_AOP_TO_CODEC_CLP_EN	IN	32
AOP_FUNC_3	13	GPIO_AOP_TO_R1_SPI_CS_L	GPIO_AOP_TO_R1_SPI_CS_L	IN	42
AOP_FUNC_4	13	GPIO_AOP_FROM_R1_INT	GPIO_AOP_FROM_R1_INT	IN	42
AOP_FUNC_5	13	GPIO_AOP_TO_CODEC_RESET_L	GPIO_AOP_TO_CODEC_RESET_L	OUT	32
AOP_FUNC_6	13	GPIO_AOP_FROM_NFC_HOST_WAKE	GPIO_AOP_FROM_NFC_HOST_WAKE	OUT	42
AOP_FUNC_7	13	GPIO_AOP_FROM_SPKAMP_BOT_ARC_INT_L	GPIO_AOP_FROM_SPKAMP_BOT_ARC_INT_L	OUT	33 35
AOP_FUNC_8	13	GPIO_AOP_TO_WLAN_CONTEXT_A	GPIO_AOP_TO_WLAN_CONTEXT_A	OUT	42
AOP_FUNC_9	13	GPIO_AOP_TO_IMU_SPI_CS_L	GPIO_AOP_TO_IMU_SPI_CS_L	OUT	26 42
AOP_FUNC_10	13	GPIO_AOP_TO_R1_TIME_SYNC	GPIO_AOP_TO_R1_TIME_SYNC	IN	42
AOP_FUNC_11	13	NC_AOP_GPIO11	NC_AOP_GPIO11		
AOP_FUNC_12	13	GPIO_AOP_FROM_ROMEO_B2B_DETECT	GPIO_AOP_FROM_ROMEO_B2B_DETECT	IN	47
AOP_FUNC_13	13	CLK_AP_TO_TOUCH_SCAN	CLK_AP_TO_TOUCH_SCAN		10 50
AOP_FUNC_14	13	NC_AOP_GPIO14	NC_AOP_GPIO14		
AOP_FUNC_15	13	GPIO_AOP_BI_PROX_INT_L	GPIO_AOP_BI_PROX_INT_L	IN	48
AOP_FUNC_16	13	GPIO_AOP_FROM_ALS_INT_L	GPIO_AOP_FROM_ALS_INT_L	IN	48
AOP_FUNC_17	13	GPIO_AOP_FROM_K2_INT_L	GPIO_AOP_FROM_K2_INT_L	IN	51
AOP_FUNC_18	13	GPIO_AOP_FROM_COMPASS_INT	GPIO_AOP_FROM_COMPASS_INT	IN	4 42
AOP_FUNC_19	13	NC_AOP_GPIO19	NC_AOP_GPIO19		
AOP_FUNC_20	13	GPIO_AOP_FROM_TOUCH_CTS	GPIO_AOP_FROM_TOUCH_CTS	IN	50
AOP_FUNC_21	13	GPIO_AOP_FROM_TOUCH_INT_L	GPIO_AOP_FROM_TOUCH_INT_L	IN	50
AOP_FUNC_22	13	GPIO_AOP_TO_WLAN_CONTEXT_B	GPIO_AOP_TO_WLAN_CONTEXT_B	OUT	42

PMU

HOLD Bit: Held Through 1 Reset

IRQ

HOLD Bit: Held Through 1 Reset

HOLD Bit: Held Through 1 Reset

HOLD Bit: Held Through 1 Reset

Sequenced GPIOs

GPIO_1	22	GPIO_PMU_TO_CCG2_RESET_L	GPIO_PMU_TO_CCG2_RESET_L	OUT	49
GPIO_2	22	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	GPIO_PMU_TO_NAND_LOW_BATT_BOOT_L	OUT	18
GPIO_3	22	SWD_NUB_BI_PMU_SWDIO	SWD_NUB_BI_PMU_SWDIO	OUT	4 13
GPIO_4	22	NC_PMU_GPIO_4	NC_PMU_GPIO_4		
GPIO_5	22	GPIO_PMU_NFC_TO_ARC_TRIG	GPIO_PMU_NFC_TO_ARC_TRIG	OUT	35 42
GPIO_6	22	GPIO_PMU_NFC_TO_ARC_RESET_L	GPIO_PMU_NFC_TO_ARC_RESET_L	OUT	35 42
GPIO_7	22	GPIO_PMU_TO_BBPMU_RESET_L	GPIO_PMU_TO_BBPMU_RESET_L	OUT	42
GPIO_8	22	NC_PMU_GPIO8	NC_PMU_GPIO8		
GPIO_9	22	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L	GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L	OUT	42
GPIO_10	22	NC_PMU_GPIO10	NC_PMU_GPIO10		
GPIO_11	22	NC_PMU_GPIO11	NC_PMU_GPIO11		
GPIO_12	22	GPIO_PMU_FROM_CODEC_WAKE_L	GPIO_PMU_FROM_CODEC_WAKE_L	IN	32
GPIO_13	22	GPIO_PMU_FROM_YANGTZE_INT_L	GPIO_PMU_FROM_YANGTZE_INT_L	OUT	24
GPIO_14	22	GPIO_PMU_TO_R1_RESET_L	GPIO_PMU_TO_R1_RESET_L	OUT	42
GPIO_15	22	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	GPIO_PMU_TO_AMUX_PMU_SUPER_TP	OUT	22
GPIO_16	22	GPIO_PMU_FROM_WLAN_HOST_WAKE	GPIO_PMU_FROM_WLAN_HOST_WAKE	OUT	42
GPIO_17	22	GPIO_PMU_TO_WLAN_REG_ON	GPIO_PMU_TO_WLAN_REG_ON	OUT	42
GPIO_18	22	GPIO_PMU_TO_WLAN_R1_32K_CLK	GPIO_PMU_TO_WLAN_R1_32K_CLK	OUT	22 42
GPIO_19	22	GPIO_PMU_TO_SPKAMP_BOT_RESET_L	GPIO_PMU_TO_SPKAMP_BOT_RESET_L	OUT	33
GPIO_20	22	GPIO_PMU_TO_NFC_EN	GPIO_PMU_TO_NFC_EN	OUT	42
GPIO_21	22	GPIO_PMU_TO_BOOST_EN	GPIO_PMU_TO_BOOST_EN	OUT	23
GPIO_22	22	I2C2_AP_SCL	I2C2_AP_SCL	IN	11 53
GPIO_23	22	GPIO_PMU_TO_DISPLAY_RESET_L	GPIO_PMU_TO_DISPLAY_RESET_L	OUT	49
GPIO_24	22	GPIO_PMU_TO_DISPLAY_PANICB	GPIO_PMU_TO_DISPLAY_PANICB	OUT	49
GPIO_25	22	GPIO_PMU_TO_DOTARA_EN_EXT_1V8	GPIO_PMU_TO_DOTARA_EN_EXT_1V8	OUT	42

SOC

1.2V

GPIO_AP_FROM_WLAN_TIME_SYNC_1V2

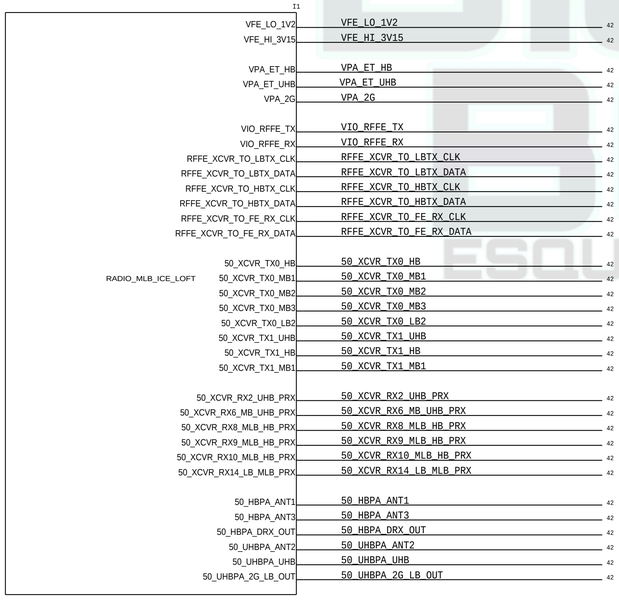
GPIO_AP_TO_BB_COREDUMP_1V2

GPIO_AP_FROM_BB_RESET_DETECT_1V2_L

GPIO_AP_FROM_SPKRAMP_TOP_INT_1V2_L

GPIO_0	12	GPIO_AP_CANARY2_1V2	GPIO_AP_CANARY2_1V2	IN	42
GPIO_1	12	NC_AP_GPIO1	NC_AP_GPIO1		
GPIO_2	12	NC_AP_GPIO2	NC_AP_GPIO2		
GPIO_3	12	GPIO_AP_FROM_WLAN_TIME_SYNC_1V2	GPIO_AP_FROM_WLAN_TIME_SYNC_1V2	IN	42
GPIO_4	12	GPIO_AP_TO_BB_COREDUMP_1V2	GPIO_AP_TO_BB_COREDUMP_1V2	IN	42
GPIO_5	12	GPIO_AP_FROM_BB_RESET_DETECT_1V2_L	GPIO_AP_FROM_BB_RESET_DETECT_1V2_L		42
GPIO_6	12	GPIO_AP_FROM_SPKRAMP_TOP_INT_1V2_L	GPIO_AP_FROM_SPKRAMP_TOP_INT_1V2_L	IN	34
GPIO_7	12	NC_AP_GPIO7	NC_AP_GPIO7		
GPIO_8	12	NC_AP_GPIO8	NC_AP_GPIO8		
GPIO_9	12	GPIO_BOARD_REV3	GPIO_BOARD_REV3	IN	6
GPIO_10	12	GPIO_BOARD_REV2	GPIO_BOARD_REV2	IN	6
GPIO_11	12	GPIO_BOARD_REV1	GPIO_BOARD_REV1	IN	6
GPIO_12	12	GPIO_BOARD_REV0	GPIO_BOARD_REV0	IN	6
GPIO_13	12	NC_AP_GPIO13	NC_AP_GPIO13		
GPIO_14	12	NC_AP_GPIO14	NC_AP_GPIO14		
GPIO_15	12	GPIO_AP_BI_CCG2_SWDIO	GPIO_AP_BI_CCG2_SWDIO	BI	4 40
GPIO_16	12	NC_AP_GPIO16	NC_AP_GPIO16		
GPIO_17	12	NC_AP_GPIO17	NC_AP_GPIO17		
GPIO_18	12	NC_AP_GPIO18	NC_AP_GPIO18		
GPIO_19	12	PP1V8_IO	PP1V8_IO		19 28 44 49 52
GPIO_20	12	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	GPIO_AP_TO_SPKRAMP_TOP_RESET_L	OUT	34
GPIO_21	12	GPIO_AP_CANARY1	GPIO_AP_CANARY1	OUT	42
GPIO_22	12	GPIO_AP_TO_NFC_DEV_WAKE	GPIO_AP_TO_NFC_DEV_WAKE	OUT	42
GPIO_23	12	NC_AP_GPIO23	NC_AP_GPIO23		
GPIO_24	12	GPIO_AP_FROM_CODEC_INT_L	GPIO_AP_FROM_CODEC_INT_L	IN	32
GPIO_25	12	GPIO_AP_FROM_BT_AUDIO_SYNC	GPIO_AP_FROM_BT_AUDIO_SYNC	IN	42
GPIO_26	12	NC_AP_GPIO26	NC_AP_GPIO26		
GPIO_27	12	NC_AP_GPIO27	NC_AP_GPIO27		
GPIO_28	12	GPIO_AP_TO_AMUX_PMU_SYNC	GPIO_AP_TO_AMUX_PMU_SYNC	OUT	22
GPIO_29	12	GPIO_AP_TO_TOUCH_RESET_L	GPIO_AP_TO_TOUCH_RESET_L	OUT	50
GPIO_30	12	NC_AP_GPIO30	NC_AP_GPIO30		
GPIO_31	12	GPIO_AP_TO_CCG2_SWCLK	GPIO_AP_TO_CCG2_SWCLK	BI	4 40

AP_GPIO19 IS PMU ID: AVUS=1, WHITNEY=NC



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN MHZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0017191502	ENGINEERING RELEASED	2019-04-14

ICE19.0 RADIO_MLB_LOFT

LAST_MODIFICATION=Sun Apr 14 18:20:31 2019

PAGE	CSA	CONTENTS	SYNC	DATE
58	1	SCH,RADIO_MLB_ICE_LOFT		
59	2	HB SPAD		04/06/2018
60	3	UHB MLB SPAD		04/06/2018

60 59 57 VFE_LO_1V2
60 59 57 IO VFE_HI_3V15

59 57 IO VPA_ET_HB
60 57 IO VPA_ET_UHB
60 57 IO VPA_2G

60 59 57 IO VIO_RFFE_TX
60 59 57 IO VIO_RFFE_RX
60 57 IO RFFE_XCVR_TO_LBTX_CLK
60 57 IO RFFE_XCVR_TO_LBTX_DATA
60 59 57 IO RFFE_XCVR_TO_HBTX_CLK
60 59 57 IO RFFE_XCVR_TO_HBTX_DATA
60 59 57 IO RFFE_XCVR_TO_FE_RX_CLK
60 59 57 IO RFFE_XCVR_TO_FE_RX_DATA

59 57 IO 50_XCVR_TX0_HB
60 57 IO 50_XCVR_TX0_MB1
60 57 IO 50_XCVR_TX0_MB2
59 57 IO 50_XCVR_TX0_MB3
60 57 IO 50_XCVR_TX0_LB2
60 57 IO 50_XCVR_TX1_UHB
59 57 IO 50_XCVR_TX1_HB
59 57 IO 50_XCVR_TX1_MB1

60 57 IO 50_XCVR_RX2_UHB_PRX
59 57 IO 50_XCVR_RX6_MB_UHB_PRX
59 57 IO 50_XCVR_RX8_MLB_HB_PRX
59 57 IO 50_XCVR_RX9_MLB_HB_PRX
59 57 IO 50_XCVR_RX10_MLB_HB_PRX
60 57 IO 50_XCVR_RX14_LB_MLB_PRX

59 57 IO 50_HBPA_ANT1
59 57 IO 50_HBPA_ANT3
59 57 IO 50_HBPA_DRX_OUT
60 57 IO 50_UHBPA_ANT2
60 57 IO 50_UHBPA_UHB
60 57 IO 50_UHBPA_2G_LB_OUT

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_WIDE	50_WIDE	A_DIELECTRIC_4XV_50_WIDE_SE
50_WIDE	50_THIN	A_DIELECTRIC_4XD_50_WIDE_SE
50_THIN	50_THIN	A_DIELECTRIC_4XD_50_THIN_SE
50_WIDE_L1_THIN	50_WIDE	A_DIELECTRIC_4XV_50_WIDE_SE
50_WIDE_L1_THIN	50_THIN	A_DIELECTRIC_4XD_50_WIDE_L1_THIN_SE
RF_SHIELD	GND	DEFAULT
RF_SHIELD	RF_SHIELD	A_DIELECTRIC_2XD
RFFE_SHIELD	GND	DEFAULT
RFFE_SHIELD	RFFE_SHIELD	DEFAULT

HB SPAD

VPA_ET_HB
C1400_K 12PF ±0.1PF 16V NP0/C0G 01005 RADIO_HB_PAD
C1430_K 5.6PF ±0.1PF 16V NP0/C0G 01005 RADIO_HB_PAD
VFE_HI_3V15
VIO_RFFE_TX
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
C1404_K 10PF ±0.1PF 16V NP0/C0G 01005 RADIO_HB_PAD
C1405_K 10PF ±0.1PF 16V NP0/C0G 01005 NOSTUFF RADIO_HB_PAD
C1406_K 10PF ±0.1PF 16V NP0/C0G 01005 NOSTUFF RADIO_HB_PAD
C1402_K 0.47UF 20% 6.3V X5R 01005-1
VIO_RFFE_RX
RFFE_XCVR_TO_FE_RX_CLK
RFFE_XCVR_TO_FE_RX_DATA
C1407_K 10PF ±0.1PF 16V NP0/C0G 01005 RADIO_HB_PAD
C1408_K 10PF ±0.1PF 16V NP0/C0G 01005 NOSTUFF RADIO_HB_PAD
C1409_K 10PF ±0.1PF 16V NP0/C0G 01005 NOSTUFF RADIO_HB_PAD
VFE_LO_1V2
C1401_K 1000PF 10% 6.3V X5R-CERM 01005 RADIO_HB_PAD

H1 SDATA_RX
G1 SCLK_RX
F1 VIO_RX
N18 SDATA_TX
N19 SCLK_TX
M18 VIO_TX
M19 VBATT
P17 VCC1
P18 VCC2
D1 VDD_LNA

USID RX=0X0E
USID TX=0X02

50_XCVR_TX0_MB3 → P13 TX_MB_IN1
50_XCVR_TX1_MB1 → O14 TX_MB_IN2
50_XCVR_TX0_HB → P15 TX_HB_IN1
50_XCVR_TX1_HB → P14 TX_HB_IN2
50_UHBPA_MLB_OUT → B15 MLB_IN
50_UHBPA_2G_HB_OUT → B17 2G_IN
50_XCVR_RX6_MB_UHB_PRX ← Q4 PRX_OUT1
50_XCVR_RX8_MLB_HB_PRX ← Q8 PRX_OUT2
50_XCVR_RX9_MLB_HB_PRX ← Q2 PRX_OUT3
50_XCVR_RX10_MLB_HB_PRX ← Q6 PRX_OUT4

PA_HB_K
AFEM-8100-AP1
DSBGA
SYM 1 OF 2

DRX_OUT B11 50_HBPA_DRX_OUT_M
R1402_K 0.00 5% 1/20W MF 0201 RADIO_HB_PAD
C1415_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
C1431_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
50_HBPA_DRX_OUT → TO HB DSM

ANT1 B19 50_HBPA_ANT1_M
R1404_K 0.00 5% 1/20W MF 0201 RADIO_HB_PAD
C1423_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
C1414_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
50_HBPA_ANT1 → TO LAT TRIPLEXER4

ANT2 D19 NC

ANT3 F19 50_HBPA_ANT3_M
R1410_K 0.00 5% 1/20W MF 0201 RADIO_HB_PAD
C1411_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
C1420_K 0.5PF ±0.05PF 25V C0G-CERM 0201 RADIO_HB_PAD NOSTUFF
50_HBPA_ANT3 → TO UAT COUPLER

MIMO_RX_OUT B13 NC

PA_HB_K
AFEM-8100-AP1
DSBGA
SYM 2 OF 2

A1	GND	GND	G19		
A2	GND	GND	G20		
A3	GND	GND	H8		
A4	GND	GND	H9		
A5	GND	GND	H10		
A6	GND	GND	H11		
A7	GND	GND	H12		
A8	GND	GND	H13		
A9	GND	GND	H14		
A10	GND	GND	H15		
A11	GND	GND	H16		
A12	GND	GND	H17		
A13	GND	GND	H18		
A14	GND	GND	H19		
A15	GND	GND	H20		
A16	GND	GND	J1		
A17	GND	GND	J8		
A18	GND	GND	J9		
A19	GND	GND	J10		
A20	GND	GND	J11		
B1	GND	GND	J12		
B2	GND	GND	J13		
B3	GND	GND	J14		
B4	GND	GND	J15		
B5	GND	GND	J16		
B6	GND	GND	J17		
B7	GND	GND	J18		
B8	GND	GND	J19		
B9	GND	GND	J20		
B10	GND	GND	K1		
B12	GND	GND	K8		
B14	GND	GND	K9		
B16	GND	GND	K10		
B18	GND	GND	K11		
B20	GND	GND	K12		
C1	GND	GND	K20		
C2	GND	GND	L1		
C3	GND	GND	L8		
C4	GND	GND	L9		
C5	GND	GND	L10		
C6	GND	GND	L11		
C7	GND	GND	L12		
C8	GND	GND	L20		
C9	GND	GND	M1		
C10	GND	GND	M8		
C11	GND	GND	M9		
C19	GND	GND	M10		
C20	GND	GND	M11		
D2	GND	GND	M12		
D3	GND	GND	M20		
D4	GND	GND	N1		
D5	GND	GND	N8		
D6	GND	GND	N9		
D7	GND	GND	N10		
D8	GND	GND	N11		
D9	GND	GND	N12		
D10	GND	GND	N20		
D11	GND	GND	O1		
D20	GND	GND	O8		
E1	GND	GND	O9		
E2	GND	GND	O10		
E3	GND	GND	O11		
E4	GND	GND	O12		
E5	GND	GND	O13		
E6	GND	GND	O15		
E7	GND	GND	O16		
E8	GND	GND	O19		
E9	GND	GND	O20		
E10	GND	GND	P1		
E11	GND	GND	P8		
E19	GND	GND	P9		
E20	GND	GND	P10		
		GND	P11		
		GND	P12		
		GND	P16		
F5	GND	GND	P19		
F6	GND	GND	P20		
F7	GND	GND	Q1		
F8	GND	GND	Q3		
F9	GND	GND	Q5		
F10	GND	GND	Q7		
F11	GND	GND	Q9		
F20	GND	GND	Q10		
G8	GND	GND	Q11		
G9	GND	GND	Q12		
G10	GND	GND	Q13		
G11	GND	GND	Q14		
G12	GND	GND	Q15		
G13	GND	GND	Q16		
G14	GND	GND	Q17		
G15	GND	GND	Q18		
G16	GND	GND	Q19		
G17	GND	GND	Q20		
G18	GND				

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SCOPE P/S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RFFE_SHIELD	S	A_DIELECTRIC_2X	*RFFE*, VIO_RFFE*	Y

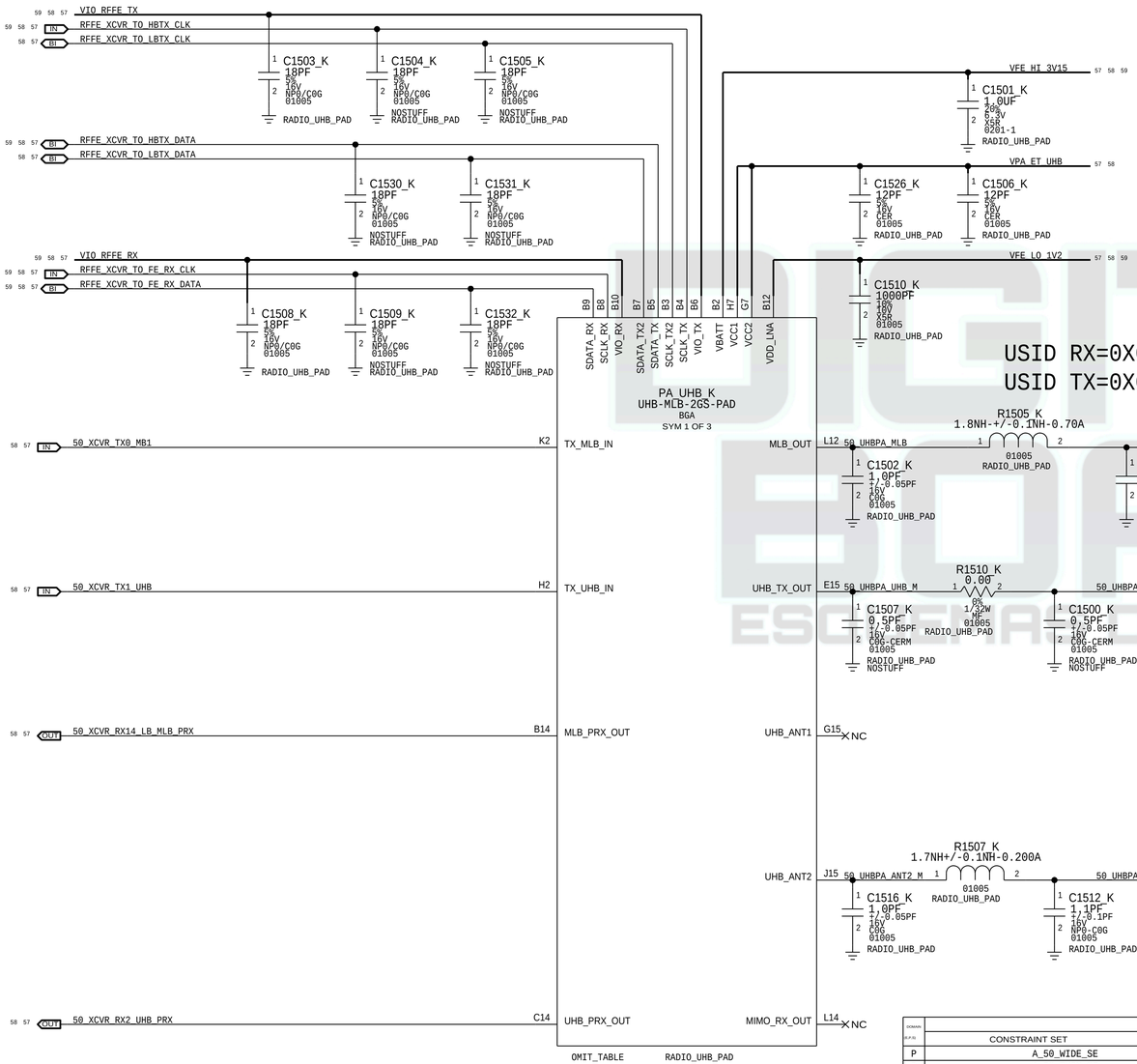
DOMAIN P,P,S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	VIO_RFFE*, VFE_LO_1V2
P	PWR_200UM	VFE_HI_3V15
P	PWR_SHAPE	VPA_ET_HB, VPA_ET_UHB, VPA_2G

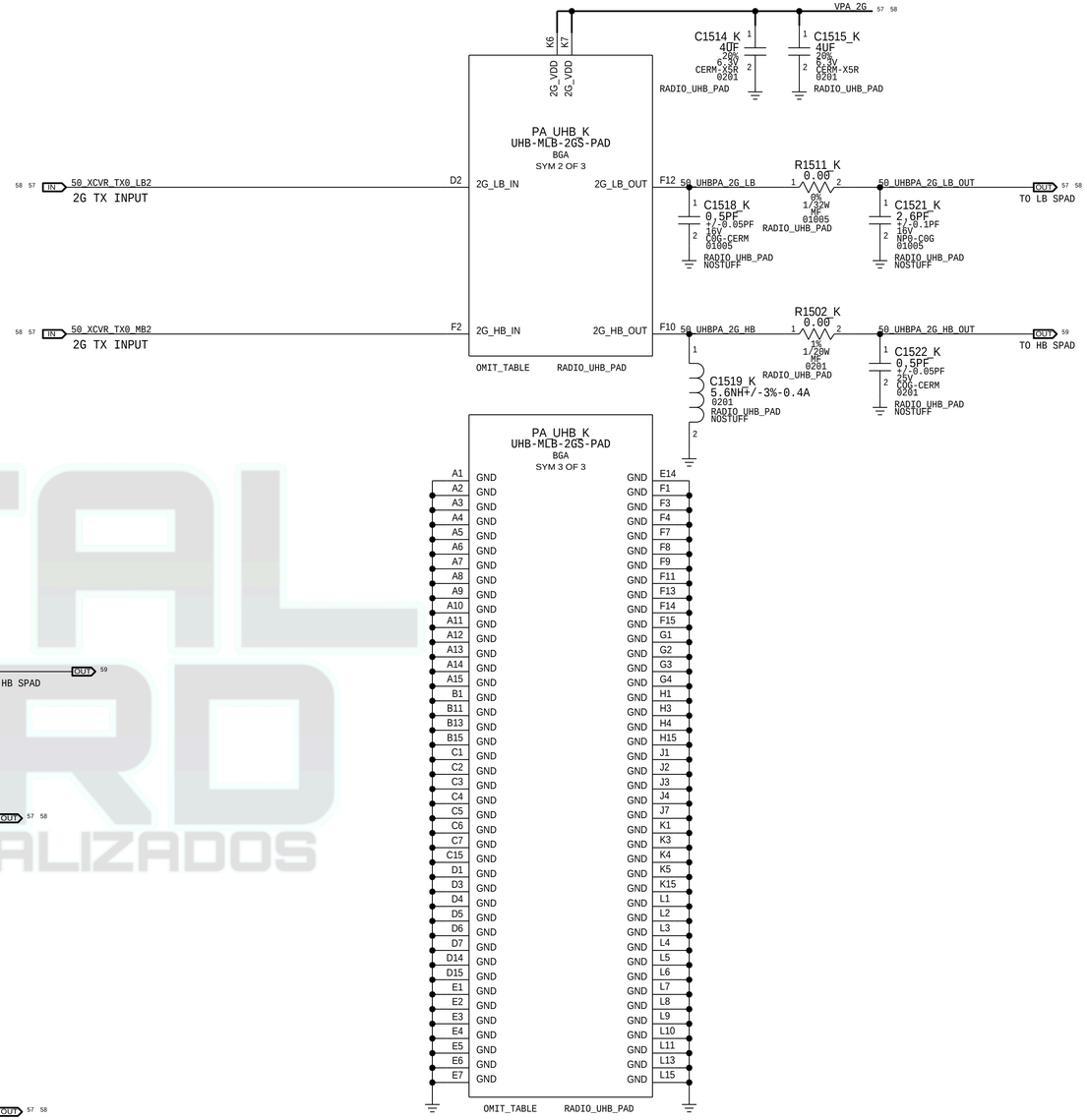
DOMAIN P,P,S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_XCVR*
P	A_50_WIDE_SE	50_HBPA_ANT1, 50_HBPA_ANT3, 50_HBPA_ANT3_M, 50_HBPA_DRX*
P	A_50_WIDE_L1_THIN_SE	50_HBPA_ANT1_M

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	SCOPE P/S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_XCVR*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_HBPA_ANT1, 50_HBPA_ANT3, 50_HBPA_ANT3_M, 50_HBPA_DRX*	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_HBPA_ANT1_M	Y

UHB MLB SPAD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01913	1	SKY78201-18	PA_UHB_K	ROW
353S01914	1	SKY78221-11	PA_UHB_K	USCH





NET RULE ASSIGNMENT		
SCHEM DP NO	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_WIDE_SE	50_UHBPA_2G_LB*,50_UHBPA_2G_HB
P	A_50_THIN_SE	50_UHBPA_MLB*, 50_UHBPA_2G_HB_OUT
P	A_50_WIDE_L1_THIN_SE	50_UHBPA_UHB*, 50_UHBPA_ANT*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR ON HIPRO
CLASS NAME	SCHEM DP NO	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_UHBPA_2G_LB*, 50_UHBPA_2G_HB	Y
50_THIN	S	A_DIELECTRIC_2X	50_UHBPA_MLB*, 50_UHBPA_2G_HB_OUT	Y
50_WIDE_L1_THIN	S	A_DIELECTRIC_2X_50_WIDE_L1_THIN_SE	50_UHBPA_UHB*, 50_UHBPA_ANT*	Y

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

N104 MLB BOTTOM BOARD

LAST_MODIFICATION=Tue May 28 17:48:05 2019

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-04049	1	SCH,MLB_BOT,N104	SCH	CRITICAL	?
820-01525	1	PCB,MLB_BOT,N104	PCB	CRITICAL	?

Sub Designs

SOURCE PROJECT	SUB-DESIGN NAME	VERSION	HARD/SOFT	SYNC_DATE/TIME
D42	DOE_HIER_NFC	0.49.0	H	2019_05_08_02:13:46
D43	RADIO_MLB_ICE	0.137.0	H	2019_05_16_17:54:06
D42	ROSE_MLB	0.56.0	H	2019_05_08_02:14:06
N104	RADIO_MLB_ICE_FF	0.81.0	S	2019_05_28_17:35:34
D42	LAA_MLB	0.29.0	H	2019_05_21_09:58:18
D42	WIFI_MLB	0.39.0	H	2019_05_08_02:13:26

Global Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
132S00185	132S0316	ALT_PARTS	ALL	CAP,CER,X5R,0.1UF,20%,6.3V,01005
138S0706	138S0739	ALT_PARTS	ALL	CAP,CER,X5R,1UF,20%,10V,0201,SAMSUNG
138S00049	138S0831	ALT_PARTS	ALL	CAP,CER,X5R,2.2UF,20%,6.3V,0201,KYOCERA
138S00133	138S00128	ALT_PARTS	ALL	CAP,CER,X5R,0.47UF,20%,6.3V,MUR,01005
138S00269	138S00128	ALT_PARTS	ALL	CAP,X5R,0.47UF,20%,6.3v,01005,TY
132S00232	132S00014	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,10%,6.3V,K,01005
132S00233	132S00014	ALT_PARTS	ALL	CAP,CER,X5R,0.22UF,10%,6.3V,T,01005
155S00414	155S0876	ALT_PARTS	ALL	FERR 80,10 OHM,50%,1.1A,0.05 DCR,01005
138S00246	138S00185	ALT_PARTS	ALL	FERR 80,10 OHM,50%,1.1A,0.05 DCR,01005
371S00108	371S00062	ALT_PARTS	ALL	0201, Schottky Diodes
155S00200	155S00400	ALT_PARTS	ALL	FERR 80,1500OHM,25%,200MA,0.7DCR,01005,TY
155S00194	155S00400	ALT_PARTS	ALL	FERR 80,1500OHM,25%,200MA,0.800CR,01005,TDK
155S00400	155S00200	ALT_PARTS	ALL	FERR 80,1500OHM,25%,200MA,0.7DCR,01005,MUR
155S00194	155S00200	ALT_PARTS	ALL	FERR 80,1500OHM,25%,200MA,0.800CR,01005,TDK
138S1103	138S0719	ALT_PARTS	ALL	CAP,CER,X5R,4.7UF,20%,10V,0402,TY

SYSTEM WIDE

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME		CONSTRAINT SET		DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
GND		S	DEFAULT	GND ?	
90_OHM		P	A_90_OHM_DIFF	DP:DP_*90* ?	

SYSTEM WIDE

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME		CONSTRAINT SET		DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
PWR_SHAPE		P	PWR_SHAPE	PP_VDD_MAIN ?	
PWR_SHAPE		P	PWR_50UM	PP1V0_S4,PP1V2_S2 ?	
PWR_SHAPE		P	PWR_80UM	PP1V8_S4,PP1V8_S2 ?	

SYSTEM OVERRIDES

DOMAIN (E.P.D)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_WLAN_G_TRX0_VOID_DTCK
P	A_50_THIN_SE	50_ANT5_WLAN_G
P	A_50_THIN_SE	50_UWB_ANT2_6G

CLASS DEFINITIONS				COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME		CONSTRAINT SET		DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN		S	A_DIELECTRIC_2X	50_WLAN_G_TRX0_VOID_DTCK Y	
50_THIN		S	A_DIELECTRIC_2X	50_ANT5_WLAN_G Y	
50_THIN		S	A_DIELECTRIC_2X	50_UWB_ANT2_6G Y	

CONSTRAINTS

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from: interlay, shortest distance is used unless 'L' is defined	EXAMPLE: 1,2,L,5,3L,4L 2
A_DIELECTRIC_(N)XD XV,XVL,X Calculates dielectric distance from Hybrid Table and interlay, shortest distance is used unless L defined	EXAMPLE: 2,2DL,3D,5D,7V,4VL,10VL 2,2D,4D,4V
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from: interlay, shortest distance is used unless 'L' is defined	EXAMPLE: 2_4_6_3L ?

RADIOS

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_WIDE		ZONE NAME= PRIMARY	
TOP	ISL3	50	0.169
ISL6	ISL4,BOTTOM	50	0.095
ISL3	TOP,ISL4	50	0.44

HYBRID IMPEDANCE RULE			
TRACE LAYER	REFERENCE LAYER(s)	REQUIRED IMPEDANCE	TRACE WIDTH (OPTIONAL)
RULE NAME= 50_THIN		ZONE NAME= PRIMARY	
TOP	ISL2	50	0.061
ISL3	ISL2,ISL4	50	0.029
ISL5	ISL4,ISL6	50	0.044
ISL7	BOTTOM,ISL6	50	0.029

CAPPED RULE EXAMPLE:SMD2ALL:SMD_TO_SMD:MVIA2ALL:SHAPE2ALL	LAYER X=ALL/EXT/INT INT=ALL	VALUE (MM)	RULE NAME(S) EXAMPLE: 2D,2V,3DL-5DL,3VL
LINE2SMD	?	0.070	2,2D,4D,4V
MVIA2MVIA	?	=0.065	2,2D,4D,4V
MVIA2SMD	?	=0.070	2,2D,4D,4V
MVIA2SHAPE	?	=0.070	2,2D,4D,4V
SMD2SMD	?	0.070	2,2D,4D,4V
SMD2SHAPE	?	0.070	2,2D,4D,4V
LINE2SHAPE	?	0.165	2
LINE2MVIA	?	0.165	2

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME		CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
E_PCIE_WLAN	E	PCIE_BOT	DP:DP_*90_PCIE*_WLAN*	?
E_PCIE_BB	E	PCIE_BOT	DP:DP_*90_PCIE*_BB*	?
E_GENERIC	E	GENERIC_DP	DP:DP_*NTC*,DP_50_ET*	?
E_DIGRF	E	DIGRF_DP	DP:DP_90_DIGRF*	?

Global Capacitors

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00138	138S00139	ALT_PARTS	ALL	CAP,4.7UF,20%,4V,KYO,0201
138S00164	138S00139	ALT_PARTS	ALL	CAP,4UF,20%,4V,TY,0201

CRITICAL PART#	COMMENT
138S00139	CAP,X5R,4.0UF,20%,4V,MUR,0201

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00048	138S00003	ALT_PARTS	ALL	0402,15uF,6.3V, Kyocera

CRITICAL PART#	COMMENT
138S00003	0402,15uF,6.3

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00128	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,Murata
138S00269	138S00133	ALT_PARTS	ALL	01005,0.47uF,6.3V,TY

CRITICAL PART#	COMMENT
138S00133	01005,0.47uF, 6.3V

FIDUCIALS

Crosses

FD0500 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0501 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0502 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0503 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0504 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0505 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY
FD0506 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY

Squares

FD0507 FID 0P55Q-CROSS-NSP 1 — ROOM=ASSEMBLY

ST0500 STIFFENER-UAT-MLB-X1403 SM 1 — OMIT_TABLE

PTH0501 P2MM SM PP
PTH0502 P2MM SM PP

ST0502 STIFFENER-LAT-MLB-X1403 SM 1 — OMIT_TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-19412	1	STIFFENER,MLB,NORTH,N104	ST0500	CRITICAL	?
806-19413	1	STIFFENER,MLB,SOUTH,N104	ST0502	CRITICAL	?

WLAN UF CAPS

CKPLUS_WAIVE=TERMSHORTED R0501 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0502 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0503 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0504 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0505 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0507 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0508 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0509 0.00 0% 1/32W MF 01005
CKPLUS_WAIVE=TERMSHORTED R0510 0.00 0% 1/32W MF 01005

XCVR UF CAPS

CKPLUS_WAIVE=TERMSHORTED R0527 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0528 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R051 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0512 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0513 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0514 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0515 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0516 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0529 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0517 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0518 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0519 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0520 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0521 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0522 0.00 0% 1/32W MF 01005 ROOM=XCVR

14 VRF_LO_1V15

CKPLUS_WAIVE=TERMSHORTED R0523 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0524 0.00 0% 1/32W MF 01005 ROOM=XCVR
CKPLUS_WAIVE=TERMSHORTED R0525 0.00 0% 1/32W MF 01005 ROOM=XCVR

Test/Probe Points - BOTTOM

Test Points

14 13 9 5 IN PP_VDD_MAIN

TP0700 TP0701 TP0702 TP0703 TP0704 TP0705 TP0706 TP0707 TP0708 TP0709 TP0710 TP0717 TP0711 TP0712 TP0713 TP0714

TP-P55 A ROOM=TEST_BOT

9 PP_GPU_LVCC — TP0715

9 PP_CPU_PCORE_LVCC — TP0716

9 AMUX_PMU_AY — TP0720

9 AMUX_PMU_BY — TP0721

9 PP_VBUS1_E75 — TP0723

9 GPIO_ISP_TO_CAM_PMU1_RESET_L — TP0724

9 4 PP_BATT_VCC_YANGTZE — TP0725

9 4 PP_BATT_VCC_YANGTZE — TP0726

9 4 PP_BATT_VCC_YANGTZE — TP0738

9 PP_VDD_MAIN_OV_R — TP0727

9 IO_PMU_TO_SYSTEM_RESET_L — TP0730

9 IO_HYDRA_TO_AP_FORCE_DFU — TP0729

10 5 DOTARA_COIL2 — TP0731

9 5 PP_VBUS2_DOTARA — TP0732

10 5 DOTARA_AC1 — TP0733

5 PP_DOTARA_VRECT — TP0734

6 5 PP_DOTARA_VMID — TP0735

PROBE POINTS

YETI Boost

8 IN PP_LED1_BOOST_OUT 1 PP — PP0760 P2MM-NSM SM

WLAN PCIe

13 9 IN 90_PCIE3_AP_TO_WLAN_REFCLK_P 1 PP — PP0782 P2MM-NSM SM
13 9 IN 90_PCIE3_AP_TO_WLAN_REFCLK_N 1 PP — PP0783 P2MM-NSM SM
13 9 IN 90_PCIE3_AP_TO_WLAN_TX_P 1 PP — PP0784 P2MM-NSM SM
13 9 IN 90_PCIE3_AP_TO_WLAN_TX_N 1 PP — PP0785 P2MM-NSM SM
13 9 IN 90_PCIE3_AP_FROM_WLAN_RX_P 1 PP — PP0787 P2MM-NSM SM
13 9 IN 90_PCIE3_AP_FROM_WLAN_RX_N 1 PP — PP0788 P2MM-NSM SM

BB PCIe

14 9 IN 90_PCIE4_AP_FROM_BB_RX_P 1 PP — PP0740 P2MM-NSM SM
14 9 IN 90_PCIE4_AP_FROM_BB_RX_N 1 PP — PP0741 P2MM-NSM SM
14 9 IN 90_PCIE4_AP_TO_BB_TX_P 1 PP — PP0742 P2MM-NSM SM
14 9 IN 90_PCIE4_AP_TO_BB_TX_N 1 PP — PP0743 P2MM-NSM SM
14 9 IN 90_PCIE4_AP_TO_BB_REFCLK_P 1 PP — PP0744 P2MM-NSM SM
14 9 IN 90_PCIE4_AP_TO_BB_REFCLK_N 1 PP — PP0745 P2MM-NSM SM

VALIDATION

9 8 IN GPIO_CAM_PMU1_TO_STROBE_DRIVER_HWEN 1 PP — PP0703 P2MM-NSM SM
13 9 7 IN SPI0_AOP_TO_IMU_R1_SCLK 1 PP — PP0705 P2MM-NSM SM
13 9 7 IN SPI0_AOP_TO_IMU_R1_MOSI 1 PP — PP0706 P2MM-NSM SM

12 9 IN IO_BUTTON_RINGER_A 1 PP — PP0700 P2MM-NSM SM
12 8 IN IO_BUTTON_VOL_DOWN_L 1 PP — PP0701 P2MM-NSM SM
12 9 IN IO_BUTTON_VOL_UP_L 1 PP — PP0702 P2MM-NSM SM
11 9 IN IO_BUTTON_SIDE_L 1 PP — PP0704 P2MM-NSM SM

Dotara

6 5 IN IO_DOTARA_TO_DOMBRA_EN 1 PP — PP0720 P2MM-NSM SM
9 5 IN GPIO_PMU_TO_DOTARA_EN_EXT_1V8 1 PP — PP0721 P2MM-NSM SM
5 DOTARA_GPIO6 1 PP — PP0722 P2MM-NSM SM
5 DOTARA_GPIO4 1 PP — PP0723 P2MM-NSM SM
5 IO_DOTARA_DFT1 1 PP — PP0724 P2MM-NSM SM
5 IO_DOTARA_DFT2 1 PP — PP0725 P2MM-NSM SM
9 5 SPMI0_NUB_TO_PMU_DOTARA_CLK 1 PP — PP0726 P2MM-NSM SM
9 5 SPMI0_NUB_BI_PMU_DOTARA_DATA 1 PP — PP0727 P2MM-NSM SM
5 DOTARA_TX_GATE_2 1 PP — PP0728 P2MM-NSM SM
5 SWD_DOTARA 1 PP — PP0729 P2MM-NSM SM
5 I2C_DOTARA_SDA 1 PP — PP0730 P2MM-NSM SM
5 I2C_DOTARA_SCL 1 PP — PP0731 P2MM-NSM SM
5 DOTARA_GPIO3 1 PP — PP0732 P2MM-NSM SM

GROUND CANARIES

9 GND — RWT_EXCLUDE
9 GND

Dotara

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S00246	138S00185	ALT_PARTS	ALL	CAP,X5R,2.2UF,20%25v,0402
376S00362	376S00295	ALT_PARTS	ALL	ONSEMI,TX FET

CRITICAL PART#	COMMENT
138s00185	CAP,X5R,14UF,20%,4V,MUR,0402

Board ID Map

N104	D42	D43
ANA3 GND ANA4 GND	ANA3 1V8 ANA4 1V8	ANA3 1V8 ANA4 GND

Pull-Ups

PP1V8_DOTARA
R3463 10K 5% 1/32W MF 01005 ROOM=DOTARA
IO_PMU_TO_DOTARA_RESET_L

MTP

IO_DOTARA_OTP_WREN
R3464 0.00 0% 1/32W MF 01005 ROOM=DOTARA
NOSTUFF
IO_DOTARA_TCK
IO_DOTARA_OTP_WREN
R3466 0.00 0% 1/32W MF 01005 ROOM=DOTARA
IO_DOTARA_INT

IO_TOUCH_TO_MANY_SCAN_ACTIVE_R
R3465 10K 5% 1/32W MF 01005 ROOM=DOTARA

PP_DOTARA_VRECT
C3440 220PF 5% 25V C0G 01005 ROOM=DOTARA
C3432 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA
C3433 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA
C3434 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA
C3435 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA
C3436 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOMBRA
C3437 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA

OMIT XW3401 SHORT-10L-0.05MM-SM ROOM=DOTARA
PP_DOTARA_VRECT_SENSE
R3431 0.02 1% 1/6W MF 0402
PP_DOTARA_VMID_SENSE
OMIT XW3400 SHORT-10L-0.05MM-SM ROOM=DOTARA
PP_DOTARA_VMID
C3438 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA
C3441 220PF 5% 25V C0G 01005 ROOM=DOTARA

PP_DOTARA_VRECT
DOTARA_AC2
R3412 100K 1% 1/20W MF 201 ROOM=DOTARA
R3411 100K 1% 1/20W MF 201 ROOM=DOTARA
R3485 499 1% 1/32W MF 01005
DOTARA_BOOT_FILT
C3429 0.1UF 10% 25V X5R 0201 ROOM=DOTARA

D1 D2 D3 D4 D5 D6 D7 D8 — RECT
E8 RECT_S
E7 VMID_S
F4 F5 F6 F7 F8 — VMID
H1 VMID5
PP5V0_DOTARA_VMID
C3461 1UF 20% 16V CER-X5R 0201 ROOM=DOTARA

U3400 STPMB0 CSP ROOM=DOTARA

DOTARA_VCAP1	E4	VCAP1
DOTARA_VCAP2	E5	VCAP2
DOTARA_CLAMP1	B3	CLAMP1
DOTARA_COMM1	B4	COMM1
DOTARA_BOOT	H4	BOOT
	C3	NC BOOT1_GATE1
	C4	NC BOOT1_GATE2
DOTARA_BOOT1	C1	BOOT1
DOTARA1_BOOT_XW	B1	AC1
	B2	AC1
DOTARA_AC1	C2	AC1
DOTARA_AC2	B7	AC2
	B8	AC2
DOTARA2_BOOT_XW	C7	AC2
DOTARA_BOOT2	C8	BOOT2
DOTARA_TX_GATE_2	C6	BOOT2_GATE1
	C5	NC BOOT2_GATE2
DOTARA_COMM2	B5	COMM2
DOTARA_CLAMP2	B6	CLAMP2
	H8	NC ANA1
	H7	NC ANA2
	H6	ANA3
	H5	ANA4
	L1	ILIM_BOOST
	H3	NC TX_MODE
	J2	NC OVP_ON
	K7	ALERT*

CLK_IN	K5	CLK_BBPMU_TO_DOTARA_38M4_1V8 IN
FB_BOOST	H2	ANALOG_FB_DOMBRA OUT
EN_BOOST	L2	IO_DOTARA_TO_DOMBRA_EN OUT
FPWM_BOOST	K2	IO_DOTARA_TO_DOMBRA_FPWM OUT
FPWM_IN	J3	IO_TOUCH_TO_MANY_SCAN_ACTIVE_R
VOUT	G4	PP_VBUS2_DOTARA
VOUT	G5	
VOUT	G6	
VOUT	G7	
VOUT	G8	
VDD5	J1	PP5V0_VDD_DOTARA
VDD_1P8D	F1	
VDD_1P8	F2	PP1V8_DOTARA
SCLK	K6	SPMI0_NUB_TO_PMU_DOTARA_CLK IN
SDATA	M6	SPMI0_NUB_BI_PMU_DOTARA_DATA BI
SDATA	N6	
SDATA	P6	
SDA	L6	I2C_DOTARA_SDA (OKPLUS_WA1VE=I2C_PULLUP)
SCL	J6	I2C_DOTARA_SCL (OKPLUS_WA1VE=I2C_PULLUP)
INT	L7	IO_DOTARA_INT
RESET*	L5	IO_PMU_TO_DOTARA_RESET_L IN
GPIO1	K4	SWD_DOTARA BI
GPIO2	L4	GPIO_DOTARA_TO_BBPMU_CLK_EN OUT
GPIO3	M4	DOTARA_GPIO3
GPIO3	N4	
GPIO3	P4	
GPIO4	M3	DOTARA_GPIO4 IN
GPIO4	N3	
GPIO4	P3	
GPIO5	L3	IO_DOTARA_TCK
GPIO6	K3	DOTARA_GPIO6 IN
VSYS_1P8_AON	K8	
EN_EXT_1P8	E2	GPIO_PMU_TO_DOTARA_EN_EXT_1V8 IN
VSYS_ANA	K1	PP_VDD_MAIN
VSYS_1P8	E1	PP1V8_S2
OTP_WREN	M5	IO_DOTARA_OTP_WREN
OTP_WREN	N5	
OTP_WREN	P5	
DFT1	J4	IO_DOTARA_DFT1
DFT2	J5	IO_DOTARA_DFT2

PGND: A1 A2 A3 A4 A5 A6 A7 A8
DGND: G1 G2 J7 J8 L8 M1 M2 M7 M8 N1 N2 N7 N8 P1 P2 P7 P8
AGND: E3 E6 F3 G3

C3421 4700PF 10% 50V X7R-CERM 0402
C3422 0.033UF 10% 50V X7R 0402
C3423 0.1UF 10% 25V X5R 0201
XW3410 OMIT SHORT-10L-0.1MM-SM
C3424 2200PF 10% 50V X5R 0201
C3425 2200PF 10% 50V X5R 0201 BOMOPTION=NOSTUFF
C3426 4700PF 10% 50V X7R-CERM 0402
C3427 0.033UF 10% 50V X7R 0402
C3428 0.1UF 10% 25V X5R 0201
XW3411 DOTARA_BOOT2

COIL2
DOTARA_TX_GATE_2
Q3400 DMT12H065LFDF UDFN2020 ROOM=DOTARA NOSTUFF
DOTARA_TX_BANK_2
R3401 100K 1% 1/20W MF 201 ROOM=DOTARA
C3401 0.068UF 10% 100V X6S 0402 NOSTUFF
C3402 0.047UF 10% 100V X6S 0402 NOSTUFF
C3403 0.047UF 10% 100V X6S 0402 NOSTUFF
C3404 0.068UF 10% 100V X6S 0402 NOSTUFF
DOTARA_COIL2
R3402 100K 1% 1/20W MF 201 ROOM=DOTARA
C3406 0.033UF 10% 100V X6S 0402 NOSTUFF
C3407 0.047UF 10% 100V X6S 0402 NOSTUFF
C3408 0.047UF 10% 100V X6S 0402 NOSTUFF
C3409 0.047UF 10% 100V X6S 0402 NOSTUFF
C3410 0.047UF 10% 100V X6S 0402 NOSTUFF
C3411 0.047UF 10% 100V X6S 0402 NOSTUFF

n104 Dotara Brd ID:
ANA3=GND, ANA4=GND

ANALOG_DOTARA_TO_DOMBRA_ILIM
R3413 0.00 0% 1/32W MF 01005 ROOM=DOTARA
ANALOG_DOTARA_TO_DOMBRA_ILIM_R

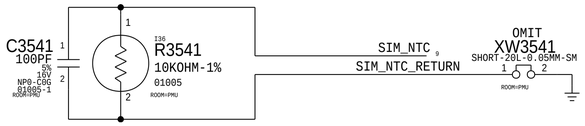
NOSTUFF
R3452 0.00 0% 1/32W MF 01005 ROOM=DOTARA_DOMBRA
IO_TOUCH_TO_MANY_SCAN_ACTIVE

C3468 220PF 5% 25V C0G 01005 ROOM=DOTARA
C3467 220PF 5% 25V C0G 01005 ROOM=DOTARA
C3462 0.47UF 20% 25V X5R 0201 ROOM=DOTARA
C3463 2.2UF 20% 25V X5R 0402-0P1MM ROOM=DOTARA

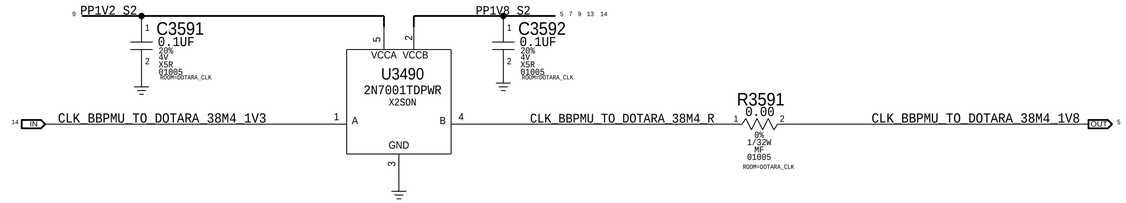
C3464 1UF 20% 16V CER-X5R 0201 ROOM=DOTARA
C3465 1UF 20% 6.3V X5R 0201 ROOM=DOTARA

R3461 10K 5% 1/32W MF 01005 ROOM=DOTARA
C3469 1.0UF 20% 6.3V X5R 0201-1

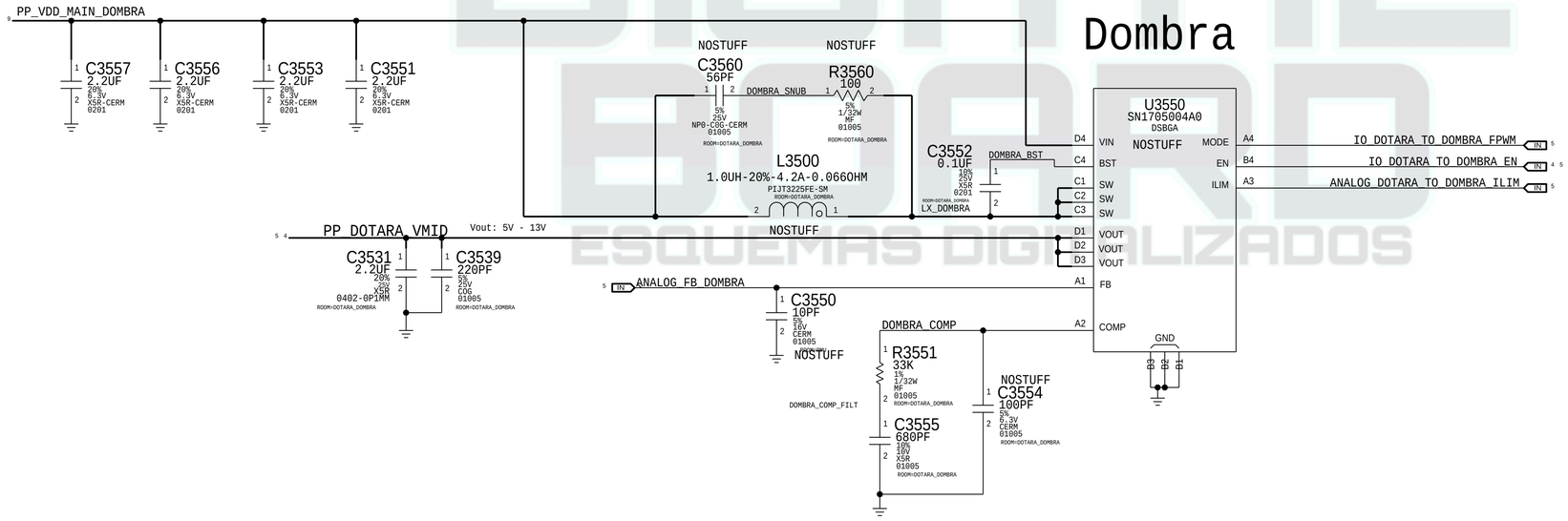
SIM NTC



Dotara Clock Buffer



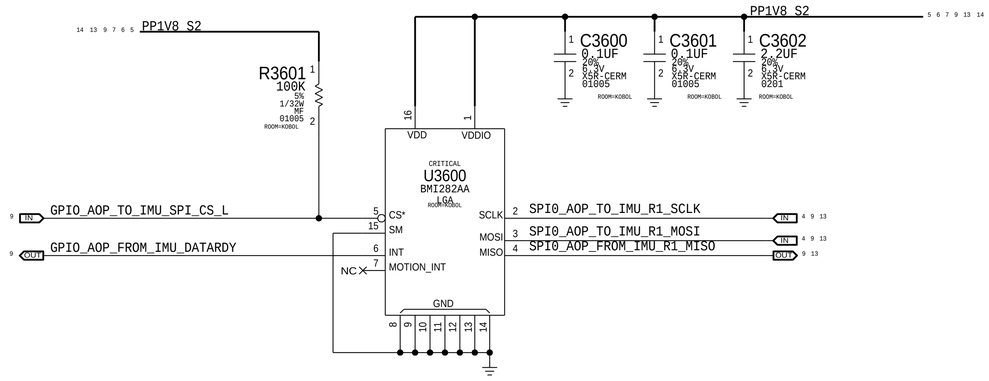
Dombra



Need 0 ohm R for termination on C3560,R3560,C3552,R3551,C3555
To be controlled by build matrix

Kobol - Accel & Gyro

APN: 338S00367

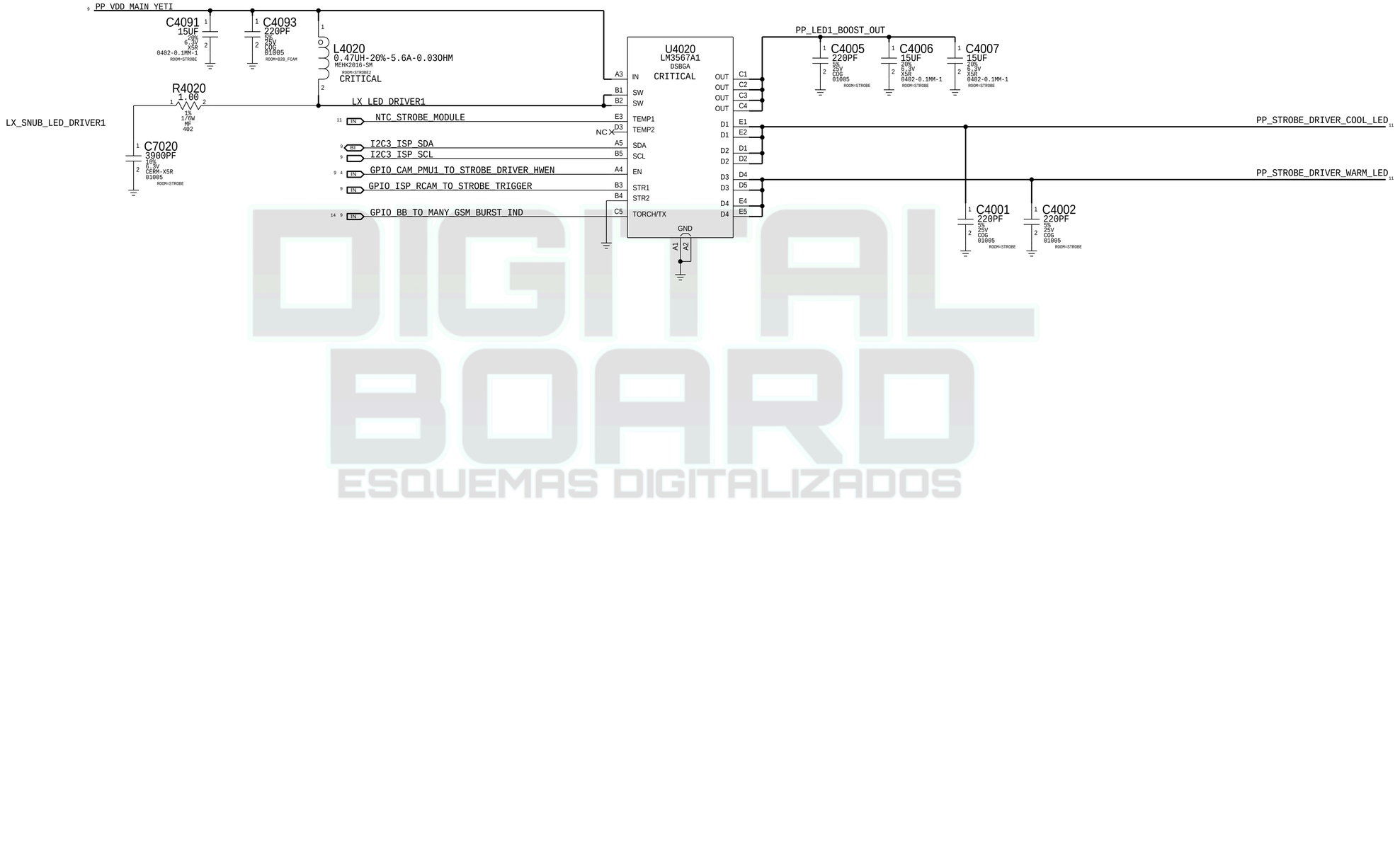


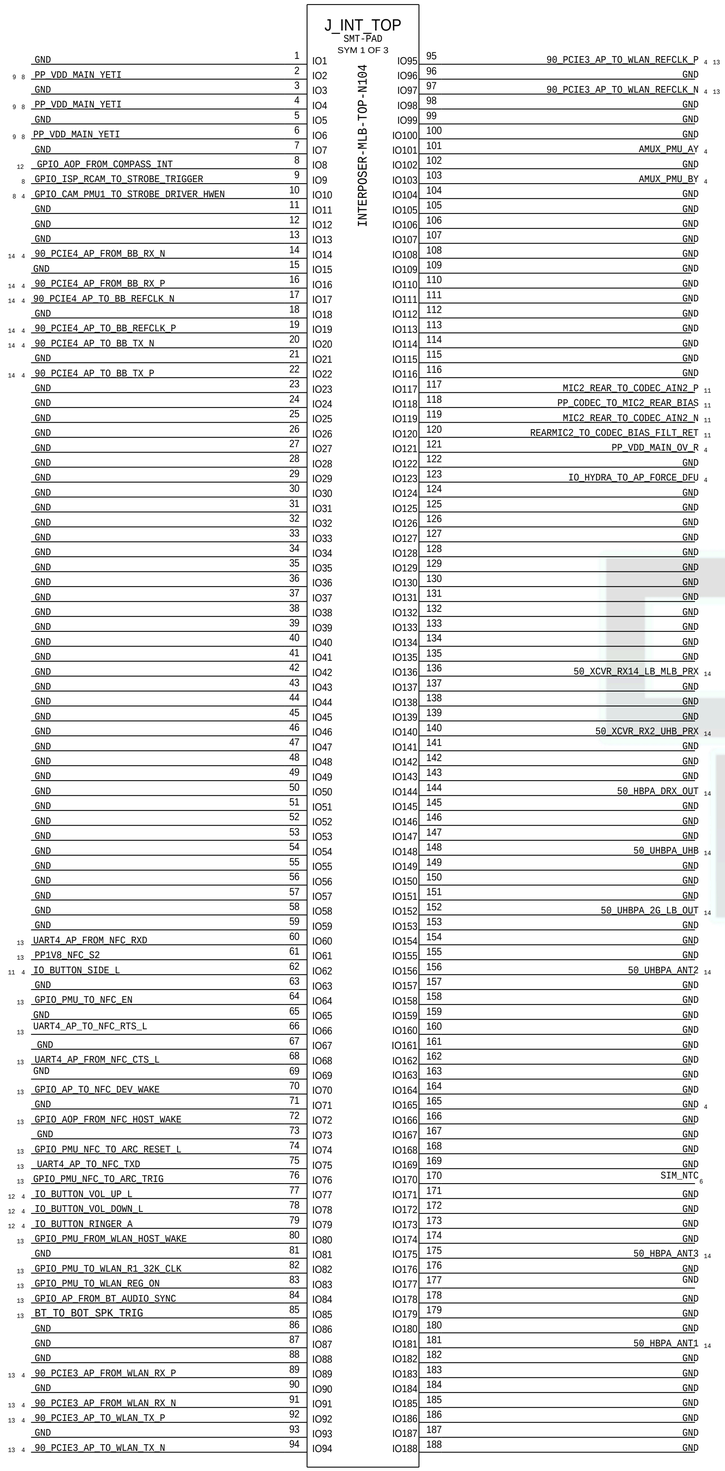
Yeti Inductor Alt

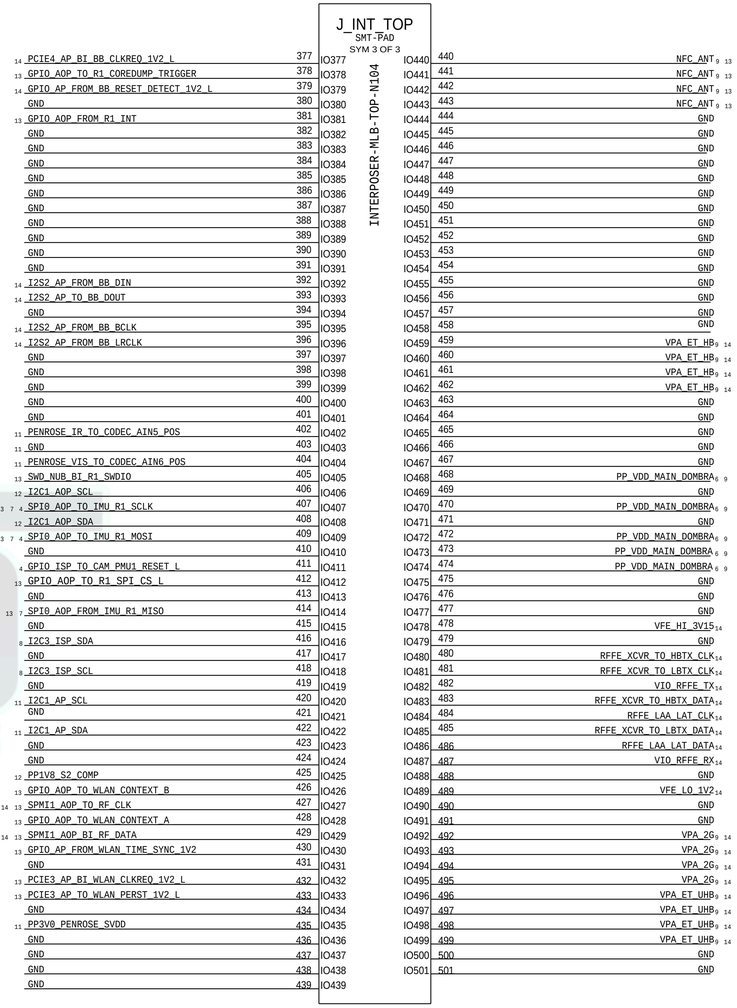
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00872	152S00918	ALT_PARTS	ALL	TDK,IND,MLZ,0.47UH,5.6A,30MΩ,2016
152S00847	152S00918	ALT_PARTS	ALL	CYNTEC,IND,MLD,0.47UH,5.6A,20MΩ,2016

LED STROBE DRIVER (YETI)

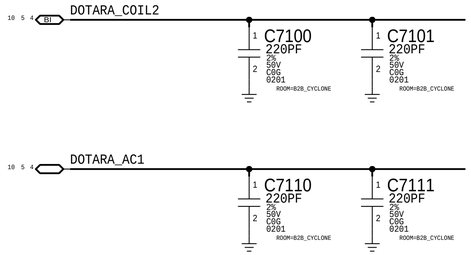
APN:353S01818
I2C Address (7-bit): 0x65





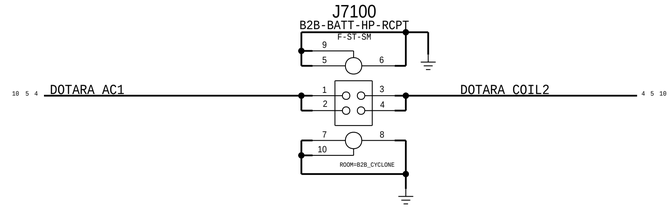


Cyclone Filtering

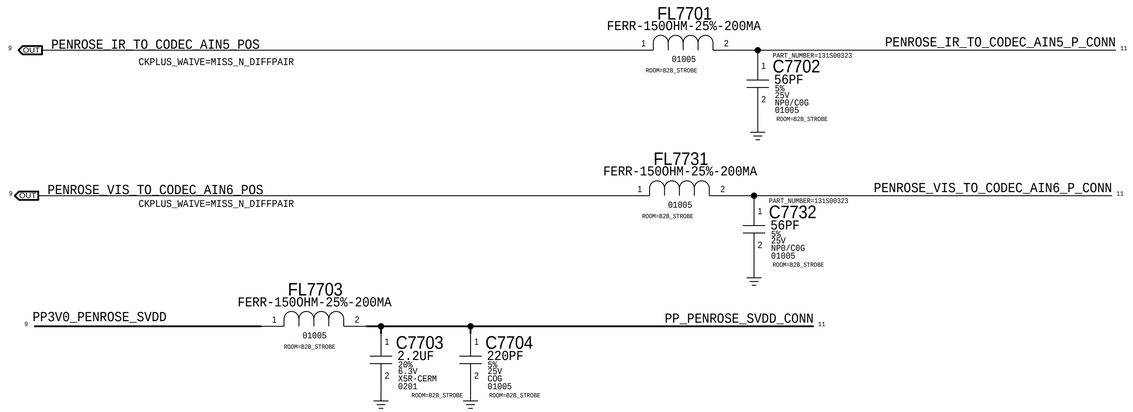


CYCLONE B2B

RCPT: 516S00485 <-- This one on MLB
PLUG: 516S00486

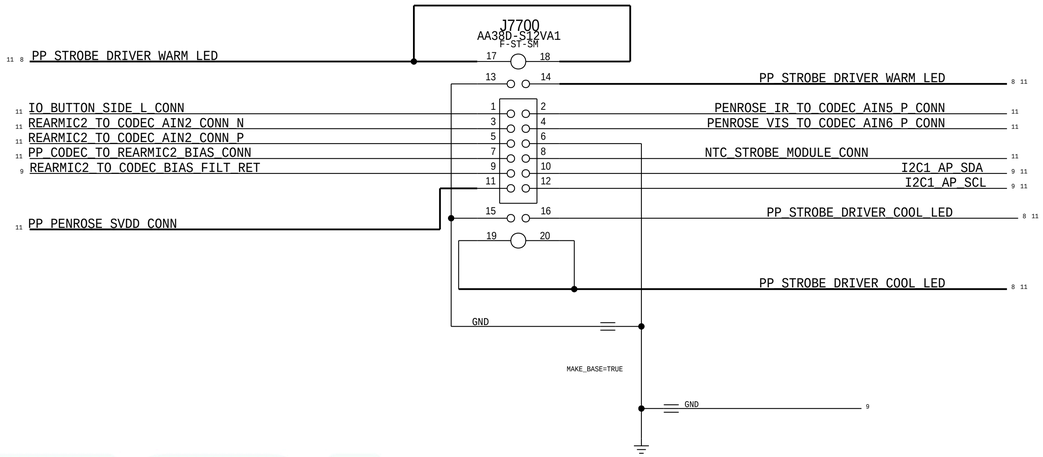


PENROSE

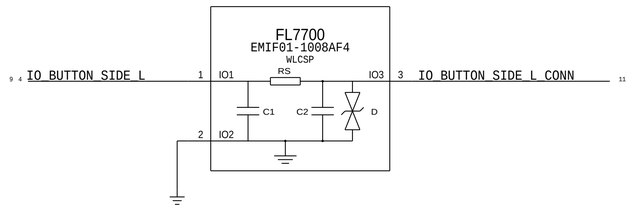


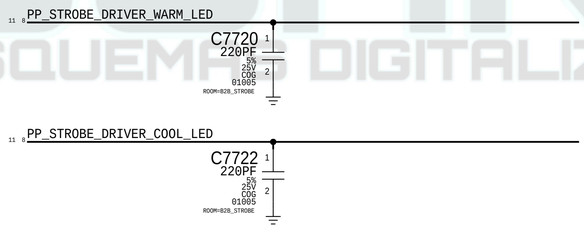
Strobe Connector

RCPT: 516S00530 <-- This one on MLB
PLUG: 516S00382

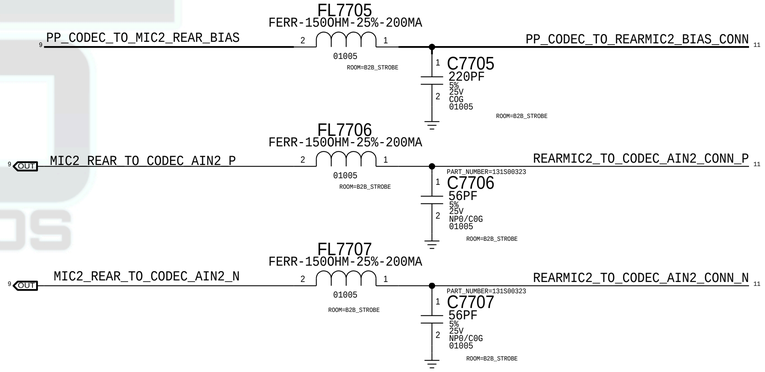


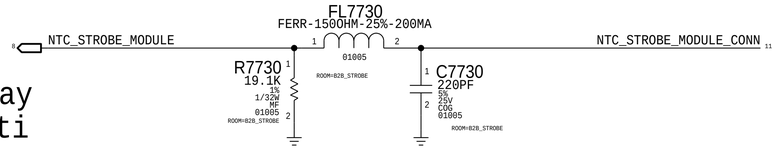
Strobe Filtering





MIC2 (ANC REF)





R7730 value may change for Yeti

UAT CONNECTOR

RCPT: 516S00532 <-- This one on MLB
PLUG: 516S00533

J_UAT_K
MM3531-2700A18
F-ST-SM

UAT_SUBUS_A_B2B	1	10	
R1_TUNER_GPO2_CONN	2	11	50_ANT4
PP_VDD_BTPA3V3_CONN	3	12	
R1_TUNER_GPO1_CONN	4	13	50_ANT2
IO_BUTTON_VOL_UP_CONN_L	5	14	
	6	15	UAT_SUBUS_B_B2B
COMPASS_TO_AOP_INT_CONN	7	16	IO_BUTTON_VOL_DOWN_CONN_L
PP1V8_COMPASS_CONN	8	17	I2C1_AOP_SDA
IO_BUTTON_RINGER_A_CONN	9	18	I2C1_AOP_SCL
	SHLD		
	19	25	
	20	26	
	21	27	
	22	28	
	23	29	
	24	30	

ARROW CONNECTOR

RCPT: 516S00434 <-- This one on MLB
PLUG: 516S00435

J_ARROW_R
MLF06
F-ST-SM

	16	
	12	8
	13	9
50_R1_AOA1	4	1
	5	2 → 50_R1_AOA3
50_R1_AOA0	6	3
		7
	14	10
	15	11
		17

FL8462
FERR-1500HM-25%-200MA
01005
ROOM=B2B_BUTTON
R1_TUNER_GPO1 → R1_TUNER_GPO1_CONN
C8462 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_BUTTON
PART_NUMBER=131S00323

FL8461
FERR-1500HM-25%-200MA
01005
ROOM=B2B_BUTTON
R1_TUNER_GPO2 → R1_TUNER_GPO2_CONN
C8461 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_BUTTON
PART_NUMBER=131S00323

FL8460
FERR-1500HM-25%-200MA
01005
ROOM=B2B_BUTTON
PP_VDD_BTPA3V3 → PP_VDD_BTPA3V3_CONN
C8460 220PF 5% 25V C0G 01005 ROOM=B2B_BUTTON

BUTTONS

FL8440
EMIF01-1008AF4
WLCSP
IO_BUTTON_RINGER_A → IO_BUTTON_RINGER_A_CONN
C1 C2 D
ROOM=B2B_STROBE

FL8441
EMIF01-1008AF4
WLCSP
IO_BUTTON_VOL_DOWN_L → IO_BUTTON_VOL_DOWN_CONN_L
C1 C2 D
ROOM=B2B_STROBE

FL8442
EMIF01-1008AF4
WLCSP
IO_BUTTON_VOL_UP_L → IO_BUTTON_VOL_UP_CONN_L
C1 C2 D
ROOM=B2B_STROBE

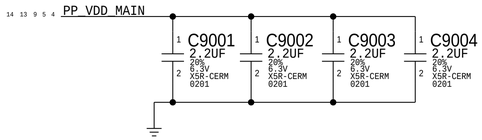
Compass

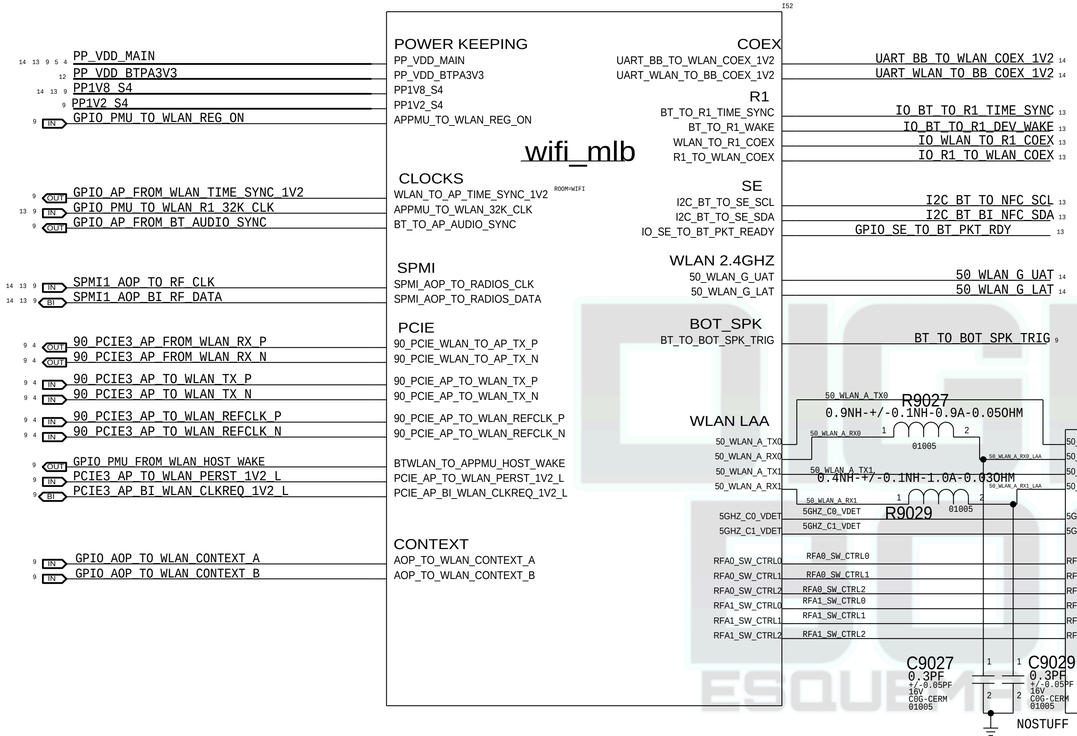
FL8450
FERR-1500HM-25%-200MA
01005
ROOM=B2B_BUTTON
PP1V8_S2_COMP → PP1V8_COMPASS_CONN
C8450 220PF 5% 25V C0G 01005 ROOM=B2B_BUTTON

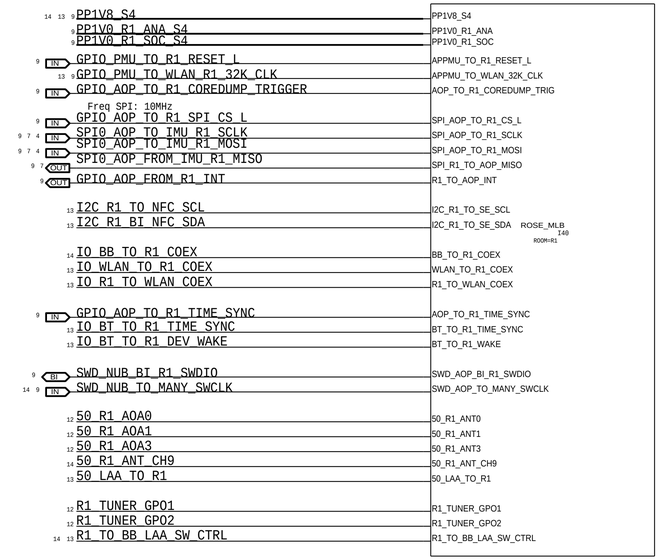
I2C1_AOP_SCL → CKPLUS_WAIVE=I2C_PULLUP
C8431 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_BUTTON
PART_NUMBER=131S00323

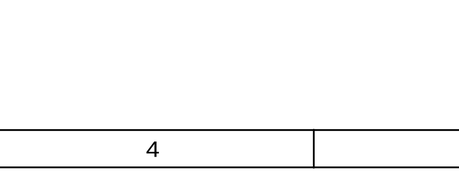
I2C1_AOP_SDA → CKPLUS_WAIVE=I2C_PULLUP
C8432 56PF 5% 25V NP0/C0G 01005 ROOM=B2B_BUTTON
PART_NUMBER=131S00323

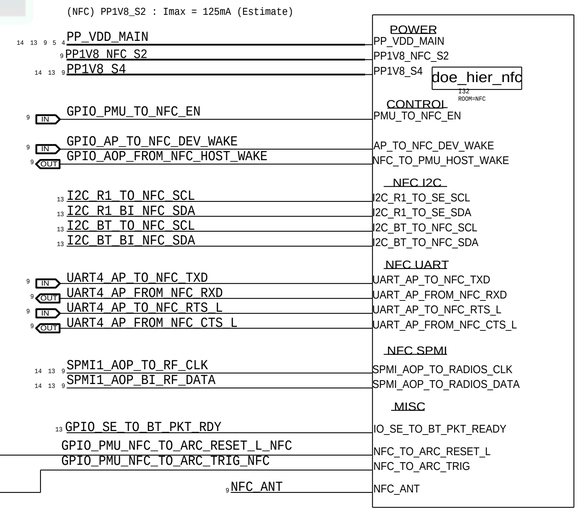
R8433 0.00 5% 1/32W MF 01005 ROOM=B2B_BUTTON
GPIO_AOP_FROM_COMPASS_INT → COMPASS_TO_AOP_INT_CONN
C8433 220PF 5% 25V C0G 01005 ROOM=B2B_BUTTON

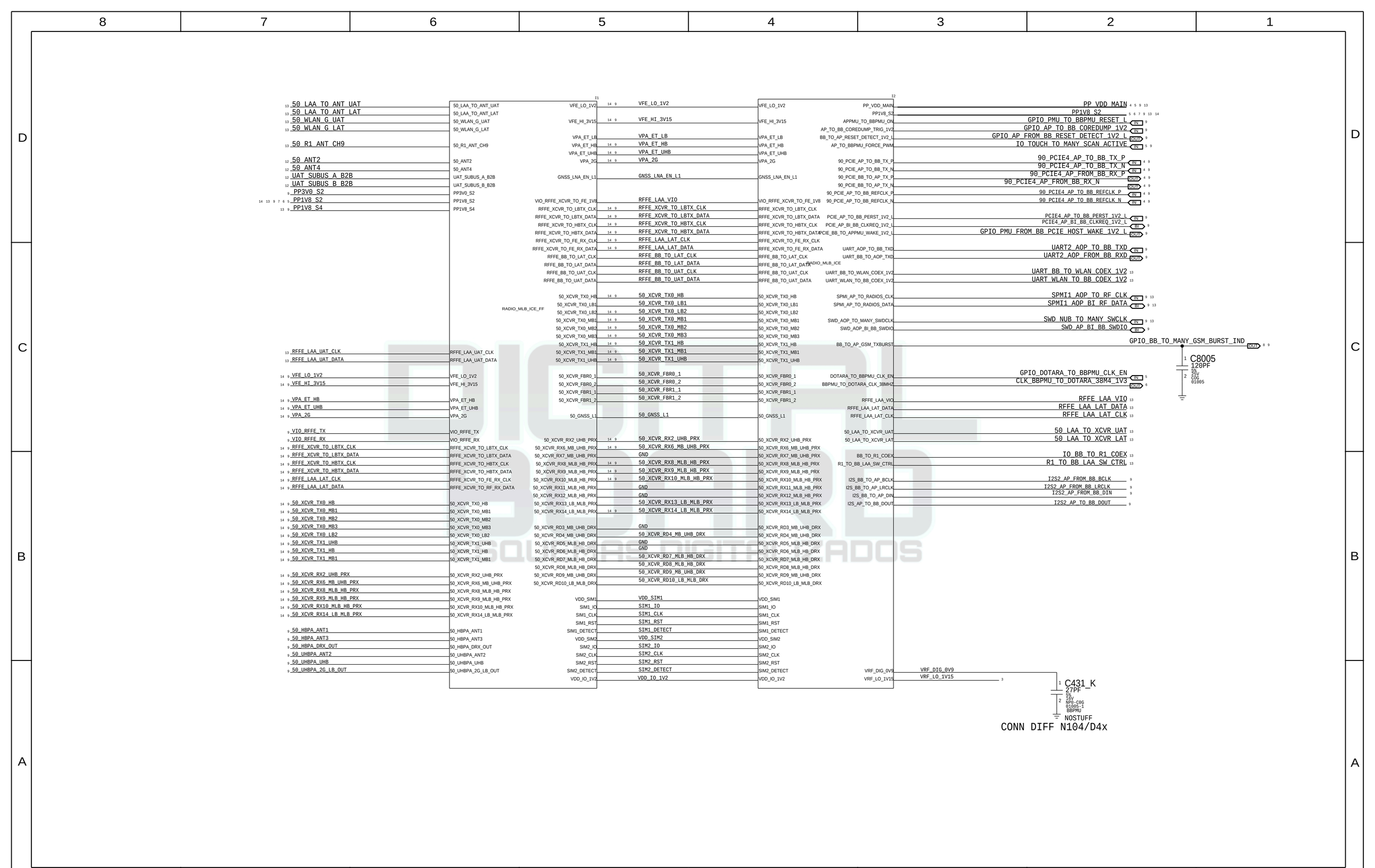

14 13 9 5 4 PP_VDD_MAIN
C9001 2.2UF 20% 6.3V X5R-CERM 0201
C9002 2.2UF 20% 6.3V X5R-CERM 0201
C9003 2.2UF 20% 6.3V X5R-CERM 0201
C9004 2.2UF 20% 6.3V X5R-CERM 0201


I52
wifi_mlb
ROOM=WIFI
POWER KEEPING
PP_VDD_MAIN
PP_VDD_BTPA3V3
PP1V8_S4
PP1V2_S4
APPMU_TO_WLAN_REG_ON
CLOCKS
WLAN_TO_AP_TIME_SYNC_1V2
APPMU_TO_WLAN_32K_CLK
BT_TO_AP_AUDIO_SYNC
SPMI
SPMI_AOP_TO_RADIOS_CLK
SPMI_AOP_TO_RADIOS_DATA
PCIE
90_PCIE_WLAN_TO_AP_TX_P
90_PCIE_WLAN_TO_AP_TX_N
90_PCIE_AP_TO_WLAN_TX_P
90_PCIE_AP_TO_WLAN_TX_N
90_PCIE_AP_TO_WLAN_REFCLK_P
90_PCIE_AP_TO_WLAN_REFCLK_N
BTWLAN_TO_APPMU_HOST_WAKE
PCIE_AP_TO_WLAN_PERST_1V2_L
PCIE_AP_BI_WLAN_CLKREQ_1V2_L
CONTEXT
AOP_TO_WLAN_CONTEXT_A
AOP_TO_WLAN_CONTEXT_B
COEX
UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2
R1
BT_TO_R1_TIME_SYNC
BT_TO_R1_WAKE
WLAN_TO_R1_COEX
R1_TO_WLAN_COEX
SE
I2C_BT_TO_SE_SCL
I2C_BT_TO_SE_SDA
IO_SE_TO_BT_PKT_READY
WLAN 2.4GHZ
50_WLAN_G_UAT
50_WLAN_G_LAT
BOT_SPK
BT_TO_BOT_SPK_TRIG
PP_VDD_MAIN
PP_VDD_BTPA3V3
PP1V8_S4
PP1V2_S4
GPIO_PMU_TO_WLAN_REG_ON
GPIO_AP_FROM_WLAN_TIME_SYNC_1V2
GPIO_PMU_TO_WLAN_R1_32K_CLK
GPIO_AP_FROM_BT_AUDIO_SYNC
SPMI1_AOP_TO_RF_CLK
SPMI1_AOP_BI_RF_DATA
90_PCIE3_AP_FROM_WLAN_RX_P
90_PCIE3_AP_FROM_WLAN_RX_N
90_PCIE3_AP_TO_WLAN_TX_P
90_PCIE3_AP_TO_WLAN_TX_N
90_PCIE3_AP_TO_WLAN_REFCLK_P
90_PCIE3_AP_TO_WLAN_REFCLK_N
GPIO_PMU_FROM_WLAN_HOST_WAKE
PCIE3_AP_TO_WLAN_PERST_1V2_L
PCIE3_AP_BI_WLAN_CLKREQ_1V2_L
GPIO_AOP_TO_WLAN_CONTEXT_A
GPIO_AOP_TO_WLAN_CONTEXT_B
UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2
IO_BT_TO_R1_TIME_SYNC
IO_BT_TO_R1_DEV_WAKE
IO_WLAN_TO_R1_COEX
IO_R1_TO_WLAN_COEX
I2C_R1_TO_NFC_SCL
I2C_R1_BI_NFC_SDA
GPIO_SE_TO_BT_PKT_RDY
50_WLAN_G_UAT
50_WLAN_G_LAT
BT_TO_BOT_SPK_TRIG
WLAN LAA
50_WLAN_A_TX0
50_WLAN_A_RX0
50_WLAN_A_TX1
50_WLAN_A_RX1
5GHZ_C0_VDET
5GHZ_C1_VDET
RFA0_SW_CTRL0
RFA0_SW_CTRL1
RFA0_SW_CTRL2
RFA1_SW_CTRL0
RFA1_SW_CTRL1
RFA1_SW_CTRL2
R9027 0.9NH-+/-0.1NH-0.9A-0.05OHM 01005
R9029 0.4NH-+/-0.1NH-1.0A-0.03OHM 01005
C9027 0.3PF +/-0.05PF 16V C0G-CERM 01005
C9029 0.3PF +/-0.05PF 16V C0G-CERM 01005
NOSTUFF
I53
LAA_MLB
ROOM=LAA
PP_VDD_MAIN
PP1V8_S2
PP1V8_S4
50_LAA_TO_ANT_LAT
50_LAA_TO_ANT_UAT
50_LAA_TO_XCVR_LAT
50_LAA_TO_XCVR_UAT
RFFE_LAA_LAT_VIO
RFFE_LAA_LAT_CLK
RFFE_LAA_LAT_DATA
RFFE_LAA_UAT_VIO
RFFE_LAA_UAT_CLK
RFFE_LAA_UAT_DATA
50_LAA_TO_R1
R1_TO_BB_LAA_SW_CTRL


PP1V8_S4
PP1V0_R1_ANA_S4
PP1V0_R1_SOC_S4
GPIO_PMU_TO_R1_RESET_L
GPIO_PMU_TO_WLAN_R1_32K_CLK
GPIO_AOP_TO_R1_COREDUMP_TRIGGER
Freq SPI: 10MHz
GPIO_AOP_TO_R1_SPI_CS_L
SPI0_AOP_TO_IMU_R1_SCLK
SPI0_AOP_TO_IMU_R1_MOSI
SPI0_AOP_FROM_IMU_R1_MISO
GPIO_AOP_FROM_R1_INT
I2C_R1_TO_NFC_SCL
I2C_R1_TO_NFC_SDA
IO_BB_TO_R1_COEX
IO_WLAN_TO_R1_COEX
IO_R1_TO_WLAN_COEX
GPIO_AOP_TO_R1_TIME_SYNC
IO_BT_TO_R1_TIME_SYNC
IO_BT_TO_R1_DEV_WAKE
SWD_NUB_BI_R1_SWDIO
SWD_NUB_TO_MANY_SWCLK
50_R1_AOA0
50_R1_AOA1
50_R1_AOA3
50_R1_ANT_CH9
50_LAA_TO_R1
R1_TUNER_GPO1
R1_TUNER_GPO2
R1_TO_BB_LAA_SW_CTRL
POWER UP SEQUENCE: Assert PMU_TO_R1_RESET_L >500uS after PP1V8_S4 AND PP1V0_S4 rails


GPIO_PMU_NFC_TO_ARC_RESET_L
GPIO_PMU_NFC_TO_ARC_TRIG
D8000 60.4K 1% 1/32W TK 01005
D8001 60.4K 1% 1/32W TK 01005


(NFC) PP1V8_S2 : Imax = 125mA (Estimate)
POWER
PP_VDD_MAIN
PP1V8_NFC_S2
PP1V8_S4
doe_hier_nfc
I32 ROOM=NFC
CONTROL
GPIO_PMU_TO_NFC_EN
GPIO_AP_TO_NFC_DEV_WAKE
GPIO_AOP_FROM_NFC_HOST_WAKE
NFC I2C
I2C_R1_TO_NFC_SCL
I2C_R1_BI_NFC_SDA
I2C_BT_TO_NFC_SCL
I2C_BT_BI_NFC_SDA
NFC UART
UART4_AP_TO_NFC_TXD
UART4_AP_FROM_NFC_RXD
UART4_AP_TO_NFC_RTS_L
UART4_AP_FROM_NFC_CTS_L
NFC SPMI
SPMI1_AOP_TO_RF_CLK
SPMI1_AOP_BI_RF_DATA
MISC
GPIO_SE_TO_BT_PKT_RDY
GPIO_PMU_NFC_TO_ARC_RESET_L_NFC
GPIO_PMU_NFC_TO_ARC_TRIG_NFC
NFC_ANT


50_LAA_TO_ANT_UAT
50_LAA_TO_ANT_LAT
50_WLAN_G_UAT
50_WLAN_G_LAT
50_R1_ANT_CH9
50_ANT2
50_ANT4
UAT_SUBUS_A_B2B
UAT_SUBUS_B_B2B
PP3V0_S2
PP1V8_S2
PP1V8_S4
RFFE_LAA_UAT_CLK
RFFE_LAA_UAT_DATA
VFE_LO_1V2
VFE_HI_3V15
VPA_ET_HB
VPA_ET_UHB
VPA_2G
VIO_RFFE_TX
VIO_RFFE_RX
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_LAA_LAT_CLK
RFFE_LAA_LAT_DATA
50_XCVR_TX0_HB
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX0_LB2
50_XCVR_TX1_UHB
50_XCVR_TX1_HB
50_XCVR_TX1_MB1
50_XCVR_RX2_UHB_PRX
50_XCVR_RX6_MB_UHB_PRX
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
50_XCVR_RX14_LB_MLB_PRX
50_HBPA_ANT1
50_HBPA_ANT3
50_HBPA_DRX_OUT
50_UHBPA_ANT2
50_UHBPA_UHB
50_UHBPA_2G_LB_OUT
I1
50_LAA_TO_ANT_UAT
50_LAA_TO_ANT_LAT
50_WLAN_G_UAT
50_WLAN_G_LAT
50_R1_ANT_CH9
50_ANT2
50_ANT4
UAT_SUBUS_A_B2B
UAT_SUBUS_B_B2B
PP3V0_S2
PP1V8_S2
PP1V8_S4
RFFE_LAA_UAT_CLK
RFFE_LAA_UAT_DATA
VFE_LO_1V2
VFE_HI_3V15
VPA_ET_HB
VPA_ET_UHB
VPA_2G
VIO_RFFE_TX
VIO_RFFE_RX
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_LAA_LAT_CLK
RFFE_LAA_LAT_DATA
50_XCVR_TX0_HB
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX0_LB2
50_XCVR_TX1_UHB
50_XCVR_TX1_HB
50_XCVR_TX1_MB1
50_XCVR_RX2_UHB_PRX
50_XCVR_RX6_MB_UHB_PRX
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
50_XCVR_RX14_LB_MLB_PRX
50_HBPA_ANT1
50_HBPA_ANT3
50_HBPA_DRX_OUT
50_UHBPA_ANT2
50_UHBPA_UHB
50_UHBPA_2G_LB_OUT
VFE_LO_1V2
VFE_HI_3V15
VPA_ET_LB
VPA_ET_HB
VPA_ET_UHB
VPA_2G
GNSS_LNA_EN_L1
VIO_RFFE_XCVR_TO_FE_1V8
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_XCVR_TO_FE_RX_CLK
RFFE_XCVR_TO_FE_RX_DATA
RFFE_BB_TO_LAT_CLK
RFFE_BB_TO_LAT_DATA
RFFE_BB_TO_UAT_CLK
RFFE_BB_TO_UAT_DATA
50_XCVR_TX0_HB
50_XCVR_TX0_LB1
50_XCVR_TX0_LB2
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX1_HB
50_XCVR_TX1_MB1
50_XCVR_TX1_UHB
50_XCVR_FBR0_1
50_XCVR_FBR0_2
50_XCVR_FBR1_1
50_XCVR_FBR1_2
50_GNSS_L1
50_XCVR_RX2_UHB_PRX
50_XCVR_RX6_MB_UHB_PRX
50_XCVR_RX7_MB_UHB_PRX
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
50_XCVR_RX11_MLB_HB_PRX
50_XCVR_RX12_MLB_HB_PRX
50_XCVR_RX13_LB_MLB_PRX
50_XCVR_RX14_LB_MLB_PRX
50_XCVR_RD3_MB_UHB_DRX
50_XCVR_RD4_MB_UHB_DRX
50_XCVR_RD5_MLB_HB_DRX
50_XCVR_RD6_MLB_HB_DRX
50_XCVR_RD7_MLB_HB_DRX
50_XCVR_RD8_MLB_HB_DRX
50_XCVR_RD9_MB_UHB_DRX
50_XCVR_RD10_LB_MLB_DRX
VDD_SIM1
SIM1_IO
SIM1_CLK
SIM1_RST
SIM1_DETECT
VDD_SIM2
SIM2_IO
SIM2_CLK
SIM2_RST
SIM2_DETECT
VDD_IO_1V2
RADIO_MLB_ICE_FF
VFE_LO_1V2
VFE_HI_3V15
VPA_ET_LB
VPA_ET_HB
VPA_ET_UHB
VPA_2G
GNSS_LNA_EN_L1
RFFE_LAA_VIO
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_LAA_LAT_CLK
RFFE_LAA_LAT_DATA
RFFE_BB_TO_LAT_CLK
RFFE_BB_TO_LAT_DATA
RFFE_BB_TO_UAT_CLK
RFFE_BB_TO_UAT_DATA
50_XCVR_TX0_HB
50_XCVR_TX0_LB1
50_XCVR_TX0_LB2
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX1_HB
50_XCVR_TX1_MB1
50_XCVR_TX1_UHB
50_XCVR_FBR0_1
50_XCVR_FBR0_2
50_XCVR_FBR1_1
50_XCVR_FBR1_2
50_GNSS_L1
50_XCVR_RX2_UHB_PRX
GND
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
GND
GND
50_XCVR_RX13_LB_MLB_PRX
50_XCVR_RX14_LB_MLB_PRX
GND
50_XCVR_RD4_MB_UHB_DRX
GND
GND
50_XCVR_RD7_MLB_HB_DRX
50_XCVR_RD8_MLB_HB_DRX
50_XCVR_RD9_MB_UHB_DRX
50_XCVR_RD10_LB_MLB_DRX
VDD_SIM1
SIM1_IO
SIM1_CLK
SIM1_RST
SIM1_DETECT
VDD_SIM2
SIM2_IO
SIM2_CLK
SIM2_RST
SIM2_DETECT
VDD_IO_1V2
I2
VFE_LO_1V2
VFE_HI_3V15
VPA_ET_LB
VPA_ET_HB
VPA_ET_UHB
VPA_2G
GNSS_LNA_EN_L1
VIO_RFFE_XCVR_TO_FE_1V8
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_XCVR_TO_FE_RX_CLK
RFFE_XCVR_TO_FE_RX_DATA
RFFE_BB_TO_LAT_CLK
RFFE_BB_TO_LAT_DATA
RFFE_BB_TO_UAT_CLK
RFFE_BB_TO_UAT_DATA
50_XCVR_TX0_HB
50_XCVR_TX0_LB1
50_XCVR_TX0_LB2
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX1_HB
50_XCVR_TX1_MB1
50_XCVR_TX1_UHB
50_XCVR_FBR0_1
50_XCVR_FBR0_2
50_XCVR_FBR1_1
50_XCVR_FBR1_2
50_GNSS_L1
50_XCVR_RX2_UHB_PRX
50_XCVR_RX6_MB_UHB_PRX
50_XCVR_RX7_MB_UHB_PRX
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
50_XCVR_RX11_MLB_HB_PRX
50_XCVR_RX12_MLB_HB_PRX
50_XCVR_RX13_LB_MLB_PRX
50_XCVR_RX14_LB_MLB_PRX
50_XCVR_RD3_MB_UHB_DRX
50_XCVR_RD4_MB_UHB_DRX
50_XCVR_RD5_MLB_HB_DRX
50_XCVR_RD6_MLB_HB_DRX
50_XCVR_RD7_MLB_HB_DRX
50_XCVR_RD8_MLB_HB_DRX
50_XCVR_RD9_MB_UHB_DRX
50_XCVR_RD10_LB_MLB_DRX
VDD_SIM1
SIM1_IO
SIM1_CLK
SIM1_RST
SIM1_DETECT
VDD_SIM2
SIM2_IO
SIM2_CLK
SIM2_RST
SIM2_DETECT
VDD_IO_1V2
PP_VDD_MAIN
PP1V8_S2
APPMU_TO_BBPMU_ON
AP_TO_BB_COREDUMP_TRIG_1V2
BB_TO_AP_RESET_DETECT_1V2_L
AP_TO_BBPMU_FORCE_PWM
90_PCIE_AP_TO_BB_TX_P
90_PCIE_AP_TO_BB_TX_N
90_PCIE_BB_TO_AP_TX_P
90_PCIE_BB_TO_AP_TX_N
90_PCIE_AP_TO_BB_REFCLK_P
90_PCIE_AP_TO_BB_REFCLK_N
PCIE_AP_TO_BB_PERST_1V2_L
PCIE_AP_BI_BB_CLKREQ_1V2_L
PCIE_BB_TO_APPMU_WAKE_1V2_L
UART_AOP_TO_BB_TXD
UART_BB_TO_AOP_TXD
RADIO_MLB_ICE
UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2
SPMI_AP_TO_RADIOS_CLK
SPMI_AP_TO_RADIOS_DATA
SWD_AOP_TO_MANY_SWDCLK
SWD_AOP_BI_BB_SWDIO
BB_TO_AP_GSM_TXBURST
DOTARA_TO_BBPMU_CLK_EN
BBPMU_TO_DOTARA_CLK_38MHZ
RFFE_LAA_VIO
RFFE_LAA_LAT_DATA
RFFE_LAA_LAT_CLK
50_LAA_TO_XCVR_UAT
50_LAA_TO_XCVR_LAT
BB_TO_R1_COEX
R1_TO_BB_LAA_SW_CTRL
I2S_BB_TO_AP_BCLK
I2S_BB_TO_AP_LRCLK
I2S_BB_TO_AP_DIN
I2S_AP_TO_BB_DOUT
VRF_DIG_0V9
VRF_LO_1V15
PP_VDD_MAIN
PP1V8_S2
GPIO_PMU_TO_BBPMU_RESET_L
GPIO_AP_TO_BB_COREDUMP_1V2
GPIO_AP_FROM_BB_RESET_DETECT_1V2_L
IO_TOUCH_TO_MANY_SCAN_ACTIVE
90_PCIE4_AP_TO_BB_TX_P
90_PCIE4_AP_TO_BB_TX_N
90_PCIE4_AP_FROM_BB_RX_P
90_PCIE4_AP_FROM_BB_RX_N
90_PCIE4_AP_TO_BB_REFCLK_P
90_PCIE4_AP_TO_BB_REFCLK_N
PCIE4_AP_TO_BB_PERST_1V2_L
PCIE4_AP_BI_BB_CLKREQ_1V2_L
GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L
UART2_AOP_TO_BB_TXD
UART2_AOP_FROM_BB_RXD
UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2
SPMI1_AOP_TO_RF_CLK
SPMI1_AOP_BI_RF_DATA
SWD_NUB_TO_MANY_SWCLK
SWD_AP_BI_BB_SWDIO
GPIO_BB_TO_MANY_GSM_BURST_IND
GPIO_DOTARA_TO_BBPMU_CLK_EN
CLK_BBPMU_TO_DOTARA_38M4_1V3
RFFE_LAA_VIO
RFFE_LAA_LAT_DATA
RFFE_LAA_LAT_CLK
50_LAA_TO_XCVR_UAT
50_LAA_TO_XCVR_LAT
IO_BB_TO_R1_COEX
R1_TO_BB_LAA_SW_CTRL
I2S2_AP_FROM_BB_BCLK
I2S2_AP_FROM_BB_LRCLK
I2S2_AP_FROM_BB_DIN
I2S2_AP_TO_BB_DOUT
C8005
120PF
5%
25V
C0G
01005
C431_K
27PF
5%
16V
NP0-C0G
01005-1
BBPMU
NOSTUFF
CONN DIFF N104/D4x

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

DOE_HIER_NFC

LAST_MODIFICATION=Tue May 28 17:48:04 2019

N104 (RTM6.3) MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00033	1	CAP,CER,C0G,680PF,2%,25V,0201	C7514_S	NFC_RTM63
131S0731	1	CAP,CER,C0G,100PF,2%,50V,0201	C7512_S	NFC_RTM63
152S01028	1	IND,WW,84NH,2.5%,1.1A,0402	L7500_S	NFC_RTM63
152S01028	1	IND,WW,84NH,2.5%,1.1A,0402	L7501_S	NFC_RTM63

D42 (RTM6.1) MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S00033	1	CAP,CER,C0G,680PF,2%,25V,0201	C7514_S	NFC_RTM61
152S01116	1	IND,MULT,82NH,2.5%,0402	L7500_S	NFC_RTM61
152S01116	1	IND,MULT,82NH,2.5%,0402	L7501_S	NFC_RTM61

D43 (RTM6.2) MATCHING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0882	1	CAP,CER,C0G,390PF,2%,25V,0201	C7514_S	NFC_RTM62
131S00017	1	CAP,CER,C0G,47PF,2%,50V,0201	C7550_S	NFC_RTM62
131S00017	1	CAP,CER,C0G,47PF,2%,50V,0201	C7551_S	NFC_RTM62
152S01117	1	IND,MULT,91NH,2.5%,0.55A,0402	L7500_S	NFC_RTM62
152S01117	1	IND,MULT,91NH,2.5%,0.55A,0402	L7501_S	NFC_RTM62

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00077	197S00206	BOM_TABLE_ALTS	Y7500_S	XTAL,27P12 MHZ
197S00076	197S00206	BOM_TABLE_ALTS	Y7500_S	XTAL,27P12 MHZ

16 13 IN — PP_VDD_MAIN — VOLTAGE=3.8
16 13 — PP1V8_NFC_S2 — VOLTAGE=1.8
16 13 IN — PP1V8_S4 — VOLTAGE=1.8V

16 13 IO — I2C_R1_TO_NFC_SCL
16 13 IO — I2C_R1_BI_NFC_SDA
16 13 IO — I2C_BT_TO_NFC_SCL
16 13 IO — I2C_BT_BI_NFC_SDA

16 13 IO — SPMI1_AOP_TO_RF_CLK
16 13 IO — SPMI1_AOP_BI_RF_DATA

16 13 IN — GPIO_PMU_TO_NFC_EN
16 13 OUT — GPIO_AOP_FROM_NFC_HOST_WAKE
16 13 IN — GPIO_AP_TO_NFC_DEV_WAKE

16 13 IN — UART4_AP_TO_NFC_TXD
16 13 OUT — UART4_AP_FROM_NFC_RXD
16 13 IN — UART4_AP_TO_NFC_RTS_L
16 13 OUT — UART4_AP_FROM_NFC_CTS_L

16 13 OUT — GPIO_SE_TO_BT_PKT_RDY

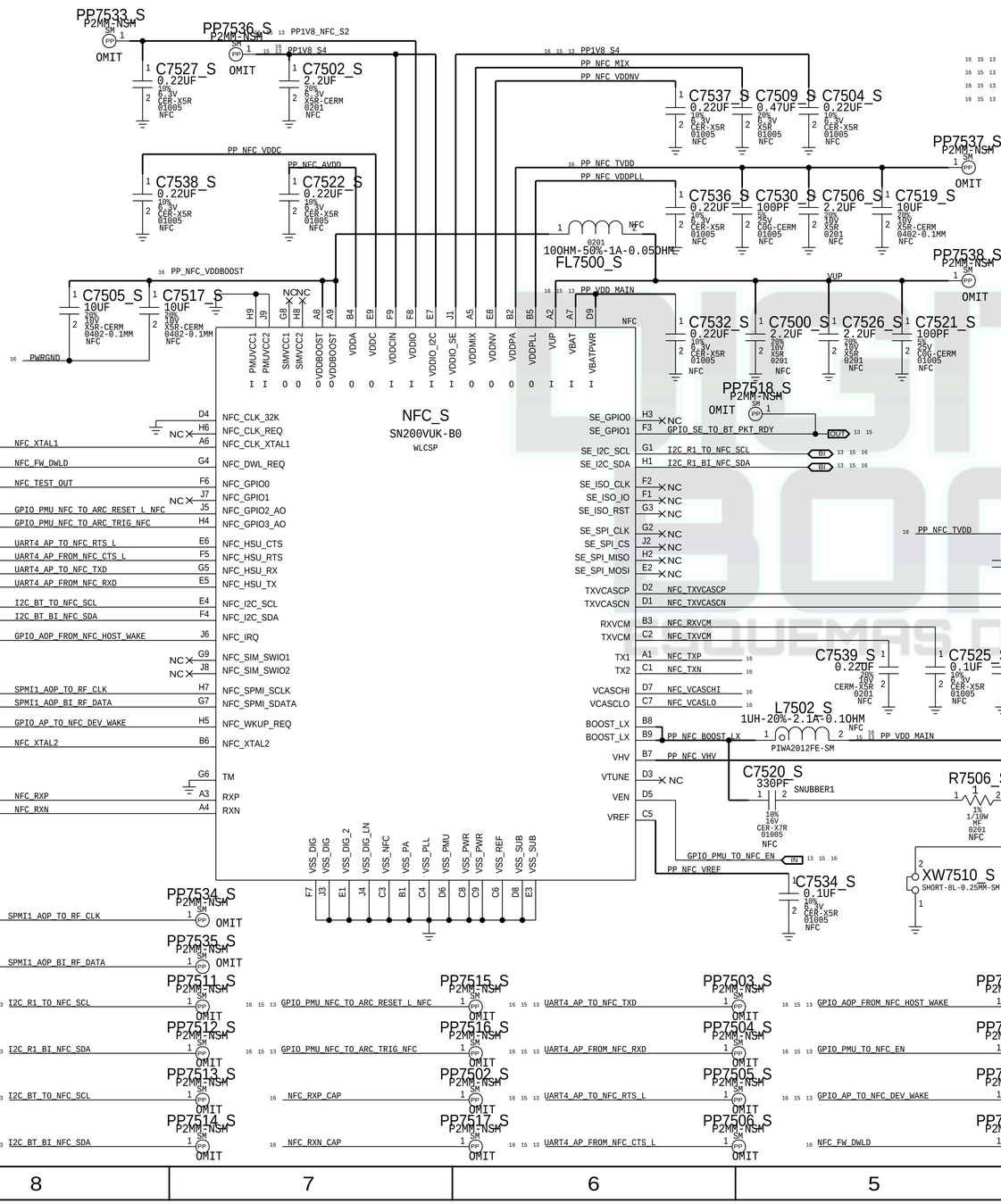
16 13 OUT — GPIO_PMU_NFC_TO_ARC_RESET_L_NFC
16 13 OUT — GPIO_PMU_NFC_TO_ARC_TRIG_NFC

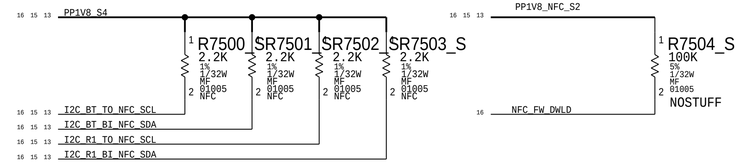
16 13 IO — NFC_ANT

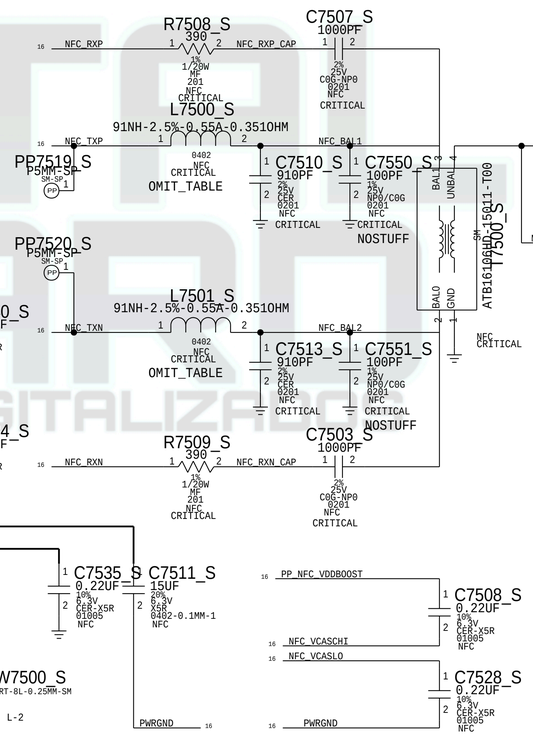
STOCKHOLM

NFC CONTROLLER

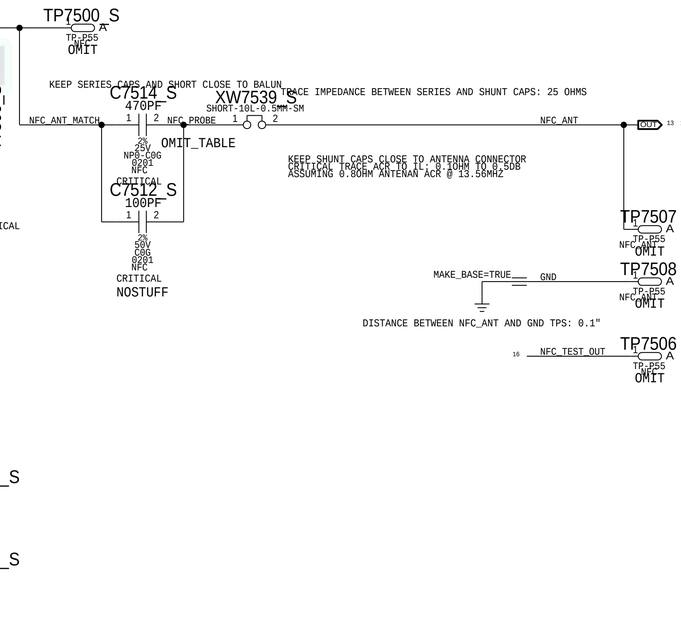
	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
	P PWR_SHAPE	NFC_ANT*, NFC_TX*, NFC_BAL*, NFC_PROBE*
	P PWR_300UM	PP_NFC*
	P PWR_200UM	NFC_RX*, NFC_VCAS*
	P PWR_SHAPE	VUP







NFC FRONT END



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

ARROW MLB

LAST_MODIFICATION=Tue May 28 17:48:04 2019

POWER
- 18 13 PP1V8_S4
- 18 13 IO PP1V0_R1_ANA_S4
- 18 13 IO PP1V0_R1_SOC_S4

HOST IPC
- 18 13 IO SPI0_AOP_TO_IMU_R1_SCLK
- 18 13 IO GPIO_AOP_TO_R1_SPI_CS_L
- 18 13 IO SPI0_AOP_FROM_IMU_R1_MISO
- 18 13 IO SPI0_AOP_TO_IMU_R1_MOSI
- 18 13 IO GPIO_AOP_TO_R1_COREDUMP_TRIGGER
- 18 13 IO GPIO_AOP_FROM_R1_INT

RESET/CLOCK
- 18 13 IO GPIO_PMU_TO_R1_RESET_L
- 18 13 IO GPIO_PMU_TO_WLAN_R1_32K_CLK
- 18 13 IO GPIO_AOP_TO_R1_TIME_SYNC

DEBUG
- 18 13 IO SWD_NUB_TO_MANY_SWCLK
- 18 13 IO SWD_NUB_BI_R1_SWDIO

SPMI/COEX GPIOS
- 18 13 IO IO_R1_TO_WLAN_COEX
- 18 13 IO IO_BB_TO_R1_COEX
- 18 13 IO IO_WLAN_TO_R1_COEX

SE IPC
- 18 13 IO I2C_R1_TO_NFC_SCL
- 18 13 IO I2C_R1_BI_NFC_SDA

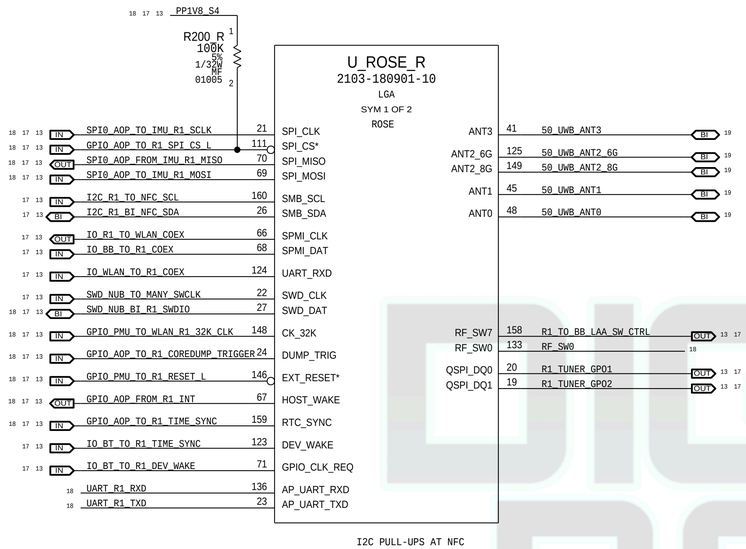
BT TIME SYNC / WAKE
- 18 13 IO IO_BT_TO_R1_TIME_SYNC
- 18 13 IO IO_BT_TO_R1_DEV_WAKE

ANTENNA SWITCH CTRL
- 18 13 IO R1_TUNER_GPO1
- 18 13 IO R1_TUNER_GPO2
- 18 13 IO R1_TO_BB_LAA_SW_CTRL

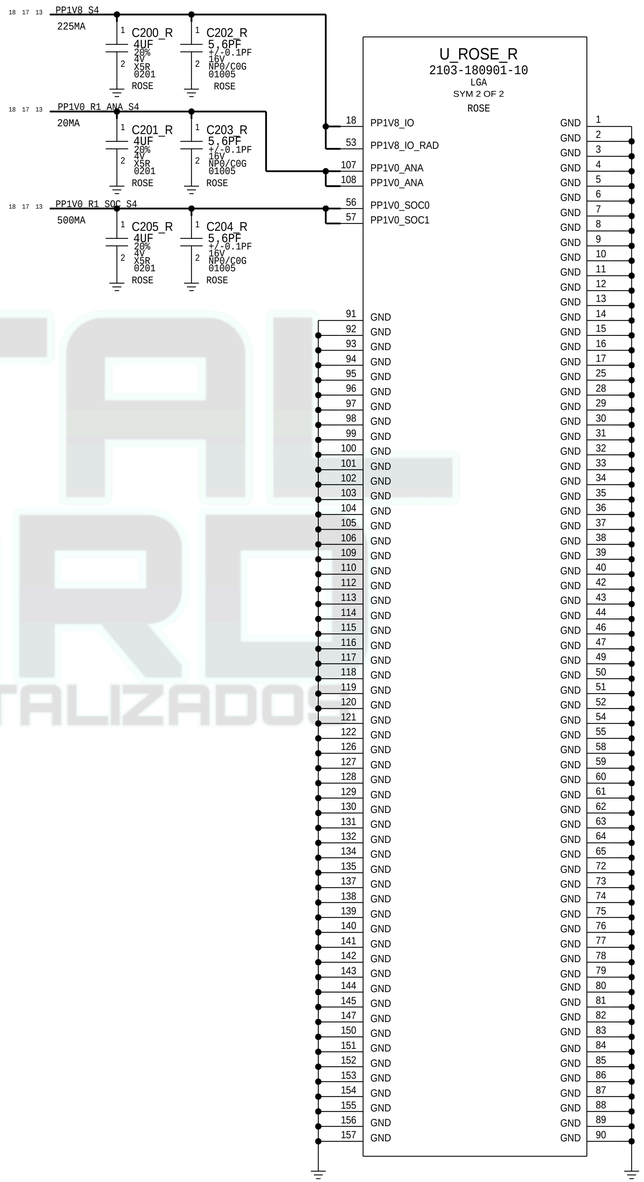
ANTENNA
- 19 13 IO 50_R1_AOA0
- 19 13 IO 50_R1_AOA1
- 19 13 IO 50_R1_AOA3
- 19 13 IO 50_R1_ANT_CH9
- 19 13 IO 50_LAA_TO_R1

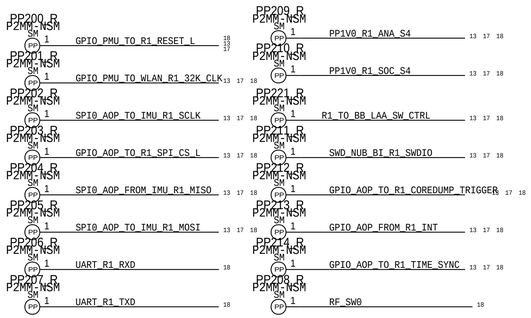
SCH #: 951-07279
PCB #: 920-05369
BOM #: 939-05686

MODULE

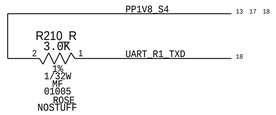


I2C PULL-UPS AT NFC

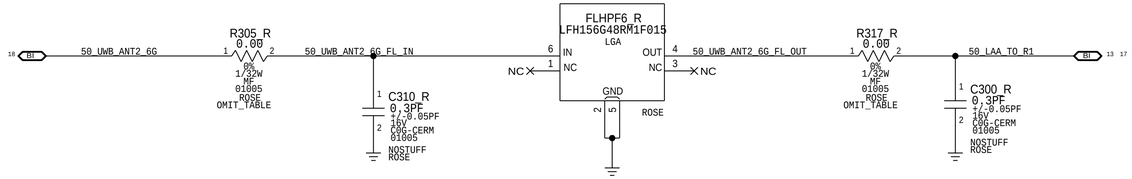


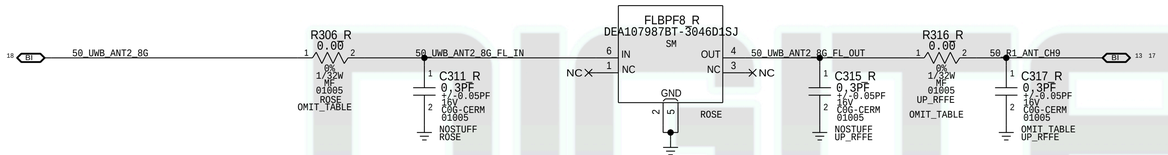


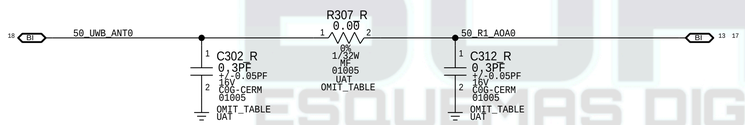
UNSECURE BOOT BOOTSTRAP PULLUP

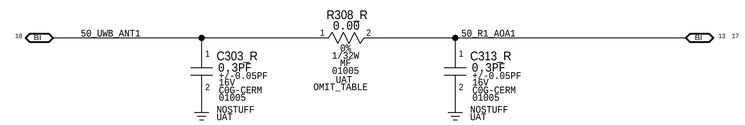


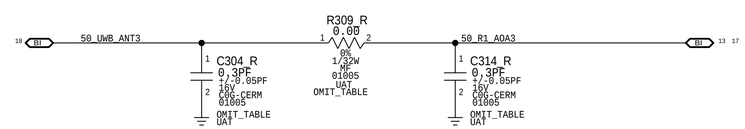
FILTERS/MATCHING AND ANTENNA











DOMAIN (P.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
	P A_50_WIDE_SE	50_R1*, 50_UWB*, 50_LAA_TO_R1*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CUSTOMIZE
CLASS NAME		CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE		S A_DIELECTRIC_2X_50_WIDE_SE	50_R1*, 50_UWB*, 50_LAA_TO_R1* ?	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0161	1	RES,MF,0 OHM,1/32W,01005	R305_R	ROSE.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R317_R	ROSE.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R306_R	ROSE.X
152S01109	1	IND,FILM,0.6NH,950MA,01005	R316_R	ROSE.X
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C317_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C304_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C314_R	ROSE.X
152S01109	1	IND,FILM,0.6NH,950MA,01005	R309_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C303_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C313_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C302_R	ROSE.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C312_R	ROSE.X
152S00494	1	IND,FILM,0.8NH,900MA,01005	R307_R	ROSE.X
152S00494	1	IND,FILM,0.8NH,900MA,01005	R308_R	ROSE.X
131S0369	1	CAP,CER,C0G,0.5PF,16V,01005	C315_R	ROSE.X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00497	1	IND,FILM,0.5NH,1000MA,01005	R305_R	ROSE.0
152S00497	1	IND,FILM,0.5NH,1000MA,01005	R317_R	ROSE.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R306_R	ROSE.0
152S00492	1	IND,FILM,1.0NH,900MA,01005	R316_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C317_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C304_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C314_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R309_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R308_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C302_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C312_R	ROSE.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R307_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C303_R	ROSE.0
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C313_R	ROSE.0
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C315_R	ROSE.0

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00664	339S00665	ALT_PARTS	U_ROSE_R	MODULE,STRIDER,ES5.1

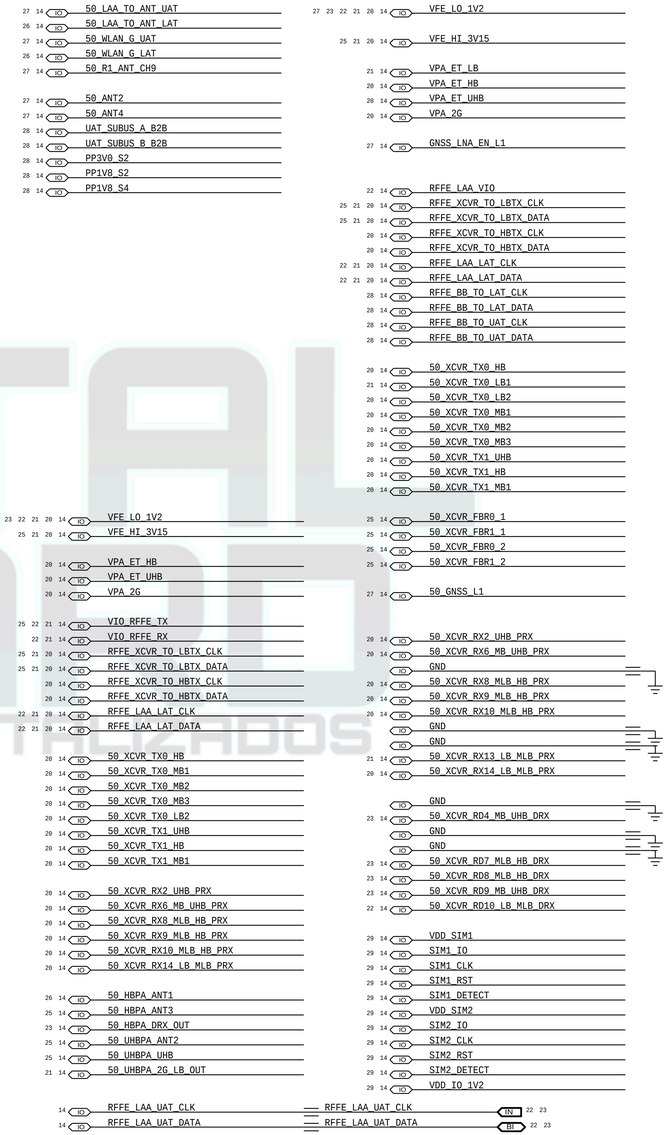
1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN MHZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

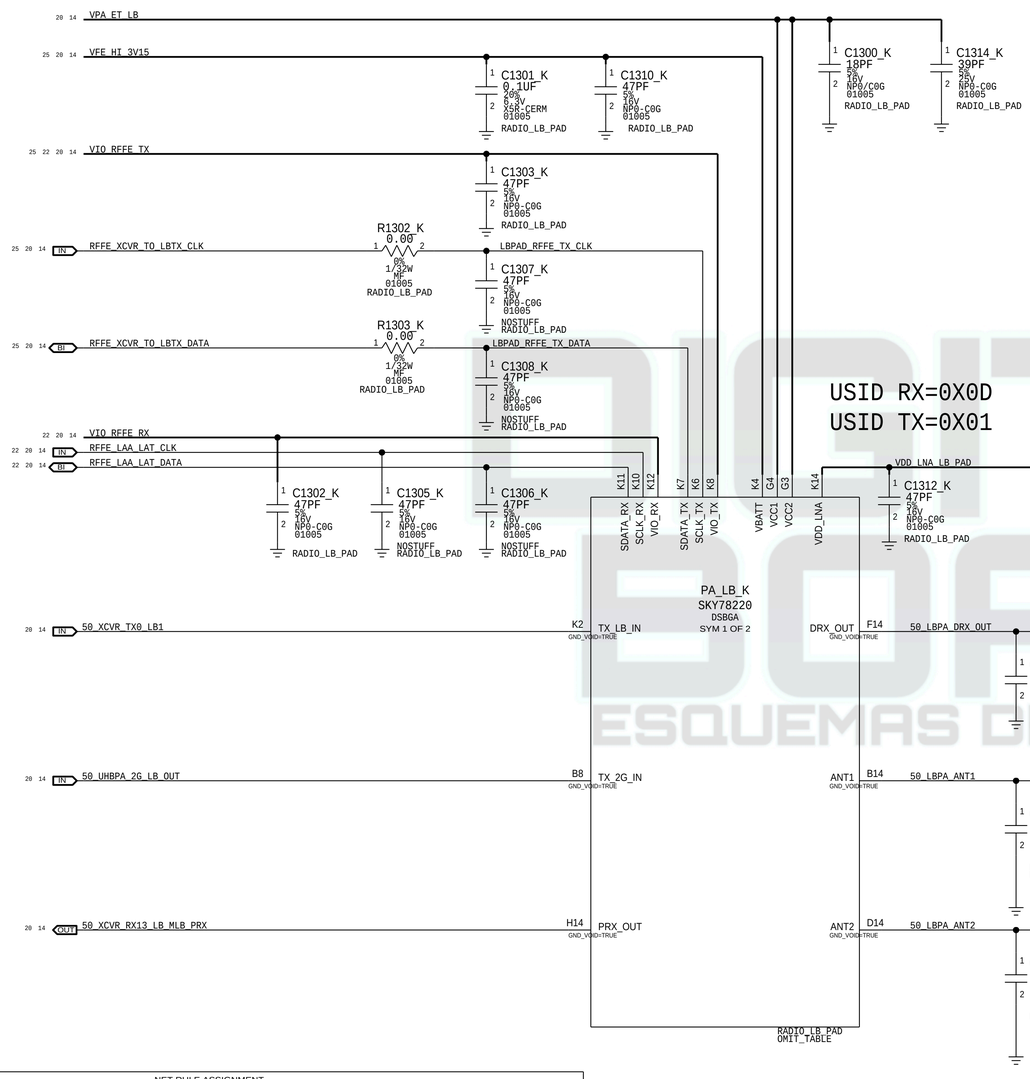
ICE19.0 RADIO_MLB_FF

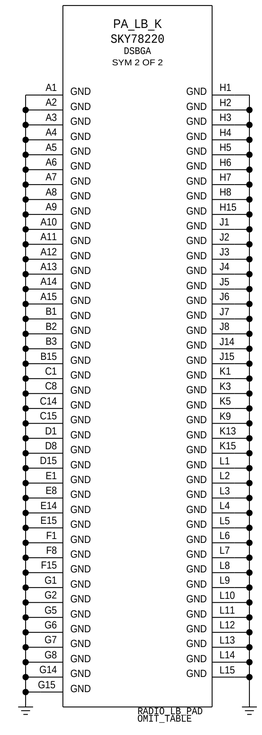
LAST_MODIFICATION=Tue May 28 18:07:13 2019

PAGE	CSA	CONTENTS	SYNC	DATE
20	1	SCH,RADIO_MLB_ICE_FF		01/17/2018
21	2	LB SPAD		04/05/2018
22	3	LB DIVERSITY RECEIVE LNA		04/05/2018
23	4	HB DIVERSITY RECEIVE LNA		01/17/2018
24	5	MIMO RECIEVE LNA		01/17/2018
25	6	LOWER & UPPER COUPLER		01/17/2018
26	7	LOWER ANTENNA FEEDS		01/17/2018
27	8	UPPER ANTENNA FEEDS		01/17/2018
28	9	ANTENNA SYSTEM		01/17/2018
29	10	SIM		



LB SPAD





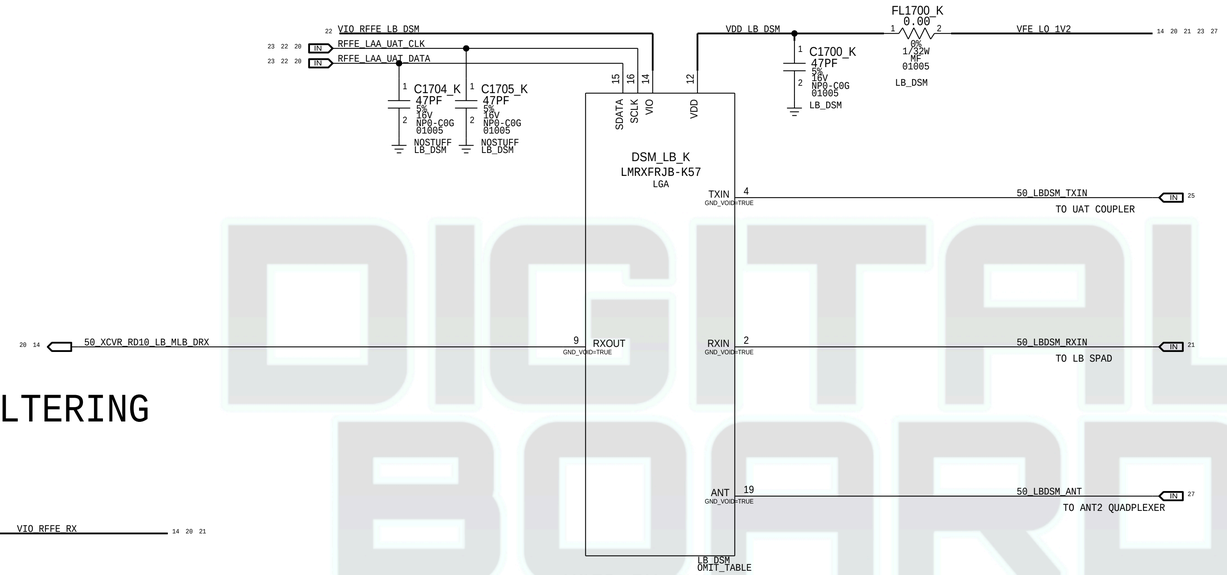
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01907	1	SKY78220-11	PA_LB_K	ROW
353S01908	1	SKY78223-11	PA_LB_K	USCH

DOMAIN (E.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_UHBPA_2G_LB_OUT*, 50_LBPA_DRX_OUT
P	A_50_THIN_SE	50_LBPA_ANT*, 50_LB_TX_ANT1*
P	A_50_WIDE_SE	50_LBPA_TX

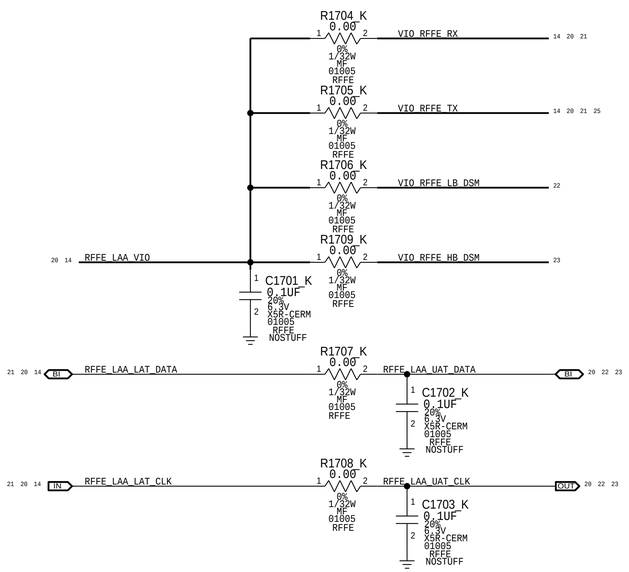
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	S=S T=T	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_UHBPA_2G_LB_OUT*, 50_LBPA_DRX_OUT	Y
50_THIN	S	A_DIELECTRIC_2X	50_LBPA_ANT*, 50_LB_TX_ANT1*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_LBPA_TX	Y

DOMAIN (E.P.S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VDD_LNA_LB_PAD

LB DIVERSITY RECEIVE LNA



RFFE FILTERING



USID RX=0X0A

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01922	1	MURATA, LMRXFRJB-K57 ES1.0	DSM_LB_K	ROW
353S01923	1	MURATA, LMRXFRJB-K69 ES1.0	DSM_LB_K	USCH

DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_WIDE_SE	50_LBDSM_RXIN
P	A_50_THIN_SE	50_LBDSM_TX*, 50_LBDSM_RXOUT*, 50_LBDSM_ANT*
P	A_50_THIN_SE	50_LBDSM_RXIN_M

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	(S)HIELD (D)IFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_LBDSM_RXIN	Y
50_THIN	S	A_DIELECTRIC_2X	50_LBDSM_TX*, 50_LBDSM_RXOUT*, 50_LBDSM_ANT*	Y
50_THIN	S	A_DIELECTRIC_2X	50_LBDSM_RXIN_M	Y

DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VDD_LB_DSM

HB DIVERSITY RECEIVE LNA

DECOUPLING SHARED WITH LB DSM

22 VIO_RFFE_HB_DSM

22 20 IN RFFE_LAA_UAT_CLK

22 20 BI RFFE_LAA_UAT_DATA

C1801_K 47PF 5% 16V NP0-C0G 01005 HB_DSM

C1800_K 47PF 5% 16V NP0-C0G 01005 NOSTUFF HB_DSM

C1803_K 47PF 5% 16V NP0-C0G 01005 NOSTUFF HB_DSM

SDATA 11 SCLK 12 VIO 10 VDD 9

VDD_HB_DSM

C1802_K 0.1UF 20% 6.3V X5R-CERM 01005 HB_DSM

R1801_K 0.00 0% 1/32W MF 01005 HB_DSM

VFE_LO_1V2 14 20 21 22 27

DSM_HB_K SKYI3789 LGA SYM 1 OF 2

UHB_TX_IN 14 GND_VOID=TRUE 50_HBDSM_UHB_TXIN FROM UAT COUPLER IN 25

20 14 OUT 50_XCVR_RD4_MB_UHB_DRX 28 RXOUT_DRX1 GND_VOID=TRUE

UHB_ANT1 17 GND_VOID=TRUE 50_HBDSM_UHB_ANT1

R1821_K 5.6PF +/-0.1PF 16V NP0-C0G-CERM 01005 HB_DSM

50_ANT4_UHB IN 27 TO ANT4

L1811_K 3.3NH-+/-0.1NH-0.4A-0.25OHM 01005 HB_DSM

L1803_K 1.3PF +/-0.05PF 16V C0G 01005 NOSTUFF HB_DSM

20 14 OUT 50_XCVR_RD8_MLB_HB_DRX 2 RXOUT_DRX2 GND_VOID=TRUE

MHB_ANT1 20 GND_VOID=TRUE 50_HBDSM_MHB_ANT1

R1804_K 1.6NH-+/-0.1NH-0.70A 01005 HB_DSM

50_ANT2_MLB_MB_HB IN 27 TO ANT2

L1802_K 4.7NH-3%-0.270A 01005 NOSTUFF HB_DSM

L1810_K 0.5PF +/-0.05PF 16V C0G-CERM 01005 HB_DSM

20 14 OUT 50_XCVR_RD7_MLB_HB_DRX 4 RXOUT_DRX3 GND_VOID=TRUE

MHB_RX_IN 25 GND_VOID=TRUE 50_HBDSM_MHB_RX_IN

R1806_K 0.00 0% 1/32W MF 01005 HB_DSM

50_HBPA_DRX_OUT IN 14 20 TO HB SPAD

L1805_K 4.7NH-3%-0.270A 01005 NOSTUFF HB_DSM

L1807_K 4.7NH-3%-0.270A 01005 NOSTUFF HB_DSM

20 14 OUT 50_XCVR_RD9_MB_UHB_DRX 6 RXOUT_DRX4 GND_VOID=TRUE

MHB_TX_IN 23 GND_VOID=TRUE 50_HBDSM_MHB_TXIN FROM UAT COUPLER IN 25

HB_DSM OMIT_TABLE

USID RX=0X0B

DSM_HB_K SKYI3789 LGA SYM 2 OF 2

GND 1, 3, 5, 7, 8, 13, 15, 16, 18, 19, 21, 22, 24, 26, 27

HB_DSM OMIT_TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S01916	1	SKY13789-13	DSM_HB_K	ROW
353S01909	1	SKY13799-12	DSM_HB_K	USCH

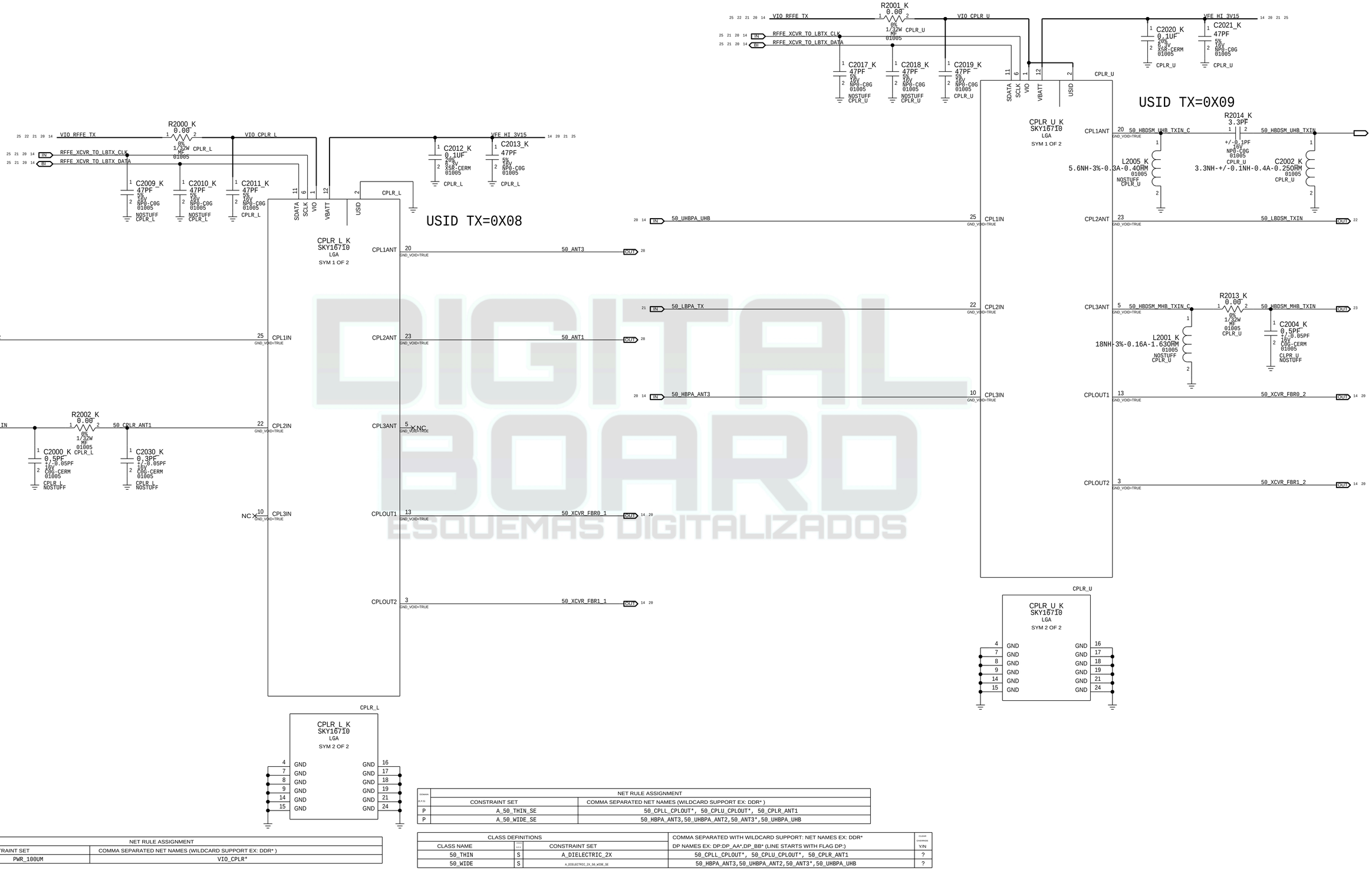
DOMAIN / P,F,S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_HBDSM_RXOUT*, 50_HBDSM_MHB_RX_IN
P	A_50_THIN_SE	50_HBDSM_MHB_TXIN*, 50_HBDSM_UHB_TXIN*
P	A_50_WIDE_SE	50_HBPA_DRX_OUT*
P	A_50_THIN_SE	50_HBDSM_MHB_ANT*, 50_HBDSM_UHB_ANT*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	P,F,S	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_HBDSM_RXOUT*, 50_HBDSM_MHB_RX_IN	Y
50_THIN	S	A_DIELECTRIC_2X	50_HBDSM_MHB_TXIN*, 50_HBDSM_UHB_TXIN*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_HBPA_DRX_OUT*	Y
50_THIN	S	A_DIELECTRIC_2X	50_HBDSM_MHB_ANT*, 50_HBDSM_UHB_ANT*	Y

DOMAIN / P,F,S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VDD_HB_DSM

MIMO DSM NOT APPLICABLE TO ICE19.0

LOWER/UPPER COUPLER

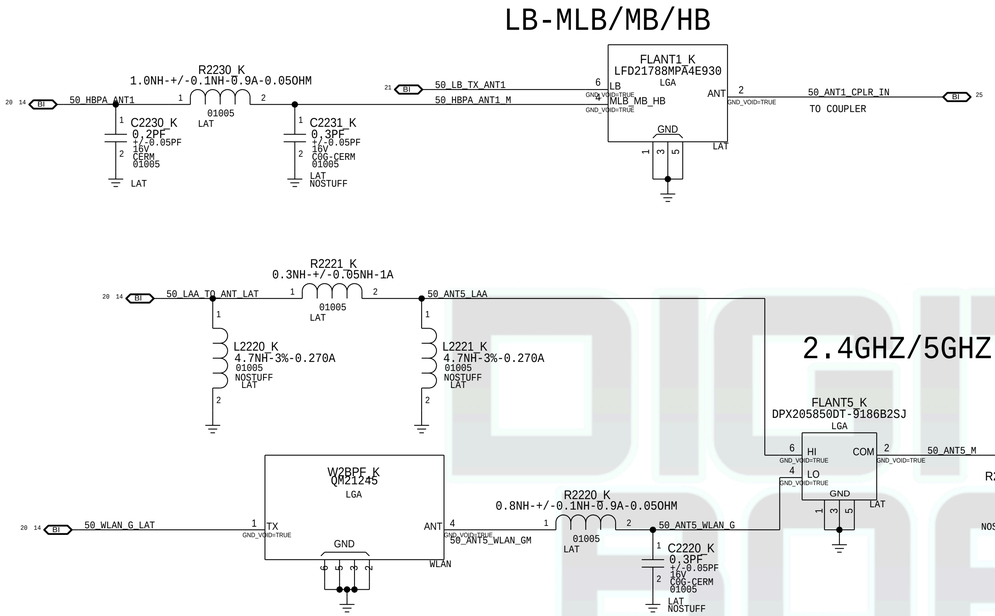


DOMAIN / P, N	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	VIO_CPLR*

DOMAIN / P, N	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_CPLL_CPLOUT*, 50_CPLU_CPLOUT*, 50_CPLR_ANT1
P	A_50_WIDE_SE	50_HBPA_ANT3,50_UHBPA_ANT2,50_ANT3*,50_UHBPA_UHB

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	DIFF P,N	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_CPLL_CPLOUT*, 50_CPLU_CPLOUT*, 50_CPLR_ANT1	?
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_HBPA_ANT3,50_UHBPA_ANT2,50_ANT3*,50_UHBPA_UHB	?

LOWER ANTENNA FEEDS



UAT ANTENNAS

ANT2	ANT4
LB	R1
LMB/MB/HB	5GHZ
L1 GNSS	UHB
2.4GHZ	

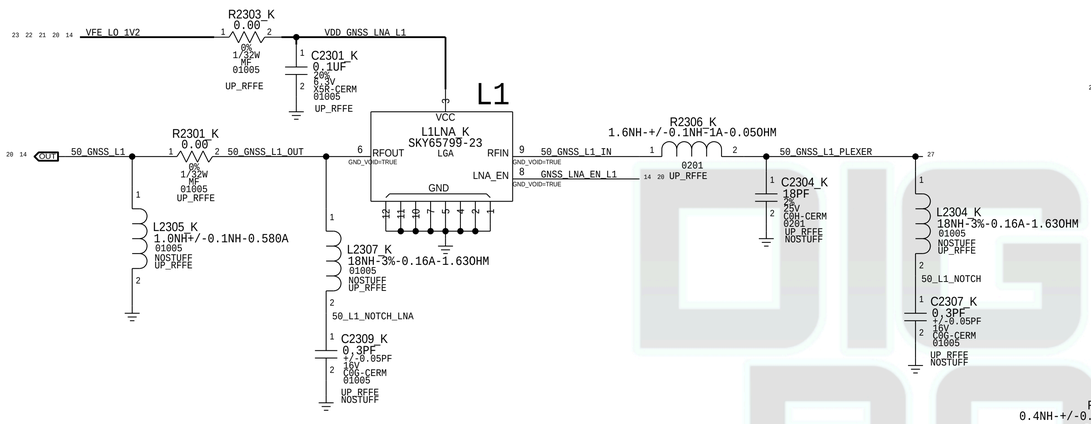
LAT ANTENNAS

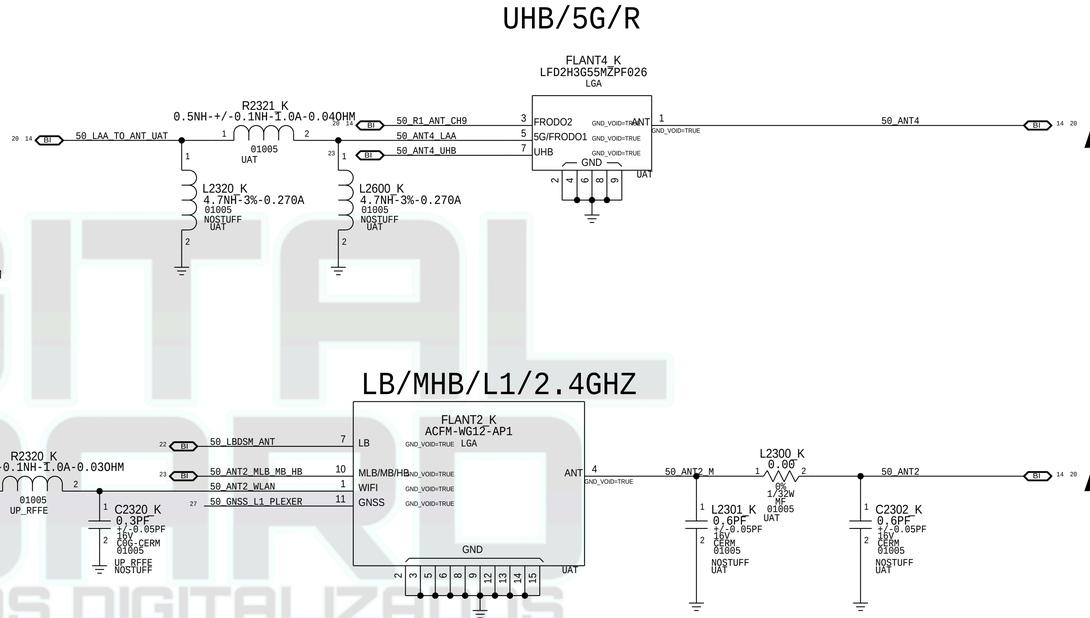
ANT1	ANT3	ANT5
LB	UHB	2.4GHZ
LMB/MB/HB		5GHZ

DOMAIN (C,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_ANT1_CPLR_IN, 50_HBPA_ANT1*
P	A_50_WIDE_SE	50_ANT1, 50_ANT5*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_ANT1_CPLR_IN, 50_HBPA_ANT1*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT1, 50_ANT5*	Y

UPPER ANTENNA FEEDS





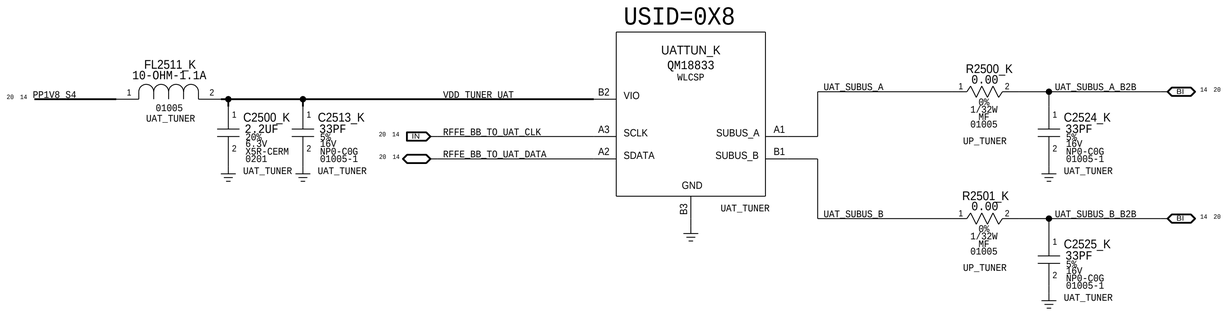
DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_L1*, 50_GNSS_L1*, 50_LAA_TO_ANT_UAT, 50_ANT2_MLB_MB_HB, 50_ANT4_UHB
P	A_50_WIDE_SE	50_ANT2, 50_ANT2_M, 50_ANT2_WLAN, 50_ANT4, 50_ANT4_LAA

DOMAIN (P,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VDD_GNSS_LNA*

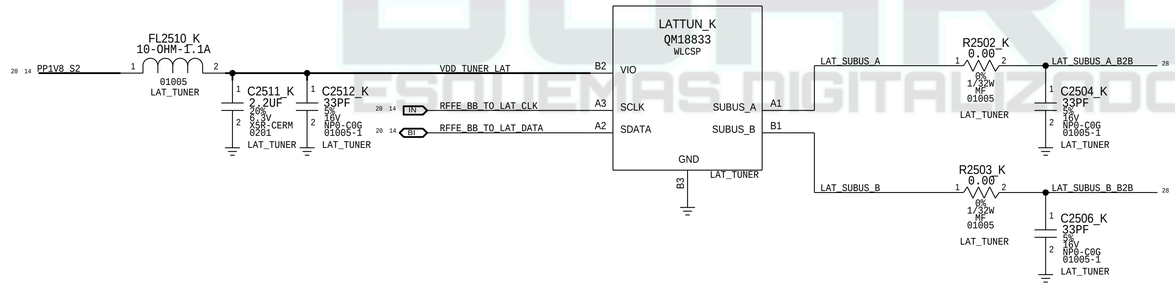
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DIAGNOSE
CLASS NAME	TYPE (P,P,S)	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN	S	A_DIELECTRIC_2X	50_L1*, 50_GNSS_L1*, 50_LAA_TO_ANT_UAT, 50_ANT2_MLB_MB_HB, 50_ANT4_UHB	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_ANT2, 50_ANT2_M, 50_ANT2_WLAN, 50_ANT4, 50_ANT4_LAA	Y

ANTENNA SYSTEM

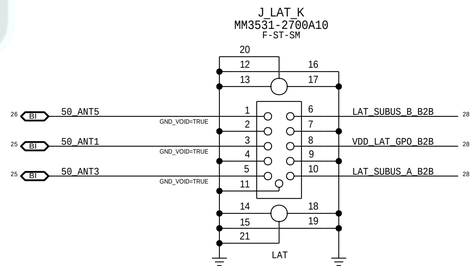
UAT SUBUS



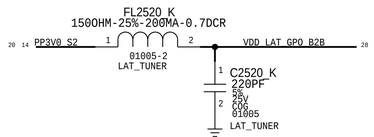
LAT SUBUS



LAT



FL2520_K



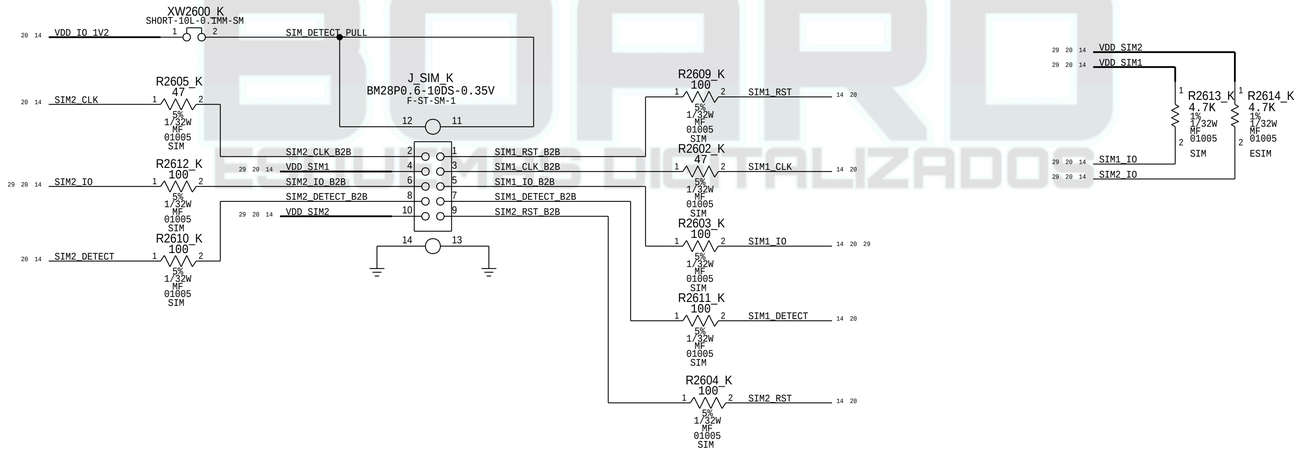
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CHANGE
CLASS NAME	DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD	S	A_DIELECTRIC_2X	LAT_SUBUS*, UAT_SUBUS*	Y

DOMAIN P-P-SI	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_200UM	VDD_TUNER_*, VDD_LAT_GPO*
P	PWR_100UM	LAT_SUBUS*, UAT_SUBUS*

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0158	1	100K RES 5%, 01005	R508_K	ICE19.0

PULL-UP SIM2 DETECT

SIM FLEX



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

ICE19 RADIO_MLB DVT

LAST_MODIFICATION=Tue May 28 17:48:01 2019

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33	4	BBPMU: RAILS (2/2)		01/08/2018
34	5	BB: INTERFACE (1/3)		01/08/2018
35	6	BB: MEMORY & TRACING (2/3)		01/08/2018
36	7	BB: POWER (3/3)		01/08/2018
37	8	XCVR: TX & GNSS (1/3)		01/08/2018
38	9	XCVR: INTERFACE & PWR (2/3)		01/08/2018
39	10	XCVR: PRX DRX (3/3)		01/08/2018
40	11	ET		01/08/2018
41	12	TEST POINTS		01/08/2018

PP_VDD_MAIN
PP1V8_S2
GPIO_PMU_TO_BBPMU_RESET_L
GPIO_AP_TO_BB_COREDUMP_1V2
GPIO_AP_FROM_BB_RESET_DETECT_1V2_L
IO_TOUCH_TO_MANY_SCAN_ACTIVE

90_PCIE4_AP_FROM_BB_RX_P
90_PCIE4_AP_FROM_BB_RX_N
90_PCIE4_AP_TO_BB_TX_P
90_PCIE4_AP_TO_BB_TX_N
90_PCIE4_AP_TO_BB_REFCLK_P
90_PCIE4_AP_TO_BB_REFCLK_N

PCIE4_AP_BI_BB_CLKREQ_1V2_L
PCIE4_AP_TO_BB_PERST_1V2_L
GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L

SWD_NUB_TO_MANY_SWCLK
SWD_AP_BI_BB_SWDIO

UART2_AOP_FROM_BB_RXD
UART2_AOP_TO_BB_TXD

UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2

SPMI1_AOP_TO_RF_CLK
SPMI1_AOP_BI_RF_DATA

GPIO_BB_TO_MANY_GSM_BURST_IND

GPIO_DOTARA_TO_BBPMU_CLK_EN
CLK_BBPMU_TO_DOTARA_38M4_1V3

RFFE_LAA_VIO
RFFE_LAA_LAT_DATA
RFFE_LAA_LAT_CLK

50_LAA_TO_XCVR_UAT
50_LAA_TO_XCVR_LAT

IO_BB_TO_R1_COEX
R1_TO_BB_LAA_SW_CTRL

I2S2_AP_FROM_BB_BCLK
I2S2_AP_FROM_BB_LRCLK
I2S2_AP_FROM_BB_DIN
I2S2_AP_TO_BB_DOUT

VRF_LO_1V15
VRF_DIG_0V9

VFE_LO_1V2
VFE_HI_3V15

VPA_ET_LB
VPA_ET_HB
VPA_ET_UHB
VPA_2G

GNSS_LNA_EN_L1

RFFE_LAA_VIO
RFFE_XCVR_TO_LBTX_CLK
RFFE_XCVR_TO_LBTX_DATA
RFFE_XCVR_TO_HBTX_CLK
RFFE_XCVR_TO_HBTX_DATA
RFFE_LAA_LAT_CLK
RFFE_LAA_LAT_DATA
RFFE_BB_TO_LAT_CLK
RFFE_BB_TO_LAT_DATA
RFFE_BB_TO_UAT_CLK
RFFE_BB_TO_UAT_DATA

50_XCVR_TX0_HB
50_XCVR_TX0_LB1
50_XCVR_TX0_LB2
50_XCVR_TX0_MB1
50_XCVR_TX0_MB2
50_XCVR_TX0_MB3
50_XCVR_TX1_UHB
50_XCVR_TX1_HB
50_XCVR_TX1_MB1

50_XCVR_FBR0_1
50_XCVR_FBR1_1
50_XCVR_FBR0_2
50_XCVR_FBR1_2

50_GNSS_L1

50_XCVR_RX2_UHB_PRX
50_XCVR_RX6_MB_UHB_PRX
GND
50_XCVR_RX8_MLB_HB_PRX
50_XCVR_RX9_MLB_HB_PRX
50_XCVR_RX10_MLB_HB_PRX
GND
GND
50_XCVR_RX13_LB_MLB_PRX
50_XCVR_RX14_LB_MLB_PRX

GND
50_XCVR_RD4_MB_UHB_DRX
GND
GND
50_XCVR_RD7_MLB_HB_DRX
50_XCVR_RD8_MLB_HB_DRX
50_XCVR_RD9_MB_UHB_DRX
50_XCVR_RD10_LB_MLB_DRX

VDD_SIM1
SIM1_IO
SIM1_CLK
SIM1_RST
SIM1_DETECT
VDD_SIM2
SIM2_IO
SIM2_CLK
SIM2_RST
SIM2_DETECT
VDD_IO_1V2

BOM TABLES

XTAL ALTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S00156	197S00155	ALT_PARTS	Y301_K	XTAL, 38.4MHZ, TXC
197S00179	197S00155	ALT_PARTS	Y301_K	XTAL, 38.4MHZ, NDK

EEPROM ALTS

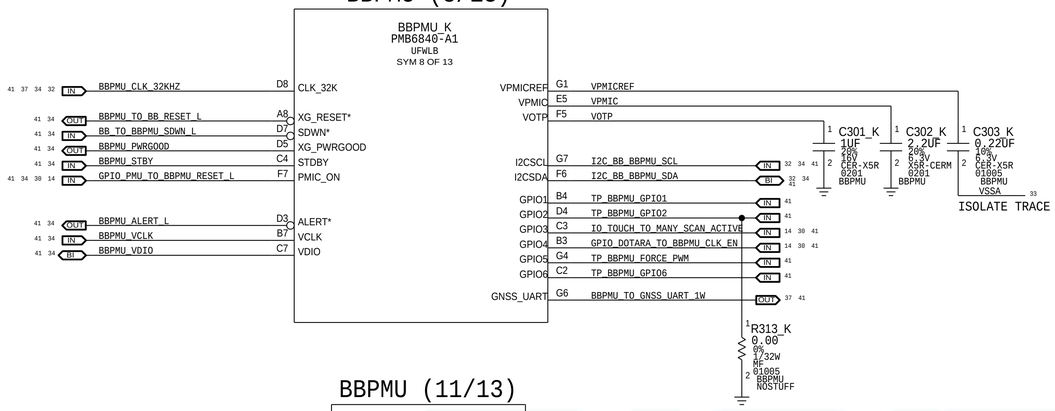
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00013	335S0894	ALT_PARTS	EEPROM_K	EEPROM,8KBIT,I2C

BBPMU ALTS

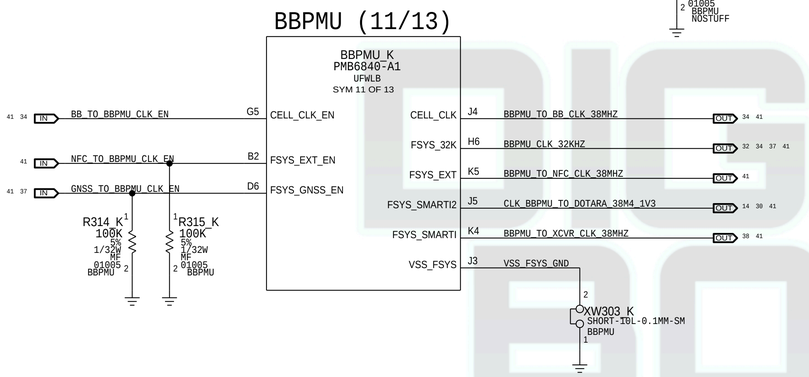
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S01141	152S01045	ALT_PARTS	L401_K,L402_K	TAIYO
152S01142	152S01043	ALT_PARTS	L405_K	TAIYO

BBPMU: CONTROL (1/2)

BBPMU (8/13)



BBPMU (11/13)



BBPMU ADC TABLES

REVISION

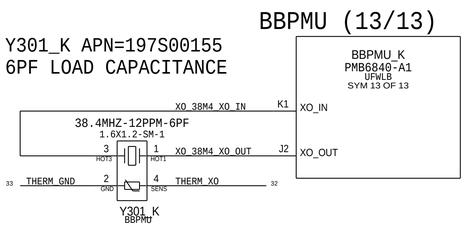
R311_K	REVISION MLB	REVISION RF DEV
0.0	PROTO0	0.1
1.2K	PROTO1	1.0
2.2K	PROTO2	2.0
3.3K	PROTO2 V2	2.1
4.7K	EVT	3.0
6.8K	CARRIER	RESERVED
8.2K	DVT	4.0
10K	PVT	5.0
12K		
15K		
18K		
22K		
27K		
33K		
39K		
47K		
56K		
82K		
100K		
120K		
150K		

HWID TABLE RDAR://36303220

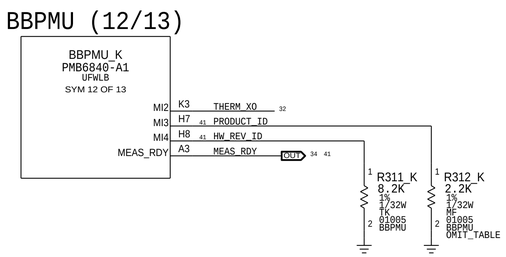
PRODUCT

R312_K	PRODUCT ID	X-CODE
0.0	RFDEV 19.1/2	
1.2K	RFDEV 19.0	
2.2K	ICE19.0 MLB	X1403
3.3K	ICE19.1 MLB	X1368
4.7K	ICE19.2 MLB	X1369
6.8K		
8.2K		
10K		
12K		
15K		
18K		
22K		
27K		
33K		
39K		
47K		
56K		
82K		
100K		
120K		
150K		

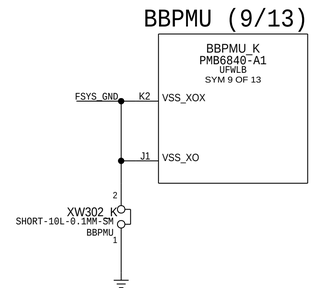
BBPMU (13/13)

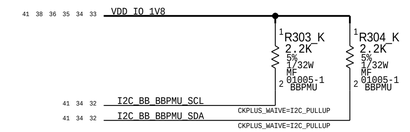


BBPMU (12/13)



BBPMU (9/13)





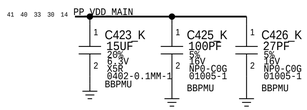
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR OVERRIDE
CLASS NAME	PREF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD	S	A_DIELECTRIC_2X	*38M*, BBPMU_CLK_32KHZ	Y
RF_SHIELD	S	A_DIELECTRIC_2X	THERM_*, FSYS_GND, VPMICREF, VSSA	Y

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RF_SHIELD	GND	DEFAULT
RF_SHIELD	RF_SHIELD	A_DIELECTRIC_2XD

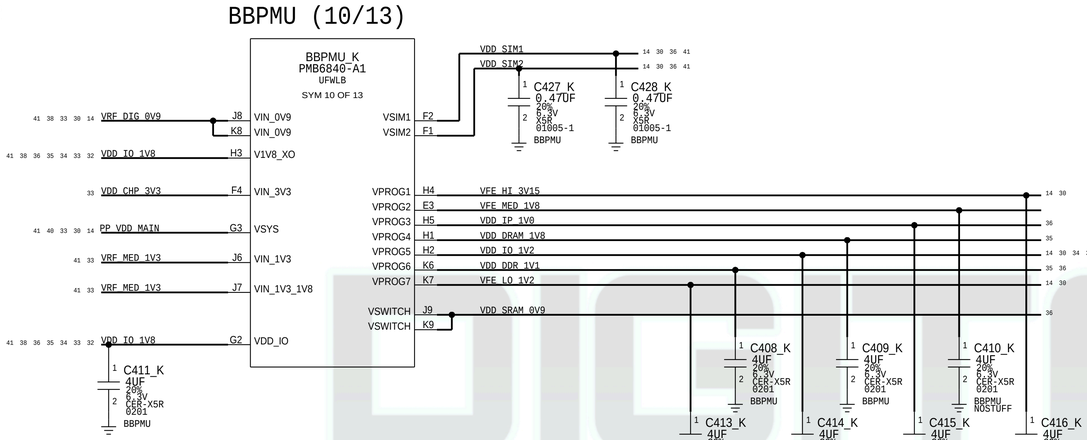
COMMA SEPARATED P,F,S	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_100UM	VPMICREF, VPMIC, VOTP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
118S00118	1	2.2K 01005 1%	R312_K	ICE19.0
118S00119	1	3.3K 01005 1%	R312_K	ICE19.1
118S0636	1	4.7K 01005 1%	R312_K	ICE19.2

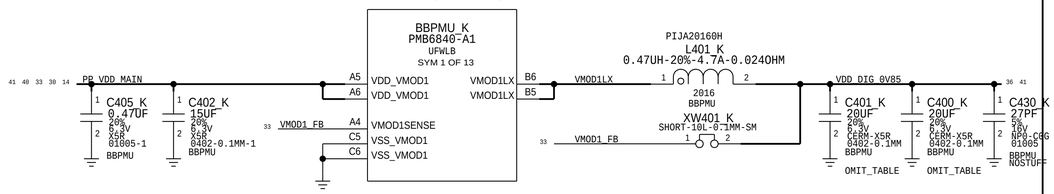
BBPMU: RAILS (2/2)



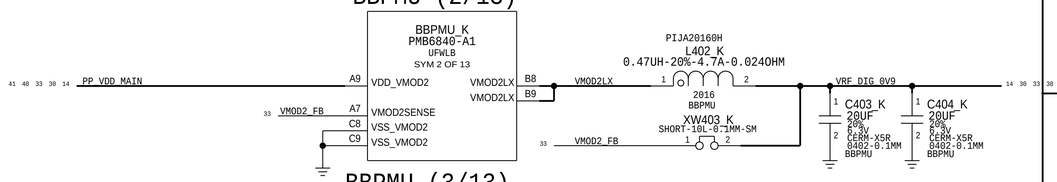
BBPMU (10/13)



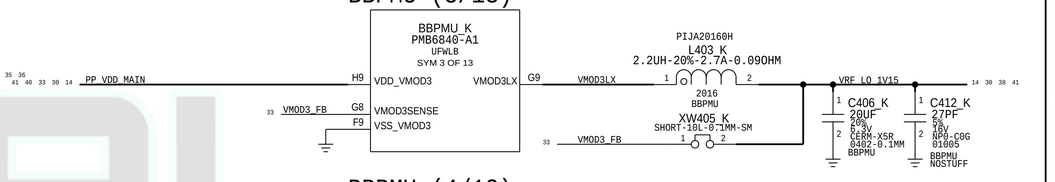
BBPMU (1/13)



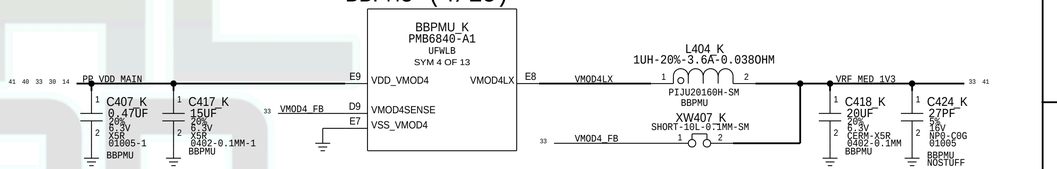
BBPMU (2/13)



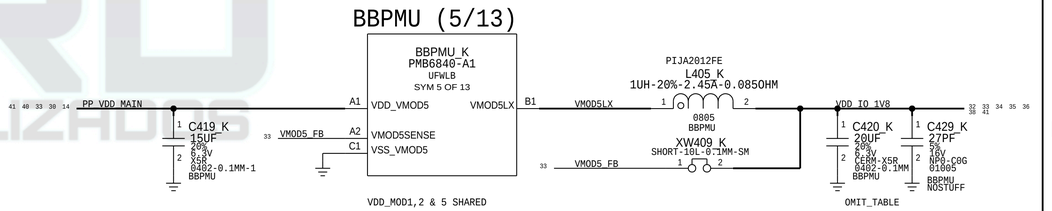
BBPMU (3/13)



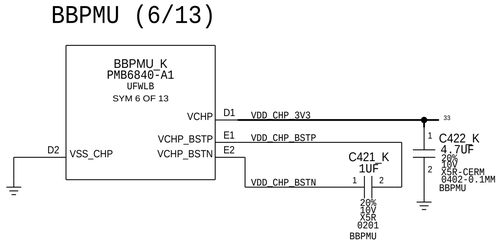
BBPMU (4/13)



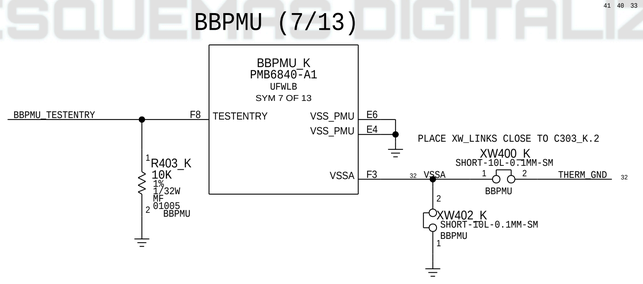
BBPMU (5/13)



BBPMU (6/13)



BBPMU (7/13)



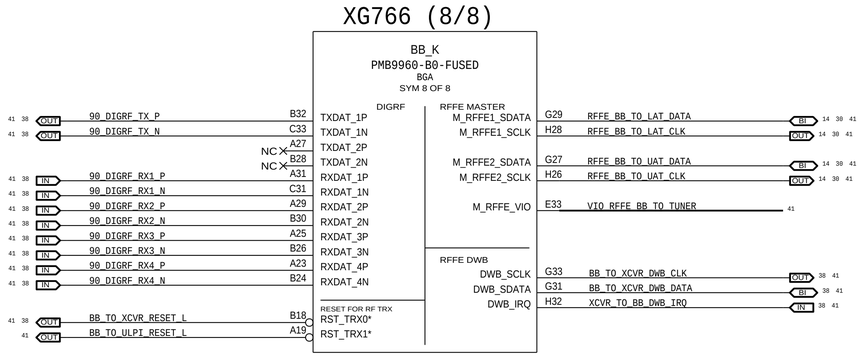
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
138S0884	1	20UF 0.7MM MAX 0402, 6.3V	C400_K,C401_K,C420_K	ICE19.0
138S00144	1	26UF 0.65MM MAX 0402, 4V	C400_K,C401_K,C420_K	ICE19.1
138S00144	1	26UF 0.65MM MAX 0402, 4V	C400_K,C401_K,C420_K	ICE19.2

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR CONVERSE
CLASS NAME	CONSTRAINT SET		DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD	S	A_DIELECTRIC_2X	VMOD*FB	Y

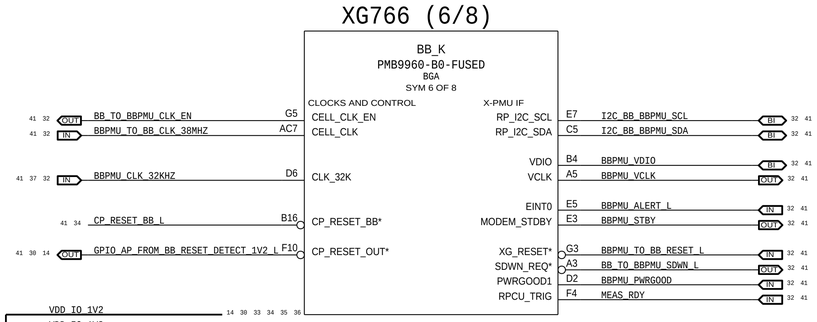
DOMAIN, DP:D:	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_SHAPE	VMOD*LX, VDD_DIG_0V85, VRF_DIG_0V9
P	PWR_SHAPE	VRF_MED_1V3, VRF_LO_1V15
P	PWR_SHAPE	VDD_IO_1V8
P	PWR_SHAPE	VDD_DDR_1V1,VDD_DRAM_1V8,VFE_LO_1V2,VDD_IP_1V0,VDD_SRAM_0V9,VDD_IO_1V2*
P	PWR_200UM	VDD_CHP*,VFE_HI_3V15,VFE_MED_1V8
P	PWR_100UM	VDD_SIM1*,VDD_SIM2*

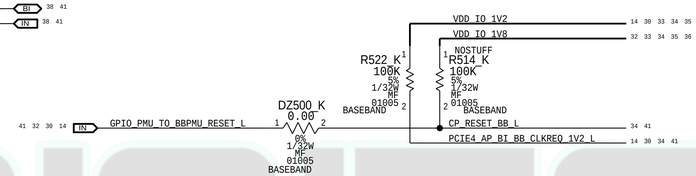
BB: INTERFACE (1/3)

XG766 (8/8)

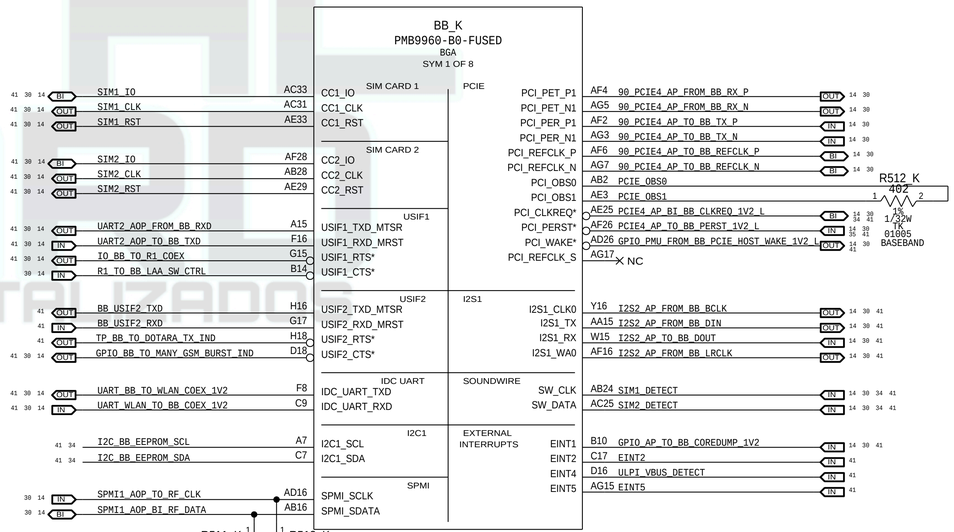


XG766 (6/8)

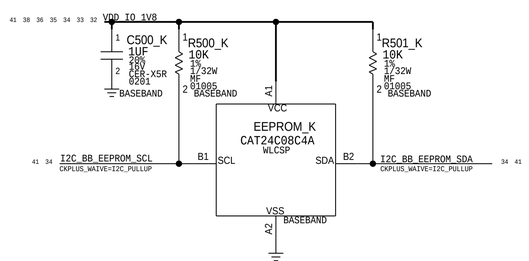




XG766 (1/8)



BB EEPROM



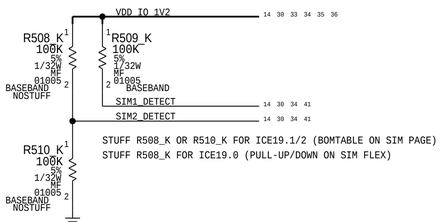
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	NON-DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD	S	A_DIELECTRIC_2X	PCIE_OBS*, BBPMU_VDIO, BBPMU_VCLK	Y
RFFE_SHIELD	S	A_DIELECTRIC_2X	*RFFE*, *SPMI*, BB_TO_XCVR_DWB*, XCVR_TO_BB_DWB*	Y

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	NON-DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
DIGRF	S	A_DIELECTRIC_2X	90_DIGRF*	Y

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
DIGRF	DIGRF	DEFAULT
DIGRF	GND	DEFAULT

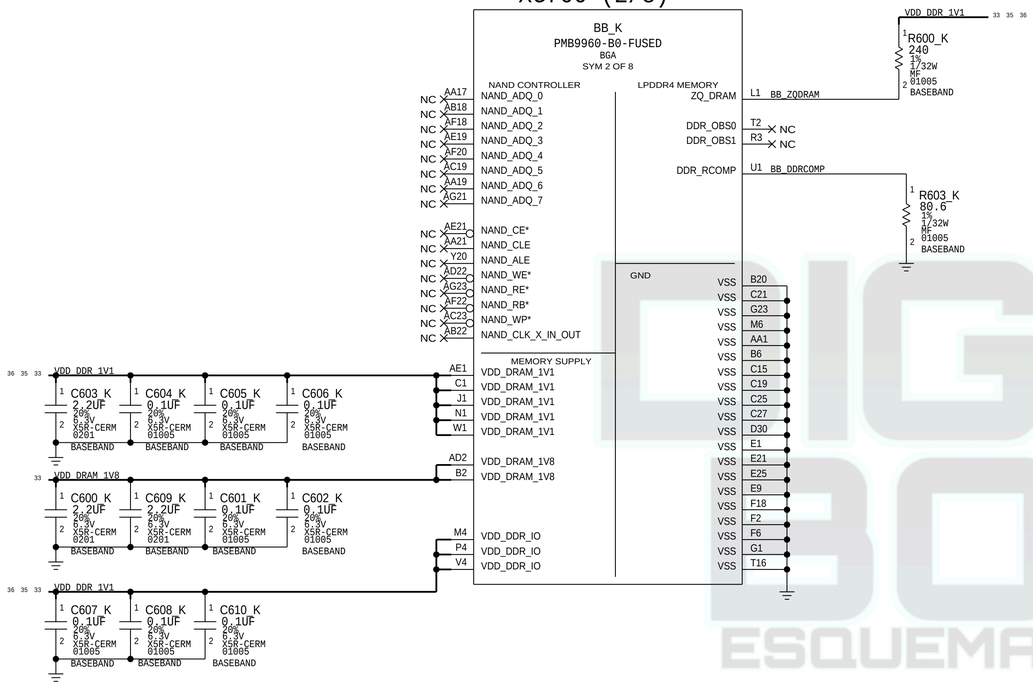
CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
RFFE_SHIELD	RFFE_SHIELD	DEFAULT
RFFE_SHIELD	GND	DEFAULT

DOMAIN (P,E)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_90_OHM_DIFF	90_DIGRF*
E	DIGRF_DP	90_DIGRF*

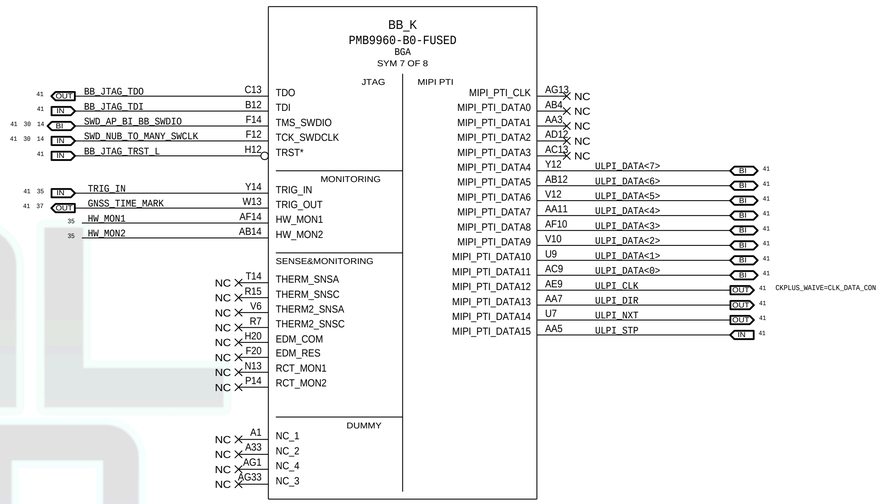


BB: MEMORY & TRACING (2/3)

XG766 (2/8)



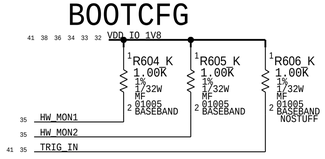
XG766 (7/8)

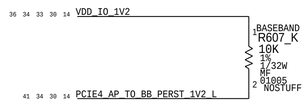


	HW_MON1	HW_MON2	TRIG_IN
NAND	0	0	1
FLASHLESS	1	0	1
FLASHLESS WDOG DIS	1	1	0
NAND (NON-SECURE)	1	1	1

BOOTSTRAPS ARE INTERNALLY PULLED DOWN

BOOTCFG





PERST_L IS PULLED DOWN ON AP_DEV.
BB REQUIRES PERST_L BE PULLED UP WHEN PCIE IS NOT USED
ASSUME THAT IN NAND BOOT, PCIE IS NOT USED

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLASS OVERRIDE
CLASS NAME	****	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
RF_SHIELD	S	A_DIELECTRIC_2X	BB_ZQDRAM, BB_DDRCOMP	Y

BB: POWER (3/3)

XG766 (3/8)

BB_K
PMB9960-B0-FUSED
BGA
SYM 3 OF 8
POWER

VDD_DIG_MAIN: A13, A9, AD10, AD14, AG27, E17, G13, G19, G25, M10, P10, R13, W11
VDD_DIG_2G: J15
VDD_DIG_3G: C3, D8, E13, E15
VDD_DIG_TD: N7
VDD_DIG_LTE: AB26, AB30, AB32, AC21, AD24, AD28, AE17, AE31, H24, J17, J19, J29, J31, J33, K24, K26, N17, N19, N21, N23, N25, N27, N29, N31, N33, R17, R19, R21, T22, T24, T26, T28, T30, T32, W17, W19, W21, W23, W25, W27, W29, W31, W33

VDD_SRAM_CPU: AB8, AC3, V8, Y4, Y6
VDD_SRAM_MAIN: AC15, AC5, AE13, T12
VDD_SRAM_JHARQ0: M12, M14
VDD_SRAM_JHARQ1: U15, V14
VDD_SRAM_2G: K14
VDD_SRAM_3G: D12, D10, D14, D4
VDD_SRAM_LTE: AA23, AA25, AA27, AA29, V24, AA31, AA33, AB20, AD18, AD32, AE23, AE27, AF30, J23, J25, K18, K20, K22, K28, K30, K32, M18, M20, M22, M24, M26, M28, M30, M32, R23, R25, R27, R29, R31, R33, T18, T20, V18, V20, V22, V26, V28, V30, V32

41 36 33 VDD_DIG_0V85
- C700_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C704_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C703_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C707_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C708_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C713_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C711_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C715_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND

VDD_SRAM_0V9 → 33 36

XG766 (4/8)

BB_K
PMB9960-B0-FUSED
BGA
SYM 4 OF 8
POWER

41 36 33 VDD_DIG_0V85
- C716_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C718_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C721_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_DIG_CDMA: D26
VDD_DIG_RAU: E31, F30
VDD_DIG_DPU: H6, H8, J9, K6
VDD_DIG_DMIF: P6, N5, R5
VDD_SRAM_CDMA: E27
VDD_SRAM_RAU: D28, E29, F28
VDD_SRAM_DPU: J3, J7, G7, J5, L5
VDD_SRAM_UPC: D20, D22, D24, E19, E23
VDD_SRAM_TD: M8

- C720_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C729_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C724_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C730_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_SRAM_0V9 → 33 36

VSS: G9, H14, H2, H30, H4, J13, J21, J27, K2, K4, L11, L13, L17, L19, L21, L23, L25, L27, L29, L31, L33, L9, M16, M2, N11, N15, N3, P12, P16, P18, P2, P20, P22, P24, P26, P28, P30, P32, R11, AG9

XG766 (5/8)

BB_K
PMB9960-B0-FUSED
BGA
SYM 5 OF 8
POWER

35 33 VDD_DDR_1V1
41 36 33 VDD_DIG_0V85
- C725_K 1UF 20% 10V X5R-CERM 0201 BASEBAND
- C732_K 0.47UF 20% 6.3V X5R-CERM 01005-1 BASEBAND
- C741_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C736_K 1UF 20% 10V X5R-CERM 0201 BASEBAND
- C740_K 1UF 20% 10V X5R-CERM 0201 BASEBAND

36 33 VDD_IP_1V0
- C726_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C733_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C737_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C742_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_LDO_H_CPU: W9
VDD_LDO_H_UPC: A21
VDD_LDO_L_CPU: Y8
VDD_LDO_L_UPC: B22
VDD_LDO_ADPLL_DDR: R1
VDD_LDO_PLL_HOST: AF8
VDD_LDO_PLL_PHY: K12
VDD_LDO_PLL_UPC: C23
VDD_LDO_PLL_DPU: K8
VDD_LDO_PLL_L2: AF12
VDD_LDO_PLL_CPU: W5
VDD_LDO_PLL_DMIF: T6
VDD_LDO_PLL_3G: E11
VDD_LDO_PLL_LTE: K16
VDD_LDO_PLL_CDMA: F26
VDD_LDO_PLL_ETH: AE7

VSS: T4, T8, U13, U17, U19, U21, U23, U25, U27, U29, U31, U33, V16, V2, W3, W7, Y18, Y2, Y22, Y24, Y26, Y28, Y30, Y32, AA13, AA9, AB6

BG_VREF_IN1: U3
BG_VREF_OUT1: U5 NC
BG_VREF_IN2: G11
BG_VREF_OUT2: K10 NC

VDD_PCIE: AE5
VDD_PCIE_IO: AD6
VDD_LDO_DIGRF: C29
- C744_K 1UF 20% 10V X5R-CERM 0201 BASEBAND
- C747_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C750_K 1UF 20% 10V X5R-CERM 0201 BASEBAND
- C753_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_IP_1V0 → 33 36

VDD_SIM1_IO: AF32
VDD_SIM2_IO: AG29
VDD_SIM1 → 14 30 33 41
VDD_SIM2 → 14 30 33 41

VDD_EMAC_IO: AG11
VCC_ETH_BIAS1: AD8 NC
- C755_K 0.47UF 20% 6.3V X5R 01005-1 BASEBAND
- C756_K 0.47UF 20% 6.3V X5R 01005-1 BASEBAND

VDD_1V8_IO_1: A17
VDD_1V8_IO_2: AG19
VDD_1V8_IO_3: B8
VDD_IO_1V8 → 32 33 34 35 36 38 41

VDD_AP_IO_1: A11
VDD_AP_IO_2: AG25
VDD_IO_1V2 → 14 30 33 34 35
- C745_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C748_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND
- C751_K 4.7UF 20% 10V X5R-CERM 0402-0.1MM BASEBAND
- C754_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_RFFE_1V8: D32, F32
VDD_VIO_1V8: F24
- C746_K 1UF 20% 10V X5R-CERM 0201 BASEBAND
- C749_K 0.1UF 20% 6.3V X5R-CERM 01005 BASEBAND

VDD_IO_1V8 → 32 33 34 35 36 38 41

VCCIOF_1V8: AC11
VDD_DIG_0V85 → 33 36 41

VCCF_1V2: AB10 NC
VCCFHV_2V4: Y10 NC

**DUE TO FUSE IO INCORRECT VOLTAGE

LDO_MON1: F22 NC
LDO_MON2: G21 NC
LDO_MON3: C11 NC
LDO_MON4: H22 NC
LDO_MON5: H10 NC
LDO_MON6: J11 NC
LDO_MON7: N9 NC
LDO_MON8: P8 NC
LDO_MON9: R9 NC
LDO_MON10: T10 NC
LDO_MON11: U11 NC

PLL_MON1: L3 NC
PLL_MON2: L7 NC

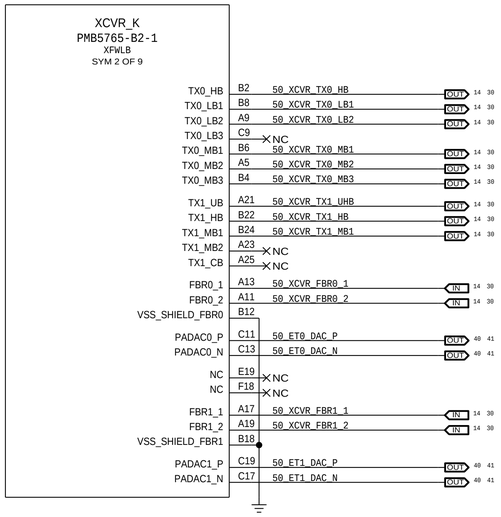
VSS: AC1, AC17, AC27, AC29, AD20, AD30, AD4, AE11, AE15, AF24, AG31

VSS_SENSE: L15 → VSS_SENSE 41

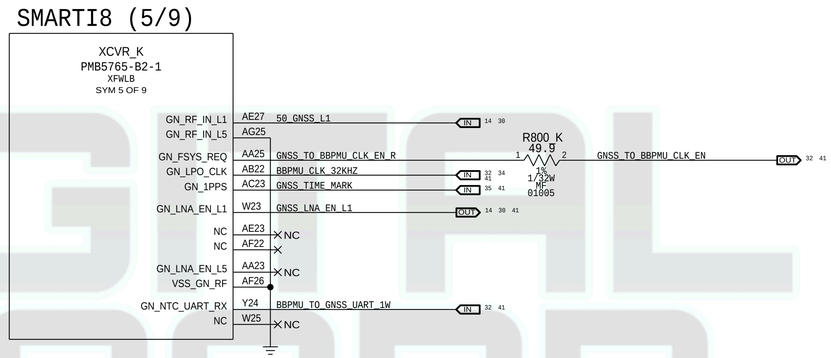
VDD_AP_IO = 1.2V

XCVR: TRANSMIT & GNSS (1/3)

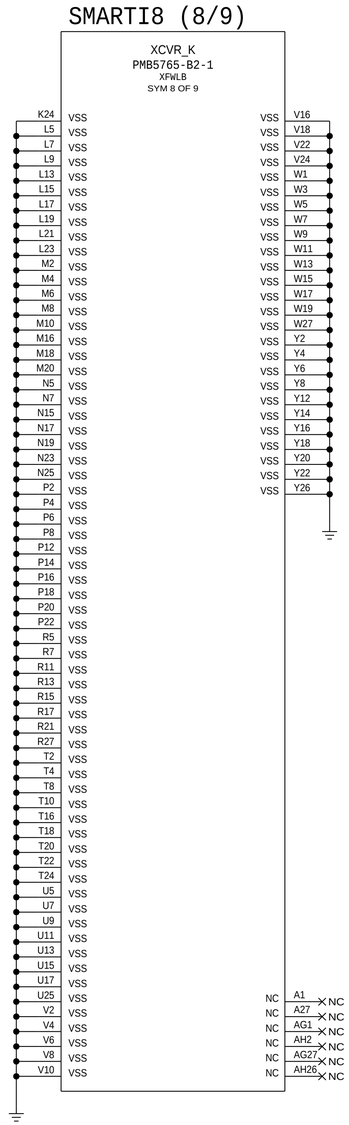
SMARTI8 (2/9)



SMARTI8 (5/9)



SMARTI8 (8/9)

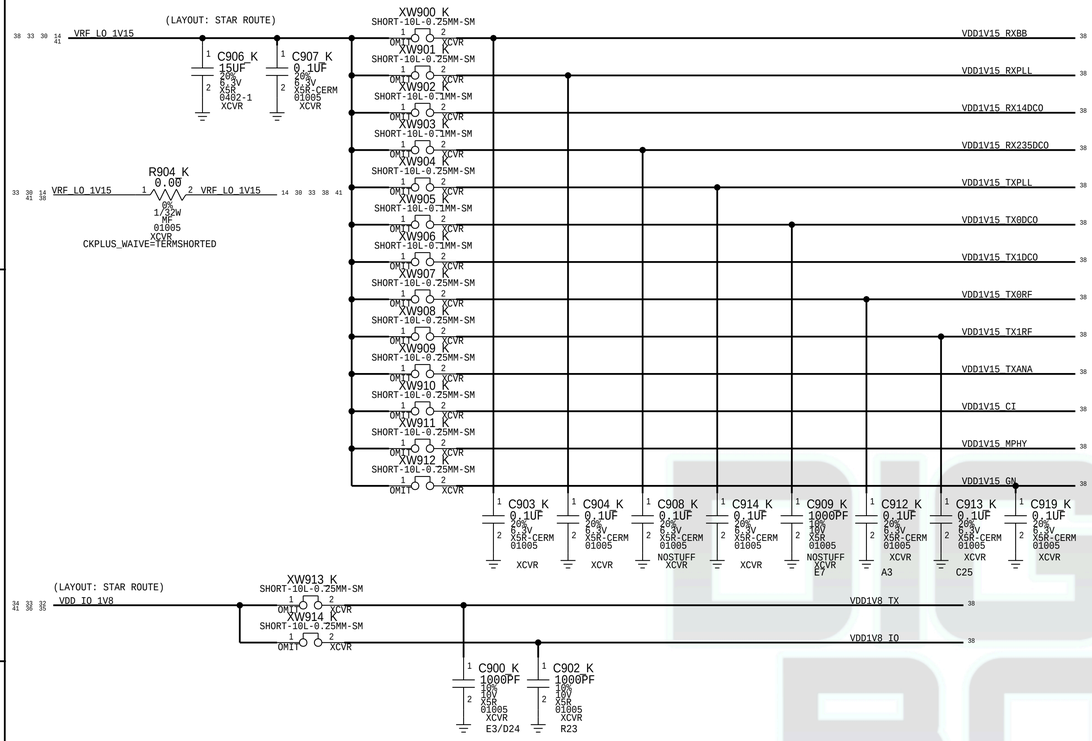


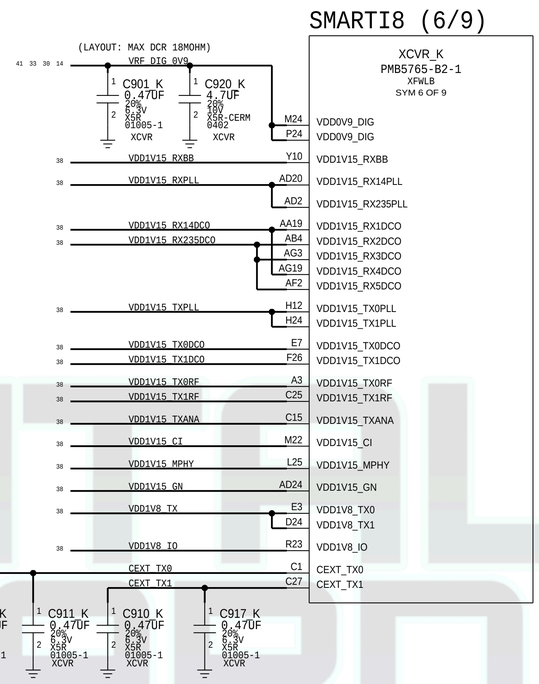
CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
50_WIDE	50_WIDE	A_DIELECTRIC_4XV_50_WIDE_SE
50_WIDE	50_THIN	A_DIELECTRIC_4XD_50_WIDE_SE
50_WIDE	50_THIN_UNSHIELDED	A_DIELECTRIC_4XD_50_WIDE_SE
50_THIN	50_THIN	A_DIELECTRIC_4XD_50_THIN_SE
50_THIN	50_THIN_UNSHIELDED	A_DIELECTRIC_4XD_50_THIN_SE
50_THIN_UNSHIELDED	50_THIN_UNSHIELDED	A_DIELECTRIC_2X

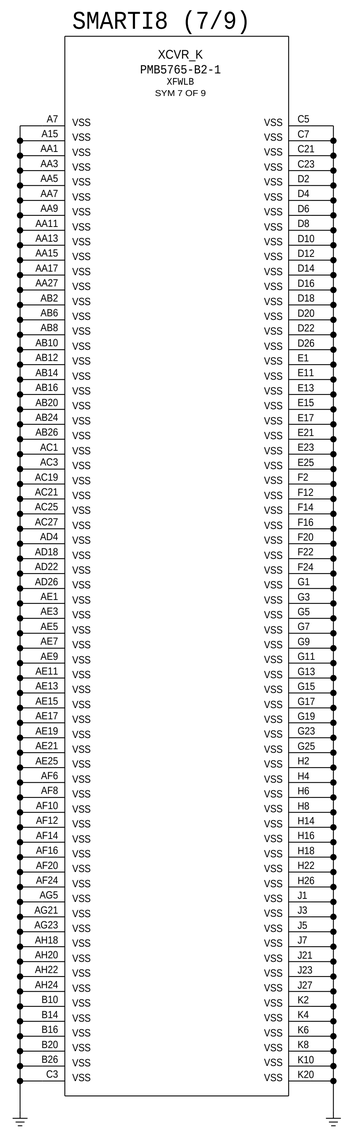
SCHEME (P,E,N)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_XCVR*
P	GENERIC_DP	50_ET*
E	GENERIC_DP	50_ET*

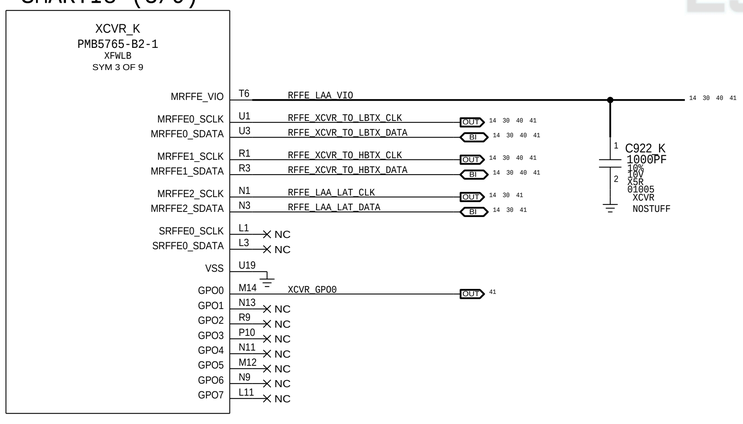
CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR DUMMIES
CLASS NAME	TRACE STYLE	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_TX0_LB2, 50_XCVR_TX0_MB2	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_TX0_HB, 50_XCVR_TX0_LB1, 50_XCVR_TX0_MB1	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_TX0_MB3	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_TX1*, 50_XCVR_FBR*	Y
RF_SHIELD	S	A_DIELECTRIC_2X	50_ET*	Y
GENERIC_DP	P	GENERIC_DP	DP:DP_50_ET*	Y

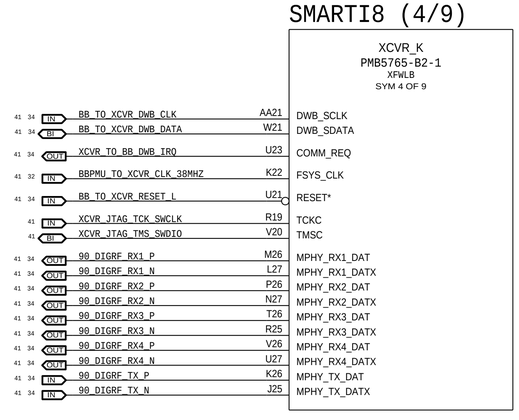
XCVR: INTERFACE & PWR (2/3)











DOMAIN / R-F-XL	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_300UM	VDD1V15*, VDD1V8_TX, VDD1V8_IO
P	PWR_200UM	CEXT_TX*
P	PWR_100UM	VIO_RFFE*

XCVR: PRIMARY DIVERSITY RX (3/3)

SMARTI8 PRX (1/9)

XCVR_K
PMB5765-B2-1
XFWLB
SYM 1 OF 9

NC	V14	NC	
NC	T14	NC	
NC	V12	NC	
NC	T12	NC	
RX1	AG17	50_LAA_TO_XCVR_LAT	50_LAA_TO_XCVR_LAT (MAKE_BASE=TRUE) IN 14 30
RX2	AH16	50_XCVR_RX2_UHB_PRX	IN 14 30
RX3	AG15		
RX4	AH14		
RX5	AG13		
RX6	AH12	50_XCVR_RX6_MB_UHB_PRX	IN 14 30
RX7	AG11	GND	IN 14 30
RX8	AH10	50_XCVR_RX8_MLB_HB_PRX	IN 14 30
RX9	AG9	50_XCVR_RX9_MLB_HB_PRX	14 30
RX10	AH8	50_XCVR_RX10_MLB_HB_PRX	IN 14 30
RX11	AC9	GND	IN 14 30
RX12	AD8	GND	IN 14 30
RX13	AG7	50_XCVR_RX13_LB_MLB_PRX	IN 14 30
RX14	AH6	50_XCVR_RX14_LB_MLB_PRX	IN 14 30

CONNECT ALL UNUSED RX PORTS TO GND

SMARTI8 DRX (9/9)

XCVR_K
PMB5765-B2-1
XFWLB
SYM 9 OF 9

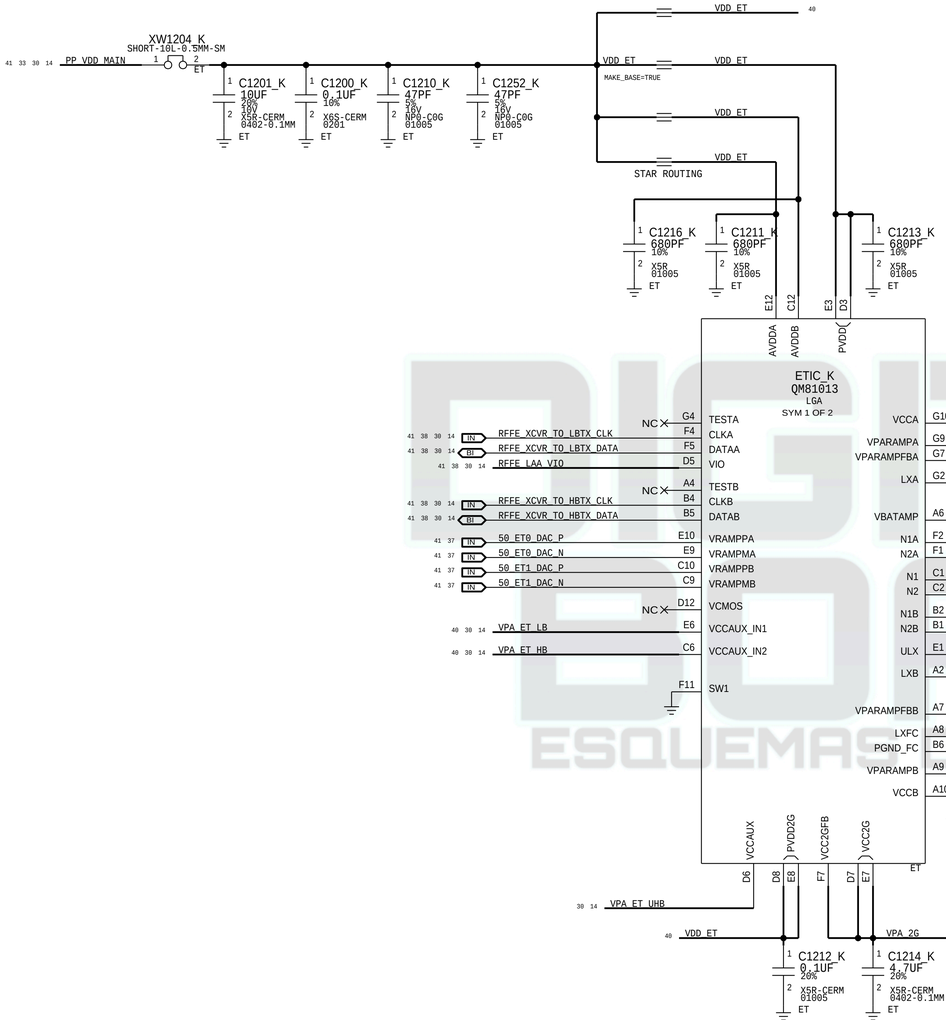
RD1	AC17	50_XCVR_RD1_LAA_DRX	R1000_K 0.00 1 2 50_LAA_TO_XCVR_UAT IN 14 30 (RES 1/32W 01005 XCVR)
RD2	AD16		
RD3	AC15	GND	IN 14 30
RD4	AD14	50_XCVR_RD4_MB_UHB_DRX	IN 14 30
RD5	AC13	GND	IN 14 30
RD6	AD12	GND	IN 14 30
RD7	AC11	50_XCVR_RD7_MLB_HB_DRX	IN 14 30
RD8	AD10	50_XCVR_RD8_MLB_HB_DRX	IN 14 30
RD9	AC7	50_XCVR_RD9_MB_UHB_DRX	IN 14 30
RD10	AD6	50_XCVR_RD10_LB_MLB_DRX	IN 14 30

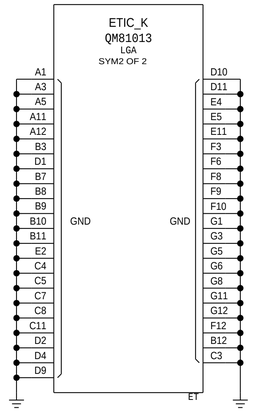
CONNECT ALL UNUSED RD PORTS TO GND.

DOMAIN (P,F,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_LAA_TO_XCVR*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR CHANNEL
CLASS NAME	S/D/C	CONSTRAINT SET		Y/N
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_LAA_TO_XCVR*	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_RX2_*, 50_XCVR_RX10*	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_RX13*, 50_XCVR_RX14*	Y
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_RX6*, 50_XCVR_RX7*, 50_XCVR_RX8*	Y
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_RX9*,50_XCVR_RX11*,50_XCVR_RX12*	Y
50_THIN	S	A_DIELECTRIC_2X	50_XCVR_RD10*	Y
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_RD1_*, 50_XCVR_RD3*, 50_XCVR_RD4*	Y
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_RD5*, 50_XCVR_RD6*, 50_XCVR_RD7*	Y
50_THIN_UNSHIELDED	S	A_DIELECTRIC_2X	50_XCVR_RD8*, 50_XCVR_RD9*	Y

ET MODULATOR





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00811	1	2.2UH 2012 20% 1.0MM	L1201_K	ICE19.0
152S00882	1	2.2UH 2012 20% 0.8MM	L1201_K	ICE19.1
152S00882	1	2.2UH 2012 20% 0.8MM	L1201_K	ICE19.2
152S00811	1	2.2UH 2012 20% 1.0MM	L1202_K	ICE19.0
152S00882	1	2.2UH 2012 20% 0.8MM	L1202_K	ICE19.1
152S00882	1	2.2UH 2012 20% 0.8MM	L1202_K	ICE19.2
152S00750	1	2.2UH 1608 20% 0.8MM	L1205_K	ICE19.0
152S00750	1	2.2UH 1608 20% 0.8MM	L1205_K	ICE19.1
152S00750	1	2.2UH 1608 20% 0.8MM	L1205_K	ICE19.2
131S00382	1	5.6PF 01005	C1251_K	ICE19.0

DOMAIN (P/S)	NET RULE ASSIGNMENT
CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_SHAPE, VPA_ET_LB, VPA_ET_HB, VPA_ET_UHB, VPA_2G
P	PWR_SHAPE, VDD_ET*, V*_ET, VET_LX*, VET_ULX
P	PWR_SHAPE, VET_N*

DEBUG: TEST POINTS

PP2408_K P2MM-NSM SM 1 GPIO_AP_TO_BB_COREDUMP_1V2 — 14 30 34
PP2410_K P2MM-NSM SM 1 BB_TO_XCVR_RESET_L — 34 38
PP2412_K P2MM-NSM SM 1 IO_TOUCH_TO_MANY_SCAN_ACTIVE — 14 30 32
PP2416_K P2MM-NSM SM 1 GPIO_DOTARA_TO_BBPMU_CLK_EN — 14 30 32
PP240A_K P2MM-NSM SM 1 TP_BBPMU_GPIO1 — 32
PP240B_K P2MM-NSM SM 1 TP_BBPMU_GPIO2 — 32
PP240C_K P2MM-NSM SM 1 TP_BBPMU_FORCE_PWM — 32
PP240D_K P2MM-NSM SM 1 TP_BBPMU_GPIO6 — 32

PP2400_K P2MM-NSM SM 1 BBPMU_CLK_32KHZ — 32 34 37
PP2401_K P2MM-NSM SM 1 BB_TO_BBPMU_SDWN_L — 32 34
PP2403_K P2MM-NSM SM 1 BBPMU_PWRGOOD — 32 34
PP2405_K P2MM-NSM SM 1 BBPMU_STBY — 32 34
PP2407_K P2MM-NSM SM 1 GPIO_PMU_TO_BBPMU_RESET_L — 14 30 32 34 41
PP2409_K P2MM-NSM SM 1 BBPMU_ALERT_L — 32 34
PP2411_K P2MM-NSM SM 1 BBPMU_VDIO — 32 34
PP240F_K P2MM-NSM SM 1 UART2_AOP_FROM_BB_RXD — 14 30 34 41
PP240F_K P2MM-NSM SM 1 UART2_AOP_TO_BB_TXD — 14 30 34 41
PP2422_K P2MM-NSM SM 1 BBPMU_VCLK — 32 34
PP2425_K P2MM-NSM SM 1 BBPMU_TO_BB_RESET_L — 32 34
PP2418_K P2MM-NSM SM 1 GNSS_LNA_EN_L1 — 14 30 37

PP24010_K P2MM-NSM SM 1 MEAS_RDY — 32 34
PP2415_K P2MM-NSM SM 1 TP_BB_TO_DOTARA_TX_IND — 34

PP240G_K P2MM-NSM SM 1 I2S2_AP_FROM_BB_BCLK — 14 30 34
PP240H_K P2MM-NSM SM 1 I2S2_AP_FROM_BB_DIN — 14 30 34
PP240I_K P2MM-NSM SM 1 I2S2_AP_TO_BB_DOUT — 14 30 34
PP240J_K P2MM-NSM SM 1 I2S2_AP_FROM_BB_LRCLK — 14 30 34

PP2420_K P2MM-NSM SM 1 BBPMU_TO_GNSS_UART_1W — 32 37
PP2423_K P2MM-NSM SM 1 GNSS_TIME_MARK — 35 37
PP2426_K P2MM-NSM SM 1 BB_TO_BBPMU_CLK_EN — 32 34
PP2427_K P2MM-NSM SM 1 NFC_TO_BBPMU_CLK_EN — 32
PP2428_K P2MM-NSM SM 1 GNSS_TO_BBPMU_CLK_EN — 32 37
PP2429_K P2MM-NSM SM 1 BBPMU_TO_BB_CLK_38MHZ — 32 34
PP2433_K P2MM-NSM SM 1 GPIO_BB_TO_MANY_GSM_BURST_IND — 14 30 34
PP2431_K P2MM-NSM SM 1 I2C_BB_BBPMU_SCL — 32 34
PP2432_K P2MM-NSM SM 1 I2C_BB_BBPMU_SDA — 32 34

PCIE PROBE POINTS ON TOP LEVEL

PCIE

PP2446_K P2MM-NSM SM 1 PCIE4_AP_BI_BB_CLKREQ_1V2_L — 14 30 34
PP2447_K P2MM-NSM SM 1 PCIE4_AP_TO_BB_PERST_1V2_L — 14 30 34 35
PP2448_K P2MM-NSM SM 1 GPIO_PMU_FROM_BB_PCIE_HOST_WAKE_1V2_L — 14 30 34

PP240K_K P2MM-NSM SM 1 BB_USIF2_TXD — 34
PP240L_K P2MM-NSM SM 1 BB_USIF2_RXD — 34
PP240M_K P2MM-NSM SM 1 BBPMU_TO_NFC_CLK_38MHZ — 32

PP2496_K P2MM-NSM SM 1 PRODUCT_ID — 32
PP2497_K P2MM-NSM SM 1 HW_REV_ID — 32

PP2419_K P2MM-NSM SM 1 UART_BB_TO_WLAN_COEX_1V2 — 14 30 34 41
PP2421_K P2MM-NSM SM 1 UART_WLAN_TO_BB_COEX_1V2 — 14 30 34 41
PP2453_K P2MM-NSM SM 1 I2C_BB_EEPROM_SCL — 34
PP2454_K P2MM-NSM SM 1 I2C_BB_EEPROM_SDA — 34
PP2455_K P2MM-NSM SM 1 GPIO_AP_FROM_BB_RESET_DETECT_1V2_L — 14 30 34
PP240N_K P2MM-NSM SM 1 IO_BB_TO_R1_COEX — 14 30 34

PP2456_K P2MM-NSM SM 1 CLK_BBPMU_TO_DOTARA_38M4_1V3 — 14 30 32
PP2457_K P2MM-NSM SM 1 SIM1_CLK — 14 30 34 41
PP2458_K P2MM-NSM SM 1 SIM1_RST — 14 30 34 41
PP2459_K P2MM-NSM SM 1 SIM1_DETECT — 14 30 34 41
PP2460_K P2MM-NSM SM 1 SIM1_IO — 14 30 34 41
PP2461_K P2MM-NSM SM 1 SIM2_CLK — 14 30 34 41
PP2462_K P2MM-NSM SM 1 SIM2_RST — 14 30 34 41
PP2463_K P2MM-NSM SM 1 SIM2_DETECT — 14 30 34 41
PP2464_K P2MM-NSM SM 1 SIM2_IO — 14 30 34 41
PP2465_K P2MM-NSM SM 1 VDD_SIM1 — 14 30 33 36 41
PP2466_K P2MM-NSM SM 1 VDD_SIM2 — 14 30 33 36 41
PP2413_K P2MM-NSM SM 1 BBPMU_TO_XCVR_CLK_38MHZ — 32 38
PP2414_K P2MM-NSM SM 1 VSS_SENSE — 36

PP2417_K P2MM-NSM SM 1 EINT2 — 34
PP2430_K P2MM-NSM SM 1 ULPI_VBUS_DETECT — 34 41
PP2436_K P2MM-NSM SM 1 EINT5 — 34

SMPS LOADING

PP24S1_K P2MM-NSM SM 1 VDD_DIG_0V85 — 33 36
PP24S2_K P2MM-NSM SM 1 VRF_DIG_0V9 — 14 30 33 38
PP24S3_K P2MM-NSM SM 1 VRF_LO_1V15 — 14 30 33 38
PP24S4_K P2MM-NSM SM 1 VRF_MED_1V3 — 33
PP24S5_K P2MM-NSM SM 1 VDD_IO_1V8 — 32 33 34 35 36 38 41

ET

PP2434_K P2MM-NSM SM 1 50_ET0_DAC_P — 40 37
PP2435_K P2MM-NSM SM 1 50_ET0_DAC_N — 40 37
PP2491_K P2MM-NSM SM 1 50_ET1_DAC_P — 40 37
PP2492_K P2MM-NSM SM 1 50_ET1_DAC_N — 40 37

RFFE

PP2467_K P2MM-NSM SM 1 RFFE_BB_TO_LAT_DATA — 14 30 34
PP2468_K P2MM-NSM SM 1 RFFE_BB_TO_LAT_CLK — 14 30 34
PP2469_K P2MM-NSM SM 1 RFFE_BB_TO_UAT_DATA — 14 30 34
PP2470_K P2MM-NSM SM 1 RFFE_BB_TO_UAT_CLK — 14 30 34
PP2439_K P2MM-NSM SM 1 VIO_RFFE_BB_TO_TUNER — 34
PP2471_K P2MM-NSM SM 1 RFFE_XCVR_TO_LBTX_DATA — 14 30 38 40
PP2472_K P2MM-NSM SM 1 RFFE_XCVR_TO_LBTX_CLK — 14 30 38 40
PP2473_K P2MM-NSM SM 1 RFFE_XCVR_TO_HBTX_DATA — 14 30 38 40
PP2474_K P2MM-NSM SM 1 RFFE_XCVR_TO_HBTX_CLK — 14 30 38 40
PP2498_K P2MM-NSM SM 1 RFFE_LAA_LAT_CLK — 14 30 38
PP2499_K P2MM-NSM SM 1 RFFE_LAA_LAT_DATA — 14 30 38
PP2495_K P2MM-NSM SM 1 RFFE_LAA_VIO — 14 30 38 40

JTAG

PP2450_K P2MM-NSM SM 1 BB_JTAG_TDO — 35 41
PP2449_K P2MM-NSM SM 1 BB_JTAG_TDI — 35 41
PP2452_K P2MM-NSM SM 1 SWD_AP_BI_BB_SWDIO — 14 30 35 41
PP2483_K P2MM-NSM SM 1 SWD_NUB_TO_MANY_SWCLK — 14 30 35 41
PP2484_K P2MM-NSM SM 1 BB_JTAG_TRST_L — 35 41
PP2485_K P2MM-NSM SM 1 TRIG_IN — 35
PP2486_K P2MM-NSM SM 1 XCVR_JTAG_TCK_SWCLK — 38
PP2487_K P2MM-NSM SM 1 XCVR_JTAG_TMS_SWDIO — 38

DIG-RF

PP2475_K P2MM-NSM SM 1 90_DIGRF_TX_P — 34 38
PP2476_K P2MM-NSM SM 1 90_DIGRF_TX_N — 34 38
PP2477_K P2MM-NSM SM 1 90_DIGRF_RX1_P — 34 38
PP2478_K P2MM-NSM SM 1 90_DIGRF_RX1_N — 34 38
PP2479_K P2MM-NSM SM 1 90_DIGRF_RX2_P — 34 38 41 34
PP2490_K P2MM-NSM SM 1 90_DIGRF_RX2_N — 34 38 41 35 30 14
PP2481_K P2MM-NSM SM 1 90_DIGRF_RX3_P — 34 38
PP2482_K P2MM-NSM SM 1 90_DIGRF_RX3_N — 34 38
PP2424_K P2MM-NSM SM 1 90_DIGRF_RX4_P — 34 38
PP2493_K P2MM-NSM SM 1 90_DIGRF_RX4_N — 34 38
PP2488_K P2MM-NSM SM 1 BB_TO_XCVR_DWB_DATA — 34 38
PP2489_K P2MM-NSM SM 1 BB_TO_XCVR_DWB_CLK — 34 38
PP2490_K P2MM-NSM SM 1 XCVR_TO_BB_DWB_IRQ — 34 38
PP240P_K P2MM-NSM SM 1 XCVR_GPO0 — 38

STUFF ONLY FOR VENDOR CONFIG

R2400_K 0.00Ω 0% 1/32W MF 01005 NOSTUFF
41 38 36 35 34 33 32 VDD_IO_1V8 — 1 — 2 — PP1V8_S2 — 14 30

POWERS LAA FEMS

JDEBUG_K BM28P0.6-44DS-0.35V F-ST-SM

41 40 33 30 14 PP_VDD_MAIN	45		46	PP_VDD_MAIN
41 34 32 30 14 GPIO_PMU_TO_BBPMU_RESET_L	1		2	NC
	3		4	NC
35 ULPI_DATA<7>	5		6	BB_JTAG_TDI
35 ULPI_DATA<6>	7		8	BB_JTAG_TDO
35 ULPI_DATA<5>	9		10	BB_JTAG_TRST_L
35 ULPI_DATA<4>	11		12	CP_RESET_BB_L
35 ULPI_DATA<3>	13		14	
35 ULPI_DATA<2>	15		16	VDD_SIM1
35 ULPI_DATA<1>	17		18	SIM1_RST
35 ULPI_DATA<0>	19		20	SIM1_IO
35 ULPI_CLK	21		22	SIM1_CLK
35 ULPI_DIR	23		24	SIM1_DETECT
35 ULPI_NXT	25		26	VDD_SIM2
35 ULPI_STP	27		28	SIM2_RST
34 BB_TO_ULPI_RESET_L	29		30	SIM2_IO
	31		32	SIM2_CLK
NC	33		34	SIM2_DETECT
NC	35		36	
NC	37		38	UART_BB_TO_WLAN_COEX_1V2
41 ULPI_VBUS_DETECT	39		40	UART_WLAN_TO_BB_COEX_1V2
41 35 30 14 SWD_NUB_TO_MANY_SWCLK	41		42	UART2_AOP_TO_BB_TXD
41 35 30 14 SWD_AP_BI_BB_SWDIO	43		44	UART2_AOP_FROM_BB_RXD
	47		48	

NOSTUFF

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

WIFI_MLB (GODFATHER)

LAST_MODIFICATION=Tue May 28 17:48:01 2019

PAGE	CSA	CONTENTS	SYNC	DATE
42	1	WIFI: TABLE OF CONTENTS		
43	2	GODFATHER		05/08/2018

WIFI: TABLE OF CONTENTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0598	1	CAP,CER,C0G,1.2PF,16V,01005	C230_W	WIFI.0
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C231_W	WIFI.0
131S0598	1	CAP,CER,C0G,1.2PF,16V,01005	C243_W	WIFI.0
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C244_W	WIFI.0
152S00498	1	IND,FILM,0.4NH,1000MA,,01005	R233_W	WIFI.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R235_W	WIFI.0
152S00500	1	IND,FILM,2.6NH,450MA,01005	R237_W	WIFI.0
152S00500	1	IND,FILM,2.6NH,450MA,,01005	R238_W	WIFI.0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
131S0648	1	CAP,CER,C0G,0.3PF,16V,01005	C230_W	WIFI.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C231_W	WIFI.X
131S00030	1	CAP,CER,C0G,0.4PF,16V,01005	C243_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R233_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R235_W	WIFI.X
152S00416	1	IND,FILM,1.2NH,800MA,01005	R237_W	WIFI.X
152S00492	1	IND,FILM,1.0NH,01005	R238_W	WIFI.X

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S00648	339S00647	ALT_PARTS	U_WLAN_W	WIFI,GODFATHER,ES4.5

WLAN SYMBOL IO PORTS

POWER
- PP_VDD_MAIN — VOLTAGE=3.8
- PP1V8_S4 — VOLTAGE=1.8V
- PP1V2_S4 — VOLTAGE=1.2
- PP_VDD_BTPA3V3 — VOLTAGE=3.3

CONTROL
- GPIO_PMU_TO_WLAN_REG_ON

CLOCKS
- GPIO_PMU_TO_WLAN_R1_32K_CLK
- GPIO_AP_FROM_WLAN_TIME_SYNC_1V2
- GPIO_AP_FROM_BT_AUDIO_SYNC

WLAN PCIE
- 90_PCIE3_AP_TO_WLAN_REFCLK_P
- 90_PCIE3_AP_TO_WLAN_REFCLK_N
- 90_PCIE3_AP_TO_WLAN_TX_P
- 90_PCIE3_AP_TO_WLAN_TX_N
- 90_PCIE3_AP_FROM_WLAN_RX_P
- 90_PCIE3_AP_FROM_WLAN_RX_N
- PCIE3_AP_TO_WLAN_PERST_1V2_L
- PCIE3_AP_BI_WLAN_CLKREQ_1V2_L
- GPIO_PMU_FROM_WLAN_HOST_WAKE

R1
- IO_BT_TO_R1_TIME_SYNC
- IO_BT_TO_R1_DEV_WAKE
- IO_WLAN_TO_R1_COEX
- IO_R1_TO_WLAN_COEX

AOP
- GPIO_AOP_TO_WLAN_CONTEXT_A
- GPIO_AOP_TO_WLAN_CONTEXT_B

COEX
- UART_BB_TO_WLAN_COEX_1V2
- UART_WLAN_TO_BB_COEX_1V2

ANTENNA
- 50_WLAN_G_UAT
- 50_WLAN_G_LAT

NFC
- I2C_BT_TO_NFC_SCL
- I2C_BT_BI_NFC_SDA
- GPIO_SE_TO_BT_PKT_RDY

SPMI
- SPMI1_AOP_TO_RF_CLK
- SPMI1_AOP_BI_RF_DATA

BOT_SPK
- BT_TO_BOT_SPK_TRIG

LAA
- 50_WLAN_A_TX0
- 50_WLAN_A_RX0
- 50_WLAN_A_TX1
- 50_WLAN_A_RX1
- 5GHZ_C0_VDET
- 5GHZ_C1_VDET
- RFA0_SW_CTRL0
- RFA0_SW_CTRL1
- RFA0_SW_CTRL2
- RFA1_SW_CTRL0
- RFA1_SW_CTRL1
- RFA1_SW_CTRL2

SCHEMATIC APN: 951-08430

WIFI/BT

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
WLAN_SHIELD	WLAN_SHIELD	DEFAULT
WLAN_SHIELD	GND	DEFAULT

DOMAIN (E,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	PWR_SHAPE	ASR*, CSR*, ABUCK*, CBUCK*
P	PWR_80UM	PP_VDD_BTPA3V3

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR* DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	CLEAR OVERRIDE Y/N
CLASS NAME	DOMAIN E,P,S	CONSTRAINT SET		
WLAN_SHIELD	S	A_DIELECTRIC_2X	RFA0_SW*, RFA1_SW*	Y
RF_SHIELD	S	A_DIELECTRIC_2X	5GHZ_C*	Y
50_THIN	S	A_DIELECTRIC_2X	50_WLAN_A*	Y
50_WIDE	S	A_DIELECTRIC_2X_50_WIDE_SE	50_WLAN_G*	Y

DOMAIN (E,P,S)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
P	A_50_THIN_SE	50_WLAN_A*
P	A_50_WIDE_SE	50_WLAN_G*

U_WLAN_W
LBEE5XV1VC-400
LGA
SYM 1 OF 3
SYM 2 OF 3
SYM 3 OF 3
PP1V2_S4
PP_VDD_BTPA3V3
PP_VDD_MAIN
L253_W 2.2UH-20%-1.1A-0.293OHM
L255_W 2.2UH-20%-1.1A-0.293OHM
C254_W
C256_W
ASR_LVX
ABUCK_1P12V
CSR_LVX
CBUCK_0P9V
OMIT_TABLE
NOSTUFF
50_WLAN_A_TX0
50_WLAN_A_RX0
5GHZ_C0_VDET
50_WLAN_A_TX1
50_WLAN_A_RX1
5GHZ_C1_VDET
50_WLAN_G_UAT
50_WLAN_G_LAT
RFA0_SW_CTRL0
RFA0_SW_CTRL1
RFA0_SW_CTRL2
RFA1_SW_CTRL0
RFA1_SW_CTRL1
RFA1_SW_CTRL2
TX_5G_C0_MAIN
RX_5G_C0_MAIN
TSSI_5G_C0_CHIP
TX_5G_C1_MAIN
RX_5G_C1_MAIN
TSSI_5G_C1_CHIP
2G_ANT_C0
2G_ANT_C1
WL_DIVERSITY_CORE0
WL_DIVERSITY_CORE1
WL_GPIO_7
WL_GPIO_16
WL_GPIO_21
WIFI_TO_SENSORC_COEX
SENSORC_TO_WIFI_COEX
BT_TO_SENSORA_COEX
WLBT_WL_FAST_UART_RX
WLBT_WL_FAST_UART_RTS_OUT
WLBT_WL_FAST_UART_CTS_IN
WLBT_WL_FAST_UART_TX
WLAN_TDI/CXT_A
WLAN_TDO/CXT_B
WLAN_TRST_L
JTAG_SEL
SWD_CLK
SWD_DAT
LHL_GPIO2
LBIST_MBIST
WLBT_BT_UART_CTS_L
WLBT_BT_UART_RXD
WLBT_BT_UART_RTS_L
WLBT_BT_UART_TXD
WLBT_WL_HOST_WAKE
WLBT_WL_REG_ON
WLBT_BT_DEV_WAKE
BT_TO_SENSORC_WAKE
SE_I2C_CLK
SE_I2C_DAT
BT_TO_SENSORC_TIME_SYNC
GPIO_SENSORB_TO_BT_SYNC
SOC_TO_BT_TIME_SYNC
BT_TO_AP_TIME_SYNC
WLAN_TO_SENSORA_EN
WLBT_CLK_32K
PP1V8_IO
SPMI_CLK
SPMI_DAT
UART_WLAN_RXD_1V2
UART_WLAN_RTS_L_1V2
UART_WLAN_CTS_L_1V2
UART_WLAN_UART_TXD_1V2
GPIO_AOP_TO_WLAN_CONTEXT_A
GPIO_AOP_TO_WLAN_CONTEXT_B
JTAG_WLAN_TRST_L
JTAG_WLAN_SEL
JTAG_WLAN_TMS
JTAG_WLAN_TCK
UART_AP_TO_BTWLAN_RTS_L
UART_AP_TO_BTWLAN_TXD
UART_BTWLAN_TO_AP_RTS_L
UART_BTWLAN_TO_AP_TXD
GPIO_PMU_FROM_WLAN_HOST_WAKE
GPIO_PMU_TO_WLAN_REG_ON
BT_TO_BOT_SPK_TRIG
IO_BT_TO_R1_DEV_WAKE
I2C_BT_TO_NFC_SCL
I2C_BT_BI_NFC_SDA
IO_BT_TO_R1_TIME_SYNC
GPIO_SE_TO_BT_PKT_RDY
GPIO_AP_FROM_BT_AUDIO_SYNC
TP_WLAN_TO_DOTARA_TX_IND
GPIO_PMU_TO_WLAN_R1_32K_CLK
PP1V8_S4
SPMI1_AOP_TO_RF_CLK
SPMI1_AOP_BI_RF_DATA
WLBT_BT_REG_ON
WLAN_TIME_SYNC
WLBT_WL_PCIE_PERST_L
WLBT_WL_PCIE_CLKREQ_L
90_WLBT_WL_PCIE_RD_P
90_WLBT_WL_PCIE_RD_N
90_WLBT_WL_PCIE_TD_P
90_WLBT_WL_PCIE_TD_N
90_WLBT_WL_PCIE_REFCLK_P
90_WLBT_WL_PCIE_REFCLK_N
WLBT_SECI_OUT
WLBT_SECI_IN
TP_BT_REG_ON
GPIO_AP_FROM_WLAN_TIME_SYNC_1V2
PCIE3_AP_TO_WLAN_PERST_1V2_L
UART_BB_TO_WLAN_COEX_1V2
UART_WLAN_TO_BB_COEX_1V2
90_PCIE3_AP_TO_WLAN_REFCLK_N
90_PCIE3_AP_TO_WLAN_REFCLK_P
90_PCIE3_AP_FROM_WLAN_RX_N
90_PCIE3_AP_FROM_WLAN_RX_P
90_PCIE3_AP_TO_WLAN_TX_N
90_PCIE3_AP_TO_WLAN_TX_P
PCIE3_AP_BI_WLAN_CLKREQ_1V2_L
WL_GPIO_21_1V2
IO_WLAN_TO_R1_COEX
IO_R1_TO_WLAN_COEX
TP_BT_TO_DOTARA_TX_IND
PCIE PROBE POINTS ON TOP LEVEL
PP1V2_S4
PP1V8_S4
GPIO_SE_TO_BT_PKT_RDY
BT_TO_BOT_SPK_TRIG
GPIO_PMU_FROM_WLAN_HOST_WAKE
PCIE3_AP_TO_WLAN_PERST_1V2_L
PCIE3_AP_BI_WLAN_CLKREQ_1V2_L
GPIO_AOP_TO_WLAN_CONTEXT_A
GPIO_AOP_TO_WLAN_CONTEXT_B
TP_BT_TO_DOTARA_TX_IND
TP_WLAN_TO_DOTARA_TX_IND
GPIO_PMU_TO_WLAN_REG_ON
TP_BT_REG_ON
GPIO_PMU_TO_WLAN_R1_32K_CLK
GPIO_AP_FROM_BT_AUDIO_SYNC
GPIO_AP_FROM_WLAN_TIME_SYNC_1V2
IO_WLAN_TO_R1_COEX
IO_R1_TO_WLAN_COEX
IO_BT_TO_R1_DEV_WAKE
IO_BT_TO_R1_TIME_SYNC
BOOTSTRAPS
WL_GPIO7 0:JTAG 1:SWD
WL_GPIO21 0:BT PCIE 1:BT UART
JTAG_WLAN_SEL
NOSTUFF= JTAG DISABLED
WL_GPIO_21_1V2
NOSTUFF=BT OVER PCIE
GND
WLAN

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
7	0017939155	ENGINEERING RELEASED	2019-05-28

LAA_WIFI (GODFATHER)

LAST_MODIFICATION=Tue May 28 17:48:01 2019

PAGE	CSA	CONTENTS	SYNC	DATE
44 FEM_MODULES	1	FEM MODULES		05/08/2018
45	2	FEM MODULES		05/08/2018

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00492	1	IND,FILM,1.0NH,900MA,01005	R362_W	WIFI.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R363_W	WIFI.0
152S00498	1	IND,FILM,0.4NH,1000MA,01005	R372_W	WIFI.0
152S00496	1	IND,FILM,0.6NH,950MA,01005	R373_W	WIFI.0
131S0648	1	CAP,CER,C0G,0.3PF,16V,01005	C361_W	WIFI.0

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
152S00419	1	IND,FILM,1.1NH,01005	R362_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R363_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R372_W	WIFI.X
117S0161	1	RES,MF,0 OHM,1/32W,01005	R373_W	WIFI.X
131S0893	1	CAP,CER,C0G,0.2PF,16V,01005	C361_W	WIFI.X

LAA

45 13 IO 50_WLAN_A_TX0
45 13 IO 50_WLAN_A_RX0_LAA
45 13 IO 50_WLAN_A_TX1
45 13 IO 50_WLAN_A_RX1_LAA
45 13 IO 5GHZ_C0_VDET
45 13 IO 5GHZ_C1_VDET
45 13 IO RFA0_SW_CTRL0
45 13 IO RFA0_SW_CTRL1
45 13 IO RFA0_SW_CTRL2
45 13 IO RFA1_SW_CTRL0
45 13 IO RFA1_SW_CTRL1
45 13 IO RFA1_SW_CTRL2

45 13 IO PP_VDD_MAIN
45 13 IO PP1V8_S2
45 13 IO PP1V8_S4
45 13 IO 50_LAA_TO_ANT_LAT
45 13 IO 50_LAA_TO_ANT_UAT
45 13 IO 50_LAA_TO_XCVR_LAT
45 13 IO 50_LAA_TO_XCVR_UAT
45 13 IO RFFE_LAA_VIO
45 13 IO RFFE_LAA_LAT_CLK
45 13 IO RFFE_LAA_LAT_DATA
45 13 IO RFFE_LAA_VIO
45 13 IO RFFE_LAA_UAT_CLK
45 13 IO RFFE_LAA_UAT_DATA
45 13 IO 50_LAA_TO_R1
45 13 IO R1_TO_BB_LAA_SW_CTRL

SCHEMATIC APN: 951-08431

FEM MODULES

STUFF ONLY FOR VENDOR CONFIG

GOMAN (E.P.D)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
	P PWR_100UM	PP1V8_UAT_FEM_LNA, PP1V8_LAT_FEM_LNA, RFFE_*VIO, PP_1V8_VIO_LAA*

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR (spacing)
CLASS NAME	DIFF	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*.DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
WLAN_SHIELD		S A_DIELECTRIC_2X	RFA0_SW*, RFA1_SW*	?
RF_SHIELD		S A_DIELECTRIC_2X	*R1_TO_BB_LAA_SW*, 5GHZ_C*	?
50_THIN		S A_DIELECTRIC_2X	50_WLAN_A*	?
50_WIDE		S A_DIELECTRIC_2X_50_WIDE_SE	50_LAA_TO_ANT_LAT	?
50_THIN_UNSHIELDED		S A_DIELECTRIC_2X	50_LAA_TO_XCVR*	?

GOMAN (E.P.D)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)
	P A_50_THIN_SE	50_WLAN_A*, 50_LAA_TO_XCVR*
	P A_50_WIDE_SE	50_LAA_TO_ANT_LAT

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
WLAN_SHIELD	WLAN_SHIELD	DEFAULT
WLAN_SHIELD	GND	DEFAULT

5GHZ UAT FEED

R311_W 0.00 0% 1/32W MF 01005 UAT_FEM NOSTUFF — PP1V8_S2 → PP1V8_S4

FL302_W 10-OHM-1.1A 01005 UAT_FEM — PP1V8_S4 → PP1V8_UAT_FEM_LNA

C304_W 33PF 5% 16V NP0/C0G 01005-1 UAT_FEM

C305_W 10UF 20% 10V X5R-CERM 0402-0.1MM UAT_FEM

C306_W 33PF 5% 16V NP0/C0G 01005-1 UAT_FEM

PP_VDD_MAIN

R363_W 0.00 0% 1/32W MF 01005 UAT_FEM OMIT_TABLE — 50_WLAN_A_TX0 → 50_WLAN_A_TX0_VOID_FEM_IN

C366_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF UAT_FEM

U_5G_U_W MDFEGFFB-126 LGA

16	5G_TX_IN GND_VOID=TRUE
20	VDET
24	RF_SW_CTRL0
35	RF_SW_CTRL1
28	RF_SW_CTRL2
26	RF_SW_CTRL3
12	LAA_RX GND_VOID=TRUE
4	RFFE_DATA
3	RFFE_CLK
23	USID1
8	VDD_1V8
18	VCC1_PA
19	VCC2_PA
14	5G_RX GND_VOID=TRUE
6	ANT GND_VOID=TRUE
2	RFFE_VIO
10	SAM GND_VOID=TRUE
GND	1 5 7 9 11 13 15 17 21 22 25 27 29 30 31 32 33 34

R362_W 0.00 0% 1/32W MF 01005 UAT_FEM OMIT_TABLE — 50_WLAN_A_RX0_VOID_FEM_OUT → 50_WLAN_A_RX0_LAA (OUT)

C361_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF UAT_FEM

50_LAA_TO_ANT_UAT (BI)

50_LAA_TO_R1 (BI)

C379_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

C382_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

C381_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

C380_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

5GHZ_C0_VDET (OUT)

RFA0_SW_CTRL0 (IN)

RFA0_SW_CTRL1 (IN)

RFA0_SW_CTRL2 (IN)

R1_TO_BB_LAA_SW_CTRL (IN)

50_LAA_TO_XCVR_UAT (OUT)

RFFE_LAA_UAT_DATA (BI)

RFFE_LAA_UAT_CLK (IN)

C321_W 18PF 5% 16V NP0/C0G 01005 UAT_FEM NOSTUFF

C322_W 18PF 5% 16V NP0/C0G 01005 UAT_FEM NOSTUFF

R310_W 0.00 01005 UAT_FEM — RFFE_LAA_VIO (IN) → PP_1V8_VIO_LAA_UAT

C323_W 18PF 5% 16V NP0/C0G 01005 UAT_FEM

PRODUCT_ID=0X41 (LAA RDM)
USID RX=0X6 (LAA RDM)

5GHZ LAT FEED

1X10UF / 4X2.2UF CAPS ADDED ON TOP LEVEL

FL312_W 10-OHM-1.1A 01005 LAT_FEM — PP1V8_S2 → PP1V8_LAT_FEM_LNA

C314_W 33PF 5% 16V NP0/C0G 01005-1 LAT_FEM

PP_VDD_MAIN

C316_W 33PF 5% 16V NP0/C0G 01005-1 LAT_FEM

R373_W 0.00 0% 1/32W MF 01005 LAT_FEM OMIT_TABLE — 50_WLAN_A_TX1 → 50_WLAN_A_TX1_VOID_FEM_IN

C376_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF LAT_FEM

U_5G_L_W MDFEGFFB-126 LGA

16	5G_TX_IN GND_VOID=TRUE
20	VDET
24	RF_SW_CTRL0
35	RF_SW_CTRL1
28	RF_SW_CTRL2
26	RF_SW_CTRL3
12	LAA_RX GND_VOID=TRUE
4	RFFE_DATA
3	RFFE_CLK
23	USID1
8	VDD_1V8
18	VCC1_PA
19	VCC2_PA
14	5G_RX GND_VOID=TRUE
6	ANT GND_VOID=TRUE
2	RFFE_VIO
10	SAM GND_VOID=TRUE
GND	1 5 7 9 11 13 15 17 21 22 25 27 29 30 31 32 33 34

R372_W 0.00 0% 1/32W MF 01005 LAT_FEM OMIT_TABLE — 50_WLAN_A_RX1_VOID_FEM_OUT → 50_WLAN_A_RX1_LAA (OUT)

C371_W 0.3PF +/-0.05PF 16V C0G-CERM 01005 NOSTUFF LAT_FEM

50_LAA_TO_ANT_LAT (BI)

C383_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

R375_W 0.00 0% 1/32W MF 01005 LAT_FEM — RFA1_SW_CTRL1 → RFA1_SW_CTRL1_FEM

C384_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

R376_W 0.00 0% 1/32W MF 01005 LAT_FEM — RFA1_SW_CTRL2 → RFA1_SW_CTRL2_FEM

C385_W 10PF 5% 16V NP0/C0G 01005 UAT_FEM

RFA1_SW_CTRL0 (IN)

RFA1_SW_CTRL1 (IN)

RFA1_SW_CTRL2 (IN)

5GHZ_C1_VDET (OUT)

50_LAA_TO_XCVR_LAT (OUT)

RFFE_LAA_LAT_DATA (BI)

RFFE_LAA_LAT_CLK (IN)

C325_W 18PF 5% 16V NP0/C0G 01005 LAT_FEM NOSTUFF

C324_W 18PF 5% 16V NP0/C0G 01005 LAT_FEM NOSTUFF

R364_W 0.00 01005 LAT_FEM — RFFE_LAA_VIO (IN) → PP_1V8_VIO_LAA_LAT

C333_W 18PF 5% 16V NP0/C0G 01005 LAT_FEM

PRODUCT_ID=0X41 (LAA RPM)
USID RX=0X5 (LAA RPM)