

AN IMPROVED VIRTUAL ANALOG MODEL OF THE MOOG LADDER FILTER

Stefano D'Angelo* and Vesa Välimäki

Aalto University, School of Electrical Engineering
Department of Signal Processing and Acoustics
P.O. Box 13000, FI-00076, AALTO, Espoo, Finland

ABSTRACT

The Moog ladder structure is a well known filter used in musical sound synthesizers and in music production. Previously several digital models have attempted to imitate its nonlinear and self-oscillating characteristics. In this paper we derive a novel circuit-based model for the Moog filter and discretize it using the bilinear transform. The proposed nonlinear digital filter compares favorably against Huovilainen's model, which is the best previous white-box model for the Moog filter. The harmonic distortion characteristics of the proposed model match closely with those of a SPICE simulation. Furthermore, the novel model realistically enters the self-oscillation mode and maintains it. The proposed model requires only 12 more basic operations per output sample than Huovilainen's model, but includes the same number of nonlinear functions, which dominate the computational load. The novel nonlinear digital filter is applicable in virtual analog music synthesis and in musical audio effects processing.

Index Terms—Acoustic signal processing, audio systems, circuit simulation, music, resonator filters

1. INTRODUCTION

Real-time digital simulation of analog circuits, also known as virtual analog modeling, is today an active area of research in audio processing [1, 2, 3, 4]. This is especially true in the case of filters employed in music production, of which the Moog ladder filter [5] is one of the best known examples.

1.1. Relation to prior work

Modeling of Moog synthesizer circuits has been the subject of many studies. In particular, the filter circuit has been thoroughly analyzed in [6, 7], which also provide linear digital implementations, as well as in [1, 8, 9]. Additionally, other analog filters with a similar circuit topology [10, 11, 12, 13] and the Moog oscillator waveforms [14] have been studied. However, one of the most desired features of the Moog ladder filter is the “warmth” in the output sound that is due to

the nonlinear behavior of the circuit. Several attempts to digitally emulate this characteristic have been made, ranging from “heuristic” [15, 16], to black-box [17, 18], and physical modeling [19, 20] approaches. Huovilainen [19, 21] derived what is, so far, the best white-box simulation method that preserves the nonlinearity of the filter.

This paper describes a new derivation based on circuit analysis of the continuous-time large-signal model of the filter's core circuit, then proposes a new digital implementation of it. This new implementation is confronted with the previous simulator described in [19] and it is shown to produce outputs that more closely resemble Ngspice [22] simulation results, which are taken as a reference. Furthermore, it also improves on the accuracy in reproducing the self-oscillating effect of the real filter.

Section 2 analyzes the filter circuit in order to derive a realistic large-signal model of it. Section 3 describes its discretization and provides the proposed digital implementation. Section 4 compares the new simulator with the previous one and with Ngspice results. Section 5 concludes the paper.

2. ANALYSIS OF THE MOOG LADDER FILTER

Fig. 1 shows the transistor ladder circuit at the heart of the Moog ladder filter [5]. At the “bottom” of this circuit is a differential transistor pair, depicted in Fig. 2(a), which is driven by the control current I_{ctl} and into which the input voltage and

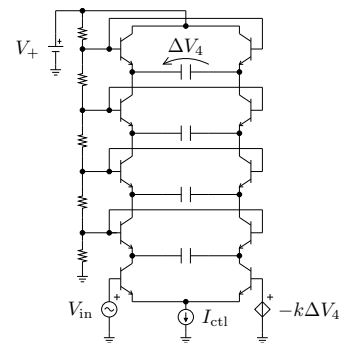


Fig. 1: The Moog ladder circuit [5].

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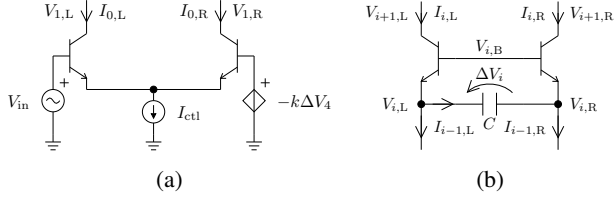


Fig. 2: (a) Differential pair and (b) ladder stage.

part of the phase inverted output are fed. This is connected to a series of four stages, each containing two transistors and one capacitor. A single ladder stage is represented in Fig. 2(b). The “top” of the last stage is directly connected to the voltage generator V_+ , which also powers a series of resistors placed between transistor bases of consecutive stages.

In this work we assume that the current gain factor (*beta*) of the transistors is infinite, therefore the base currents are null and the base voltages are constant. The same initial assumption can be found in [19].

2.1. Differential pair

By assuming that the *beta* of a transistor is infinite, the large-signal Ebers-Moll model [23] reduces to

$$I_E \approx -I_C \approx I_S \left(e^{\frac{V_{BE}}{V_T}} - e^{\frac{V_{BC}}{V_T}} \right), \quad (1)$$

thus, since $I_{ctl} = I_{0,L} + I_{0,R}$, we obtain

$$I_{0,L} = \frac{I_{ctl} e^{\frac{k\Delta V_4}{V_T}} + I_S \left(e^{-\frac{V_{1,R}}{V_T}} - e^{-\frac{V_{1,L}}{V_T}} \right)}{e^{\frac{k\Delta V_4}{V_T}} + e^{-\frac{V_{in}}{V_T}}}, \quad (2)$$

where k is the feedback coefficient and V_T is the thermal voltage. This basic result will be used for the derivation of the global model of the circuit later on.

2.2. Single stage

Since all capacitors in the circuit have the same capacitance value C , it is possible to express the emitter current of each transistor as

$$I_{i,s} = I_{i-1,s} \pm C \frac{d\Delta V_i}{dt} \Rightarrow I_{i,s} = I_{0,s} \pm C \sum_{j=1}^i \frac{d\Delta V_j}{dt}, \quad (3)$$

where s is either L (left) and the sign in both expressions is +, or it is R (right) and the sign is -.

From (1) and (3) it follows that

$$e^{-\frac{V_{i,s}}{V_T}} = \frac{I_{0,s} \pm C \sum_{j=1}^i \frac{d\Delta V_j}{dt}}{I_S} e^{-\frac{V_{i,B}}{V_T}} + e^{-\frac{V_{i+1,s}}{V_T}}, \quad (4)$$

and iteratively substiting $V_{i+1,s}$, while also taking into account that $V_{5,L} = V_{5,R} = V_+$, it is possible to obtain

$$e^{-\frac{V_{i,s}}{V_T}} = \frac{\alpha_i \left(I_{0,s} \pm C \sum_{j=1}^i \frac{d\Delta V_j}{dt} \right) + \beta_i}{I_S} + e^{-\frac{V_+}{V_T}}, \quad (5)$$

where $\alpha_i = \sum_{j=i}^4 e^{-\frac{V_{j,B}}{V_T}}$, $\beta_i = C \sum_{j=i+1}^4 \alpha_j \frac{d\Delta V_j}{dt}$ for $i = 1 \dots 3$, while $\beta_4 = 0$. Therefore

$$e^{\frac{\Delta V_i}{V_T}} = \frac{\alpha_i I_{ctl} + 2\gamma}{\alpha_i \left(I_{0,L} + C \sum_{j=1}^i \frac{d\Delta V_j}{dt} \right) + \beta_i + \gamma} - 1, \quad (6)$$

where $\gamma = I_S e^{-\frac{V_+}{V_T}}$.

2.3. Global model

Substituting (5) into (2), solving for the bottom left-branch current $I_{0,L}$ and then substituting again into (6), we obtain

$$e^{\frac{\Delta V_i}{V_T}} = \frac{\alpha_i I_{ctl} + 2\gamma}{\alpha_i \left(\zeta_i I_{ctl} + C \sum_{j=1}^i \eta_j \frac{d\Delta V_j}{dt} \right) + \eta_i \beta_i + \gamma} - 1, \quad (7)$$

where $\zeta_i = \frac{e^{\frac{k\Delta V_4}{V_T}} + \alpha_i}{e^{\frac{k\Delta V_4}{V_T}} + e^{-\frac{V_{in}}{V_T}} + 2\alpha_i}$ and $\eta_i = \frac{e^{\frac{k\Delta V_4}{V_T}} + e^{-\frac{V_{in}}{V_T}}}{e^{\frac{k\Delta V_4}{V_T}} + e^{-\frac{V_{in}}{V_T}} + 2\alpha_i}$.

Since $\alpha_i \ll e^{-\frac{V_{in}}{V_T}}$ for all i and $\gamma \approx 0$, the previous expression can be reasonably approximated as

$$e^{\frac{\Delta V_i}{V_T}} \approx \frac{1}{\frac{1}{1 + e^{-\frac{V_{in} + k\Delta V_4}{V_T}}} + \frac{C}{I_{ctl}} \sum_{j=1}^i \frac{d\Delta V_j}{dt}} - 1, \quad (8)$$

or equivalently as

$$\frac{d\Delta V_i}{dt} = -\frac{I_{ctl}}{2C} \left[\tanh\left(\frac{\Delta V_i}{2V_T}\right) + \tanh\left(\frac{V_{in} + k\Delta V_4}{2V_T}\right) \right] - \sum_{j=1}^{i-1} \frac{d\Delta V_j}{dt}. \quad (9)$$

By comparing the previous expression for consecutive stages, for $i > 1$ we obtain

$$\frac{d\Delta V_i}{dt} = \frac{I_{ctl}}{2C} \left[\tanh\left(\frac{\Delta V_{i-1}}{2V_T}\right) - \tanh\left(\frac{\Delta V_i}{2V_T}\right) \right], \quad (10)$$

which coupled with

$$\frac{d\Delta V_1}{dt} = -\frac{I_{ctl}}{2C} \left[\tanh\left(\frac{\Delta V_1}{2V_T}\right) + \tanh\left(\frac{V_{in} + k\Delta V_4}{2V_T}\right) \right] \quad (11)$$

defines our continuous-time large-signal model of the circuit. This is similar to the model derived in [19]. The differences are in that, in [19], the right side of the equations is not divided by 2 and the output voltage of the first stage, and hence of all stages, has opposite polarity. The inversion of polarity does not make any difference in practice.

3. DIGITAL IMPLEMENTATION

Differential equations (10) and (11) show how the derivative of the output voltage at each stage depends instantly on the

output voltages of both the previous stage and the current stage. For the discretization of such expressions to be computable, we approximated the derivative value by adding a fictitious unit delay to the argument of hyperbolic tangents where self-dependencies would occur, as well as, on a global level, to ΔV_4 when fed back to the first stage. Therefore, the resulting discrete-time model is given by

$$d\Delta V_1[n] = -\frac{I_{\text{ctl}}}{2C} \left[\tanh\left(\frac{\Delta V_i[n-1]}{2V_T}\right) + \tanh\left(\frac{V_{\text{in}}[n] + k\Delta V_4[n-1]}{2V_T}\right) \right], \quad (12)$$

$$d\Delta V_i[n] = \frac{I_{\text{ctl}}}{2C} \left[\tanh\left(\frac{\Delta V_{i-1}[n]}{2V_T}\right) - \tanh\left(\frac{\Delta V_i[n-1]}{2V_T}\right) \right]. \quad (13)$$

3.1. Bilinear transform

The output voltage at each stage is calculated by applying a bilinear-transformed integrator to the derivative estimate. The linear constant-coefficient difference (LCCD) equation defining the integrator is

$$V_i[n] = V_i[n-1] + \frac{dV_i[n] + dV_i[n-1]}{2f_s}, \quad (14)$$

where $dV_i[n]$ is the input, $V_i[n]$ is the output, and f_s is the sample rate.

Furthermore, by applying basic block diagram properties, the first stage can be simplified to resemble the others as indicated in Fig. 3, which shows the optimized block diagram representation of the entire discrete-time filter. This is composed by a total of 5 hyperbolic tangent evaluations, 13 unit delays, 13 additions, 9 multiplications, and a sign change. It is also interesting to notice that each ladder stage is implemented by a second-order nonlinear filter, as indicated by Figs. 3(b) and 3(c). The integrator block included in the ladder stages is the bilinear integrator (14).

3.2. Tuning the cutoff frequency

When low amplitude signals are applied to the filter, the hyperbolic tangent in each stage operates almost linearly, thus the LCCD equation of a stage becomes

$$\Delta V_i[n] \approx \Delta V_i[n-1] + A(\Delta V_{i-1}[n] + \Delta V_{i-1}[n-1] - \Delta V_i[n-1] - \Delta V_i[n-2]), \quad (15)$$

where $A = I_{\text{ctl}}/(8f_s CV_T)$. This corresponds, in the z -domain, to

$$\frac{\Delta V_i(z)}{\Delta V_{i-1}(z)} = \frac{A + Az^{-1}}{1 + (A-1)z^{-1} + Az^{-2}}, \quad (16)$$

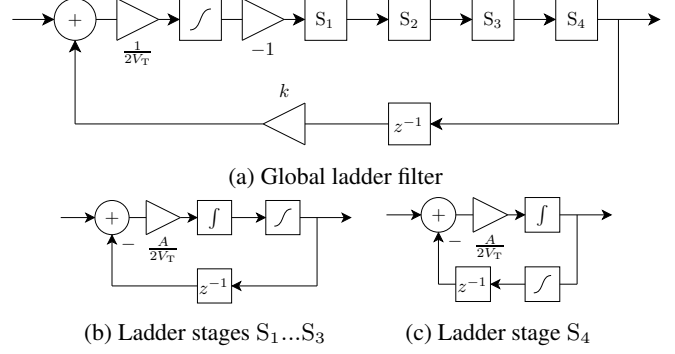


Fig. 3: Proposed implementation, where $V_T \approx 26$ mV at room temperature.

which can be mapped to the Laplace domain using the inverse bilinear transform as

$$\frac{\Delta V_i(s)}{\Delta V_{i-1}(s)} = ABf_s \left[\frac{1 + A + B}{s + f_s(1 - A - B)} - \frac{1 - A - B}{s + f_s(1 - A + B)} \right], \quad (17)$$

where $B = \sqrt{A^2 - 6A + 1}$. Since $A > 0$ and $B > 0$, the leading pole has the cutoff frequency

$$f_c = \frac{f_s}{2\pi}(1 - A - B), \quad (18)$$

from which I_{ctl} is derived as $I_{\text{ctl}} = 8\pi CV_T \frac{f_s - \pi f_c}{f_s + \pi f_c} f_c$, and therefore the cutoff frequency can be set by parameter A in Figs. 3(b) and 3(c) as

$$A = \pi \frac{f_c}{f_s} \frac{1 - \pi \frac{f_c}{f_s}}{1 + \pi \frac{f_c}{f_s}}. \quad (19)$$

4. EVALUATION

In this section the proposed implementation is confronted with the previous model presented in [19]. Both are based on approximate discrete-time solutions of analogous continuous-time differential equations constituting the large-signal model of each circuit stage, which results in a clear similarity between the top-level filter structures. At the stage level, however, the previous model uses first-order filters, while the new model uses second-order filters, as outlined in Section 3.

They also show similar performance despite the addition, in the new model, of a total of 12 operations, namely 3 multiplications, 4 additions, 4 unit delays, and a sign change, since the extra computational cost introduced is negligible when compared to the 5 hyperbolic tangent evaluations that are present in both implementations. However, this might not be the case if these last operations are implemented by table

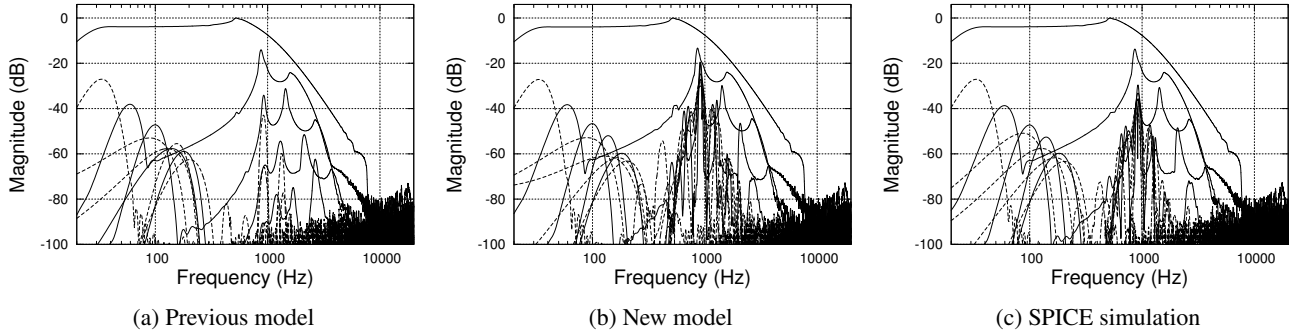


Fig. 4: Normalized harmonic spectra up to the 10th harmonic of the outputs obtained by exciting the models operating at a 384-kHz sample rate with a 2-s long, 0.1 V logarithmically swept sine from 20 Hz to 100 kHz and applying the analysis technique described in [24] on the output signals. The model parameters are set so that the cutoff frequency of each ladder stage is 1 kHz and the global feedback gain value is 4.0. The fundamental and odd harmonic responses are represented by solid lines, and the even harmonic responses are shown by dashed lines.

lookup or polynomial approximation, yet the total computational cost is sufficiently small for practical real-time implementations.

In order to evaluate the quality of the generated outputs, both models were confronted with the results obtained by using the SPICE-based [25] Ngspice circuit simulator [22] and feeding it with the same test input signals. In particular we performed *logsweep analysis* [24] to check the static harmonic response, by using a 2-s long, 0.1 V logarithmically swept sine from 20 Hz to 100 kHz with the simulators operating at a 384-kHz sample rate, with the cutoff frequency of 1 kHz and a feedback gain value of 4.0. The normalized harmonic spectra of the output signals up to 10th harmonic are shown in Fig. 4. It is immediate to notice that the new model shows significant improvement in distortion characteristics around the cutoff frequency. Further analysis of the differences in the responses by subtracting the model response from the SPICE simulation would be misleading because of frequency warping.

It was indeed expected that at a feedback gain value such that the dominant poles of the global filter are located on the imaginary axis, the system would start to self oscillate at the cutoff frequency. It can be shown that such value is $k = 4.0$ [6], and the previous analysis on one side confirms the theoretical result through circuit simulation, while on the other it shows that the new model is more realistic, in this regard, than the previous one, which instead starts to self oscillate at higher feedback levels.

A further confirmation of the different behavior w.r.t. self-oscillation between the two implementations can be seen in Fig. 5, which visualizes the outputs obtained by exciting the two models operating at a 96-kHz sample rate, with the stage cutoff frequency of 1 kHz and a feedback gain value of 4.0, with a 1-s long, 1 V, 1.5708 kHz sine wave. As soon as the input excitation stops, the self-oscillation effect starts to take place in both models, but while it keeps steady in the new one,

it rapidly fades out in the other.

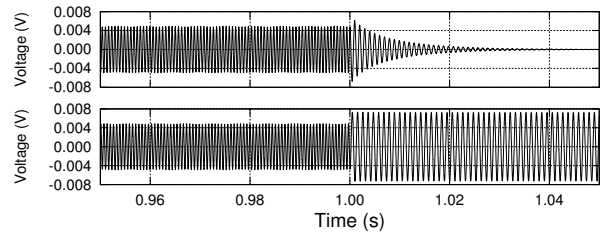


Fig. 5: Outputs obtained by exciting the previous model (top) and the new model (bottom) operating at a 96-kHz sample rate, with the stage cutoff frequency of 1 kHz and a feedback gain value of 4.0, with a 1-s long, 1 V, 1.5708 kHz sine wave.

In the end, the proposed solution does not substantially improve the tuning and phase shifting errors described in [19], thus still needing compensation for these unwanted side effects [16].

5. CONCLUSIONS

A new derivation of the large-signal model of the Moog ladder filter and a new digital implementation were presented. This new implementation was evaluated by confronting the generated outputs with those obtained from a previous model [19] and from the Ngspice [22] circuit simulator.

Despite a small extra computational cost, which is most likely negligible in any practical implementation, the new simulator was found to provide a more realistic output and to model the self-oscillating effect of the circuit more accurately than its predecessor. The novel Moog ladder filter will be useful in virtual analog music synthesizers and in audio effects processing. Audio examples are available at <http://www.acoustics.hut.fi/go/icassp13-moog>.

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