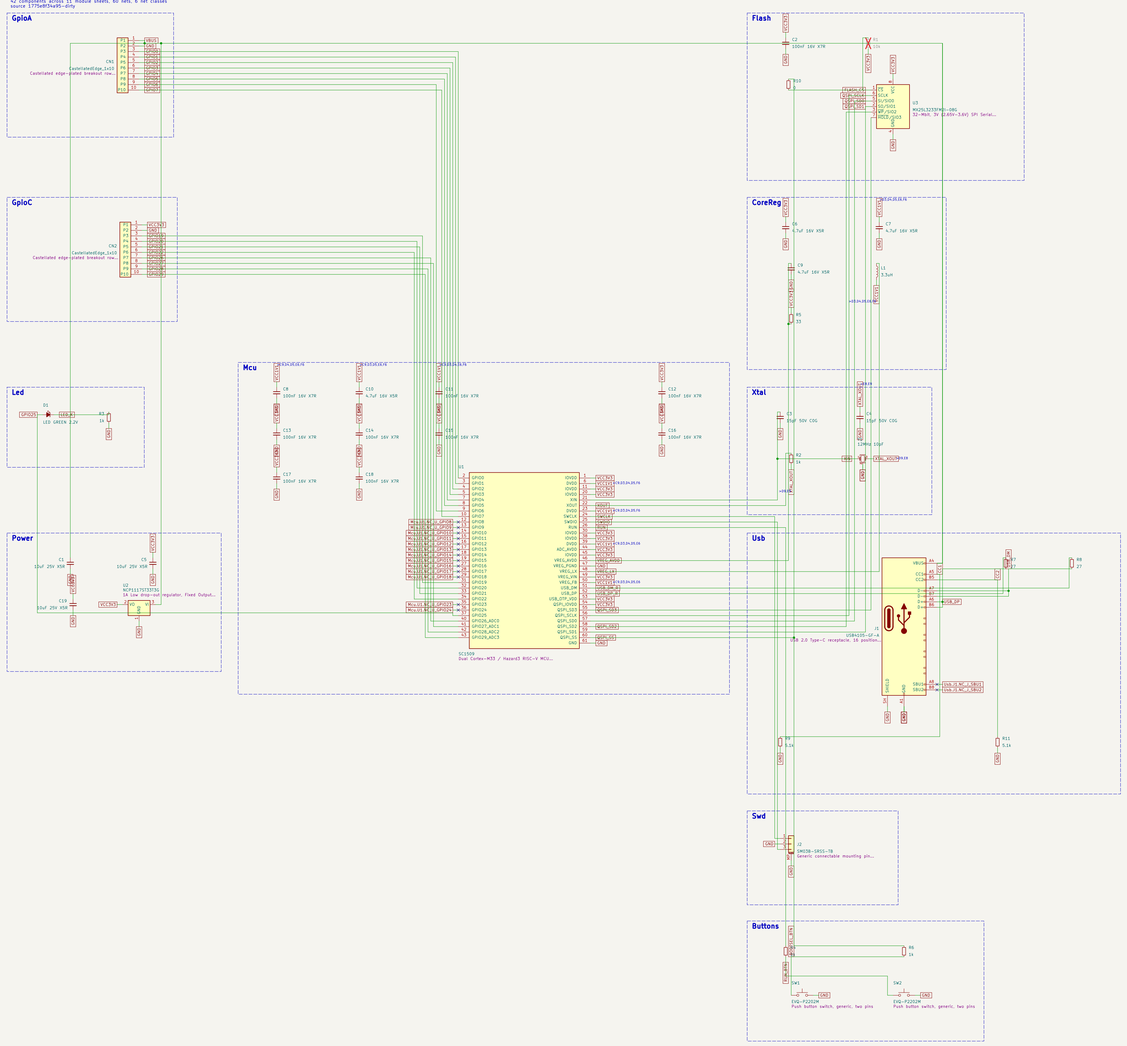
BOARD
Test-board
Small RP2350A test board (39 components, 2L, 51x21mm) used as a KiCadRoutingTools test bed.
2 copper layers, 1.00 mm finished
42 components across 11 module sheets, 60 nets, 6 net classes
source 1775e0f3ba95-dirty



Net	Pins	Zones
BOOTSEL_BTN	2	J8 J9
CC1	2	F9 G8
CC2	2	F9 G10
FLASH_CS	3	A9 B8 B9
GND	59	A2 A8 B9 C2 C8 C9 D3 D4 D5 D7 E2 E3 E4 E5 E7 E8 E9 F1 F2 F6 G6 G9 H10 H4 H8 J8 J9
GPIO0	2	A2 E5
GPIO1	2	A2 E5
GPIO19	2	C2 F5
GPIO2	2	A2 E5
GPIO20	2	C2 F5
GPIO21	2	C2 F5
GPIO22	2	C2 F5
GPIO25	2	E1 F5
GPIO26	2	C2 F5
GPIO27	2	C2 F5
GPIO28	2	C2 G5
GPIO29	2	C2 G5
GPIO3	2	A2 E5
GPIO4	2	A2 E5
GPIO5	2	A2 E5
GPIO6	2	A2 E5
GPIO7	2	B2 E5
LED_K	2	D2 E1
Mcu.U1.MC_U_GPIO10	1	F5
Mcu.U1.MC_U_GPIO11	1	F5
Mcu.U1.MC_U_GPIO12	1	F5
Mcu.U1.MC_U_GPIO13	1	F5
Mcu.U1.MC_U_GPIO14	1	F5
Mcu.U1.MC_U_GPIO15	1	F5
Mcu.U1.MC_U_GPIO16	1	F5
Mcu.U1.MC_U_GPIO17	1	F5
Mcu.U1.MC_U_GPIO18	1	F5
Mcu.U1.MC_U_GPIO23	1	F5
Mcu.U1.MC_U_GPIO24	1	F5
Mcu.U1.MC_U_GPIO8	1	E5
Mcu.U1.MC_U_GPIO9	1	F5
QSPI_SCLK	2	B9 F6
QSPI_SD0	2	B9 F6
QSPI_SD1	2	B9 G6
QSPI_SD2	2	B9 F6
QSPI_SD3	2	B9 F6
QSPI_SS	3	A8 G6 J9
RUN	2	F6 J8
RUN_BTN	2	J8 J9
SWCLK	2	E6 H8
SWDIO	2	E6 J8
USB_DM	3	F11 F9
USB_DM_R	2	F11 F8
USB_DP	3	F10 F9
USB_DP_R	2	F10 F6
Usb.U1.MC_U_SBU1	1	G9
Usb.U1.MC_U_SBU2	1	G9
VBUS	7	A2 F1 F2 F9
VCC1V1	9	C9 D3 D4 D5 E6 F6
VCC3V3	26	A8 A9 C2 C8 D7 D8 E3 E4 E5 E6 E7 F1 F2 F6
VREG_AVDD	3	C8 D8 F6
VREG_LX	2	C9 F6
VIN	3	D8 E6 E9
VOUT	2	E6 E8
XTAL_XOUT	3	D9 E8 E9

#	Refs	Qty	Value	MPN	Manufacturer	Package	Note
1	C1,C3,C19	3	10uF 25V X5R	CL21A106KAC1JNNC	Samsung Electro-Mechanics	0805	
2	C2,C8,C11-C18	10	100nF 16V X7R	CL05B104KO5NNNC	Samsung Electro-Mechanics	0402	
3	C3,C4	2	15pF 50V C0G	CL05C150JB5NNNC	Samsung Electro-Mechanics	0402	
4	C6,C7,C9,C10	4	4.7uF 16V X5R	CL05A475MO5NUNC	Samsung Electro-Mechanics	0402	
5	CN1,CN2	2	CastelatedEdge_1x10				not in BOM, PCB feature
6	D1	1	LED-SMT0R-2.2V	APT2012SGC	Kingbright	0805	
7	J1	1	USB4105-GF-A	USB4105-GF-A	GCT		
8	J2	1	SM03B-SRSS-TB	SM03B-SRSS-TB	JST		
9	L1	1	3.3uH	ASTA-B20161053N3-10L-T	Abracon	2016 metric (0806)	
10	R1	1	10k	ERJ-2RKF1002X	Panasonic Electronic Components	0402	
11	R10	1	0	RC0402JR-07R0RL	Yageo	0402	
12	R3	1	1k	RC0603FR-071KL	Yageo	0603	
13	R2,R4,R6	3	1k	RC0402FR-071KL	Yageo	0402	
14	R5	1	33	RC0402FR-0733RL	Yageo	0402	
15	R7,R9	2	27	RC0402FR-0727RL	Yageo	0402	
16	R8,R11	2	5.1k	RC0402FR-075K1L	Yageo	0402	
17	SW1,SW2	2	EVQ-P2202M	EVQ-P2202M	Panasonic		
18	U1	1	SC1509	SC1509	Raspberry Pi	QFN-60 7x7mm 0.4mm pitch	
19	U2	1	NCP1117ST33T3G	NCP1117ST33T3G	onsemi	SOT-223-3	
20	U3	1	MX25L3233FM2I-08G	MX25L3233FM2I-08G	Macronix	SOP-8 (208mil)	
21	Y1	1	12MHz 10pF	ABMM-272-T3	Abracon	3225,4Pin	

NET CLASSES ON THIS SHEET
GND — GND_DEF
  GND is the ground plane, not a routed trace (HW-TB-PCB26): no track width governs almost nothing. The class exists so pin GND's stitching vias to 0.6/0.3 and to give the pour an explicit identity.
VBUS, VCC1V1, VCC3V3, VREG_AVDD, VREG_LX — PWR
  track width 0.4mm for loop inductance, not current capacity (HW-TB-PCB25). Broader than the default so these nets route cleanly through dense areas.
QSPI_SD0, QSPI_SD1, QSPI_SD2, QSPI_SD3, QSPI_SCLK, QSPI_SS — QSPI_BUS
  track width 0.16mm, inside HW-TB-PCB19's 0.15-0.2mm band.
USB_DM, USB_DM_R, USB_DP, USB_DP_R — USB_FS_DIFF
  90 ohm differential target, 0.8mm / 0.15mm gap (HW-TB-PCB13 HARD). Design-intent-by-geometry: no impedance coupon is ordered, and KiCad's project schema has no impedance field, so this text is the only place the intent lives. Pairs are routed as two independent traces, not a diff pair.
  track-to-track 3W rule and lines in layout/kicad_drc are a net class 0.5 is unsatisfiable at the USB-C land pattern and cost 15 of 44 routed nets.
  USB_DM_R / USB_DP_R: 0.15mm
  clearance 0.45mm is a 3x keep-out from digital and switching nets (HW-TB-PCB23 HARD), not a fab minimum — the one class whose clearance encodes design intent rather than a manufacturing floor.

POWER
  HW-TB-COMP02: the LDO's continuous rating shall exceed the worst-case 3V3 load (41.6mA, 3W-specced section 3 power budget) by a factor of >=10.
  HW-TB-COMP03: the LDO shall output VOUT ±2% (HW-TB-COMP04) at its nominal output voltage in excess of 1.0 A; but every electrical characteristic — output voltage, line and load regulation, dropout — is specified to 800mA, and its 1000mA figure is the MAXIMUM CURRENT LIMIT (HW-TB-COMP05), not a rating it must hold continuously. Sustained load is not a continuous rating. The requirement still passes, at 19.2x against a required 10x.
  check: _LDO_MAX >= _MAX_LOADED*10
  HW-TB-COMP06: LDO dropout shall be <=0.4V at 1.0mA
  HW-TB-COMP07(b): input headroom against the USB VBUS minimum, not its 5V nominal. Datasheet: the 3.3V fixed part is guaranteed over Vin = 4.75V to 15V, dropout 0.95V typ / 1.1V max at Iout = 1A, so 4.75V is the worst-case input at which the regulator still holds 3V3. USB 2.0 section 7.2.2: a high-power port supplies >=4.75V at a full-unit load.
  CORRECTION: dropout is specified "Measured at Vout -100 mV", so the guarantee is Vin >= 3.20 + 0.4 = 3.60V, not 3.20V. At 3.60V the 3V3 rail sags 100mV and a 3.3V-logic input sees a bus-powered hub. Therefore has <100mV of margin, not the "exactly zero" this comment used to claim, and the binding limit is not the LDO at all: RP2350 Table 1441 puts a 3.135V floor on IOVDD, so the USB-powered case is marginal by design, not by accident. Recorded as intent. Consequence: a series Schottky would break only the already-marginal 4.80V case, so the dropout budget is NOT a second justification for HW-TB-CONN05's zero VBUS protection: D1's forward-voltage/reverse-leakage argument stands on its own. See HW-TB-COMP02b.
  Tolerance propagation: HW-TB-COMP02 (3V3 >= 3.135V) + HW-TB-COMP07 (Vin >= 4.75V) = 1.615V — dropout term is a tolerance stack, not a single number, so it can be checked by inspection.
  check: _VBUS_MIN - _VOUT >= _DROPOUT_MAX
  where _DROPOUT_MAX=1.15V, _VBUS_MIN=4.75V, _VOUT=3.3V
  HW-TB-COMP08: the LDO's input capacitance shall be >=4.7uF MINIMUM, not 5V nominal. At USB 2.0 7.2.2's 4.75V a high-power port leaves 0.35V over the 1.15V max dropout at the 4.40V floor: a bus-powered function must still work at the headroom is EXACTLY ZERO. Accepted. This is why HW-TB-COMP07(b) uses 4.75V, not 5V, and why the 10uF bulk capacitance is specified on top of this.
  HW-TB-CONN09 — C15: 10uF IS the whole USB inrush budget [USB 2.0 7.2.4.1 caps a bus-powered function at 10uF ||: 4ninh]. Nothing further goes on VBUS without re-deriving this or adding a soft-start. Bulk capacitance on VBUS belongs at the connector, not downstream, so it charges through its current limit, not through the cable, so it does not cause
  HW-TB-COMP02a / D16 — the NCP1117's 4.7uF, ESR 33mohm-2.2ohm[1 in ONE POINT on a boundary curve, not two independent limits. At the 10uF fitted the ESR floor is 20.1mohm; at the~25.5uF the loop really sees it is 10mohm. Paralleling MLCCs on this rail therefore INCREASES margin, contrary to the datasheet's "minimum". This is not provable from archived data — open verification item, closed by a bench step-load.
  NCP1117 datasheet — C1 must sit within the shortest possible track of U2's input and ground terminals.

CORE0R0
  HW-TB-RP2040-DS section 2.1: VREG_AVDD draws ~200uA through a 33 ohm filter resistor. The IR drop is so negligible against the 3.3V rail or the analogue supply is starved.
  check: _C_DROP < _Voltage*10mV?
  HW-TB-RP2040-DS section 2.9.1.1: VCC/CC/VCS/RS/LS must follow the RP-008280-DS Figure 23 geometry, adjacent to the VREG pins.
  HW-TB-COMP03 — L1 is polarity-marked and its orientation is NOT automated. A reversed part is a dead board. Verify pin 1 against the footprint.
  F3 — VREG_PGND is on the GND net. RP-008280-DS 2.1 requires its switching current to return directly to PGND as a star point without disturbing the rest of GND. That is a ROUTING specification this matrix cannot express.
  F2 — the~spec 8/4 asks for a DVDD test point; none is fitted. Probe the C7 or C10 pads, or L1 pad 2.

MCU
  HW-TB-COMP06 [D15] — 15 supply pins covered by 13 capacitors. 100% coverage. Pins 44/45 share one cap and pins 53/54 share another; both are RP-008280-DS 2.2.1's own documented sharing deviation. C10 is the 4.7uF at DVDD, deviation (b), and belongs on the side of the package opposite the other bulk caps.
  Ask the coverage question per PIN, never per capacitor. The eight VCC3V3 decouplers are one net and one MPN and are electrically interchangeable, so which pin a cap is NAMED for is a cosmetic choice, not a coverage gap. The audit counts pins, not capacitors.
  F2 — ADC_AVDD (pin 44) lies straight to VCC3V3 and shares its decoupling with pin 45, matching the RP1 reference, which fits no ADC_AVDD filter. Consequence: NO ADC ACCURACY CLAIM can be made on this board.
  Rail ranges are declared on the io[] rather than asserted in a check[]: an io[foo=1] does not
  surface the caller's voltage at module-evaluation time, so such a check would pass unconditionally — worse than none. DVDD 1.8-3.3V is the package range; this board runs 3.3V.

FLASH
  F3 — boot depends on the RP2350's pad pull-ups on SD2/SD3, with QE=0 the flash's own WP#/HOLD# are floating inputs. Nothing in this schematic guarantees, therefore, a boot. Nothing in this matrix does the same. If a bench build fails to boot, check this first: the fix is pull-ups on SD2/SD3 (~2.2 kohm).
  HW-TB-COMP06 — U3 pin 8 (flash VCC) needs a 100nF pad within 3mm, same rule as the MCU supply pins.

XTAL
  RP-008280-DS chapter 4, worked exactly as the guide works it: the two load capacitors are in series from the crystal's point of view. '15*C4/(C3+C4)', and stray capacitance from the PCB and pins adds to both sides. The guide assumes 3pF of stray and lands on 10.5pF against a 12pF target. Close enough.
  check: (_C_EFFECTIVE - _C_TARGET).abs() <= Capacitance("1pF")
  F1 — 12MHz 10pF, 50ppm, 2-pin.
  HW-TB-PCB22/PCB23 — each leg <=10mm, 0.15mm trace, ZERO vias, legs symmetric within 1mm, >=0.45mm from digital and switching nets. GND guard pour.
  R2 sits in the XOUT leg AHEAD of C4 — read off Raspberry Pi's shipped .kicad_pcb, not from the guide's prose, which is ambiguous on the ordering.

USB
  HW-TB-PCB16 HARD — R1/R8 (27 ohm series) shall be placed close to the MCU; not to the connector. Long unbuffered traces from connector to MCU degrade signal margin.
  HW-TB-CONN04 — the two CC pulldowns shall NEVER be tied together. A single shared 5.1k still enumerates on an A-to-C cable and fails only on C-to-C, which is exactly the bug that survives casual bench testing.

SWD
  J2 — RP-008189-DS's 100 ohm source-termination resistors on SWCLK/SWDIO are 'highly recommended' but NOT fitted: the part budget is fixed at 39 and RP's own RP2350 Minimal omits them too. What
  is given up is slew limiting and ESD/short-circuit current limiting on the two debug pins.

BUTTONS
  R6 — external pull-ups and no RC debounce, both deliberate: RUN and QSPI_SS both have internal pull-ups, and BOOTSEL is sampled once at reset where contact bounce is harmless.

LED
  Two independent bounds: the APT2012SGC's 25mA absolute maximum forward current, and a floor that keeps the indicator actually visible.
  F1 — R3 = 1k, 2.2V, 1.0mA, 0.22W. The installations below rather than repeated there as string literals, that is what makes these checks bind with independent literals, editing one value changed the nameplate and the check went on passing over its own private constants — a consistency assertion about nothing.
  _V_F is the datasheet's 2.2V typ AT If=20mA. <8% this operating point. A 5mA green dim LED would read 1.9V and still pass this check — the datasheet curve is not modelled here.
  using If max 2.0V instead gives 0.80mA. The honest reading is a band of roughly 0.8-1.5mA, not the point value 1mA<spec.mid's power budget calls "defined". Both bounds below hold across it.
  check: _I_MAX <= _I_ABSMAX(1mA)
  check: _LED > Current("0.5mA")
  F7 — GPIO25 is Pico's own LED pin, so stock Pico firmware blinks this board unchanged. The cost is one GPIO and one pin. Anode to 3V3, cathode to CC1 on the short edge. GPIO16/17/18 on side B are free alternates if placement gets tight.

GPIOA
  HW-TB-CONN03 — a castellated edge row is a PCB feature, not a purchased part; 10 pads, zero solder joints, BOM quantity 0. Ten pads per edge is 62.5% of the 4.80mm routing channel; twenty would be 125% and would not fit.

GPIOC
  HW-TB-CONN03 — a castellated edge row is a PCB feature, not a purchased part; 10 pads, zero solder joints, BOM quantity 0. Ten pads per edge is 62.5% of the 4.80mm routing channel; twenty would be 125% and would not fit.

%2 components on one flat sheet; module frames replace the page hierarchy
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Small RP2350A test board (39 components, 2L, 51x21mm) used as a...
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File: test-board.kicad_sch

Title: test-board -- all sheets
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KiCad 7.0.X, 10.0.2 | Id: 1/1