# ARTIX UltraScale+
# SoM Module
# ACAU15
# User Manual

ALINX

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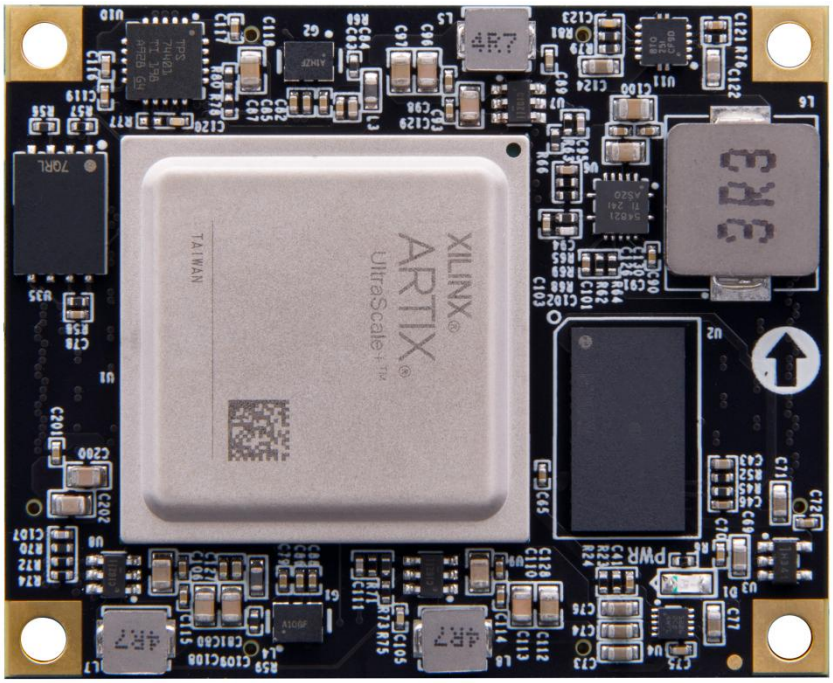
# 1. ACAU15 Core Board Introduction

ACAU15 (core board model, the same below) FPGA core board, adopt ARTIX chip, it is based on XCAU15P-2FFVB676I of XILINX company ARTIX UltraScale+ Family. This high-performance core board developed by this chip has the characteristics of high speed, high bandwidth, high capacity, and is suitable for use in high-speed data communication, video image processing, high-speed data acquisition, and other fields.

This core board uses one Micron's DDR4 Chip MT40A512M16LY-062EIT, with a 16 bit data bus bandwidth and a total capacity of 8Gb; The maximum operating speed of DDR4 SDRAM can reach 1200MHz (data rate 2400Mbps). In addition, a 256MBit QSPI FLASH is also integrated on the core board for starting storage configurations and system files.

This core board extends to 72 IO ports with level standard 3.3V, 102 IO ports with level standard 1.8V, and 12 pairs of GTH high-speed RX/TX differential signals. For users who require a lot of IO, this core board will be a good choice. Moreover, the routing between the FPGA chip and the interface has been processed with equal length and differential processing, and the core board size is only 45 * 55 (mm), which is very suitable for secondary development.




ACAU15 Front view

## 2. FPGA Chip

The FPGA development board uses Xilinx's ARTIX UltraScale+ FPGA chip, model number XCAU15P-2FFVB676I. The speed class is 2 and the temperature class is industrial. This model is a FFVB676 package with 676 pins. The chip naming rules for Xilinx ARTIX UltraScale+ FPGA are shown in Figure 2-1 below:

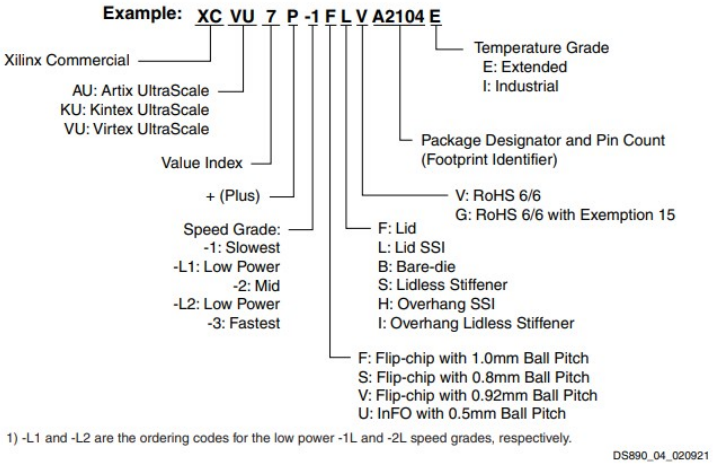



*Figure 4:* **UltraScale+ FPGA Ordering Information**

**The main parameters of the FPGA chip XCAU15P are as follows:**

| Name | Specific parameters |
|---|---|
| Logic Cells | 170100 |
| CLB LUTs | 77760 |
| CLB flip-flops | 155520 |
| Block RAM (kb) | 5223 |
| DSP Slices | 576 |
| CMTs | 3 |
| GTH 16.3Gb/s Transceiver | 12 |
| Speed Grade | -2 |
| Temperature Grade | Industrial |

## 3. Active Differential Crystal Oscillator

The core board ACAU15 is equipped with two active differential crystal oscillators from Sitime Corporation, one is at 200MHz and model SiT9121AI-2B1-33E200.00000, used for the system master clock of FPGA and for generating DDR4 control clock; The other

one is at 156.25MHz, model SiT9121AI-2B1-33E156.250000, used for the reference clock input of the GTH transceiver.

### 3.1 200Mhz differential clock

In Figure 3-1, G1 is the system clock source for 200M active differential crystal oscillator circuit we mentioned above for the development board. The crystal oscillator output is connected to the BANK65 global clock pin MRCC (T24 and U24) of the FPGA. This 200Mhz differential clock can be used to drive the user logic circuit inside of the FPGA. Users can generate clocks of different frequencies by configuring the PLLs and DCMs inside of the FPGA.

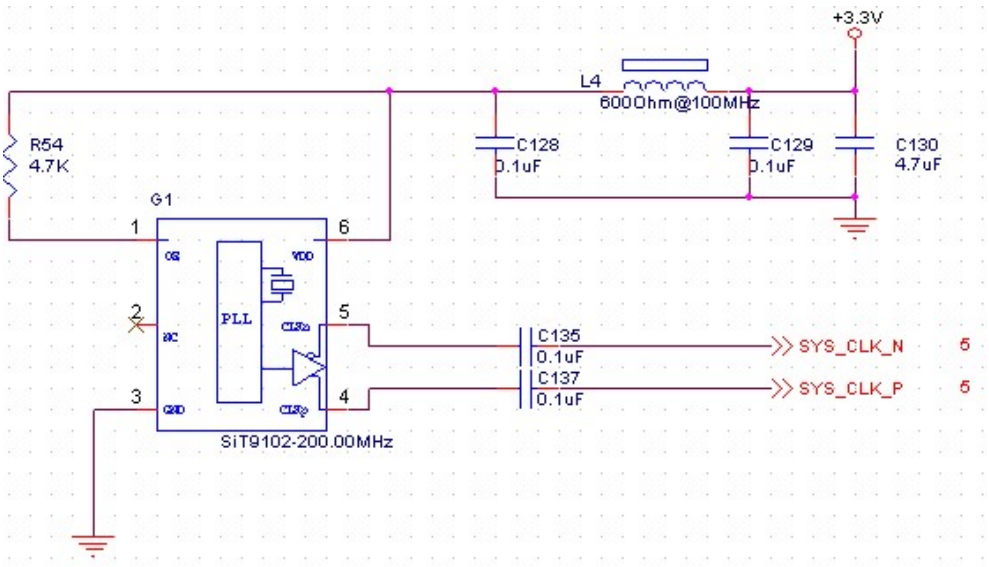



Figure 3-1 200M Active differential crystal oscillator

**System Clock pin assignments:**

| Signal Name | FPGA Pin |
|---|---|
| **SYS_CLK_P** | T24 |
| **SYS_CLK_N** | U24 |

### 3.2 156.25 Mhz differential clock

In Figure 3-2, G2 is the 156.25M active differential crystal oscillator circuit, where the clock serves as a reference input clock for the GTH module inside of the FPGA. Crystal oscillator output connected to BANK225 clock pin MGTREFCLK1P of FPGA GTH_ 225 (T7) and MGTREFCLK1N_ 225 (T6).

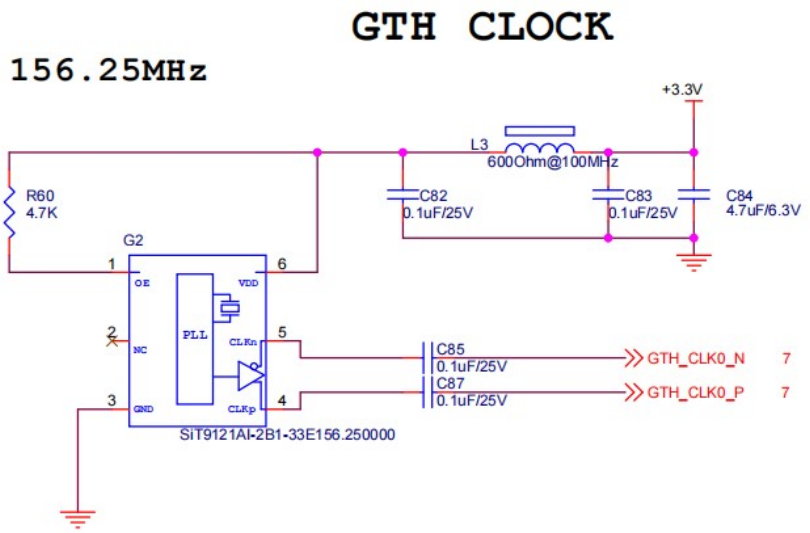



Figure 3-2 156.25Mhz Active differential crystal oscillator

**System Clock pin assignments:**

| Signal Name | FPGA Pin |
|---|---|
| **GTH_CLK0_P** | T7 |
| **GTH_CLK0_N** | T6 |

## 4. DDR4

The ACAU15 core board is equipped with Micron's 8Gbit DDR4 chip, model MT40A512M16LY-062EIT. The bus width of DDR is a total of 16 bits. The maximum operating speed of DDR4 SDRAM can reach 1200MHz (data rate 2400Mbps). The DDR4 storage system is directly connected to the memory interface of the FPGA's BANK 66. The specific configuration of DDR4 SDRAM is shown in Table 4-1.

Table 2-4-1 DDR3 SDRAM Configuration

| Bit No. | Chip Model | Capacity | Manufacturer |
|---|---|---|---|
| U2 | MT40A512M16LY-062EIT | 512M x 16bit | micron |

The hardware design of DDR4 requires strict consideration of signal integrity. When designing the circuit and PCB, we have fully considered matching resistance/terminal resistance, line impedance control, and line length control to ensure the high-speed and stable operation of DDR4.

The hardware connection method between FPGA and DDR4 DRAM is shown in Figure 4-1:

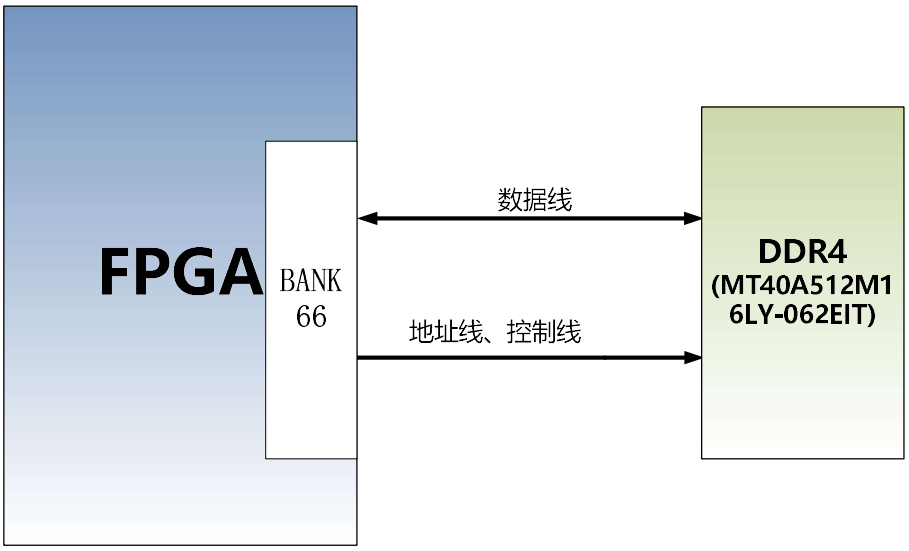



Figure 4-1 DDR4 DRAM Schematic

**DDR4 DRAM pin assignments:**

| Signal Name | FPGA Pin Name | FPGA Pin No. |
|---|---|---|
| PL_DDR4_A0 | IO_L13N_T2L_N1_GC_QBC_66 | G25 |
| PL_DDR4_A1 | IO_L8N_T1L_N3_AD5N_66 | M26 |
| PL_DDR4_A2 | IO_L10N_T1U_N7_QBC_AD4N_66 | L25 |
| PL_DDR4_A3 | IO_L19N_T3L_N1_DBC_AD9N_66 | E26 |
| PL_DDR4_A4 | IO_L8P_T1L_N2_AD5P_66 | M25 |
| PL_DDR4_A5 | IO_T3U_N12_66 | F22 |
| PL_DDR4_A6 | IO_L17P_T2U_N8_AD10P_66 | H26 |
| PL_DDR4_A7 | IO_L16P_T2U_N6_QBC_AD3P_66 | F24 |
| PL_DDR4_A8 | IO_L17N_T2U_N9_AD10N_66 | G26 |
| PL_DDR4_A9 | IO_L12P_T1U_N10_GC_66 | J23 |
| PL_DDR4_A10 | IO_L15P_T2L_N4_AD11P_66 | J25 |
| PL_DDR4_A11 | IO_L12N_T1U_N11_GC_66 | J24 |
| PL_DDR4_A12 | IO_L16N_T2U_N7_QBC_AD3N_66 | F25 |
| PL_DDR4_A13 | IO_L14N_T2L_N3_GC_66 | H24 |
| PL_DDR4_ACT_B | IO_L9P_T1L_N4_AD12P_66 | K25 |
| PL_DDR4_BA0 | IO_L15N_T2L_N5_AD11N_66 | J26 |
| PL_DDR4_BA1 | IO_T2U_N12_66 | G22 |
| PL_DDR4_BG0 | IO_L7P_T1L_N0_QBC_AD13P_66 | L22 |

| | | |
|---|---|---|
| PL_DDR4_CAS_B | IO_L18N_T2U_N11_AD2N_66 | H22 |
| PL_DDR4_CKE | IO_L7N_T1L_N1_QBC_AD13N_66 | L23 |
| PL_DDR4_CLK_N | IO_L11N_T1U_N9_GC_66 | K23 |
| PL_DDR4_CLK_P | IO_L11P_T1U_N8_GC_66 | K22 |
| PL_DDR4_CS_B | IO_L14P_T2L_N2_GC_66 | H23 |
| PL_DDR4_PAR | IO_L10P_T1U_N6_QBC_AD4P_66 | L24 |
| PL_DDR4_RAS_B | IO_L18P_T2U_N10_AD2P_66 | H21 |
| PL_DDR4_OTD | IO_T1U_N12_66 | M24 |
| PL_DDR4_WE_B | IO_L9N_T1L_N5_AD12N_66 | K26 |
| PL_DDR4_DM0 | IO_L19P_T3L_N0_DBC_AD9P_66 | E25 |
| PL_DDR4_DM1 | IO_L1P_T0L_N0_DBC_66 | L18 |
| PL_DDR4_DQ0 | IO_L20P_T3L_N2_AD1P_66 | F23 |
| PL_DDR4_DQ1 | IO_L21N_T3L_N5_AD8N_66 | D25 |
| PL_DDR4_DQ2 | IO_L20N_T3L_N3_AD1N_66 | E23 |
| PL_DDR4_DQ3 | IO_L24N_T3U_N11_66 | B26 |
| PL_DDR4_DQ4 | IO_L21P_T3L_N4_AD8P_66 | D24 |
| PL_DDR4_DQ5 | IO_L23P_T3U_N8_66 | D26 |
| PL_DDR4_DQ6 | IO_L24P_T3U_N10_66 | B25 |
| PL_DDR4_DQ7 | IO_L23N_T3U_N9_66 | C26 |
| PL_DDR4_DQ8 | IO_L2P_T0L_N2_66 | M20 |
| PL_DDR4_DQ9 | IO_L3N_T0L_N5_AD15N_66 | J20 |
| PL_DDR4_DQ10 | IO_L3P_T0L_N4_AD15P_66 | J19 |
| PL_DDR4_DQ11 | IO_L2N_T0L_N3_66 | M21 |
| PL_DDR4_DQ12 | IO_L6P_T0U_N10_AD6P_66 | L20 |
| PL_DDR4_DQ13 | IO_L5N_T0U_N9_AD14N_66 | J21 |
| PL_DDR4_DQ14 | IO_L6N_T0U_N11_AD6N_66 | K20 |
| PL_DDR4_DQ15 | IO_L5P_T0U_N8_AD14P_66 | K21 |
| PL_DDR4_DQS0_N | IO_L22N_T3U_N7_DBC_AD0N_66 | C24 |
| PL_DDR4_DQS0_P | IO_L22P_T3U_N6_DBC_AD0P_66 | D23 |
| PL_DDR4_DQS1_N | IO_L4N_T0U_N7_DBC_AD7N_66 | L19 |
| PL_DDR4_DQS1_P | IO_L4P_T0U_N6_DBC_AD7P_66 | M19 |
| PL_DDR4_RST | IO_L13P_T2L_N0_GC_QBC_66 | G24 |

## 5. QSPI Flash

A 256Mbit QSPI FLASH chip with the model MT25QU256ABA1EW9-0SIT is used on the core board, which uses the 1.8V CMOS voltage standard. Due to its non-volatile nature, QSPI FLASH can serve as the boot image for FPGA systems in use. These images mainly include FPGA bit files, soft core application code, and other user data files.

The specific models and related parameters of SPI FLASH are shown in the table below:

| Position | Model | Capacity | Factory |
|---|---|---|---|
| U35 | MT25QU256ABA1EW9-0SIT | 256M Bit | Micron |

Table 5-1 QSPI FLASH Specification

QSPI FLASH is connected to the dedicated pins of BANK0 on the FPGA chip, The clock pin is connected to the CCLK0 of BANK0, and other data and chip selection signals are connected to the D00-D03 and FCS pins of BANK0, respectively. Figure 5-1 is a schematic diagram of the connection between QSPI Flash and FPGA chips.

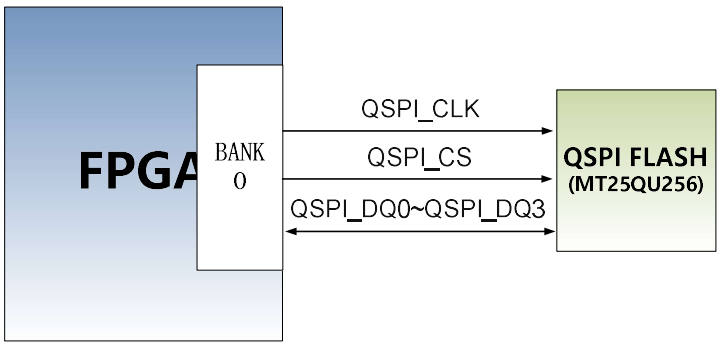



Figure 5-1 QSPI Flash Schematic

**QSPI Flash pin assignments:**

| Signal Name | FPGA Pin Name | FPGA Pin No. |
|---|---|---|
| QSPI_CLK | CCLK_0 | Y11 |
| QSPI_CS | RDWR_FCS_B_0 | AA12 |
| QSPI_DQ0 | D00_MOSI_0 | AD11 |
| QSPI_DQ1 | D01_DIN_0 | AC12 |
| QSPI_DQ2 | D02_0 | AC11 |
| QSPI_DQ3 | D03_0 | AE11 |

## 6. LED Light

There is one red LED on the ACAU15 core board, which is the power indicator light (PWR). When the core board is powered on, the power indicator light will light up; The schematic diagram of LED light hardware connection is shown in Figure 6-1:

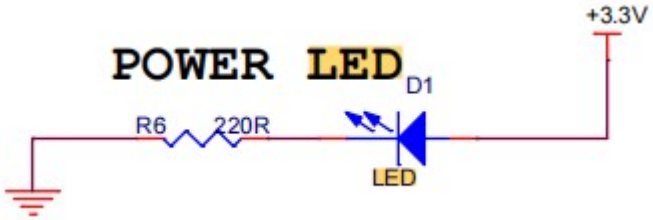
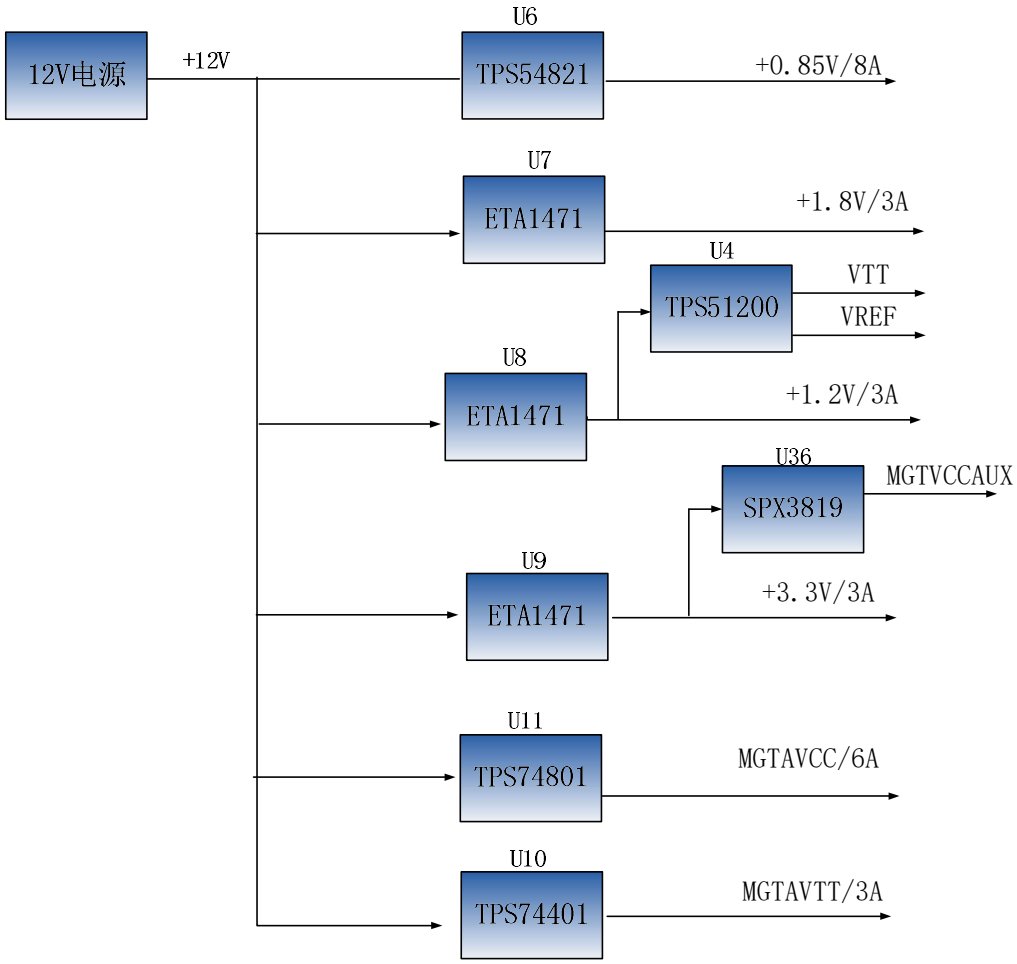



Figure 6-1 Schematic diagram of LED light hardware connection

## 7. Power Supply

The power supply voltage range of the ACAU15 core board is+5V~+17V (typical value+12V), which is supplied to the core board by connecting the Carrier Board. On the core board, the TPS54821RHL DCDC power chip provides core power of 0.85V for XCAU15P. In addition, the power supplies for BANK64, BANK65, and BANK66 are generated using the DCDC chip ETA1471. Users can replace the resistor to change the IO level to 1.2V (note that these BANK power supplies cannot exceed 1.8V), and the IO levels for BANK84, 85, and 86 are 3.3V. The power supply of the GTH transceiver is generated by the LDO chip.




As the power supply of Artix UltraScale+FPGA requires a power on sequence, we have designed the circuit according to the power supply requirements of the chip. The sequence of the power is like : VCCINT (1.0V) ->VCCBRAM (1.0V) ->(1.5V, 3.3V, VCCIO) and 1.0V ->MGTAVCC ->MGTAVTT, ensuring the normal operation of the chip.

## 8. Expansion Port

The back of the core board has a total of 4 high-speed expansion ports, connected to the carrier board using 4 80Pin inter board connectors. The IO ports of the FPGA are connected to these 4 expansion ports through differential cabling. The PIN pin spacing of the connector is 0.5mm, and it is configured with the motherboard connector to achieve high-speed data communication.

**Expansion Port CON1**

The 80 Pin connector CON1 is used to connect the VCCIN power supply (+12V) of the carrier board, ground, and regular IO of the FPGA. It should be noted that CON1 has 52 pins connected to the IO port of BANK64, and the voltage standard is 1.8V. The pin allocation of the CON1 expansion port is shown in Figure 2-8-1:

Figure 2-8-1: Expansion CON1Pin Assignment

| CON1 Pin | Signal Name | FPGA Pin No. | Level standard | CON1 Pin | Signal Name | FPGA Pin No. | Level standard |
|---|---|---|---|---|---|---|---|
| PIN1 | VCCIN | - | 12V | PIN2 | VCCIN | - | 12V |
| PIN3 | VCCIN | - | 12V | PIN4 | VCCIN | - | 12V |
| PIN5 | VCCIN | - | 12V | PIN6 | VCCIN | - | 12V |
| PIN7 | VCCIN | - | 12V | PIN8 | VCCIN | - | 12V |
| PIN9 | GND | - | GND | PIN10 | GND | - | GND |
| PIN11 | B64_T0U | AF23 | 1.8V | PIN12 | B64_L4_N | AD26 | 1.8V |
| PIN13 | B64_T1U | AF20 | 1.8V | PIN14 | B64_L4_P | AC26 | 1.8V |
| PIN15 | B64_T2U | AE18 | 1.8V | PIN16 | B64_L2_N | AB26 | 1.8V |
| PIN17 | B64_T3U | AC16 | 1.8V | PIN18 | B64_L2_P | AB25 | 1.8V |
| PIN19 | GND | - | GND | PIN20 | GND | - | GND |
| PIN21 | B64_L10_N | AB22 | 1.8V | PIN22 | B64_L1_N | AE26 | 1.8V |
| PIN23 | B64_L10_P | AA22 | 1.8V | PIN24 | B64_L1_P | AE25 | 1.8V |
| PIN25 | B64_L8_N | AE23 | 1.8V | PIN26 | B64_L3_N | AF25 | 1.8V |
| PIN27 | B64_L8_P | AD23 | 1.8V | PIN28 | B64_L3_P | AF24 | 1.8V |
| PIN29 | GND | - | GND | PIN30 | GND | - | GND |
| PIN31 | B64_L7_N | AF22 | 1.8V | PIN32 | B64_L6_N | AC24 | 1.8V |
| PIN33 | B64_L7_P | AE22 | 1.8V | PIN34 | B64_L6_P | AB24 | 1.8V |
| PIN35 | B64_L9_N | AC23 | 1.8V | PIN36 | B64_L5_N | AD25 | 1.8V |
| PIN37 | B64_L9_P | AC22 | 1.8V | PIN38 | B64_L5_P | AD24 | 1.8V |
| PIN39 | GND | - | GND | PIN40 | GND | - | GND |
| PIN41 | B64_L12_N | AC21 | 1.8V | PIN42 | B64_L11_N | AE21 | 1.8V |
| PIN43 | B64_L12_P | AB21 | 1.8V | PIN44 | B64_L11_P | AD21 | 1.8V |
| PIN45 | B64_L14_N | AD19 | 1.8V | PIN46 | B64_L13_N | AE20 | 1.8V |
| PIN47 | B64_L14_P | AC19 | 1.8V | PIN48 | B64_L13_P | AD20 | 1.8V |
| PIN49 | GND | - | GND | PIN50 | GND | - | GND |
| PIN51 | B64_L19_N | Y21 | 1.8V | PIN52 | B64_L21_N | AB20 | 1.8V |
| PIN53 | B64_L19_P | Y20 | 1.8V | PIN54 | B64_L21_P | AA20 | 1.8V |
| PIN55 | B64_L20_N | AB19 | 1.8V | PIN56 | B64_L24_N | AA18 | 1.8V |
| PIN57 | B64_L20_P | AA19 | 1.8V | PIN58 | B64_L24_P | Y18 | 1.8V |
| PIN59 | GND | - | GND | PIN60 | GND | - | GND |
| PIN61 | B64_L23_N | AA17 | 1.8V | PIN62 | B64_L15_N | AF19 | 1.8V |
| PIN63 | B64_L23_P | Y17 | 1.8V | PIN64 | B64_L15_P | AF18 | 1.8V |
| PIN65 | B64_L18_N | AE16 | 1.8V | PIN66 | B64_L17_N | AF17 | 1.8V |
| PIN67 | B64_L18_P | AD16 | 1.8V | PIN68 | B64_L17_P | AE17 | 1.8V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PIN69 | GND | - | GND | PIN70 | GND | - | GND |
| PIN71 | FPGA_DONE | AB11 | 1.8V | PIN72 | B64_L16_N | AD18 | 1.8V |
| PIN73 | PROGRAM_B | AB9 | 1.8V | PIN74 | B64_L16_P | AC18 | 1.8V |
| PIN75 | INIT_B | W10 | 1.8V | PIN76 | B64_L22_N | AC17 | 1.8V |
| PIN77 | NC | - | Null | PIN78 | B64_L22_P | AB17 | 1.8V |
| PIN79 | NC | - | Null | PIN80 | NC | - | Null |

**Expansion port CON2**

The connector CON2 of 80Pin is used to expand the IO of BANK65 and BANK84, as well as 4-way JTAG signals in FPGA. The voltage standard of BANK84 is 3.3V, while the voltage standard of BANK65 is 1.8V. The pin allocation of the CON2 expansion port is shown in Figure 2-8-2:

**Figure 2-8-2: Expansion CON2 Pin Assignment**

| CON2 Pin | Signal Name | FPGA Pin No. | Level standard | CON2 Pin | Signal Name | FPGA Pin No. | Level standard |
|---|---|---|---|---|---|---|---|
| PIN1 | B65_L22_N | P23 | 1.8V | PIN2 | B65_T2U | N26 | 1.8V |
| PIN3 | B65_L22_P | N23 | 1.8V | PIN4 | B65_T1U | AA23 | 1.8V |
| PIN5 | B65_L18_N | R26 | 1.8V | PIN6 | B65_T0U | W21 | 1.8V |
| PIN7 | B65_L18_P | R25 | 1.8V | PIN8 | B65_T3U | T19 | 1.8V |
| PIN9 | GND | - | GND | PIN10 | GND | - | GND |
| PIN11 | B65_L14_N | U25 | 1.8V | PIN12 | B65_L24_N | N22 | 1.8V |
| PIN13 | B65_L14_P | T25 | 1.8V | PIN14 | B65_L24_P | N21 | 1.8V |
| PIN15 | B65_L17_N | P26 | 1.8V | PIN16 | B65_L15_N | P24 | 1.8V |
| PIN17 | B65_L17_P | P25 | 1.8V | PIN18 | B65_L15_P | N24 | 1.8V |
| PIN19 | GND | - | GND | PIN20 | GND | - | GND |
| PIN21 | B65_L16_N | V26 | 1.8V | PIN22 | B65_L19_N | R23 | 1.8V |
| PIN23 | B65_L16_P | U26 | 1.8V | PIN24 | B65_L19_P | R22 | 1.8V |
| PIN25 | B65_L10_N | W26 | 1.8V | PIN26 | B65_L5_N | T23 | 1.8V |
| PIN27 | B65_L10_P | W25 | 1.8V | PIN28 | B65_L5_P | T22 | 1.8V |
| PIN29 | GND | - | GND | PIN30 | GND | - | GND |
| PIN31 | B65_L11_N | W23 | 1.8V | PIN32 | B65_L12_N | W24 | 1.8V |
| PIN33 | B65_L11_P | V23 | 1.8V | PIN34 | B65_L12_P | V24 | 1.8V |
| PIN35 | B65_L2_N | U22 | 1.8V | PIN36 | B65_L8_N | Y26 | 1.8V |
| PIN37 | B65_L2_P | U21 | 1.8V | PIN38 | B65_L8_P | Y25 | 1.8V |
| PIN39 | GND | - | GND | PIN40 | GND | - | GND |
| PIN41 | B65_L23_N | P19 | 1.8V | PIN42 | B65_L21_N | R21 | 1.8V |
| PIN43 | B65_L23_P | N19 | 1.8V | PIN44 | B65_L21_P | R20 | 1.8V |
| PIN45 | B65_L3_N | U20 | 1.8V | PIN46 | B65_L4_N | V22 | 1.8V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PIN47 | B65_L3_P | T20 | 1.8V | PIN48 | B65_L4_P | V21 | 1.8V |
| PIN49 | GND | - | GND | PIN50 | GND | - | GND |
| PIN51 | B65_L20_N | P21 | 1.8V | PIN52 | B65_L9_N | AA25 | 1.8V |
| PIN53 | B65_L20_P | P20 | 1.8V | PIN54 | B65_L9_P | AA24 | 1.8V |
| PIN55 | B65_L6_N | W20 | 1.8V | PIN56 | B65_L7_N | Y23 | 1.8V |
| PIN57 | B65_L6_P | W19 | 1.8V | PIN58 | B65_L7_P | Y22 | 1.8V |
| PIN59 | GND | - | GND | PIN60 | GND | - | GND |
| PIN61 | B65_L1_N | V19 | 1.8V | PIN62 | B84_L2_N | AF13 | 3.3V |
| PIN63 | B65_L1_P | U19 | 1.8V | PIN64 | B84_L2_P | AE13 | 3.3V |
| PIN65 | B84_L6_N | AB16 | 3.3V | PIN66 | B84_L1_N | AF15 | 3.3V |
| PIN67 | B84_L6_P | AB15 | 3.3V | PIN68 | B84_L1_P | AF14 | 3.3V |
| PIN69 | GND | - | GND | PIN70 | GND | - | GND |
| PIN71 | FPGA_TCK | AE12 | 1.8V | PIN72 | B84_L3_N | AE15 | 3.3V |
| PIN73 | FPGA_TDI | AB12 | 1.8V | PIN74 | B84_L3_P | AD15 | 3.3V |
| PIN75 | FPGA_TMS | AB10 | 1.8V | PIN76 | B84_L4_N | AD14 | 3.3V |
| PIN77 | FPGA_TDO | Y10 | 1.8V | PIN78 | B84_L4_P | AD13 | 3.3V |
| PIN79 | NC | - | Null | PIN80 | NC | - | Null |

**Expansion port CON3**

The 80Pin connector CON3 is used to extend the regular IO of BANK84, BANK85, and BANK86 in FPGA. The voltage standards for BANK84, BANK85, and BANK86 are all 3.3V. The pin allocation of the CON3 expansion port is shown in Figure 2-8-3:

**Figure 2-8-3: Expansion CON3 Pin Assignment**

| CON3 Pin | Signal Name | FPGA Pin No. | Level standard | CON3 Pin | Signal Name | FPGA Pin No. | Level standard |
|---|---|---|---|---|---|---|---|
| PIN1 | B84_L8_N | AB14 | 3.3V | PIN2 | B84_L5_N | AC14 | 3.3V |
| PIN3 | B84_L8_P | AA14 | 3.3V | PIN4 | B84_L5_P | AC13 | 3.3V |
| PIN5 | B84_L12_N | W13 | 3.3V | PIN6 | B84_L11_N | AA13 | 3.3V |
| PIN7 | B84_L12_P | W12 | 3.3V | PIN8 | B84_L11_P | Y13 | 3.3V |
| PIN9 | GND | - | GND | PIN10 | GND | - | GND |
| PIN11 | B84_L7_N | AA15 | 3.3V | PIN12 | B84_L9_N | Y16 | 3.3V |
| PIN13 | B84_L7_P | Y15 | 3.3V | PIN14 | B84_L9_P | W16 | 3.3V |
| PIN15 | B84_L10_N | W15 | 3.3V | PIN16 | NC | | Null |
| PIN17 | B84_L10_P | W14 | 3.3V | PIN18 | NC | | Null |
| PIN19 | GND | - | GND | PIN20 | GND | - | GND |
| PIN21 | B85_L1_N | K9 | 3.3V | PIN22 | B85_L3_N | H9 | 3.3V |
| PIN23 | B85_L1_P | K10 | 3.3V | PIN24 | B85_L3_P | J9 | 3.3V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PIN25 | B85_L2_N | J10 | 3.3V | PIN26 | B85_L6_N | F9 | 3.3V |
| PIN27 | B85_L2_P | J11 | 3.3V | PIN28 | B85_L6_P | F10 | 3.3V |
| PIN29 | GND | - | GND | PIN30 | GND | - | GND |
| PIN31 | B85_L4_N | G11 | 3.3V | PIN32 | B85_L5_N | G9 | 3.3V |
| PIN33 | B85_L4_P | H11 | 3.3V | PIN34 | B85_L5_P | G10 | 3.3V |
| PIN35 | B85_L11_N | A10 | 3.3V | PIN36 | B85_L9_N | C9 | 3.3V |
| PIN37 | B85_L11_P | B10 | 3.3V | PIN38 | B85_L9_P | D9 | 3.3V |
| PIN39 | GND | - | GND | PIN40 | GND | - | GND |
| PIN41 | B85_L8_N | D10 | 3.3V | PIN42 | B85_L10_N | A9 | 3.3V |
| PIN43 | B85_L8_P | D11 | 3.3V | PIN44 | B85_L10_P | B9 | 3.3V |
| PIN45 | B85_L7_N | E10 | 3.3V | PIN46 | B85_L12_N | B11 | 3.3V |
| PIN47 | B85_L7_P | E11 | 3.3V | PIN48 | B85_L12_P | C11 | 3.3V |
| PIN49 | GND | - | GND | PIN50 | GND | - | GND |
| PIN51 | B86_L2_N | H13 | 3.3V | PIN52 | B86_L1_N | H12 | 3.3V |
| PIN53 | B86_L2_P | J13 | 3.3V | PIN54 | B86_L1_P | J12 | 3.3V |
| PIN55 | B86_L4_N | J14 | 3.3V | PIN56 | B86_L5_N | F12 | 3.3V |
| PIN57 | B86_L4_P | J15 | 3.3V | PIN58 | B86_L5_P | G12 | 3.3V |
| PIN59 | GND | - | GND | PIN60 | GND | - | GND |
| PIN61 | B86_L9_N | C13 | 3.3V | PIN62 | B86_L3_N | G14 | 3.3V |
| PIN63 | B86_L9_P | C14 | 3.3V | PIN64 | B86_L3_P | H14 | 3.3V |
| PIN65 | B86_L8_N | D13 | 3.3V | PIN66 | B86_L7_N | E12 | 3.3V |
| PIN67 | B86_L8_P | D14 | 3.3V | PIN68 | B86_L7_P | E13 | 3.3V |
| PIN69 | GND | - | GND | PIN70 | GND | - | GND |
| PIN71 | B86_L11_N | A12 | 3.3V | PIN72 | B86_L10_N | B12 | 3.3V |
| PIN73 | B86_L11_P | A13 | 3.3V | PIN74 | B86_L10_P | C12 | 3.3V |
| PIN75 | B86_L6_N | F13 | 3.3V | PIN76 | B86_L12_N | A14 | 3.3V |
| PIN77 | B86_L6_P | F14 | 3.3V | PIN78 | B86_L12_P | B14 | 3.3V |
| PIN79 | NC | - | Null | PIN80 | NC | - | Null |

**Expansion port CON4**

The 80Pin connector CON4 is used to extend the transceiver interfaces of BANK224, BANK225, and BANK226 in FPGA. The pin allocation of the CON4 expansion port is shown in Figure 2-8-4:

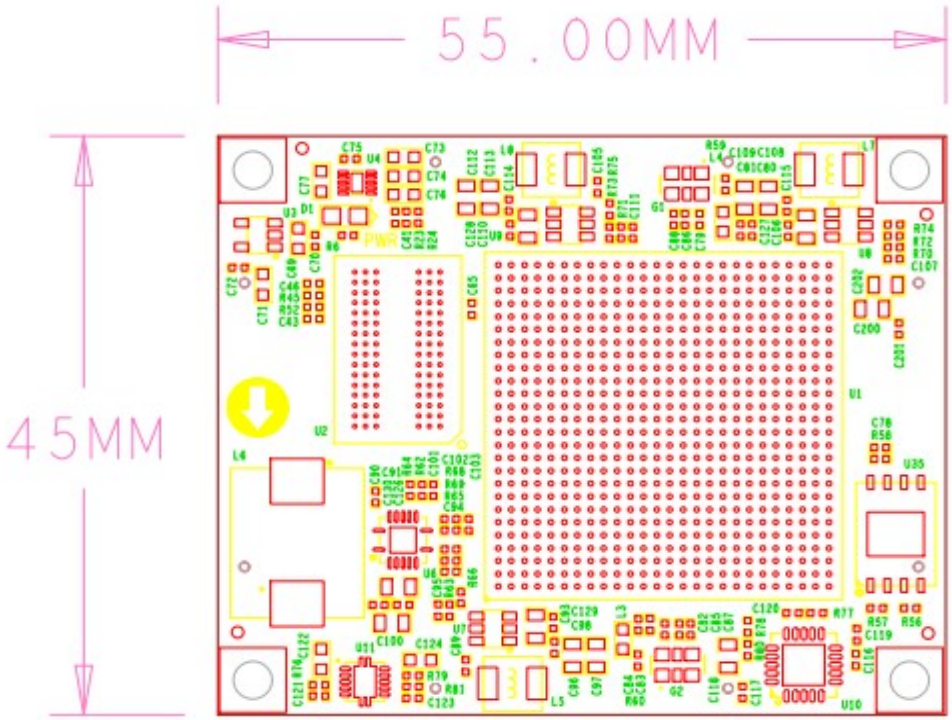
**Figure 2-8-4: Expansion CON4 Pin Assignment**

| CON4 Pin | Signal Name | FPGA Pin No. | Level standard | CON4 Pin | Signal Name | FPGA Pin No. | Level standard |
|---|---|---|---|---|---|---|---|
| PIN1 | 224_TX0_N | AF6 | 1.2V | PIN2 | 224_RX0_N | AF1 | 1.2V |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| PIN3 | 224_TX0_P | AF7 | 1.2V | PIN4 | 224_RX0_P | AF2 | 1.2V |
| PIN5 | GND | - | GND | PIN6 | GND | - | GND |
| PIN7 | 224_TX1_N | AE8 | 1.2V | PIN8 | 224_RX1_N | AE3 | 1.2V |
| PIN9 | 224_TX1_P | AE9 | 1.2V | PIN10 | 224_RX1_P | AE4 | 1.2V |
| PIN11 | GND | - | GND | PIN12 | GND | - | GND |
| PIN13 | 224_TX2_N | AD6 | 1.2V | PIN14 | 224_RX2_N | AD1 | 1.2V |
| PIN15 | 224_TX2_P | AD7 | 1.2V | PIN16 | 224_RX2_P | AD2 | 1.2V |
| PIN17 | GND | - | GND | PIN18 | GND | - | GND |
| PIN19 | 224_TX3_N | AC4 | 1.2V | PIN20 | 224_RX3_N | AB1 | 1.2V |
| PIN21 | 224_TX3_P | AC5 | 1.2V | PIN22 | 224_RX3_P | AB2 | 1.2V |
| PIN23 | GND | - | GND | PIN24 | GND | - | GND |
| PIN25 | 225_CLK0_N | V6 | 1.2V | PIN26 | 224_CLK0_N | AB6 | 1.2V |
| PIN27 | 225_CLK0_P | V7 | 1.2V | PIN28 | 224_CLK0_P | AB7 | 1.2V |
| PIN29 | GND | - | GND | PIN30 | GND | - | GND |
| PIN31 | 225_TX0_N | AA4 | 1.2V | PIN32 | 225_RX0_N | Y1 | 1.2V |
| PIN33 | 225_TX0_P | AA5 | 1.2V | PIN34 | 225_RX0_P | Y2 | 1.2V |
| PIN35 | GND | - | GND | PIN36 | GND | - | GND |
| PIN37 | 225_TX1_N | W4 | 1.2V | PIN38 | 225_RX1_N | V1 | 1.2V |
| PIN39 | 225_TX1_P | W5 | 1.2V | PIN40 | 225_RX1_P | V2 | 1.2V |
| PIN41 | GND | - | GND | PIN42 | GND | - | GND |
| PIN43 | 225_TX2_N | U4 | 1.2V | PIN44 | 225_RX2_N | T1 | 1.2V |
| PIN45 | 225_TX2_P | U5 | 1.2V | PIN46 | 225_RX2_P | T2 | 1.2V |
| PIN47 | GND | - | GND | PIN48 | GND | - | GND |
| PIN49 | 225_TX3_N | R4 | 1.2V | PIN50 | 225_RX3_N | P1 | 1.2V |
| PIN51 | 225_TX3_P | R5 | 1.2V | PIN52 | 225_RX3_P | P2 | 1.2V |
| PIN53 | GND | - | GND | PIN54 | GND | - | GND |
| PIN55 | 226_TX0_N | N4 | 1.2V | PIN56 | 226_RX0_N | M1 | 1.2V |
| PIN57 | 226_TX0_P | N5 | 1.2V | PIN58 | 226_RX0_P | M2 | 1.2V |
| PIN59 | GND | - | GND | PIN60 | GND | - | GND |
| PIN61 | 226_TX1_N | L4 | 1.2V | PIN62 | 226_RX1_N | K1 | 1.2V |
| PIN63 | 226_TX1_P | L5 | 1.2V | PIN64 | 226_RX1_P | K2 | 1.2V |
| PIN65 | GND | - | GND | PIN66 | GND | - | GND |
| PIN67 | 226_TX2_N | J4 | 1.2V | PIN68 | 226_RX2_N | H1 | 1.2V |
| PIN69 | 226_TX2_P | J5 | 1.2V | PIN70 | 226_RX2_P | H2 | 1.2V |
| PIN71 | GND | - | GND | PIN72 | GND | - | GND |
| PIN73 | 226_TX3_N | G4 | 1.2V | PIN74 | 226_RX3_N | F1 | 1.2V |
| PIN75 | 226_TX3_P | G5 | 1.2V | PIN76 | 226_RX3_P | F2 | 1.2V |

| PIN77 | GND | - | GND | PIN78 | GND | - | GND |
|---|---|---|---|---|---|---|---|
| PIN79 | 226_CLK0_P | P7 | 1.2V | PIN80 | 226_CLK0_N | P6 | 1.2V |

## 9. Size Dimension




Top View