Xilinx FPGA Platform

User Manual

ACKU5 SoM

ALINX

Version Record

Version	Modify Record
REV1.0	First Release

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Part 1 ACKU5 SoM

Part 1.1 Introduction

ACKU5(SoM Module, the same below) SoM, FPGA chip is based on Xilinx FPGA Kintex Ultrascale+ main chip xcku5pffvb676 design. The SoM connects two DDR4 memory chips to the HP port of the FPGA to form 32-bit data bandwidth, and each DDR4 capacity is up to 1GB. The memory bandwidth on the HP side is up to 85Gb/s. In addition, the SoM is also integrated with two 256MBit QSPI FLASH, used to start storage configuration and system files.

The SoM uses a board-to-board connector to expand 179 IO, and the level of the outgoing IO can be modified by replacing the LDO chip on the baseboard to meet the user's requirements of non-level interface; In addition, the SoM has been expanded to 16 pairs of high-speed transceiver interfaces. For users who need a lot of IO, this SoM will be a good choice. In addition, the IO connection part, the wiring between the FPGA chip and the interface is isometric and differential processing, and the SoM size is only 80*60 (mm), which is very suitable for secondary development.

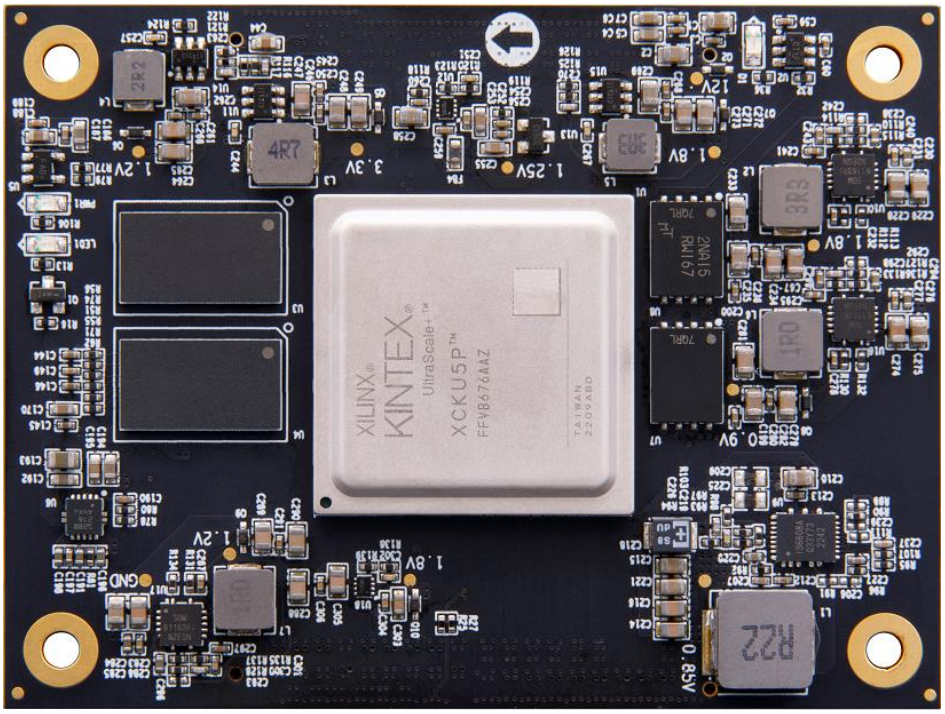


Figure 2-1-1 ACKU5 SoMFront view

Part 1.2 FPGA Chip

As mentioned above, the FPGA model we used is xcku5pffvb676, belonging to Xilinx Company's Kintex Ultrascale+ series products, speed class 6, temperature class industrial. This model is in FFVB676 package with 676 pins. The chip naming rules of Xilinx Kintex Ultrascale+ FPGA are as follows:

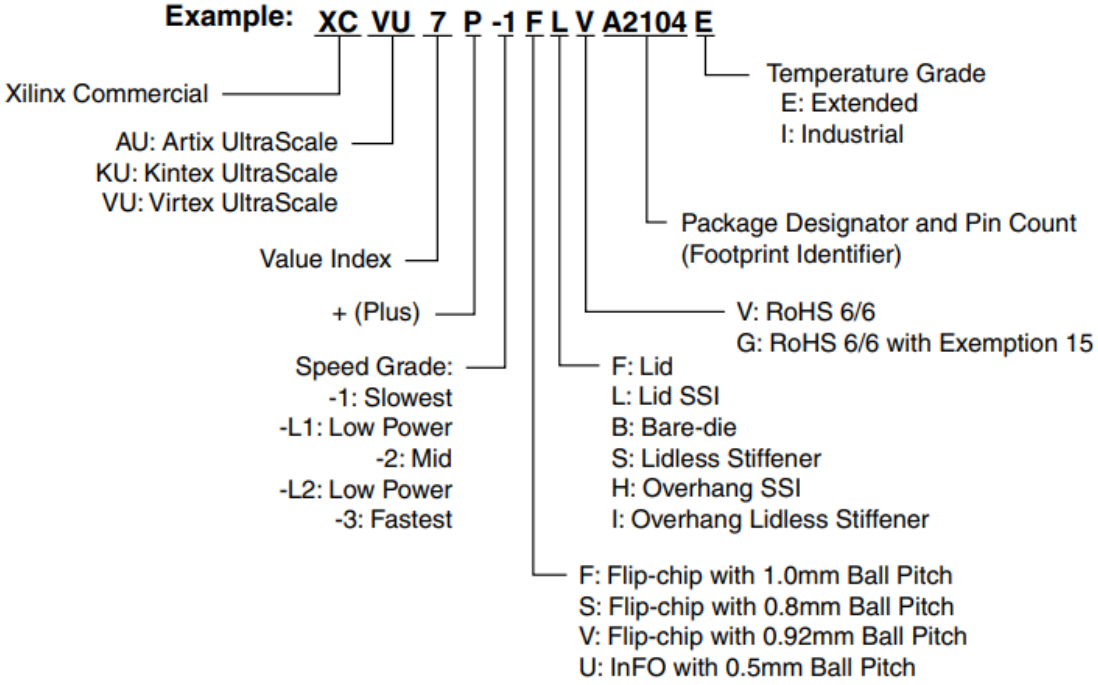


Figure 2-2-1 is the physical diagram of the FPGA chip used in the development board.

Figure 2-2-2 Actual FPGA chip

The main parameters of the FPGA chip are as follows:

Name	Specific parameter
Logic Cells	475K
Flip-Flop	433,920

LUTs	216,960
Total Block RAM	16.9Mb
DSP Slices	1824
CMTs	4
GTY/Gb/s	16/28.21
PCIe Gen3 x16	1
Speed Grade	-6
Temperature Grade	Industrial grade

Part 1.3 DDR4

The ACKU5 development board is equipped with two Micron 1GB DDR4 chips, model MT40A512M16LY-062E, connected to the HP end of the FPGA, composed of 32-bit data bus bandwidth and 2GB capacity. DDR4 SDRAM has a maximum operating data rate of 2666Mbps on the FPGA side, and the two-chip DDR4 memory system is directly connected to the memory interface of BANK 66 and R67. The DDR4 SDRAM configuration is shown in Table 2-3-1 below.

Position	Chip Model	Capacity	Factory
U3、U4	MT40A512M16LY-062E	512Mx 16bit	Micron

Table 2-3-1 DDR4 SDRAM Configuration

DDR4 hardware design needs to strictly consider signal integrity, we have fully considered the matching resistance/terminal resistance, line impedance control, line isometric control in the circuit design and PCB design, to ensure the high-speed and stable operation of DDR4.

Figure 2-3-1 shows the hardware connection of DDR4 on the FPGA:

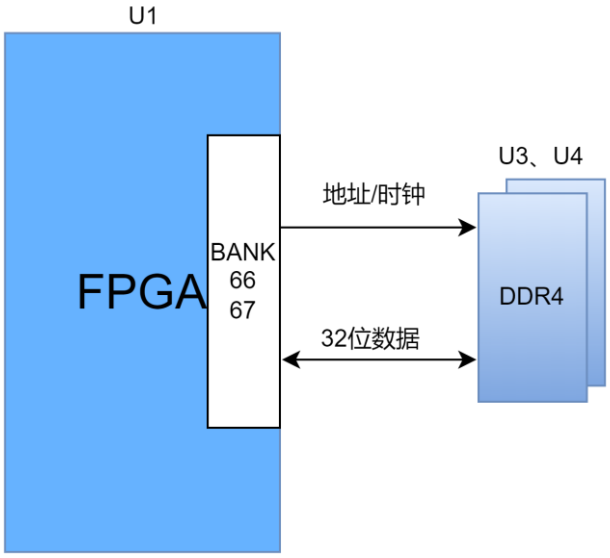
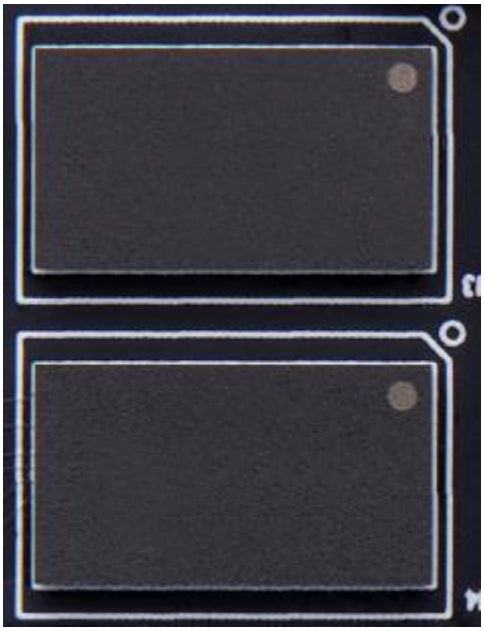


Figure 2-3-1 Schematic diagram of DDR4 DRAM

Figure 2-3-2 Photo of two DDR4 DRAM pieces of the development board



DDR4 SDRAM Pin assignment:

Signal Name	Pin No.
DDR4_D0	C16
DDR4_D1	G16
DDR4_D2	D15
DDR4_D3	G17
DDR4_D4	H17
DDR4_D5	H16
DDR4_D6	D16

DDR4_D7	E15
DDR4_D8	B19
DDR4_D9	C17
DDR4_D10	B20
DDR4_D11	B15
DDR4_D12	A19
DDR4_D13	A15
DDR4_D14	A20
DDR4_D15	B17
DDR4_D16	G20
DDR4_D17	D19
DDR4_D18	D20
DDR4_D19	F19
DDR4_D20	G21
DDR4_D21	E18
DDR4_D22	D18
DDR4_D23	F18
DDR4_D24	C23
DDR4_D25	C22
DDR4_D26	A24
DDR4_D27	B22
DDR4_D28	A25
DDR4_D29	D21
DDR4_D30	B24
DDR4_D31	E21
DDR4_DM0	G15
DDR4_DM1	C18
DDR4_DM2	H18
DDR4_DM3	A22
DDR4_DQS0_N	E17
DDR4_DQS0_P	E16
DDR4_DQS1_N	A18
DDR4_DQS1_P	A17
DDR4_DQS2_N	E20
DDR4_DQS2_P	F20

DDR4_DQS3_N	B21
DDR4_DQS3_P	C21
DDR4_A0	D26
DDR4_A1	D25
DDR4_A2	E26
DDR4_A3	C24
DDR4_A4	C26
DDR4_A5	F24
DDR4_A6	M26
DDR4_A7	B25
DDR4_A8	G26
DDR4_A9	B26
DDR4_A10	E25
DDR4_A11	H26
DDR4_A12	D23
DDR4_A13	F25
DDR4_ACT_B	J26
DDR4_BA0	M25
DDR4_BA1	F23
DDR4_BG0	K26
DDR4_CAS_B	E23
DDR4_CKE	L24
DDR4_CLK_N	G25
DDR4_CLK_P	G24
DDR4_CS_B	D24
DDR4_OTD	H24
DDR4_PAR	J25
DDR4_RAS_B	F22
DDR4_RST	L25
DDR4_WE_B	K25

Part 1.4 QSPI Flash

The SoM board is equipped with two 256MBit Quad-SPI FLASH chips, model MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the

non-volatile nature of QSPI FLASH, in use, it can store FPGA configuration Bin files and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Table 2-4-1 QSPI Flash models and parameters

Position	Chip Model	Capacity	Factory
U7、U8	MT25QU256ABA1EW9	256Mbit	Micron

The QSPI FLASH is connected to the dedicated pins of the FPGA chip, where the clock pin is connected to the CCLK0 dedicated to BANK0, and the data pin is connected to BANK0 and BANK65 respectively. Figure 2-4-1 shows the connection diagram of QSPI Flash and FPGA chip.

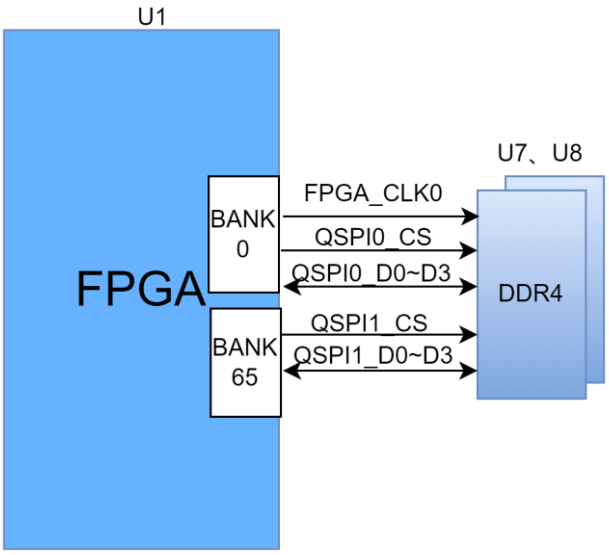


Figure 4-1 QSPI Flash Schematic

Configure chip pin assignment:

Signal Name	FPGA Pin No.
QSPI_CLK	Y11
QSPI0_CS	AA12
QSPI0_DQ0	AD11
QSPI0_DQ1	AC12
QSPI0_DQ2	AC11
QSPI0_DQ3	AE11
QSPI1_CS	U22
QSPI1_DQ0	N23
QSPI1_DQ1	P23

QSPI1_DQ2	R20
QSPI1_DQ3	R21

Part 1.5 Clock configuration

A 200Mhz 2-channel differential active clock is provided on the core board for the FPGA system. The differential clock source is provided for the FPGA logical part. The schematic diagram of the clock circuit design is shown in Figure 2-5-1 below:

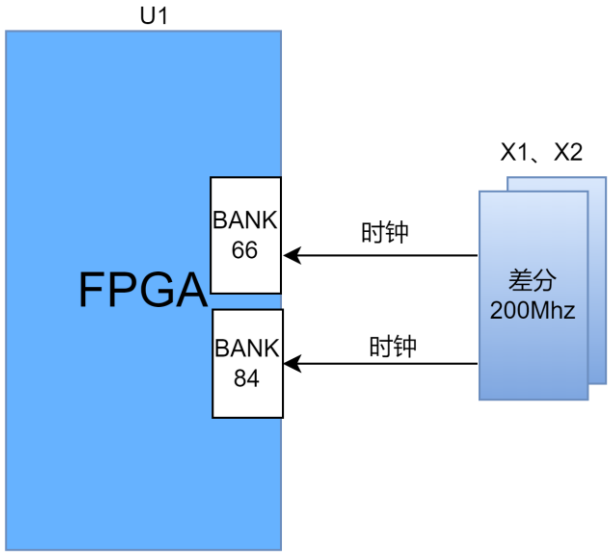


Figure 2-5-1 Clock source on the core board

FPGA system clock source

Two 200MHz differential crystal oscillators are provided on the board to provide reference clocks for the DDR4 controller and FPGA logic. The crystal output is connected to the global clock of the FPGA BANK66 and BANK84, which can be used to drive the DDR4 controller and user logic circuits within the FPGA. Figure 2-5-2 shows the schematic diagram of the clock source.

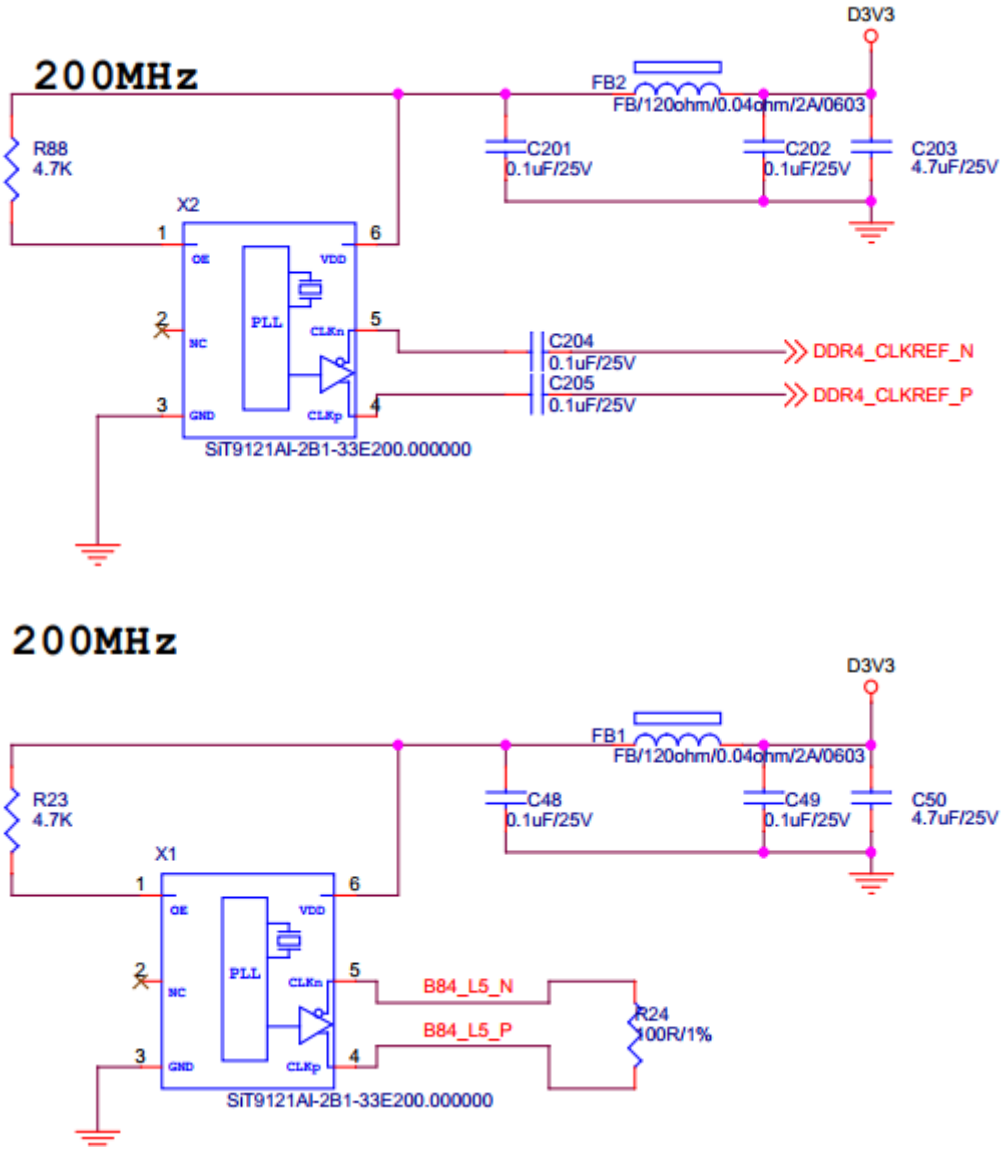


Figure 2-5-2 System clock source

Clock pin assignment:

Signal Name	FPGA Pin
B84_L5_P	AC13
B84_L5_N	AC14
DDR4_CLKREF_P	K22
DDR4_CLKREF_N	K23

Part 1.6 LED Light

The ACKU5 SoM board has three red LED lights, of which 1 is a power indicator

(PWR1), 1 is a configuration LED (D1), and a user indicator (LED1). The indicator light will light up when the core is powered on; When the FPGA is configured, the configuration LED lights up. User indicators can be used to customize function indicators. The schematic diagram of LED light hardware connection is shown in Figure 2-6-1:

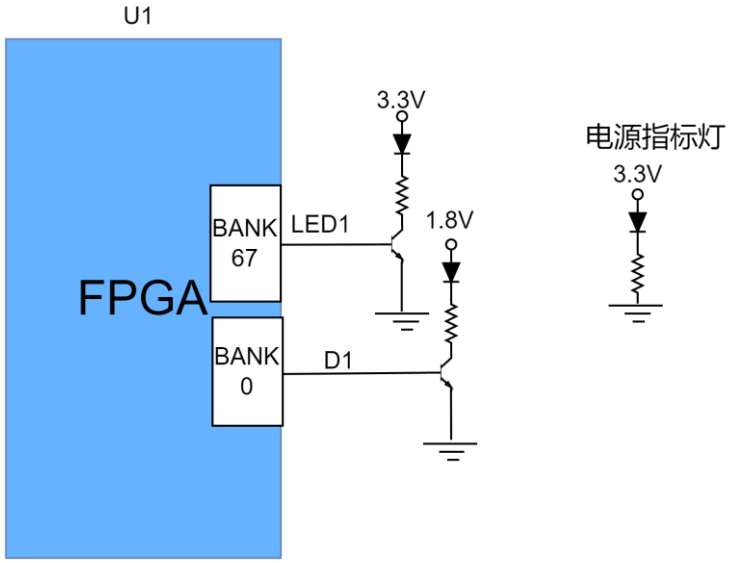


Figure 2-6-1 Schematic diagram of hardware connection of LED lights on the SoM board

Part 1.7 Power Supply

The power supply voltage of the ACKU5 SoM board is +12V, which is connected to the mainboard. The power supply design diagram on the board is shown in Figure 2-7-1 below:

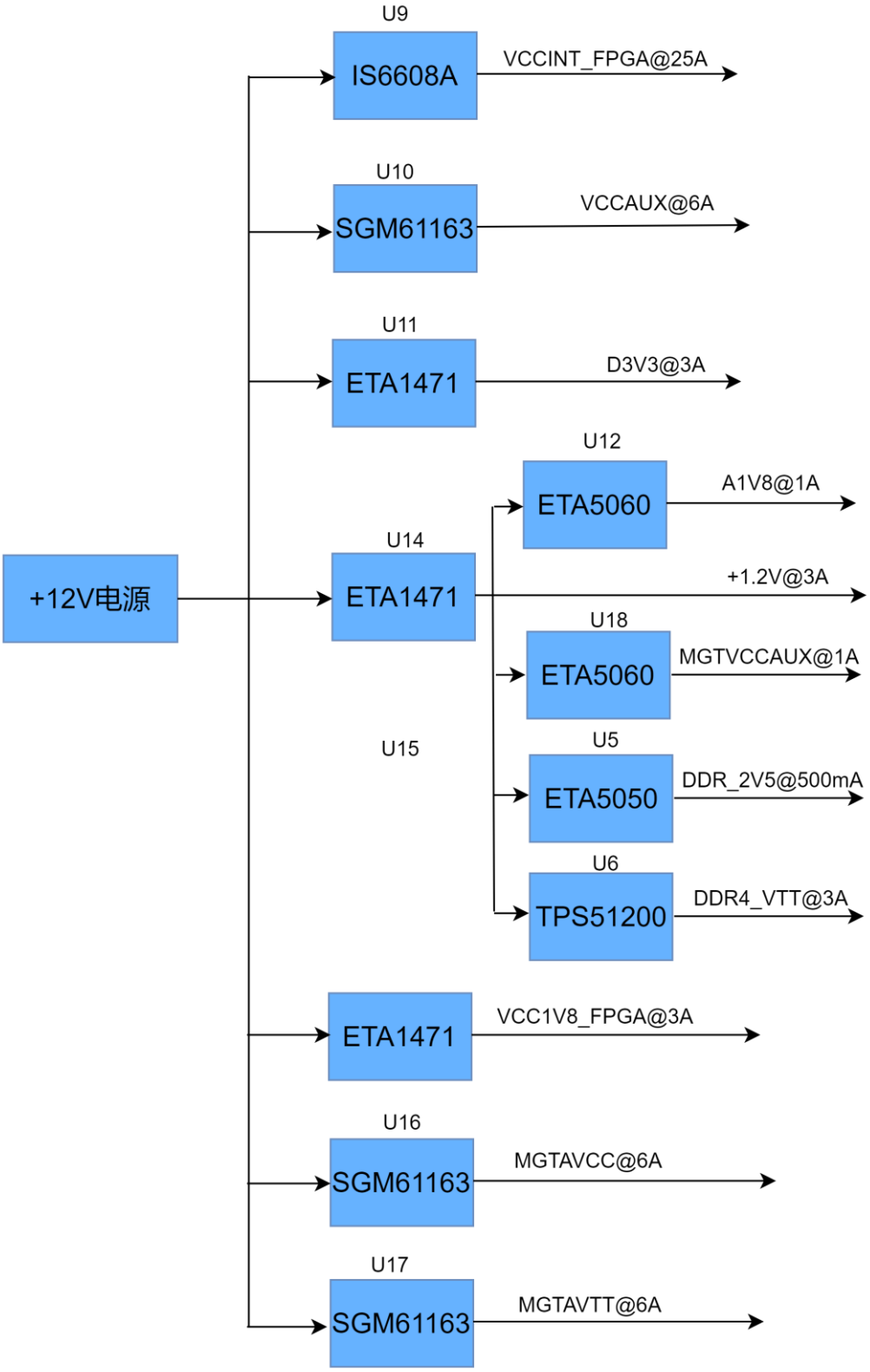


Figure 2-7-1 Schematic diagram of the power interface part

+12V generates FPGA core power supply through DCDC power chip IS6608, with output current up to 25A, which can meet the current requirements of core voltage. +12V power supply and then through 3 DCDC chips SGM61163 to generate VCCAUX,

MGTAVCC, MGTAVTT power supply to FPGA auxiliary power supply and high-speed transceiver power supply. At the same time, the +12V power supply is generated by the DCDC chip ETA1471 to generate +1.2V, VCC1V8_FPGA, D3V3 power supply to the BANK and peripherals of DDR4 and FPGA. In addition, D3V3 generates the auxiliary power supply of the high-speed transceiver and the ADC power supply of the FPGA through two LDO chips, ETA5060, +1.8V; The VTT and DDR2V5 voltages for DDR4 are generated by the TPS51200 and ETA5050.

Due to the requirements of the power-on sequence of the power supply of the FPGA, in the circuit design, we have designed in accordance with the power supply requirements of the chip to ensure the normal operation of the chip.

Part 1.8: Size Dimension

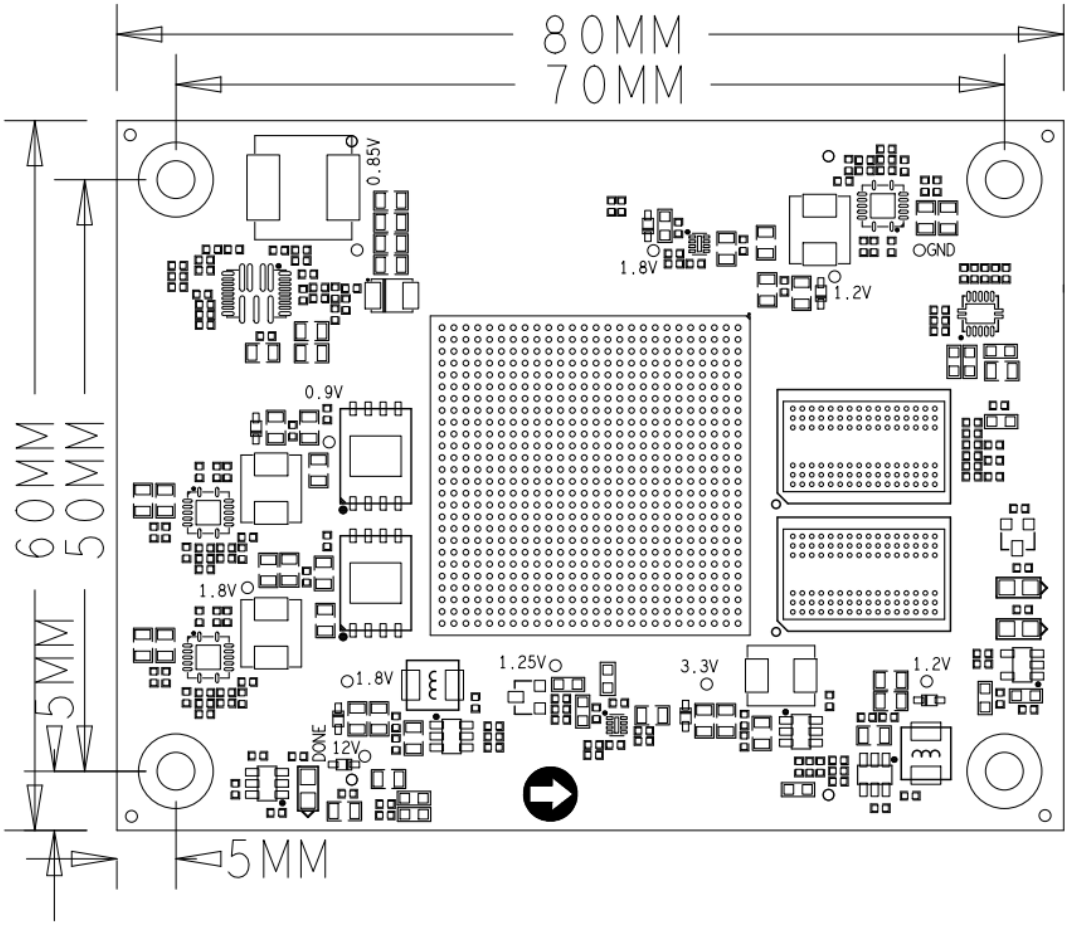


Figure 2-8-1 Top View

Part 1.9: Connector pin definition

The SoM board has two high-speed expansion ports, which are connected to the baseboard using two 240Pin inter-board connectors (J1 to J2). The power supply of the core board is input by the J2 connector.

J1 Pin assignment for connectors

J1Pin	Signal Name	FPGA Pin No.	J1Pin	Signal Name	FPGA Pin No.
A1	POWER_ALT	-	B1	POWER_SDA	-
A2	-	-	B2	POWER_SCL	-
A3	GND	-	B3	GND	-
A4	FPGA_TDI	AB12	B4	FPGA_TCK	AE12
A5	FPGA_TMS	AB10	B5	FPGA_TDO	Y10
A6	GND	-	B6	GND	-
A7	-	-	B7	-	-
A8	-	-	B8	-	-
A9	GND	-	B9	GND	-
A10	-	-	B10	-	-
A11	-	-	B11	-	-
A12	GND	-	B12	GND	-
A13	B87_L3_N	G14	B13	B87_L4_N	J14
A14	B87_L3_P	H14	B14	B87_L4_P	J15
A15	GND	-	B15	GND	-
A16	B87_L2_N	H13	B16	B87_L1_N	H12
A17	B87_L2_P	J13	B17	B87_L1_P	J12
A18	GND	-	B18	GND	-
A19	B87_L5_N	F12	B19	B87_L6_N	F13
A20	B87_L5_P	G12	B20	B87_L6_P	F14
A21	GND	-	B21	GND	-
A22	B87_L7_N	E12	B22	B87_L8_N	D13
A23	B87_L7_P	E13	B23	B87_L8_P	D14
A24	GND	-	B24	GND	-
A25	B87_L10_N	B12	B25	B87_L11_N	A12
A26	B87_L10_P	C12	B26	B87_L11_P	A13
A27	GND	-	B27	GND	-
A28	B87_L9_N	C13	B28	B87_L12_N	A14
A29	B87_L9_P	C14	B29	B87_L12_P	B14

A30	GND	-	B30	GND	-
A31	GND	-	B31	GND	-
A32	MGT226_CLK0_P	P7	B32	MGT226_CLK1_P	M7
A33	MGT226_CLK0_N	P6	B33	MGT226_CLK1_N	M6
A34	GND	-	B34	GND	-
A35	MGT226_TX0_P	N5	B35	MGT226_RX0_P	M2
A36	MGT226_TX0_N	N4	B36	MGT226_RX0_N	M1
A37	GND	-	B37	GND	-
A38	MGT226_TX1_P	L5	B38	MGT226_RX1_P	K2
A39	MGT226_TX1_N	L4	B39	MGT226_RX1_N	K1
A40	GND	-	B40	GND	-
A41	MGT226_TX2_P	J5	B41	MGT226_RX2_P	H2
A42	MGT226_TX2_N	J4	B42	MGT226_RX2_N	H1
A43	GND	-	B43	GND	-
A44	MGT226_TX3_P	G5	B44	MGT226_RX3_P	F2
A45	MGT226_TX3_N	G4	B45	MGT226_RX3_N	F1
A46	GND	-	B46	GND	-
A47	MGT227_CLK1_P	H7	B47	MGT227_CLK0_P	K7
A48	MGT227_CLK1_N	H6	B48	MGT227_CLK0_N	K6
A49	GND	-	B49	GND	-
A50	MGT227_TX0_P	F7	B50	MGT227_RX0_P	D2
A51	MGT227_TX0_N	F6	B51	MGT227_RX0_N	D1
A52	GND	-	B52	GND	-
A53	MGT227_TX1_P	E5	B53	MGT227_RX1_P	C4
A54	MGT227_TX1_N	E4	B54	MGT227_RX1_N	C3
A55	GND	-	B55	GND	-
A56	MGT227_TX2_P	D7	B56	MGT227_RX2_P	B2
A57	MGT227_TX2_N	D6	B57	MGT227_RX2_N	B1
A58	GND	-	B58	GND	-
A59	MGT227_TX3_P	B7	B59	MGT227_RX3_P	A4
A60	MGT227_TX3_N	B6	B60	MGT227_RX3_N	A3

J1Pin	Signal Name	FPGA Pin No.	J1Pin	Signal Name	FPGA Pin No.
C1	MGT224_TX0_N	AF6	D1	MGT224_RX0_N	AF1

C2	MGT224_TX0_P	AF7	D2	MGT224_RX0_P	AF2
C3	GND	-	D3	GND	-
C4	MGT224_TX1_N	AE8	D4	MGT224_RX1_N	AE3
C5	MGT224_TX1_P	AE9	D5	MGT224_RX1_P	AE4
C6	GND	-	D6	GND	-
C7	MGT224_TX2_N	AD6	D7	MGT224_RX2_N	AD1
C8	MGT224_TX2_P	AD7	D8	MGT224_RX2_P	AD2
C9	GND	-	D9	GND	-
C10	MGT224_TX3_N	AC4	D10	MGT224_RX3_N	AB1
C11	MGT224_TX3_P	AC5	D11	MGT224_RX3_P	AB2
C12	GND	-	D12	GND	-
C13	MGT224_CLK1_N	Y6	D13	MGT224_CLK0_N	AB6
C14	MGT224_CLK1_P	Y7	D14	MGT224_CLK0_P	AB7
C15	GND	-	D15	GND	-
C16	MGT225_TX0_N	AA4	D16	MGT225_RX0_N	Y1
C17	MGT225_TX0_P	AA5	D17	MGT225_RX0_P	Y2
C18	GND	-	D18	GND	-
C19	MGT225_TX1_N	W4	D19	MGT225_RX1_N	V1
C20	MGT225_TX1_P	W5	D20	MGT225_RX1_P	V2
C21	GND	-	D21	GND	-
C22	MGT225_TX2_N	U4	D22	MGT225_RX2_N	T1
C23	MGT225_TX2_P	U5	D23	MGT225_RX2_P	T2
C24	GND	-	D24	GND	-
C25	MGT225_TX3_N	R4	D25	MGT225_RX3_N	P1
C26	MGT225_TX3_P	R5	D26	MGT225_RX3_P	P2
C27	GND	-	D27	GND	-
C28	MGT225_CLK1_N	T6	D28	MGT225_CLK0_N	V6
C29	MGT225_CLK1_P	T7	D29	MGT225_CLK0_P	V7
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-
C32	-	-	D32	-	-
C33	-	-	D33	-	-
C34	GND	-	D34	GND	-
C35	-	-	D35	FPGA_VN_IN	R13
C36	-	-	D36	FPGA_VP_IN	P14
C37	GND	-	D37	GND	-
C38	GND	-	D38	GND	-
C39	B86_L2_N	J10	D39	B86_L4_N	G11

C40	B86_L2_P	J11	D40	B86_L4_P	H11
C41	GND	-	D41	GND	-
C42	B86_L3_N	H9	D42	B86_L1_N	K9
C43	B86_L3_P	J9	D43	B86_L1_P	K10
C44	GND	-	D44	GND	-
C45	B86_L9_N	C9	D45	B86_L5_N	G9
C46	B86_L9_P	D9	D46	B86_L5_P	G10
C47	GND	-	D47	GND	-
C48	B86_L6_N	F9	D48	B86_L10_N	A9
C49	B86_L6_P	F10	D49	B86_L10_P	B9
C50	GND	-	D50	GND	-
C51	B86_L7_N	E10	D51	B86_L8_N	D10
C52	B86_L7_P	E11	D52	B86_L8_P	D11
C53	GND	-	D53	GND	-
C54	B86_L11_N	A10	D54	B86_L12_N	B11
C55	B86_L11_P	B10	D55	B86_L12_P	C11
C56	GND	-	D56	GND	-
C57	-	-	D57	-	-
C58	-	-	D58	-	-
C59	-	-	D59	-	-
C60	-	-	D60	-	-

J2 Pin assignment for connectors

J2 Pin	Signal Name	FPGA Pin No.	J2 Pin	Signal Name	FPGA Pin No.
A1	+12V	-	B1	+12V	-
A2	-	-	B2	-	-
A3	GND	-	B3	GND	-
A4	VCCIO_65	P22,U23,Y24	B4	VCCIO_64	AA21,AB18,AD22
A5	-	-	B5	-	-
A6	GND	-	B6	GND	-
A7	GND	-	B7	GND	-
A8	-	-	B8	-	-
A9	-	-	B9	-	-
A10	GND	-	B10	GND	-
A11	B84_L2_N	AF13	B11	B84_L1_N	AF15
A12	B84_L2_P	AE13	B12	B84_L1_P	AF14
A13	GND	-	B13	GND	-

A14	B84_L9_N	Y16	B14	B84_L6_N	AB16
A15	B84_L9_P	W16	B15	B84_L6_P	AB15
A16	GND	-	B16	GND	-
A17	B64_L7_N	AF22	B17	B64_L8_N	AE23
A18	B64_L7_P	AE22	B18	B64_L8_P	AD23
A19	GND	-	B19	GND	-
A20	B64_L3_N	AF25	B20	B64_T2U	AE18
A21	B64_L3_P	AF24	B21	B64_T1U	AF20
A22	GND	-	B22	GND	-
A23	B64_L1_N	AE26	B23	B64_L11_N	AE21
A24	B64_L1_P	AE25	B24	B64_L11_P	AD21
A25	GND	-	B25	GND	-
A26	B64_L4_N	AD26	B26	B64_L5_N	AD25
A27	B64_L4_P	AC26	B27	B64_L5_P	AD24
A28	GND	-	B28	GND	-
A29	B64_L6_N	AC24	B29	B64_L9_N	AC23
A30	B64_L6_P	AB24	B30	B64_L9_P	AC22
A31	GND	-	B31	GND	-
A32	B64_L2_N	AB26	B32	B64_L10_N	AB22
A33	B64_L2_P	AB25	B33	B64_L10_P	AA22
A34	GND	-	B34	GND	-
A35	B64_T3U	AC16	B35	B64_L20_N	AB19
A36	B65_T1U	AA23	B36	B64_L20_P	AA19
A37	GND	-	B37	GND	-
A38	B65_L6_N	W20	B38	B65_L9_N	AA25
A39	B65_L6_P	W19	B39	B65_L9_P	AA24
A40	GND	-	B40	GND	-
A41	B65_L1_N	V19	B41	B65_L8_N	Y26
A42	B65_L1_P	U19	B42	B65_L8_P	Y25
A43	GND	-	B43	GND	-
A44	B65_L3_N	U20	B44	B65_L5_N	T23
A45	B65_L3_P	T20	B45	B65_L5_P	T22
A46	GND	-	B46	GND	-
A47	B66_L4_N	L19	B47	B65_L19_N	R23
A48	B66_L4_P	M19	B48	B65_L19_P	R22
A49	GND	-	B49	GND	-

A50	B66_L2_N	M21	B50	B65_L16_N	V26
A51	B66_L2_P	M20	B51	B65_L16_P	U26
A52	GND	-	B52	GND	-
A53	B66_L5_N	J21	B53	B65_T3U	T19
A54	B66_L5_P	K21	B54	-	-
A55	GND	-	B55	GND	-
A56	B66_L3_N	J20	B56	B65_L17_N	P26
A57	B66_L3_P	J19	B57	B65_L17_P	P25
A58	GND	-	B58	GND	-
A59	B66_L1_N	K18	B59	B65_L15_N	P24
A60	B66_L1_P	L18	B60	B65_L15_P	N24

J2 Pin	Signal Name	FPGA Pin No.	J2 Pin	Signal Name	FPGA Pin No.
C1	+12V	-	D1	+12V	-
C2	-	-	D2	-	-
C3	GND	-	D3	GND	-
C4	VCCAUX_PG	-	D4	FMC_HPC0_VREF_A_M2C	W18，V18
C5	-	-	D5	-	-
C6	GND	-	D6	GND	-
C7	GND	-	D7	GND	-
C8	B84_L11_N	AA13	D8	B84_L12_N	W13
C9	B84_L11_P	Y13	D9	B84_L12_P	W12
C10	GND	-	D10	GND	-
C11	B84_L3_N	AE15	D11	B84_L10_N	W15
C12	B84_L3_P	AD15	D12	B84_L10_P	W14
C13	GND	-	D13	GND	-
C14	B84_L4_N	AD14	D14	B84_L8_N	AB14
C15	B84_L4_P	AD13	D15	B84_L8_P	AA14
C16	GND	-	D16	GND	-
C17	B64_L17_N	AF17	D17	B84_L7_N	AA15
C18	B64_L17_P	AE17	D18	B84_L7_P	Y15
C19	GND	-	D19	GND	-
C20	B64_L15_N	AF19	D20	B64_L13_N	AE20
C21	B64_L15_P	AF18	D21	B64_L13_P	AD20
C22	GND	-	D22	GND	-

C23	B64_L16_N	AD18	D23	B64_L18_N	AE16
C24	B64_L16_P	AC18	D24	B64_L18_P	AD16
C25	GND	-	D25	GND	-
C26	B64_L14_N	AD19	D26	B64_L22_N	AC17
C27	B64_L14_P	AC19	D27	B64_L22_P	AB17
C28	GND	-	D28	GND	-
C29	B64_L12_N	AC21	D29	B64_L21_N	AB20
C30	B64_L12_P	AB21	D30	B64_L21_P	AA20
C31	GND	-	D31	GND	-
C32	B64_L24_N	AA18	D32	B64_L23_N	AA17
C33	B64_L24_P	Y18	D33	B64_L23_P	Y17
C34	GND	-	D34	GND	-
C35	-	-	D35	B64_L19_N	Y21
C36	-	-	D36	B64_L19_P	Y20
C37	GND	-	D37	GND	-
C38	-	-	D38	USER_DEF_CLOCK_P	J23
C39	-	-	D39	USER_DEF_CLOCK_N	J24
C40	GND	-	D40	GND	-
C41	B65_L10_N	W26	D41	B65_L12_N	W24
C42	B65_L10_P	W25	D42	B65_L12_P	V24
C43	GND	-	D43	GND	-
C44	B65_L11_N	W23	D44	B65_L7_N	Y23
C45	B65_L11_P	V23	D45	B65_L7_P	Y22
C46	GND	-	D46	GND	-
C47	B65_L4_N	V22	D47	B65_L23_N	P19
C48	B65_L4_P	V21	D48	B65_L23_P	N19
C49	GND	-	D49	GND	-
C50	B65_L20_N	P21	D50	B65_L24_N	N22
C51	B65_L20_P	P20	D51	B65_L24_P	N21
C52	GND	-	D52	GND	-
C53	B65_L14_N	U25	D53	B65_L13_N	U24
C54	B65_L14_P	T25	D54	B65_L13_P	T24
C55	GND	-	D55	GND	-
C56	B65_T2U	N26	D56	B65_L18_N	R26
C57	B65_L2_P	U21	D57	B65_L18_P	R25
C58	GND	-	D58	GND	-

C59	-	-	D59	-	-
C60	VCCO_84	AC15,Y24	D60	VCCO_86_87	E9,H10,E14,H25