Zynq UltraScale+ MPSoC Core Board ACU19EG User Manual

ALINX

Version Record

Version	Date	Released By	Description
REV1.0		Rachel Zhou	First Release

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1.1 ACU19EG Core Board Introduction

ZYNQ chip on ACU19EG (core board model, the same below) FPGA core board is based on XCZU19EG-2FFVC1760I, a chip belongs to XILINX company's Zynq UltraScale+MPSoCs EV series.

This core board uses 9 pieces of Micron's DDR4 chips MT40A512M16GE, of which 5 DDR4 chips are mounted on the PS side, formed a 72-bit data bus bandwidth (ECC is supported), while 4 DDR4 chips are mounted on the PL side, formed a 64-bit data bus width. Each DDR4 chip has a capacity of 2GB, and the highest operating speed of DDR4 SDRAM can reach 1200MHz (data rate 2400Mbps). In addition, 2 pieces of 512MBit QSPI FLASH and an 32GB eMMC FLASH chip are also integrated on the core board to start storage configuration and system files.

To connect to the carrier board, eight 120Pin board-to-board connectors of this core board extend USB2.0 interface, Gigabit Ethernet interface, SD card interface and other remaining MIO ports on the PS side; Meanwhile, they also extend 4 pairs of PS MGT high-speed transceiver interface; As well as the 48-way GHT/GTY transceiver and almost all IO ports on the PL side (HP I/O: 240, HD I/O: 96). The wiring between the XCZU19EG chip and the interface has been processed with equal length and differences, and the core board size is only 80*80 (mm), which is very suitable for secondary development.

1.2 ZYNQ Chip

The FPGA core board ACU19EG uses XCZU19EG-2FFVC1760I, the chip of Xilinx's Zynq UltraScale+ MPSoCs EG series. The PS system of the ZU19EG chip integrates 4 ARM Cortex™-A53 processors with a speed of up to 1.3Ghz and supports Level 2 Cache; it also contains 2 Cortex-R5 processors with a speed of up to 533Mhz.

The ZU19EG chip supports 32-bit or 64-bit DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 memory chips, and has rich high-speed interfaces on the PS side, such as PCIE Gen2, USB3.0, SATA 3.1, and DisplayPort. At the same time, it also supports USB2.0, Gigabit Ethernet, SD/SDIO, I2C, CAN, UART, GPIO and other interfaces. The PL side contains a wealth of programmable logic units, DSP and internal RAM.

Figure 1-2-1 detailed the Overall Block Diagram of ZU19EG.

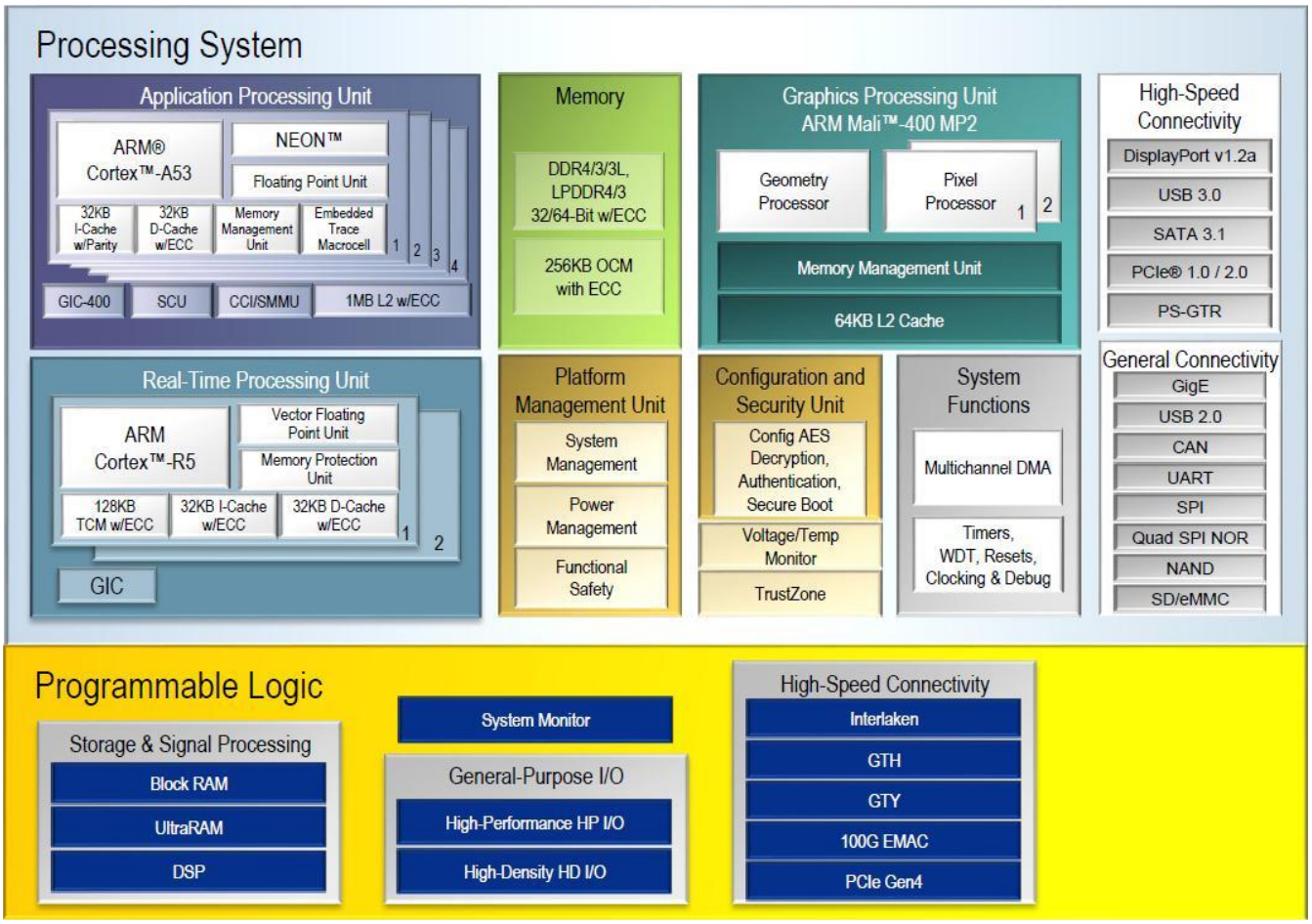


Figure 1-2-1: Overall Block Diagram of the ZYNQ ZU19EG Chip

The main parameters of PS system are as follows:

- ARM quad-core Cortex™-A53 processor with a speed of up to 1.3GHz, each CPU 32KB level 1 instruction and data cache, 1MB level 2 cache, shared by 2 CPUs.
- ARM dual-core Cortex-R5 processor with a speed of up to 533MHz, each CPU 32KB level 1 instruction and data cache, and 128K tightly coupled memory.
- External storage interface, support 32/64bit DDR4/3/3L, LPDDR4/3 interface.
- Static storage interface, support NAND, 2xQuad-SPI FLASH.

- High-speed connection interface, support PCIe Gen2 x 4, 2 x USB3.0, Sata 3.1, Display Port, 4 x Tri-mode, Gigabit Ethernet.
- Common connection interfaces: 2 x USB2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO.
- Power management: Support the four-part division of power supply: Full/Low/PL/Battery.
- Encryption algorithm: support RSA, AES and SHA.
- System monitoring: 10-bit 1Mbps AD sampling for temperature and voltage detection.

The main parameters of the PL logic are as follows:

- System Logic Cells: 1143K
- CLB Flip-flops: 1045K
- CLB LUTs: 523K
- Block RAM: 34.6Mb
- Clock Management Units (CMTs): 11
- DSP Slices: 1968
- GTH 16.3Gb/s Transceiver: 44

XCZU19EG-2FFVC1760I chip' s speed grade is -2, industrial grade, package is FFVC1760.

1.3 DDR4 DRAM

The ACU19EG core board is equipped with 9 Micron 2GB DDR4 chips, model MT40A1G16KD-062E, among which 5 pieces are mounted on the PS side to form a 72-bit data bus bandwidth (ECC is supported), and each chip has a DDR capacity of 2GB. And another 4 pieces are mounted on the PL side to form a 64-bit data bus bandwidth, and each piece has a DDR capacity of 2GB. The maximum speed of DDR4 SDRAM at PS side can reach 1200MHz (data rate is 2400Mbps) and four DDR4 memory systems are directly connected to the BANK504 memory interface of the PS side. DDR4 SDRAM on the PL side can run up to 1200MHz (data rate 2400Mbps), and four DDR4 chips are connected to the BANK69,70,71 interface of the FPGA. The specific configurations of DDR4 SDRAM on the PS and PL side are shown in Table 1-3-1 below.

Position	Bit Number	Chip Model	Capacity	Factory
PS	U4,U5,U6,U7,U162	MT40A1G16KD-062E	1G x 16bit	Micron
PL	U18,U19,U20,U21	MT40A1G16KD-062E	1G x 16bit	Micron

Table 1-3-1: DDR4 SDRAM Configuration

The design of DDR4 hardware requires strict consideration of signal integrity. We have fully considered the matching resistance/terminal resistance, trace impedance control, and trace length control in circuit design and PCB design to ensure high-speed and stable operation of DDR4.

The hardware connection of DDR4 SDRAM on the PS side is shown in Figure 1-3-1:

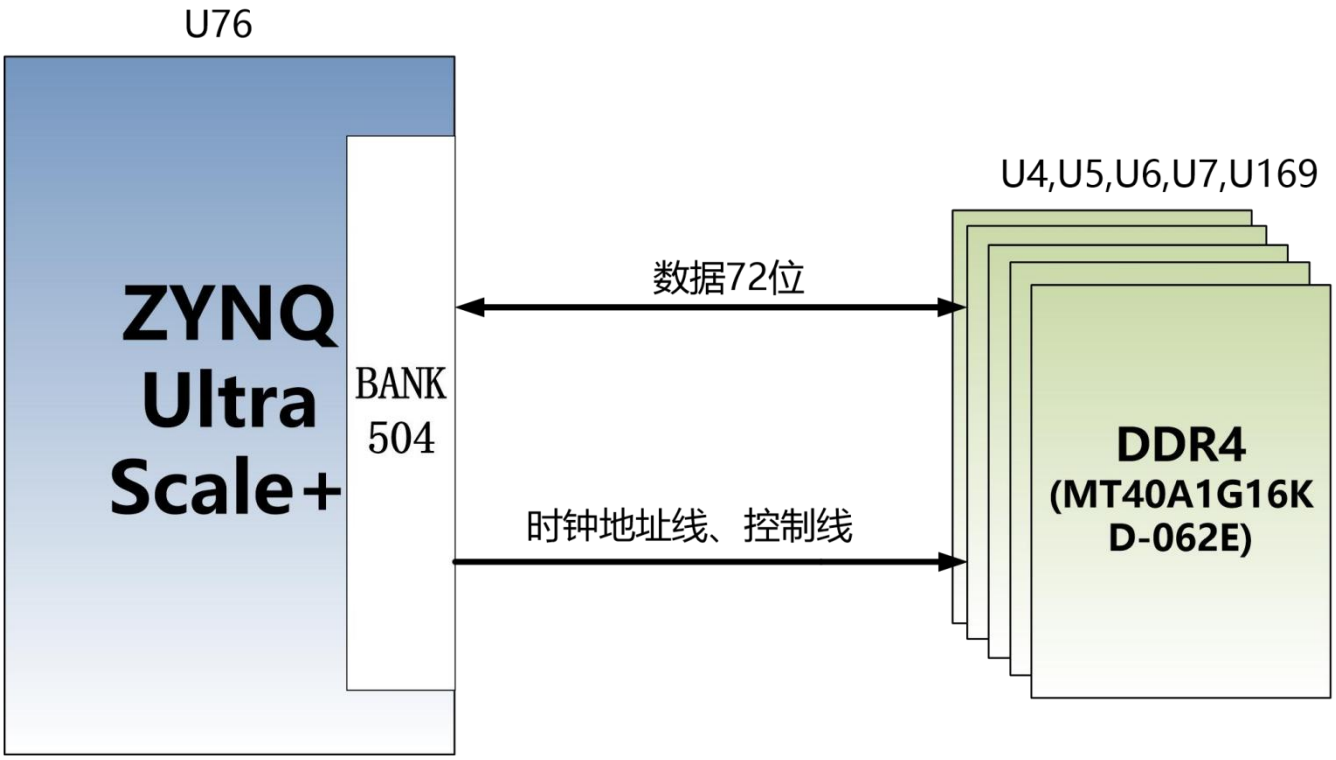


Figure 1-3-1: DDR4 DRAM schematic diagram

The hardware connection of DDR4 SDRAM on the Pl side is shown in Figure 1-3-2:

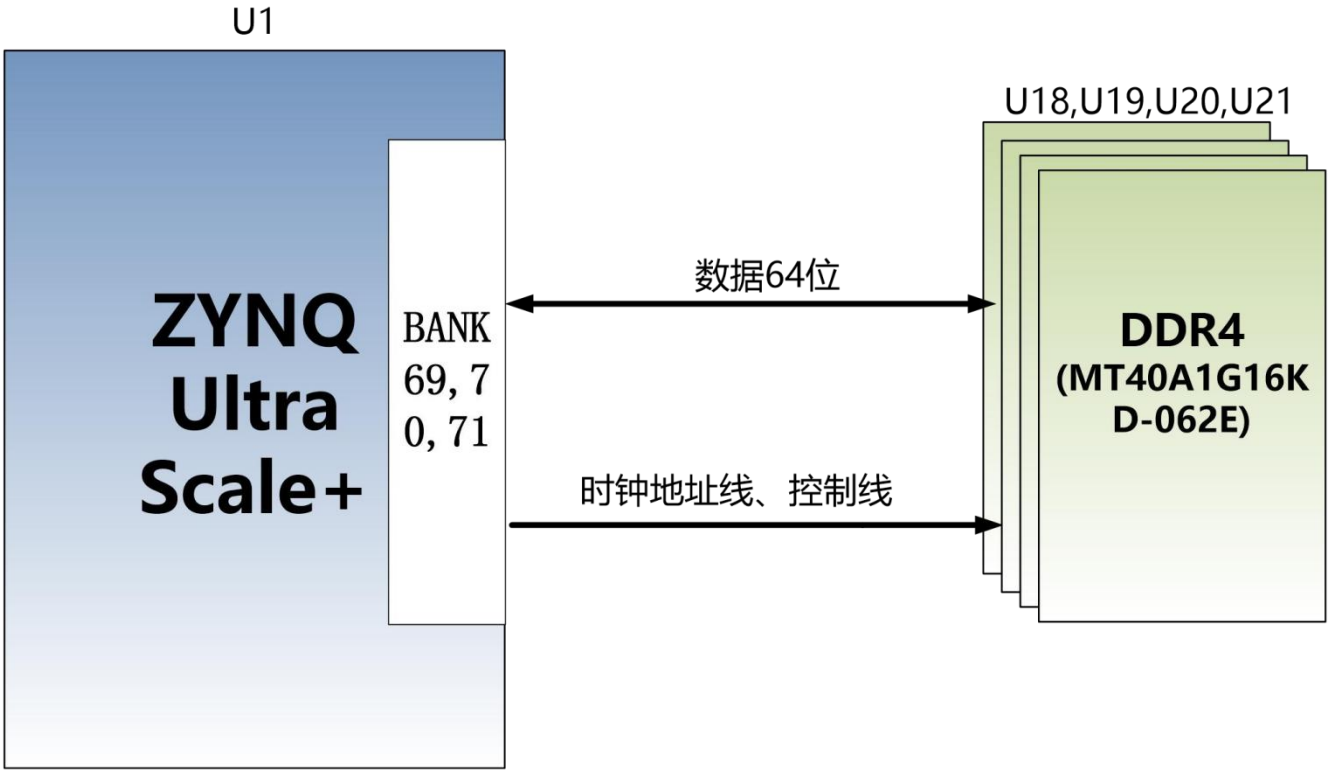


Figure 1-3-2: DDR4 DRAM schematic diagram

DDR4 DRAM pin assignment on the PS side:

Signal Name	Pin Name	Pin Number
PS_DDR4_DQS0_N	PS_DDR_DQS_N0_504	BA30
PS_DDR4_DQS0_P	PS_DDR_DQS_P0_504	AY30
PS_DDR4_DQS1_N	PS_DDR_DQS_N1_504	AY33
PS_DDR4_DQS1_P	PS_DDR_DQS_P1_504	AY32
PS_DDR4_DQS2_N	PS_DDR_DQS_N2_504	AT30
PS_DDR4_DQS2_P	PS_DDR_DQS_P2_504	AR30
PS_DDR4_DQS3_N	PS_DDR_DQS_N3_504	AT32
PS_DDR4_DQS3_P	PS_DDR_DQS_P3_504	AR32
PS_DDR4_DQS4_N	PS_DDR_DQS_N4_504	AR40
PS_DDR4_DQS4_P	PS_DDR_DQS_P4_504	AP40
PS_DDR4_DQS5_N	PS_DDR_DQS_N5_504	AK37
PS_DDR4_DQS5_P	PS_DDR_DQS_P5_504	AJ37
PS_DDR4_DQS6_N	PS_DDR_DQS_N6_504	AU41
PS_DDR4_DQS6_P	PS_DDR_DQS_P6_504	AU40
PS_DDR4_DQS7_N	PS_DDR_DQS_N7_504	AL41
PS_DDR4_DQS7_P	PS_DDR_DQS_P7_504	AL40
PS_DDR4_DQS8_N	PS_DDR_DQS_N8_504	AY40
PS_DDR4_DQS8_P	PS_DDR_DQS_P8_504	AY39
PS_DDR4_DQ0	PS_DDR_DQ0_504	AV29

PS_DDR4_DQ1	PS_DDR_DQ1_504	AW30
PS_DDR4_DQ2	PS_DDR_DQ2_504	AW29
PS_DDR4_DQ3	PS_DDR_DQ3_504	AW31
PS_DDR4_DQ4	PS_DDR_DQ4_504	BB31
PS_DDR4_DQ5	PS_DDR_DQ5_504	BB30
PS_DDR4_DQ6	PS_DDR_DQ6_504	BB29
PS_DDR4_DQ7	PS_DDR_DQ7_504	BA31
PS_DDR4_DQ8	PS_DDR_DQ8_504	BB33
PS_DDR4_DQ9	PS_DDR_DQ9_504	BA32
PS_DDR4_DQ10	PS_DDR_DQ10_504	BA33
PS_DDR4_DQ11	PS_DDR_DQ11_504	BB34
PS_DDR4_DQ12	PS_DDR_DQ12_504	AV31
PS_DDR4_DQ13	PS_DDR_DQ13_504	AW32
PS_DDR4_DQ14	PS_DDR_DQ14_504	AV32
PS_DDR4_DQ15	PS_DDR_DQ15_504	AV33
PS_DDR4_DQ16	PS_DDR_DQ16_504	AN29
PS_DDR4_DQ17	PS_DDR_DQ17_504	AP29
PS_DDR4_DQ18	PS_DDR_DQ18_504	AP30
PS_DDR4_DQ19	PS_DDR_DQ19_504	AP31
PS_DDR4_DQ20	PS_DDR_DQ20_504	AT31
PS_DDR4_DQ21	PS_DDR_DQ21_504	AU30

PS_DDR4_DQ22	PS_DDR_DQ22_504	AU31
PS_DDR4_DQ23	PS_DDR_DQ23_504	AU29
PS_DDR4_DQ24	PS_DDR_DQ24_504	AV34
PS_DDR4_DQ25	PS_DDR_DQ25_504	AU33
PS_DDR4_DQ26	PS_DDR_DQ26_504	AT33
PS_DDR4_DQ27	PS_DDR_DQ27_504	AU34
PS_DDR4_DQ28	PS_DDR_DQ28_504	AN33
PS_DDR4_DQ29	PS_DDR_DQ29_504	AP32
PS_DDR4_DQ30	PS_DDR_DQ30_504	AN32
PS_DDR4_DQ31	PS_DDR_DQ31_504	AN31
PS_DDR4_DQ32	PS_DDR_DQ32_504	AN41
PS_DDR4_DQ33	PS_DDR_DQ33_504	AN42
PS_DDR4_DQ34	PS_DDR_DQ34_504	AP42
PS_DDR4_DQ35	PS_DDR_DQ35_504	AP41
PS_DDR4_DQ36	PS_DDR_DQ36_504	AN39
PS_DDR4_DQ37	PS_DDR_DQ37_504	AR38
PS_DDR4_DQ38	PS_DDR_DQ38_504	AP39
PS_DDR4_DQ39	PS_DDR_DQ39_504	AN38
PS_DDR4_DQ40	PS_DDR_DQ40_504	AL37
PS_DDR4_DQ41	PS_DDR_DQ41_504	AL38
PS_DDR4_DQ42	PS_DDR_DQ42_504	AK38

PS_DDR4_DQ43	PS_DDR_DQ43_504	AK39
PS_DDR4_DQ44	PS_DDR_DQ44_504	AJ36
PS_DDR4_DQ45	PS_DDR_DQ45_504	AL35
PS_DDR4_DQ46	PS_DDR_DQ46_504	AJ35
PS_DDR4_DQ47	PS_DDR_DQ47_504	AK35
PS_DDR4_DQ48	PS_DDR_DQ48_504	AR42
PS_DDR4_DQ49	PS_DDR_DQ49_504	AT41
PS_DDR4_DQ50	PS_DDR_DQ50_504	AT42
PS_DDR4_DQ51	PS_DDR_DQ51_504	AT40
PS_DDR4_DQ52	PS_DDR_DQ52_504	AV42
PS_DDR4_DQ53	PS_DDR_DQ53_504	AV41
PS_DDR4_DQ54	PS_DDR_DQ54_504	AV39
PS_DDR4_DQ55	PS_DDR_DQ55_504	AV38
PS_DDR4_DQ56	PS_DDR_DQ56_504	AM39
PS_DDR4_DQ57	PS_DDR_DQ57_504	AM38
PS_DDR4_DQ58	PS_DDR_DQ58_504	AM40
PS_DDR4_DQ59	PS_DDR_DQ59_504	AM41
PS_DDR4_DQ60	PS_DDR_DQ60_504	AJ42
PS_DDR4_DQ61	PS_DDR_DQ61_504	AK42
PS_DDR4_DQ62	PS_DDR_DQ62_504	AK40
PS_DDR4_DQ63	PS_DDR_DQ63_504	AK41

PS_DDR4_DQ64	PS_DDR4_DQ64_504	BB40
PS_DDR4_DQ65	PS_DDR4_DQ65_504	BA41
PS_DDR4_DQ66	PS_DDR4_DQ66_504	BA42
PS_DDR4_DQ67	PS_DDR4_DQ67_504	BA40
PS_DDR4_DQ68	PS_DDR4_DQ68_504	AW42
PS_DDR4_DQ69	PS_DDR4_DQ69_504	AW40
PS_DDR4_DQ70	PS_DDR4_DQ70_504	AW41
PS_DDR4_DQ71	PS_DDR4_DQ71_504	AW39
PS_DDR4_DM0	PS_DDR_DM0_504	AY29
PS_DDR4_DM1	PS_DDR_DM1_504	AY34
PS_DDR4_DM2	PS_DDR_DM2_504	AR29
PS_DDR4_DM3	PS_DDR_DM3_504	AR33
PS_DDR4_DM4	PS_DDR_DM4_504	AR39
PS_DDR4_DM5	PS_DDR_DM5_504	AL36
PS_DDR4_DM6	PS_DDR_DM6_504	AU39
PS_DDR4_DM7	PS_DDR_DM7_504	AL42
PS_DDR4_DM8	PS_DDR_DM8_504	AY42
PS_DDR4_A0	PS_DDR_A0_504	BA38
PS_DDR4_A1	PS_DDR_A1_504	BB36
PS_DDR4_A2	PS_DDR_A2_504	BA35
PS_DDR4_A3	PS_DDR_A3_504	BB35

PS_DDR4_A4	PS_DDR_A4_504	BB38
PS_DDR4_A5	PS_DDR_A5_504	AY35
PS_DDR4_A6	PS_DDR_A6_504	AP37
PS_DDR4_A7	PS_DDR_A7_504	AT36
PS_DDR4_A8	PS_DDR_A8_504	AR35
PS_DDR4_A9	PS_DDR_A9_504	AT35
PS_DDR4_A10	PS_DDR_A10_504	AU35
PS_DDR4_A11	PS_DDR_A11_504	AU36
PS_DDR4_A12	PS_DDR_A12_504	AW36
PS_DDR4_A13	PS_DDR_A13_504	AW37
PS_DDR4_ACT_B	PS_DDR_ACT_N_504	AR37
PS_DDR4_ALERT_B	PS_DDR_ALERT_N_504	AM36
PS_DDR4_BA0	PS_DDR_BA0_504	AN37
PS_DDR4_BA1	PS_DDR_BA1_504	AN36
PS_DDR4_BG0	PS_DDR_BG0_504	AP36
PS_DDR4_CAS_B	PS_DDR_A15_504	AW34
PS_DDR4_CKE0	PS_DDR_CKE0_504	AY38
PS_DDR4_CLK0_N	PS_DDR_CK_N0_504	BA37
PS_DDR4_CLK0_P	PS_DDR_CK0_504	BA36
PS_DDR4_CS0_B	PS_DDR_CS_N0_504	AY37
PS_DDR4_ODT0	PS_DDR_ODT0_504	BB39

PS_DDR4_PARITY	PS_DDR_PARITY_504	AM35
PS_DDR4_RAS_B	PS_DDR_A16_504	AR34
PS_DDR4_RESET_B	PS_DDR_RAM_RST_N_504	AM34
PS_DDR4_WE_B	PS_DDR_A14_504	AW35

DDR4 DRAM pin assignment on the PL side:

Signal Name	Pin Name	Pin Number
PL_DDR4_DQS0_N	IO_L10N_T1U_N7_QBC_AD4N_70	G23
PL_DDR4_DQS0_P	IO_L10P_T1U_N6_QBC_AD4P_70	H23
PL_DDR4_DQS1_N	IO_L4N_T0U_N7_DBC_AD7N_70	K24
PL_DDR4_DQS1_P	IO_L4P_T0U_N6_DBC_AD7P_70	L24
PL_DDR4_DQS2_N	IO_L22N_T3U_N7_DBC_AD0N_70	B26
PL_DDR4_DQS2_P	IO_L22P_T3U_N6_DBC_AD0P_70	B25
PL_DDR4_DQS3_N	IO_L16N_T2U_N7_QBC_AD3N_70	E27
PL_DDR4_DQS3_P	IO_L16P_T2U_N6_QBC_AD3P_70	E26
PL_DDR4_DQS4_N	IO_L10N_T1U_N7_QBC_AD4N_69	A32
PL_DDR4_DQS4_P	IO_L10P_T1U_N6_QBC_AD4P_69	B31
PL_DDR4_DQS5_N	IO_L4N_T0U_N7_DBC_AD7N_69	F30
PL_DDR4_DQS5_P	IO_L4P_T0U_N6_DBC_AD7P_69	G30
PL_DDR4_DQS6_N	IO_L22N_T3U_N7_DBC_AD0N_69	A40
PL_DDR4_DQS6_P	IO_L22P_T3U_N6_DBC_AD0P_69	A39

PL_DDR4_DQS7_N	IO_L16N_T2U_N7_QBC_AD3N_69	C34
PL_DDR4_DQS7_P	IO_L16P_T2U_N6_QBC_AD3P_69	D34
PL_DDR4_DQ0	IO_L12N_T1U_N11_GC_70	G25
PL_DDR4_DQ1	IO_L9N_T1L_N5_AD12N_70	J24
PL_DDR4_DQ2	IO_L11P_T1U_N8_GC_70	H25
PL_DDR4_DQ3	IO_L8N_T1L_N3_AD5N_70	J26
PL_DDR4_DQ4	IO_L12P_T1U_N10_GC_70	H24
PL_DDR4_DQ5	IO_L8P_T1L_N2_AD5P_70	K26
PL_DDR4_DQ6	IO_L11N_T1U_N9_GC_70	H26
PL_DDR4_DQ7	IO_L9P_T1L_N4_AD12P_70	J23
PL_DDR4_DQ8	IO_L2P_T0L_N2_70	M25
PL_DDR4_DQ9	IO_L6P_T0U_N10_AD6P_70	M23
PL_DDR4_DQ10	IO_L2N_T0L_N3_70	L25
PL_DDR4_DQ11	IO_L6N_T0U_N11_AD6N_70	L23
PL_DDR4_DQ12	IO_L3P_T0L_N4_AD15P_70	N24
PL_DDR4_DQ13	IO_L5N_T0U_N9_AD14N_70	N23
PL_DDR4_DQ14	IO_L3N_T0L_N5_AD15N_70	N25
PL_DDR4_DQ15	IO_L5P_T0U_N8_AD14P_70	P23
PL_DDR4_DQ16	IO_L20N_T3L_N3_AD1N_70	A28
PL_DDR4_DQ17	IO_L24P_T3U_N10_70	A24
PL_DDR4_DQ18	IO_L21N_T3L_N5_AD8N_70	B27

PL_DDR4_DQ19	IO_L23N_T3U_N9_70	C25
PL_DDR4_DQ20	IO_L20P_T3L_N2_AD1P_70	A27
PL_DDR4_DQ21	IO_L21P_T3L_N4_AD8P_70	C26
PL_DDR4_DQ22	IO_L24N_T3U_N11_70	A25
PL_DDR4_DQ23	IO_L23P_T3U_N8_70	C24
PL_DDR4_DQ24	IO_L15P_T2L_N4_AD11P_70	F27
PL_DDR4_DQ25	IO_L14P_T2L_N2_GC_70	F25
PL_DDR4_DQ26	IO_L17P_T2U_N8_AD10P_70	D27
PL_DDR4_DQ27	IO_L14N_T2L_N3_GC_70	E25
PL_DDR4_DQ28	IO_L15N_T2L_N5_AD11N_70	F28
PL_DDR4_DQ29	IO_L18P_T2U_N10_AD2P_70	F24
PL_DDR4_DQ30	IO_L17N_T2U_N9_AD10N_70	D28
PL_DDR4_DQ31	IO_L18N_T2U_N11_AD2N_70	E24
PL_DDR4_DQ32	IO_L11N_T1U_N9_GC_69	D31
PL_DDR4_DQ33	IO_L9P_T1L_N4_AD12P_69	A29
PL_DDR4_DQ34	IO_L12P_T1U_N10_GC_69	C30
PL_DDR4_DQ35	IO_L9N_T1L_N5_AD12N_69	A30
PL_DDR4_DQ36	IO_L11P_T1U_N8_GC_69	E31
PL_DDR4_DQ37	IO_L8P_T1L_N2_AD5P_69	C29
PL_DDR4_DQ38	IO_L12N_T1U_N11_GC_69	C31
PL_DDR4_DQ39	IO_L8N_T1L_N3_AD5N_69	B30

PL_DDR4_DQ40	IO_L3N_T0L_N5_AD15N_69	F32
PL_DDR4_DQ41	IO_L5P_T0U_N8_AD14P_69	G28
PL_DDR4_DQ42	IO_L2N_T0L_N3_69	H30
PL_DDR4_DQ43	IO_L6P_T0U_N10_AD6P_69	J28
PL_DDR4_DQ44	IO_L2P_T0L_N2_69	J30
PL_DDR4_DQ45	IO_L6N_T0U_N11_AD6N_69	H28
PL_DDR4_DQ46	IO_L3P_T0L_N4_AD15P_69	F31
PL_DDR4_DQ47	IO_L5N_T0U_N9_AD14N_69	F29
PL_DDR4_DQ48	IO_L24P_T3U_N10_69	C42
PL_DDR4_DQ49	IO_L21N_T3L_N5_AD8N_69	A38
PL_DDR4_DQ50	IO_L23P_T3U_N8_69	B40
PL_DDR4_DQ51	IO_L20N_T3L_N3_AD1N_69	B37
PL_DDR4_DQ52	IO_L24N_T3U_N11_69	B42
PL_DDR4_DQ53	IO_L20P_T3L_N2_AD1P_69	B36
PL_DDR4_DQ54	IO_L23N_T3U_N9_69	B41
PL_DDR4_DQ55	IO_L21P_T3L_N4_AD8P_69	A37
PL_DDR4_DQ56	IO_L15N_T2L_N5_AD11N_69	C33
PL_DDR4_DQ57	IO_L17N_T2U_N9_AD10N_69	A35
PL_DDR4_DQ58	IO_L15P_T2L_N4_AD11P_69	D33
PL_DDR4_DQ59	IO_L14N_T2L_N3_GC_69	B33
PL_DDR4_DQ60	IO_L14P_T2L_N2_GC_69	B32

PL_DDR4_DQ61	IO_L18N_T2U_N11_AD2N_69	A34
PL_DDR4_DQ62	IO_L17P_T2U_N8_AD10P_69	B35
PL_DDR4_DQ63	IO_L18P_T2U_N10_AD2P_69	A33
PL_DDR4_DM0	IO_L7P_T1L_N0_QBC_AD13P_70	K27
PL_DDR4_DM1	IO_L1P_T0L_N0_DBC_70	P26
PL_DDR4_DM2	IO_L19P_T3L_N0_DBC_AD9P_70	C28
PL_DDR4_DM3	IO_L13P_T2L_N0_GC_QBC_70	G26
PL_DDR4_DM4	IO_L7P_T1L_N0_QBC_AD13P_69	E29
PL_DDR4_DM5	PIO_L1P_T0L_N0_DBC_69	K29
PL_DDR4_DM6	IO_L19P_T3L_N0_DBC_AD9P_69	C36
PL_DDR4_DM7	IO_L13P_T2L_N0_GC_QBC_69	E32
PL_DDR4_A0	IO_L6N_T0U_N11_AD6N_71	M21
PL_DDR4_A1	IO_L5N_T0U_N9_AD14N_71	N21
PL_DDR4_A2	IO_L16N_T2U_N7_QBC_AD3N_71	E20
PL_DDR4_A3	IO_L5P_T0U_N8_AD14P_71	P21
PL_DDR4_A4	IO_L17P_T2U_N8_AD10P_71	E21
PL_DDR4_A5	IO_L15N_T2L_N5_AD11N_71	E19
PL_DDR4_A6	IO_L6P_T0U_N10_AD6P_71	M22
PL_DDR4_A7	IO_L7N_T1L_N1_QBC_AD13N_71	J19
PL_DDR4_A8	IO_L9N_T1L_N5_AD12N_71	J21
PL_DDR4_A9	IO_L16P_T2U_N6_QBC_AD3P_71	F20

PL_DDR4_A10	IO_L8P_T1L_N2_AD5P_71	L20
PL_DDR4_A11	IO_L3P_T0L_N4_AD15P_71	M20
PL_DDR4_A12	IO_L4P_T0U_N6_DBC_AD7P_71	N20
PL_DDR4_A13	IO_L7P_T1L_N0_QBC_AD13P_71	K19
PL_DDR4_CS_B	IO_L4N_T0U_N7_DBC_AD7N_71	N19
PL_DDR4_ACT_B	IO_L8N_T1L_N3_AD5N_71	K20
PL_DDR4_ODT	IO_L9P_T1L_N4_AD12P_71	K21
PL_DDR4_WE_B	IO_L10N_T1U_N7_QBC_AD4N_71	J22
PL_DDR4_BA0	IO_L10P_T1U_N6_QBC_AD4P_71	K22
PL_DDR4_BA1	IO_L15P_T2L_N4_AD11P_71	F19
PL_DDR4_CAS_B	IO_L11N_T1U_N9_GC_71	H19
PL_DDR4_RAS_B	IO_L11P_T1U_N8_GC_71	H20
PL_DDR4_CLK_N	IO_L13N_T2L_N1_GC_QBC_71	G21
PL_DDR4_CLK_P	IO_L13P_T2L_N0_GC_QBC_71	G22
PL_DDR4_BG0	IO_L14N_T2L_N3_GC_71	F22
PL_DDR4_CKE	IO_L17N_T2U_N9_AD10N_71	D21
PL_DDR4_RST	IO_L14P_T2L_N2_GC_71	F23

1.4 QSPI Flash

The FPGA core board ACU19EG is equipped with two 256MBit Quad-SPI FLASH chip to form an 8-bit bandwidth data bus, the flash model is MT25QU512ABB1EW9-0SIT,

which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used as a boot device for the system to store the boot image of the system. These images mainly include FPGA bit files, ARM application code, and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 1-4-1.

Position	Model	Capacity	Factory
U2,U3	MT25QU512ABB1EW9-0SIT	512M bit	Micron

Table 1-4-1: QSPI FLASH Specification

QSPI FLASH is connected to the GPIO port of the BANK500 in the PS section of the ZYNQ chip. In the system design, the GPIO port functions of these PS ports need to be configured as the QSPI FLASH interface. Figure 1-4-1 shows the QSPI Flash in the schematic.

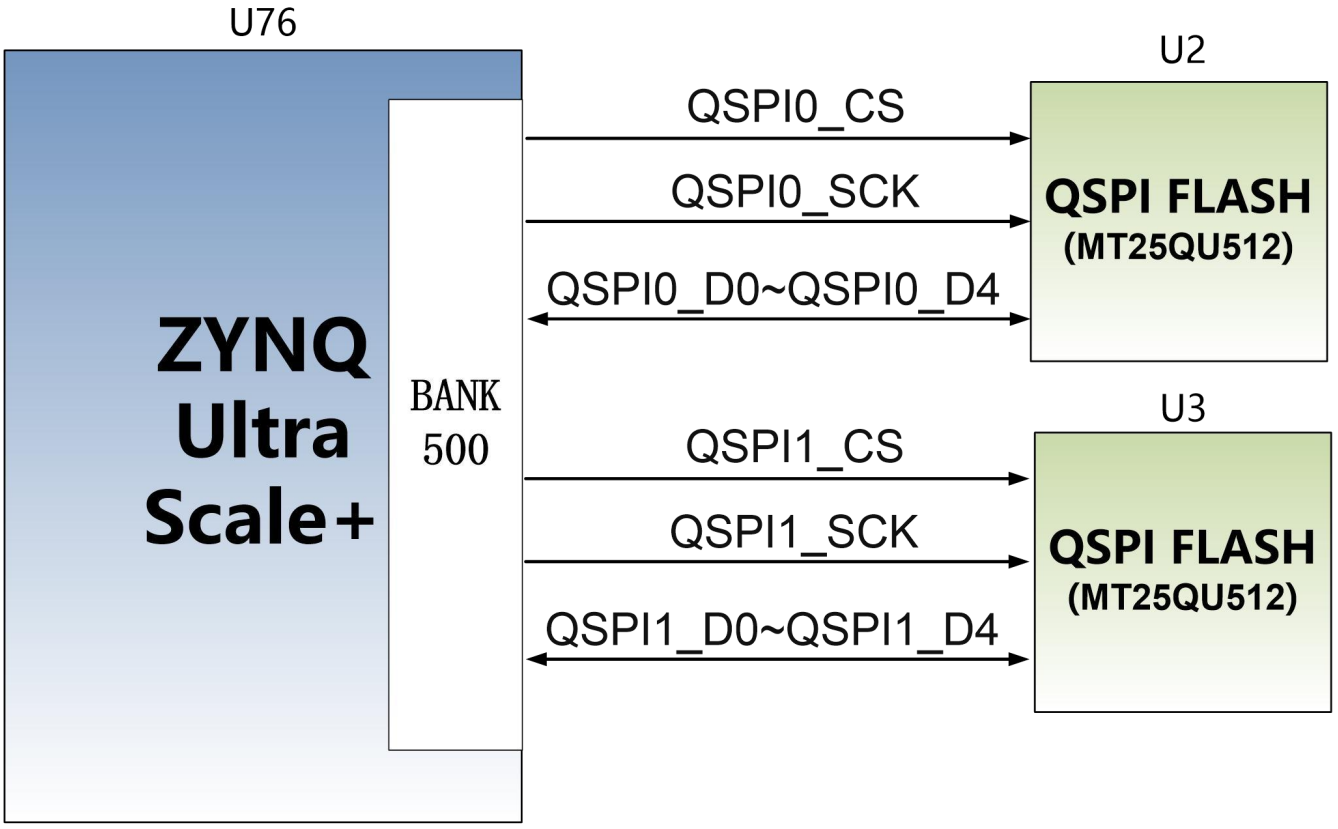


Figure 1-4-1: QSPI Flash in the schematic

Configure chip pin assignments:

Signal Name	Pin Name	Pin Number
MIO5_QSPI0_SS_B	PS_MIO5_500	AL32
MIO0_QSPI0_SCLK	PS_MIO0_500	AM33
MIO4_QSPI0_IO0	PS_MIO4_500	AL33
MIO1_QSPI0_IO1	PS_MIO1_500	AM29
MIO2_QSPI0_IO2	PS_MIO2_500	AM31
MIO3_QSPI0_IO3	PS_MIO3_500	AM30
MIO7_QSPI1_SS_B	PS_MIO7_500	AL30
MIO12_QSPI1_SCLK	PS_MIO12_500	AJ34
MIO8_QSPI1_IO0	PS_MIO8_500	AK33
MIO9_QSPI1_IO1	PS_MIO9_500	AK34
MIO10_QSPI1_IO2	PS_MIO10_500	AK30
MIO11_QSPI1_IO3	PS_MIO11_500	AK32

1.5 eMMC Flash

The ACU19EG core board is equipped with MTFC32GAPALBH-IT, a large-capacity 32GB eMMC FLASH chip, which supports the HS-MMC interface of the JEDEC e-MMC V5.0 standard, and supports 1.8V or 3.3V level. The data width of eMMC FLASH and ZYNQ connection is 8bit. Due to the large-capacity and non-volatile characteristics of eMMC FLASH, it can be used as a large-capacity storage device in the ZYNQ system,

such as storing ARM applications, system files and other user data files The specific models and related parameters of eMMC FLASH are shown in Table 1-5-1.

Position	Model	Capacity	Factory
U8	MTFC32GAPALBH-IT	32G Byte	Micron

Table 1-5-1: eMMC FLASH Specification

The eMMC FLASH is connected to the GPIO port of PS' s BANK500 of the ZYNQ UltraScale+. As for the design of system, it is necessary to configure the GPIO port function of the PS side as an EMMC interface. Figure 1-5-1 shows eMMC Flash in the schematic diagram.

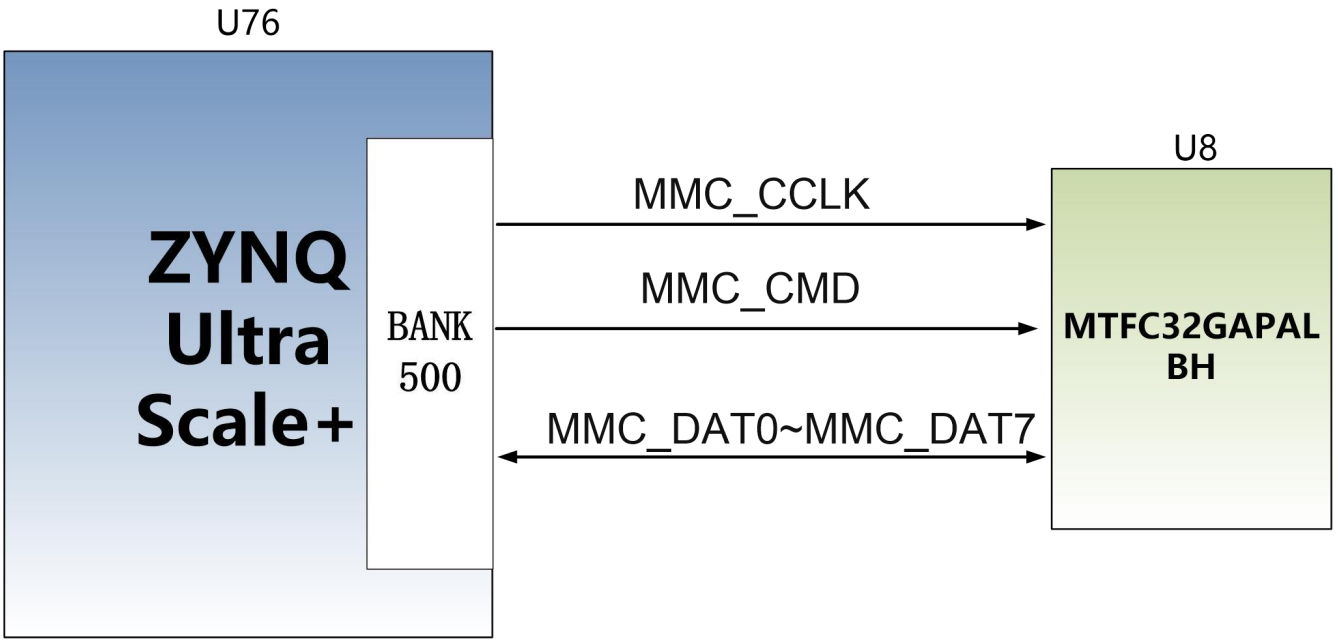


Figure 1-5-1: eMMC Flash in the schematic

Configuration Chip pin assignment:

Signal Name	Pin Name	Pin Number
MMC_CCLK	PS_MIO22_500	AH32
MMC_CMD	PS_MIO21_500	AF35

MMC_DAT0	PS_MIO13_500	AD34
MMC_DAT1	PS_MIO14_500	AJ32
MMC_DAT2	PS_MIO15_500	AD35
MMC_DAT3	PS_MIO16_500	AJ31
MMC_DAT4	PS_MIO17_500	AJ30
MMC_DAT5	PS_MIO18_500	AE34
MMC_DAT6	PS_MIO19_500	AE35
MMC_DAT7	PS_MIO20_500	AH34
MMC_RSTN	PS_MIO23_500	AG35

1.6 Clock configuration

The core board provides reference clock and RTC real-time clock for PS system and PL logic respectively, so that PS system and PL logic can work independently. The schematic diagram of the clock circuit design is shown in Figure 1-6-1:

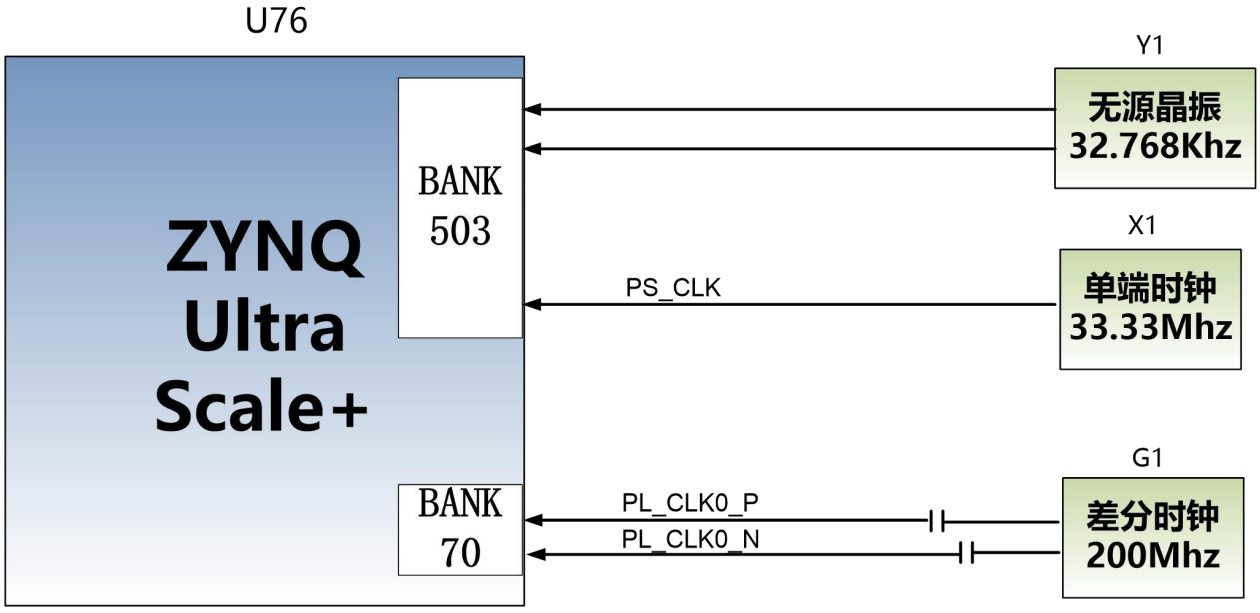


Figure 1-6-1: Core Board Clock Source

PS System RTC Real Time Clock

The passive crystal Y1 on the core board provides a 32.768KHz real-time clock source for the PS system. The crystal is connected to the PS_PADI_503 and PS_PADO_503 pins of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 1-6-2:

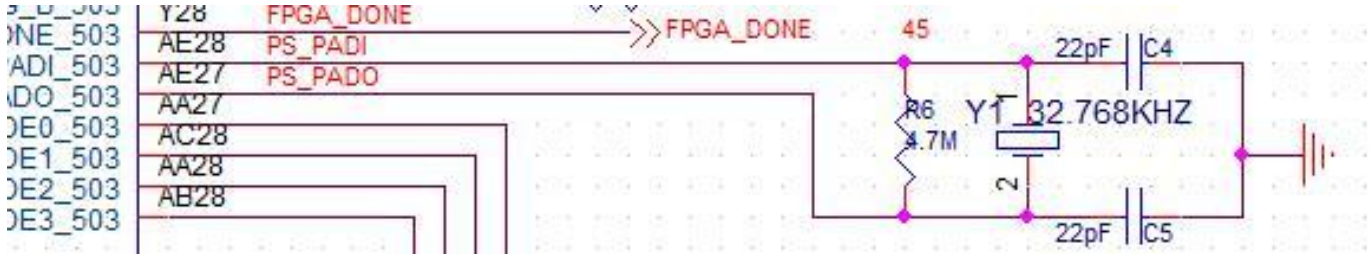


Figure 1-6-2: Passive Crystal Oscillator for RTC

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	AC27

PS System Clock Source

The X1 crystal on the core board provides a 33.333MHz clock input for the PS part. The clock input is connected to the PS_REF_CLK_503 pin of BANK503 of the ZYNQ chip. The schematic diagram is shown in Figure 1-6-3:

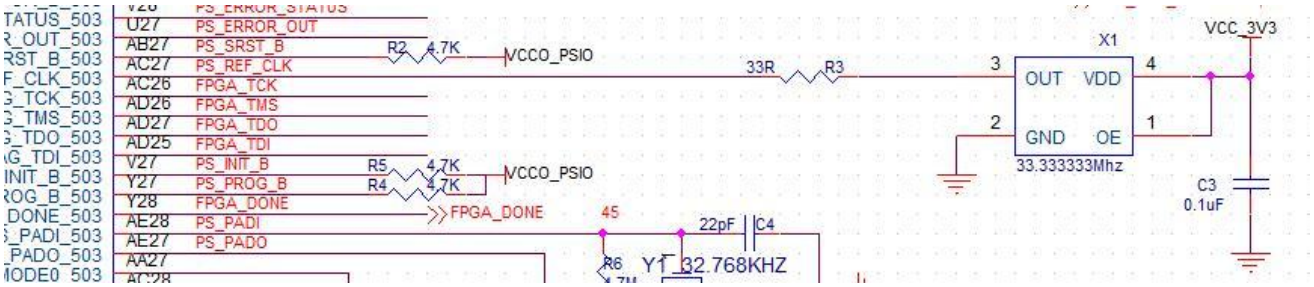


Figure 1-6-3: Active Crystal in PS part

Clock pin assignment:

Signal Name	Pin
PS_REF_CLK	AC27

PL System Clock Source

The core board provides a differential 200MHz PL system clock source for the reference clock of the DDR4 controller. The crystal oscillator output is connected to the global clock (MRCC) of PL BANK71. This global clock can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of this clock source is shown in Figure 1-6-4.

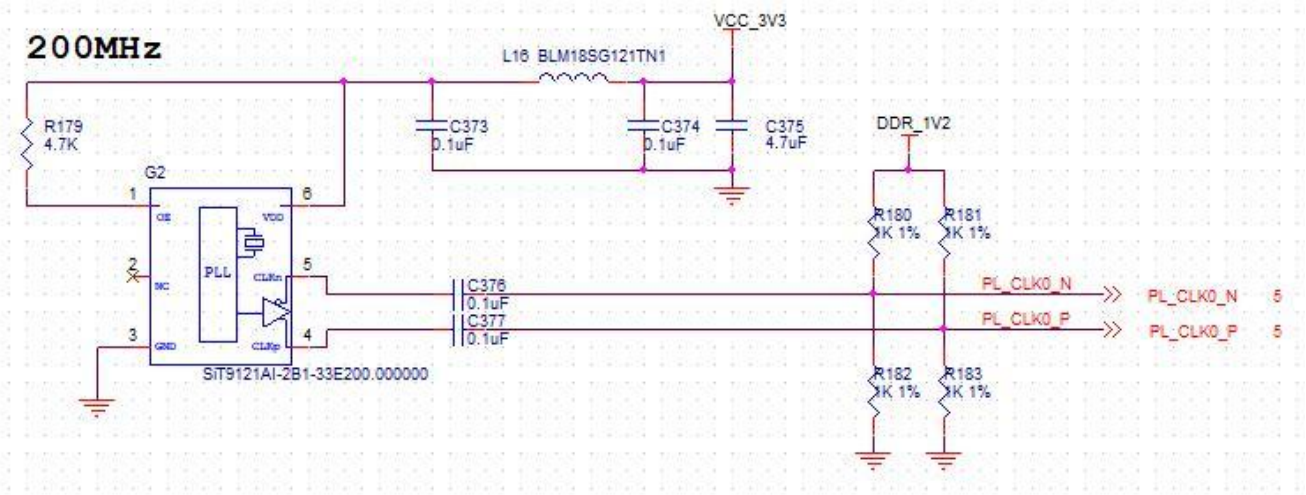


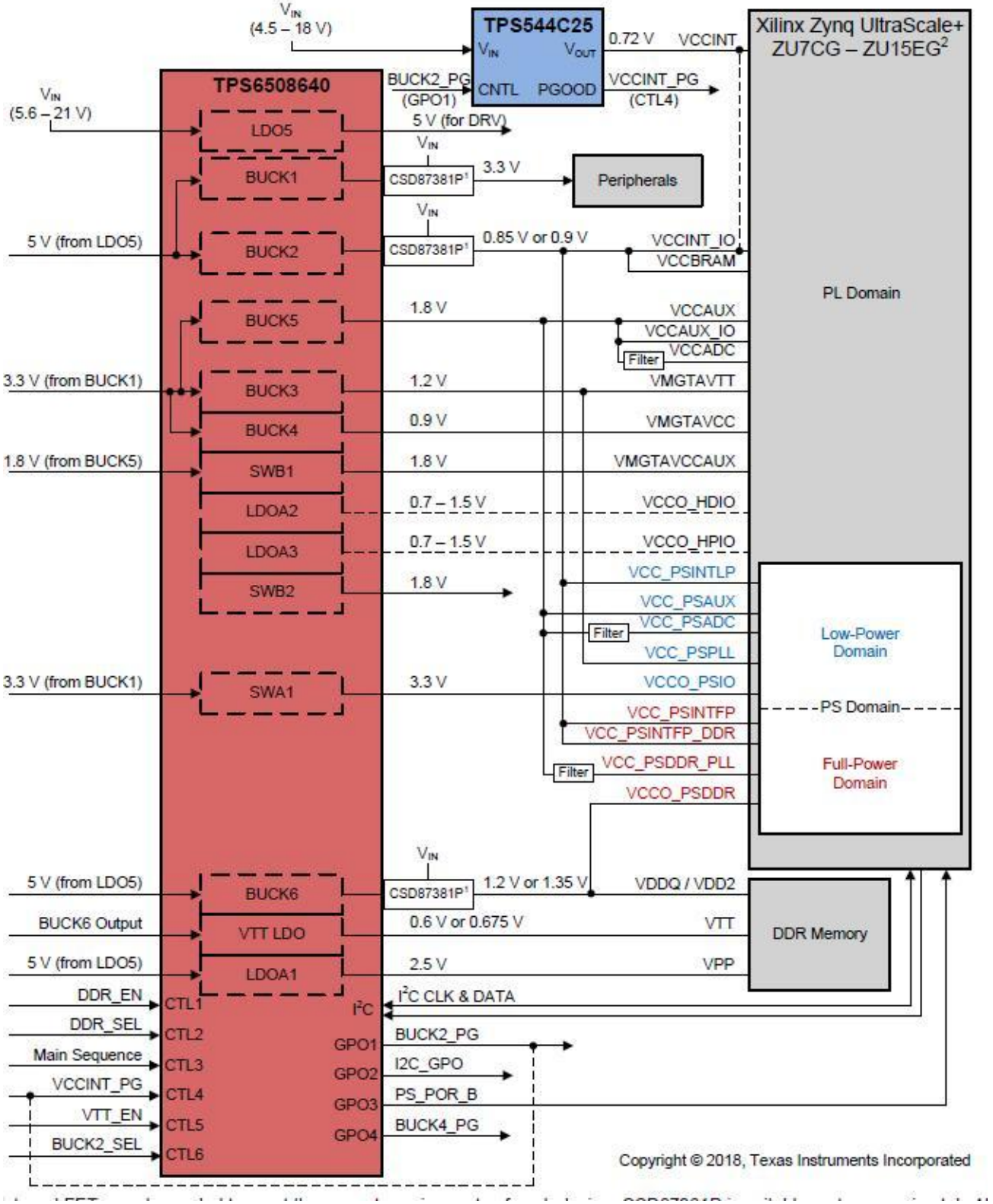
Figure 1-6-4: PL system clock source

Clock pin assignment:

Signal Name	Pin
PL_CLK0_P	H21
PL_CLK0_N	G20

1.7 Power Supply

The power supply voltage of the ACU19EG core board is +12V, which is supplied by connecting the carrier board. The core board uses one MAX20796GFB+ power chips to achieve a 60A current to provide XCZU19EG with 0.85V core power, uses two TPS74801DRCR power chips generate 0.85V and 1.8V voltages respectively to supply power to the PS_MGT, and uses two MAX20812AFH+ power chips generate 2-channel 0.9V and 2-channel 1.2V voltages respectively to supply power to the PL-MGT. In addition, it also uses one PMIC chip TPS6508640 to generate all other power supplies required by the XCZU15EG chip. For the design of TPS6508640 power supply , please refer to the power supply chip manual. The design block diagram is as follows:


V_IN (4.5 – 18 V)
TPS544C25
V_IN
V_OUT
CNTL
PGOOD
0.72 V
VCCINT
Xilinx Zynq UltraScale+ ZU7CG – ZU15EG²
BUCK2_PG (GPO1)
VCCINT_PG (CTL4)
TPS6508640
V_IN (5.6 – 21 V)
LDO5
5 V (for DRV)
BUCK1
CSD87381P¹
3.3 V
Peripherals
5 V (from LDO5)
BUCK2
0.85 V or 0.9 V
VCCINT_IO
VCCBRAM
PL Domain
BUCK5
1.8 V
VCCAUX
VCCAUX_IO
VCCADC
Filter
3.3 V (from BUCK1)
BUCK3
1.2 V
VMGTAVTT
BUCK4
0.9 V
VMGTAVCC
1.8 V (from BUCK5)
SWB1
1.8 V
VMGTAVCCAUX
LDOA2
0.7 – 1.5 V
VCCO_HDIO
LDOA3
0.7 – 1.5 V
VCCO_HPIO
SWB2
1.8 V
VCC_PSINTLP
VCC_PSAUX
VCC_PSADC
Filter
VCC_PSPLL
Low-Power Domain
3.3 V (from BUCK1)
SWA1
3.3 V
VCCO_PSIO
PS Domain
VCC_PSINTFP
VCC_PSINTFP_DDR
VCC_PSDDR_PLL
Filter
Full-Power Domain
VCCO_PSDDR
5 V (from LDO5)
BUCK6
1.2 V or 1.35 V
VDDQ / VDD2
BUCK6 Output
VTT LDO
0.6 V or 0.675 V
VTT
DDR Memory
5 V (from LDO5)
LDOA1
2.5 V
VPP
DDR_EN
CTL1
I²C
I²C CLK & DATA
DDR_SEL
CTL2
GPO1
BUCK2_PG
Main Sequence
CTL3
GPO2
I2C_GPO
VCCINT_PG
CTL4
GPO3
PS_POR_B
VTT_EN
CTL5
GPO4
BUCK4_PG
BUCK2_SEL
CTL6
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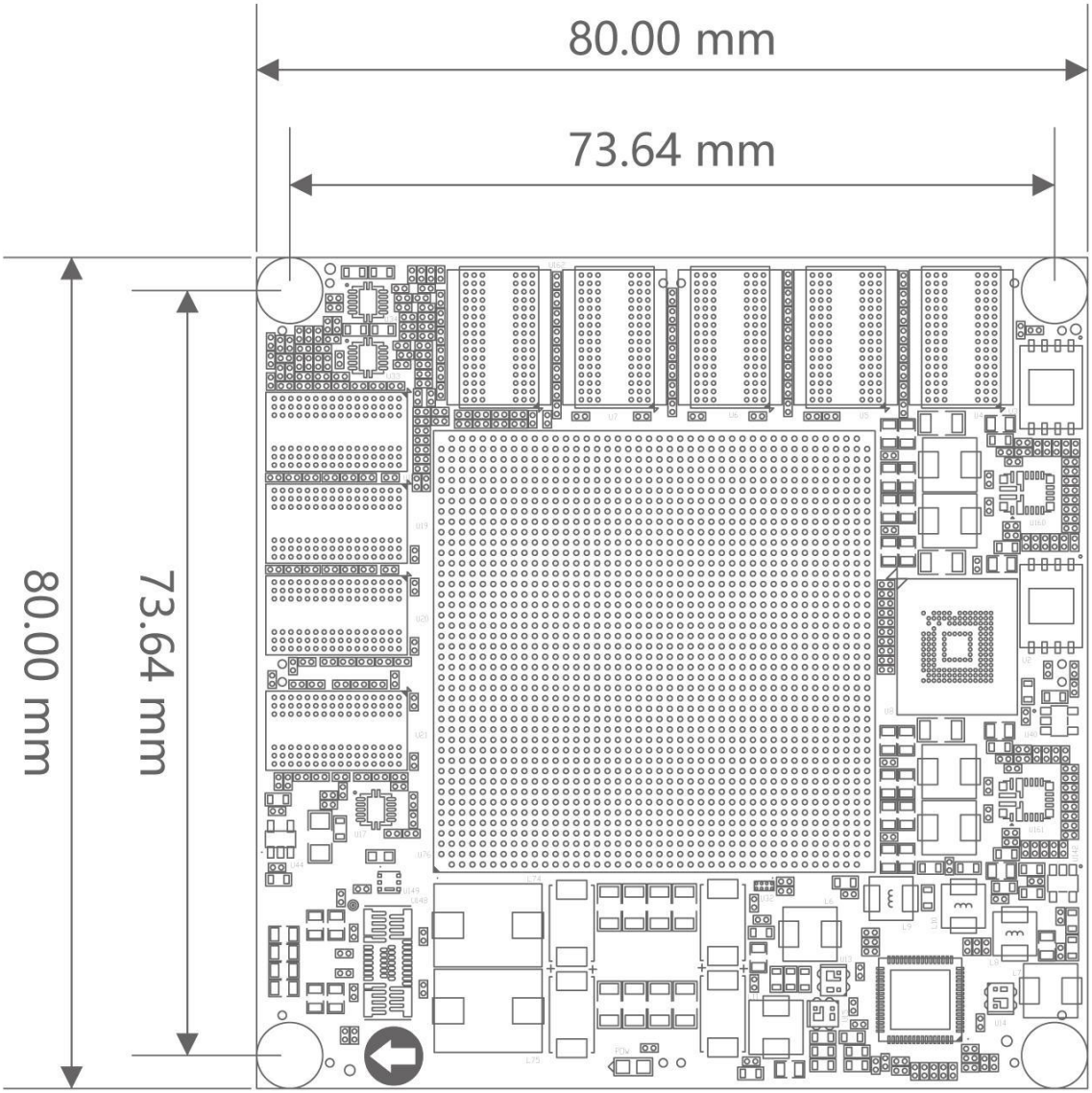
1.8 ACU19EG Core Board Size Dimension

Top View:



1.9 Board to Board Connectors Pin Assignment

The core board has a total of eight high-speed expansion ports. It uses eight 120-pin inter-board connectors (J29~J36) to connect to the carrier board. The connectors used is Panasonic AXK5A2137YG, and the corresponding connector model in the carrier board is Panasonic AXK6A2337YG.

Pin assignment of board to board connector J29

The J29 is connected to the GTY transceiver signal of BANK128, 129,130,131.

J29 Pin	Signal Name	Pin Number	J29 Pin	Signal Name	Pin Number
1	131_CLK0_P	L32	2	131_CLK1_P	J32
3	131_CLK0_N	L33	4	131_CLK1_N	J33
5	GND		6	GND	
7	131_RX3_P	D39	8	131_TX3_P	E36
9	131_RX3_N	D40	10	131_TX3_N	E37
11	GND		12	GND	
13	131_RX2_P	E41	14	131_TX2_P	F34
15	131_RX2_N	E42	16	131_TX2_N	F35
17	GND		18	GND	
19	131_RX1_P	F39	20	131_TX1_P	G36
21	131_RX1_N	F40	22	131_TX1_N	G37
23	GND		24	GND	
25	131_RX0_P	G41	26	131_TX0_P	H34
27	131_RX0_N	G42	28	131_TX0_N	H35
29	GND		30	GND	
31	130_CLK0_P	R32	32	130_CLK1_P	N32
33	130_CLK0_N	R33	34	130_CLK1_N	N33
35	GND		36	GND	
37	130_RX3_P	H39	38	130_TX3_P	J36
39	130_RX3_N	H40	40	130_TX3_N	J37
41	GND		42	GND	
43	130_RX2_P	J41	44	130_TX2_P	K34
45	130_RX2_N	J42	46	130_TX2_N	K35

47	GND		48	GND	
49	130_RX1_P	K39	50	130_TX1_P	L36
51	130_RX1_N	K40	52	130_TX1_N	L37
53	GND		54	GND	
55	130_RX0_P	L41	56	130_TX0_P	M34
57	130_RX0_N	L42	58	130_TX0_N	M35
59	GND		60	GND	
61	129_CLK0_P	W32	62	129_CLK1_P	U32
63	129_CLK0_N	W33	64	129_CLK1_N	U33
65	GND		66	GND	
67	129_RX3_P	M39	68	129_TX3_P	N36
69	129_RX3_N	M40	70	129_TX3_N	N37
71	GND		72	GND	
73	129_RX2_P	N41	74	129_TX2_P	P34
75	129_RX2_N	N42	76	129_TX2_N	P35
77	GND		78	GND	
79	129_RX1_P	P39	80	129_TX1_P	R36
81	129_RX1_N	P40	82	129_TX1_N	R37
83	GND		84	GND	
85	129_RX0_P	R41	86	129_TX0_P	T34
87	129_RX0_N	R42	88	129_TX0_N	T35
89	GND		90	GND	
91	128_CLK0_P	AB34	92	128_CLK1_P	AA32
93	128_CLK0_N	AB35	94	128_CLK1_N	AA33
95	GND		96	GND	
97	128_RX3_P	T39	98	128_TX3_P	U36
99	128_RX3_N	T40	100	128_TX3_N	U37
101	GND		102	GND	
103	128_RX2_P	U41	104	128_TX2_P	V34
105	128_RX2_N	U42	106	128_TX2_N	V35
107	GND		108	GND	
109	128_RX1_P	V39	110	128_TX1_P	W36
111	128_RX1_N	V40	112	128_TX1_N	W37
113	GND		114	GND	
115	128_RX0_P	W41	116	128_TX0_P	Y34
117	128_RX0_N	W42	118	128_TX0_N	Y35
119	GND		120	GND	

Pin assignment of board to board connector J30

J31 is connected to the IO of BANK64 and BANK65. The level standard of BANK64, 65 is +1.8V.

J30 Pin	Signal Name	Pin Number	J30 Pin	Signal Name	Pin Number
1	B65_L10_N	AV28	2	B65_L18_N	AT28
3	B65_L10_P	AU28	4	B65_L18_P	AR28
5	B65_L16_N	AP27	6	B65_L15_N	AN26
7	B65_L16_P	AN27	8	B65_L15_P	AM26
9	GND		10	GND	
11	B65_L13_N	AT27	12	B65_L9_N	AW27
13	B65_L13_P	AR27	14	B65_L9_P	AV27
15	B65_L5_N	AY28	16	B65_L12_N	AT26
17	B65_L5_P	AY27	18	B65_L12_P	AT25
19	GND		20	GND	
21	B65_L8_N	AW26	22	B65_L11_N	AU26
23	B65_L8_P	AV26	24	B65_L11_P	AU25
25	B65_L20_N	AP25	26	B65_L6_N	BB28
27	B65_L20_P	AP24	28	B65_L6_P	BA28
29	GND		30	GND	
31	B65_L4_N	BB26	32	B65_L14_N	AR25
33	B65_L4_P	BA26	34	B65_L14_P	AR24
35	B65_L2_N	BB25	36	B65_L3_N	BA25
37	B65_L2_P	BB24	38	B65_L3_P	AY25
39	GND		40	GND	
41	B65_L7_N	AV24	42	B65_L1_N	AY24
43	B65_L7_P	AU24	44	B65_L1_P	AW24
45	B65_L21_N	AN24	46	B65_L22_N	AN23
47	B65_L21_P	AM24	48	B65_L22_P	AM23
49	GND		50	GND	
51	B65_L19_N	AT23	52	B65_L23_N	AL23
53	B65_L19_P	AR23	54	B65_L23_P	AK23
55	B65_L24_N	AK24	56	B65_L17_N	AN28
57	B65_L24_P	AJ24	58	B65_L17_P	AM28
59	GND		60	GND	
61	B64_L23_P	AJ21	62	B64_L1_P	BA23

63	B64_L23_N	AJ20	64	B64_L1_N	BB23
65	B64_L24_P	AJ22	66	B64_L16_P	AN21
67	B64_L24_N	AK22	68	B64_L16_N	AP21
69	GND		70	GND	
71	B64_L7_P	AU23	72	B64_L22_P	AK20
73	B64_L7_N	AV23	74	B64_L22_N	AK19
75	B64_L2_P	AY23	76	B64_L19_P	AM19
77	B64_L2_N	AY22	78	B64_L19_N	AN19
79	GND		80	GND	
81	B64_L20_P	AM21	82	B64_L14_P	AT20
83	B64_L20_N	AM20	84	B64_L14_N	AU19
85	B64_L11_P	AU21	86	B64_L3_P	BA22
87	B64_L11_N	AV21	88	B64_L3_N	BA21
89	GND		90	GND	
91	B64_L18_P	AP19	92	B64_L5_P	BB20
93	B64_L18_N	AR19	94	B64_L5_N	BB19
95	B64_L8_P	AV22	96	B64_L6_P	BA18
97	B64_L8_N	AW22	98	B64_L6_N	BB18
99	GND		100	GND	
101	B64_L21_P	AL22	102	B64_L9_P	AW20
103	B64_L21_N	AL21	104	B64_L9_N	AW19
105	B64_L15_P	AN22	106	B64_L10_P	AY19
107	B64_L15_N	AP22	108	B64_L10_N	AY18
109	GND		110	GND	
111	B64_L13_P	AT22	112	B64_L4_P	AY20
113	B64_L13_N	AT21	114	B64_L4_N	BA20
115	B64_L17_P	AP20	116	B64_L12_P	AU20
117	B64_L17_N	AR20	118	B64_L12_N	AV19
119	GND		120	GND	

Pin assignment of board to board connector J32

J32 is connected to the IO of BANK66 and BANK67. The level standard of BANK66, 67 is +1.8V.

J32 Pin	Signal Name	Pin Number	J32 Pin	Signal Name	Pin Number

1	B66_L3_P	AW17	2	B66_L4_P	BA15
3	B66_L3_N	AW16	4	B66_L4_N	BB15
5	B66_L1_P	AY17	6	B66_L15_P	AU18
7	B66_L1_N	BA17	8	B66_L15_N	AV18
9	GND		10	GND	
11	B66_L13_P	AV17	12	B66_L16_P	AR18
13	B66_L13_N	AV16	14	B66_L16_N	AT18
15	B66_L17_P	AR17	16	B66_L2_P	BA16
17	B66_L17_N	AT17	18	B66_L2_N	BB16
19	GND		20	GND	
21	B66_L5_P	AY15	22	B66_L20_P	AL18
23	B66_L5_N	AY14	24	B66_L20_N	AM18
25	B66_L19_P	AJ18	26	B66_L21_P	AN18
27	B66_L19_N	AK18	28	B66_L21_N	AN17
29	GND		30	GND	
31	B66_L11_P	AW15	32	B66_L14_P	AT15
33	B66_L11_N	AW14	34	B66_L14_N	AU15
35	B66_L24_P	AN16	36	B66_L18_P	AT16
37	B66_L24_N	AP16	38	B66_L18_N	AU16
39	GND		40	GND	
41	B66_L22_P	AJ17	42	B66_L23_P	AL16
43	B66_L22_N	AK17	44	B66_L23_N	AM16
45	B66_L10_P	AU13	46	B66_L12_P	AU14
47	B66_L10_N	AV13	48	B66_L12_N	AV14
49	GND		50	GND	
51	B66_L7_P	AY12	52	B66_L9_P	BA10
53	B66_L7_N	BA12	54	B66_L9_N	BB10
55	B66_L8_P	BA11	56	B66_L6_P	BA13
57	B66_L8_N	BB11	58	B66_L6_N	BB13
59	GND		60	GND	
61	B67_L23_P	AM13	62	B67_L15_P	AR15
63	B67_L23_N	AN13	64	B67_L15_N	AR14
65	B67_L12_P	AT11	66	B67_L7_P	AV12
67	B67_L12_N	AT10	68	B67_L7_N	AW12
69	GND		70	GND	
71	B67_L16_P	AN12	72	B67_L11_P	AT13
73	B67_L16_N	AP12	74	B67_L11_N	AT12

75	B67_L14_P	AP10	76	B67_L13_P	AR13
77	B67_L14_N	AR10	78	B67_L13_N	AR12
79	GND		80	GND	
81	B67_L9_P	AW11	82	B67_L24_P	AJ14
83	B67_L9_N	AW10	84	B67_L24_N	AK14
85	B67_L3_P	AW8	86	B67_L22_P	AN14
87	B67_L3_N	AY8	88	B67_L22_N	AP14
89	GND		90	GND	
91	B67_L1_P	AW9	92	B67_L19_P	AL15
93	B67_L1_N	AY9	94	B67_L19_N	AM15
95	B67_L20_P	AJ15	96	B67_L17_P	AM11
97	B67_L20_N	AK15	98	B67_L17_N	AN11
99	GND		100	GND	
101	B67_L4_P	BA8	102	B67_L21_P	AL14
103	B67_L4_N	BA7	104	B67_L21_N	AM14
105	B67_L10_P	AV9	106	B67_L8_P	AU11
107	B67_L10_N	AV8	108	B67_L8_N	AV11
109	GND		110	GND	
111	B67_L2_P	BB9	112	B67_L5_P	BA6
113	B67_L2_N	BB8	114	B67_L5_N	BB6
115	B67_L6_P	BB5	116	B67_L18_P	AM10
117	B67_L6_N	BB4	118	B67_L18_N	AN10
119	GND		120	GND	

Pin assignment of board to board connector J33

The J33 is connected to the GTH transceiver signals of BANK224, 225, 226, 227.

J33 Pin	Signal Name	Pin Number	J33 Pin	Signal Name	Pin Number
1	224_TX0_N	AY3	2	224_RX0_N	BA1
3	224_TX0_P	AY4	4	224_RX0_P	BA2
5	GND		6	GND	
7	224_TX1_N	AW5	8	224_RX1_N	AW1
9	224_TX1_P	AW6	10	224_RX1_P	AW2
11	GND		12	GND	
13	224_TX2_N	AU5	14	224_RX2_N	AV3
15	224_TX2_P	AU6	16	224_RX2_P	AV4

17	GND		18	GND	
19	224_TX3_N	AT7	20	224_RX3_N	AU1
21	224_TX3_P	AT8	22	224_RX3_P	AU2
23	GND		24	GND	
25	224_CLK0_N	AK11	26	224_CLK1_N	AJ9
27	224_CLK0_P	AK12	28	224_CLK1_P	AJ10
29	GND		30	GND	
31	225_TX0_N	AR5	32	225_RX0_N	AT3
33	225_TX0_P	AR6	34	225_RX0_P	AT4
35	GND		36	GND	
37	225_TX1_N	AP7	38	225_RX1_N	AR1
39	225_TX1_P	AP8	40	225_RX1_P	AR2
41	GND		42	GND	
43	225_TX2_N	AN5	44	225_RX2_N	AP3
45	225_TX2_P	AN6	46	225_RX2_P	AP4
47	GND		48	GND	
49	225_TX3_N	AM7	50	225_RX3_N	AN1
51	225_TX3_P	AM8	52	225_RX3_P	AN2
53	GND		54	GND	
55	225_CLK0_N	AH11	56	225_CLK1_N	AG9
57	225_CLK0_P	AH12	58	225_CLK1_P	AG10
59	GND		60	GND	
61	226_TX0_N	AL5	62	226_RX0_N	AM3
63	226_TX0_P	AL6	64	226_RX0_P	AM4
65	GND		66	GND	
67	226_TX1_N	AK7	68	226_RX1_N	AL1
69	226_TX1_P	AK8	70	226_RX1_P	AL2
71	GND		72	GND	
73	226_TX2_N	AJ5	74	226_RX2_N	AK3
75	226_TX2_P	AJ6	76	226_RX2_P	AK4
77	GND		78	GND	
79	226_TX3_N	AH7	80	226_RX3_N	AJ1
81	226_TX3_P	AH8	82	226_RX3_P	AJ2
83	GND		84	GND	
85	226_CLK0_N	AF11	86	226_CLK1_N	AE9
87	226_CLK0_P	AF12	88	226_CLK1_P	AE10
89	GND		90	GND	

91	227_TX0_N	AG5	92	227_RX0_N	AH3
93	227_TX0_P	AG6	94	227_RX0_P	AH4
95	GND		96	GND	
97	227_TX1_N	AF7	98	227_RX1_N	AG1
99	227_TX1_P	AF8	100	227_RX1_P	AG2
101	GND		102	GND	
103	227_TX2_N	AE5	104	227_RX2_N	AF3
105	227_TX2_P	AE6	106	227_RX2_P	AF4
107	GND		108	GND	
109	227_TX3_N	AD7	110	227_RX3_N	AE1
111	227_TX3_P	AD8	112	227_RX3_P	AE2
113	GND		114	GND	
115	227_CLK0_N	AD11	116	227_CLK1_N	AC9
117	227_CLK0_P	AD12	118	227_CLK1_P	AC10
119	GND		120	GND	

Pin assignment of board to board connector J34

The J34 is connected to the GTH transceiver signals of BANK228, 229, 230, 231.

J34 Pin	Signal Name	Pin Number	J34 Pin	Signal Name	Pin Number
1	228_TX0_N	AC5	2	228_RX0_N	AD3
3	228_TX0_P	AC6	4	228_RX0_P	AD4
5	GND		6	GND	
7	228_TX1_N	AB7	8	228_RX1_N	AC1
9	228_TX1_P	AB8	10	228_RX1_P	AC2
11	GND		12	GND	
13	228_TX2_N	AA5	14	228_RX2_N	AB3
15	228_TX2_P	AA6	16	228_RX2_P	AB4
17	GND		18	GND	
19	228_TX3_N	Y7	20	228_RX3_N	AA1
21	228_TX3_P	Y8	22	228_RX3_P	AA2
23	GND		24	GND	
25	228_CLK1_N	AA9	26	228_CLK0_N	AB11
27	228_CLK1_P	AA10	28	228_CLK0_P	AB12
29	GND		30	GND	

31	229_TX0_N	W5	32	229_RX0_N	Y3
33	229_TX0_P	W6	34	229_RX0_P	Y4
35	GND		36	GND	
37	229_TX1_N	V7	38	229_RX1_N	W1
39	229_TX1_P	V8	40	229_RX1_P	W2
41	GND		42	GND	
43	229_TX2_N	U5	44	229_RX2_N	V3
45	229_TX2_P	U6	46	229_RX2_P	V4
47	GND		48	GND	
49	229_TX3_N	T7	50	229_RX3_N	U1
51	229_TX3_P	T8	52	229_RX3_P	U2
53	GND		54	GND	
55	229_CLK1_N	W9	56	229_CLK0_N	Y11
57	229_CLK1_P	W10	58	229_CLK0_P	Y12
59	GND		60	GND	
61	230_TX0_N	R5	62	230_RX0_N	T3
63	230_TX0_P	R6	64	230_RX0_P	T4
65	GND		66	GND	
67	230_TX1_N	P7	68	230_RX1_N	R1
69	230_TX1_P	P8	70	230_RX1_P	R2
71	GND		72	GND	
73	230_TX2_N	N5	74	230_RX2_N	P3
75	230_TX2_P	N6	76	230_RX2_P	P4
77	GND		78	GND	
79	230_TX3_N	M7	80	230_RX3_N	N1
81	230_TX3_P	M8	82	230_RX3_P	N2
83	GND		84	GND	
85	230_CLK1_N	U9	86	230_CLK0_N	V11
87	230_CLK1_P	U10	88	230_CLK0_P	V12
89	GND		90	GND	
91	231_TX0_N	L5	92	231_RX0_N	M3
93	231_TX0_P	L6	94	231_RX0_P	M4
95	GND		96	GND	
97	231_TX1_N	K3	98	231_RX1_N	L1
99	231_TX1_P	K4	100	231_RX1_P	L2
101	GND		102	GND	
103	231_TX2_N	J5	104	231_RX2_N	J1

105	231_TX2_P	J6	106	231_RX2_P	J2
107	GND		108	GND	AC20
109	231_TX3_N	H3	110	231_RX3_N	G1
111	231_TX3_P	H4	112	231_RX3_P	G2
113	GND		114	GND	
115	231_CLK1_N	R9	116	231_CLK0_N	T11
117	231_CLK1_P	R10	118	231_CLK0_P	T12
119	GND		120	GND	

Pin assignment of board to board connector J35

J35 is connected to +12V power supply and IO of BANK91,BANK93 and BANK94;

The level standard of BANK91,93,94 is 3.3V.

J35 Pin	Signal Name	Pin Number	J35 Pin	Signal Name	Pin Number
1	+12V		2	GND	
3	+12V		4	GND	
5	+12V		6	GND	
7	+12V		8	GND	
9	+12V		10	GND	
11	+12V		12	GND	
13	+12V		14	GND	
15	+12V		16	GND	
17	+12V		18	GND	
19	+12V		20	GND	
21	+12V		22	GND	
23	+12V		24	GND	
25	+12V		26	GND	
27	+12V		28	GND	
29	+12V		30	GND	
31	GND		32	GND	
33	B94_L5_N	D3	34	B94_L8_N	C3
35	B94_L5_P	D4	36	B94_L8_P	C4
37	B94_L7_N	C5	38	B94_L12_N	A4
39	B94_L7_P	C6	40	B94_L12_P	A5
41	GND		42	GND	

43	B94_L3_N	E2	44	B94_L4_N	D1
45	B94_L3_P	E3	46	B94_L4_P	E1
47	B94_L6_N	C1	48	B94_L9_N	B1
49	B94_L6_P	D2	50	B94_L9_P	B2
51	GND		52	GND	
53	B94_L1_N	F4	54	B94_L11_N	B5
55	B94_L1_P	F5	56	B94_L11_P	B6
57	B94_L10_N	A3	58	B94_L2_N	E4
59	B94_L10_P	B3	60	B94_L2_P	E5
61	GND		62	GND	
63	B93_L10_N	A7	64	B93_L1_N	F6
65	B93_L10_P	B7	66	B93_L1_P	G6
67	B93_L9_N	D6	68	B93_L5_N	F7
69	B93_L9_P	E6	70	B93_L5_P	G7
71	GND		72	GND	
73	B93_L7_N	D7	74	B93_L2_N	H8
75	B93_L7_P	E7	76	B93_L2_P	J8
77	B93_L8_N	C8	78	B93_L4_N	E9
79	B93_L8_P	D8	80	B93_L4_P	F9
81	GND		82	GND	
83	B93_L3_N	H9	84	B93_L6_N	F8
85	B93_L3_P	J9	86	B93_L6_P	G8
87	B93_L11_N	A8	88	B93_L12_N	C9
89	B93_L11_P	B8	90	B93_L12_P	D9
91	GND		92	GND	
93	B91_L12_N	A9	94	B91_L7_N	E10
95	B91_L12_P	A10	96	B91_L7_P	E11
97	B91_L5_N	F10	98	B91_L1_N	H10
99	B91_L5_P	G10	100	B91_L1_P	J11
101	GND		102	GND	
103	B91_L10_N	B10	104	B91_L9_N	C11
105	B91_L10_P	C10	106	B91_L9_P	D11
107	B91_L11_N	B11	108	B91_L2_N	G11
109	B91_L11_P	B12	110	B91_L2_P	H11
111	GND		112	GND	
113	B91_L3_N	G12	114	B91_L8_N	D12
115	B91_L3_P	H13	116	B91_L8_P	E12

117	B91_L4_N	G13	118	B91_L6_N	F12
119	B91_L4_P	H14	120	B91_L6_P	F13

Pin assignment of board to board connector J36

The J36 is connected to the BANK power supply of VCCIO64~68 and the IO of BANK68 and BANK90. BANK68 has a level standard of +1.8V and BANK90 has a level standard of +3.3V.

J36 Pin	Signal Name	Pin Number	J36 Pin	Signal Name	Pin Number
1	VCCO_68		2	B68_L16_N	A12
3	VCCO_68		4	B68_L16_P	B13
5	GND		6	B68_L17_N	A13
7	GND		8	B68_L17_P	A14
9	VCCO_67		10	GND	
11	VCCO_67		12	B68_L15_N	C13
13	GND		14	B68_L15_P	D13
15	GND		16	B68_L1_N	N15
17	VCCO_66		18	B68_L1_P	P15
19	VCCO_66		20	GND	
21	GND		22	B68_L14_N	D14
23	GND		24	B68_L14_P	E15
25	VCCO_64		26	B68_L13_N	E14
27	VCCO_64		28	B68_L13_P	F14
29	GND		30	GND	
31	GND		32	B68_L18_N	B15
33	VCCO_65		34	B68_L18_P	C15
35	VCCO_65		36	B68_L12_N	F15
37	GND		38	B68_L12_P	G16
39	GND		40	GND	
41	悬空		42	B68_L20_N	B16
43	悬空		44	B68_L20_P	C16
45	悬空		46	B68_L19_N	D16
47	悬空		48	B68_L19_P	E16
49	GND		50	GND	

51	悬空		52	B68_L22_N	A17
53	悬空		54	B68_L22_P	B17
55	悬空		56	B68_L21_N	D17
57	悬空		58	B68_L21_P	E17
59	GND		60	GND	
61	B90_L12_N	J12	62	B68_L24_N	A18
63	B90_L12_P	J13	64	B68_L24_P	B18
65	B90_L7_N	K12	66	B68_L23_N	C18
67	B90_L7_P	L12	68	B68_L23_P	D18
69	GND		70	GND	
71	B90_L10_N	K10	72	B68_L7_N	G15
73	B90_L10_P	K11	74	B68_L7_P	H15
75	B90_L8_N	L13	76	B68_L5_N	K15
77	B90_L8_P	L14	78	B68_L5_P	K16
79	GND		80	GND	
81	B90_L11_N	J14	82	B68_L11_N	F17
83	B90_L11_P	K14	84	B68_L11_P	G17
85	B90_L5_N	M13	86	B68_L10_N	F18
87	B90_L5_P	N13	88	B68_L10_P	G18
89	GND		90	GND	
91	B90_L4_N	N14	92	B68_L8_N	H16
93	B90_L4_P	P14	94	B68_L8_P	J16
95	B90_L3_N	P13	96	B68_L6_N	K17
97	B90_L3_P	R14	98	B68_L6_P	L17
99	GND		100	GND	
101	B90_L2_N	N12	102	B68_L9_N	H18
103	B90_L2_P	P12	104	B68_L9_P	J18
105	B90_L9_N	L10	106	B68_L3_N	M16
107	B90_L9_P	M10	108	B68_L3_P	M17
109	GND		110	GND	
111	B90_L6_N	M11	112	B68_L4_N	L15
113	B90_L6_P	M12	114	B68_L4_P	M15
115	B90_L1_N	N10	116	B68_L2_N	N16
117	B90_L1_P	N11	118	B68_L2_P	P16
119	GND		120	GND	