8-Channel AD Acquisition Module AN706 User Manual

ALINX

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Part 1: 8-Channel AD Acquisition Module Parameters

- Module VPN: AN706
- AD Chip: AD7606
- Channel: 8-channel
- AD bits: 16-bit
- Max Sample Rate: 200KSPS
- Input Voltage Rate: -5V~+5V
- PCB layers of Module: 4-Layer，independent power layer and GND layer
- Module Interface: 40-pin 0.1 inch spacing female header, download direction
- Ambient Temperature (with power applied: -40°~85°, all the chips on module to meet the industrial requirements
- Input interface: 8 SMA interfaces and 16-pin headers with 2.54 pitch (Pin Each channel has positive and negative two Pin)
- Measurement accuracy: Within 0.5mV

Part 2: Module structure

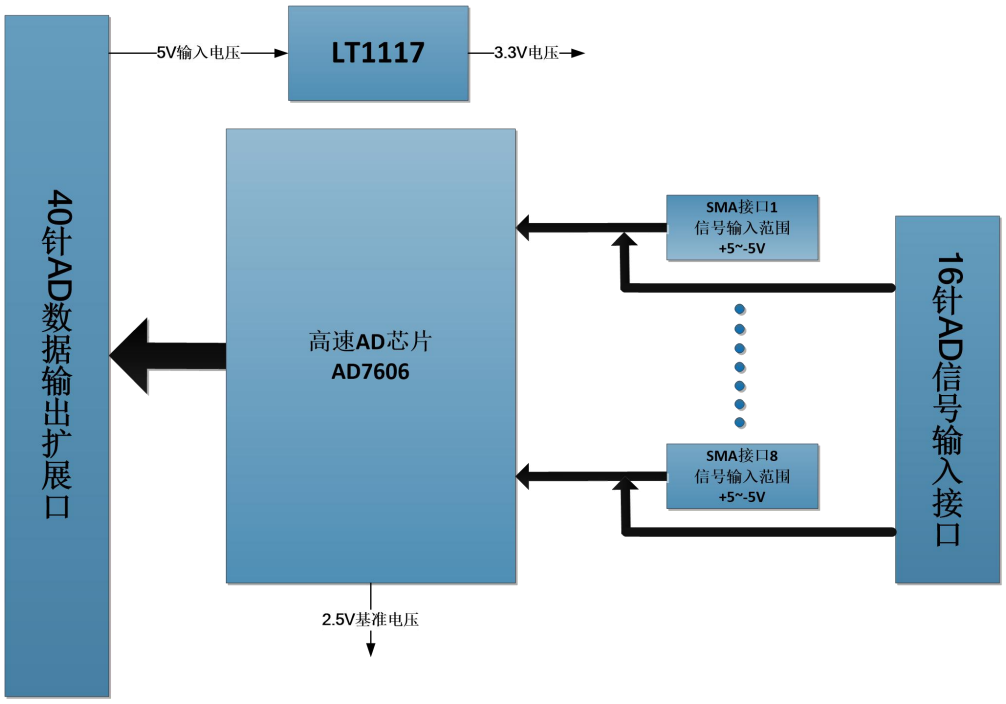


Figure 2-1: The 8-channel AD module structure

Part 3: AD7606 Chip Introduction

The AD76061 is 16-bit, simultaneous sampling, analog-to-digital data acquisition systems (DAS) with eight, six, and four channels, respectively. Each part contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, a 16-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference

The input clamp protection circuitry can tolerate voltages up to ±16.5 V. The AD7606/AD7606-6/AD7606-4 operate from a single 5 V supply and can accommodate ±10 V and ±5 V true bipolar input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to ±16.5 V.

The AD7606 has 1 MΩ analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input

impedance eliminate the need for driver op amps and external bipolar supplies. The AD7606/AD7606-6/AD7606-4 antialiasing filter has a 3 dB cutoff frequency of 22 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the 3 dB bandwidth.

Part 4: AD7606 Chip Functional Block Diagram

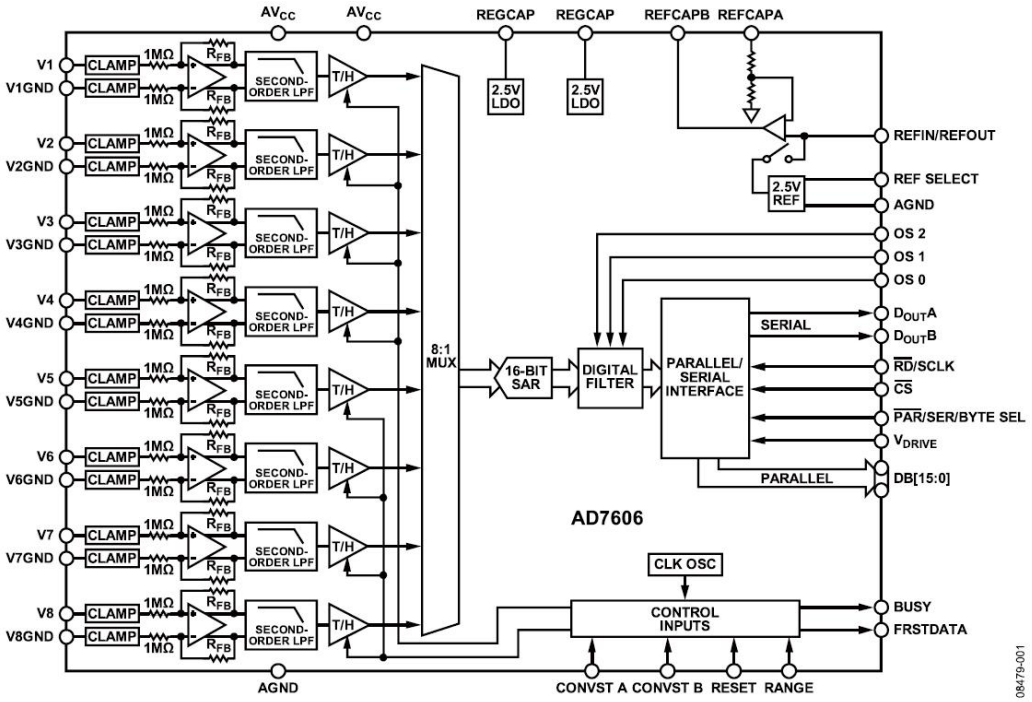
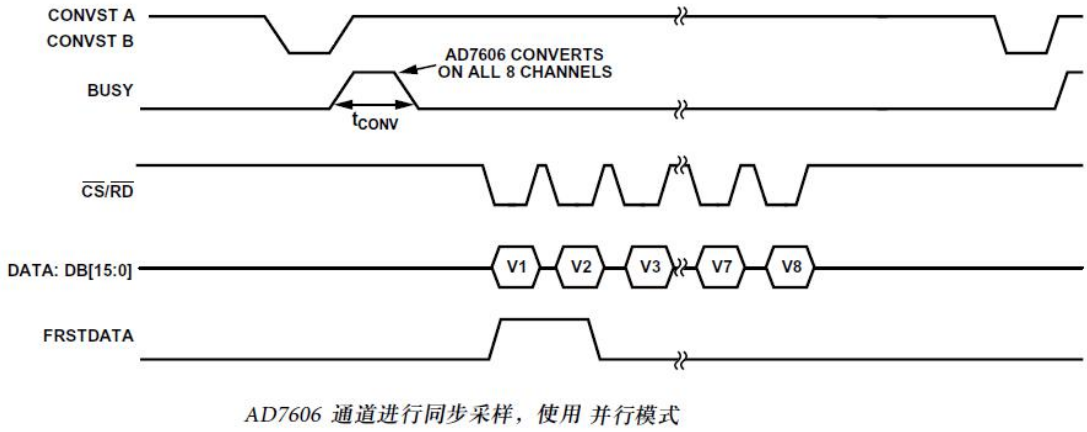


Figure 4-1: AD7606 Functional Block Diagram

Part 5: AD7606 Chip Timing Specification



AD7606 通道进行同步采样，使用 并行模式

Figure5-1: AD7606 Timing Diagrams

The AD7606 allow simultaneous sampling of all eight analog input channels. All channels are sampled simul-taneously when both CONVST pins (CONVST A, CONVST B) are tied together. A single CONVST signal is used to control both CONVST x inputs. The rising edge of this common CONVST signal initiates simultaneous sampling on all analog input channels (V1 to V8).

The AD7606 contains an on-chip oscillator that is used to perform the conversions. The conversion time for all ADC channels is t_{CONV}. The BUSY signal indicates to the user when conversions are in progress, so when the rising edge of CONVST is applied, BUSY goes logic high and transitions low at the end of the entire conversion process. The falling edge of the BUSY signal is used to place all eight track-and-hold amplifiers back into track mode. The falling edge of BUSY also indicates that the new data can now be read from the parallel bus (DB[15:0]), the $D_{OUT}A$ and $D_{OUT}B$ serial data lines, or the parallel byte bus, DB[7:0].

Part 6: AD7606 Chip Pin Configuration

In the AN706 8-channel AD module hardware circuit design, we set the AD7606's operating mode by adding pull-up or pull-down resistors to the three configuration pins of the AD7606.

1. The AD7606 supports an external reference input or an internal reference. If an external reference is used, the REFIN/REFOUT of the chip requires an external 2.5V reference. If using an internal reference voltage. The REFIN/REFOUT pin is an internal 2.5V reference. The REF SELECT pin is used to select the internal reference or external reference. In this module, because the accuracy of the internal reference voltage of the AD7606 is also very high (2.49V~2.505V), the circuit design chooses to use the internal reference voltage.

Pin Name	Set level	Description
REF SELECT	High Level	Use internal reference voltage 2.5V

2. The AD7606's AD conversion data acquisition can be in parallel mode or serial mode. The user can set the communication mode by setting the PAR/SER/BYTE SEL pin level. in the AN706 module design, select parallel mode to read AD data of AD7606

Pin Name	Set level	Description
PAR/SER/BYTE SEL	Low Level	Select parallel interface

3. The RANGE pin is used to select either ±10 V or ±5 V as the input range in AD9767. In the ±5 V range, 1LSB=152.58uV. In the ±10 V range, 1LSB=305.175 uV. In the circuit design of AN706 module, select ±5V analog voltage input range

Pin Name	Set level	Description
RANGE	Low Level	Analog signal input range selection：±5V

4. The AD7606 contains an optional digital first-order sinc filter that should be used in applications where slower throughput rates are used or where higher signal-to-noise ratio or dynamic range is desirable. The oversampling ratio of the digital filter is controlled using the oversampling pins, OS [2:0] (see Table below). OS 2 is the MSB control bit, and OS 0 is the LSB control bit. Table below provides the oversampling bit decoding to select the different oversample rates. The OS pins are latched on the falling edge of BUSY.

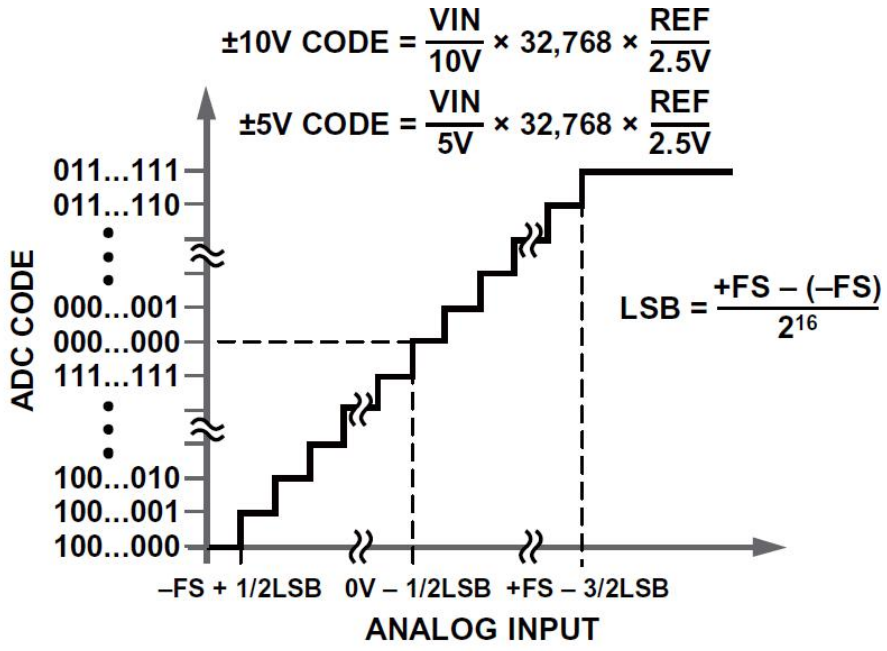
Table 9. Oversample Bit Decoding

OS[2:0]	OS Ratio	SNR 5 V Range (dB)	SNR 10 V Range (dB)	3 dB BW 5 V Range (kHz)	3 dB BW 10 V Range (kHz)	Maximum Throughput CONVST Frequency (kHz)
000	No OS	89	90	15	22	200
001	2	91.2	92	15	22	100
010	4	92.6	93.6	13.7	18.5	50
011	8	94.2	95	10.3	11.9	25
100	16	95.5	96	6	6	12.5
101	32	96.4	96.7	3	3	6.25
110	64	96.9	97	1.5	1.5	3.125
111	Invalid					

In the hardware design of the AN706 module, OS[2:0] leads to the external interface, and the FPGA or CPU can select whether to use the filter by controlling the pin level of OS[2:0] to achieve higher measurement accuracy.

Part 7: AD7606 Chip ADC TRANSFER FUNCTION

The output coding of the AD7606 is two's complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB and 3/2 LSB. The LSB size is FSR/65,536 for the AD7606. The ideal transfer characteristic for the AD7606 is shown in Figure 7-1.



	+FS	MIDSCALE	–FS	LSB
±10V RANGE	+10V	0V	–10V	305μV
±5V RANGE	+5V	0V	–5V	152μV

Figure 7-1: AD7606 Transfer Characteristics

Part 8: Interface definition (The labeled pin on the PCB is pin 1)

Pin	Signal Name	Description	Pin	Signal Name	Description
1	GND	Ground	2	VCC	+5V
3	OS1	Oversampling Select	4	OS0	Oversampling Select
5	CONVSTAB	Data conversion	6	OS2	Oversampling Select
7	RD	Read	8	RESET	Reset
9	BUSY	Busy	10	CS	Chip Select

11			12	FIRSTDATA	First data
13			14		
15	DB0	AD Data Bus	16	DB1	AD Data Bus
17	DB2	AD Data Bus	18	DB3	AD Data Bus
19	DB4	AD Data Bus	20	DB5	AD Data Bus
21	DB6	AD Data Bus	22	DB7	AD Data Bus
23	DB8	AD Data Bus	24	DB9	AD Data Bus
25	DB10	AD Data Bus	26	DB11	AD Data Bus

Part 9: AN706 Module Experimental procedure

1) First, connect the AN706 module to the 34-pin standard expansion port of the ALINX FPGA Development Board (In case the development board is powered off).
2) Connect your signal source to the AN706 Module input connector (Note: AD port input range: -5V~+5V).
3) Download the program to the FPGA using the Quartus II or ISE software (if you need the testing programs, send email to rachel.zhou@alinx.com.cn).
4) Open the serial debugging assistant tool and set the communication baud rate of the serial port as follows

Figure 9-1: The Serial Debugging Assistant Tool

5) The voltage value of the 8-channel signal input of the AN706 module will appear in the serial communication. (Because the 8-way data is displayed in one line in the serial debugging assistant, we need to enlarge the interface.)

Figure 9-2: Serial Communication

The above data is 8 channels of data without signal input, because the AD signal input is in a floating state, and the AD conversion output data is about 1.75V.

Example: If you connect the input of channel 1 with the 3.3V test pin on the AN706 module with a DuPont line to test the voltage of 3.3V on the module.

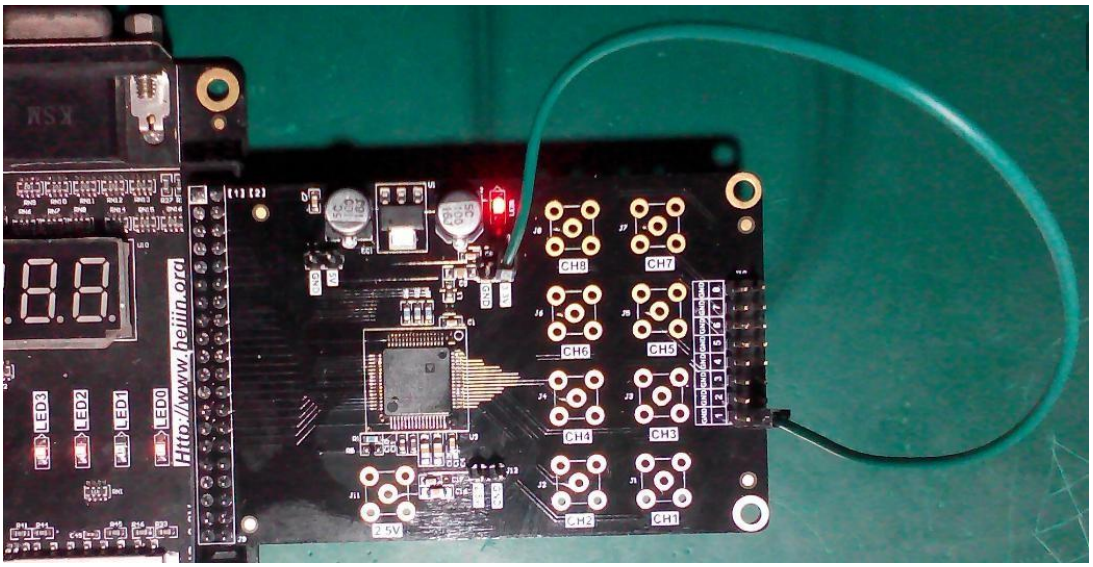


Figure 9-3: Channel 1 with 3.3V test pin

At this time, the measurement data of AD1 displayed on the serial interface is about +3.3074.

Figure 9-4: Test pin voltage display on the serial interface

Part 10: AN706 Module Measurement Accuracy

By measuring the applied voltage and the high-precision voltmeter, the actual measurement accuracy of the AD706 module is within 0.5mV within the -5V to +5V voltage input range.

The following table shows the results of eight channels for four analog voltages. The first column is the data measured by the high-precision digital multimeter, and the last eight columns are the results of the AD module's AD module measurement.

基准(mV)	CH1测量值(mV)	CH2测量值(mV)	CH3测量值(mV)	CH4测量值(mV)	CH5测量值(mV)	CH6测量值(mV)	CH7测量值(mV)	CH8测量值(mV)
64	63.7	64.2	64	63.7	63.7	63.6	64.5	63.3
1542.6	1542.9	1543.2	1543.4	1543.1	1543.1	1543.0	1543.8	1542.6
3050	3050.9	3050.3	3051.6	3050.6	3050.3	3050.9	3051.3	3050
4528.7	4529.2	4529.8	4530.6	4530	4529.7	4530.1	4530.4	4529.1

Table 10-1: Testing Voltage

In this test routine, the oversampling override enable filter is not used to improve the accuracy of the AN706 module. For users who want to further improve the accuracy of sampling and the sampling speed is not high, it can be set in the program. Method of sampling magnification, you can set the oversampling ratio in the program.

Part 11: AN706 Module test program description

The following is a brief description of the ideas for each Verilog test programs, and users can also refer to the note description in the code.

1. **Top level program: ad706_test.v**

   Define the FPGA and AN706 modules and the serial port to receive and send the signal input and output, and instantiate three subroutines (ad7606.v, volt_cal.v and uart.v).

2. **AD data acquisition program: ad7606.v**

According to the timing of the AD7606, sample 16 analog signals AD converted 16-bit data. The program first sends the CONVSTAB signal to the AD7606 to start AD data conversion, and waits for the Busy signal to go low to read the data of AD channel 1 to channel 16 in sequence.

AD Voltage Conversion (1 LSB)=5V/ 32758=0.15 mV

AD 电压换算(1 LSB) = 5V / 32758 = 0.15mV

3. **Voltage conversion program for AD data: volt_cal.v**

   The program converts the 16-bit data collected from ad7606.v, Bit[15] into positive and negative signs, and Bit[14:0] first converts it into a voltage value by the following formula, and then converts the hexadecimal voltage value into 20-digit BCD code.

4. **Serial port sending program: uart.v**

   Timing sends 8 channels of voltage data to the PC through uart. The serial port's transmit clock is obtained by dividing the frequency by 50Mhz, and the baud rate is 9600bps.