7-inch LCD Touch Screen Module AN970

User Manual

ALINX

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Part 1: 7” LCD Touch Screen Module Description

The ALINX 7-inch LCD touch screen module (AN970) is a combination of a 7-inch TFT LCD screen and a capacitive touch screen. The LCD screen adopts the 7-inch TFT LCD screen of Tianma. The model of the LCD screen is TM070RDH13.

The AN970 LCD touch screen module consists of a TFT LCD screen, a capacitive touch screen and a driver board. Figure 1-1 is the AN970 module product photo as below:

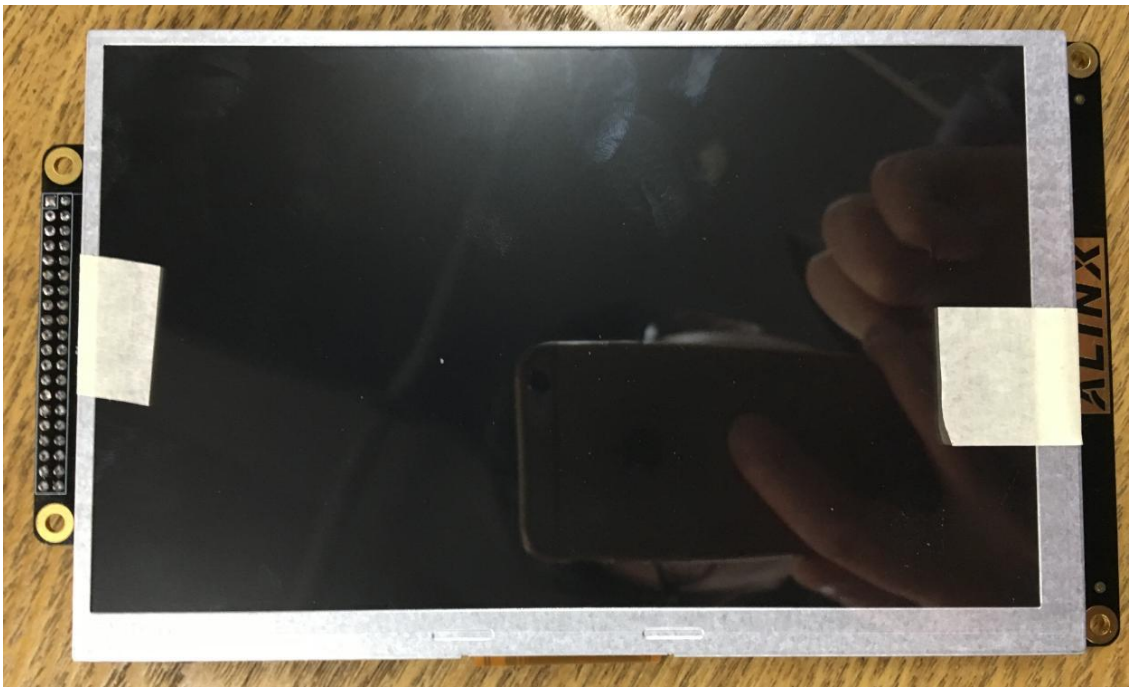

Figure 1-1: AN970 Module Product Photo

Part 1.1: AN970 LCD Touch Screen Module Detail Parameter

7”LCD display LCD Touch Screen module detail parameter listed:

- 7”LCD display module size dimension: detailed as Figure 1-2
- LCD screen size: 7.0 inches (diagonal)

- Display pixels: 800 (horizontal) x 480 (vertical)
- Color depth: 16.7M colors (RGB 24-bit color)
- Power and power consumption: single power supply 5V, power consumption is 1.8 watts

Figure 1-3: AN871 Module Size Dimension

Part 1.2: AN970 LCD Drive Timing

Horizontal Input Timing

The LCD screen display mode starts from the top left corner of the screen and is displayed point by point from left to right. Each time a line is displayed, it returns to the start position of the next line on the left side of the screen. During this time, the rows need to be blanked, and at the end of each line, the line sync signal is used for synchronization. There are two ways to drive the LCD, one is HV mode and the other is DE mode, both of which can drive the LCD screen, and the data is sampled on the rising edge of DCLK.

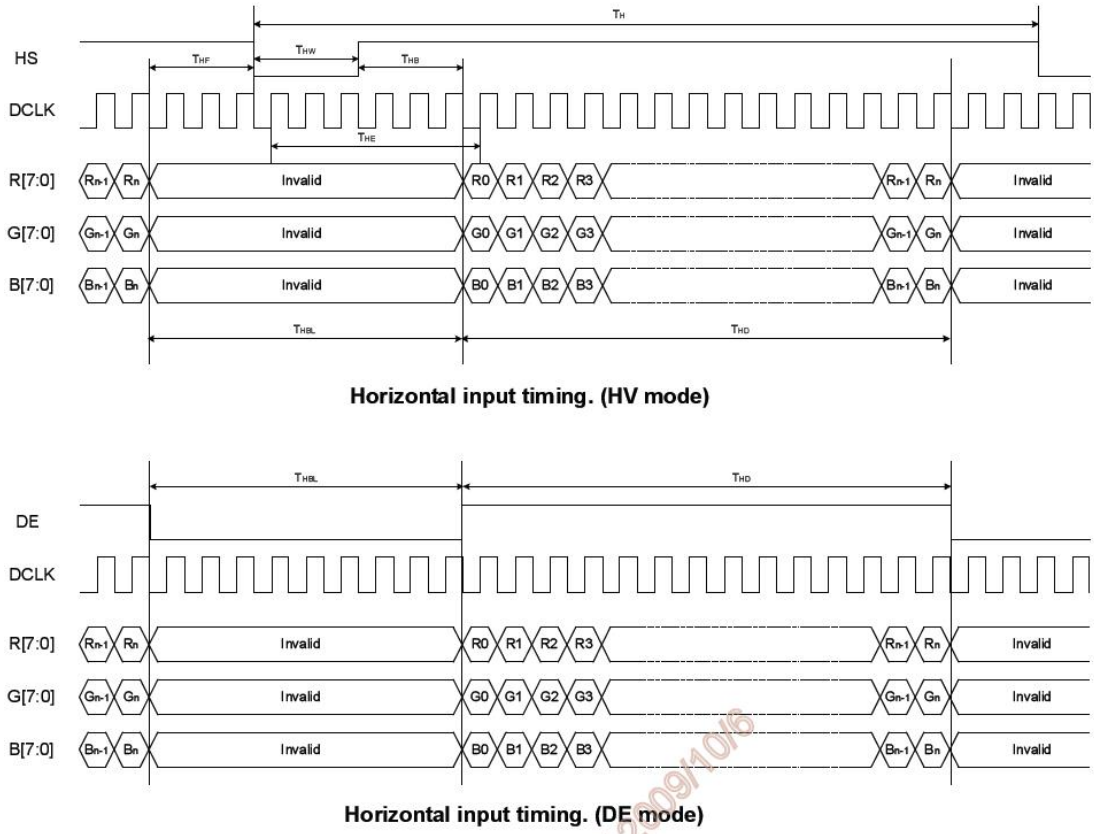

Figure 1-4: Horizontal Input Timing

Table 1-1 detailed the parameters of horizontal input timing

Horizontal Input Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
DCLK frequency	FDCLK	25	33	40	MHz	
DCLK period	TDCLK	25	30.3	40	ns	
Hsync Period (=THD+THBL)	TH	889	1056	1183	DCLK	
Active Area	THD	--	800	--	DCLK	
Horizontal Blanking	THBL	89	256	383	DCLK	
Hsync Front Porch	THF	1	40	--	DCLK	
Delay from Hsync to 1st data	THE	88	216	343	DCLK	
Hsync Pulse Width	THW	1	128	136	DCLK	
Hsync Back Porch	THB	T_{HE}-T_{HW}	88	T_{HE}-T_{HW}	DCLK	

Table 1-1: The Parameters of Horizontal Input Timing

Part 2: Hardware Connection

40-pin 0.1”spacing female header P4, connect directly to the expansion port of the development board with a 40-pin female header, so that the connection is simple and reliable.

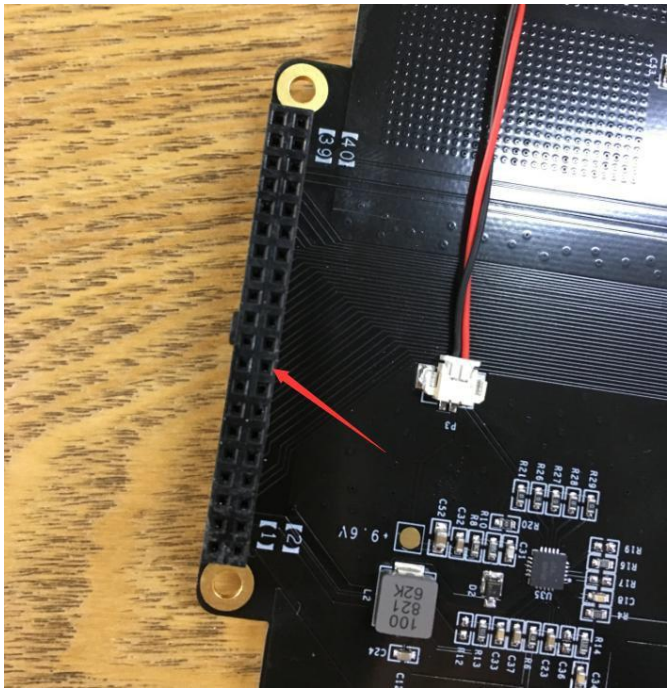

Figure 2-1: The 7-inch LCD Touch Screen Module Connection Interfaces

40-pin female header connection

The signal definition of the female header 40-pin is compatible with the 40-pin expansion port on the ALINX FPGA development board, and can be directly inserted into the development board. The following is a schematic diagram of the hardware connection between the AX301B development board and the 7-inch LCD touch screen module:

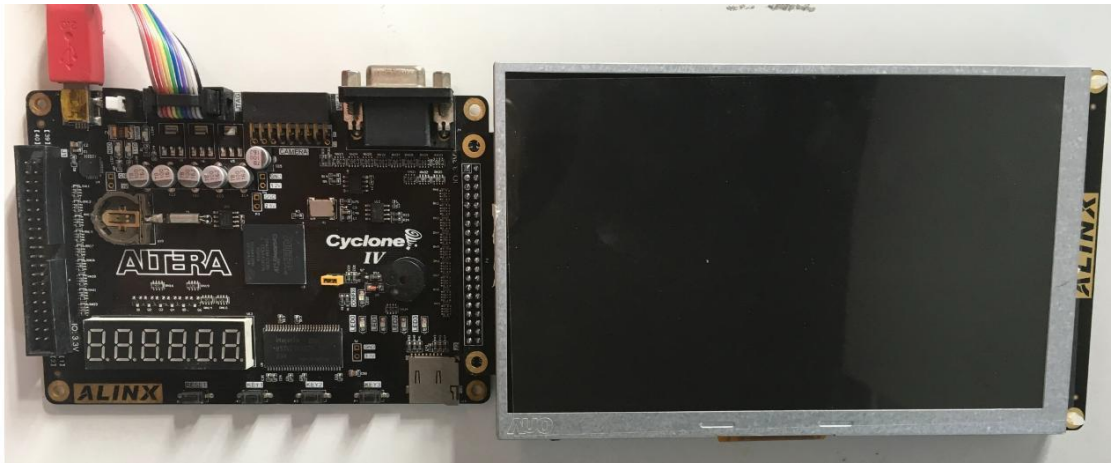

Figure 2-2: Hardware connection

The signal definition of the 40-pin 0.1”spacing female headers on the 7-inch LCD touch screen module is shown in the figure 2-3 and Table 2-1

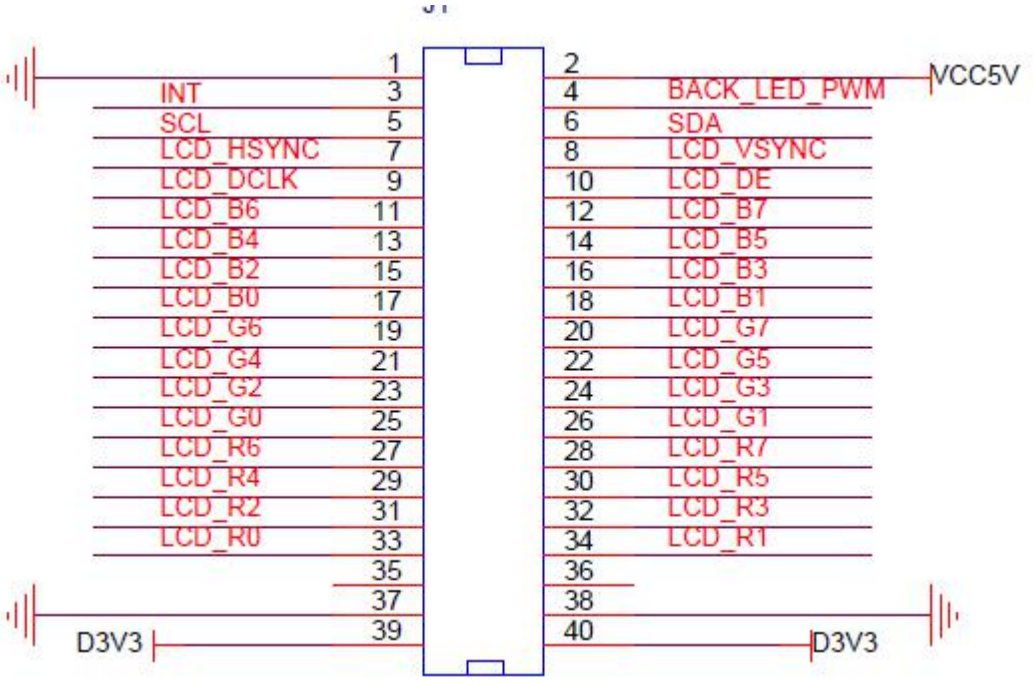

Figure 2-3: The connector on the PCB

Pin Name	Pin of P4	Description	Pin Name	Pin of P4	Description
GND	Pin1	Reference Ground	VCC5V	Pin2	5V Power Input
INIT	Pin3	Screen interrupt	BACK_LED_PWM	Pin4	Back light PWM Control
SCL	Pin5	Screen I2C Clock	SDA	Pin6	Touch I2C Data
LCD_HSYNC	Pin7	Horizontal Synchronize	LCD_VSYNC	Pin8	Vertical Synchronize
LCD_DCLK	Pin9	Pixel Clock	LCD_DE	Pin10	Date Enable
LCD_B6	Pin11	Bit 6 of blue data	LCD_B7	Pin12	Bit 7 of blue data
LCD_B4	Pin13	Bit 4 of blue data	LCD_B5	Pin14	Bit 5 of blue data
LCD_B2	Pin15	Bit 2 of blue data	LCD_B3	Pin16	Bit 3 of blue data
LCD_B0	Pin17	Bit 0 of blue data	LCD_B1	Pin18	Bit 1 of blue data
LCD_G6	Pin19	Bit6 of green data	LCD_G7	Pin20	Bit 7 of green data
LCD_G4	Pin21	Bit4 of green data	LCD_G5	Pin22	Bit 5 of green data
LCD_G2	Pin23	Bit2 of green data	LCD_G3	Pin24	Bit 3 of green data
LCD_G0	Pin25	Bit0 of green data	LCD_G1	Pin26	Bit 1 of green data
LCD_R6	Pin27	Bit 6 of red data	LCD_R7	Pin28	Bit 7 of red data
LCD_R4	Pin29	Bit 4 of red data	LCD_R5	Pin30	Bit 5 of red data
LCD_R2	Pin31	Bit 2 of red data	LCD_R3	Pin32	Bit 3 of red data
LCD_R0	Pin33	Bit 0 of red data	LCD_R1	Pin34	Bit 1 of red data
LCD_SDA	Pin35	LCD screen I2C data	LCD_SCL	Pin36	LCD screen I2C clock
GND	Pin37	Reference Ground	GND	Pin38	Reference Ground
D3V3	Pin39	3.3V(Reserved）	D3V3	Pin40	3.3V(Reserved）

Table 2-1: Signal Definition of the 40-pin female header

Part 3: 7”LCD Screen Display Experiment

The experiment takes the AX301B FPGA development board as an example. After the 7”LCD touch screen module and the AX301B FPGA development board are connected, use the Quartus 17.1 software to open the example project of the lcd_test we provide.

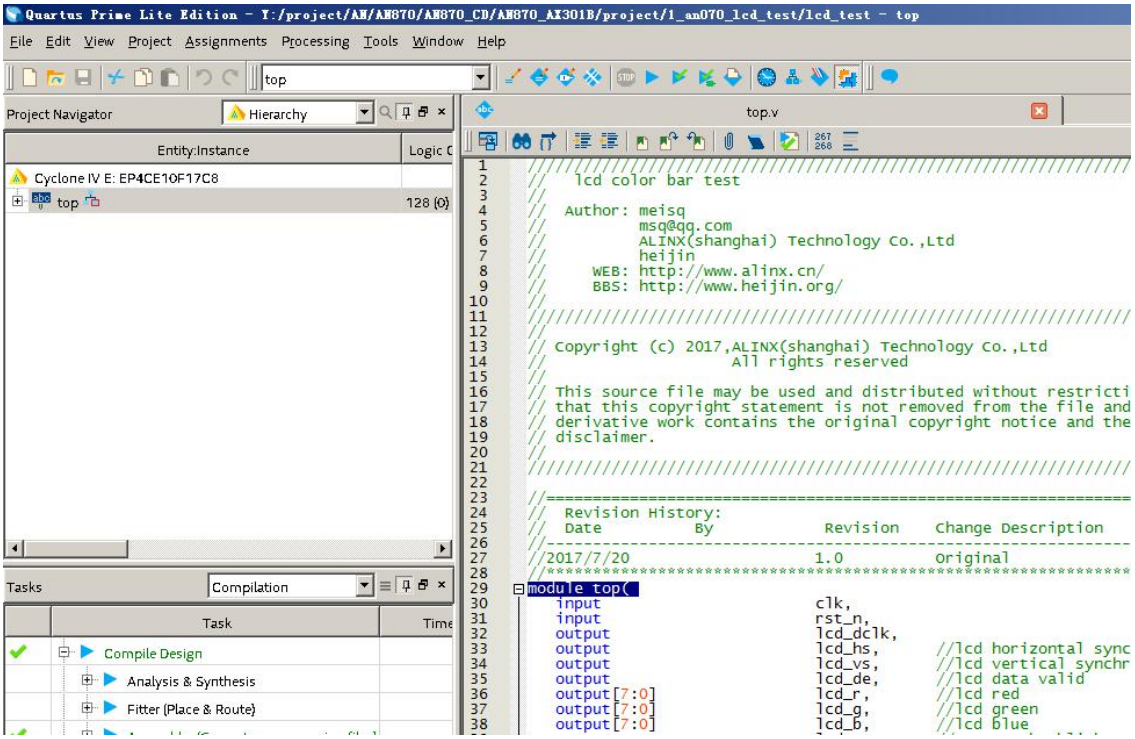

Figure 3-1: Example Project of the lcd_test we provide

Download the lcd_test.sof file to the development board and you will see the LCD screen displaying the color bar image.

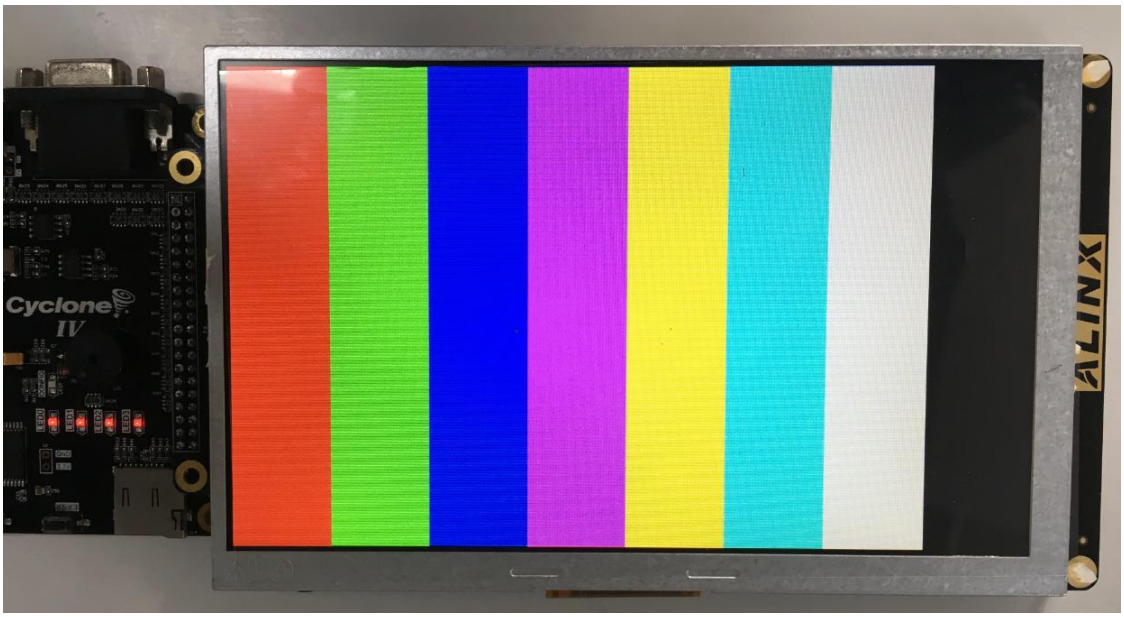

Figure 3-2: LCD Display Color Bar Image

Part 4: 50,000 pixel Camera LCD Display Experiment

This experiment demonstrates the video image of OV5640 on the 7-inch LCD screen with ALINX 7-inch LCD touch screen module. In the experiment, the AX301B development board is taken as an example, and the 8000*480 pixel video image of the OV5640 is output to the LCD for display.

Insert the OV5640 camera module into the Camera interface of the FPGA development board, and then connect the FPGA development board and the 7-inch LCD display module. Figure 4-1 detailed the connection of the AX301B development board.

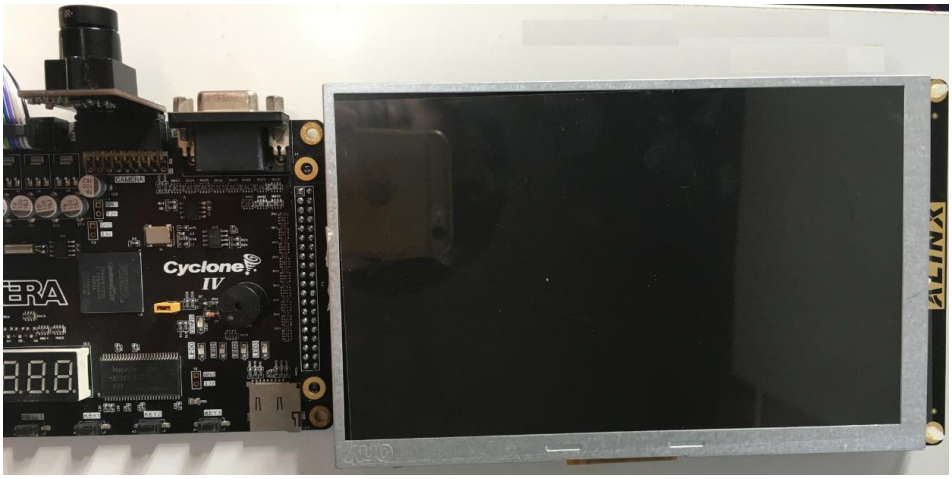

Figure 4-1: AX301B Camera LCD Display Experiment

Open the test project **sdram_ov5640_vga.qpf** in the directory of **sdram_ov7670_rgb_lcd_800480** provided by Quartus software.

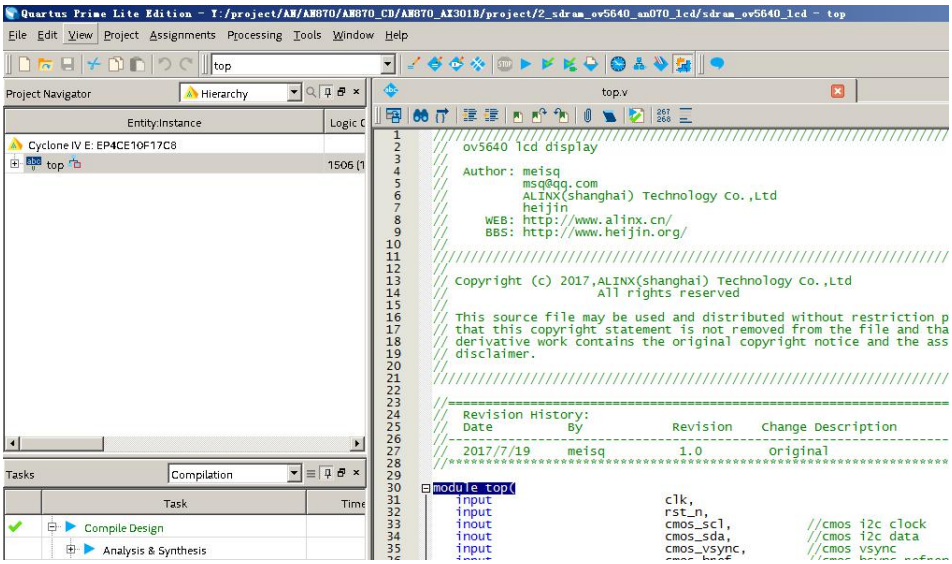

Figure 4-2: A test project sdram_ov5640_vga.qpf

Download the **sdram_ov5640_vga.sof** file to the FPGA development board, we can see the video image of the ov5640 camera on the LCD screen. Detail as Figure 4-3.

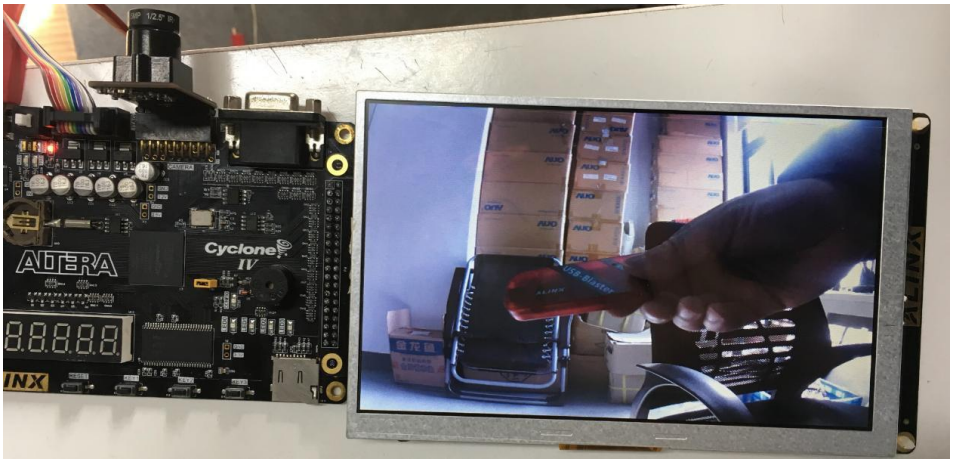

Figure 4-3: OV5640 video image LCD display effect