ALINX

AXAU25 Development Board

User Manual

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AMD Adaptive Computing Partner PREMIER

Document changes history

Chapters and sections	Review Summary
2025-11-17 V1.0	
whole	First release

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The ALINX ARTIX UltraScale+ series high-end FPGA development platform (model: AXAU25) has been officially launched. To help you quickly understand this development platform, we have prepared this user manual.

The ARTIX UltraScale+ development platform adopts a core board with expansion boards design, enabling users to repurpose the core board for secondary development. The baseboard features dual 40-pin expansion interfaces, FMC module interfaces, one Ethernet port, and PCIe3.0X4 interfaces to meet high-speed data transmission and switching requirements, making it a "professional-grade" and "all-in-one" development platform for data communication. This product is particularly suitable for students and engineers specializing in data communication and video/image processing. The development board is shown in the figure below.

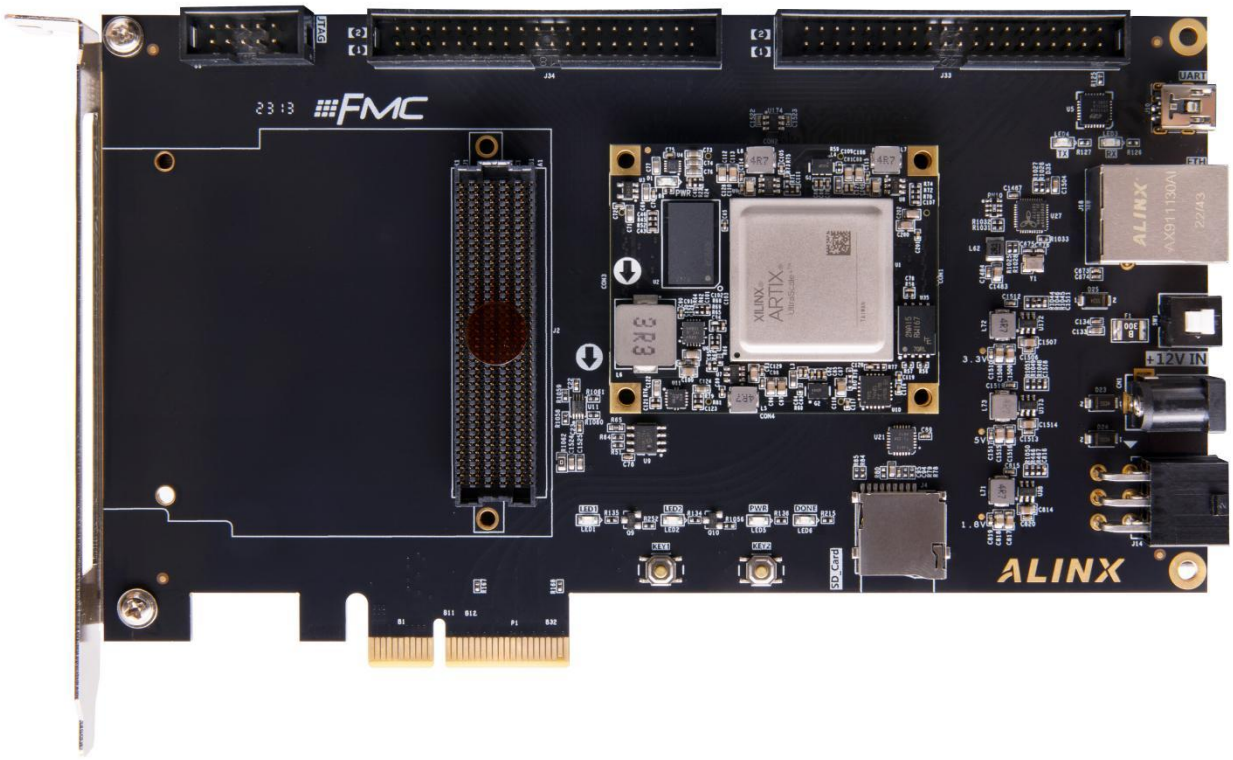

Figure 1.1.1-AXAU25 development board

01 Introduction to the Development Board

Here, we provide a brief overview of the AXAU25 FPGA development platform.

The development board's entire structure follows our established core board plus expansion board design model. The core board and expansion board are connected via a high-speed board-to-board connector.

The core board is primarily composed of an FPGA, a DDR4 memory module, and QSPI FLASH, which handles high-speed data processing and storage. The 16-bit data width enables efficient data transfer between the FPGA and DDR4, while the 8GB DDR4 capacity provides ample buffer space for data operations. The system utilizes Xilinx's ARTIX UltraScale+ series XCAU25P FPGA in FFVB676 package. With a clock frequency of 1200MHz and 2400Mbps data rate, the FPGA achieves optimal performance for high-speed multi-channel data processing. Additionally, the XCAU25P features 12-channel GTY transceivers with 16.3Gb/s speeds, making it ideal for fiber optic and PCIe data communication. The diagram below illustrates the architecture of the entire development system:

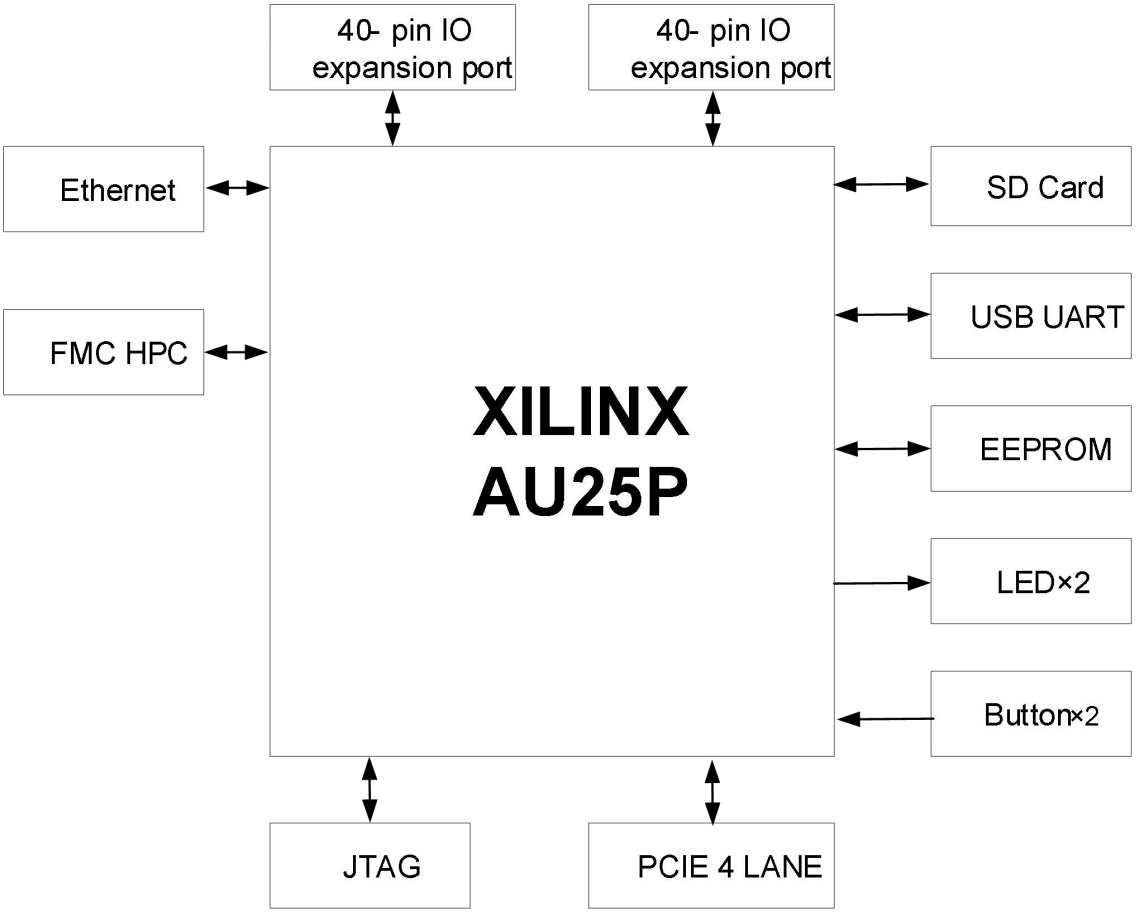

Figure 1.1.2-Schematic diagram of the development system structure

With this diagram, we can see what our development platform can do.

- The ARTIX UltraScale+ core board features an XCAU25P processor with 8Gb DDR4 memory

and 256Mb QSPI FLASH, complemented by two high-precision LVDS differential crystal oscillators from Sitime (200MHz and 156.25MHz) to ensure stable clock signals for both the FPGA system and GTY module.

- 10/100M/1000M Ethernet RJ-45 interface: The Gigabit Ethernet interface chip utilizes Jingluo's JL2121 Ethernet PHY chip to provide network communication services. The JL2121 chip supports 10/100/1000 Mbps network transmission rates, full-duplex operation, and adaptive capabilities.
- A USB UART debugging interface: A USB-UART converter for computer communication, facilitating debugging. The serial port uses Silicon Labs' CP2102GM USB-UART chip, with a MINI USB port.
- PCIe x4 interface: Supports the PCI Express 3.0 standard, providing a standard PCIe x4 high-speed data transfer interface
- Micro SD card slot: 1 Micro SD card slot for storing the operating system image and file system
- 40-pin expansion ports: Two 40-pin ports with 2.54mm spacing are reserved for external connections of ALINX modules (binocular camera, TFT LCD screen, high-speed AD module, etc.). The ports include 15V power supply, 23.3V power supplies, 3 ground lines, and 34 I/O ports.
- JTAG port: A 10-pin 2.54mm standard JTAG port for FPGA programming and debugging
- Keys: 2 user keys
- LED lights: 5 LEDs (1 on the core board, 4 on the expansion board)

02 FPGA Core Board

2.1 Introduction

The ACAU25 (core board model, hereinafter the same) is a core board based on Xilinx's ARTIX UltraScale+ series, specifically the XCAU25P variant.

The-2FFVB676I high-performance core board, developed with this chip, features high speed, high bandwidth, and high capacity, making it ideal for high-speed data communication, video image processing, and high-speed data acquisition.

The motherboard features a single 16MB MICRON MT40A512M16LY-062EIT DDR4 chip with 16-bit data bus bandwidth and 8GB capacity, supporting DDR4 SDRAM up to 1200MHz (2400Mbps data rate). It also integrates a 256MB QSPI FLASH for boot configuration and system files.

This core board features 72 standard 3.3V I/O ports, 102 standard 1.8V I/O ports, and 12 pairs of GTY high-speed RX/TX differential signals. It makes an excellent choice for users requiring extensive I/O capabilities. The PCB traces between the FPGA chip and interface are designed with equal-length and differential routing, while its compact 45×55 mm footprint provides optimal space for secondary development.

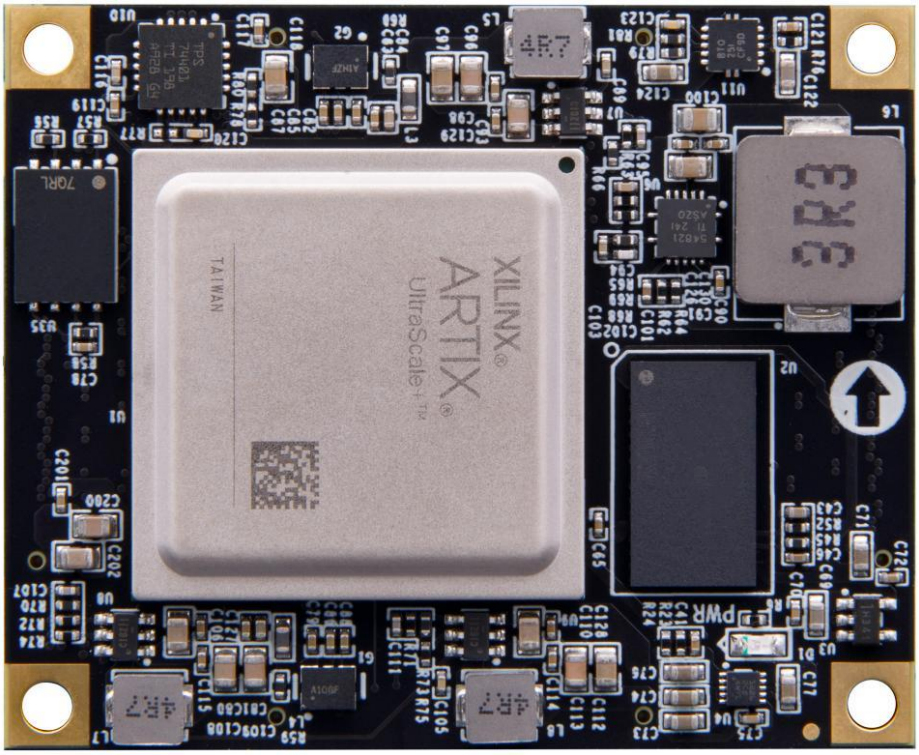

Figure 2.1.1-ACAU25 Front view of the core board

2.2 FPGA

As previously mentioned, the FPGA model we are using is the XCAU25P-2FFVB676I, part of Xilinx's ARTIX UltraScale+ series, with a speed class 2 and industrial-grade temperature rating. This model features a FFVB676 package with 676 pins. The naming convention for ARTIX UltraScale+ FPGA chips is as follows:

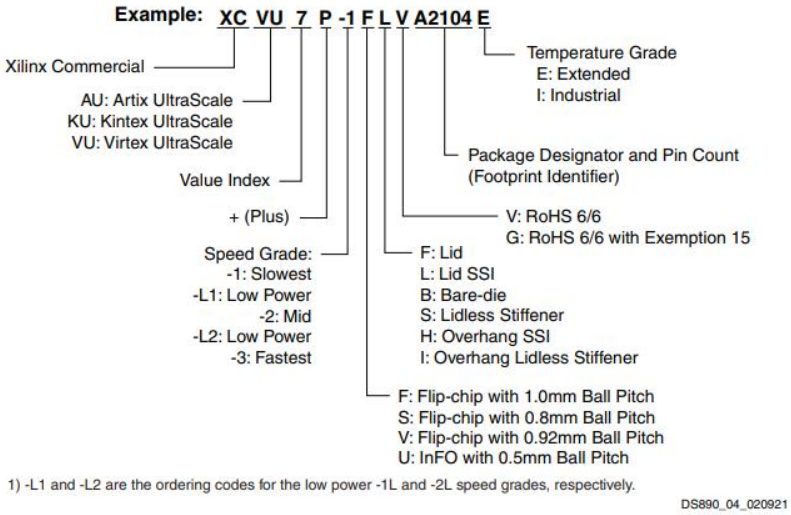

Figure 2.2.1-Chip Naming Rules

The key specifications of the FPGA chip XCAU25P are as follows:

Name	Specific parameters
Logic Cells	308437
Look up tables (CLB LUTs)	141000
Trigger (CLB flip-flop)	282000
Block RAM (kb) size	10500
DSP Processing Unit (DSP Slices)	1200
Clock Management Units (CMTs)	4
GTY 16.3Gb/s Transceiver	12
Speed level	-2
temperature grade	technical grade

Table 2.2.1-XCAU25P Main Parameters

2.3 Active Differential Crystal Oscillator

The ACAU25 core board features two active differential crystal oscillators from Sitime. The 200MHz oscillator (model SiT9121AI-2B1-33E200.000000) serves as the FPGA's system master clock and DDR4 control clock, while the 156.25MHz oscillator (model SiT9121AI-2B1-33E156.250000) provides reference clock input for the GTY transceiver.

200 MHz differential clock

The G1 in Figure 2.3.1 refers to the 200MHz active differential crystal oscillator circuit mentioned earlier, which serves as the system clock source for the development board. The oscillator output is connected to the FPGA's BANK65 global clock pin MRCC (T24 and U24). This 200MHz differential clock powers the FPGA's user logic circuits. Users can generate clocks at different frequencies by configuring the FPGA's internal PLLs and DCMs.

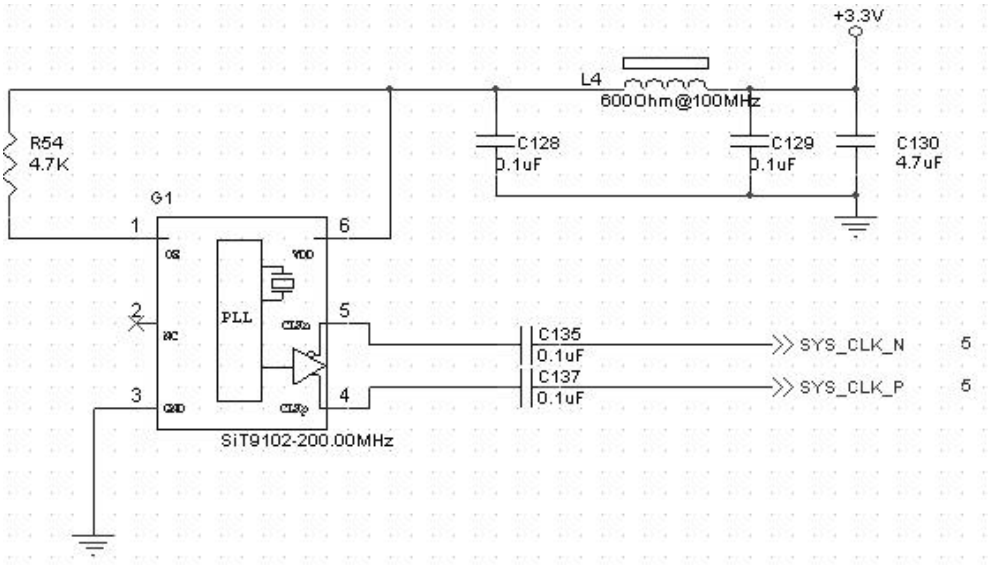

Figure 2.3.1-200MHz Schematic diagram of active differential crystal oscillator

Pin name	FPGA pin
SYS_CLK_P	T24
SYS_CLK_N	U24

Table 2.3.1-Clock Pin Assignment

156.25Mhz Differential clock

In Figure 2.3.2, G2 represents the 156.25M active differential crystal oscillator circuit, which provides the reference clock input to the FPGA's GTY module. The oscillator's output is connected to the FPGA GTY's BANK225 clock pins MGTREFCLK1P_225 (T7) and MGTREFCLK1N_225 (T6).

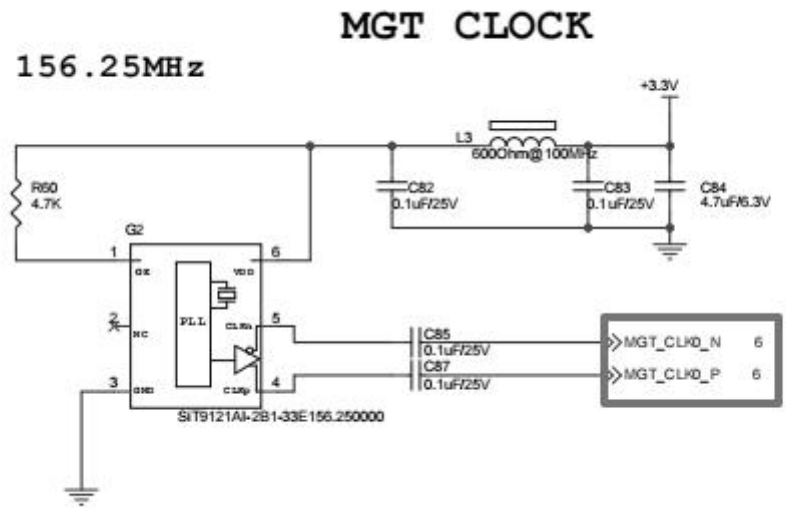

Figure 2.3.2-156.25Mhz Schematic diagram of active differential crystal oscillator

Clock pin assignment:

Pin name	FPGA pin
MGT_CLK0_P	T7
MGT_CLK0_N	T6

Table 2.3.2-1 Clock Pin Assignment

2.4 DDR4

The ACAU25 core board features a 8Gbit Micron DDR4 chip (model MT40A512M16LY-062EIT) with a 16-bit bus width. The DDR4 SDRAM supports up to 1200MHz operating frequency (2400Mbps data rate) and is directly connected to the FPGA's BANK 66 memory interface. The specific configuration of the DDR4 SDRAM is detailed in the table below.

item	Chip type	capacity	vender
U2	MT40A512M16LY-062EIT	512M x 16bit	micron

Table 2.4.1-DDR4 SDRAM Configuration

The hardware design of DDR4 requires strict consideration of signal integrity. During circuit and PCB design, we have fully considered matching resistors/termination resistors, controlled trace impedance, and maintained equal trace lengths to ensure DDR4's high-speed and stable operation. The hardware connection method between FPGA and DDR4 DRAM is shown in the figure.

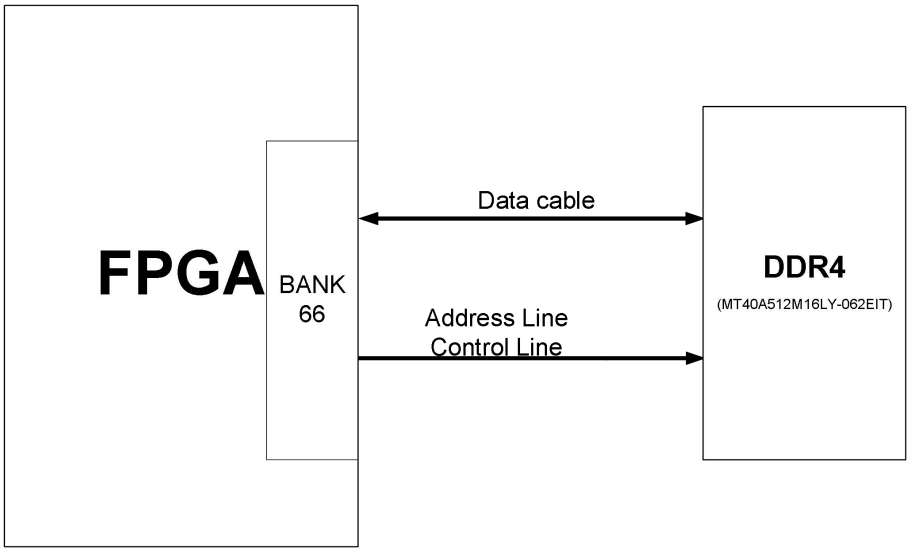

Figure 2.4.1-DDR4 DRAM schematic diagram section

DDR4 DRAM pin assignment:

Signal Name	FPGA pin name	FPGA pin number
PL_DDR4_A0	IO_L13N_T2L_N1_GC_QBC_66	G25
PL_DDR4_A1	IO_L8N_T1L_N3_AD5N_66	M26
PL_DDR4_A2	IO_L10N_T1U_N7_QBC_AD4N_66	L25
PL_DDR4_A3	IO_L19N_T3L_N1_DBC_AD9N_66	E26
PL_DDR4_A4	IO_L8P_T1L_N2_AD5P_66	M25
PL_DDR4_A5	IO_T3U_N12_66	F22
PL_DDR4_A6	IO_L17P_T2U_N8_AD10P_66	H26
PL_DDR4_A7	IO_L16P_T2U_N6_QBC_AD3P_66	F24
PL_DDR4_A8	IO_L17N_T2U_N9_AD10N_66	G26
PL_DDR4_A9	IO_L12P_T1U_N10_GC_66	J23
PL_DDR4_A10	IO_L15P_T2L_N4_AD11P_66	J25
PL_DDR4_A11	IO_L12N_T1U_N11_GC_66	J24
PL_DDR4_A12	IO_L16N_T2U_N7_QBC_AD3N_66	F25

PL_DDR4_A13	IO_L14N_T2L_N3_GC_66	H24
PL_DDR4_ACT_B	IO_L9P_T1L_N4_AD12P_66	K25
PL_DDR4_BA0	IO_L15N_T2L_N5_AD11N_66	J26
PL_DDR4_BA1	IO_T2U_N12_66	G22
PL_DDR4_BG0	IO_L7P_T1L_N0_QBC_AD13P_66	L22
PL_DDR4_CAS_B	IO_L18N_T2U_N11_AD2N_66	H22
PL_DDR4_CKE	IO_L7N_T1L_N1_QBC_AD13N_66	L23
PL_DDR4_CLK_N	IO_L11N_T1U_N9_GC_66	K23
PL_DDR4_CLK_P	IO_L11P_T1U_N8_GC_66	K22
PL_DDR4_CS_B	IO_L14P_T2L_N2_GC_66	H23
PL_DDR4_PAR	IO_L10P_T1U_N6_QBC_AD4P_66	L24
PL_DDR4_RAS_B	IO_L18P_T2U_N10_AD2P_66	H21
PL_DDR4_OTD	IO_T1U_N12_66	M24
PL_DDR4_WE_B	IO_L9N_T1L_N5_AD12N_66	K26
PL_DDR4_DM0	IO_L19P_T3L_N0_DBC_AD9P_66	E25
PL_DDR4_DM1	IO_L1P_T0L_N0_DBC_66	L18
PL_DDR4_DQ0	IO_L20P_T3L_N2_AD1P_66	F23
PL_DDR4_DQ1	IO_L21N_T3L_N5_AD8N_66	D25
PL_DDR4_DQ2	IO_L20N_T3L_N3_AD1N_66	E23
PL_DDR4_DQ3	IO_L24N_T3U_N11_66	B26
PL_DDR4_DQ4	IO_L21P_T3L_N4_AD8P_66	D24
PL_DDR4_DQ5	IO_L23P_T3U_N8_66	D26
PL_DDR4_DQ6	IO_L24P_T3U_N10_66	B25

PL_DDR4_DQ7	IO_L23N_T3U_N9_66	C26
PL_DDR4_DQ8	IO_L2P_T0L_N2_66	M20
PL_DDR4_DQ9	IO_L3N_T0L_N5_AD15N_66	J20
PL_DDR4_DQ10	IO_L3P_T0L_N4_AD15P_66	J19
PL_DDR4_DQ11	IO_L2N_T0L_N3_66	M21
PL_DDR4_DQ12	IO_L6P_T0U_N10_AD6P_66	L20
PL_DDR4_DQ13	IO_L5N_T0U_N9_AD14N_66	J21
PL_DDR4_DQ14	IO_L6N_T0U_N11_AD6N_66	K20
PL_DDR4_DQ15	IO_L5P_T0U_N8_AD14P_66	K21
PL_DDR4_DQS0_N	IO_L22N_T3U_N7_DBC_AD0N_66	C24
PL_DDR4_DQS0_P	IO_L22P_T3U_N6_DBC_AD0P_66	D23
PL_DDR4_DQS1_N	IO_L4N_T0U_N7_DBC_AD7N_66	L19
PL_DDR4_DQS1_P	IO_L4P_T0U_N6_DBC_AD7P_66	M19
PL_DDR4_RST	IO_L13P_T2L_N0_GC_QBC_66	G24

Table2.4.2-DDR4 DRAM Pin Assignment

2.5 QSPI Flash

The core board incorporates a 256Mbit QSPI FLASH chip (model MT25QU256ABA1EW9-0SIT) operating at 1.8V CMOS voltage. Its non-volatile nature enables this flash memory to serve as the boot image for FPGA systems during operation. The boot image primarily contains FPGA bit files, application code for the softcore, and other user data files. The specific model and parameters of the SPI FLASH are detailed in the table below.

Item	Chip type	Capacity	Vender
U35	MT25QU256ABA1EW9-0SIT	256M Bit	Micron

Table2.5.1-QSPI Flash Model and Specifications

The QSPI Flash is connected to the dedicated pin of BANK0 on the FPGA chip, with the clock pin linked to BANK0's CCLK0. Other data and chip select signals are connected to BANK0's

D00-D03 and FCS pins respectively. Figure 2.5.1 shows the schematic diagram of the QSPI Flash and FPGA chip connections.

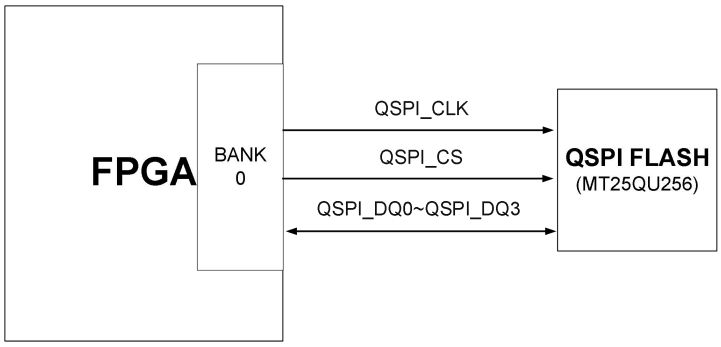

Figure 2.5.1-QSPI Flash connection diagram

Configure chip pin assignments:

Signal Name	FPGA pin name	FPGA pin number
QSPI_CLK	CCLK_0	Y11
QSPI_CS	RDWR_FCS_B_0	AA12
QSPI_DQ0	D00_MOSI_0	AD11
QSPI_DQ1	D01_DIN_0	AC12
QSPI_DQ2	D02_0	AC11
QSPI_DQ3	D03_0	AE11

Table 2.5.2-QSPI Pin Assignment

2.6 LED light

The ACAU25 core board features a red LED (Power Indicator, PWR) that activates upon power supply. The schematic diagram of the LED's hardware connection is shown in the figure.

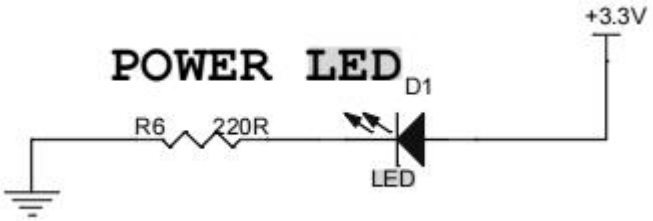

Figure 2.6.1-Schematic diagram of LED light hardware connection for development board

2.7 Power Supply

The ACAU25 core board operates within a +5V to +17V voltage range (typically +12V), powered by a connected baseboard. The TPS54821RHL DCDC chip supplies 0.85V core power to the XCAU25P, while the BANK64, BANK65, and BANK66 banks utilize the ETA1471 DCDC chip. Users can adjust the IO voltage to 1.2V by modifying resistors (note: these banks must not exceed 1.8V). BANK84, BANK85, and BANK86 maintain 3.3V IO levels. The GTY transceiver is powered by an LDO chip.

The Artix UltraScale+ FPGA's power supply requires a specific boot sequence. Our circuit design follows the chip's power specifications, with the power-up sequence being: VCCINT(1.0V)->VCCBRAM(1.0V) → (1.5 V, 3.3V, VCCIO) and 1.0V → MGTAVCC → MGTAVTT, ensuring stable operation. The diagram below illustrates the power connection configuration.

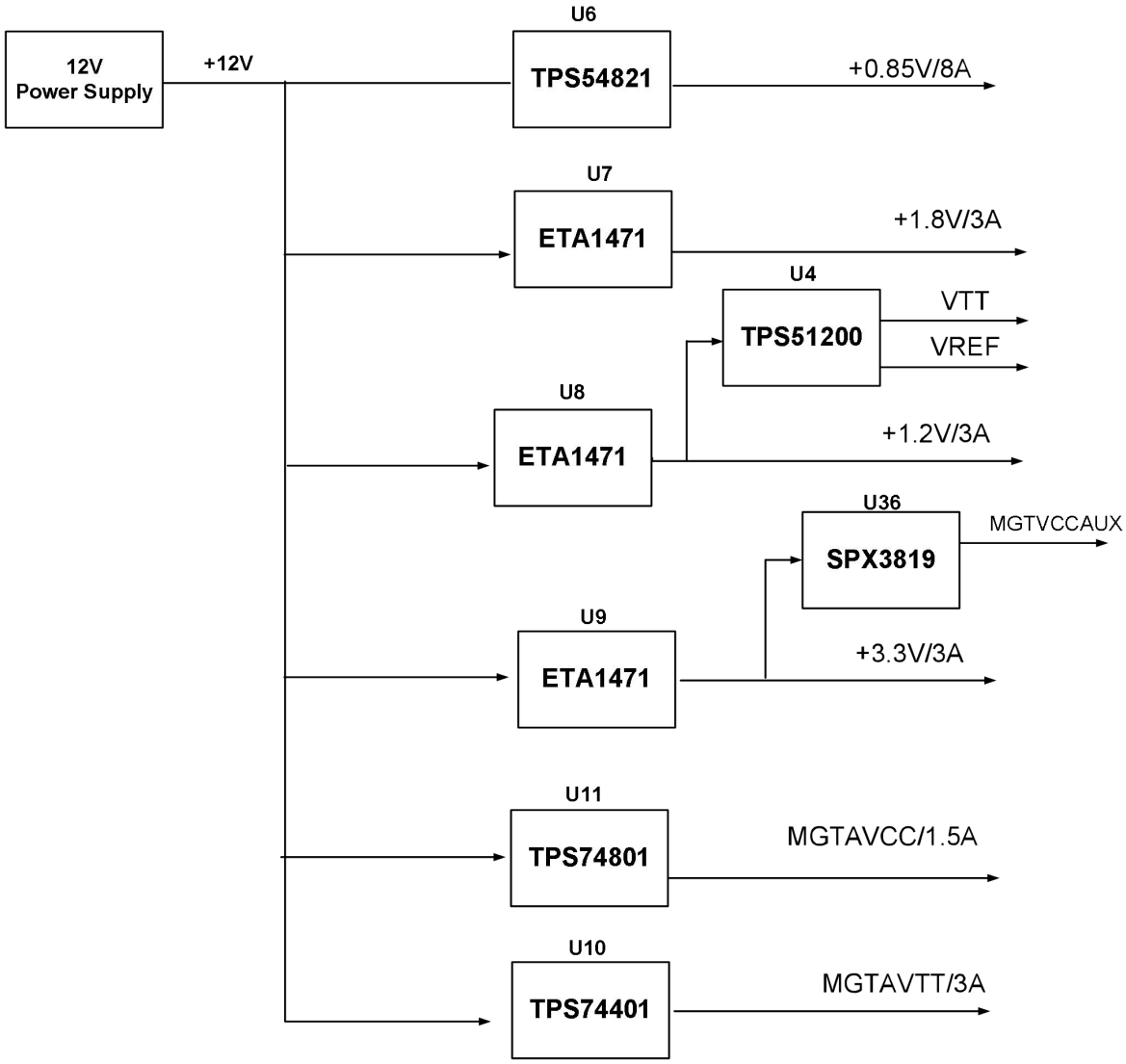

Figure 2.7.1-Power connection diagram

2.8 Extended Interface

The back of the core board features four high-speed expansion ports, connected to the base plate via four 80-pin inter-board connectors. The FPGA's I/O ports are linked to these ports through differential traces. With a 0.5mm pin pitch, the connectors' configuration enables high-speed data transfer with the base plate's female connectors.

Expansion port CON1

The 80-pin connector CON1 connects the baseboard's VCCIN power supply (+12V), ground, and FPGA's standard I/O. Notably, 52 pins of CON1 are linked to BANK64's I/O ports, all operating at 1.8V. The pin configuration for CON1's expansion port is detailed in Table 2.10.1.

CON1 Pin	Signal Name	Pin number	Level standard	CON1 Pin	Signal Name	Pin number	Level standard
PIN1	VCCIN	-	12V	PIN2	VCCIN	-	12V
PIN3	VCCIN	-	12V	PIN4	VCCIN	-	12V
PIN5	VCCIN	-	12V	PIN6	VCCIN	-	12V
PIN7	VCCIN	-	12V	PIN8	VCCIN	-	12V
PIN9	GND	-	the earth	PIN10	GND	-	the earth
PIN11	B64_T0U	AF23	1.8V	PIN12	B64_L4_N	AD26	1.8V
PIN13	B64_T1U	AF20	1.8V	PIN14	B64_L4_P	AC26	1.8V
PIN15	B64_T2U	AE18	1.8V	PIN16	B64_L2_N	AB26	1.8V
PIN17	B64_T3U	AC16	1.8V	PIN18	B64_L2_P	AB25	1.8V
PIN19	GND	-	the earth	PIN20	GND	-	the earth
PIN21	B64_L10_N	AB22	1.8V	PIN22	B64_L1_N	AE26	1.8V
PIN23	B64_L10_P	AA22	1.8V	PIN24	B64_L1_P	AE25	1.8V
PIN25	B64_L8_N	AE23	1.8V	PIN26	B64_L3_N	AF25	1.8V
PIN27	B64_L8_P	AD23	1.8V	PIN28	B64_L3_P	AF24	1.8V
PIN29	GND	-	the earth	PIN30	GND	-	the earth

PIN31	B64_L7_N	AF22	1.8V	PIN32	B64_L6_N	AC24	1.8V
PIN33	B64_L7_P	AE22	1.8V	PIN34	B64_L6_P	AB24	1.8V
PIN35	B64_L9_N	AC23	1.8V	PIN36	B64_L5_N	AD25	1.8V
PIN37	B64_L9_P	AC22	1.8V	PIN38	B64_L5_P	AD24	1.8V
PIN39	GND	-	the earth	PIN40	GND	-	the earth
PIN41	B64_L12_N	AC21	1.8V	PIN42	B64_L11_N	AE21	1.8V
PIN43	B64_L12_P	AB21	1.8V	PIN44	B64_L11_P	AD21	1.8V
PIN45	B64_L14_N	AD19	1.8V	PIN46	B64_L13_N	AE20	1.8V
PIN47	B64_L14_P	AC19	1.8V	PIN48	B64_L13_P	AD20	1.8V
PIN49	GND	-	the earth	PIN50	GND	-	the earth
PIN51	B64_L19_N	Y21	1.8V	PIN52	B64_L21_N	AB20	1.8V
PIN53	B64_L19_P	Y20	1.8V	PIN54	B64_L21_P	AA20	1.8V
PIN55	B64_L20_N	AB19	1.8V	PIN56	B64_L24_N	AA18	1.8V
PIN57	B64_L20_P	AA19	1.8V	PIN58	B64_L24_P	Y18	1.8V
PIN59	GND	-	the earth	PIN60	GND	-	the earth
PIN61	B64_L23_N	AA17	1.8V	PIN62	B64_L15_N	AF19	1.8V
PIN63	B64_L23_P	Y17	1.8V	PIN64	B64_L15_P	AF18	1.8V
PIN65	B64_L18_N	AE16	1.8V	PIN66	B64_L17_N	AF17	1.8V
PIN67	B64_L18_P	AD16	1.8V	PIN68	B64_L17_P	AE17	1.8V
PIN69	GND	-	the earth	PIN70	GND	-	the earth
PIN71	FPGA_DONE	AB11	1.8V	PIN72	B64_L16_N	AD18	1.8V
PIN73	PROGRAM_B	AB9	1.8V	PIN74	B64_L16_P	AC18	1.8V
PIN75	INIT_B	W10	1.8V	PIN76	B64_L22_N	AC17	1.8V

PIN77	NC	-	No feet	PIN78	B64_L22_P	AB17	1.8V
PIN79	NC	-	No feet	PIN80	NC	-	No feet

Table 2.10.1 Expansion Port CON1 Pin Assignment

Expand port CON2

The 80-pin connector CON2 is designed to expand the I/O capabilities of FPGA's BANK65 and BANK84, as well as provide 4-channel JTAG signals. BANK84 operates at 3.3V, while BANK65 runs at 1.8V. The pin configuration of CON2's expansion port is detailed in Table 2.10.2.

CON2 Pin	Signal name	Pin number	Level standard	CON2 Pin	signal name	Pin number	Level standard
PIN1	B65_L22_N	P23	1.8V	PIN2	B65_T2U	N26	1.8V
PIN3	B65_L22_P	N23	1.8V	PIN4	B65_T1U	AA23	1.8V
PIN5	B65_L18_N	R26	1.8V	PIN6	B65_T0U	W21	1.8V
PIN7	B65_L18_P	R25	1.8V	PIN8	B65_T3U	T19	1.8V
PIN9	GND	-	the earth	PIN10	GND	-	the earth
PIN11	B65_L14_N	U25	1.8V	PIN12	B65_L24_N	N22	1.8V
PIN13	B65_L14_P	T25	1.8V	PIN14	B65_L24_P	N21	1.8V
PIN15	B65_L17_N	P26	1.8V	PIN16	B65_L15_N	P24	1.8V
PIN17	B65_L17_P	P25	1.8V	PIN18	B65_L15_P	N24	1.8V
PIN19	GND	-	the earth	PIN20	GND	-	the earth
PIN21	B65_L16_N	V26	1.8V	PIN22	B65_L19_N	R23	1.8V
PIN23	B65_L16_P	U26	1.8V	PIN24	B65_L19_P	R22	1.8V
PIN25	B65_L10_N	W26	1.8V	PIN26	B65_L5_N	T23	1.8V
PIN27	B65_L10_P	W25	1.8V	PIN28	B65_L5_P	T22	1.8V
PIN29	GND	-	the earth	PIN30	GND	-	the earth
PIN31	B65_L11_N	W23	1.8V	PIN32	B65_L12_N	W24	1.8V

PIN33	B65_L11_P	V23	1.8V	PIN34	B65_L12_P	V24	1.8V
PIN35	B65_L2_N	U22	1.8V	PIN36	B65_L8_N	Y26	1.8V
PIN37	B65_L2_P	U21	1.8V	PIN38	B65_L8_P	Y25	1.8V
PIN39	GND	-	the earth	PIN40	GND	-	the earth
PIN41	B65_L23_N	P19	1.8V	PIN42	B65_L21_N	R21	1.8V
PIN43	B65_L23_P	N19	1.8V	PIN44	B65_L21_P	R20	1.8V
PIN45	B65_L3_N	U20	1.8V	PIN46	B65_L4_N	V22	1.8V
PIN47	B65_L3_P	T20	1.8V	PIN48	B65_L4_P	V21	1.8V
PIN49	GND	-	the earth	PIN50	GND	-	the earth
PIN51	B65_L20_N	P21	1.8V	PIN52	B65_L9_N	AA25	1.8V
PIN53	B65_L20_P	P20	1.8V	PIN54	B65_L9_P	AA24	1.8V
PIN55	B65_L6_N	W20	1.8V	PIN56	B65_L7_N	Y23	1.8V
PIN57	B65_L6_P	W19	1.8V	PIN58	B65_L7_P	Y22	1.8V
PIN59	GND	-	the earth	PIN60	GND	-	the earth
PIN61	B65_L1_N	V19	1.8V	PIN62	B84_L2_N	AF13	3.3V
PIN63	B65_L1_P	U19	1.8V	PIN64	B84_L2_P	AE13	3.3V
PIN65	B84_L6_N	AB16	3.3V	PIN66	B84_L1_N	AF15	3.3V
PIN67	B84_L6_P	AB15	3.3V	PIN68	B84_L1_P	AF14	3.3V
PIN69	GND	-	the earth	PIN70	GND	-	the earth
PIN71	FPGA_TCK	AE12	1.8V	PIN72	B84_L3_N	AE15	3.3V
PIN73	FPGA_TDI	AB12	1.8V	PIN74	B84_L3_P	AD15	3.3V
PIN75	FPGA_TMS	AB10	1.8V	PIN76	B84_L4_N	AD14	3.3V
PIN77	FPGA_TDO	Y10	1.8V	PIN78	B84_L4_P	AD13	3.3V

PIN79	NC	-	No feet	PIN80	NC	-	No feet

Table 2.10.2-Expansion Port CON2 Pin Assignment

CON3 Expansion Port

The 80Pin connector's CON3 pin is designed to expand the standard I/O of FPGA's BANK84, BANK85, and BANK86. These banks all operate at 3.3V. The pin configuration for the CON3 expansion port is detailed in Table 2.10.3.

CON3 Pin	Signal Name	Pin number	Level standard	CON3 pin	Signal Name	Pin number	Level standard
PIN1	B84_L8_N	AB14	3.3V	PIN2	B84_L5_N	AC14	3.3V
PIN3	B84_L8_P	AA14	3.3V	PIN4	B84_L5_P	AC13	3.3V
PIN5	B84_L12_N	W13	3.3V	PIN6	B84_L11_N	AA13	3.3V
PIN7	B84_L12_P	W12	3.3V	PIN8	B84_L11_P	Y13	3.3V
PIN9	GND	-	the earth	PIN10	GND	-	the earth
PIN11	B84_L7_N	AA15	3.3V	PIN12	B84_L9_N	Y16	3.3V
PIN13	B84_L7_P	Y15	3.3V	PIN14	B84_L9_P	W16	3.3V
PIN15	B84_L10_N	W15	3.3V	PIN16	NC		No feet
PIN17	B84_L10_P	W14	3.3V	PIN18	NC		No feet
PIN19	GND	-	the earth	PIN20	GND	-	the earth
PIN21	B85_L1_N	K9	3.3V	PIN22	B85_L3_N	H9	3.3V
PIN23	B85_L1_P	K10	3.3V	PIN24	B85_L3_P	J9	3.3V
PIN25	B85_L2_N	J10	3.3V	PIN26	B85_L6_N	F9	3.3V
PIN27	B85_L2_P	J11	3.3V	PIN28	B85_L6_P	F10	3.3V
PIN29	GND	-	the earth	PIN30	GND	-	the earth
PIN31	B85_L4_N	G11	3.3V	PIN32	B85_L5_N	G9	3.3V
PIN33	B85_L4_P	H11	3.3V	PIN34	B85_L5_P	G10	3.3V

PIN35	B85_L11_N	A10	3.3V	PIN36	B85_L9_N	C9	3.3V
PIN37	B85_L11_P	B10	3.3V	PIN38	B85_L9_P	D9	3.3V
PIN39	GND	-	the earth	PIN40	GND	-	the earth
PIN41	B85_L8_N	D10	3.3V	PIN42	B85_L10_N	A9	3.3V
PIN43	B85_L8_P	D11	3.3V	PIN44	B85_L10_P	B9	3.3V
PIN45	B85_L7_N	E10	3.3V	PIN46	B85_L12_N	B11	3.3V
PIN47	B85_L7_P	E11	3.3V	PIN48	B85_L12_P	C11	3.3V
PIN49	GND	-	the earth	PIN50	GND	-	the earth
PIN51	B86_L2_N	H13	3.3V	PIN52	B86_L1_N	H12	3.3V
PIN53	B86_L2_P	J13	3.3V	PIN54	B86_L1_P	J12	3.3V
PIN55	B86_L4_N	J14	3.3V	PIN56	B86_L5_N	F12	3.3V
PIN57	B86_L4_P	J15	3.3V	PIN58	B86_L5_P	G12	3.3V
PIN59	GND	-	the earth	PIN60	GND	-	the earth
PIN61	B86_L9_N	C13	3.3V	PIN62	B86_L3_N	G14	3.3V
PIN63	B86_L9_P	C14	3.3V	PIN64	B86_L3_P	H14	3.3V
PIN65	B86_L8_N	D13	3.3V	PIN66	B86_L7_N	E12	3.3V
PIN67	B86_L8_P	D14	3.3V	PIN68	B86_L7_P	E13	3.3V
PIN69	GND	-	the earth	PIN70	GND	-	the earth
PIN71	B86_L11_N	A12	3.3V	PIN72	B86_L10_N	B12	3.3V
PIN73	B86_L11_P	A13	3.3V	PIN74	B86_L10_P	C12	3.3V
PIN75	B86_L6_N	F13	3.3V	PIN76	B86_L12_N	A14	3.3V
PIN77	B86_L6_P	F14	3.3V	PIN78	B86_L12_P	B14	3.3V
PIN79	NC	-	No feet	PIN80	NC	-	No feet

Table2.10.3-CON3 Pin Assignment

Expand port CON4

The 80Pin connector CON4 is designed to expand the transceiver interfaces of FPGA's BANK224, BANK225, and BANK226. The pin configuration of the CON4 expansion port is detailed in Table 2.10.4.

CON4 pin	Signal name	Pin number	Level standard	CON3 Pin	Signal name	Pin number	Level standard
PIN1	224_TX0_N	AF6	1.2V	PIN2	224_RX0_N	AF1	1.2V
PIN3	224_TX0_P	AF7	1.2V	PIN4	224_RX0_P	AF2	1.2V
PIN5	GND	-	the earth	PIN6	GND	-	the earth
PIN7	224_TX1_N	AE8	1.2V	PIN8	224_RX1_N	AE3	1.2V
PIN9	224_TX1_P	AE9	1.2V	PIN10	224_RX1_P	AE4	1.2V
PIN11	GND	-	the earth	PIN12	GND	-	the earth
PIN13	224_TX2_N	AD6	1.2V	PIN14	224_RX2_N	AD1	1.2V
PIN15	224_TX2_P	AD7	1.2V	PIN16	224_RX2_P	AD2	1.2V
PIN17	GND	-	the earth	PIN18	GND	-	the earth
PIN19	224_TX3_N	AC4	1.2V	PIN20	224_RX3_N	AB1	1.2V
PIN21	224_TX3_P	AC5	1.2V	PIN22	224_RX3_P	AB2	1.2V
PIN23	GND	-	the earth	PIN24	GND	-	the earth
PIN25	225_CLK0_N	V6	1.2V	PIN26	224_CLK0_N	AB6	1.2V
PIN27	225_CLK0_P	V7	1.2V	PIN28	224_CLK0_P	AB7	1.2V
PIN29	GND	-	the earth	PIN30	GND	-	the earth
PIN31	225_TX0_N	AA4	1.2V	PIN32	225_RX0_N	Y1	1.2V
PIN33	225_TX0_P	AA5	1.2V	PIN34	225_RX0_P	Y2	1.2V
PIN35	GND	-	the earth	PIN36	GND	-	the earth
PIN37	225_TX1_N	W4	1.2V	PIN38	225_RX1_N	V1	1.2V

PIN39	225_TX1_P	W5	1.2V	PIN40	225_RX1_P	V2	1.2V
PIN41	GND	-	the earth	PIN42	GND	-	the earth
PIN43	225_TX2_N	U4	1.2V	PIN44	225_RX2_N	T1	1.2V
PIN45	225_TX2_P	U5	1.2V	PIN46	225_RX2_P	T2	1.2V
PIN47	GND	-	the earth	PIN48	GND	-	the earth
PIN49	225_TX3_N	R4	1.2V	PIN50	225_RX3_N	P1	1.2V
PIN51	225_TX3_P	R5	1.2V	PIN52	225_RX3_P	P2	1.2V
PIN53	GND	-	the earth	PIN54	GND	-	the earth
PIN55	226_TX0_N	N4	1.2V	PIN56	226_RX0_N	M1	1.2V
PIN57	226_TX0_P	N5	1.2V	PIN58	226_RX0_P	M2	1.2V
PIN59	GND	-	the earth	PIN60	GND	-	the earth
PIN61	226_TX1_N	L4	1.2V	PIN62	226_RX1_N	K1	1.2V
PIN63	226_TX1_P	L5	1.2V	PIN64	226_RX1_P	K2	1.2V
PIN65	GND	-	the earth	PIN66	GND	-	the earth
PIN67	226_TX2_N	J4	1.2V	PIN68	226_RX2_N	H1	1.2V
PIN69	226_TX2_P	J5	1.2V	PIN70	226_RX2_P	H2	1.2V
PIN71	GND	-	the earth	PIN72	GND	-	the earth
PIN73	226_TX3_N	G4	1.2V	PIN74	226_RX3_N	F1	1.2V
PIN75	226_TX3_P	G5	1.2V	PIN76	226_RX3_P	F2	1.2V
PIN77	GND	-	the earth	PIN78	GND	-	the earth
PIN79	226_CLK0_P	P7	1.2V	PIN80	226_CLK0_N	P6	1.2V

Table 2.10.4-Expansion Port Pin Assignment for CON4

2.9 Structure Diagram

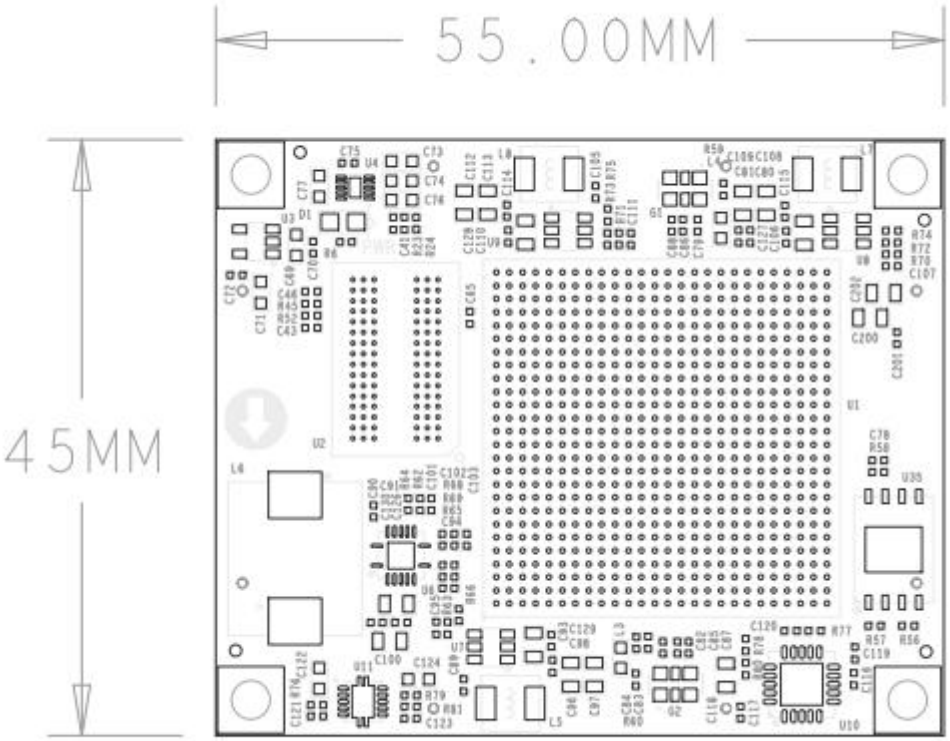

Figure 2.9.1-Core Board Structure Diagram (Top View)

03 Extension Plate

3.1 Introduction

Through the previous function introduction, we can understand the functions of the expansion board

- 1 Gigabit Ethernet RJ-45 port
- PCIe x4 interface
- 1 FMC expansion port
- 1 USB UART Debug Interface
- Micro SD card slot 1
- 1 EEPROM
- JTAG Debug Port
- 2-way 40-pin expansion port
- 2 independent buttons
- 2 user LED lights

3.2 Gigabit Ethernet interface

The AXAU25 development board provides network communication services through Jinglue Semiconductor's industrial-grade Ethernet GPHY chip (JL2121-N040I). The JL2121 chip supports 10/100/1000 Mbps network transmission rates and communicates with the FPGA's MAC layer via the RGMII interface. The JL2121D supports MDI/MDX auto-adaptation, various speed adaptation, and Master/Slave auto-adaptation, while managing PHY registers through the MDIO bus.

Upon power-on, the JL2121 detects specific IO voltage levels to determine its operational mode. Table 3.2.1 outlines the default configuration parameters of the GPHY chip after power-on.

Configure Pin	explain	Configuration
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY address for MDIO/MDC mode	PHY Address is 001
RXD1_TXDLY	TX clock with 2ns delay	delayed
RXD0_RXDLY	RX clock 2ns delay	delayed

Table 3.2.1-PHY chip default configuration values

When the network is connected to a Gigabit Ethernet, the FPGA and PHY chip JL2121 communicate via the RGMII bus. The transmission clock operates at 125MHz, with data sampled during both the rising and falling edges of the clock.

When the network connects to a 100 Mbps Ethernet, the FPGA and PHY chip JL2121 communicate via the RMII bus with a 25 MHz clock. Data is sampled during both the rising and falling edges of the clock. The schematic design of the Gigabit Ethernet is shown in Figure 3.2.1.

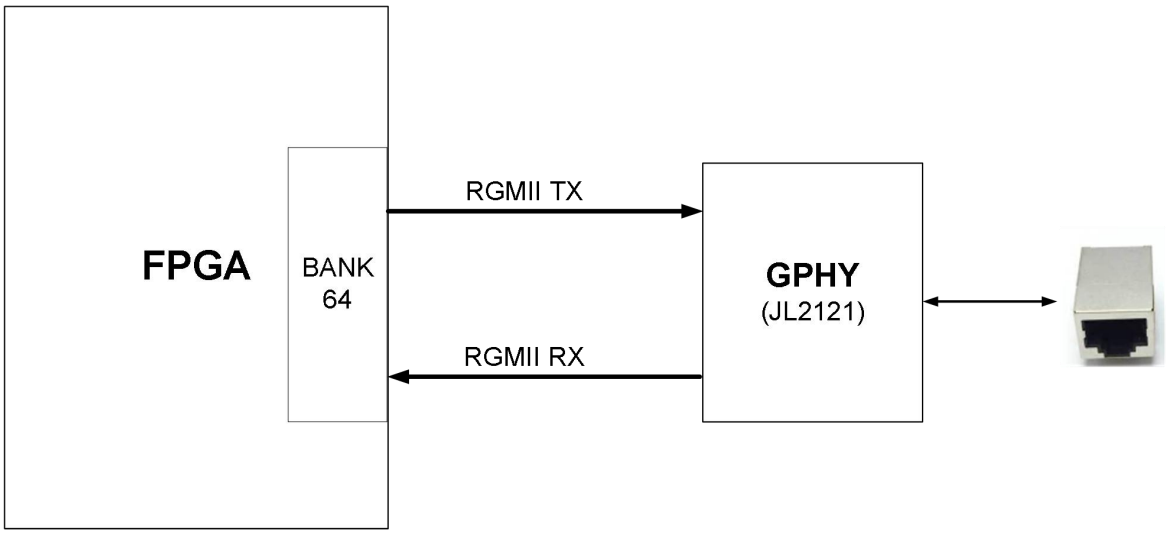

Figure 3.2.1-Schematic diagram of Gigabit Ethernet interface design

The Ethernet FPGA pin assignments are as follows:

Signal Name	FPGA pin name	FPGA pin number	Remarks
PHY_RESET	B64_T0U	AF23	Reset the PHY chip
PHY_MDC	B64_T1U	AF20	MDIO Management Clock
PHY_MDIO	B64_T2U	AE18	MDIO management data
PHY_RXC	B64_L11_P	AD21	RGMII receive clock
PHY_RXDV	B64_L11_N	AE21	Receive valid data signal
PHY_RXD0	B64_L9_P	AC22	Receive data Bit0
PHY_RXD1	B64_L9_N	AC23	Receive data Bit1
PHY_RXD2	B64_L8_P	AD23	Receive data Bit2

PHY_RXD3	B64_L8_N	AE23	Receive data Bit3
PHY_GTXC	B64_L18_N	AE16	RGMII send clock
PHY_TXEN	B64_L18_P	AD16	Send enable signal
PHY_TXD0	B64_L24_P	Y18	Send data bit0
PHY_TXD1	B64_L24_N	AA18	Send data bit1
PHY_TXD2	B64_L6_P	AB24	Send data bit2
PHY_TXD3	B64_L6_N	AC24	Send data bit3

Table3.2.1-Ethernet Pin Assignment

3.3 PCIe3.0 X4 interface

The AXU25 expansion board features an industrial-grade PCIe Gen3 x4 interface for high-speed data transfer. Its PCIE card dimensions comply with standard PCIe specifications, enabling direct installation in any standard PC's x4 PCIe slot.

The PCIe interface's transmit and receive signals are directly connected to the FPGA's GTX transceiver. Both TX and RX signals for the four channels are connected to the FPGA in differential mode, enabling a single-channel communication rate of up to 8G bit bandwidth. The reference clock for PCIe is supplied to the development board via the PC's PCIe slot, operating at a frequency of 100MHz.

The schematic design of the PCIe interface on the development board is shown in Figure 3.3.1, where the TX transmit signal and reference clock CLK are connected in AC coupling mode.

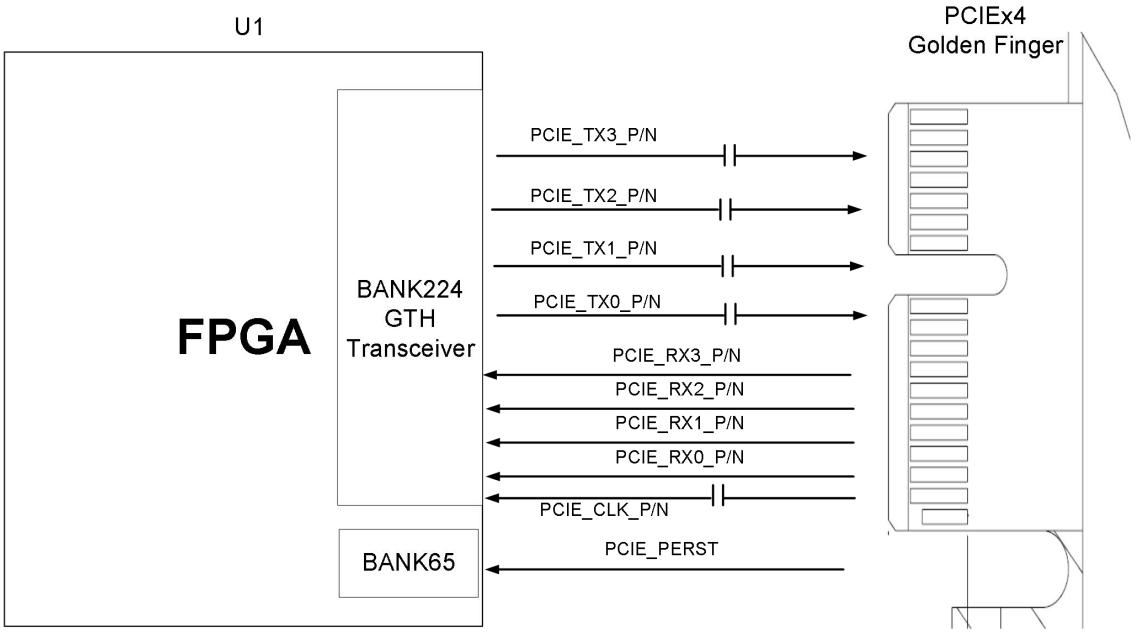

Figure 3.3.1-PCIe x4 Design Schematic

The PCIe x4 interface FPGA pin assignments are as follows:

Network name	FPGA pin	Remarks
PCIE_RX0_P	AB2	Positive data reception on PCIE channel 0
PCIE_RX0_N	AB1	PCIE channel 0 data reception negative
PCIE_RX1_P	AD2	Positive data reception on PCIE channel 1
PCIE_RX1_N	AD1	PCIE channel 1 data reception negative
PCIE_RX2_P	AE4	Positive data reception on PCIE channel 2
PCIE_RX2_N	AE3	PCIE Channel 2 Data Reception Negative
PCIE_RX3_P	AF2	PCIE Channel 3 Data Reception Positive
PCIE_RX3_N	AF1	PCIE channel 3 data reception negative
PCIE_TX0_P	AC5	Positive data transmission on PCIE channel 0
PCIE_TX0_N	AC4	Negative data transmission on PCIE channel 0
PCIE_TX1_P	AD7	Positive data transmission on PCIE channel 1
PCIE_TX1_N	AD6	Negative data transmission on PCIE channel 1

PCIE_TX2_P	AE9	Positive data transmission on PCIE channel 2
PCIE_TX2_N	AE8	Negative data transmission on PCIE channel 2
PCIE_TX3_P	AF7	Positive data transmission on PCIE channel 3
PCIE_TX3_N	AF6	Negative data transmission on PCIE channel 3
PCIE_CLK_P	AB7	Positive reference clock for PCIE
PCIE_CLK_N	AB6	Negative reference clock for PCIE
PCIE_PERST	T19	PCIE reset signal

Table 3.3.1-PCIe x4 Pin Assignment

3.4 FMC Connector

The AXU25 expansion board features a standard FMC HPC expansion port, enabling external connection to Xilinx or our own ALINX FMC modules (including HDMI I/O modules, dual-camera modules, high-speed AD modules, and more).

The FMC expansion port connects 37 pairs of differential signals to the IO of BANK64 and BANK65 on the Artix UltraScale+ FPGA chip, operating at 1.8V with LVDS data communication. Eight pairs of GTY transceiver signals connect to BANK225 and BANK226. The pin assignments for the FMC connectors are shown in the table below.

Signal Name	**FPGA pin name**	**FPGA pin number**	**Remarks**
FMC_SCL	B65_L16_N	V26	FMC's I2C communication clock
FMC_SDA	B65_L16_P	U26	FMC's I2C communication data
FMC_CLK0_N	B65_L14_N	U25	LA reference clock negative
FMC_CLK0_P	B65_L14_P	T25	LA reference clock path 1 Positive
FMC_CLK1_P	B64_L12_P	AB21	LA reference clock path 2 negative
FMC_CLK1_N	B64_L12_N	AC21	LA reference clock path 2 Positive
FMC_LA00_CC_N	B65_L11_N	W23	LA reference to the 0th data (clock) negative
FMC_LA00_CC_P	B65_L11_P	V23	LA reference data (clock) on path 0

FMC_LA01_CC_N	B65_L12_N	W24	LA reference to the first data path (clock) negative
FMC_LA01_CC_P	B65_L12_P	V24	LA reference data (clock) path 1 Positive
FMC_LA02_N	B65_L15_N	P24	LA reference data path 2 negative
FMC_LA02_P	B65_L15_P	N24	LA reference data channel 2 Positive
FMC_LA03_N	B65_L24_N	N22	LA reference data path 3 negative
FMC_LA03_P	B65_L24_P	N21	LA reference data channel 3 Positive
FMC_LA04_N	B65_L18_N	R26	LA reference data path 4 negative
FMC_LA04_P	B65_L18_P	R25	LA reference data channel 4 Positive
FMC_LA05_N	B65_L17_N	P26	LA reference data path 5 negative
FMC_LA05_P	B65_L17_P	P25	LA reference data channel 5 Positive
FMC_LA06_N	B65_L22_N	P23	LA reference data channel 6 negative
FMC_LA06_P	B65_L22_P	N23	LA reference data channel 6 Positive
FMC_LA07_N	B65_L20_N	P21	LA reference data on the 7th channel is negative
FMC_LA07_P	B65_L20_P	P20	LA reference data channel 7 Positive
FMC_LA08_N	B65_L21_N	R21	LA reference data channel 8 negative
FMC_LA08_P	B65_L21_P	R20	LA reference data channel 8 Positive
FMC_LA09_N	B65_L23_N	P19	LA reference data channel 9 negative
FMC_LA09_P	B65_L23_P	N19	LA reference data channel 9 Positive
FMC_LA10_N	B65_L10_N	W26	LA reference data on the 10th channel is negative
FMC_LA10_P	B65_L10_P	W25	LA reference data channel 10 Positive
FMC_LA11_N	B65_L5_N	T23	LA reference data path 11 negative
FMC_LA11_P	B65_L5_P	T22	LA reference data channel 11 Positive
FMC_LA12_N	B65_L19_N	R23	LA reference data on the 12th channel is negative

FMC_LA12_P	B65_L19_P	R22	LA reference data channel 12 Positive
FMC_LA13_N	B65_L3_N	U20	LA reference data path 13 negative
FMC_LA13_P	B65_L3_P	T20	LA reference data channel 13 Positive
FMC_LA14_N	B65_L1_N	V19	LA reference data path 14 negative
FMC_LA14_P	B65_L1_P	U19	LA reference data channel 14 Positive
FMC_LA15_N	B65_L4_N	V22	LA reference data path 15 negative
FMC_LA15_P	B65_L4_P	V21	LA reference data channel 15 Positive
FMC_LA16_N	B65_L2_N	U22	LA reference data on channel 16 is negative
FMC_LA16_P	B65_L2_P	U21	LA reference data channel 16 Positive
FMC_LA17_CC_N	B64_L14_N	AD19	LA reference 17th data (clock) negative
FMC_LA17_CC_P	B64_L14_P	AC19	LA is referencing the 17th data line (clock)
FMC_LA18_CC_N	B64_L13_N	AE20	LA reference 18th data (clock) negative
FMC_LA18_CC_P	B64_L13_P	AD20	LA is referencing the 18th data (clock) channel
FMC_LA19_N	B64_L7_N	AF22	LA reference data path 19 negative
FMC_LA19_P	B64_L7_P	AE22	LA reference data channel 19 Positive
FMC_LA20_N	B64_L17_N	AF17	LA reference data path 20 negative
FMC_LA20_P	B64_L17_P	AE17	LA reference data channel 20 Positive
FMC_LA21_N	B64_L23_N	AA17	LA reference data path 21 negative
FMC_LA21_P	B64_L23_P	Y17	LA reference data path 21 Positive
FMC_LA22_N	B64_L22_N	AC17	LA reference data path 22 negative
FMC_LA22_P	B64_L22_P	AB17	LA reference data channel 22 Positive
FMC_LA23_N	B64_L21_N	AB20	LA reference data path 23 negative
FMC_LA23_P	B64_L21_P	AA20	LA reference data channel 23 Positive

FMC_LA24_N	B64_L16_N	AD18	LA reference data path 24 negative
FMC_LA24_P	B64_L16_P	AC18	LA reference data channel 24 Positive
FMC_LA25_N	B64_L10_N	AB22	LA reference data path 25 negative
FMC_LA25_P	B64_L10_P	AA22	LA reference data channel 25 Positive
FMC_LA26_N	B64_L19_N	Y21	LA reference data path 26 negative
FMC_LA26_P	B64_L19_P	Y20	LA reference data channel 26 Positive
FMC_LA27_N	B64_L20_N	AB19	LA reference data path 27 negative
FMC_LA27_P	B64_L20_P	AA19	LA reference data channel 27 Positive
FMC_LA28_N	B64_L15_N	AF19	LA reference data path 28 negative
FMC_LA28_P	B64_L15_P	AF18	LA reference data channel 28 Positive
FMC_LA29_N	B64_L1_N	AE26	LA reference data path 29 negative
FMC_LA29_P	B64_L1_P	AE25	LA reference data channel 29 Positive
FMC_LA30_N	B64_L3_N	AF25	LA reference data path 30 negative
FMC_LA30_P	B64_L3_P	AF24	LA reference data channel 30 Positive
FMC_LA31_N	B64_L5_N	AD25	LA reference data path 31 negative
FMC_LA31_P	B64_L5_P	AD24	LA reference data path 31 Positive
FMC_LA32_N	B64_L4_N	AD26	LA reference data path 32 negative
FMC_LA32_P	B64_L4_P	AC26	LA reference data channel 32 Positive
FMC_LA33_N	B64_L2_N	AB26	LA reference data path 33 negative
FMC_LA33_P	B64_L2_P	AB25	LA reference data channel 33 Positive
FMC_PRSNT	B65_L8_N	Y26	The FMC module has a signal
FMC_GBTCLK0_M2C_N	225_CLK0_N	V6	FMC transceiver reference clock input 0 negative
FMC_GBTCLK0_M2C_P	225_CLK0_P	V7	The FMC transceiver reference clock input 0 is positive

FMC_DP0_C2M_N	225_TX0_N	AA4	FMC transceiver data transmission 0 negative
FMC_DP0_C2M_P	225_TX0_P	AA5	FMC transceiver data transmission 0 positive
FMC_DP0_M2C_N	225_RX0_N	Y1	FMC transceiver data reception 0 negative
FMC_DP0_M2C_P	225_RX0_P	Y2	FMC transceiver data reception 0 positive
FMC_DP1_C2M_N	225_TX1_N	W4	FMC transceiver sends a negative data signal
FMC_DP1_C2M_P	225_TX1_P	W5	FMC transceiver data transmission 1 positive
FMC_DP1_M2C_N	225_RX1_N	V1	FMC transceiver data reception 1 negative
FMC_DP1_M2C_P	225_RX1_P	V2	FMC transceiver data reception 1 positive
FMC_DP2_C2M_N	225_TX2_N	U4	FMC transceiver data transmission 2 negative
FMC_DP2_C2M_P	225_TX2_P	U5	FMC transceiver data transmission 2 positive
FMC_DP2_M2C_N	225_RX2_N	T1	FMC transceiver data reception 2 negative
FMC_DP2_M2C_P	225_RX2_P	T2	FMC transceiver data reception 2 positive
FMC_DP3_C2M_N	225_TX3_N	R4	FMC transceiver data transmission 3 negative
FMC_DP3_C2M_P	225_TX3_P	R5	FMC transceiver data transmission 3 positive
FMC_DP3_M2C_N	225_RX3_N	P1	FMC transceiver data reception 3 negative
FMC_DP3_M2C_P	225_RX3_P	P2	FMC transceiver data reception 3 positive
FMC_DP4_C2M_N	226_TX0_N	N4	FMC transceiver data transmission 4 negative
FMC_DP4_C2M_P	226_TX0_P	N5	FMC transceiver data transmission 4 positive
FMC_DP4_M2C_N	226_RX0_N	M1	FMC transceiver data reception 4 negative
FMC_DP4_M2C_P	226_RX0_P	M2	FMC transceiver data reception 4 positive
FMC_DP5_C2M_N	226_TX1_N	L4	FMC transceiver data transmission 5 negative
FMC_DP5_C2M_P	226_TX1_P	L5	FMC transceiver data transmission 5 positive
FMC_DP5_M2C_N	226_RX1_N	K1	FMC transceiver data reception 5 negative
FMC_DP5_M2C_P	226_RX1_P	K2	FMC transceiver data reception 5 positive

FMC_DP6_C2M_N	226_TX2_N	J4	FMC transceiver sends 6 negative data
FMC_DP6_C2M_P	226_TX2_P	J5	FMC transceiver data transmission 6 positive
FMC_DP6_M2C_N	226_RX2_N	H1	FMC transceiver data reception 6 negative
FMC_DP6_M2C_P	226_RX2_P	H2	FMC transceiver data reception 6 positive
FMC_DP7_C2M_N	226_TX3_N	G4	FMC transceiver data transmission 7 negative
FMC_DP7_C2M_P	226_TX3_P	G5	FMC transceiver data transmission 7 positive
FMC_DP7_M2C_N	226_RX3_N	F1	FMC transceiver data reception 7 negative
FMC_DP7_M2C_P	226_RX3_P	F2	FMC transceiver data reception 7 positive
FMC_GBTCLK1_M2C_P	226_CLK0_P	P7	FMC transceiver reference clock input 1 positive
FMC_GBTCLK1_M2C_N	226_CLK0_N	P6	FMC transceiver reference clock input 1 negative

Table3.4.1-FMC Connector Pin Assignment

3.5 USB to Serial Port

The development board incorporates the Silicon Labs CP2102GM USB-UART chip, featuring a MINI USB port for serial communication with a PC via a USB cable. The schematic of the USB UART circuit design is shown in Figure 3.5.1.

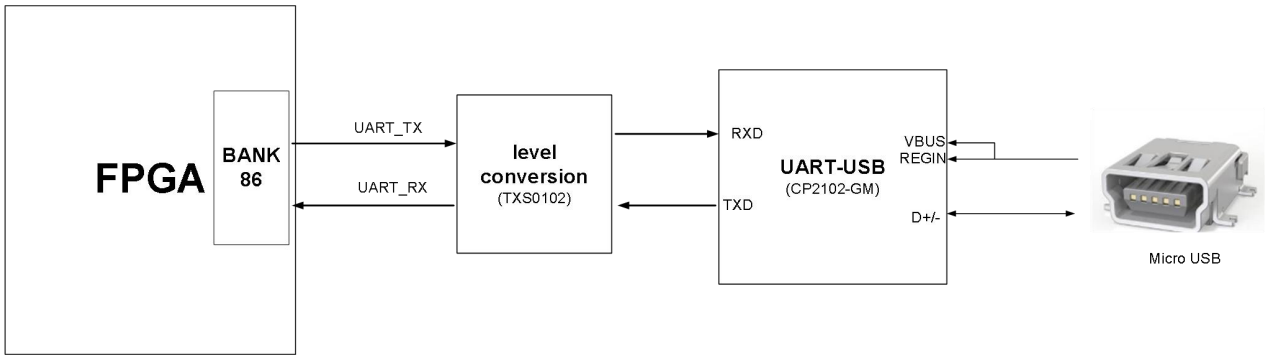

Figure 3.5.1-USB Serial-to-Parallel Port Schematic

FPGA pin configuration for UART to serial port conversion:

Signal Name	FPGA pin name	FPGA pin number	Remarks
UART1_RXD	B86_L11_N	A12	Uart data-in
UART1_TXD	B86_L11_P	A13	Uart presentation of information

Table 3.5.1-UART Serial Port Pin Assignment

3.6 TF Card Slot

TF cards are now widely used storage devices. The TF card we developed supports both SPI and SD modes. The schematic diagram is shown below.

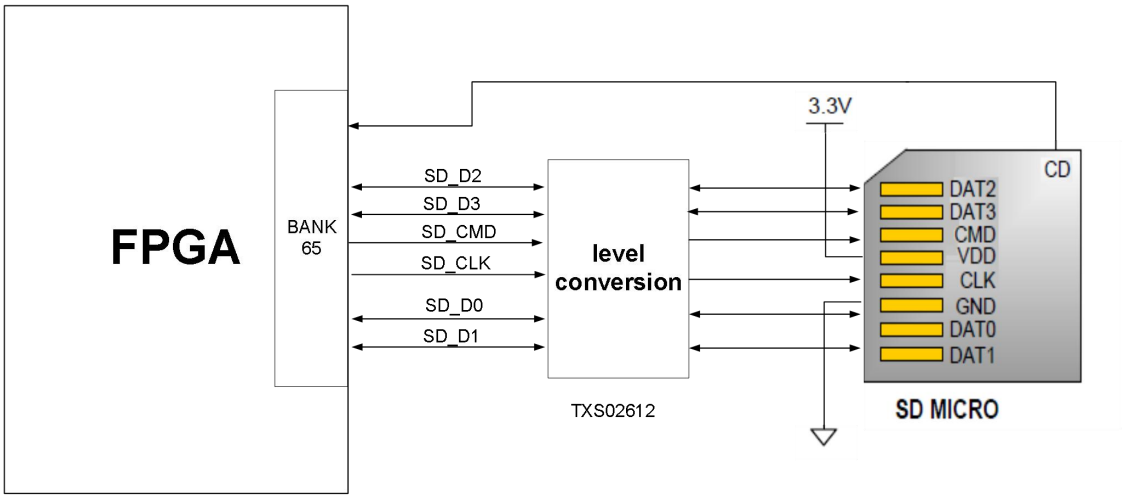

Figure 3.6.1-TF Card Slot Schematic

SD Card Slot Pin Assignment

Signal Name	FPGA pin name	FPGA pin number	Remarks
SD_CD	B65_L8_P	Y25	SD card insertion signal
SD_CLK	B65_L9_N	AA25	SD clock signal
SD_CMD	B65_L9_P	AA24	SD command signal
SD_D0	B65_L7_P	Y22	SD Data Data0
SD_D1	B65_L7_N	Y23	SD Data Data1
SD_D2	B65_L6_N	W20	SD Data Data2

SD_D3	B65_L6_P	W19	SD Data Data3

Table3.6.1-SD Card Slot Pin Assignment

3.7 EEPROM 24LC04

The AXU25 development board features a 24LC04 EEPROM (256x8-bit, 4Kbit capacity) with two 256-byte blocks, communicating via the I2C bus. This EEPROM is specifically designed to demonstrate I2C bus communication. The EEPROM's I2C signal is connected to the BANK14 IO port on the FPGA. The schematic diagram below illustrates the EEPROM's design.

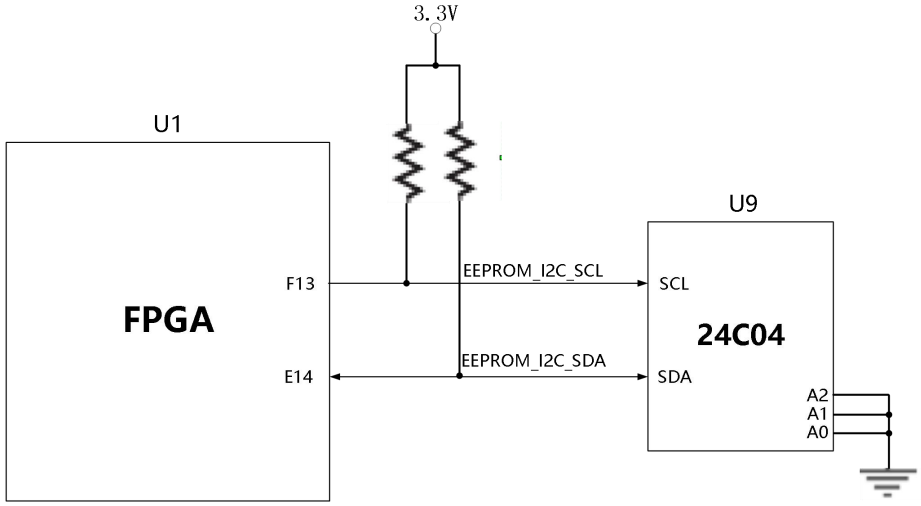

Figure 3.7.1-EEPROM schematic section

Pin name	FPGA pin name	FPGA pin
EEPROM_I2C_SCL	B86_L12_N	A14
EEPROM_I2C_SDA	B86_L12_P	B14

Table 3.7.1-EEPROM Pin Assignment

3.8 JTAG Interface

The development board features a JTAG interface for downloading FPGA programs or firmware to the FLASH memory. To prevent damage to the FPGA chip during hot-plugging, we added a protection diode to the JTAG signal, ensuring the voltage stays within the FPGA's operational range. When plugging or unplugging the JTAG cable, avoid hot-plugging.

3.9 Expansion Port

The expansion board features two 2.54mm standard 40-pin expansion ports (J33 and J34) for connecting ALINX modules or custom external circuits. These ports provide 40 signal lines: 15V power line, 23.3V power lines, 3 ground lines, and 34 I/O lines. The I/O signals operate at 3.3V. Direct connections between I/O lines and 5V devices must be avoided to prevent FPGA damage. For 5V devices, a level-shifting chip is required.

J33 pin number	FPGA pin name	FPGA pin number	Level standard
J33_1	-	-	the earth
J33_2	-	-	Power supply 5V
J33_3	B86_L4_P	J15	IO 3.3V
J33_4	B86_L4_N	J14	IO 3.3V
J33_5	B86_L2_P	J13	IO 3.3V
J33_6	B86_L2_N	H13	IO 3.3V
J33_7	B85_L7_P	E11	IO 3.3V
J33_8	B85_L7_N	E10	IO 3.3V
J33_9	B85_L8_P	D11	IO 3.3V
J33_10	B85_L8_N	D10	IO 3.3V
J33_11	B85_L11_P	B10	IO 3.3V
J33_12	B85_L11_N	A10	IO 3.3V
J33_13	B85_L4_P	H11	IO 3.3V
J33_14	B85_L4_N	G11	IO 3.3V
J33_15	B85_L2_P	J11	IO 3.3V
J33_16	B85_L2_N	J10	IO 3.3V
J33_17	B85_L1_P	K10	IO 3.3V
J33_18	B85_L1_N	K9	IO 3.3V

J33_19	B84_L2_N	AF13	IO 3.3V
J33_20	B84_L2_P	AE13	IO 3.3V
J33_21	B84_L1_N	AF15	IO 3.3V
J33_22	B84_L1_P	AF14	IO 3.3V
J33_23	B84_L3_N	AE15	IO 3.3V
J33_24	B84_L3_P	AD15	IO 3.3V
J33_25	B84_L4_N	AD14	IO 3.3V
J33_26	B84_L4_P	AD13	IO 3.3V
J33_27	B84_L6_N	AB16	IO 3.3V
J33_28	B84_L6_P	AB15	IO 3.3V
J33_29	B84_L10_P	W14	IO 3.3V
J33_30	B84_L10_N	W15	IO 3.3V
J33_31	B84_L7_P	Y15	IO 3.3V
J33_32	B84_L7_N	AA15	IO 3.3V
J33_33	B84_L12_P	W12	IO 3.3V
J33_34	B84_L12_N	W13	IO 3.3V
J33_35	B84_L8_P	AA14	IO 3.3V
J33_36	B84_L8_N	AB14	IO 3.3V
J33_37	-	-	the earth
J33_38	-	-	the earth
J33_39	-	-	3.3V power supply
J33_40	-	-	3.3V power supply

Table 3.9.1-J33 Expansion Port Pin Assignment

Pin configuration for J34 expansion port FPGA

J34 pin number	FPGA pin name	FPGA pin number	Level standard
J34_1	-	-	the earth
J34_2	-	-	Power supply 5V
J34_3	B84_L5_N	AC14	IO 3.3V
J34_4	B84_L5_P	AC13	IO 3.3V
J34_5	B84_L11_N	AA13	IO 3.3V
J34_6	B84_L11_P	Y13	IO 3.3V
J34_7	B84_L9_N	Y16	IO 3.3V
J34_8	B84_L9_P	W16	IO 3.3V
J34_9	B85_L3_N	H9	IO 3.3V
J34_10	B85_L3_P	J9	IO 3.3V
J34_11	B85_L6_N	F9	IO 3.3V
J34_12	B85_L6_P	F10	IO 3.3V
J34_13	B85_L5_N	G9	IO 3.3V
J34_14	B85_L5_P	G10	IO 3.3V
J34_15	B85_L9_N	C9	IO 3.3V
J34_16	B85_L9_P	D9	IO 3.3V
J34_17	B85_L10_N	A9	IO 3.3V
J34_18	B85_L10_P	B9	IO 3.3V
J34_19	B85_L12_N	B11	IO 3.3V
J34_20	B85_L12_P	C11	IO 3.3V
J34_21	B86_L1_N	H12	IO 3.3V

J34_22	B86_L1_P	J12	IO 3.3V
J34_23	B86_L5_N	F12	IO 3.3V
J34_24	B86_L5_P	G12	IO 3.3V
J34_25	B86_L3_N	G14	IO 3.3V
J34_26	B86_L3_P	H14	IO 3.3V
J34_27	B86_L7_N	E12	IO 3.3V
J34_28	B86_L7_P	E13	IO 3.3V
J34_29	B86_L10_N	B12	IO 3.3V
J34_30	B86_L10_P	C12	IO 3.3V
J34_31	B86_L6_N	F13	IO 3.3V
J34_32	B86_L6_P	F14	IO 3.3V
J34_33	B86_L8_P	D14	IO 3.3V
J34_34	B86_L8_N	D13	IO 3.3V
J34_35	B86_L9_P	C14	IO 3.3V
J34_36	B86_L9_N	C13	IO 3.3V
J34_37	-	-	the earth
J34_38	-	-	the earth
J34_39	-	-	3.3V power supply
J34_40	-	-	3.3V power supply

Table3.9.2-J34 Expansion Port Pin Assignment

3.10 Key

The expansion board features two user buttons (KEY1 and KEY2), both connected to the FPGA's standard I/O pins. These buttons operate on a low-level logic system: they pull the FPGA's I/O input voltage to low when pressed, and high when left unpressed. The button circuitry is detailed in Figure 3.10.1.

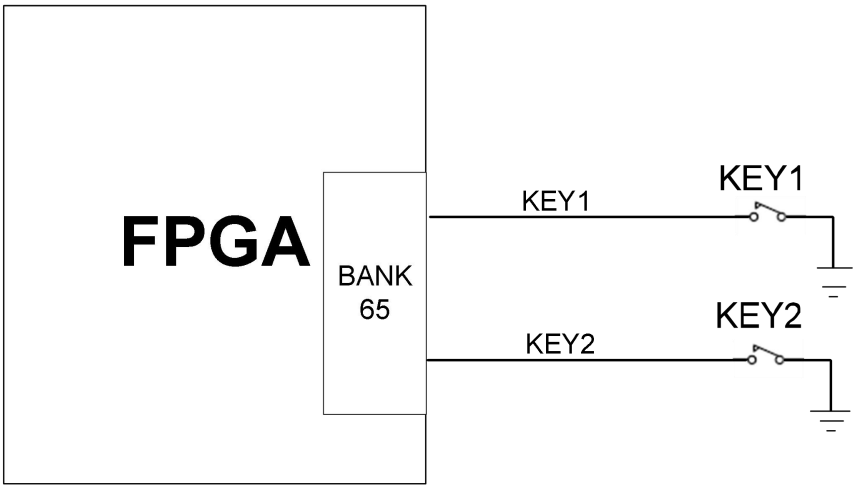

Figure 3.10.1-Schematic diagram of button hardware design

Signal Name	FPGA pin name	FPGA pin number	Remarks
KEY1	B65_T2U	N26	User Key 1
KEY2	B65_T1U	AA23	User button 2

Table3.10.1-Button Pin Assignment

3.11 LED light

The expansion board features six red LEDs: one power indicator (PWR), two USB UART data transmission indicators, two user LEDs (LED1-LED2), and one configuration indicator (DONE). When powered, the power indicator illuminates. User LEDs 1-2 connect to the FPGA's standard I/O ports. When the I/O voltage is set to high, the LEDs light up; when set to low, they turn off. The DONE indicator extinguishes upon successful FPGA configuration. The schematic diagram of the LED hardware connections is shown in the figure.

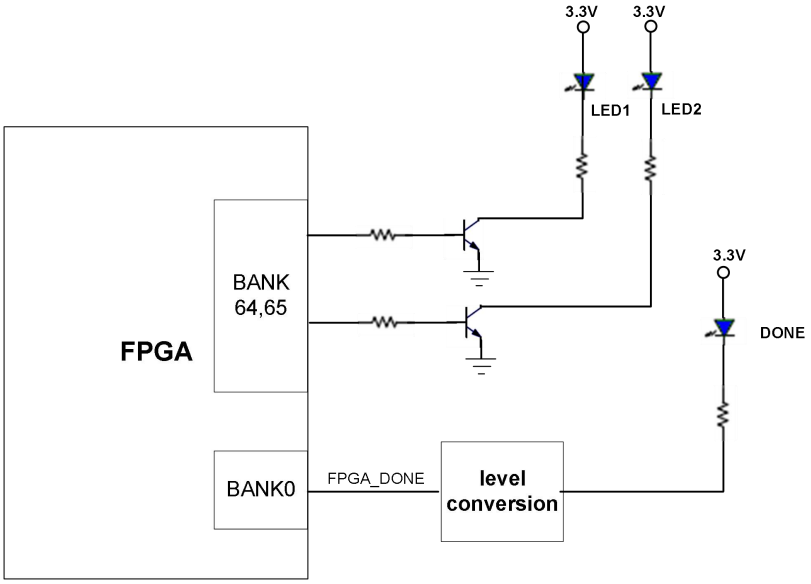

Figure 3.11.1-Schematic Diagram of LED Light Hardware Design

Signal Name	FPGA pin name	FPGA pin number	Remarks
LED1	B65_T0U	W21	User-defined indicator light
LED2	B64_T3U	AC16	User-defined indicator light

Table 3.11.1-LED Pin Assignment

3.12 Power Supply

The development board requires a DC12V power input. Use its built-in power supply exclusively to prevent damage. The expansion board converts the power through a 4-channel DC/DC converter (ETA1471FT2G) into four outputs: +5V,+3.3V,+1.8V and VADJ. The VADJ output can be adjusted to 1.2V via a jumper cap for dedicated power to the FMC module. Additionally, the +12V power from the expansion board is distributed to the core board through inter-board connectors. The power layout is illustrated in the diagram below.

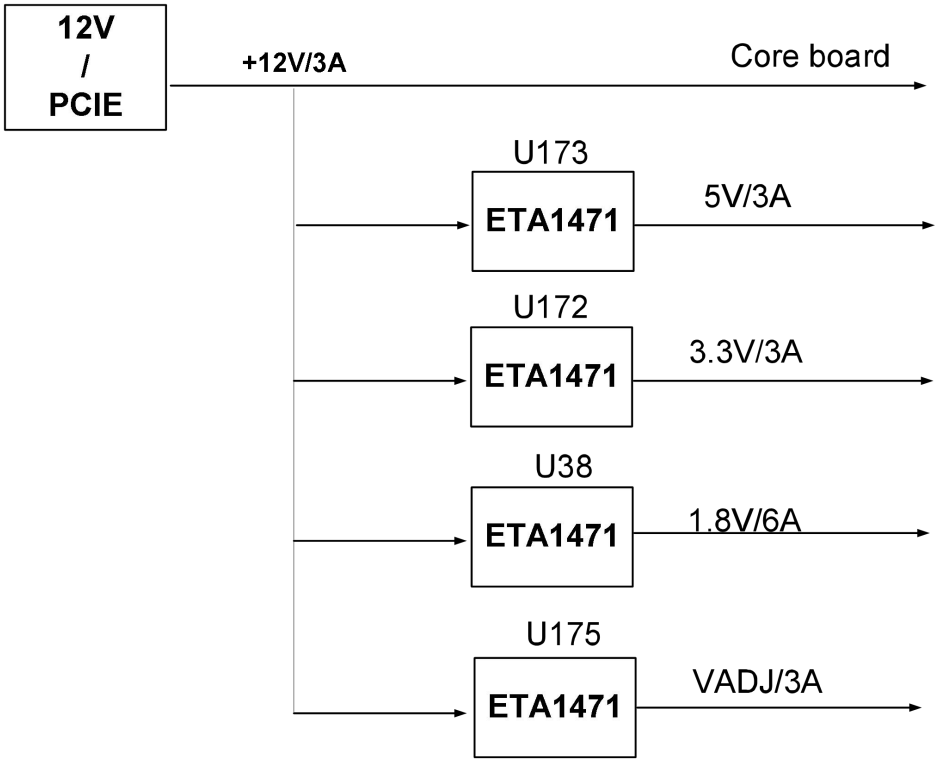

Figure 3.12.1-Schematic diagram of the extension board power supply

3.13 Structural dimensions

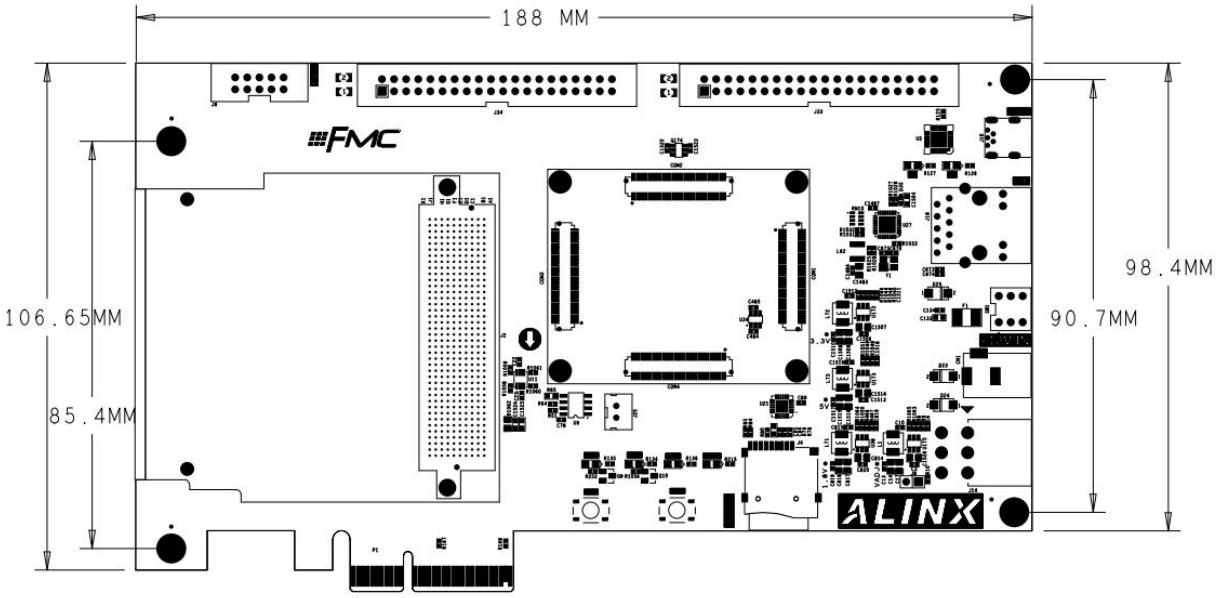

Figure 3.13.1-Top view of the development board

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