Xilinx FPGA Development Platform User Manual

AXKU15

Development Board

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Version Record

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The development board (model: AXKU15) based on the Xilinx FPGA Kintex Ultrascale+ development platform of Alinx Electronic Technology has been officially released. To let users have a quick understanding of this development platform, we have written this user manual.

This Kintex Ultrascale+ FPGA development platform adopts the mode of SOM module plus base board, which is convenient for users to develop and utilize the SOM for the second time. The module uses the solution of Xilinx's Kintex Ultrascale+ chip XCKU15PFFVE1517, which mounts five 1GB high-speed DDR4 SDRAM chips and two 512Mb QSPI FLASH chips.

In the design of the base board, we have expanded rich peripheral interfaces for users, such as one PCIe3.0x16 interface, two FMC HPC interfaces, one Gigabit Ethernet interface, two QSFP28 optical fiber interfaces, two MIPIx4 input interfaces, one UART serial interface, one SD card interface and so on. It is a "professional" FPGA development platform, which can meet the requirements of high-speed data exchange, video transmission processing and industrial control. It is possible for high-speed data transmission and exchange, early verification, and later application of data processing. It is believed that such a product is very suitable for students, engineers and other groups engaged in FPGA development.

Figure 1: AXKU15 development board

Part 1: Development Board Introduction

Here is a brief introduction to the functionality of the Kintex Ultrascale+ AXKU15 development platform.

The whole structure of the development board is designed by inheriting our consistent SOM module + expansion board model. High-speed inter-board connectors are used between the module and the expansion board.

The module is mainly composed of XCKU15PFFVE1517 + 5 DDR4 + QSPI FLASH minimum systems. Using Xilinx's Kintex Ultrascale+ series chip, model XCKU15PFFVE1517. Five DDR4 memory chips are connected to the HP port of the FPGA chip. The capacity of each DDR4 chip is up to 1GB bytes, forming a data bit width of 80 bits. Two 512Mb QSPI FLASHs are used to statically store configuration files or other user data of the FPGA chip.

The base board expands abundant peripheral interfaces for the module, including one PCIe3.0x16 interface, two FMC HPC interfaces, one gigabit network interface, two MIPI input interfaces, one UART serial interface, one SD card interface, and some keys and LEDs.

The following Figure 2 shows the structure of the entire development system:

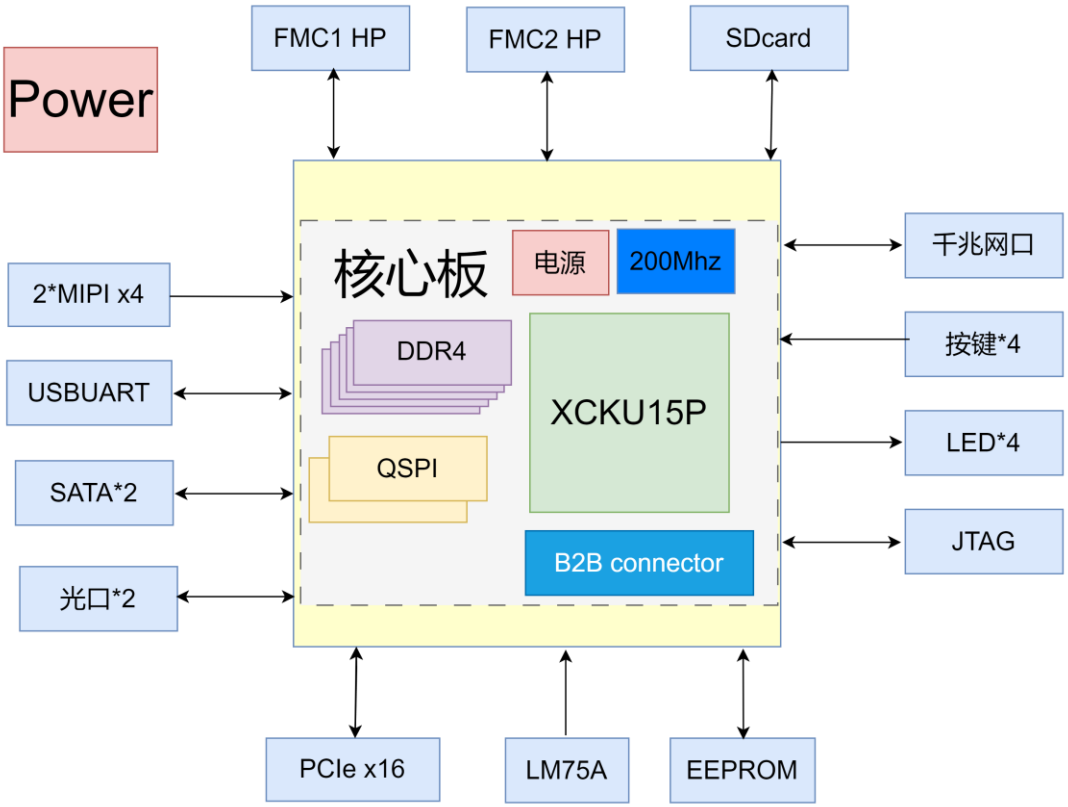

Figure 2: Structure of AXKU15

Through this diagram, we can see the interfaces and functions that our development platform can contain.

- **FPGA SOM module**

It is composed of the minimum system of XCKU15P + 5 DDR4 + 2 QSPI FLASH. In addition, two crystal oscillators provide the clock, and two 200MHz crystal oscillators provide the reference clock for FPGA logic and DDR control.

- **PCIe3.0 x16 interface**

It supports PCI Express 3.0 standard, provides standard PCIe x16 high-speed data transmission interface, and the communication rate of single channel can be up to 8GBaud.

- **2 * FMC HPC interface**

Eight high-speed transceivers in the FPGA are connected to high-speed pins dedicated for the FMC HPC, wherein one FMC interface leads out 34 pairs of LA signal differential pairs, 2 pairs of clock signals and 24 pairs of HA signals; The other FMC interface leads out 34 pairs of LA signal differential pairs and 2 pairs of clock signals, which can meet the requirements of high-speed signal transmission, comply with the FMC standard, and can be used for various FMC modules (HDMI input and output modules, high-speed AD modules, etc.).

- **1 * Gigabit network interface**

Gigabit Ethernet interface chip uses JL2121D Ethernet PHY chip to provide network communication services for users. The chip supports 10/100/1,000 Mbps network transmission rate; Full-duplex and adaptive.

- **2 * MIPI input interface**

Onboard two MIPI lanex4 input interfaces, supporting up to 2.5Gb/s, is used to connect MIPI camera module.

- **USB Uart interface**

One Uart to USB interface is used to communicate with the computer, which is convenient for users to debug. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- **Micro SD deck**

One Micro SD deck for storing OS images and file systems.

- **2 * SATA interface**

Two standard SATA interfaces can be used to connect SATA peripherals, such as solid-state drives with SATA interfaces.

- **JTAG debug port**

One 10-pin 2.54 mm standard JTAG port is used to download and debug the FPGA program. Users can debug and download the FPGA system through the XILINX downloader.

- **Led light**

7 LEDs, 3 on the module and 7 on the base board. 1 power indicator on the module; 1 DONE configuration indicator and user indicator. There is one power indicator, four user indicators, and two serial port indicators on the base board.

- **Key**

4 user buttons on the base board.

Part 2: ACKU15 SOM Module

Part 2.1: Introduction

ACKU15 (SOM model, the same below) SOM module, FPGA chip is based on the Xilinx FPGA Kintex Ultrascale+ main chip XCKU15PFFVE1517 design. The module connects five DDR4 memory chips to the HP port of the FPGA to form an 80-bit data bandwidth, and the capacity of each DDR4 chip is up to 1GB. Memory bandwidth on the HP side is up to 210Gb/s. In addition, two QSPI FLASHs of 512MBit size are integrated on the module, which are used to start storage configuration and system files.

This module expands 256 HPIOs and 88 HDIOs by using a board-to-board connector. The level of the outgoing IO can be modified by replacing the LDO chip on the base board to meet the user's requirement of not using a level interface. In addition, the module also expands 24 pairs of GTY and 32 pairs of GTH high-speed transceiver interfaces. This module will be a good choice for users who need a lot of IO and high-speed transceivers. Moreover, in the IO connection part, the wiring between the FPGA chip and the interface is processed with equal length and difference, and the size of the module is only 80 * 80 (mm), which is very suitable for secondary development.

Figure 3: Front View of ACKU15 Module

Part 2.2: FPGA Chip

As mentioned above, the model of the FPGA we used is XCKU15PFFVE1517, which belongs to the Kintex Ultrascale+ series of Xilinx, with a speed grade of 2 and an industrial temperature grade. This model is in the FFVE1517 package with 1517 pins. The chip naming rule of Xilinx Kintex Ultrascale+ FPGA is as follows:

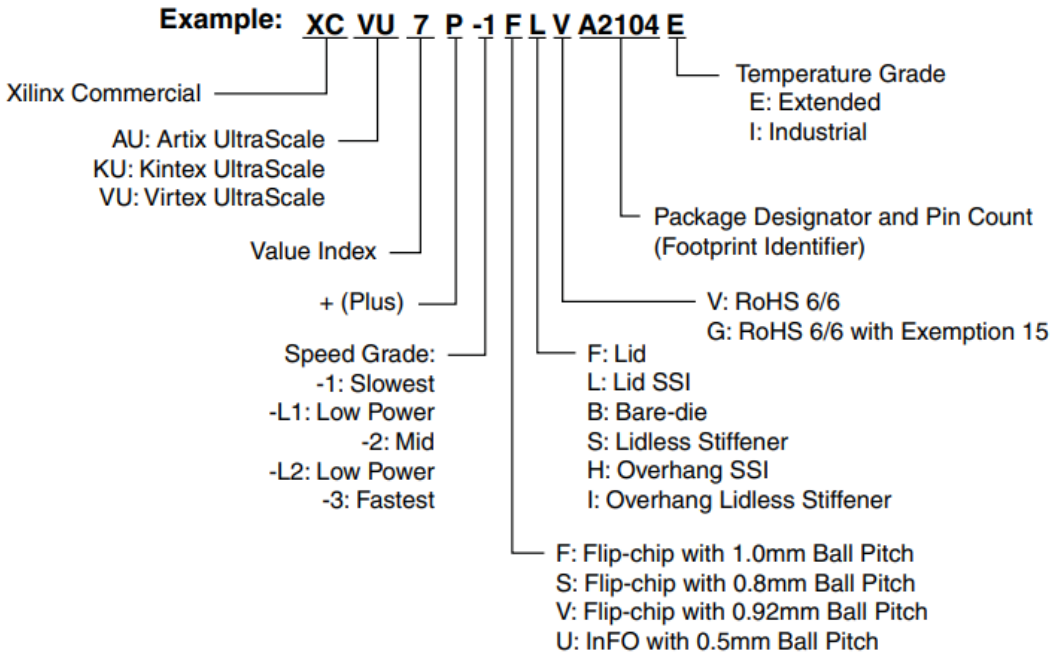

Figure 4: Ordering Information

Figure 5 is the physical picture of the FPGA chip used in the development board.

Figure 5: Physical FPGA chip

The main parameters of the FPGA chip are as follows:

Name	Specific parameters
Logic Cells	1143K
Trigger (FF)	1,045,440
LUTs	522,720
Total Block RAM	34.6Mb
DSP Slices	1968
CMTs	11
GTY/Gb/s	24/28.21Gb
GTH/Gb/s	32/16.3Gb
PCIe Gen3 x16	1
Speed rating	-2
Temperature class	Industrial grade

Table 1: Main parameters of the FPGA chip

Part 2.3: DDR4

The ACKU15 SOM module is equipped with five Micron 1GB DDR4 chips, model MT40A512M16LY-062 E, which are connected to the HP side of the FPGA to form an 80-bit data bus with a capacity of 5GB. The maximum running data rate of DDR4 SDRAM on the FPGA side is 2,666Mbps, and five DDR4 memory systems are directly connected to the memory interfaces of BANK 66, 67 and 68. The specific configuration of DDR4 SDRAM is shown in Table 2 below.

Tag number	Chip model	Capacity	Manufacturer
U3、U4、U7、U8、U9	MT40A512M16LY-062E	512Mx 16bit	Micron

Table 2: DDR4 SDRAM Configuration

The hardware design of DDR4 needs to strictly consider the signal integrity. We have fully considered the matching resistor/termination resistor, trace impedance control, and trace length control in the circuit design and PCB design to ensure the high-speed and stable operation of DDR4.

The hardware connection mode of DDR4 on the FPGA side is shown in Figure 6:

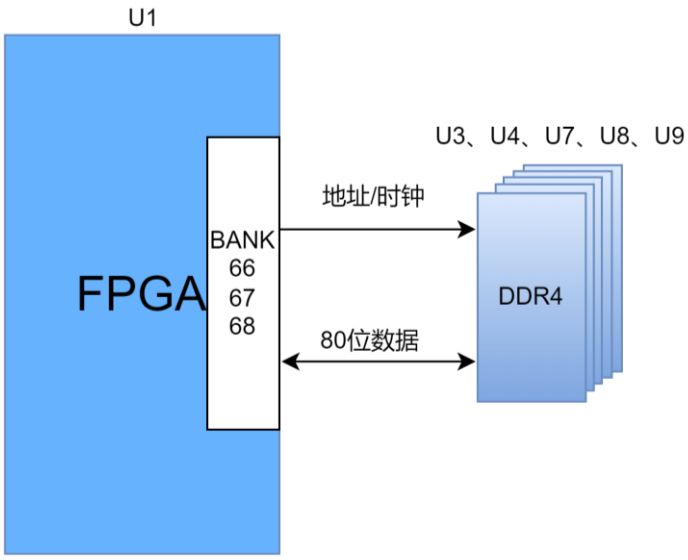

Figure 6: DDR4 DRAM Schematic

Figure 7 shows the physical picture of two DDR4 DRAMs of the development board.

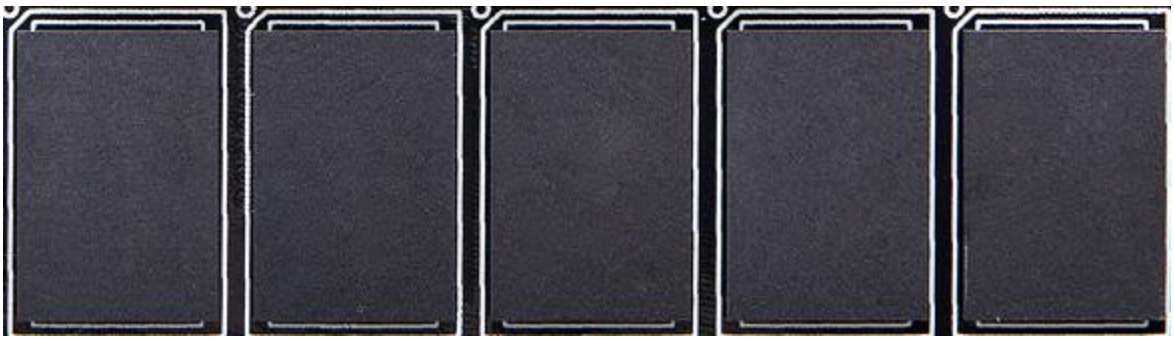

Figure 7: Physical drawing of 4 DDR4 DRAM

DDR4 SDRAM pin assignment:

Signal name	Pin number
DDR4_D0	AJ28
DDR4_D1	AK27
DDR4_D2	AK26
DDR4_D3	AL27
DDR4_D4	AJ26
DDR4_D5	AN26
DDR4_D6	AN27
DDR4_D7	AK28
DDR4_D8	AK22
DDR4_D9	AL24
DDR4_D10	AJ23
DDR4_D11	AM25
DDR4_D12	AH23
DDR4_D13	AK24
DDR4_D14	AK23
DDR4_D15	AJ24
DDR4_D16	AN25
DDR4_D17	AP23
DDR4_D18	AP24
DDR4_D19	AT25
DDR4_D20	AN23
DDR4_D21	AP26
DDR4_D22	AP25
DDR4_D23	AT26
DDR4_D24	AU23
DDR4_D25	AV26
DDR4_D26	AU24
DDR4_D27	AW25
DDR4_D28	AT24
DDR4_D29	AW26
DDR4_D30	AV23
DDR4_D31	AV27
DDR4_D32	AM38
DDR4_D33	AK39
DDR4_D34	AL37
DDR4_D35	AL39
DDR4_D36	AN38
DDR4_D37	AJ39
DDR4_D38	AL36
DDR4_D39	AM39
DDR4_D40	AM35
DDR4_D41	AL35
DDR4_D42	AM34
DDR4_D43	AL34
DDR4_D44	AH33
DDR4_D45	AK35

DDR4_D46	AJ33
DDR4_D47	AJ34
DDR4_D48	AK32
DDR4_D49	AL32
DDR4_D50	AJ30
DDR4_D51	AM33
DDR4_D52	AH31
DDR4_D53	AH32
DDR4_D54	AJ29
DDR4_D55	AM32
DDR4_D56	AL29
DDR4_D57	AM30
DDR4_D58	AM29
DDR4_D59	AN33
DDR4_D60	AP28
DDR4_D61	AL30
DDR4_D62	AP29
DDR4_D63	AN32
DDR4_D64	AU29
DDR4_D65	AW31
DDR4_D66	AW28
DDR4_D67	AV31
DDR4_D68	AT29
DDR4_D69	AU30
DDR4_D70	AW29
DDR4_D71	AT30
DDR4_D72	AT35
DDR4_D73	AW34
DDR4_D74	AU33
DDR4_D75	AU34
DDR4_D76	AU32
DDR4_D77	AT36
DDR4_D78	AU35
DDR4_D79	AW35
DDR4_DM0	AL25
DDR4_DM1	AM23
DDR4_DM2	AR23
DDR4_DM3	AW23
DDR4_DM4	AM37
DDR4_DM5	AK33
DDR4_DM6	AH30
DDR4_DM7	AM28
DDR4_DM8	AU28
DDR4_DM9	AV35
DDR4_DQS0_N	AH27
DDR4_DQS0_P	AH26
DDR4_DQS1_N	AJ25
DDR4_DQS1_P	AH25

DDR4_DQS2_N	AR27
DDR4_DQS2_P	AR26
DDR4_DQS3_N	AV25
DDR4_DQS3_P	AU25
DDR4_DQS4_N	AK38
DDR4_DQS4_P	AK37
DDR4_DQS5_N	AN36
DDR4_DQS5_P	AN35
DDR4_DQS6_N	AL31
DDR4_DQS6_P	AK31
DDR4_DQS7_N	AN31
DDR4_DQS7_P	AN30
DDR4_DQS8_N	AW30
DDR4_DQS8_P	AV30
DDR4_DQS9_N	AV33
DDR4_DQS9_P	AV32
DDR4_OTD	AR33
DDR4_PAR	AV36
DDR4_RAS_B	AP35
DDR4_RST	AH34
DDR4_WE_B	AP31
DDR4_A0	AV38
DDR4_A1	AR38
DDR4_A2	AV37
DDR4_A3	AR36
DDR4_A4	AU39
DDR4_A5	AP38
DDR4_A6	AT31
DDR4_A7	AP39
DDR4_A8	AV28
DDR4_A9	AT39
DDR4_A10	AU38
DDR4_A11	AW36
DDR4_A12	AR37
DDR4_A13	AR39
DDR4_ACT_B	AT37
DDR4_ALERT_B	AK34
DDR4_BA0	AW33
DDR4_BA1	AP36
DDR4_BG0	AR31
DDR4_CAS_B	AP34
DDR4_CKE	AU37
DDR4_CLK_N	AT34
DDR4_CLK_P	AR34
DDR4_CLKREF_N	AT32
DDR4_CLKREF_P	AR32
DDR4_CS_B	AP33

Table 3: DDR4 SDRAM pin assignment

Part 2.4: QSPI Flash

The module is equipped with two Quad-SPI FLASH chips of 512MBit size, model MT25QU512ABA1EW9, which uses 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store the configuration Bin file of the FPGA as well as other user data files during use. See Table 4 for the specific model and relevant parameters of QSPI FLASH.

Tag number	Type of chip	Capacity	Manufacturer
U10、U11	MT25QU512ABB1EW9	256Mbit	Micron

Table 4: Model and Parameters of QSPI Flash

The QSPI FLASH is connected to a dedicated pin of the FPGA chip, wherein the clock pin is connected to CCLK0 of the dedicated BANK0, and the data pins are respectively connected to BANK0 and BANK65. Figure 8 is the connection diagram of QSPI Flash and FPGA chip.

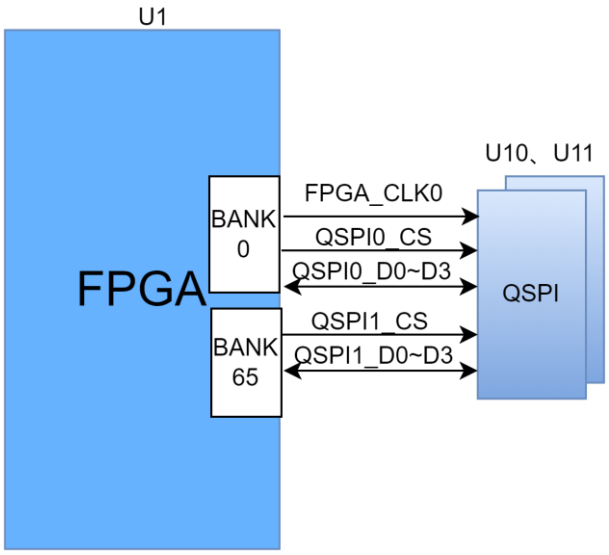

Figure 8: QSPI Flash Connection Diagram

Configure chip pin assignment:

Signal name	FPGA pin number
QSPI_CLK	AD23
QSPI0_CS	AG22
QSPI0_DQ0	AD25
QSPI0_DQ1	AD26
QSPI0_DQ2	AE22
QSPI0_DQ3	AE23
QSPI1_CS	AV11
QSPI1_DQ0	AM12
QSPI1_DQ1	AN12
QSPI1_DQ2	AR13
QSPI1_DQ3	AR12

Table 5: QSPI Flash pin assignment

Part 2.5: Clock Configuration

The module provides two 200Mhz differential active clocks for the FPGA system. And provide differential clock sources for that logic part of the FPGA respectively. The schematic diagram of the clock circuit design is shown in Figure 9 below:

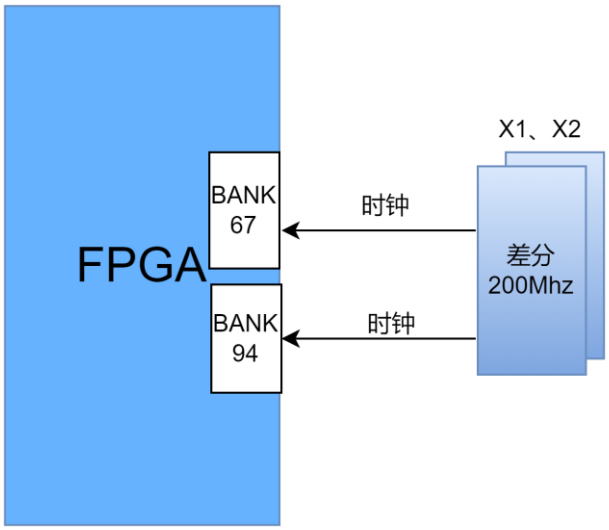

Figure 9: SOM module Clock Source

FPGA system clock source:

Two 200MHz differential crystals are provided on the board to provide a reference clock for the DDR4 controller and FPGA logic. The output of the crystal oscillator is connected to the global clock of the FPGA BANK66 and BANK84, which can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of the clock source is shown in Figure 10-12.

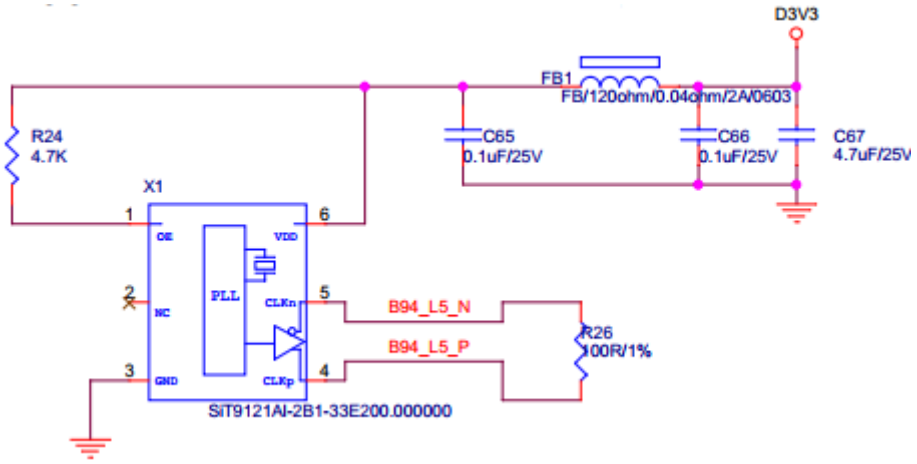

Figure 10: System clock source

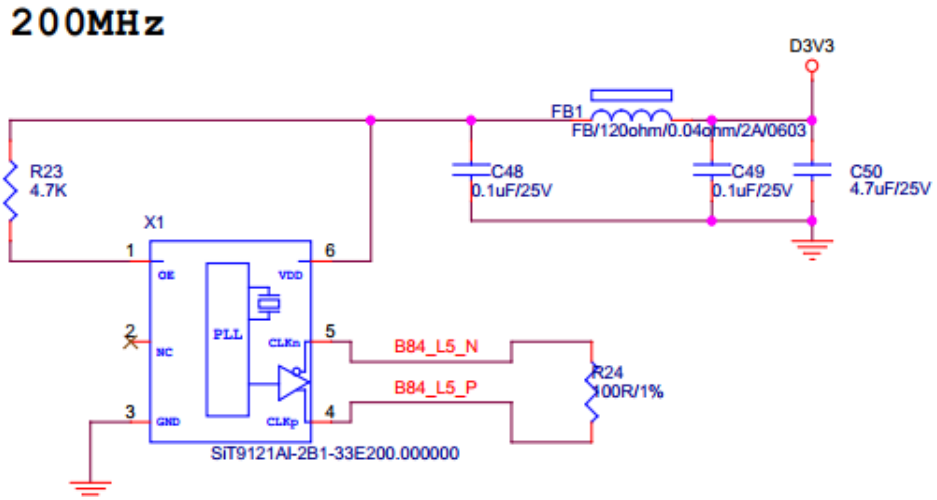

Figure 11: System clock source

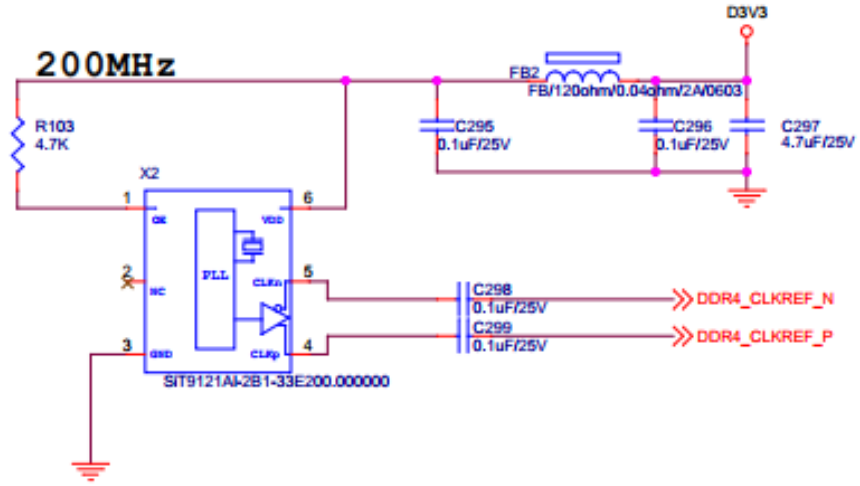

Figure 12: System clock source

Clock pin assignment:

Signal name	FPGA pins
B94_L5_P	G12
B94_L5_N	E11
DDR4_CLKREF_P	AR32
DDR4_CLKREF_N	AT32

Table 6: Clock pin assignments

Part 2.6: LED Light

There are three red LEDs on the ACKU15 module, one of which is a power indicator (PWR1), one of which is a configuration LED (D1), and a user indicator (LED 1). The indicator lights up when the module is powered up, and the configuration LED lights up when the FPGA has configured the program. User indicator lights can be used to customize the function indication. Schematic diagram of hardware connection of LED lamp is shown in Figure 13:

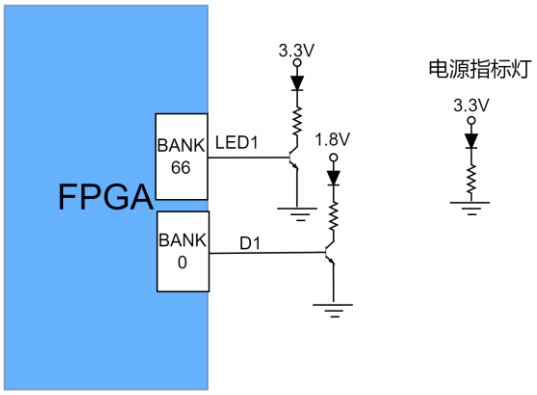

Figure 13: Schematic diagram of hardware connection of LED lamp on module

Part 2.7: Power source

The power supply voltage of the ACKU15 module is +12V, which is supplied through the connection base board. The power supply design diagram on the board is shown in Figure 14 below:

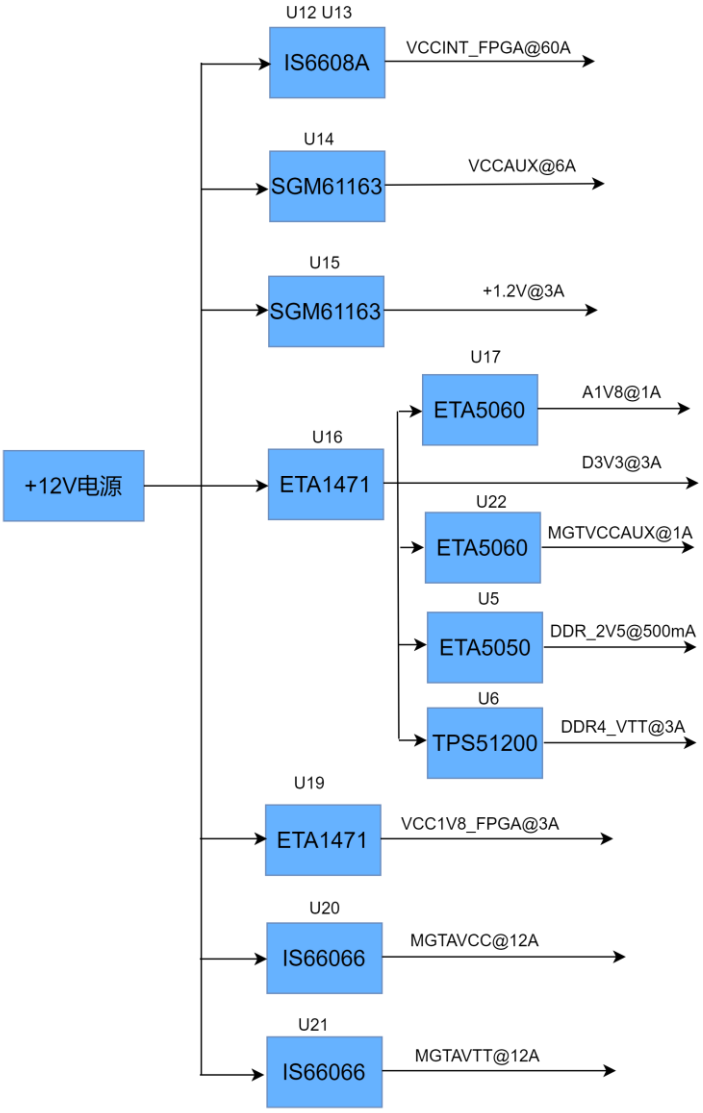

Figure 14: Power interface part in the schematic diagram

The +12V generates the FPGA core power supply through the DCDC power supply chip IS6608, and the output current is up to 60A, which can meet the current demand of the core voltage. The +12V power supply supplies power to the FPGA auxiliary power supply and the high-speed transceiver through three DCDC chips: SGM61163 generates VCCAUX, and IS66066 generates MGTAVCC and MGTAVTT power supplies. At the same time, the +12V power supply generates +1.2V through the DCDC chips ETA1471 and SGM61163. The VCC1V8_FPGA and D3V3 power supplies power to the BANK and peripherals of DDR4 and FPGA. In addition, D3V3 generates the auxiliary power supply of the high-speed transceiver and the ADC power supply +1.8V of the FPGA through two LDO chips ETA5060; the VTT and DDR2V5 voltages of DDR4 are generated by TPS51200 and ETA5050.

Because the power supply of FPGA has the requirement of power-on sequence, in the circuit design, we have designed according to the power supply requirements of the chip to ensure the normal work of the chip.

Part 2.8: Structure Diagram

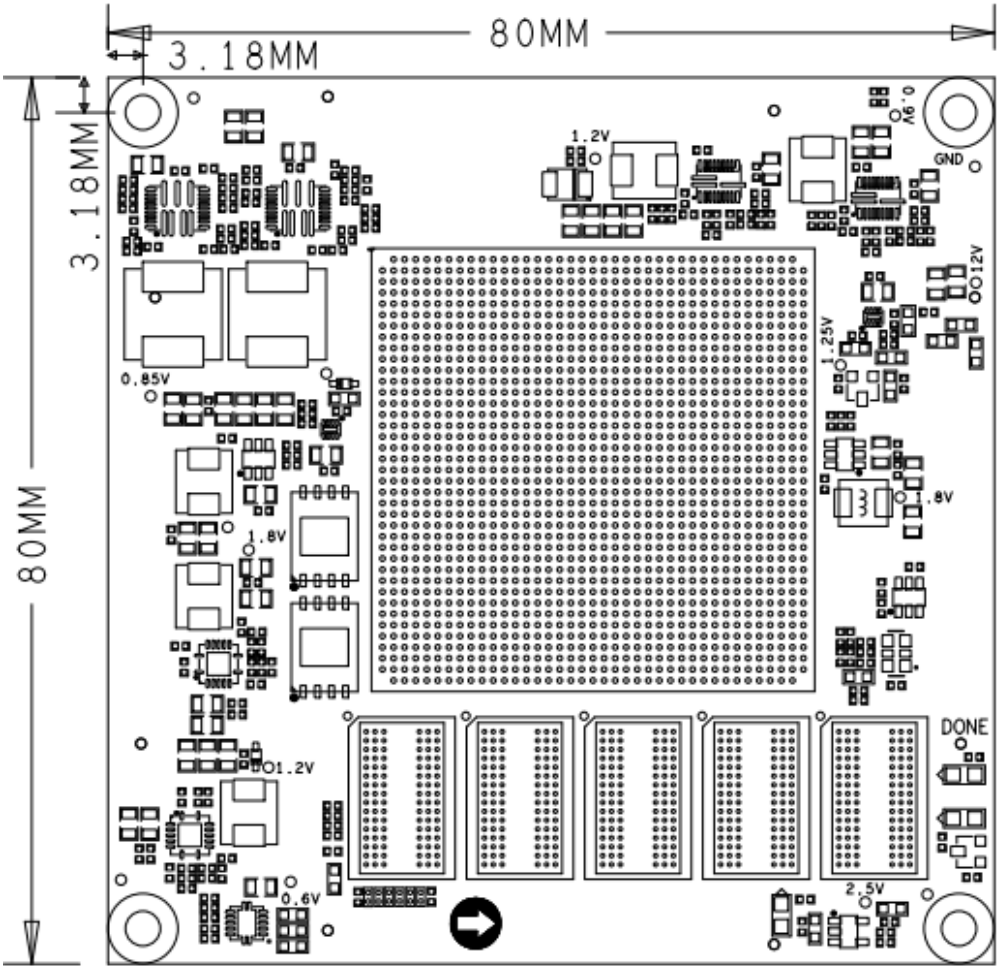

Figure 15: Top View

Part 2.9: Connector pin definition

The module is extended with four high-speed expansion ports, which are connected to the base board by four 240Pin inter-board connectors (J1 ~ J4), and the power supply of the module is input by the J3 connector.

Pin Assignments for J1 Connector:

J1 pin	Signal name	FPGA pin number	J1 pin	Signal name	FPGA pin number
A1	B90_L10_N	B4	B1	B90_L12_N	A6
A2	B90_L10_P	B5	B2	B90_L12_P	B6
A3	B90_L8_N	C4	B3	B90_L11_N	A3
A4	B90_L8_P	C5	B4	B90_L11_P	A4
A5	GND	-	B5	GND	-
A6	B90_L9_N	B2	B6	B90_L7_N	C3
A7	B90_L9_P	C2	B7	B90_L7_P	D3
A8	B90_L4_N	E1	B8	B90_L6_N	D1
A9	B90_L4_P	F1	B9	B90_L6_P	D2
A10	GND	-	B10	GND	-
A11	B90_L5_N	D5	B11	B90_L3_N	F2
A12	B90_L5_P	D6	B12	B90_L3_P	F3
A13	B90_L1_N	E4	B13	B90_L2_N	E3
A14	B90_L1_P	E5	B14	B90_L2_P	F4
A15	GND	-	B15	GND	-
A16	B91_L11_N	A9	B16	B91_L9_N	A7
A17	B91_L11_P	B10	B17	B91_L9_P	B7
A18	B91_L12_N	A11	B18	B91_L10_N	A8
A19	B91_L12_P	B11	B19	B91_L10_P	B9
A20	GND	-	B20	GND	-
A21	B91_L7_N	C7	B21	B91_L5_N	D7
A22	B91_L7_P	C8	B22	B91_L5_P	D8
A23	B91_L3_N	E8	B23	B91_L1_N	E6
A24	B91_L3_P	F9	B24	B91_L1_P	F6
A25	GND	-	B25	GND	-
A26	B91_L8_N	C9	B26	B91_L2_N	F7
A27	B91_L8_P	C10	B27	B91_L2_P	F8
A28	B91_L6_N	D10	B28	B91_L4_N	E9
A29	B91_L6_P	D11	B29	B91_L4_P	E10
A30	GND	-	B30	GND	-
A31	B93_L12_N	K10	B31	B93_L10_N	K13
A32	B93_L12_P	K11	B32	B93_L10_P	L13
A33	B93_L7_N	L14	B33	B93_L11_N	L11
A34	B93_L7_P	M14	B34	B93_L11_P	L12
A35	GND	-	B35	GND	-
A36	B93_L9_N	M10	B36	B93_L8_N	M11
A37	B93_L9_P	N10	B37	B93_L8_P	M12
A38	B93_L3_N	P12	B38	B93_L4_N	P10
A39	B93_L3_P	P13	B39	B93_L4_P	P11
A40	GND	-	B40	GND	-
A41	B93_L6_N	N12	B41	B93_L2_N	R13
A42	B93_L6_P	N13	B42	B93_L2_P	R14
A43	B93_L5_N	N14	B43	B93_L1_N	P15
A44	B93_L5_P	N15	B44	B93_L1_P	R15
A45	GND	-	B45	GND	-

A46	GND	-	B46	GND	-
A47	MGT227_CLK0_P	AE12	B47	MGT227_CLK1_P	AD10
A48	MGT227_CLK0_N	AE11	B48	MGT227_CLK1_N	AD9
A49	GND	-	B49	GND	-
A50	MGT227_RX3_P	AD2	B50	MGT227_TX3_P	AD6
A51	MGT227_RX3_N	AD1	B51	MGT227_TX3_N	AD5
A52	GND	-	B52	GND	-
A53	MGT227_RX2_P	AE4	B53	MGT227_TX2_P	AE8
A54	MGT227_RX2_N	AE3	B54	MGT227_TX2_N	AE7
A55	GND	-	B55	GND	-
A56	MGT227_RX1_P	AF2	B56	MGT227_TX1_P	AF6
A57	MGT227_RX1_N	AF1	B57	MGT227_TX1_N	AF5
A58	GND	-	B58	GND	-
A59	MGT227_RX0_P	AG4	B59	MGT227_TX0_P	AG8
A60	MGT227_RX0_N	AG3	B60	MGT227_TX0_N	AG7

Table 7: Pin Assignments for J1 Connector

J1 pin	Signal name	FPGA pin number	J1 pin	Signal name	FPGA pin number
C1	MGT231_CLK0_P	U12	D1	MGT231_CLK1_P	T10
C2	MGT231_CLK0_N	U11	D2	MGT231_CLK1_N	T9
C3	GND	-	D3	GND	-
C4	MGT231_RX3_P	H2	D4	MGT231_TX3_P	H6
C5	MGT231_RX3_N	H1	D5	MGT231_TX3_N	H5
C6	GND	-	D6	GND	-
C7	MGT231_RX2_P	J4	D7	MGT231_TX2_P	J8
C8	MGT231_RX2_N	J3	D8	MGT231_TX2_N	J7
C9	GND	-	D9	GND	-
C10	MGT231_RX1_P	K2	D10	MGT231_TX1_P	K6
C11	MGT231_RX1_N	K1	D11	MGT231_TX1_N	K5
C12	GND	-	D12	GND	-
C13	MGT231_RX0_P	L4	D13	MGT231_TX0_P	L8
C14	MGT231_RX0_N	L3	D14	MGT231_TX0_N	L7
C15	GND	-	D15	GND	-
C16	MGT230_RX3_P	M2	D16	MGT230_TX3_P	M6
C17	MGT230_RX3_N	M1	D17	MGT230_TX3_N	M5
C18	GND	-	D18	GND	-
C19	MGT230_RX2_P	N4	D19	MGT230_TX2_P	N8
C20	MGT230_RX2_N	N3	D20	MGT230_TX2_N	N7
C21	GND	-	D21	GND	-
C22	MGT230_RX1_P	P2	D22	MGT230_TX1_P	P6
C23	MGT230_RX1_N	P1	D23	MGT230_TX1_N	P5
C24	GND	-	D24	GND	-
C25	MGT230_RX0_P	R4	D25	MGT230_TX0_P	R8
C26	MGT230_RX0_N	R3	D26	MGT230_TX0_N	R7
C27	GND	-	D27	GND	-
C28	MGT230_CLK1_P	V10	D28	MGT230_CLK0_P	W12
C29	MGT230_CLK1_N	V9	D29	MGT230_CLK0_N	W11
C30	GND	-	D30	GND	-

C31	MGT229_RX3_P	T2	D31	MGT229_TX3_P	T6
C32	MGT229_RX3_N	T1	D32	MGT229_TX3_N	T5
C33	GND	-	D33	GND	-
C34	MGT229_RX2_P	U4	D34	MGT229_TX2_P	U8
C35	MGT229_RX2_N	U3	D35	MGT229_TX2_N	U7
C36	GND	-	D36	GND	-
C37	MGT229_RX1_P	V2	D37	MGT229_TX1_P	V6
C38	MGT229_RX1_N	V1	D38	MGT229_TX1_N	V5
C39	GND	-	D39	GND	-
C40	MGT229_RX0_P	W4	D40	MGT229_TX0_P	W8
C41	MGT229_RX0_N	W3	D41	MGT229_TX0_N	W7
C42	GND	-	D42	GND	-
C43	MGT229_CLK1_P	Y10	D43	MGT229_CLK0_P	AA12
C44	MGT229_CLK1_N	Y9	D44	MGT229_CLK0_N	AA11
C45	GND	-	D45	GND	-
C46	GND	-	D46	GND	-
C47	MGT228_RX3_P	Y2	D47	MGT228_TX3_P	Y6
C48	MGT228_RX3_N	Y1	D48	MGT228_TX3_N	Y5
C49	GND	-	D49	GND	-
C50	MGT228_RX2_P	AA4	D50	MGT228_TX2_P	AA8
C51	MGT228_RX2_N	AA3	D51	MGT228_TX2_N	AA7
C52	GND	-	D52	GND	-
C53	MGT228_RX1_P	AB2	D53	MGT228_TX1_P	AB6
C54	MGT228_RX1_N	AB1	D54	MGT228_TX1_N	AB5
C55	GND	-	D55	GND	-
C56	MGT228_RX0_P	AC4	D56	MGT228_TX0_P	AC8
C57	MGT228_RX0_N	AC3	D57	MGT228_TX0_N	AC7
C58	GND	-	D58	GND	-
C59	MGT228_CLK0_P	AC12	D59	MGT228_CLK1_P	AB10
C60	MGT228_CLK0_N	AC11	D60	MGT228_CLK1_N	AB9

Table 8: Pin Assignments for J1 Connector

Pin Assignments for J2 Connector:

J2 pin	Signal name	FPGA pin number	J2 pin	Signal name	FPGA pin number
A1	FPGA_VP_IN	W20	B1	FPGA_TDI	AG24
A2	FPGA_VN_IN	Y19	B2	FPGA_TDO	AG27
A3	GND	-	B3	GND	-
A4	B64_L1_P	AU22	B4	B64_L19_P	AH21
A5	B64_L1_N	AV22	B5	B64_L19_N	AJ21
A6	GND	-	B6	GND	-
A7	B64_L21_P	AJ20	B7	B64_L10_P	AK21
A8	B64_L21_N	AJ19	B8	B64_L10_N	AL21
A9	GND	-	B9	GND	-
A10	B64_L8_P	AL22	B10	B65_L17_P	AJ16
A11	B64_L8_N	AM22	B11	B65_L17_N	AJ15
A12	GND	-	B12	GND	-
A13	B65_L18_P	AK16	B13	B65_L16_P	AK17

A14	B65_L18_N	AL16	B14	B65_L16_N	AL17
A15	GND	-	B15	GND	-
A16	B65_L20_P	AN13	B16	B65_L14_P	AM15
A17	B65_L20_N	AP13	B17	B65_L14_N	AN15
A18	GND	-	B18	GND	-
A19	B65_L11_P	AR14	B19	B65_L10_P	AP16
A20	B65_L11_N	AT14	B20	B65_L10_N	AR16
A21	GND	-	B21	GND	-
A22	B65_L7_P	AV16	B22	B65_L8_P	AT15
A23	B65_L7_N	AW16	B23	B65_L8_N	AU15
A24	GND	-	B24	GND	-
A25	B65_L9_P	AV15	B25	B65_L6_P	AU14
A26	B65_L9_N	AW15	B26	B65_L6_N	AU13
A27	GND	-	B27	GND	-
A28	VCCIO_64	AK20、AN19、AT8	B28	B65_T2U	AN16
A29	VCCIO_65	AK15、AN14、AT13	B29	B65_T3U	AP10
A30	GND	-	B30	GND	-
A31	B65_L5_P	AV13	B31	B65_L3_P	AW14
A32	B65_L5_N	AV12	B32	B65_L3_N	AW13
A33	GND	-	B33	GND	-
A34	B65_L12_P	AP15	B34	B65_L24_P	AM14
A35	B65_L12_N	AP14	B35	B65_L24_N	AM13
A36	GND	-	B36	GND	-
A37	B65_L13_P	AL15	B37	B65_L15_P	AJ14
A38	B65_L13_N	AL14	B38	B65_L15_N	AK14
A39	GND	-	B39	GND	-
A40	B65_L1_P	AW11	B40	B65_L4_P	AU10
A41	B65_L1_N	AW10	B41	B65_L4_N	AV10
A42	GND	-	B42	GND	-
A43	B65_L19_P	AT12	B43	B65_L23_P	AP11
A44	B65_L19_N	AT11	B44	B65_L23_N	AR11
A45	GND	-	B45	GND	-
A46	GND	-	B46	GND	-
A47	MGT225_RX0_P	AR4	B47	MGT225_TX0_P	AR8
A48	MGT225_RX0_N	AR3	B48	MGT225_TX0_N	AR7
A49	GND	-	B49	GND	-
A50	MGT225_RX1_P	AP2	B50	MGT225_TX1_P	AP6
A51	MGT225_RX1_N	AP1	B51	MGT225_TX1_N	AP5
A52	GND	-	B52	GND	-
A53	MGT225_RX2_P	AN4	B53	MGT225_TX2_P	AN8
A54	MGT225_RX2_N	AN3	B54	MGT225_TX2_N	AN7
A55	GND	-	B55	GND	-
A56	MGT225_RX3_P	AM2	B56	MGT225_TX3_P	AM6
A57	MGT225_RX3_N	AM1	B57	MGT225_TX3_N	AM5
A58	GND	-	B58	GND	-
A59	MGT225_CLK0_P	AJ12	B59	MGT225_CLK1_P	AH10
A60	MGT225_CLK0_N	AJ11	B60	MGT225_CLK1_N	AH9

Table 9: Pin Assignments for J2 Connector

J2 pin	Signal name	FPGA pin number	J2 pin	Signal name	FPGA pin number
C1	FPGA_TMS	AD22	D1	B64_L9_P	AP21
C2	FPGA_TCK	AG23	D2	B64_L9_N	AP20
C3	GND	-	D3	GND	-
C4	B64_L5_P	AT22	D4	B64_L7_P	AR22
C5	B64_L5_N	AT21	D5	B64_L7_N	AR21
C6	GND	-	D6	GND	-
C7	B64_L3_P	AV21	D7	B64_L15_P	AT20
C8	B64_L3_N	AW21	D8	B64_L15_N	AT19
C9	GND	-	D9	GND	-
C10	B64_L12_P	AL20	D10	B64_L2_P	AU20
C11	B64_L12_N	AM20	D11	B64_L2_N	AV20
C12	GND	-	D12	GND	-
C13	B64_L11_P	AN21	D13	B64_L17_P	AU19
C14	B64_L11_N	AN20	D14	B64_L17_N	AU18
C15	GND	-	D15	GND	-
C16	B64_L20_P	AL19	D16	B64_L4_P	AW20
C17	B64_L20_N	AM19	D17	B64_L4_N	AW19
C18	GND	-	D18	GND	-
C19	B64_L13_P	AP19	D19	B64_L6_P	AV18
C20	B64_L13_N	AR19	D20	B64_L6_N	AW18
C21	GND	-	D21	GND	-
C22	B64_L14_P	AN18	D22	B64_L16_P	AT17
C23	B64_L14_N	AP18	D23	B64_L16_N	AU17
C24	GND	-	D24	GND	-
C25	B64_L24_P	AM18	D25	B64_L18_P	AR18
C26	B64_L24_N	AM17	D26	B64_L18_N	AR17
C27	GND	-	D27	GND	-
C28	B64_L22_P	AK19	D28	B64_L23_P	AH18
C29	B64_L22_N	AK18	D29	B64_L23_N	AJ18
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-
C32	MGT224_CLK0_P	AM10	D32	MGT224_CLK1_P	AK10
C33	MGT224_CLK0_N	AM9	D33	MGT224_CLK1_N	AK9
C34	GND	-	D34	GND	-
C35	MGT224_RX3_P	AT2	D35	MGT224_TX3_P	AT6
C36	MGT224_RX3_N	AT1	D36	MGT224_TX3_N	AT5
C37	GND	-	D37	GND	-
C38	MGT224_RX2_P	AU4	D38	MGT224_TX2_P	AU8
C39	MGT224_RX2_N	AU3	D39	MGT224_TX2_N	AU7
C40	GND	-	D40	GND	-
C41	MGT224_RX0_P	AW4	D41	MGT224_TX0_P	AW8
C42	MGT224_RX0_N	AW3	D42	MGT224_TX0_N	AW7
C43	GND	-	D43	GND	-
C44	MGT224_RX1_P	AV2	D44	MGT224_TX1_P	AV6
C45	MGT224_RX1_N	AV1	D45	MGT224_TX1_N	AV5
C46	GND	-	D46	GND	-

C47	MGT226_CLK0_P	AG12	D47	MGT226_CLK1_P	AF10
C48	MGT226_CLK0_N	AG11	D48	MGT226_CLK1_N	AF9
C49	GND	-	D49	GND	-
C50	MGT226_RX0_P	AL4	D50	MGT226_TX0_P	AL8
C51	MGT226_RX0_N	AL3	D51	MGT226_TX0_N	AL7
C52	GND	-	D52	GND	-
C53	MGT226_RX1_P	AK2	D53	MGT226_TX1_P	AK6
C54	MGT226_RX1_N	AK1	D54	MGT226_TX1_N	AK5
C55	GND	-	D55	GND	-
C56	MGT226_RX2_P	AJ4	D56	MGT226_TX2_P	AJ8
C57	MGT226_RX2_N	AJ3	D57	MGT226_TX2_N	AJ7
C58	GND	-	D58	GND	-
C59	MGT226_RX3_P	AH2	D59	MGT226_TX3_P	AH6
C60	MGT226_RX3_N	AH1	D60	MGT226_TX3_N	AH5

Table 10: Pin Assignments for J2 Connector

Pin assignment for J3 connector:

J3 pin	Signal name	FPGA pin number	J3 pin	Signal name	FPGA pin number
A1	+12V	-	B1	+12V	-
A2	+12V	-	B2	+12V	-
A3	GND	-	B3	GND	-
A4	FMC1_VREF_A_M2C_1	M27	B4	VCCIO_71	B18、E17、H16
A5	VCCAUX_PG	-	B5	FMC1_VREF_A_M2C_2	M24
A6	GND	-	B6	GND	-
A7	MGT131_RX3_P	J38	B7	MGT131_TX3_P	E33
A8	MGT131_RX3_N	J39	B8	MGT131_TX3_N	E34
A9	GND	-	B9	GND	-
A10	MGT131_RX2_P	K36	B10	MGT131_TX2_P	F35
A11	MGT131_RX2_N	K37	B11	MGT131_TX2_N	F36
A12	GND	-	B12	GND	-
A13	MGT131_RX1_P	L38	B13	MGT131_TX1_P	G33
A14	MGT131_RX1_N	L39	B14	MGT131_TX1_N	G34
A15	GND	-	B15	GND	-
A16	MGT131_RX0_P	M36	B16	MGT131_TX0_P	J33
A17	MGT131_RX0_N	M37	B17	MGT131_TX0_N	J34
A18	GND	-	B18	GND	-
A19	MGT131_CLK0_P	T27	B19	MGT131_CLK1_P	R29
A20	MGT131_CLK0_N	T28	B20	MGT131_CLK1_N	R30
A21	GND	-	B21	GND	-
A22	MGT129_RX3_P	U38	B22	MGT129_TX3_P	R33
A23	MGT129_RX3_N	U39	B23	MGT129_TX3_N	R34
A24	GND	-	B24	GND	-
A25	MGT129_RX2_P	V36	B25	MGT129_TX2_P	T31
A26	MGT129_RX2_N	V37	B26	MGT129_TX2_N	T32
A27	GND	-	B27	GND	-
A28	MGT129_RX1_P	W38	B28	MGT129_TX1_P	U33

A29	MGT129_RX1_N	W39	B29	MGT129_TX1_N	U34
A30	GND	-	B30	GND	-
A31	MGT129_RX0_P	Y36	B31	MGT129_TX0_P	V31
A32	MGT129_RX0_N	Y37	B32	MGT129_TX0_N	V32
A33	GND	-	B33	GND	-
A34	MGT129_CLK0_P	Y27	B34	MGT129_CLK1_P	W29
A35	MGT129_CLK0_N	Y28	B35	MGT129_CLK1_N	W30
A36	GND	-	B36	GND	-
A37	MGT127_CLK0_P	AE29	B37	MGT127_CLK1_P	AC29
A38	MGT127_CLK0_N	AE30	B38	MGT127_CLK1_N	AC30
A39	GND	-	B39	GND	-
A40	MGT127_RX3_P	AE38	B40	MGT127_TX3_P	AC33
A41	MGT127_RX3_N	AE39	B41	MGT127_TX3_N	AC34
A42	GND	-	B42	GND	-
A43	MGT127_RX2_P	AF36	B43	MGT127_TX2_P	AD31
A44	MGT127_RX2_N	AF37	B44	MGT127_TX2_N	AD32
A45	GND	-	B45	GND	-
A46	MGT127_RX1_P	AG38	B46	MGT127_TX1_P	AE33
A47	MGT127_RX1_N	AG39	B47	MGT127_TX1_N	AE34
A48	GND	-	B48	GND	-
A49	MGT127_RX0_P	AH36	B49	MGT127_TX0_P	AF31
A50	MGT127_RX0_N	AH37	B50	MGT127_TX0_N	AF32
A51	GND	-	B51	GND	-
A52	FMC2_VREF_A_M2C_1	AH20	B52	GND	-
A53	FMC2_VREF_A_M2C_2	AH16	B53	GND	-
A54	GND	-	B54	GND	-
A55	GND	-	B55	+12V	-
A56	GND	-	B56	+12V	-
A57	+12V	-	B57	GND	-
A58	+12V	-	B58	VCCIO_71	B18、E17、H16
A59	GND	-	B59	FMC1_VREF_A_M2C_2	M24
A60	FMC1_VREF_A_M2C_1	M27	B60	GND	-

Table 11: Pin Assignments for J3 Connector

J3 pin	Signal name	FPGA pin number	J3 pin	Signal name	FPGA pin number
C1	+12V	-	D1	+12V	-
C2	+12V	-	D2	+12V	-
C3	GND	-	D3	GND	-
C4	VCCIO_70	B23、E22、H21	D4	VCCIO_69	B28、E27、H26
C5	FMC1_VREF_A_M2C_3	M17	D5	GND	-
C6	GND	-	D6	MGT132_TX3_P	A33
C7	MGT132_RX3_P	C38	D7	MGT132_TX3_N	A34
C8	MGT132_RX3_N	C39	D8	GND	-
C9	GND	-	D9	MGT132_TX2_P	B35
C10	MGT132_RX2_P	E38	D10	MGT132_TX2_N	B36
C11	MGT132_RX2_N	E39	D11	GND	-
C12	GND	-	D12	MGT132_TX1_P	C33
C13	MGT132_RX1_P	G38	D13	MGT132_TX1_N	C34

C14	MGT132_RX1_N	G39	D14	GND	-
C15	GND	-	D15	MGT132_TX0_P	D35
C16	MGT132_RX0_P	H36	D16	MGT132_TX0_N	D36
C17	MGT132_RX0_N	H37	D17	GND	-
C18	GND	-	D18	MGT132_CLK1_P	N29
C19	MGT132_CLK0_P	P27	D19	MGT132_CLK1_N	N30
C20	MGT132_CLK0_N	P28	D20	GND	-
C21	GND	-	D21	MGT130_TX3_P	L33
C22	MGT130_RX3_P	N38	D22	MGT130_TX3_N	L34
C23	MGT130_RX3_N	N39	D23	GND	-
C24	GND	-	D24	MGT130_TX2_P	M31
C25	MGT130_RX2_P	P36	D25	MGT130_TX2_N	M32
C26	MGT130_RX2_N	P37	D26	GND	-
C27	GND	-	D27	MGT130_TX1_P	N33
C28	MGT130_RX1_P	R38	D28	MGT130_TX1_N	N34
C29	MGT130_RX1_N	R39	D29	GND	-
C30	GND	-	D30	MGT130_TX0_P	P31
C31	MGT130_RX0_P	T36	D31	MGT130_TX0_N	P32
C32	MGT130_RX0_N	T37	D32	GND	-
C33	GND	-	D33	MGT130_CLK1_P	U29
C34	MGT130_CLK0_P	V27	D34	MGT130_CLK1_N	U30
C35	MGT130_CLK0_N	V28	D35	GND	-
C36	GND	-	D36	MGT128_CLK1_P	AA29
C37	MGT128_CLK0_P	AB27	D37	MGT128_CLK1_N	AA30
C38	MGT128_CLK0_N	AB28	D38	GND	-
C39	GND	-	D39	MGT128_TX3_P	W33
C40	MGT128_RX3_P	AA38	D40	MGT128_TX3_N	W34
C41	MGT128_RX3_N	AA39	D41	GND	-
C42	GND	-	D42	MGT128_TX2_P	Y31
C43	MGT128_RX2_P	AB36	D43	MGT128_TX2_N	Y32
C44	MGT128_RX2_N	AB37	D44	GND	-
C45	GND	-	D45	MGT128_TX1_P	AA33
C46	MGT128_RX1_P	AC38	D46	MGT128_TX1_N	AA34
C47	MGT128_RX1_N	AC39	D47	GND	-
C48	GND	-	D48	MGT128_TX0_P	AB31
C49	MGT128_RX0_P	AD36	D49	MGT128_TX0_N	AB32
C50	MGT128_RX0_N	AD37	D50	GND	-
C51	GND	-	D51	GND	-
C52	GND	-	D52	GND	-
C53	GND	-	D53	GND	-
C54	GND	-	D54	+12V	-
C55	+12V	-	D55	+12V	-
C56	+12V	-	D56	GND	-
C57	GND	-	D57	VCCIO_69	B28、E27、H26
C58	VCCIO_70	B23、E22、H21	D58	GND	-
C59	FMC1_VREF_A_M2C_3	M17	D59	MGT132_TX3_P	A33
C60	GND	-	D60	MGT132_TX3_N	A34

Table 12: Pin Assignments for J3 Connector

Pin assignments for the J4 connector:

J4 pin	Signal name	FPGA pin number	J4 pin	Signal name	FPGA pin number
A1	VCCO_90_91_93_94	E2、F5、B8、F10、K12、N11、B13、G13	B1	POWER_SCL	-
A2	GND	-	B2	GND	-
A3	B94_L9_N	C12	B3	B94_L6_N	E11
A4	B94_L9_P	D12	B4	B94_L6_P	F11
A5	B94_L8_N	D13	B5	B94_L7_N	F12
A6	B94_L8_P	E13	B6	B94_L7_P	F13
A7	GND	-	B7	GND	-
A8	B71_L1_N	M15	B8	B71_L10_N	F14
A9	B71_L1_P	M16	B9	B71_L10_P	G15
A10	GND	-	B10	GND	-
A11	B71_L18_N	D15	B11	B71_L4_N	L16
A12	B71_L18_P	D16	B12	B71_L4_P	L17
A13	GND	-	B13	GND	-
A14	B71_L6_N	K14	B14	B71_L5_N	J16
A15	B71_L6_P	K15	B15	B71_L5_P	K16
A16	GND	-	B16	GND	-
A17	B71_L14_N	F16	B17	B71_L11_N	G16
A18	B71_L14_P	F17	B18	B71_L11_P	G17
A19	GND	-	B19	GND	-
A20	B70_L11_N	F21	B20	B70_L20_N	B20
A21	B70_L11_P	G21	B21	B70_L20_P	C20
A22	GND	-	B22	GND	-
A23	B70_L2_N	M20	B23	B70_L18_N	D20
A24	B70_L2_P	M19	B24	B70_L18_P	E20
A25	GND	-	B25	GND	-
A26	B70_L6_N	K21	B26	B70_L1_N	M22
A27	B70_L6_P	K20	B27	B70_L1_P	M21
A28	GND	-	B28	GND	-
A29	B70_L7_N	H22	B29	B70_L8_N	J21
A30	B70_L7_P	J22	B30	B70_L8_P	J20
A31	GND	-	B31	GND	-
A32	B70_L4_N	L22	B32	B70_L17_N	D21
A33	B70_L4_P	L21	B33	B70_L17_P	E21
A34	GND	-	B34	GND	-
A35	B70_L3_N	L24	B35	B70_L16_N	D23
A36	B70_L3_P	L23	B36	B70_L16_P	D22
A37	GND	-	B37	GND	-
A38	B70_L14_N	E24	B38	B70_L15_N	D25
A39	B70_L14_P	E23	B39	B70_L15_P	E25
A40	GND	-	B40	GND	-
A41	B70_L13_N	F24	B41	B70_L9_N	G24
A42	B70_L13_P	F23	B42	B70_L9_P	H24
A43	GND	-	B43	GND	-

A44	B69_L3_N	L27	B44	B69_L1_N	M26
A45	B69_L3_P	L26	B45	B69_L1_P	M25
A46	GND	-	B46	GND	-
A47	B69_L5_N	J26	B47	B69_L4_N	H25
A48	B69_L5_P	K26	B48	B69_L4_P	J25
A49	GND	-	B49	GND	-
A50	B69_L2_N	H27	B50	B69_L11_N	F27
A51	B69_L2_P	J27	B51	B69_L11_P	G27
A52	GND	-	B52	GND	-
A53	B69_L24_N	A29	B53	B69_L9_N	H28
A54	B69_L24_P	A28	B54	B69_L9_P	J28
A55	GND	-	B55	GND	-
A56	B69_L16_N	D30	B56	B69_L8_N	H30
A57	B69_L16_P	E30	B57	B69_L8_P	H29
A58	GND	-	B58	GND	-
A59	B69_L15_N	D31	B59	B69_L7_N	J31
A60	B69_L15_P	E31	B60	B69_L7_P	J30

Table 13: Pin Assignments for J4 Connector

J4 pin	Signal name	FPGA pin number	J4 pin	Signal name	FPGA pin number
C1	POWER_SDA	-	D1	POWER_ALT	-
C2	GND	-	D2	GND	-
C3	B94_L4_N	G10	D3	B94_L2_N	J10
C4	B94_L4_P	H10	D4	B94_L2_P	J11
C5	B94_L1_N	J12	D5	B94_L3_N	H12
C6	B94_L1_P	J13	D6	B94_L3_P	H13
C7	GND	-	D7	GND	-
C8	B71_L16_N	E15	D8	B71_L24_N	A16
C9	B71_L16_P	E16	D9	B71_L24_P	B17
C10	GND	-	D10	GND	-
C11	B71_L20_N	C14	D11	B71_L23_N	A17
C12	B71_L20_P	C15	D12	B71_L23_P	A18
C13	GND	-	D13	GND	-
C14	B71_L22_N	B15	D14	B71_L9_N	G14
C15	B71_L22_P	B16	D15	B71_L9_P	H14
C16	GND	-	D16	GND	-
C17	B71_L7_N	H15	D17	B71_L8_N	H17
C18	B71_L7_P	J15	D18	B71_L8_P	H18
C19	GND	-	D19	GND	-
C20	B71_L13_N	F18	D20	B71_L12_N	G19
C21	B71_L13_P	F19	D21	B71_L12_P	H19
C22	GND	-	D22	GND	-
C23	B71_L3_N	K18	D23	B71_L19_N	C17
C24	B71_L3_P	L18	D24	B71_L19_P	C18
C25	GND	-	D25	GND	-
C26	B71_L21_N	A19	D26	B71_L17_N	D17
C27	B71_L21_P	B19	D27	B71_L17_P	D18
C28	GND	-	D28	GND	-

C29	B71_L2_N	K19	D29	B71_L15_N	E18
C30	B71_L2_P	L19	D30	B71_L15_P	E19
C31	GND	-	D31	GND	-
C32	B70_L10_N	G20	D32	B70_L21_N	A21
C33	B70_L10_P	H20	D33	B70_L21_P	B21
C34	GND	-	D34	GND	-
C35	B70_L12_N	F22	D35	B70_L22_N	A22
C36	B70_L12_P	G22	D36	B70_L22_P	B22
C37	GND	-	D37	GND	-
C38	B70_L24_N	A24	D38	B70_L5_N	K24
C39	B70_L24_P	A23	D39	B70_L5_P	K23
C40	GND	-	D40	GND	-
C41	B70_L19_N	C23	D41	B70_L23_N	B25
C42	B70_L19_P	C22	D42	B70_L23_P	B24
C43	GND	-	D43	GND	-
C44	B69_L6_N	G26	D44	B69_L13_N	F29
C45	B69_L6_P	G25	D45	B69_L13_P	F28
C46	GND	-	D46	GND	-
C47	B69_L17_N	D26	D47	B69_L14_N	E29
C48	B69_L17_P	E26	D48	B69_L14_P	E28
C49	GND	-	D49	GND	-
C50	B69_L18_N	D28	D50	B69_L22_N	A27
C51	B69_L18_P	D27	D51	B69_L22_P	B27
C52	GND	-	D52	GND	-
C53	B69_L20_N	C28	D53	B69_L19_N	B29
C54	B69_L20_P	C27	D54	B69_L19_P	C29
C55	GND	-	D55	GND	-
C56	B69_L12_N	G30	D56	B69_L23_N	A26
C57	B69_L12_P	G29	D57	B69_L23_P	B26
C58	GND	-	D58	GND	-
C59	B69_L10_N	F31	D59	B69_L21_N	A31
C60	B69_L10_P	G31	D60	B69_L21_P	B31

Table 14: Pin Assignments for J4 Connector

Part 3: Base board

Part 3.1: Introduction

Through the previous function introduction, we can understand the functions of the base board.

- PCIe3.0 x16 interface
- 1 * Gigabit network interface
- 2 * FMC HPC interface
- 2 * MIPI input interface
- USB Uart interface
- Micro SD deck
- 2 * STATA interface
- 40-pin expansion port
- JTAG debug port
- Led light
- Key

Part 3.2: PCIe Slot

There is a PCIe x16 interface on the AXKU15 base board, which supports PCIe Gen3.0 protocol, and 8 pairs of transceivers are connected to the golden finger of PCIEx16 for data communication.

The receiving and transmitting signals of the PCIe interface are directly connected to the FPGA BANK228 ~ 231 transceivers. The 16-channel TX signals and RX signals are connected to the FPGA transceivers in the form of differential signals. The communication rate of a single channel can be as high as 8G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 16 below, in which the TX transmission signal is connected in AC coupling mode.

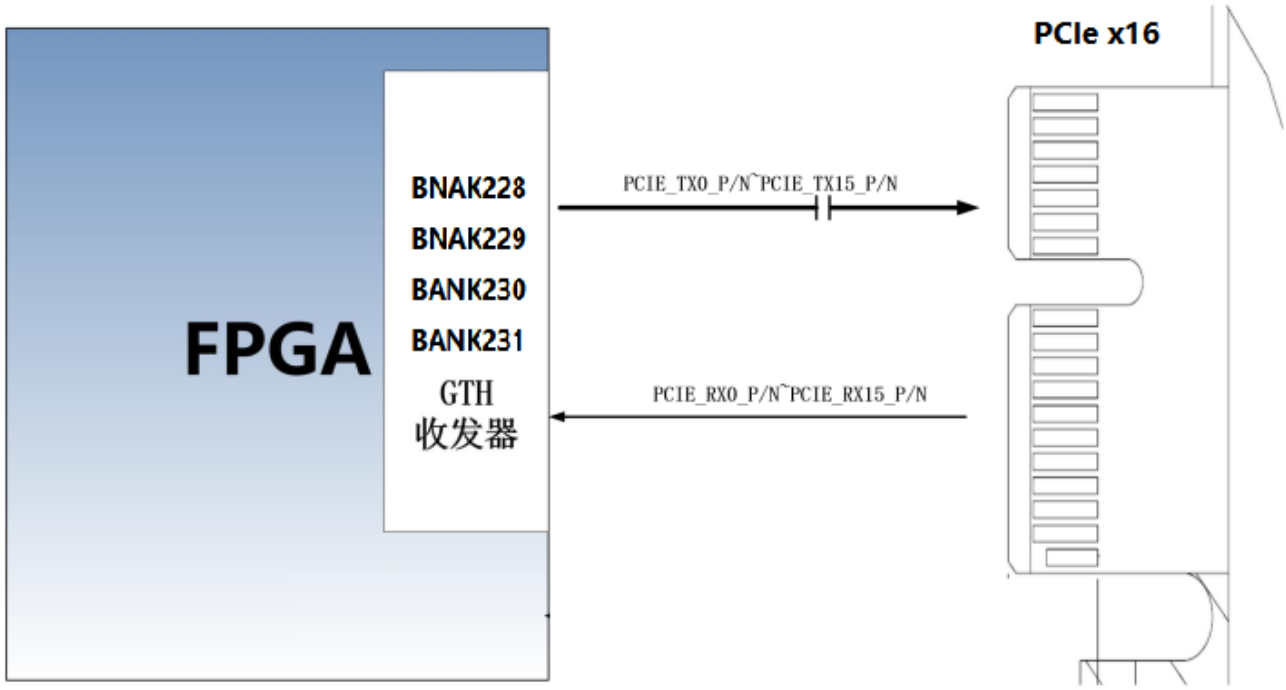

Figure 16: Schematic Diagram of PCIe Slot Design

The PCIe x16 interface FPGA pin assignments are as follows:

Signal name	FPGA pin name	Pin number	Remark
PCIE_RX0_P	MGT231_RX3_P	H2	PCIE channel 0 data receiving positive
PCIE_RX0_N	MGT231_RX3_N	H1	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	MGT231_RX2_P	J4	PCIE channel 1 data receiving positive
PCIE_RX1_N	MGT231_RX2_N	J3	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	MGT231_RX1_P	K2	PCIE channel 2 data receiving positive
PCIE_RX2_N	MGT231_RX1_N	K1	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	MGT231_RX0_P	L4	PCIE channel 3 data receiving positive
PCIE_RX3_N	MGT231_RX0_N	L3	PCIE Channel 3 Data Receive Negative
PCIE_RX4_P	MGT230_RX3_P	M2	PCIE Channel 4 Data Reception Positive
PCIE_RX4_N	MGT230_RX3_N	M1	PCIE Channel 4 Data Receive Negative
PCIE_RX5_P	MGT230_RX2_P	N4	PCIE channel 5 data receiving positive
PCIE_RX5_N	MGT230_RX2_N	N3	PCIE Channel 5 Data Receive Negative
PCIE_RX6_P	MGT230_RX1_P	P2	PCIE channel 6 data receiving positive
PCIE_RX6_N	MGT230_RX1_N	P1	PCIE Channel 6 Data Receive Negative
PCIE_RX7_P	MGT230_RX0_P	R4	PCIE channel 7 data receiving positive
PCIE_RX7_N	MGT230_RX0_N	R3	PCIE Channel 7 Data Receive Negative
PCIE_RX8_P	MGT229_RX3_P	T2	PCIE Channel 8 Data Sending Positive
PCIE_RX8_N	MGT229_RX3_N	T1	PCIE channel 8 data transmission negative
PCIE_RX9_P	MGT229_RX2_P	U4	PCIE Channel 9 Data Sending Positive
PCIE_RX9_N	MGT229_RX2_N	U3	PCIE channel 9 data transmission negative
PCIE_RX10_P	MGT229_RX1_P	V2	PCIE Channel 10 Data Sending Positive
PCIE_RX10_N	MGT229_RX1_N	V1	PCIE channel 10 data transmission negative
PCIE_RX11_P	MGT229_RX0_P	W4	PCIE Channel 11 Data Sending Positive
PCIE_RX11_N	MGT229_RX0_N	W3	PCIE channel 11 data transmission negative
PCIE_RX12_P	MGT228_RX3_P	Y2	PCIE Channel 12 Data Sending Positive

PCIE_RX12_N	MGT228_RX3_N	Y1	PCIE channel 12 data transmission negative
PCIE_RX13_P	MGT228_RX2_P	AA4	PCIE Channel 13 Data Sending Positive
PCIE_RX13_N	MGT228_RX2_N	AA3	PCIE channel 13 data transmission negative
PCIE_RX14_P	MGT228_RX1_P	AB2	PCIE Channel 14 Data Sending Positive
PCIE_RX14_N	MGT228_RX1_N	AB1	PCIE channel 14 data transmission negative
PCIE_RX15_P	MGT228_RX0_P	AC4	PCIE Channel 15 Data Sending Positive
PCIE_RX15_N	MGT228_RX0_N	AC3	PCIE channel 15 data transmission negative
PCIE_TX0_P	MGT231_TX3_P	H6	PCIE channel 0 data sending positive
PCIE_TX0_N	MGT231_TX3_N	H5	PCIE channel 0 data transmission negative
PCIE_TX1_P	MGT231_TX2_P	J8	PCIE Channel 1 Data Sending Positive
PCIE_TX1_N	MGT231_TX2_N	J7	PCIE channel 1 data transmission negative
PCIE_TX2_P	MGT231_TX1_P	K6	PCIE Channel 2 Data Sending Positive
PCIE_TX2_N	MGT231_TX1_N	K5	PCIE channel 2 data transmission negative
PCIE_TX3_P	MGT231_TX0_P	L8	PCIE Channel 3 Data Sending Positive
PCIE_TX3_N	MGT231_TX0_N	L7	PCIE channel 3 data transmission negative
PCIE_TX4_P	MGT230_TX3_P	M6	PCIE Channel 4 Data Sending Positive
PCIE_TX4_N	MGT230_TX3_N	M5	PCIE channel 4 data transmission negative
PCIE_TX5_P	MGT230_TX2_P	N8	PCIE Channel 5 Data Sending Positive
PCIE_TX5_N	MGT230_TX2_N	N7	PCIE channel 5 data transmission negative
PCIE_TX6_P	MGT230_TX1_P	P6	PCIE Channel 6 Data Sending Positive
PCIE_TX6_N	MGT230_TX1_N	P5	PCIE channel 6 data transmission negative
PCIE_TX7_P	MGT230_TX0_P	R8	PCIE Channel 7 Data Sending Positive
PCIE_TX7_N	MGT230_TX0_N	R7	PCIE channel 7 data transmission negative
PCIE_TX8_P	MGT229_TX3_P	T6	PCIE Channel 8 Data Sending Positive
PCIE_TX8_N	MGT229_TX3_N	T5	PCIE channel 8 data transmission negative
PCIE_TX9_P	MGT229_TX2_P	U8	PCIE Channel 9 Data Sending Positive
PCIE_TX9_N	MGT229_TX2_N	U7	PCIE channel 9 data transmission negative
PCIE_TX10_P	MGT229_TX1_P	V6	PCIE Channel 10 Data Sending Positive
PCIE_TX10_N	MGT229_TX1_N	V5	PCIE channel 10 data transmission negative
PCIE_TX11_P	MGT229_TX0_P	W8	PCIE Channel 11 Data Sending Positive
PCIE_TX11_N	MGT229_TX0_N	W7	PCIE channel 11 data transmission negative
PCIE_TX12_P	MGT228_TX3_P	Y6	PCIE Channel 12 Data Sending Positive
PCIE_TX12_N	MGT228_TX3_N	Y5	PCIE channel 12 data transmission negative
PCIE_TX13_P	MGT228_TX2_P	AA8	PCIE Channel 13 Data Sending Positive
PCIE_TX13_N	MGT228_TX2_N	AA7	PCIE channel 13 data transmission negative
PCIE_TX14_P	MGT228_TX1_P	AB6	PCIE Channel 14 Data Sending Positive
PCIE_TX14_N	MGT228_TX1_N	AB5	PCIE channel 14 data transmission negative
PCIE_TX15_P	MGT228_TX0_P	AC8	PCIE Channel 15 Data Sending Positive
PCIE_TX15_N	MGT228_TX0_N	AC7	PCIE channel 15 data transmission negative
PCIE_CLK_P	MGT229_CLK0_P	AA12	PCIE channel reference clock positive
PCIE_CLK_N	MGT229_CLK0_N	AA11	PCIE channel reference clock negative
FPGA_PCIE_PERST_N	B65_T3U	AP10	PCIE reset signal

Table 15: PCIe interface pin assignment

Part 3.3: Gigabit network interface

A JL21221D Ethernet PHY chip is used on the development board to provide network communication services for users. The Ethernet PHY chip is connected to the IO interface of FPGA. JL21221D chip supports 10/100/1,000 Mbps

network transmission rate and communicates with FPGA through RGMII interface. JL21221D chip supports MDI/MDX self-adaptation, various speed self-adaptation and Master/Slave self-adaptation and supports register management of PHY by MDIO bus.

When the JL21221D is powered on, it will detect the level status of some specific IOs to determine its own working mode. Table 16 describes the default setting information after the GPHY chip is powered on.

Default configuration values of PHY chip:

Configure the Pin	Explain	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY Address for MDIO/MDC Mode	PHY Address is 001
RXD1_TXDLY	TX clock 2 ns delay	Delay
RXD0_RXDLY	RX clock 2 ns delay	Delay

Table 16: PHY chip configuration

When the network is connected to Gigabit Ethernet, the data transmission between FPGA and PHY chip JL2121 is communicated through RGMII bus. The transmission clock is 125Mhz, and the data is sampled at the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through RMII bus, and the transmission clock is 25 Mhz. Data is sampled on the rising and falling edges of the clock.

Figure 17 shows the connection between FPGA and Ethernet PHY chip:

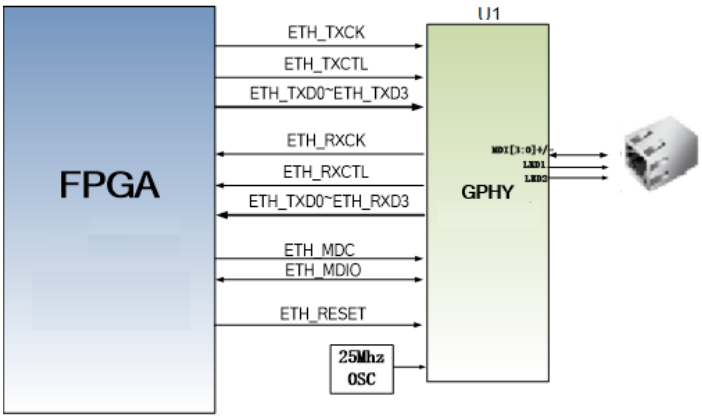

Figure 17: Connection Schematic Diagram of Gigabit Network Interface

Figure 18 is the physical diagram of the Ethernet PHY chip.

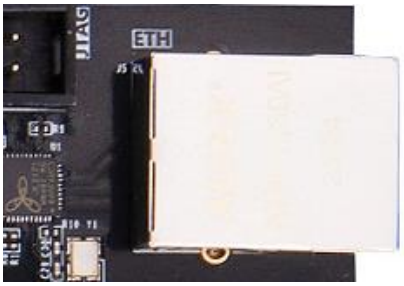

Figure 18: Physical Diagram of Ethernet PHY Chip

The FPGA pin assignments for the Ethernet PHY are as follows:

Signal name	FPGA pin number	Remark
ETH_MDC	AW10	MDIO manages the clock
ETH_MDIO	AW11	MDIO manages data
ETH_RESET	AM18	PHY chip reset
ETH_RXCK	AK17	RGMII receive clock
ETH_RXCTL	AL17	Receive data valid signal
ETH_RXD0	AL16	Receive data Bit0
ETH_RXD1	AK16	Receive data Bit1
ETH_RXD2	AU12	Receive data Bit2
ETH_RXD3	AP13	Receive data Bit3
ETH_TXCK	AR11	RGMII transmit clock
ETH_TXCTL	AN13	Send enable signal
ETH_TXD0	AJ14	Send data bit0
ETH_TXD1	AK14	Send data bit1
ETH_TXD2	AU13	Send data bit2
ETH_TXD3	AV13	Transmit data bit 3

Table 17: Ethernet PHY pin assignment

Part 3.4: FMC HPC Interface

The development board is equipped with two FMC HPC expansion ports, namely FMC1 (J12) and FMC2 (J13), which can be externally connected with XILINX or various FMC modules of Alinx (HDMI input and output module, binocular camera module, high-speed AD module, etc.).

The FMC1 expansion port includes 34 pairs of LA signal differential pairs, 2 pairs of clock signals and 24 pairs of HA signals, which are respectively connected to the FPGA chips BANK69, BANK70 and BANK71. The standard level is 1.8V by default. 8 channels of high-speed GTY transceiving signals are connected to the IO of FPGA chips BANK226 and BANK227.

The schematic diagram of the FPGA and FMC HPC connector is shown in Figure 19:

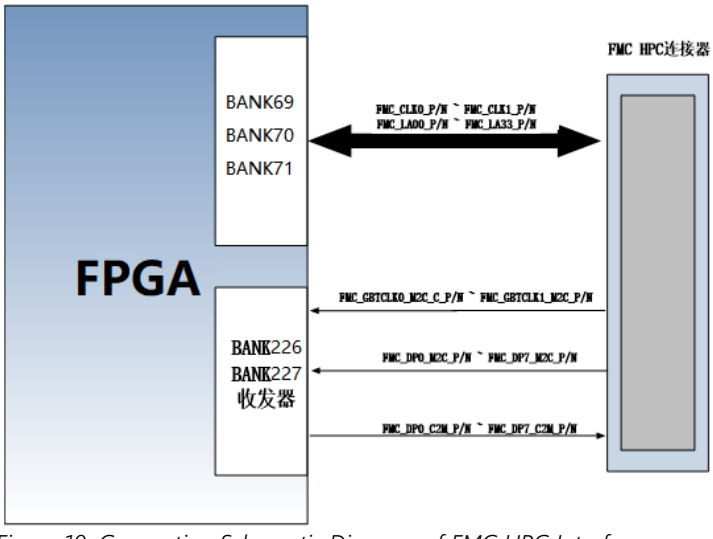

Figure 19: Connection Schematic Diagram of FMC HPC Interface

The FMC HPC J12 connector pin assignments are as follows:

Signal name	FPGA pin name	FPGA pin number	Remark
FMC1_CLK0_N	B70_L11_N	F21	FMC channel 0 input reference clock N
FMC1_CLK0_P	B70_L11_P	G21	FMC channel 0 input reference clock P
FMC1_CLK1_N	B69_L12_N	G30	FMC 1st input reference clock N
FMC1_CLK1_P	B69_L12_P	G29	FMC 1st input reference clock P
FMC1_LA00_CC_N	B70_L14_N	E24	FMC LA Channel 0 Data (Clock) N
FMC1_LA00_CC_P	B70_L14_P	E23	FMC LA Channel 0 Data (Clock) P
FMC1_LA01_CC_N	B70_L13_N	F24	FMC LA 1st data (clock) N
FMC1_LA01_CC_P	B70_L13_P	F23	FMC LA 1st data (clock) P
FMC1_LA02_N	B70_L17_N	D21	FMC LA Channel 2 Data N
FMC1_LA02_P	B70_L17_P	E21	FMC LA Channel 2 Data P
FMC1_LA03_N	B70_L24_N	A24	FMC LA Channel 3 Data N
FMC1_LA03_P	B70_L24_P	A23	FMC LA Channel 3 Data P
FMC1_LA04_N	B70_L12_N	F22	FMC LA Channel 4 Data N
FMC1_LA04_P	B70_L12_P	G22	FMC LA Channel 4 Data P
FMC1_LA05_N	B70_L6_N	K21	FMC LA Channel 5 Data N
FMC1_LA05_P	B70_L6_P	K20	FMC LA Channel 5 Data P
FMC1_LA06_N	B70_L5_N	K24	FMC LA Channel 6 Data P
FMC1_LA06_P	B70_L5_P	K23	FMC LA Channel 6 Data P
FMC1_LA07_N	B70_L4_N	L22	FMC LA Channel 7 Data N
FMC1_LA07_P	B70_L4_P	L21	FMC LA Channel 7 Data P
FMC1_LA08_N	B70_L3_N	L24	FMC LA 8th Channel Data N
FMC1_LA08_P	B70_L3_P	L23	FMC LA Channel 8 Data P
FMC1_LA09_N	B70_L2_N	M20	FMC LA Channel 9 Data N
FMC1_LA09_P	B70_L2_P	M19	FMC LA Channel 9 Data P
FMC1_LA10_N	B70_L18_N	D20	FMC LA 10th Channel Data N
FMC1_LA10_P	B70_L18_P	E20	FMC LA 10th Channel Data P
FMC1_LA11_N	B70_L23_N	B25	FMC LA Channel 11 Data N
FMC1_LA11_P	B70_L23_P	B24	FMC LA Channel 11 Data P
FMC1_LA12_N	B70_L1_N	M22	FMC LA 12th data N
FMC1_LA12_P	B70_L1_P	M21	FMC LA Channel 12 Data P
FMC1_LA13_N	B70_L21_N	A21	FMC LA Channel 13 Data N
FMC1_LA13_P	B70_L21_P	B21	FMC LA Channel 13 Data P
FMC1_LA14_N	B70_L19_N	C23	FMC LA 14th Channel Data N
FMC1_LA14_P	B70_L19_P	C22	FMC LA 14th Channel Data P
FMC1_LA15_N	B70_L20_N	B20	FMC LA Channel 15 Data N
FMC1_LA15_P	B70_L20_P	C20	FMC LA Channel 15 Data P
FMC1_LA16_N	B70_L22_N	A22	FMC LA Channel 16 Data N
FMC1_LA16_P	B70_L22_P	B22	FMC LA Channel 16 Data P
FMC1_LA17_CC_N	B69_L14_N	E29	FMC LA Channel 17 Data (Clock) N
FMC1_LA17_CC_P	B69_L14_P	E28	FMC LA 17th data (clock) P
FMC1_LA18_CC_N	B69_L13_N	F29	FMC LA 18th Data (Clock) N
FMC1_LA18_CC_P	B69_L13_P	F28	FMC LA 18th Data (Clock) P
FMC1_LA19_N	B70_L7_N	H22	FMC LA Channel 19 Data N
FMC1_LA19_P	B70_L7_P	J22	FMC LA Channel 19 Data P

FMC1_LA20_N	B69_L17_N	D26	FMC LA Channel 20 Data N
FMC1_LA20_P	B69_L17_P	E26	FMC LA Channel 20 Data P
FMC1_LA21_N	B69_L2_N	H27	FMC LA Channel 21 Data N
FMC1_LA21_P	B69_L2_P	J27	FMC LA 21th data P
FMC1_LA22_N	B69_L4_N	H25	FMC LA Channel 22 Data N
FMC1_LA22_P	B69_L4_P	J25	FMC LA Channel 22 Data P
FMC1_LA23_N	B69_L5_N	J26	FMC LA Channel 23 Data N
FMC1_LA23_P	B69_L5_P	K26	FMC LA 23rd data P
FMC1_LA24_N	B69_L15_N	D31	FMC LA Channel 24 Data N
FMC1_LA24_P	B69_L15_P	E31	FMC LA Channel 24 Data P
FMC1_LA25_N	B70_L8_N	J21	FMC LA 25th Channel Data N
FMC1_LA25_P	B70_L8_P	J20	FMC LA Channel 25 Data P
FMC1_LA26_N	B69_L1_N	M26	FMC LA Channel 26 Data N
FMC1_LA26_P	B69_L1_P	M25	FMC LA Channel 26 Data P
FMC1_LA27_N	B69_L3_N	L27	FMC LA Channel 27 Data N
FMC1_LA27_P	B69_L3_P	L26	FMC LA Channel 27 Data P
FMC1_LA28_N	B69_L16_N	D30	FMC LA 28th Channel Data N
FMC1_LA28_P	B69_L16_P	E30	FMC LA 28th Channel Data P
FMC1_LA29_N	B69_L7_N	J31	FMC LA 29th channel data N
FMC1_LA29_P	B69_L7_P	J30	FMC LA 29th channel data P
FMC1_LA30_N	B69_L11_N	F27	FMC LA 30th data N
FMC1_LA30_P	B69_L11_P	G27	FMC LA 30th data P
FMC1_LA31_N	B69_L9_N	H28	FMC LA 31st Channel Data N
FMC1_LA31_P	B69_L9_P	J28	FMC LA 31st channel data P
FMC1_LA32_N	B69_L10_N	F31	FMC LA 32nd data N
FMC1_LA32_P	B69_L10_P	G31	FMC LA 32nd data P
FMC1_LA33_N	B69_L8_N	H30	FMC LA 33rd Channel Data N
FMC1_LA33_P	B69_L8_P	H29	FMC LA 33rd channel data P
FMC1_SCL	B90_L1_P	E5	FMC I2C-bus clock
FMC1_SDA	B90_L1_N	E4	FMC I2C-bus data
FMC1_HA00_CC_N	B71_L13_N	F18	FMC HA Channel 0 Data (Clock) N
FMC1_HA00_CC_P	B71_L13_P	F19	FMC HA Channel 0 Data (Clock) P
FMC1_HA01_CC_N	B71_L11_N	G16	FMC HA 1st Data (Clock) N
FMC1_HA01_CC_P	B71_L11_P	G17	FMC HA 1st Data (Clock) P
FMC1_HA02_N	B71_L21_N	A19	FMC HA Channel 2 Data N
FMC1_HA02_P	B71_L21_P	B19	FMC HA Channel 2 Data P
FMC1_HA03_N	B71_L12_N	G19	FMC HA Channel 3 Data N
FMC1_HA03_P	B71_L12_P	H19	FMC HA Channel 3 Data N
FMC1_HA04_N	B71_L22_N	B15	FMC HA Channel 4 Data N
FMC1_HA04_P	B71_L22_P	B16	FMC HA Channel 4 Data P
FMC1_HA05_N	B71_L19_N	C17	FMC HA Channel 5 Data N
FMC1_HA05_P	B71_L19_P	C18	FMC HA Channel 5 Data P
FMC1_HA06_N	B71_L9_N	G14	FMC HA Channel 6 Data N
FMC1_HA06_P	B71_L9_P	H14	FMC HA Channel 6 Data P
FMC1_HA07_N	B71_L6_N	K14	FMC HA Channel 7 Data N
FMC1_HA07_P	B71_L6_P	K15	FMC HA Channel 7 Data P
FMC1_HA08_N	B71_L15_N	E18	FMC HA Channel 8 Data N
FMC1_HA08_P	B71_L15_P	E19	FMC HA Channel 8 Data P

FMC1_HA09_N	B71_L17_N	D17	FMC HA Channel 9 Data N
FMC1_HA09_P	B71_L17_P	D18	FMC HA Channel 9 Data P
FMC1_HA10_N	B71_L8_N	H17	FMC HA 10th Channel Data N
FMC1_HA10_P	B71_L8_P	H18	FMC HA Channel 10 Data P
FMC1_HA11_N	B71_L16_N	E15	FMC HA Channel 11 Data N
FMC1_HA11_P	B71_L16_P	E16	FMC HA Channel 11 Data P
FMC1_HA12_N	B71_L18_N	D15	FMC HA Channel 12 Data N
FMC1_HA12_P	B71_L18_P	D16	FMC HA Channel 12 Data P
FMC1_HA13_N	B71_L10_N	F14	FMC HA Channel 13 Data N
FMC1_HA13_P	B71_L10_P	G15	FMC HA Channel 13 Data P
FMC1_HA14_N	B71_L23_N	A17	FMC HA 14th Channel Data N
FMC1_HA14_P	B71_L23_P	A18	FMC HA 14th Channel Data P
FMC1_HA15_N	B71_L24_N	A16	FMC HA Channel 15 Data N
FMC1_HA15_P	B71_L24_P	B17	FMC HA Channel 15 Data P
FMC1_HA16_N	B71_L20_N	C14	FMC HA Channel 16 Data N
FMC1_HA16_P	B71_L20_P	C15	FMC HA Channel 16 Data P
FMC1_HA17_CC_N	B71_L14_N	F16	FMC HA 17th Data (Clock) N
FMC1_HA17_CC_P	B71_L14_P	F17	FMC HA 17th Data (Clock) P
FMC1_HA18_N	B70_L9_N	G24	FMC HA Channel 18 Data N
FMC1_HA18_P	B70_L9_P	H24	FMC HA Channel 18 Data P
FMC1_HA19_N	B70_L10_N	G20	FMC HA Channel 19 Data N
FMC1_HA19_P	B70_L10_P	H20	FMC HA Channel 19 Data P
FMC1_HA20_N	B71_L7_N	H15	FMC HA Channel 20 Data N
FMC1_HA20_P	B71_L7_P	J15	FMC HA Channel 20 Data P
FMC1_HA21_N	B70_L15_N	D25	FMC HA Channel 21 Data N
FMC1_HA21_P	B70_L15_P	E25	FMC HA Channel 21 Data P
FMC1_HA22_N	B70_L16_N	D23	FMC HA Channel 22 Data N
FMC1_HA22_P	B70_L16_P	D22	FMC HA Channel 22 Data P
FMC1_HA23_N	B69_L24_N	A29	FMC HA Channel 23 Data N
FMC1_HA23_P	B69_L24_P	A28	FMC HA 23rd Channel Data P
FMC1_HPC_GBTCLK0_M2C_C_P	MGT226_CLK0_P	AG12	Transceiver Reference Clock 0 Input P
FMC1_HPC_GBTCLK0_M2C_C_N	MGT226_CLK0_N	AG11	Transceiver Reference Clock 0 Input N
CLK7_P	MGT226_CLK1_P	AF10	Transceiver Reference Clock 1 Input P
CLK7_N	MGT226_CLK1_N	AF9	Transceiver Reference Clock 1 Input N
FMC1_DP0_M2C_P	MGT226_RX0_P	AL4	Transceiver Data 0 Input P
FMC1_DP0_M2C_N	MGT226_RX0_N	AL3	Transceiver Data 0 Input N
FMC1_DP1_M2C_P	MGT226_RX1_P	AK2	Transceiver Data 1 Input P
FMC1_DP1_M2C_N	MGT226_RX1_N	AK1	Transceiver Data 1 Input N
FMC1_DP2_M2C_P	MGT226_RX2_P	AJ4	Transceiver Data 2 Input P
FMC1_DP2_M2C_N	MGT226_RX2_N	AJ3	Transceiver Data 2 Input N
FMC1_DP3_M2C_P	MGT226_RX3_P	AH2	Transceiver Data 3 Input P
FMC1_DP3_M2C_N	MGT226_RX3_N	AH1	Transceiver Data 3 Input N
FMC1_DP4_M2C_P	MGT227_RX0_P	AG4	Transceiver Data 4 Input P
FMC1_DP4_M2C_N	MGT227_RX0_N	AG3	Transceiver Data 4 Input N
FMC1_DP5_M2C_P	MGT227_RX1_P	AF2	Transceiver Data 5 Input P
FMC1_DP5_M2C_N	MGT227_RX1_N	AF1	Transceiver Data 5 Input N

FMC1_DP6_M2C_P	MGT227_RX2_P	AE4	Transceiver Data 6 Input P
FMC1_DP6_M2C_N	MGT227_RX2_N	AE3	Transceiver Data 6 Input N
FMC1_DP7_M2C_P	MGT227_RX3_P	AD2	Transceiver Data 7 Input P
FMC1_DP7_M2C_N	MGT227_RX3_N	AD1	Transceiver Data 7 Input N
FMC1_DP0_C2M_P	MGT226_TX0_P	AL8	Transceiver Data 0 Output P
FMC1_DP0_C2M_N	MGT226_TX0_N	AL7	Transceiver Data 0 Output N
FMC1_DP1_C2M_P	MGT226_TX1_P	AK6	Transceiver Data 1 Output P
FMC1_DP1_C2M_N	MGT226_TX1_N	AK5	Transceiver Data 1 Output N
FMC1_DP2_C2M_P	MGT226_TX2_P	AJ8	Transceiver Data 2 Output P
FMC1_DP2_C2M_N	MGT226_TX2_N	AJ7	Transceiver Data 2 Output N
FMC1_DP3_C2M_P	MGT226_TX3_P	AH6	Transceiver Data 3 Output P
FMC1_DP3_C2M_N	MGT226_TX3_N	AH5	Transceiver Data 3 Output N
FMC1_DP4_C2M_P	MGT227_TX0_P	AG8	Transceiver Data 4 Output P
FMC1_DP4_C2M_N	MGT227_TX0_N	AG7	Transceiver Data 4 Output N
FMC1_DP5_C2M_P	MGT227_TX1_P	AF6	Transceiver data 5 output P
FMC1_DP5_C2M_N	MGT227_TX1_N	AF5	Transceiver Data 5 Output N
FMC1_DP6_C2M_P	MGT227_TX2_P	AE8	Transceiver Data 6 Output P
FMC1_DP6_C2M_N	MGT227_TX2_N	AE7	Transceiver Data 6 Output N
FMC1_DP7_C2M_P	MGT227_TX3_P	AD6	Transceiver Data 7 Output P
FMC1_DP7_C2M_N	MGT227_TX3_N	AD5	Transceiver Data 7 Output N
FMC1_HPC_GBTCLK1_M2C_C_P	MGT227_CLK0_P	AE12	Transceiver Reference Clock 0 Input P
FMC1_HPC_GBTCLK1_M2C_C_N	MGT227_CLK0_N	AE11	Transceiver Reference Clock 0 Input N
CLK2_P	MGT227_CLK1_P	AD10	Transceiver Reference Clock 1 Input P
CLK2_N	MGT227_CLK1_N	AD9	Transceiver Reference Clock 1 Input N

Table 18: FMC HPC J12 connector pin assignment

The FMC2 expansion port contains 34 pairs of LA signal differential pairs and 2 pairs of clock signals, which are connected to the FPGA chips BANK64 and BANK65 respectively. The standard level is 1.8V by default. 8 channels of high-speed GTY transceiving signals are connected to the IO of FPGA chips BANK224 and BANK225.

The schematic diagram of the FPGA and FMC HPC connector is shown in Figure 20:

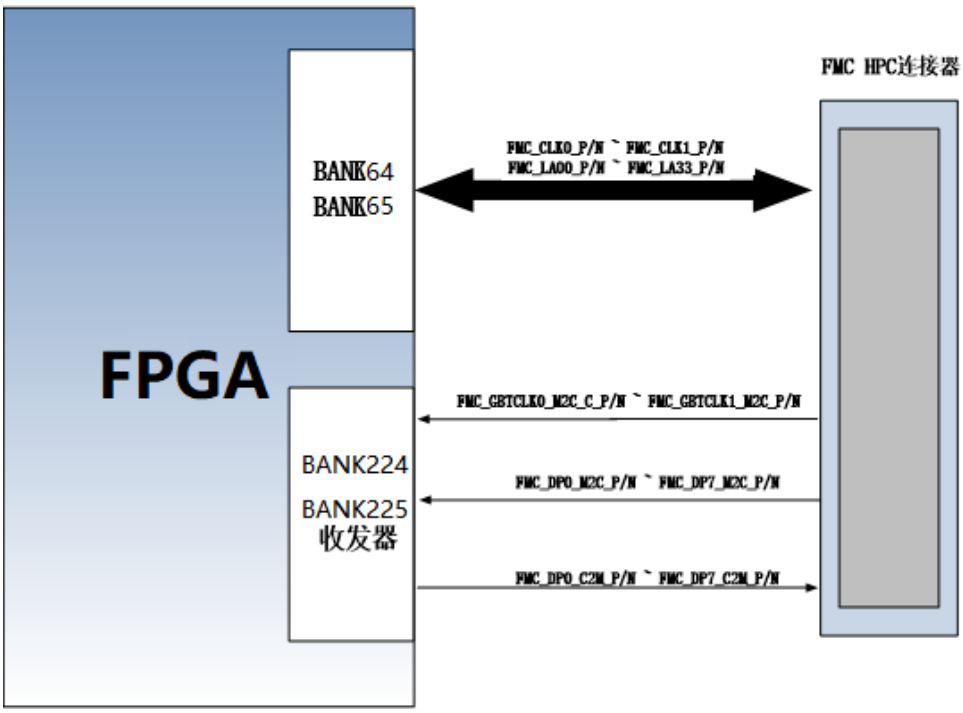

Figure 20: Connection diagram of HPC FMC

The FMC HPC J13 connector pin assignments are as follows:

Signal name	FPGA pin name	FPGA pin number	Remark
FMC2_CLK0_M2C_N	B65_L12_N	AP14	FMC channel 0 input reference clock N
FMC2_CLK0_M2C_P	B65_L12_P	AP15	FMC channel 0 input reference clock P
FMC2_CLK1_M2C_N	B64_L12_N	AM20	FMC 1st input reference clock N
FMC2_CLK1_M2C_P	B64_L12_P	AL20	FMC 1st input reference clock P
FMC2_LA00_CC_N	B65_L14_N	AN15	FMC LA Channel 0 Data (Clock) N
FMC2_LA00_CC_P	B65_L14_P	AM15	FMC LA Channel 0 Data (Clock) P
FMC2_LA01_CC_N	B65_L13_N	AL14	FMC LA 1st data (clock) N
FMC2_LA01_CC_P	B65_L13_P	AL15	FMC LA 1st data (clock) P
FMC2_LA02_N	B65_L17_N	AJ15	FMC LA Channel 2 Data N
FMC2_LA02_P	B65_L17_P	AJ16	FMC LA Channel 2 Data P
FMC2_LA03_N	B65_L5_N	AV12	FMC LA Channel 3 Data N
FMC2_LA03_P	B65_L5_P	AV13	FMC LA Channel 3 Data P
FMC2_LA04_N	B65_L19_N	AT11	FMC LA Channel 4 Data N
FMC2_LA04_P	B65_L19_P	AT12	FMC LA Channel 4 Data P
FMC2_LA05_N	B65_L24_N	AM13	FMC LA Channel 5 Data N
FMC2_LA05_P	B65_L24_P	AM14	FMC LA Channel 5 Data P
FMC2_LA06_N	B65_L8_N	AU15	FMC LA Channel 6 Data P
FMC2_LA06_P	B65_L8_P	AT15	FMC LA Channel 6 Data P
FMC2_LA07_N	B65_L10_N	AR16	FMC LA Channel 7 Data N
FMC2_LA07_P	B65_L10_P	AP16	FMC LA Channel 7 Data P
FMC2_LA08_N	B65_L11_N	AT14	FMC LA 8th Channel Data N
FMC2_LA08_P	B65_L11_P	AR14	FMC LA Channel 8 Data P
FMC2_LA09_N	B65_L9_N	AW15	FMC LA Channel 9 Data N
FMC2_LA09_P	B65_L9_P	AV15	FMC LA Channel 9 Data P
FMC2_LA10_N	B65_L4_N	AV10	FMC LA 10th Channel Data N

FMC2_LA10_P	B65_L4_P	AU10	FMC LA 10th Channel Data P
FMC2_LA11_N	B64_L10_N	AL21	FMC LA Channel 11 Data N
FMC2_LA11_P	B64_L10_P	AK21	FMC LA Channel 11 Data P
FMC2_LA12_N	B65_L7_N	AW16	FMC LA 12th data N
FMC2_LA12_P	B65_L7_P	AV16	FMC LA Channel 12 Data P
FMC2_LA13_N	B64_L9_N	AP20	FMC LA Channel 13 Data N
FMC2_LA13_P	B64_L9_P	AP21	FMC LA Channel 13 Data P
FMC2_LA14_N	B64_L7_N	AR21	FMC LA 14th Channel Data N
FMC2_LA14_P	B64_L7_P	AR22	FMC LA 14th Channel Data P
FMC2_LA15_N	B64_L11_N	AN20	FMC LA Channel 15 Data N
FMC2_LA15_P	B64_L11_P	AN21	FMC LA Channel 15 Data P
FMC2_LA16_N	B64_L8_N	AM22	FMC LA Channel 16 Data N
FMC2_LA16_P	B64_L8_P	AL22	FMC LA Channel 16 Data P
FMC2_LA17_CC_N	B64_L14_N	AP18	FMC LA Channel 17 Data (Clock) N
FMC2_LA17_CC_P	B64_L14_P	AN18	FMC LA 17th data (clock) P
FMC2_LA18_CC_N	B64_L13_N	AR19	FMC LA 18th Data (Clock) N
FMC2_LA18_CC_P	B64_L13_P	AP19	FMC LA 18th Data (Clock) P
FMC2_LA19_N	B64_L6_N	AW18	FMC LA Channel 19 Data N
FMC2_LA19_P	B64_L6_P	AV18	FMC LA Channel 19 Data P
FMC2_LA20_N	B64_L16_N	AU17	FMC LA Channel 20 Data N
FMC2_LA20_P	B64_L16_P	AT17	FMC LA Channel 20 Data P
FMC2_LA21_N	B64_L20_N	AM19	FMC LA Channel 21 Data N
FMC2_LA21_P	B64_L20_P	AL19	FMC LA 21th data P
FMC2_LA22_N	B64_L21_N	AJ19	FMC LA Channel 22 Data N
FMC2_LA22_P	B64_L21_P	AJ20	FMC LA Channel 22 Data P
FMC2_LA23_N	B64_L23_N	AJ18	FMC LA Channel 23 Data N
FMC2_LA23_P	B64_L23_P	AH18	FMC LA 23rd data P
FMC2_LA24_N	B64_L15_N	AT19	FMC LA Channel 24 Data N
FMC2_LA24_P	B64_L15_P	AT20	FMC LA Channel 24 Data P
FMC2_LA25_N	B64_L18_N	AR17	FMC LA 25th Channel Data N
FMC2_LA25_P	B64_L18_P	AR18	FMC LA Channel 25 Data P
FMC2_LA26_N	B64_L19_N	AJ21	FMC LA Channel 26 Data N
FMC2_LA26_P	B64_L19_P	AH21	FMC LA Channel 26 Data P
FMC2_LA27_N	B64_L22_N	AK18	FMC LA Channel 27 Data N
FMC2_LA27_P	B64_L22_P	AK19	FMC LA Channel 27 Data P
FMC2_LA28_N	B64_L17_N	AU18	FMC LA 28th Channel Data N
FMC2_LA28_P	B64_L17_P	AU19	FMC LA 28th Channel Data P
FMC2_LA29_N	B64_L1_N	AV22	FMC LA 29th channel data N
FMC2_LA29_P	B64_L1_P	AU22	FMC LA 29th channel data P
FMC2_LA30_N	B64_L3_N	AW21	FMC LA 30th data N
FMC2_LA30_P	B64_L3_P	AV21	FMC LA 30th data P
FMC2_LA31_N	B64_L5_N	AT21	FMC LA 31st Channel Data N
FMC2_LA31_P	B64_L5_P	AT22	FMC LA 31st channel data P
FMC2_LA32_N	B64_L4_N	AW19	FMC LA 32nd data N
FMC2_LA32_P	B64_L4_P	AW20	FMC LA 32nd data P
FMC2_LA33_N	B64_L2_N	AV20	FMC LA 33rd Channel Data N
FMC2_LA33_P	B64_L2_P	AU20	FMC LA 33rd channel data P
FMC2_SCL	B90_L2_P	F4	FMC I2C-bus clock

FMC2_SDA	B90_L2_N	E3	FMC I2C-bus data
FMC2_HPC_GBTCLK0_M2C_C_N	MGT224_CLK0_N	AM9	Transceiver Reference Clock 0 Input N
FMC2_HPC_GBTCLK0_M2C_C_P	MGT224_CLK0_P	AM10	Transceiver Reference Clock 0 Input P
MGT_A_CLOCK_N	MGT224_CLK1_N	AK9	Transceiver Reference Clock 1 Input N
MGT_A_CLOCK_P	MGT224_CLK1_P	AK10	Transceiver Reference Clock 1 Input P
FMC2_DP0_M2C_P	MGT224_RX0_P	AW4	Transceiver Data 0 Input P
FMC2_DP0_M2C_N	MGT224_RX0_N	AW3	Transceiver Data 0 Input N
FMC2_DP1_M2C_P	MGT224_RX3_P	AT2	Transceiver Data 1 Input P
FMC2_DP1_M2C_N	MGT224_RX3_N	AT1	Transceiver Data 1 Input N
FMC2_DP2_M2C_P	MGT224_RX2_P	AU4	Transceiver Data 2 Input P
FMC2_DP2_M2C_N	MGT224_RX2_N	AU3	Transceiver Data 2 Input N
FMC2_DP3_M2C_P	MGT224_RX1_P	AV2	Transceiver Data 3 Input P
FMC2_DP3_M2C_N	MGT224_RX1_N	AV1	Transceiver Data 3 Input N
FMC2_DP4_M2C_P	MGT225_RX1_P	AP2	Transceiver Data 4 Input P
FMC2_DP4_M2C_N	MGT225_RX1_N	AP1	Transceiver Data 4 Input N
FMC2_DP5_M2C_P	MGT225_RX3_P	AM2	Transceiver Data 5 Input P
FMC2_DP5_M2C_N	MGT225_RX3_N	AM1	Transceiver Data 5 Input N
FMC2_DP6_M2C_P	MGT225_RX2_P	AN4	Transceiver Data 6 Input P
FMC2_DP6_M2C_N	MGT225_RX2_N	AN3	Transceiver Data 6 Input N
FMC2_DP7_M2C_P	MGT225_RX0_P	AR4	Transceiver Data 7 Input P
FMC2_DP7_M2C_N	MGT225_RX0_N	AR3	Transceiver Data 7 Input N
FMC2_DP0_C2M_P	MGT224_TX0_P	AW8	Transceiver Data 0 Output P
FMC2_DP0_C2M_N	MGT224_TX0_N	AW7	Transceiver Data 0 Output N
FMC2_DP1_C2M_P	MGT224_TX3_P	AT6	Transceiver Data 1 Output P
FMC2_DP1_C2M_N	MGT224_TX3_N	AT5	Transceiver Data 1 Output N
FMC2_DP2_C2M_P	MGT224_TX2_P	AU8	Transceiver Data 2 Output P
FMC2_DP2_C2M_N	MGT224_TX2_N	AU7	Transceiver Data 2 Output N
FMC2_DP3_C2M_P	MGT224_TX1_P	AV6	Transceiver Data 3 Output P
FMC2_DP3_C2M_N	MGT224_TX1_N	AV5	Transceiver Data 3 Output N
FMC2_DP4_C2M_P	MGT225_TX1_P	AP6	Transceiver Data 4 Output P
FMC2_DP4_C2M_N	MGT225_TX1_N	AP5	Transceiver Data 4 Output N
FMC2_DP5_C2M_P	MGT225_TX3_P	AM6	Transceiver data 5 output P
FMC2_DP5_C2M_N	MGT225_TX3_N	AM5	Transceiver Data 5 Output N
FMC2_DP6_C2M_P	MGT225_TX2_P	AN8	Transceiver Data 6 Output P
FMC2_DP6_C2M_N	MGT225_TX2_N	AN7	Transceiver Data 6 Output N
FMC2_DP7_C2M_P	MGT225_TX0_P	AR8	Transceiver Data 7 Output P
FMC2_DP7_C2M_N	MGT225_TX0_N	AR7	Transceiver Data 7 Output N
FMC2_HPC_GBTCLK1_M2C_C_N	MGT225_CLK0_N	AJ11	Transceiver Reference Clock 0 Input N
FMC2_HPC_GBTCLK1_M2C_C_P	MGT225_CLK0_P	AJ12	Transceiver Reference Clock 0 Input P
-	MGT225_CLK1_N	AH9	Transceiver Reference Clock 1 Input N
-	MGT225_CLK1_P	AH10	Transceiver Reference Clock 1 Input P

Table 19: FMC HPC J13 connector pin assignment

Part 3.5: MIPI Interface

The AXKU15 base board is equipped with two MIPI lanex4 camera input interfaces. MIPI1 corresponds to J9 and is connected to BANK69 and BANK90 of FPGA. MIPI2 corresponds to J10, and is connected to BANK66 and BANK84 of FPGA, and is connected to BANK71 and BANK90 of FPGA. The design schematic diagram of connection is shown in Figure 21 and 22 below:

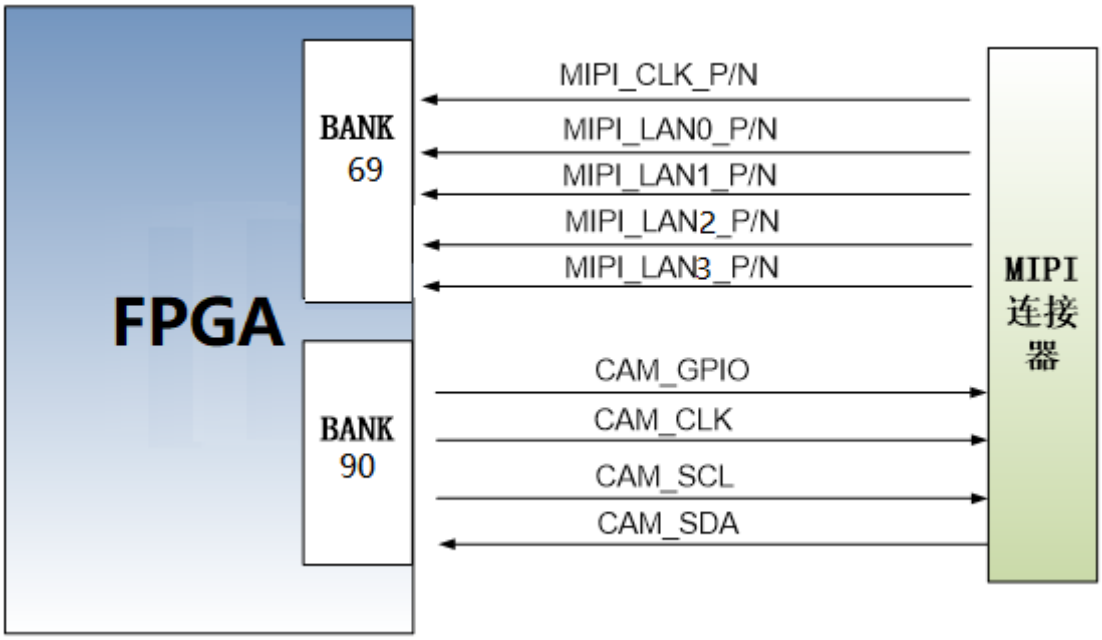

Figure 21: Schematic diagram of MIPI1 interface design

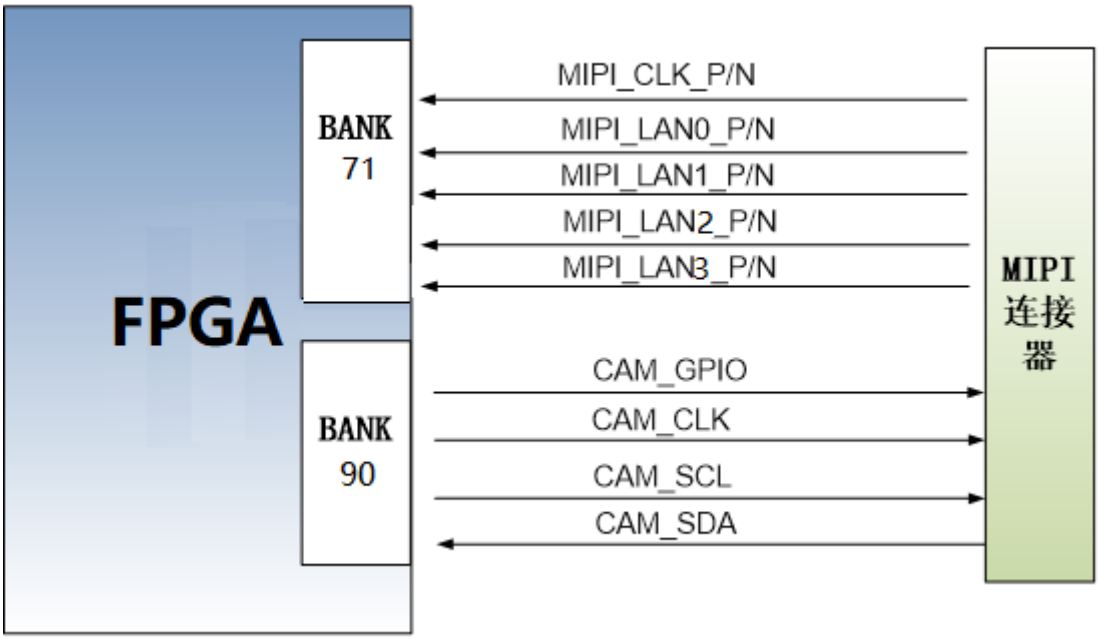

Figure 22: Schematic diagram of MIPI2 interface design

MIPI1 interface pin assignment:

Signal name	FPGA pin name	Pin number	Remark
MIPI1_CLK_P	B69_L19_P	C29	MIPI Input Clock Positive

MIPI1_CLK_N	B69_L19_N	B29	MIPI Input Clock Negative
MIPI1_LAN0_P	B69_L21_P	B31	MIPI Input Data LANE0 Positive
MIPI1_LAN0_N	B69_L21_N	A31	MIPI input data LANE0 negative
MIPI1_LAN1_P	B69_L23_P	B26	MIPI Input Data LANE1 Positive
MIPI1_LAN1_N	B69_L23_N	A26	MIPI Input Data LANE1 Negative
MIPI1_LAN2_P	B69_L20_P	C27	MIPI Input Data LANE2 Positive
MIPI1_LAN2_N	B69_L20_N	C28	MIPI input data LANE2 negative
MIPI1_LAN3_P	B69_L22_P	B27	MIPI input data LANE3 positive
MIPI1_LAN3_N	B69_L22_N	A27	MIPI input data LANE3 negative
MIPI1_CLK	B90_L8_P	C5	Clock input for the camera
MIPI1_GPIO	B90_L8_N	C4	GPIO control of the camera
MIPI1_I2C_SCL	B90_L3_P	F3	I2C clock for the camera
MIPI1_I2C_SDA	B90_L3_N	F2	I2C data for the camera

Table 20: MIPI1 interface pin assignment

MIPI2 interface pin assignment:

Signal name	FPGA pin name	Pin number	Remark
MIPI2_CLK_P	B71_L1_P	M16	MIPI Input Clock Positive
MIPI2_CLK_N	B71_L1_N	M15	MIPI Input Clock Negative
MIPI2_LAN0_P	B71_L2_P	L19	MIPI Input Data LANE0 Positive
MIPI2_LAN0_N	B71_L2_N	K19	MIPI input data LANE0 negative
MIPI2_LAN1_P	B71_L3_P	L18	MIPI Input Data LANE1 Positive
MIPI2_LAN1_N	B71_L3_N	K18	MIPI Input Data LANE1 Negative
MIPI2_LAN2_P	B71_L4_P	L17	MIPI Input Data LANE2 Positive
MIPI2_LAN2_N	B71_L4_N	L16	MIPI input data LANE2 negative
MIPI2_LAN3_P	B71_L5_P	K16	MIPI input data LANE3 positive
MIPI2_LAN3_N	B71_L5_N	J16	MIPI input data LANE3 negative
MIPI2_CLK	B90_L7_P	D3	Clock input for the camera
MIPI2_GPIO	B90_L7_N	C3	GPIO control of the camera
MIPI2_I2C_SCL	B90_L4_P	F1	I2C clock for the camera
MIPI2_I2C_SDA	B90_L4_N	E1	I2C data for the camera

Table 21: MIPI2 interface pin assignment

Part 3.6: USB To serial port

The AXKU15 base board is equipped with a Uart to USB interface for system debugging. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface, which can be connected to the USB port of the upper PC with a USB cable for separate power supply of the module and serial port data communication.

The schematic diagram of the USB Uart circuit design is shown in the following figure:

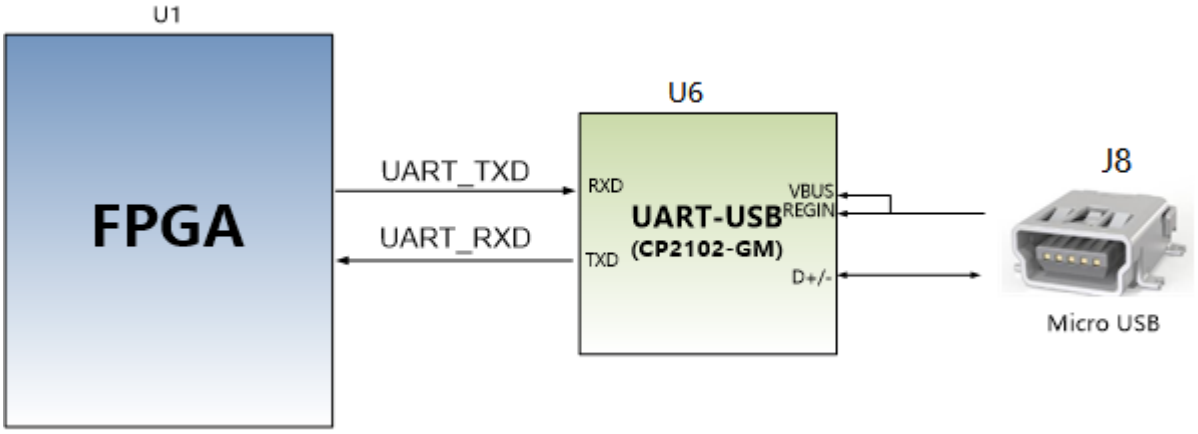

Figure 23: Schematic diagram of USB to serial port

USB to Serial FPGA pin assignment:

Signal name	FPGA pin name	Pin number	Remark
UART_RXD	B90_L6_N	D1	Uart Data Input
UART_TXD	B90_L6_P	D2	Uart Data Output

Table 22: USB to Serial FPGA pin assignment

Part 3.7: SD Card slot

The AXKU15 base board includes a Micro-type of SD card interface to provide user access to SD card memory for user data files. The SDIO signal is connected with the IO signal of the FPGA, supports the SPI mode and the SD mode, and the SD card used is a MicroSD card. The schematic diagram of FPGA and SD card connector is shown in Figure 24 below.

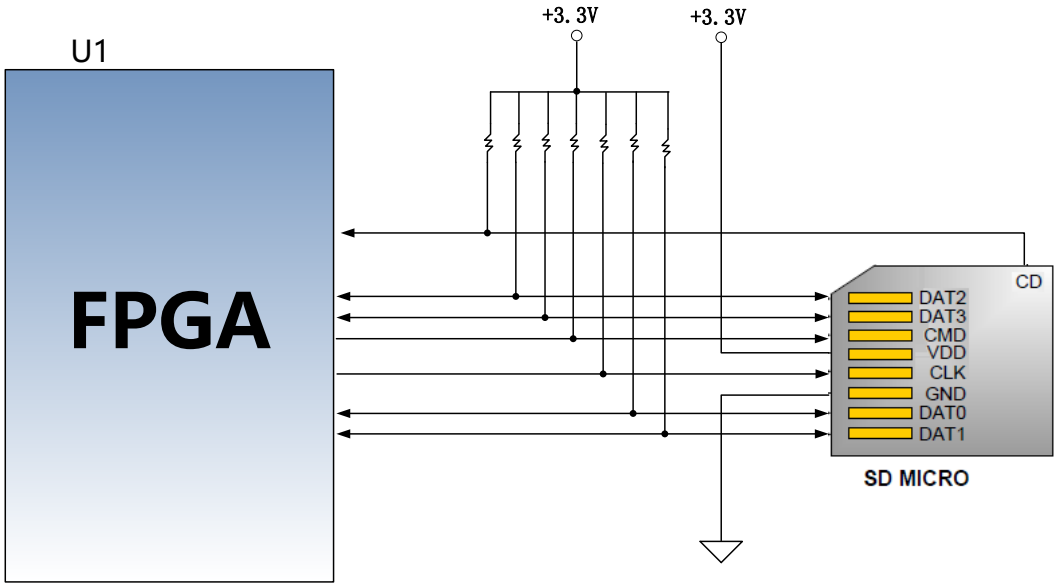

Figure 24: Schematic Diagram of SD Card Slot

SD card slot pin assignment:

Signal name	FPGA pin name	Pin number	Remark
SD_CD	B90_L11_N	A3	SD chip select signal

SD_CLK	B91_L8_P	C10	SD clock signal
SD_CMD	B91_L8_N	C9	SD command signal
SD_D0	B90_L12_N	A6	SD Data 0
SD_D1	B90_L12_P	B6	SD Data 1
SD_D2	B91_L7_N	C7	SD Data 2
SD_D3	B91_L7_P	C8	SD Data 3

Table 23: SD card slot pin assignment

Part 3.8: SATA Interface

The board is equipped with two SATA interfaces, and the differential signal of SATA is connected to GTY BANK131.

The SATA reference clock of 150Mhz is provided by the programmable clock chip Si5332BD11025-4. The schematic diagram of SATA interface design is shown in Figure 25 below:

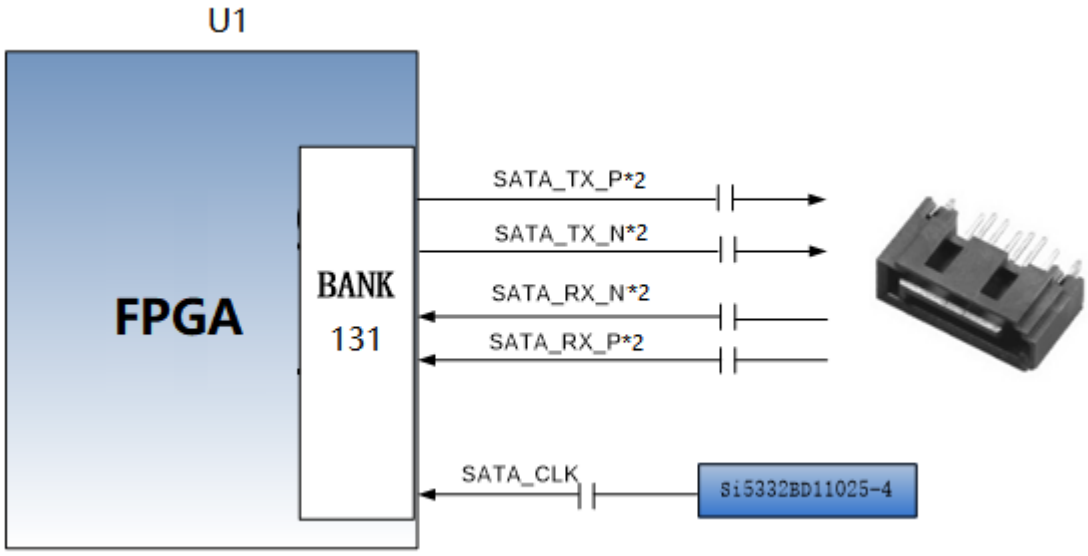

Figure 25: SATA Interface Design Diagram

The SATA interface FPGA pin assignments are as follows:

Signal name	Pin name	Pin number	Remark
SATA1_RX_N	MGT131_RX0_N	M37	SATA1 data receive negative
SATA1_RX_P	MGT131_RX0_P	M36	SATA 1 data receiving positive
SATA2_RX_N	MGT131_RX1_N	L39	SATA2 data reception is negative
SATA2_RX_P	MGT131_RX1_P	L38	SATA2 data receiving positive
SATA1_TX_N	MGT131_TX0_N	J34	SATA 1 Data Transmit Negative
SATA1_TX_P	MGT131_TX0_P	J33	SATA 1 Data Sending Positive
SATA2_TX_N	MGT131_TX1_N	G34	SATA2 data transmission is negative
SATA2_TX_P	MGT131_TX1_P	G33	SATA2 Data Sending Positive
SATACLK_N	MGT131_CLK0_N	T28	SATA Reference Clock Negative
SATACLK_P	MGT131_CLK0_P	T27	SATA reference clock positive

Table 24: SATA interface pin assignment

Part 3.9: Keys and LED Light

The AXKU15 base board has seven LEDs, one power indicator, two serial communication indicators, and four user LEDs. When the development board is powered on, the power indicator will light up; the four LEDs are connected to the IO of the FPGA, and the user can control the on and off through the program. When the IO voltage connected to the user LED is high, the user LED will light up, and when the IO voltage is low, the user LED will be off. In addition, there are four user keys on the board. The default key signal is high. When the key is pressed, the key level is low. Schematic diagram of hardware connection of user LED light and key is shown in Figure 26:

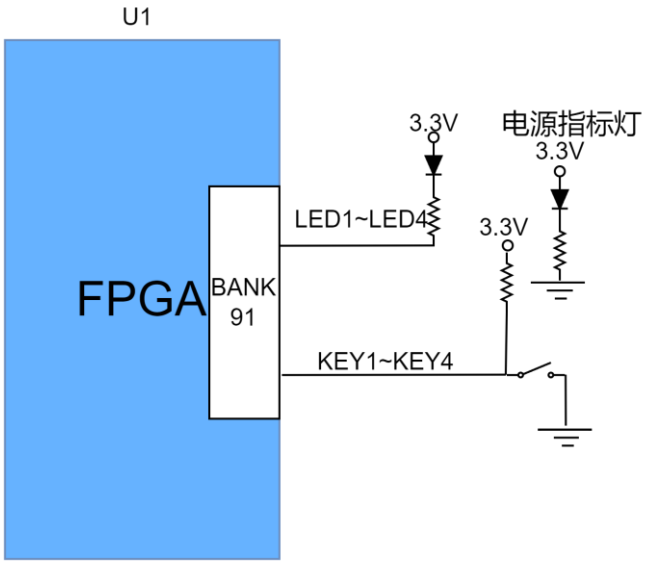

Figure 26: Schematic diagram of hardware connection of user LED light and key

Pin assignments for user LEDs and key:

Signal name	FPGA pin name	Pin number	Remark
KEY1	B91_L10_N	A8	User key 1
KEY2	B91_L10_P	B9	User key 2
KEY3	B91_L9_N	A7	User key 3
KEY4	B91_L9_P	B7	User key 4
LED1	B91_L5_P	D8	User LED 1 light
LED2	B91_L5_N	D7	User LED 2 light
LED3	B91_L6_P	D11	User LED3 light
LED4	B91_L6_N	D10	User LED4 light

Table 25: Pin assignments for user LEDs and key

Part 3.10: EEPROM

The AXP50 development board carries an EEPROM with a model of 24LC04 and a capacity of 4Kbit (2 * 256 * 8 bit), which is composed of two 256 byte blocks and communicates through the IIC bus. The on-board EEPROM is to learn how the IIC bus communicates. The I2C signal of the EEPROM is connected to the BANK B1 IO port of the FPGA end. Figure 27 below shows the design of EEPROM.

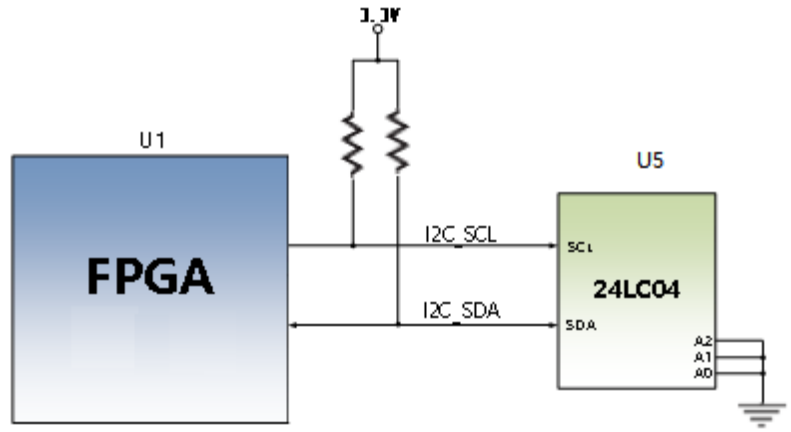

Figure 27: EEPROM Schematic Diagram

EEPROM pin assignment:

Pin name	FPGA pins
EEPROM_RTC_I2C_SCL	B2
EEPROM_RTC_I2C_SDA	C2

Table 26: EEPROM pin assignment

Part 3.11: Temperature sensor

A high-precision, low-power, digital temperature sensor chip, model LM75A from ON Semiconductor, is mounted on the AXP50 development board. The temperature accuracy of the LM75a chip is 0.125 degrees, the sensor and the FPGA are directly I2C digital interfaces, and the FPGA reads the temperature near the current development board through the I2C interface. Figure 28 below shows the design of the LM75A sensor chip.

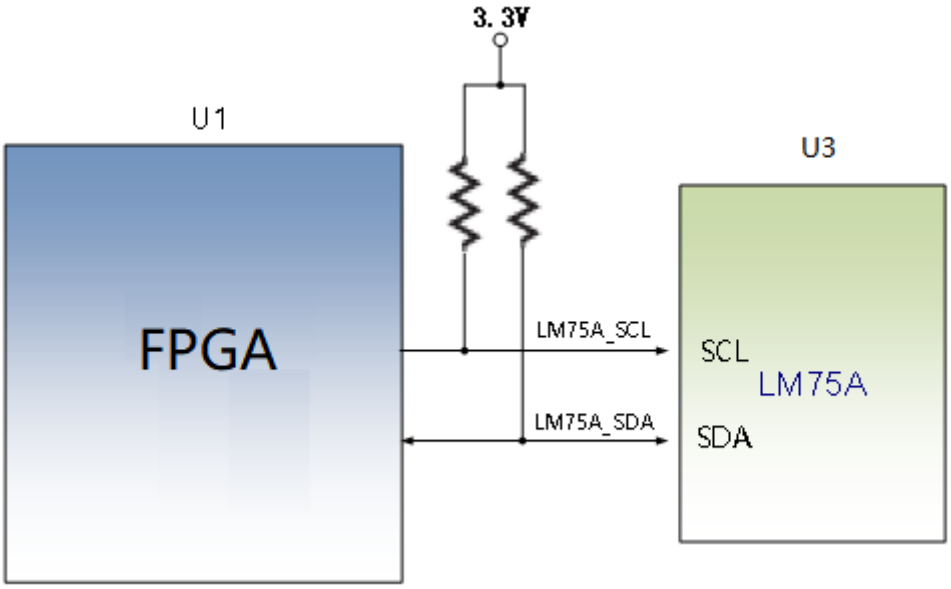

Figure 28: Schematic Diagram of LM75A Sensor

LM75a sensor pin assignment:

Pin name	FPGA pins
LM75A_SCL	B5
LM75A_SDA	B4

Table 27: LM75a sensor pin assignment

Part 3.12: Fiber Optic Interface

There are two QSFP28 optical fiber interfaces on the base board, and the user can purchase a QSFP optical module to be inserted into the four optical fiber interfaces for optical fiber data communication. The two optical interfaces are respectively connected with the four RX/TX of the GTY transceiver of BANK127-128 of the FPGA. The reference clock of BANK127-128 can be provided by Si5332BD11025-4 chip or independent crystal oscillator.

The schematic diagram of FPGA and optical fiber design is shown in Figure 29 below:

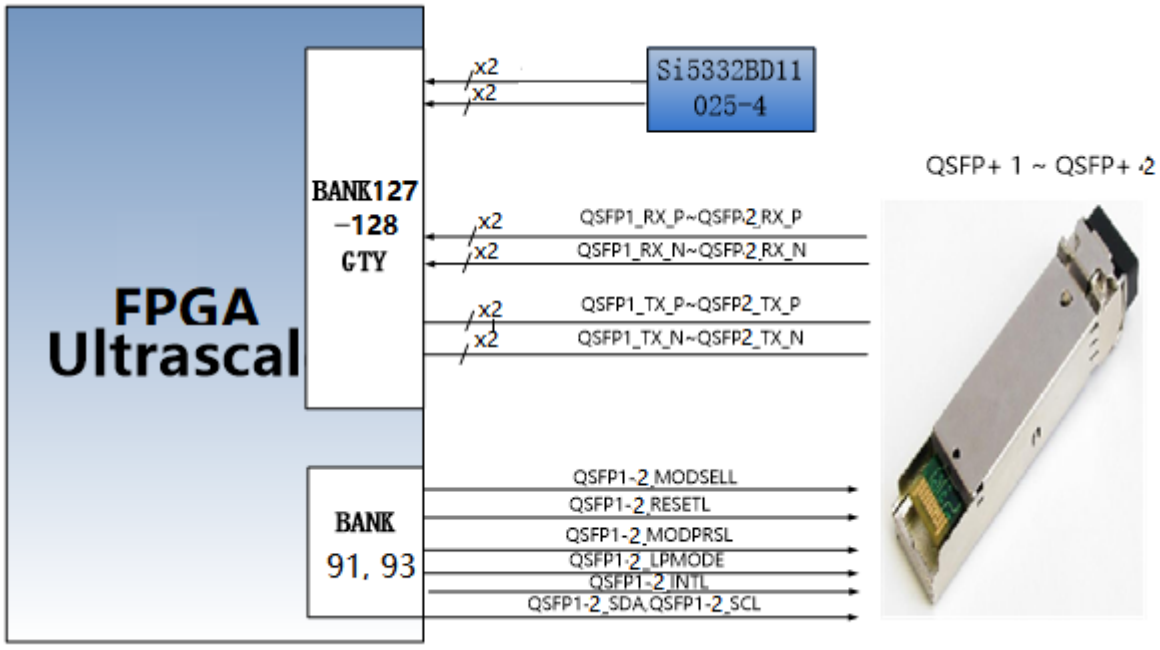

Figure 29: Schematic diagram of fiber design

The 2-way optical interface pins are assigned as follows:

Signal name	Grid label	FPGA pin number	Remark
QSFP1_RX1_N	MGT127_RX0_N	AH37	Optical module 1 data reception minus 1
QSFP1_RX1_P	MGT127_RX0_P	AH36	Optical module 1 data receiving positive 1
QSFP1_RX2_N	MGT127_RX1_N	AG39	Optical module 1 data receiving negative 2
QSFP1_RX2_P	MGT127_RX1_P	AG38	Optical module 1 data receiving positive 2
QSFP1_RX3_N	MGT127_RX2_N	AF37	Optical module 1 data receiving negative 3
QSFP1_RX3_P	MGT127_RX2_P	AF36	Optical module 1 data receiving positive 3
QSFP1_RX4_N	MGT127_RX3_N	AE39	Optical module 1 data receiving negative 4
QSFP1_RX4_P	MGT127_RX3_P	AE38	Optical module 1 data receiving positive 4
QSFP1_TX1_N	MGT127_TX0_N	AF32	Optical module 1 data sending minus 1
QSFP1_TX1_P	MGT127_TX0_P	AF31	Optical module 1 data sending positive 1

QSFP1_TX2_N	MGT127_TX1_N	AE34	Optical module 1 data sending minus 2
QSFP1_TX2_P	MGT127_TX1_P	AE33	Optical module 1 data sending positive 2
QSFP1_TX3_N	MGT127_TX2_N	AD32	Optical module 1 data sending minus 3
QSFP1_TX3_P	MGT127_TX2_P	AD31	Optical module 1 data sending positive 3
QSFP1_TX4_N	MGT127_TX3_N	AC34	Data transmission of optical module 1 minus 4
QSFP1_TX4_P	MGT127_TX3_P	AC33	Optical module 1 data sending positive 4
CLK0_N	MGT127_CLK0_N	AE30	BANK127 reference clock 0 negative
CLK0_P	MGT127_CLK0_P	AE29	BANK127 reference clock 0 positive
MGT_B_CLOCK_N	MGT127_CLK1_N	AC30	BANK127 reference clock 1 negative
MGT_B_CLOCK_P	MGT127_CLK1_P	AC29	BANK127 reference clock 1 positive
QSFP1_SCL	B91_L1_P	F6	I2C clock of optical module 1
QSFP1_SDA	B91_L2_P	F8	I2C data of optical module 1
QSFP1_INTL	B93_L10_P	L13	Interrupt signal of optical module 1
QSFP1_LPMODE	B91_L2_N	F7	Low power consumption selection signal of optical module 1
QSFP1_MODPRSL	B93_L10_N	K13	Optical module 1 presence indication signal
QSFP1_MODSELL	B93_L9_N	M10	Module selection signal of optical module 1
QSFP1_RESETL	B93_L9_P	N10	Optical module 1 reset signal
QSFP2_RX1_N	MGT128_RX0_N	AD37	Optical module 2 data reception minus 1
QSFP2_RX1_P	MGT128_RX0_P	AD36	Optical module 2 data receiving positive 1
QSFP2_RX2_N	MGT128_RX1_N	AC39	Optical module 2 data receiving negative 2
QSFP2_RX2_P	MGT128_RX1_P	AC38	Optical module 2 data receiving positive 2
QSFP2_RX3_N	MGT128_RX2_N	AB37	Optical module 2 data receiving negative 3
QSFP2_RX3_P	MGT128_RX2_P	AB36	Optical module 2 data receiving positive 3
QSFP2_RX4_N	MGT128_RX3_N	AA39	Optical module 2 data receiving negative 4
QSFP2_RX4_P	MGT128_RX3_P	AA38	Optical module 2 data receiving positive 4
QSFP2_TX1_N	MGT128_TX0_N	AB32	Optical module 2 data sending minus 1
QSFP2_TX1_P	MGT128_TX0_P	AB31	Optical module 2 data sending positive 1
QSFP2_TX2_N	MGT128_TX1_N	AA34	Optical module 2 data sending minus 2
QSFP2_TX2_P	MGT128_TX1_P	AA33	Optical module 2 data sending positive 2
QSFP2_TX3_N	MGT128_TX2_N	Y32	Optical module 2 data sending minus 3
QSFP2_TX3_P	MGT128_TX2_P	Y31	Optical module 2 data sending positive 3
QSFP2_TX4_N	MGT128_TX3_N	W34	Data transmission of optical module 2 minus 4
QSFP2_TX4_P	MGT128_TX3_P	W33	Optical module 2 data sending positive 4
CLK1_N	MGT128_CLK0_N	AB28	BANK128 reference clock 0 negative
CLK1_P	MGT128_CLK0_P	AB27	BANK128 reference clock 0 positive
CLK3_N	MGT128_CLK1_N	AA30	BANK128 reference clock 1 negative
CLK3_P	MGT128_CLK1_P	AA29	BANK128 reference clock 1 positive
QSFP2_SCL	B93_L5_N	N14	I2C clock of optical module 2
QSFP2_SDA	B93_L5_P	N15	I2C data of optical module 2
QSFP2_INTL	B91_L1_P	R15	Interrupt signal of optical module 2
QSFP2_LPMODE	B91_L2_P	N12	Low power consumption selection signal of optical module 2
QSFP2_MODPRSL	B93_L1_P	P15	Optical module 2 presence indication signal
QSFP2_MODSELL	B93_L6_N	R13	Module selection signal of optical module 2
QSFP2_RESETL	B93_L1_N	R14	Reset signal of optical module 2

Table 28: optical interface pin assignment

Part 3.13: JTAG Debugging port

A 10-PIN JTAG interface is reserved on the AXKU15 base board for downloading FPGA programs or solidifying programs to FLASH. To avoid the damage to the FPGA chip caused by live plugging, we add a protection diode on the JTAG signal to ensure that the voltage of the signal is within the acceptable range of the FPGA, to avoid the damage to the chip.

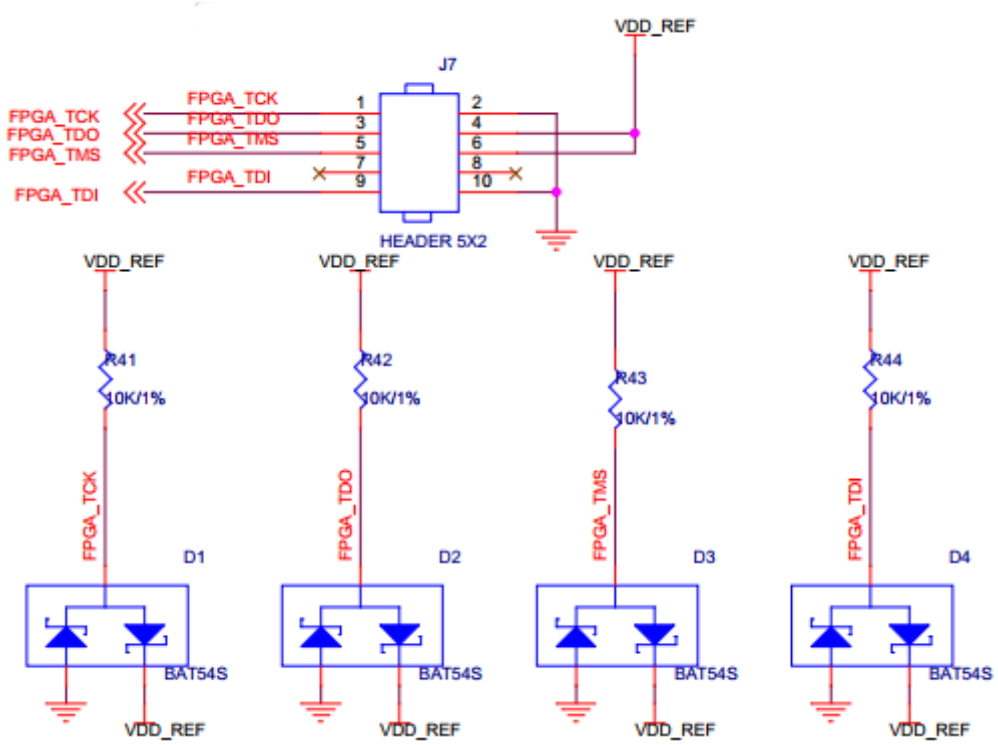

Figure 30: JTAG Interface Part in Schematic Diagram

Part 3.14: Power source

The power input voltage of the development board is DC12V, which can supply power to the board through the PCIE slot or external +12V power supply. Please use the power supply provided by the development board when supplying power from the external power supply. Do not use the power supply of other specifications to avoid damaging the development board. The 3-channel DC/DC power supply chip SGM61163 outputs +5V, FMC2 _ VADJ and 3.3V voltage respectively; ETA1471 outputs FMC1_VADJ regulated voltage. The +3.3V output at the same time is the voltage required by each FPGA BANK of the multiple LDO output JTAG.

The power supply design diagram on the board is shown in Figure 31 below:

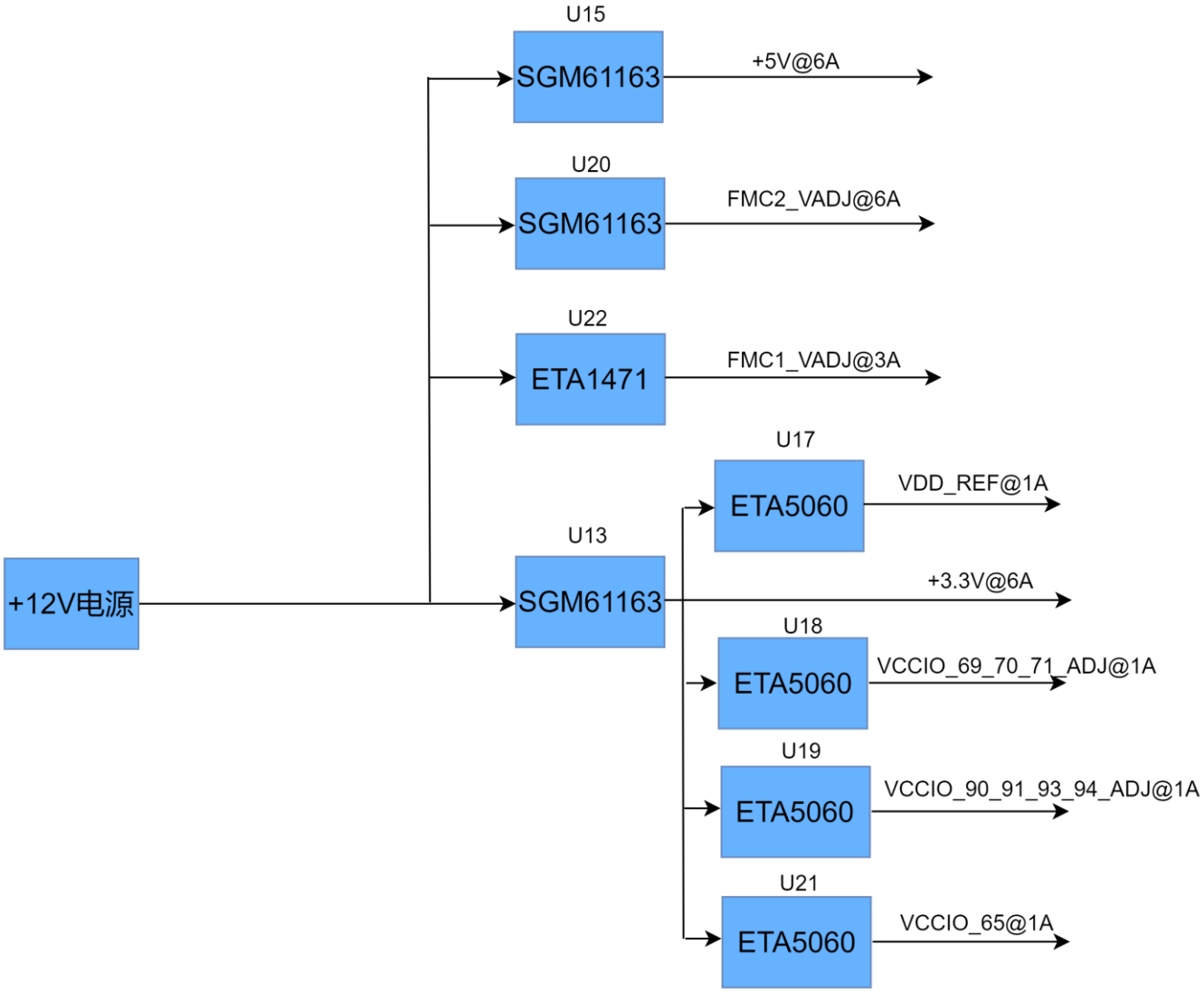

Figure 31: Power Interface Part in Schematic Diagram

The function of each power distribution is shown in the following table:

Power source	Function
+5.0V	Power supply of expansion module
FMC1_VADJ	FMC1 adjusts the voltage
FMC2_VADJ	FMC2 adjustment voltage
+3.3V	Backplane peripheral power supply
VDD_REF	JTAG Power Supply
VCCIO_65	FPGA BANK voltage
VCCIO_90_91_93_94_ADJ@1A	FPGA BANK voltage
VCCIO_69_70_71_ADJ@1A	FPGA BANK voltage

Table 29: power distribution

Part 3.14: Structural dimension drawing

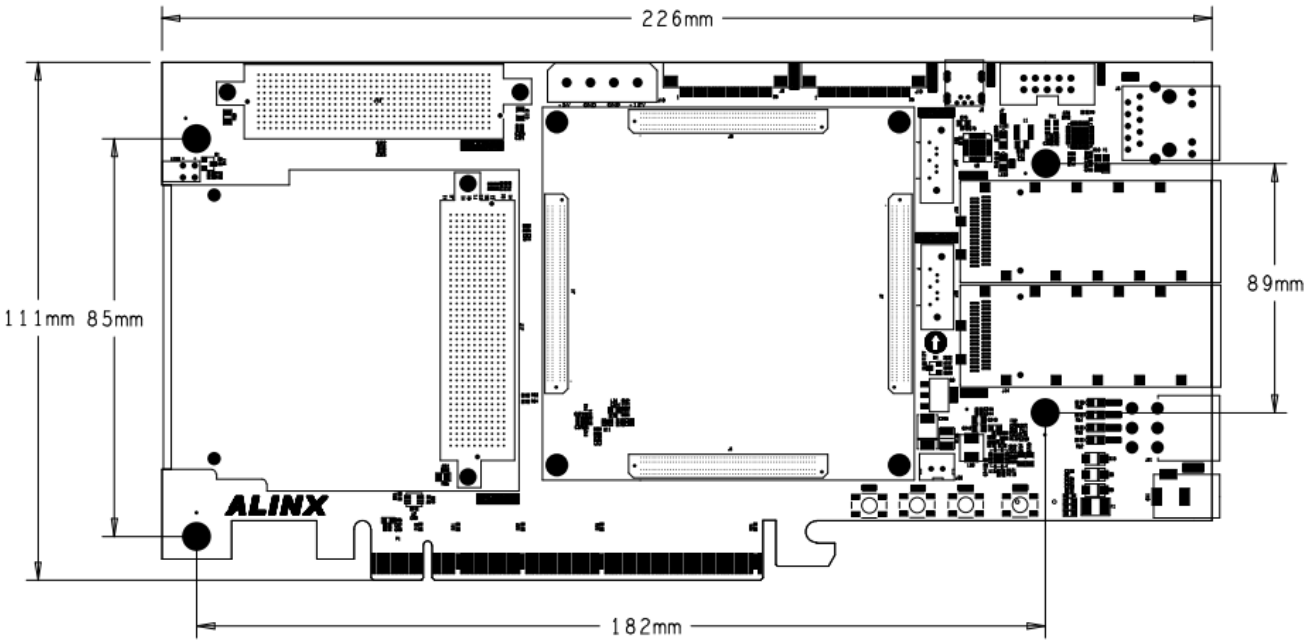

Figure 32: Top View