Xilinx FPGA Development Platform User Manual

AXKU3

Development Board

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Version Record

Version	Date	Release By	Description
Rev 1.0	2024/3/20	Kathy Xia	First Release
Rev 1.1	2024/3/29	Kathy Xia	Update the J1 and J2 connector positions incorrectly

Table of Contents

The development board (model: AXKU3) based on the Xilinx FPGA Kintex Ultrascale+ development platform of Alinx Electronic Technology has been officially released. To let you have a quick understanding of this development platform, we have compiled this user manual.

This Kintex Ultrascale+ FPGA development platform adopts the mode of SOM moule plus base board, which is convenient for users to develop and utilize the core module for the second time. The module uses the solution of Xilinx's Kintex Ultrascale+ chip xcku3pffvb676, which mounts two 1GB high-speed DDR4 SDRAM chips and two 256Mb QSPI FLASH chips.

In the design of the base board, we have expanded a wealth of peripheral interfaces for users, such as a PCIe3.0x8 interface, an FMC HPC interface, a Gigabit network interface, a MIPI input interface, an UART serial interface, an SD card interface, and a 40-pin expansion interface. It can meet the requirements of high-speed data exchange, video transmission processing and industrial control, and is a "professional" FPGA development platform. It is possible for high-speed data transmission and exchange, early verification, and later application of data processing. It is believed that such a product is very suitable for students, engineers and other groups engaged in FPGA development.

Figure 1: AXKU3 development board

Part 1: Development Board Introduction

Here is a brief introduction to the functionality of the Kintex Ultrascale+ AXKU3 development platform.

The whole structure of the development board is designed by inheriting our consistent SOM module + base board model. High-speed inter-board connectors are used between the core module and the base board.

The module is mainly composed of xcku3pffvb676 + 4 DDR4 + QSPI FLASH minimum systems. Xilinx's Kintex Ultrascale+ series chip, model xcku3pffvb676. Two DDR4 memory chips are connected to the HP port of the FPGA chip, and the capacity of each DDR4 chip is up to 1GB bytes, forming a 32-bit data bandwidth. Two 256Mb QSPI FLASHs are used to statically store configuration files or other user data of the FPGA chip.

The base board expands abundant peripheral interfaces for the module, including one PCIe3.0x8 interface, one FMC HPC interface, one Gigabit network interface, one MIPI input interface, one UART serial interface, an SD card interface, a 40-pin base board interface and some keys and LEDs.

The following figure shows the structure of the entire development system:

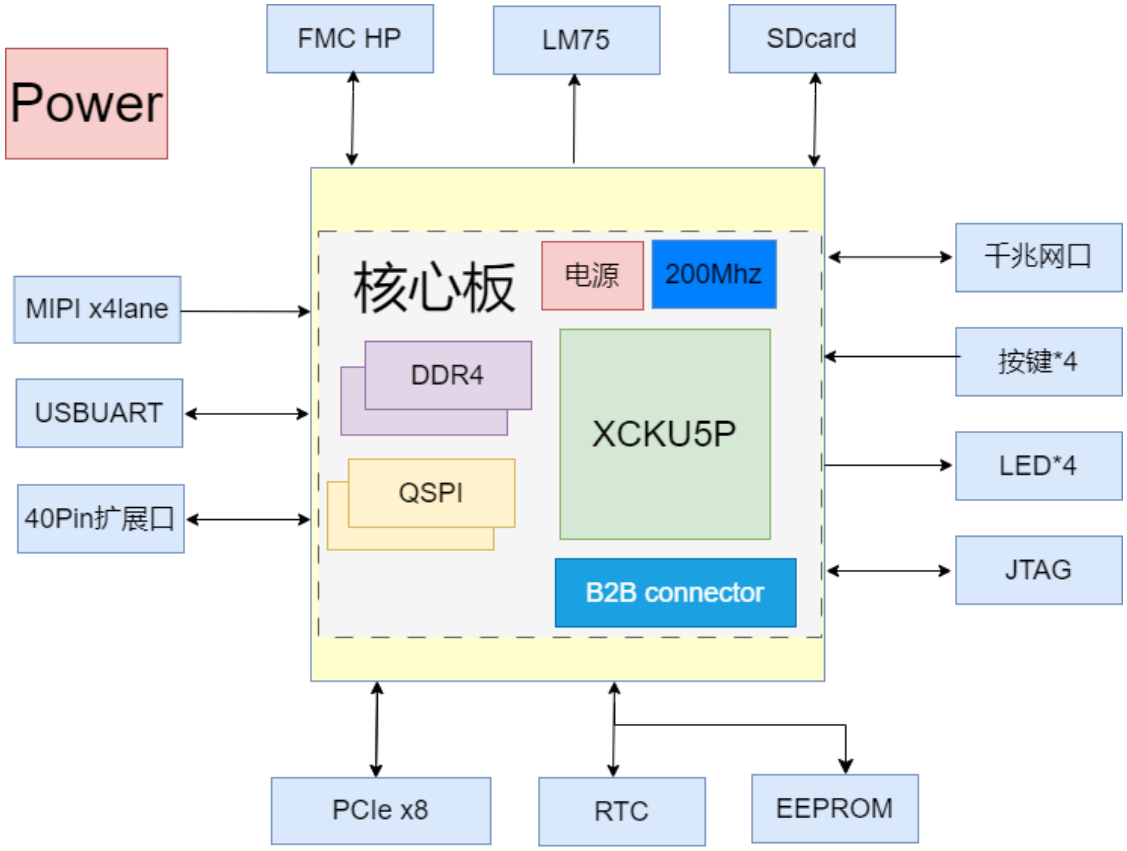

Figure 2: Structure of AXKU3

Through this diagram, we can see the interfaces and functions that our development platform can contain.

- **FPGA SOM Module**

It is composed of the minimum system of XCKU5P + 2 DDR4 + 2 QSPI FLASH. In addition, two crystal oscillators provide the clock, and two 200MHz crystal oscillators provide the reference clock for FPGA logic and DDR control.

- **PCIe3.0 x 8 interface**

It supports PCI Express 3.0 standard, provides standard PCIe x8 high-speed data transmission interface, and the communication rate of single channel can be up to 8GBaud.

- **1 * FMC HPC interface**

The 8-channel high-speed transceivers in the FPGA are connected to the high-speed pins dedicated for the FMC HPC, and 34 pairs of LA signal differential pairs and 2 pairs of clock signals of the FMC are led out, which can meet the requirements of high-speed signal transmission, comply with the FMC standard, and can be used for various FMC modules (HDMI input and output modules, high-speed AD modules, etc.).

- **1 * Gigabit network interface**

Gigabit Ethernet interface chip uses JL2121D Ethernet PHY chip to provide network communication services for users. The chip supports 10/100/1,000 Mbps network transmission rate, full-duplex and adaptive.

- **1 * MIPI input interface**

Onboard 1-channel MIPI lanex4 input interface, supporting a maximum rate of 2.5Gb/s, is used to connect the MIPI camera module.

- **USB Uart interface**

The 1-channel Uart to USB interface is used to communicate with the computer, which is convenient for users to debug. The serial port chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface.

- **Micro SD deck**

1-way Micro SD deck for storing OS images and file systems.

- **40-pin expansion port**

One 40-pin 2.54 mm pitch expansion port can be externally connected with various modules of Alinx (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port includes 1 channel of 5V power supply, 2 channels of 3.3 V power supply, 3 channels of ground, and 34 channels of IO port.

- **JTAG debug port**

One 10-pin 2.54 mm standard JTAG port is used to download and debug the FPGA program. Users can debug and download the FPGA system through the XILINX downloader.

- **Led light**

7 LEDs, 3 on the core module and 7 on the base board. 1 power indicator on the core module; 1 DONE configuration indicator and user indicator. There is one power indicator, four user indicators, and two serial port indicators on the base board.

- **Key**

4 user buttons on base board.

Part 2: ACKU3 SOM Module

Part 2.1: Introduction

ACKU3 (core module model, the same below) module, FPGA chip is based on the Xilinx FPGA Kintex Ultrascale+ main chip xcku3pffvb676 design. The module connects two DDR4 memory chips to the HP port of the FPGA to form a 32-bit data bandwidth, and the capacity of each DDR4 chip is up to 1GB. Memory bandwidth on the HP side is up to 85Gb/s. In addition, two 256MBit QSPI FLASHs are integrated on the module for boot storage configuration and system files.

This module expands 179 IOs by using a board-to-board connector. The level of the IO can be modified by replacing the LDO chip on the base board to meet the user's requirement of not using a level interface. In addition, the module also expands 16 pairs of high-speed transceiver interfaces. This module will be a good choice for users who need a lot of IO. Moreover, in the IO connection part, the wiring between the FPGA chip and the interface is processed with equal length and difference, and the size of the core module is only 80 * 60 (mm), which is very suitable for secondary development.

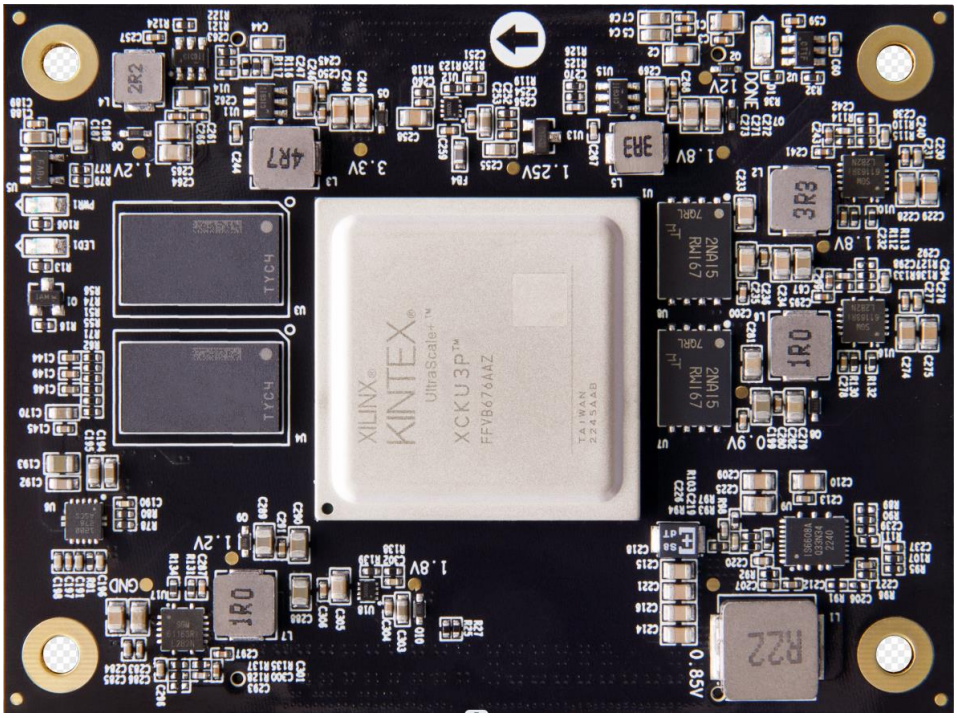

Figure 3: Front View of ACKU3 SOM Module

Part 2.2: FPGA Chip

It has been introduced before that the model of the FPGA we used is xcku3pffvb676, which belongs to the Kintex Ultrascale+ series products of Xilinx Company, with the speed grade of 2 and the temperature grade of industrial grade. This model is available in the FFVB676 package with 676 pins. The chip naming rule of Xilinx Kintex Ultrascale+ FPGA is as follows:

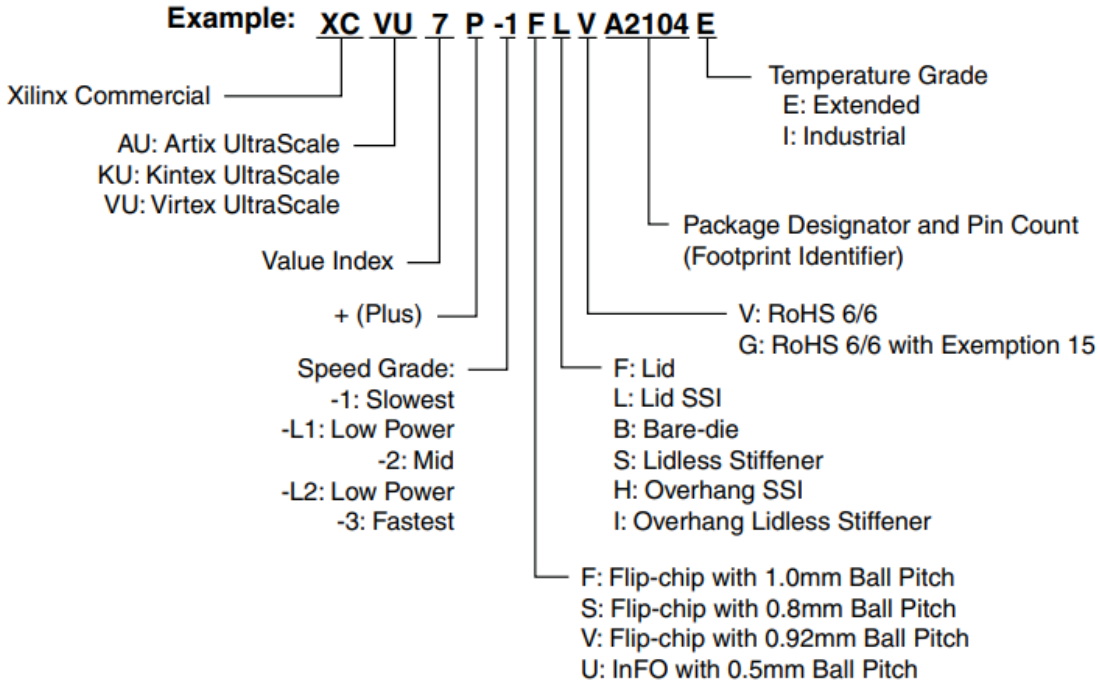

Figure 4: Ordering Information

Figure 5 is the physical picture of the FPGA chip used in the development board.

Figure 5: Physical FPGA chip

The main parameters of the FPGA chip are as follows:

Name	Specific parameters
Logic Cells	356K
Trigger (FF)	325,440
LUTs	162,720
Total Block RAM	12.7Mb
DSP Slices	1368
CMTs	4
GTY/Gb/s	16/28.21
PCIe Gen3 x16	1
Speed rating	-2
Temperature class	Industrial grade

Table 1: Main parameters of the FPGA chip

Part 2.3: DDR4

The ACKU3 development board is equipped with two Micron 1GB DDR4 chips, model MT40A512M16LY-062E, which are connected to the HP side of the FPGA to form a 32-bit data bus bandwidth and 2GB capacity. The maximum running data rate of DDR4 SDRAM on the FPGA side is 2,666Mbps, and two DDR4 memory systems are directly connected to the memory interfaces of BANK 66 and 67. The specific configuration of DDR4 SDRAM is shown in Table 2 below.

Tag number	Chip model	Capacity	Manufacturer
U3、U4	MT40A512M16LY-062E	512Mx 16bit	Micron

Table 2: DDR4 SDRAM Configuration

The hardware design of DDR4 needs to strictly consider the signal integrity. We have fully considered the matching resistor/termination resistor, trace impedance control, and trace length control in the circuit design and PCB design to ensure the high-speed and stable operation of DDR4.

The hardware connection mode of DDR4 on the FPGA side is shown in Figure 6:

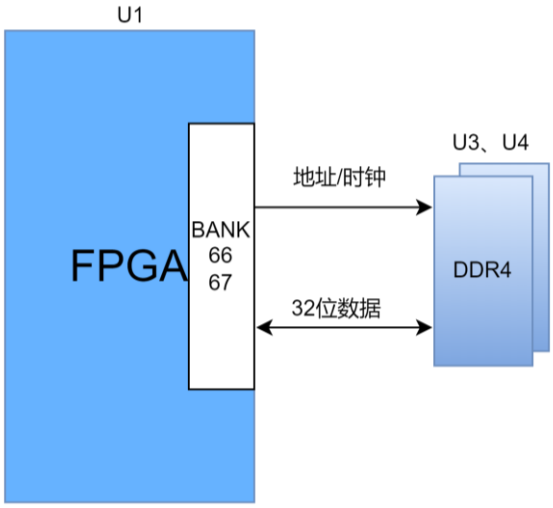

Figure 6: DDR4 DRAM Schematic

Figure 7 shows the physical picture of two DDR4 DRAMs of the development board.

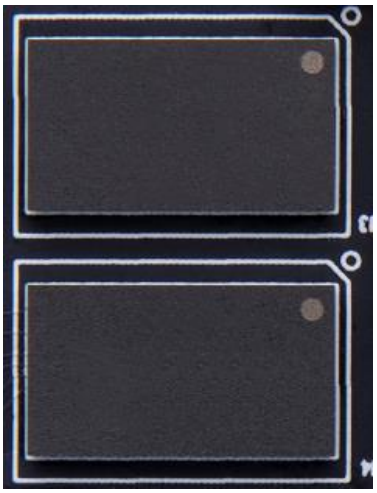

Figure 7: Physical drawing of 4 DDR4 DRAM

DDR4 SDRAM pin assignment:

Signal name	Pin number
DDR4_D0	C16
DDR4_D1	G16
DDR4_D2	D15
DDR4_D3	G17
DDR4_D4	H17
DDR4_D5	H16
DDR4_D6	D16
DDR4_D7	E15
DDR4_D8	B19
DDR4_D9	C17
DDR4_D10	B20
DDR4_D11	B15
DDR4_D12	A19
DDR4_D13	A15
DDR4_D14	A20
DDR4_D15	B17
DDR4_D16	G20
DDR4_D17	D19
DDR4_D18	D20
DDR4_D19	F19
DDR4_D20	G21
DDR4_D21	E18
DDR4_D22	D18
DDR4_D23	F18
DDR4_D24	C23
DDR4_D25	C22
DDR4_D26	A24
DDR4_D27	B22
DDR4_D28	A25
DDR4_D29	D21
DDR4_D30	B24
DDR4_D31	E21
DDR4_DM0	G15
DDR4_DM1	C18
DDR4_DM2	H18
DDR4_DM3	A22
DDR4_DQS0_N	E17
DDR4_DQS0_P	E16
DDR4_DQS1_N	A18
DDR4_DQS1_P	A17
DDR4_DQS2_N	E20
DDR4_DQS2_P	F20
DDR4_DQS3_N	B21
DDR4_DQS3_P	C21
DDR4_A0	D26

DDR4_A1	D25
DDR4_A2	E26
DDR4_A3	C24
DDR4_A4	C26
DDR4_A5	F24
DDR4_A6	M26
DDR4_A7	B25
DDR4_A8	G26
DDR4_A9	B26
DDR4_A10	E25
DDR4_A11	H26
DDR4_A12	D23
DDR4_A13	F25
DDR4_ACT_B	J26
DDR4_BA0	M25
DDR4_BA1	F23
DDR4_BG0	K26
DDR4_CAS_B	E23
DDR4_CKE	L24
DDR4_CLK_N	G25
DDR4_CLK_P	G24
DDR4_CS_B	D24
DDR4_OTD	H24
DDR4_PAR	J25
DDR4_RAS_B	F22
DDR4_RST	L25
DDR4_WE_B	K25

Table 3: DDR4 SDRAM pin assignment

Part 2.4: QSPI Flash

The core board is equipped with two 256MBit Quad-SPI FLASH chips, model MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can store the configuration Bin file of the FPGA as well as other user data files during use. See Table 4 for the specific model and relevant parameters of QSPI FLASH.

Tag number	Type of chip	Capacity	Manufacturer
U7、U8	MT25QU256ABA1EW9	256Mbit	Micron

Table 4: Model and Parameters of QSPI Flash

The QSPI FLASH is connected to a dedicated pin of the FPGA chip, wherein the clock pin is connected to CCLK0 of the dedicated BANK0, and the data pins are respectively connected to BANK0 and BANK65. Figure 8 is the connection diagram of QSPI Flash and FPGA chip.

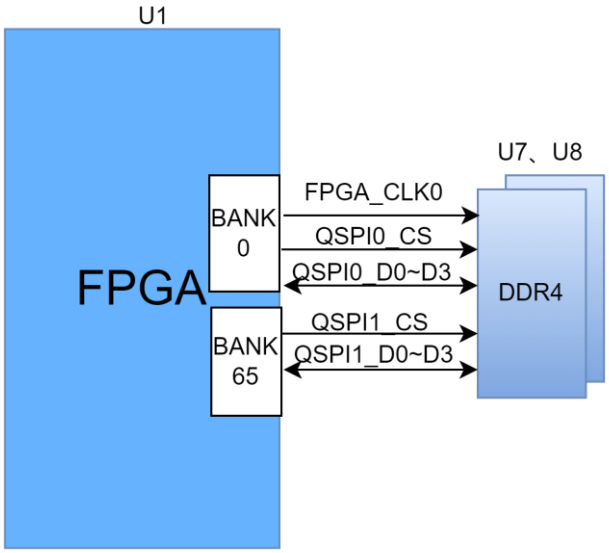

Figure 8: QSPI Flash Connection Diagram

Configure chip pin assignment:

Signal name	FPGA pin number
QSPI_CLK	Y11
QSPI0_CS	AA12
QSPI0_DQ0	AD11
QSPI0_DQ1	AC12
QSPI0_DQ2	AC11
QSPI0_DQ3	AE11
QSPI1_CS	U22
QSPI1_DQ0	N23
QSPI1_DQ1	P23
QSPI1_DQ2	R20
QSPI1_DQ3	R21

Table 5: Configure Chip Pin Assignment

Part 2.5: Clock Configuration

The module provides two 200Mhz differential active clocks for the FPGA system. And provide differential clock sources for that logic part of the FPGA respectively. The schematic diagram of the clock circuit design is shown in Figure 9 below:

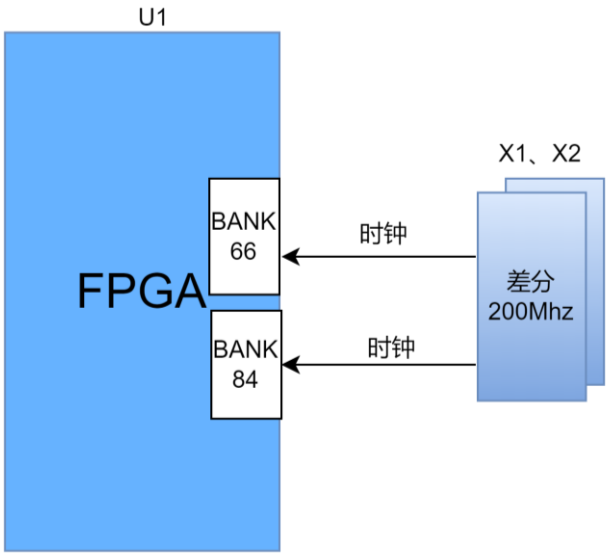

Figure 9: Module Clock Source

FPGA system clock source:

Two 200MHz differential crystals are provided on the board to provide a reference clock for the DDR4 controller and FPGA logic. The output of the crystal oscillator is connected to the global clock of the FPGA BANK66 and BANK84, which can be used to drive the DDR4 controller and user logic circuits in the FPGA. The schematic diagram of the clock source is shown in Figure 10.

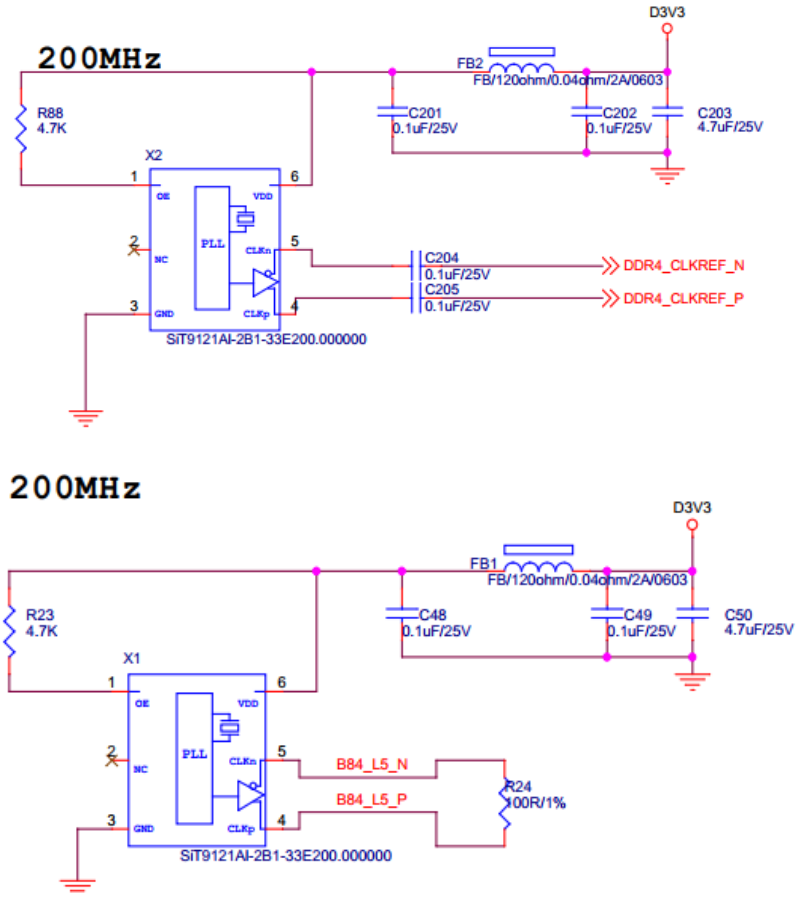

Figure 10: System clock source

Clock pin assignment:

Signal name	FPGA pins
B84_L5_P	AC13
B84_L5_N	AC14
DDR4_CLKREF_P	K22
DDR4_CLKREF_N	K23

Table 6: Clock Pin Assignment

Part 2.6: LED

There are three red LEDs on the ACKU3 module, one of which is a power indicator (PWR1), one of which is a configuration LED (D1), and a user indicator (LED1). The indicator lights up when the core module is powered up, and the configuration LED lights up when the FPGA has configured the program. User indicator lights can be used to customize the function indication. Schematic diagram of hardware connection of LED lamp is shown in Figure 11:

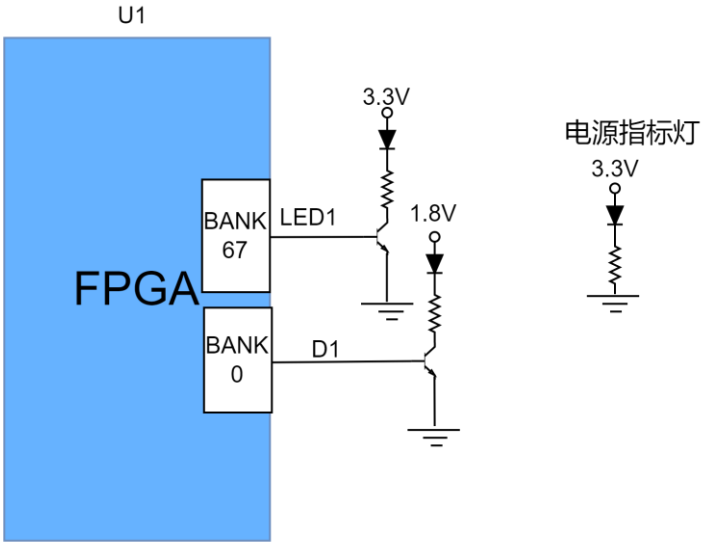

Figure 11: Schematic diagram of hardware connection of LED lamp on Module

Part 2.7: Power Source

The supply voltage of the ACKU3 module is +12V, which is supplied through the connection with base board. The power supply design diagram on the board is shown in Figure 12 below:

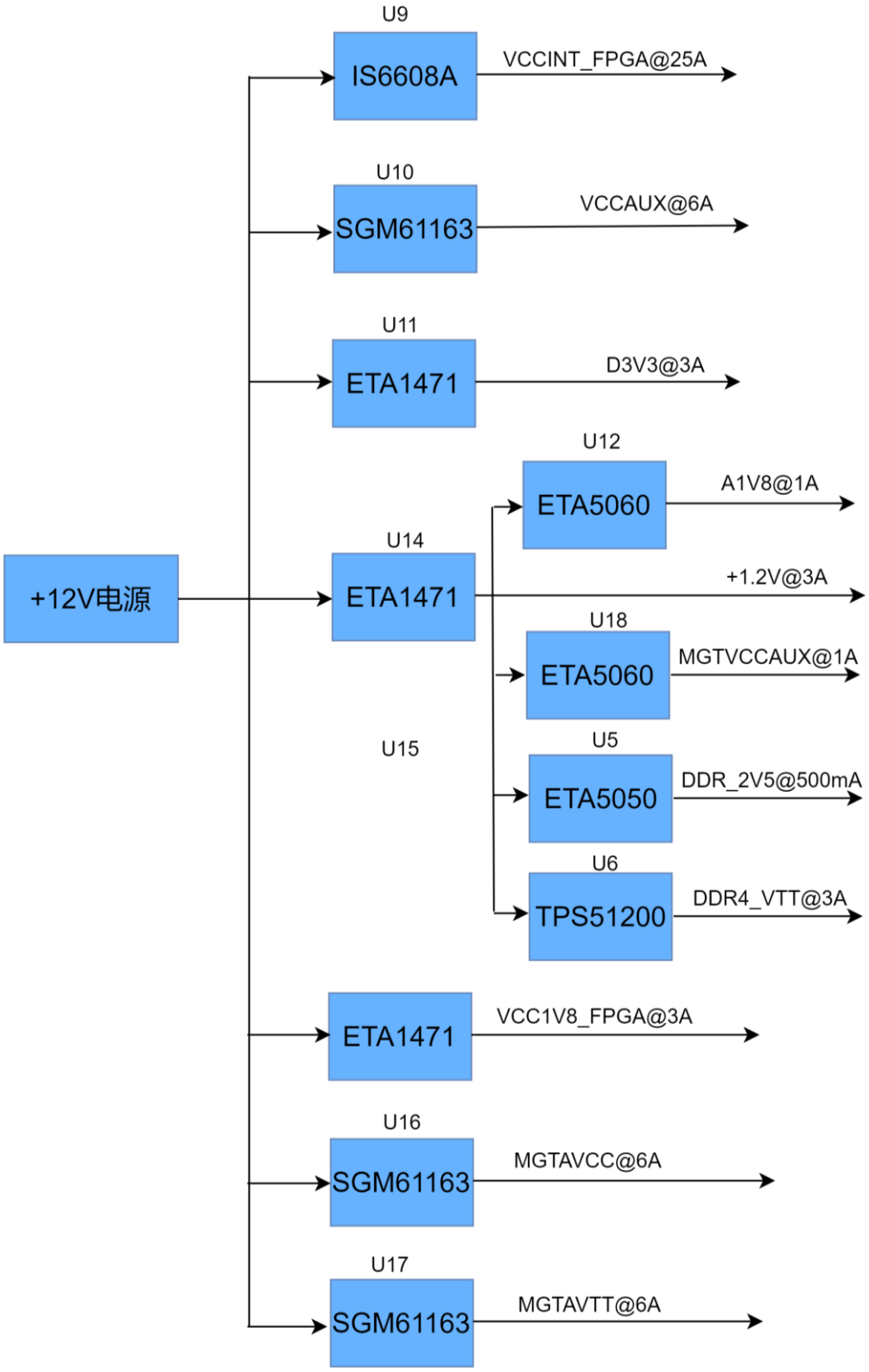

Figure 12: Power interface part in the schematic diagram

The +12V generates the FPGA core power supply through the DCDC power supply chip IS6608, and the output current is up to 25A, which can meet the current demand of the core voltage. The +12V power supply generates VCCAUX, MGTAVCC and MGTAVTT power supplies through three DCDC chips SGM61163 to supply power to the FPGA auxiliary power supply and the high-speed transceiver. At the same time, the +12V power supply generates

+1.2V through the DCDC chip ETA1471, and the VCC1V8 _ FPGA and D3V3 power supplies power to the BANK and peripherals of DDR4 and FPGA. In addition, D3V3 generates the auxiliary power supply of the high-speed transceiver and the ADC power supply + 1.8 V of the FPGA through two LDO chips ETA5060; the VTT and DDR2V5 voltages of DDR4 are generated by TPS51200 and ETA5050.

Because the power supply of FPGA has the requirement of power-on sequence, in the circuit design, we have designed according to the power supply requirements of the chip to ensure the normal work of the chip.

Part 2.8: Structure Diagram

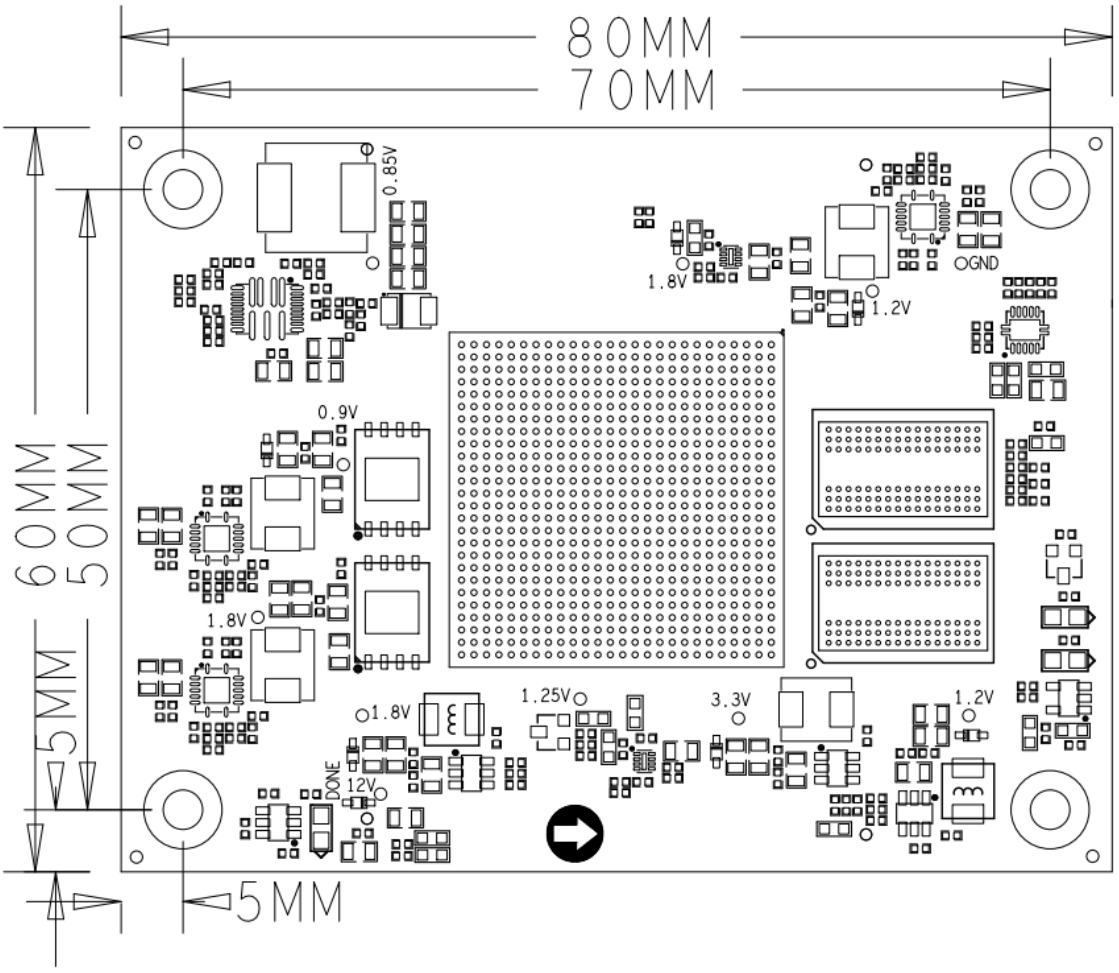

Figure 13: Top View

Part 2.9: Connector Pin Definition

The module is extended with two high-speed expansion ports, which are connected to the base board by two 240Pin inter-board connectors (J1 ~ J2), and the power supply of the module is input by the J2 connector.

Pin Assignments for J1 Connector:

J1 pin	Signal name	FPGA pin number	J1 pin	Signal name	FPGA pin number
A1	POWER_ALT	-	B1	POWER_SDA	-
A2	-	-	B2	POWER_SCL	-
A3	GND	-	B3	GND	-

A4	FPGA_TDI	AB12	B4	FPGA_TCK	AE12
A5	FPGA_TMS	AB10	B5	FPGA_TDO	Y10
A6	GND	-	B6	GND	-
A7	-	-	B7	-	-
A8	-	-	B8	-	-
A9	GND	-	B9	GND	-
A10	-	-	B10	-	-
A11	-	-	B11	-	-
A12	GND	-	B12	GND	-
A13	B87_L3_N	G14	B13	B87_L4_N	J14
A14	B87_L3_P	H14	B14	B87_L4_P	J15
A15	GND	-	B15	GND	-
A16	B87_L2_N	H13	B16	B87_L1_N	H12
A17	B87_L2_P	J13	B17	B87_L1_P	J12
A18	GND	-	B18	GND	-
A19	B87_L5_N	F12	B19	B87_L6_N	F13
A20	B87_L5_P	G12	B20	B87_L6_P	F14
A21	GND	-	B21	GND	-
A22	B87_L7_N	E12	B22	B87_L8_N	D13
A23	B87_L7_P	E13	B23	B87_L8_P	D14
A24	GND	-	B24	GND	-
A25	B87_L10_N	B12	B25	B87_L11_N	A12
A26	B87_L10_P	C12	B26	B87_L11_P	A13
A27	GND	-	B27	GND	-
A28	B87_L9_N	C13	B28	B87_L12_N	A14
A29	B87_L9_P	C14	B29	B87_L12_P	B14
A30	GND	-	B30	GND	-
A31	GND	-	B31	GND	-
A32	MGT226_CLK0_P	P7	B32	MGT226_CLK1_P	M7
A33	MGT226_CLK0_N	P6	B33	MGT226_CLK1_N	M6
A34	GND	-	B34	GND	-
A35	MGT226_TX0_P	N5	B35	MGT226_RX0_P	M2
A36	MGT226_TX0_N	N4	B36	MGT226_RX0_N	M1
A37	GND	-	B37	GND	-
A38	MGT226_TX1_P	L5	B38	MGT226_RX1_P	K2
A39	MGT226_TX1_N	L4	B39	MGT226_RX1_N	K1
A40	GND	-	B40	GND	-
A41	MGT226_TX2_P	J5	B41	MGT226_RX2_P	H2
A42	MGT226_TX2_N	J4	B42	MGT226_RX2_N	H1
A43	GND	-	B43	GND	-
A44	MGT226_TX3_P	G5	B44	MGT226_RX3_P	F2
A45	MGT226_TX3_N	G4	B45	MGT226_RX3_N	F1
A46	GND	-	B46	GND	-
A47	MGT227_CLK1_P	H7	B47	MGT227_CLK0_P	K7

A48	MGT227_CLK1_N	H6	B48	MGT227_CLK0_N	K6
A49	GND	-	B49	GND	-
A50	MGT227_TX0_P	F7	B50	MGT227_RX0_P	D2
A51	MGT227_TX0_N	F6	B51	MGT227_RX0_N	D1
A52	GND	-	B52	GND	-
A53	MGT227_TX1_P	E5	B53	MGT227_RX1_P	C4
A54	MGT227_TX1_N	E4	B54	MGT227_RX1_N	C3
A55	GND	-	B55	GND	-
A56	MGT227_TX2_P	D7	B56	MGT227_RX2_P	B2
A57	MGT227_TX2_N	D6	B57	MGT227_RX2_N	B1
A58	GND	-	B58	GND	-
A59	MGT227_TX3_P	B7	B59	MGT227_RX3_P	A4
A60	MGT227_TX3_N	B6	B60	MGT227_RX3_N	A3

Table 7: Pin Assignments for J1 Connector-1

J1 pin	Signal name	FPGA pin number	J1 pin	Signal name	FPGA pin number
C1	MGT224_TX0_N	AF6	D1	MGT224_RX0_N	AF1
C2	MGT224_TX0_P	AF7	D2	MGT224_RX0_P	AF2
C3	GND	-	D3	GND	-
C4	MGT224_TX1_N	AE8	D4	MGT224_RX1_N	AE3
C5	MGT224_TX1_P	AE9	D5	MGT224_RX1_P	AE4
C6	GND	-	D6	GND	-
C7	MGT224_TX2_N	AD6	D7	MGT224_RX2_N	AD1
C8	MGT224_TX2_P	AD7	D8	MGT224_RX2_P	AD2
C9	GND	-	D9	GND	-
C10	MGT224_TX3_N	AC4	D10	MGT224_RX3_N	AB1
C11	MGT224_TX3_P	AC5	D11	MGT224_RX3_P	AB2
C12	GND	-	D12	GND	-
C13	MGT224_CLK1_N	Y6	D13	MGT224_CLK0_N	AB6
C14	MGT224_CLK1_P	Y7	D14	MGT224_CLK0_P	AB7
C15	GND	-	D15	GND	-
C16	MGT225_TX0_N	AA4	D16	MGT225_RX0_N	Y1
C17	MGT225_TX0_P	AA5	D17	MGT225_RX0_P	Y2
C18	GND	-	D18	GND	-
C19	MGT225_TX1_N	W4	D19	MGT225_RX1_N	V1
C20	MGT225_TX1_P	W5	D20	MGT225_RX1_P	V2
C21	GND	-	D21	GND	-
C22	MGT225_TX2_N	U4	D22	MGT225_RX2_N	T1
C23	MGT225_TX2_P	U5	D23	MGT225_RX2_P	T2
C24	GND	-	D24	GND	-
C25	MGT225_TX3_N	R4	D25	MGT225_RX3_N	P1
C26	MGT225_TX3_P	R5	D26	MGT225_RX3_P	P2
C27	GND	-	D27	GND	-
C28	MGT225_CLK1_N	T6	D28	MGT225_CLK0_N	V6

C29	MGT225_CLK1_P	T7	D29	MGT225_CLK0_P	V7
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-
C32	-	-	D32	-	-
C33	-	-	D33	-	-
C34	GND	-	D34	GND	-
C35	-	-	D35	FPGA_VN_IN	R13
C36	-	-	D36	FPGA_VP_IN	P14
C37	GND	-	D37	GND	-
C38	GND	-	D38	GND	-
C39	B86_L2_N	J10	D39	B86_L4_N	G11
C40	B86_L2_P	J11	D40	B86_L4_P	H11
C41	GND	-	D41	GND	-
C42	B86_L3_N	H9	D42	B86_L1_N	K9
C43	B86_L3_P	J9	D43	B86_L1_P	K10
C44	GND	-	D44	GND	-
C45	B86_L9_N	C9	D45	B86_L5_N	G9
C46	B86_L9_P	D9	D46	B86_L5_P	G10
C47	GND	-	D47	GND	-
C48	B86_L6_N	F9	D48	B86_L10_N	A9
C49	B86_L6_P	F10	D49	B86_L10_P	B9
C50	GND	-	D50	GND	-
C51	B86_L7_N	E10	D51	B86_L8_N	D10
C52	B86_L7_P	E11	D52	B86_L8_P	D11
C53	GND	-	D53	GND	-
C54	B86_L11_N	A10	D54	B86_L12_N	B11
C55	B86_L11_P	B10	D55	B86_L12_P	C11
C56	GND	-	D56	GND	-
C57	-	-	D57	-	-
C58	-	-	D58	-	-
C59	-	-	D59	-	-
C60	-	-	D60	-	-

Table 8: Pin Assignments for J1 Connector-2

Pin Assignments for J2 Connector:

J2 pin	Signal name	FPGA pin number	J2 pin	Signal name	FPGA pin number
A1	+12V	-	B1	+12V	-
A2	-	-	B2	-	-
A3	GND	-	B3	GND	-
A4	VCCIO_65	P22,U23,Y24	B4	VCCIO_64	AA21,AB18,AD22
A5	-	-	B5	-	-
A6	GND	-	B6	GND	-
A7	GND	-	B7	GND	-
A8	-	-	B8	-	-

A9	-	-	B9	-	-
A10	GND	-	B10	GND	-
A11	B84_L2_N	AF13	B11	B84_L1_N	AF15
A12	B84_L2_P	AE13	B12	B84_L1_P	AF14
A13	GND	-	B13	GND	-
A14	B84_L9_N	Y16	B14	B84_L6_N	AB16
A15	B84_L9_P	W16	B15	B84_L6_P	AB15
A16	GND	-	B16	GND	-
A17	B64_L7_N	AF22	B17	B64_L8_N	AE23
A18	B64_L7_P	AE22	B18	B64_L8_P	AD23
A19	GND	-	B19	GND	-
A20	B64_L3_N	AF25	B20	B64_T2U	AE18
A21	B64_L3_P	AF24	B21	B64_T1U	AF20
A22	GND	-	B22	GND	-
A23	B64_L1_N	AE26	B23	B64_L11_N	AE21
A24	B64_L1_P	AE25	B24	B64_L11_P	AD21
A25	GND	-	B25	GND	-
A26	B64_L4_N	AD26	B26	B64_L5_N	AD25
A27	B64_L4_P	AC26	B27	B64_L5_P	AD24
A28	GND	-	B28	GND	-
A29	B64_L6_N	AC24	B29	B64_L9_N	AC23
A30	B64_L6_P	AB24	B30	B64_L9_P	AC22
A31	GND	-	B31	GND	-
A32	B64_L2_N	AB26	B32	B64_L10_N	AB22
A33	B64_L2_P	AB25	B33	B64_L10_P	AA22
A34	GND	-	B34	GND	-
A35	B64_T3U	AC16	B35	B64_L20_N	AB19
A36	B65_T1U	AA23	B36	B64_L20_P	AA19
A37	GND	-	B37	GND	-
A38	B65_L6_N	W20	B38	B65_L9_N	AA25
A39	B65_L6_P	W19	B39	B65_L9_P	AA24
A40	GND	-	B40	GND	-
A41	B65_L1_N	V19	B41	B65_L8_N	Y26
A42	B65_L1_P	U19	B42	B65_L8_P	Y25
A43	GND	-	B43	GND	-
A44	B65_L3_N	U20	B44	B65_L5_N	T23
A45	B65_L3_P	T20	B45	B65_L5_P	T22
A46	GND	-	B46	GND	-
A47	B66_L4_N	L19	B47	B65_L19_N	R23
A48	B66_L4_P	M19	B48	B65_L19_P	R22
A49	GND	-	B49	GND	-
A50	B66_L2_N	M21	B50	B65_L16_N	V26
A51	B66_L2_P	M20	B51	B65_L16_P	U26
A52	GND	-	B52	GND	-
A53	B66_L5_N	J21	B53	B65_T3U	T19
A54	B66_L5_P	K21	B54	-	-
A55	GND	-	B55	GND	-
A56	B66_L3_N	J20	B56	B65_L17_N	P26

A57	B66_L3_P	J19	B57	B65_L17_P	P25
A58	GND	-	B58	GND	-
A59	B66_L1_N	K18	B59	B65_L15_N	P24
A60	B66_L1_P	L18	B60	B65_L15_P	N24

Table 9: Pin Assignments for J2 Connector-1

J2 pin	Signal name	FPGA pin number	J2 pin	Signal name	FPGA pin number
C1	+12V	-	D1	+12V	-
C2	-	-	D2	-	-
C3	GND	-	D3	GND	-
C4	VCCAUX_PG	-	D4	FMC_HPC0_VREF_A_M2C	W18，V18
C5	-	-	D5	-	-
C6	GND	-	D6	GND	-
C7	GND	-	D7	GND	-
C8	B84_L11_N	AA13	D8	B84_L12_N	W13
C9	B84_L11_P	Y13	D9	B84_L12_P	W12
C10	GND	-	D10	GND	-
C11	B84_L3_N	AE15	D11	B84_L10_N	W15
C12	B84_L3_P	AD15	D12	B84_L10_P	W14
C13	GND	-	D13	GND	-
C14	B84_L4_N	AD14	D14	B84_L8_N	AB14
C15	B84_L4_P	AD13	D15	B84_L8_P	AA14
C16	GND	-	D16	GND	-
C17	B64_L17_N	AF17	D17	B84_L7_N	AA15
C18	B64_L17_P	AE17	D18	B84_L7_P	Y15
C19	GND	-	D19	GND	-
C20	B64_L15_N	AF19	D20	B64_L13_N	AE20
C21	B64_L15_P	AF18	D21	B64_L13_P	AD20
C22	GND	-	D22	GND	-
C23	B64_L16_N	AD18	D23	B64_L18_N	AE16
C24	B64_L16_P	AC18	D24	B64_L18_P	AD16
C25	GND	-	D25	GND	-
C26	B64_L14_N	AD19	D26	B64_L22_N	AC17
C27	B64_L14_P	AC19	D27	B64_L22_P	AB17
C28	GND	-	D28	GND	-
C29	B64_L12_N	AC21	D29	B64_L21_N	AB20
C30	B64_L12_P	AB21	D30	B64_L21_P	AA20
C31	GND	-	D31	GND	-
C32	B64_L24_N	AA18	D32	B64_L23_N	AA17
C33	B64_L24_P	Y18	D33	B64_L23_P	Y17
C34	GND	-	D34	GND	-
C35	-	-	D35	B64_L19_N	Y21
C36	-	-	D36	B64_L19_P	Y20
C37	GND	-	D37	GND	-
C38	-	-	D38	USER_DEF_CLOCK_P	J23
C39	-	-	D39	USER_DEF_CLOCK_N	J24

C40	GND	-	D40	GND	-
C41	B65_L10_N	W26	D41	B65_L12_N	W24
C42	B65_L10_P	W25	D42	B65_L12_P	V24
C43	GND	-	D43	GND	-
C44	B65_L11_N	W23	D44	B65_L7_N	Y23
C45	B65_L11_P	V23	D45	B65_L7_P	Y22
C46	GND	-	D46	GND	-
C47	B65_L4_N	V22	D47	B65_L23_N	P19
C48	B65_L4_P	V21	D48	B65_L23_P	N19
C49	GND	-	D49	GND	-
C50	B65_L20_N	P21	D50	B65_L24_N	N22
C51	B65_L20_P	P20	D51	B65_L24_P	N21
C52	GND	-	D52	GND	-
C53	B65_L14_N	U25	D53	B65_L13_N	U24
C54	B65_L14_P	T25	D54	B65_L13_P	T24
C55	GND	-	D55	GND	-
C56	B65_T2U	N26	D56	B65_L18_N	R26
C57	B65_L2_P	U21	D57	B65_L18_P	R25
C58	GND	-	D58	GND	-
C59	-	-	D59	-	-
C60	VCCO_84	AC15,Y24	D60	VCCO_86_87	E9,H10,E14,H25

Table 10: Pin Assignments for J2 Connector-2

Part 3: Base Board

Part 3.1: Introduction

Through the previous function introduction, we can understand the functions of the base board.

- PCIe3.0 x8 interface
- 1 * Gigabit network interface
- 1 * FMC HPC interface
- 1 * MIPI input interface
- USB Uart interface
- Micro SD deck
- 40-pin expansion port
- JTAG debug port
- Led light
- Key

Part 3.2: PCIe Slot

There is a PCIe x8 interface on the AXKU3 base board, which supports PCIe Gen3.0 protocol, and 8 pairs of transceivers are connected to the golden finger of PCIEx8 for data communication.

The receiving and transmitting signals of the PCIe interface are directly connected with the FPGA BANK224 and BANK225 transceivers. The 8-channel TX signals and RX signals are connected to the FPGA transceiver in the form of differential signals. The communication rate of a single channel can be as high as 8G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 14 below, in which the TX transmission signal is connected in AC coupling mode.

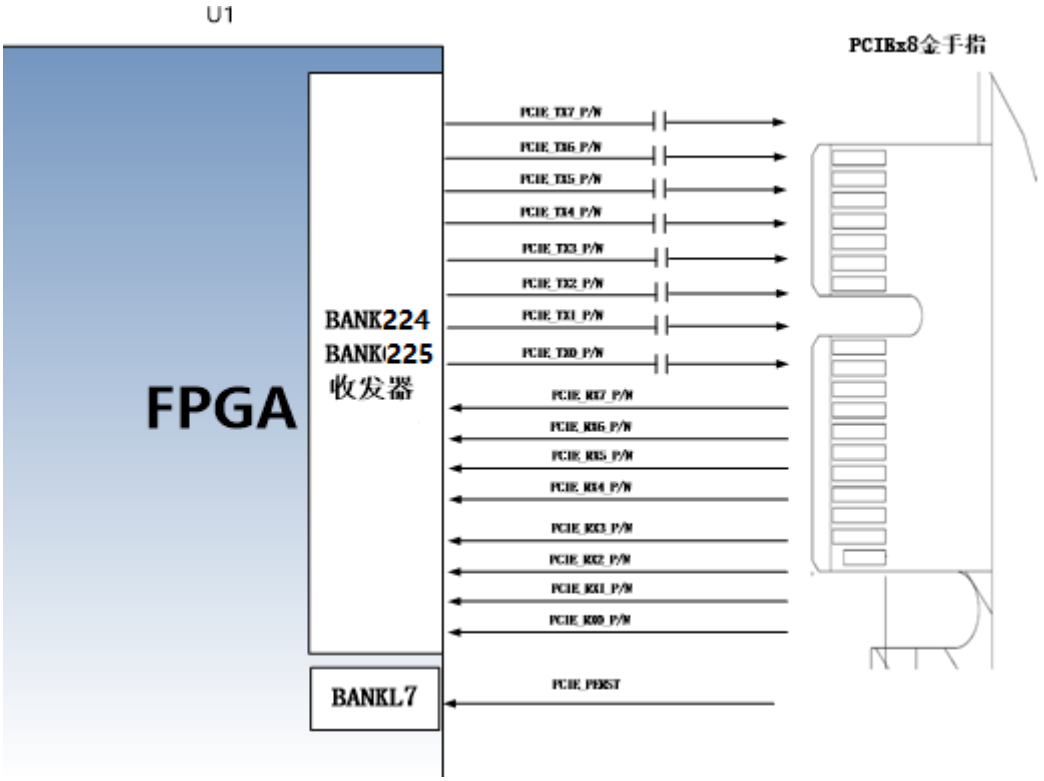

Figure 14: Schematic Diagram of PCIe Slot Design

The PCIe x8 interface FPGA pin assignments are as follows:

Signal name	FPGA pin name	Pin number	Remark
PCIE_RX0_P	MGT225_RX3_P	P2	PCIE channel 0 data receiving positive
PCIE_RX0_N	MGT225_RX3_N	P1	PCIE Channel 0 Data Receive Negative
PCIE_RX1_P	MGT225_RX2_P	T2	PCIE channel 1 data receiving positive
PCIE_RX1_N	MGT225_RX2_N	T1	PCIE Channel 1 Data Receive Negative
PCIE_RX2_P	MGT225_RX1_P	V2	PCIE channel 2 data receiving positive
PCIE_RX2_N	MGT225_RX1_N	V1	PCIE Channel 2 Data Receive Negative
PCIE_RX3_P	MGT225_RX0_P	Y2	PCIE channel 3 data receiving positive
PCIE_RX3_N	MGT225_RX0_N	Y1	PCIE Channel 3 Data Receive Negative
PCIE_RX4_P	MGT224_RX3_P	AB2	PCIE Channel 4 Data Reception Positive
PCIE_RX4_N	MGT224_RX3_N	AB1	PCIE Channel 4 Data Receive Negative
PCIE_RX5_P	MGT224_RX2_P	AD2	PCIE channel 5 data receiving positive
PCIE_RX5_N	MGT224_RX2_N	AD1	PCIE Channel 5 Data Receive Negative
PCIE_RX6_P	MGT224_RX1_P	AE4	PCIE channel 6 data receiving positive
PCIE_RX6_N	MGT224_RX1_N	AE3	PCIE Channel 6 Data Receive Negative
PCIE_RX7_P	MGT224_RX0_P	AF2	PCIE channel 7 data receiving positive
PCIE_RX7_N	MGT224_RX0_N	AF1	PCIE Channel 7 Data Receive Negative
PCIE_TX0_P	MGT225_TX3_P	R5	PCIE channel 0 data sending positive
PCIE_TX0_N	MGT225_TX3_N	R4	PCIE channel 0 data transmission negative
PCIE_TX1_P	MGT225_TX2_P	U5	PCIE Channel 1 Data Sending Positive
PCIE_TX1_N	MGT225_TX2_N	U4	PCIE channel 1 data transmission negative
PCIE_TX2_P	MGT225_TX1_P	W5	PCIE Channel 2 Data Sending Positive
PCIE_TX2_N	MGT225_TX1_N	W4	PCIE channel 2 data transmission negative
PCIE_TX3_P	MGT225_TX0_P	AA5	PCIE Channel 3 Data Sending Positive

PCIE_TX3_N	MGT225_TX0_N	AA4	PCIE channel 3 data transmission negative
PCIE_TX4_P	MGT224_TX3_P	AC5	PCIE Channel 4 Data Sending Positive
PCIE_TX4_N	MGT224_TX3_N	AC4	PCIE channel 4 data transmission negative
PCIE_TX5_P	MGT224_TX2_P	AD7	PCIE Channel 5 Data Sending Positive
PCIE_TX5_N	MGT224_TX2_N	AD6	PCIE channel 5 data transmission negative
PCIE_TX6_P	MGT224_TX1_P	AE9	PCIE Channel 6 Data Sending Positive
PCIE_TX6_N	MGT224_TX1_N	AE8	PCIE channel 6 data transmission negative
PCIE_TX7_P	MGT224_TX0_P	AF7	PCIE Channel 7 Data Sending Positive
PCIE_TX7_N	MGT224_TX0_N	AF6	PCIE channel 7 data transmission negative
PCIE_CLK_P	MGT225_CLK0_P	V7	PCIE channel reference clock positive
PCIE_CLK_N	MGT225_CLK0_N	V6	PCIE channel reference clock negative
FPGA_PCIE_PERST_N	B65_T3U	T19	Reset signal of PCIE board

Table 11: PCIe x8 Interface FPGA Pin Assignments

Part 3.3: Gigabit Network Interface

A JL21221D Ethernet PHY chip is used on the development board to provide network communication services for users. The Ethernet PHY chip is connected to the IO interface of FPGA. JL21221D chip supports 10/100/1,000 Mbps network transmission rate and communicates with FPGA through RGMII interface. JL21221D chip supports MDI/MDX self-adaptation, various speed self-adaptation and Master/Slave self-adaptation and supports register management of PHY by MDIO bus.

When the JL21221D is powered on, it will detect the level status of some specific IOs to determine its own working mode. Table 10 describes the default setting information after the GPHY chip is powered on.

Default configuration values of PHY chip:

Configure the Pin	Explain	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY Address for MDIO/MDC Mode	PHY Address is 001
RXD1_TXDLY	TX clock 2 ns delay	Delay
RXD0_RXDLY	RX clock 2 ns delay	Delay

Table 12: Default configuration values of PHY chip

When the network is connected to Gigabit Ethernet, the data transmission between FPGA and PHY chip JL2121 is communicated through RGMII bus. The transmission clock is 125Mhz, and the data is sampled at the rising edge and falling edge of the clock.

When the network is connected to 100M Ethernet, the data transmission of FPGA and PHY chip JL2121 is communicated through RMII bus, and the transmission clock is 25 Mhz. Data is sampled on the rising and falling edges of the clock.

Figure 15 shows the connection between FPGA and Ethernet PHY chip:

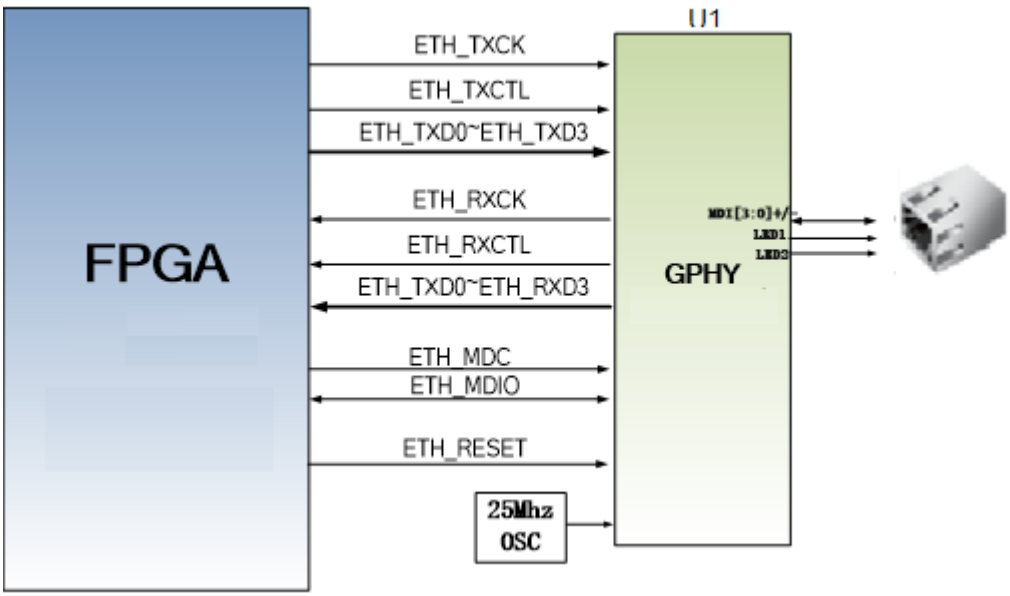

Figure 15: Connection Schematic Diagram of Gigabit Network Interface

Figure 16 is the physical diagram of the Ethernet PHY chip:

Figure 16: Physical Diagram of Ethernet PHY Chip

The FPGA pin assignments for the Ethernet PHY are as follows:

Signal name	FPGA pin number	Remark
ETH_MDC	N26	MDIO manages the clock
ETH_MDIO	U19	MDIO manages data
ETH_RESET	N22	PHY chip reset
ETH_RXCK	U21	RGMII receive clock
ETH_RXCTL	R23	Receive data valid signal
ETH_RXD0	V19	Receive data Bit0
ETH_RXD1	P20	Receive data Bit1
ETH_RXD2	P21	Receive data Bit2
ETH_RXD3	R22	Receive data Bit3
ETH_TXCK	R25	RGMII transmit clock
ETH_TXCTL	R26	Send enable signal
ETH_TXD0	V21	Send data bit0
ETH_TXD1	V22	Send data bit1
ETH_TXD2	N19	Send data bit2
ETH_TXD3	P19	Transmit data bit 3

Table 13: Ethernet PHY Pin Assignment

Part 3.4: FMC HPC Interface

The development board is equipped with an FMC HPC expansion interface, which can be externally connected with XILINX or various FMC modules of Alinx (HDMI input and output module, binocular camera module, high-speed AD module, etc.).

The FMC HPC expansion port contains 34 pairs of differential IO signals, which are respectively connected to the FPGA chips BANK64 and BANK65, and the level standard is 1.8V by default. 8 channels of high-speed GTY transceiving signals are connected to the IO of FPGA chips BANK226 and BANK227.

The schematic diagram of the FPGA and FMC HPC connector is shown in Figure 17:

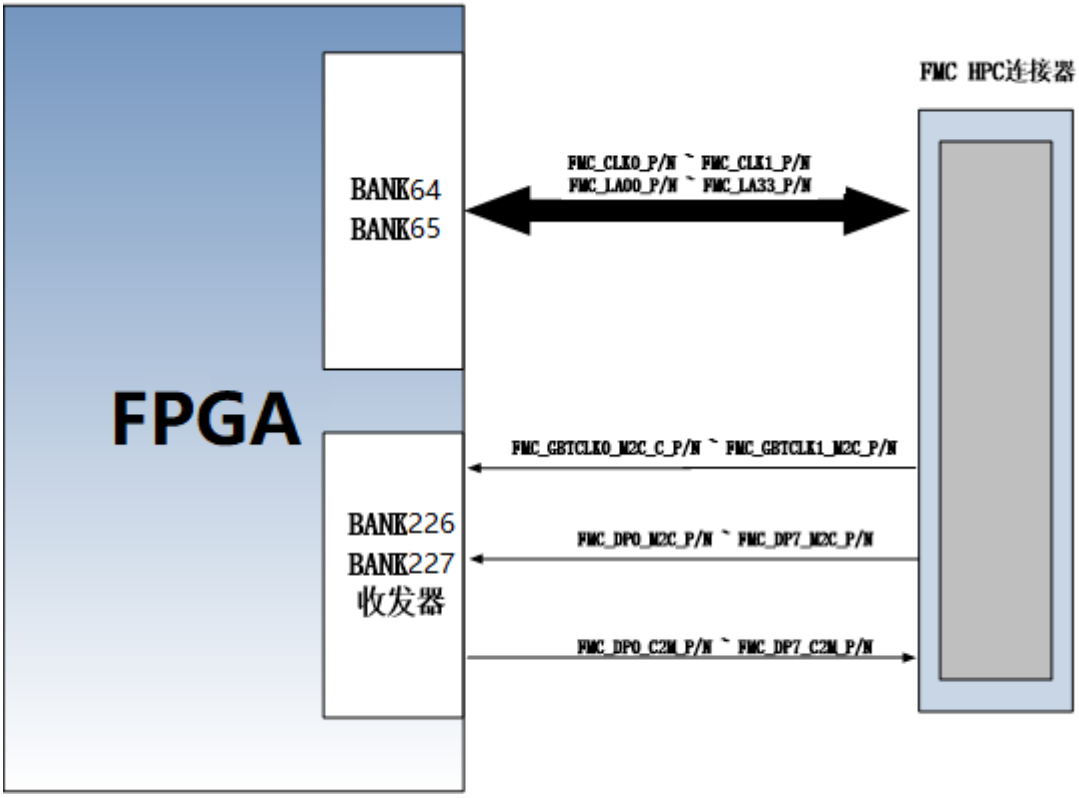

Figure 17: Connection Diagram of HPC FMC

The FMC HPC connector pin assignments are as follows:

Signal name	FPGA pin name	FPGA pin number	Remark
FMC_CLK0_N	B65_L12_N	W24	FMC 0th input reference clock N
FMC_CLK0_P	B65_L12_P	V24	FMC channel 0 input reference clock P
FMC_CLK1_N	B64_L12_N	AC21	FMC 1st input reference clock N
FMC_CLK1_P	B64_L12_P	AB21	FMC 1st input reference clock P
FMC_LA00_CC_N	B65_L14_N	U25	FMC LA Channel 0 Data (Clock) N
FMC_LA00_CC_P	B65_L14_P	T25	FMC LA Channel 0 Data (Clock) P
FMC_LA01_CC_N	B65_L13_N	U24	FMC LA 1st data (clock) N
FMC_LA01_CC_P	B65_L13_P	T24	FMC LA 1st data (clock) P
FMC_LA02_N	B65_L17_N	P26	FMC LA Channel 2 Data N
FMC_LA02_P	B65_L17_P	P25	FMC LA Channel 2 Data P
FMC_LA03_N	B65_L5_N	T23	FMC LA Channel 3 Data N

FMC_LA03_P	B65_L5_P	T22	FMC LA Channel 3 Data P
FMC_LA04_N	B65_L16_N	V26	FMC LA Channel 4 Data N
FMC_LA04_P	B65_L16_P	U26	FMC LA Channel 4 Data P
FMC_LA05_N	B64_L24_N	AA18	FMC LA Channel 5 Data N
FMC_LA05_P	B64_L24_P	Y18	FMC LA Channel 5 Data P
FMC_LA06_N	B65_L10_N	W26	FMC LA Channel 6 Data P
FMC_LA06_P	B65_L10_P	W25	FMC LA Channel 6 Data P
FMC_LA07_N	B65_L9_N	AA25	FMC LA Channel 7 Data N
FMC_LA07_P	B65_L9_P	AA24	FMC LA Channel 7 Data P
FMC_LA08_N	B65_L11_N	W23	FMC LA 8th Channel Data N
FMC_LA08_P	B65_L11_P	V23	FMC LA Channel 8 Data P
FMC_LA09_N	B65_L8_N	Y26	FMC LA Channel 9 Data N
FMC_LA09_P	B65_L8_P	Y25	FMC LA Channel 9 Data P
FMC_LA10_N	B65_L15_N	P24	FMC LA 10th Channel Data N
FMC_LA10_P	B65_L15_P	N24	FMC LA 10th Channel Data P
FMC_LA11_N	B64_L10_N	AB22	FMC LA Channel 11 Data N
FMC_LA11_P	B64_L10_P	AA22	FMC LA Channel 11 Data P
FMC_LA12_N	B65_L7_N	Y23	FMC LA 12th data N
FMC_LA12_P	B65_L7_P	Y22	FMC LA Channel 12 Data P
FMC_LA13_N	B64_L9_N	AC23	FMC LA Channel 13 Data N
FMC_LA13_P	B64_L9_P	AC22	FMC LA Channel 13 Data P
FMC_LA14_N	B64_L7_N	AF22	FMC LA 14th Channel Data N
FMC_LA14_P	B64_L7_P	AE22	FMC LA 14th Channel Data P
FMC_LA15_N	B64_L11_N	AE21	FMC LA Channel 15 Data N
FMC_LA15_P	B64_L11_P	AD21	FMC LA Channel 15 Data P
FMC_LA16_N	B64_L8_N	AE23	FMC LA Channel 16 Data N
FMC_LA16_P	B64_L8_P	AD23	FMC LA Channel 16 Data P
FMC_LA17_CC_N	B64_L14_N	AD19	FMC LA Channel 17 Data (Clock) N
FMC_LA17_CC_P	B64_L14_P	AC19	FMC LA 17th data (clock) P
FMC_LA18_CC_N	B64_L13_N	AE20	FMC LA 18th Data (Clock) N
FMC_LA18_CC_P	B64_L13_P	AD20	FMC LA 18th Data (Clock) P
FMC_LA19_N	B64_L18_N	AE16	FMC LA Channel 19 Data N
FMC_LA19_P	B64_L18_P	AD16	FMC LA Channel 19 Data P
FMC_LA20_N	B64_L16_N	AD18	FMC LA Channel 20 Data N
FMC_LA20_P	B64_L16_P	AC18	FMC LA Channel 20 Data P
FMC_LA21_N	B64_L20_N	AB19	FMC LA Channel 21 Data N
FMC_LA21_P	B64_L20_P	AA19	FMC LA 21th data P
FMC_LA22_N	B64_L21_N	AB20	FMC LA Channel 22 Data N
FMC_LA22_P	B64_L21_P	AA20	FMC LA Channel 22 Data P
FMC_LA23_N	B64_L23_N	AA17	FMC LA Channel 23 Data N
FMC_LA23_P	B64_L23_P	Y17	FMC LA 23rd data P
FMC_LA24_N	B64_L15_N	AF19	FMC LA Channel 24 Data N
FMC_LA24_P	B64_L15_P	AF18	FMC LA Channel 24 Data P
FMC_LA25_N	B64_L6_N	AC24	FMC LA 25th Channel Data N
FMC_LA25_P	B64_L6_P	AB24	FMC LA Channel 25 Data P
FMC_LA26_N	B64_L19_N	Y21	FMC LA Channel 26 Data N
FMC_LA26_P	B64_L19_P	Y20	FMC LA Channel 26 Data P
FMC_LA27_N	B64_L22_N	AC17	FMC LA 27th data N

FMC_LA27_P	B64_L22_P	AB17	FMC LA Channel 27 Data P
FMC_LA28_N	B64_L17_N	AF17	FMC LA 28th Channel Data N
FMC_LA28_P	B64_L17_P	AE17	FMC LA 28th Channel Data P
FMC_LA29_N	B64_L1_N	AE26	FMC LA 29th channel data N
FMC_LA29_P	B64_L1_P	AE25	FMC LA 29th channel data P
FMC_LA30_N	B64_L5_N	AD25	FMC LA 30th data N
FMC_LA30_P	B64_L5_P	AD24	FMC LA 30th data P
FMC_LA31_N	B64_L2_N	AB26	FMC LA 31st Channel Data N
FMC_LA31_P	B64_L2_P	AB25	FMC LA 31st channel data P
FMC_LA32_N	B64_L4_N	AD26	FMC LA 32nd data N
FMC_LA32_P	B64_L4_P	AC26	FMC LA 32nd data P
FMC_LA33_N	B64_L3_N	AF25	FMC LA 33rd Channel Data N
FMC_LA33_P	B64_L3_P	AF24	FMC LA 33rd channel data P
FMC_SCL	B84_L6_P	AB15	FMC I2C-bus clock
FMC_SDA	B84_L6_N	AB16	FMC I2C-bus data
FMC_HPC_GBTCLK0_M2C_C_N	MGT226_CLK1_N	M6	Transceiver Reference Clock 0 Input P
FMC_HPC_GBTCLK0_M2C_C_P	MGT226_CLK1_P	M7	Transceiver Reference Clock 0 Input N
FMC_HPC_GBTCLK1_M2C_C_N	MGT227_CLK1_N	H6	Transceiver Reference Clock 1 Input P
FMC_HPC_GBTCLK1_M2C_C_P	MGT227_CLK1_P	H7	Transceiver Reference Clock 1 Input N
FMC_DP0_M2C_P	MGT226_RX0_P	M2	Transceiver Data 0 Input P
FMC_DP0_M2C_N	MGT226_RX0_N	M1	Transceiver Data 0 Input N
FMC_DP1_M2C_P	MGT226_RX1_P	K2	Transceiver Data 1 Input P
FMC_DP1_M2C_N	MGT226_RX1_N	K1	Transceiver Data 1 Input N
FMC_DP2_M2C_P	MGT226_RX2_P	H2	Transceiver Data 2 Input P
FMC_DP2_M2C_N	MGT226_RX2_N	H1	Transceiver Data 2 Input N
FMC_DP3_M2C_P	MGT226_RX3_P	F2	Transceiver Data 3 Input P
FMC_DP3_M2C_N	MGT226_RX3_N	F1	Transceiver Data 3 Input N
FMC_DP4_M2C_P	MGT227_RX0_P	D2	Transceiver Data 4 Input P
FMC_DP4_M2C_N	MGT227_RX0_N	D1	Transceiver Data 4 Input N
FMC_DP5_M2C_P	MGT227_RX1_P	C4	Transceiver Data 5 Input P
FMC_DP5_M2C_N	MGT227_RX1_N	C3	Transceiver Data 5 Input N
FMC_DP6_M2C_P	MGT227_RX3_P	A4	Transceiver Data 6 Input P
FMC_DP6_M2C_N	MGT227_RX3_N	A3	Transceiver Data 6 Input N
FMC_DP7_M2C_P	MGT227_RX2_P	B2	Transceiver Data 7 Input P
FMC_DP7_M2C_N	MGT227_RX2_N	B1	Transceiver Data 7 Input N
FMC_DP0_C2M_P	MGT226_TX0_P	N5	Transceiver Data 0 Output P
FMC_DP0_C2M_N	MGT226_TX0_N	N4	Transceiver Data 0 Output N
FMC_DP1_C2M_P	MGT226_TX1_P	L5	Transceiver Data 1 Output P
FMC_DP1_C2M_N	MGT226_TX1_N	L4	Transceiver Data 1 Output N
FMC_DP2_C2M_P	MGT226_TX2_P	J5	Transceiver Data 2 Output P
FMC_DP2_C2M_N	MGT226_TX2_N	J4	Transceiver Data 2 Output N
FMC_DP3_C2M_P	MGT226_TX3_P	G5	Transceiver Data 3 Output P
FMC_DP3_C2M_N	MGT226_TX3_N	G4	Transceiver Data 3 Output N
FMC_DP4_C2M_P	MGT227_TX0_P	F7	Transceiver Data 4 Output P
FMC_DP4_C2M_N	MGT227_TX0_N	F6	Transceiver Data 4 Output N
FMC_DP5_C2M_P	MGT227_TX1_P	E5	Transceiver data 5 output P
FMC_DP5_C2M_N	MGT227_TX1_N	E4	Transceiver Data 5 Output N
FMC_DP6_C2M_P	MGT227_TX3_P	B7	Transceiver Data 6 Output P

FMC_DP6_C2M_N	MGT227_TX3_N	B6	Transceiver Data 6 Output N
FMC_DP7_C2M_P	MGT227_TX2_P	D7	Transceiver Data 7 Output P
FMC_DP7_C2M_N	MGT227_TX2_N	D6	Transceiver Data 7 Output N

Table 14: FMC HPC connector pin assignments

Part 3.5: MIPI Interface

AXKU3 base board is equipped with 1 * MIPI lanex4 camera input interface, which is connected to BANK66 and BANK84 of FPGA. The design diagram of connection is shown in Figure 18 below:

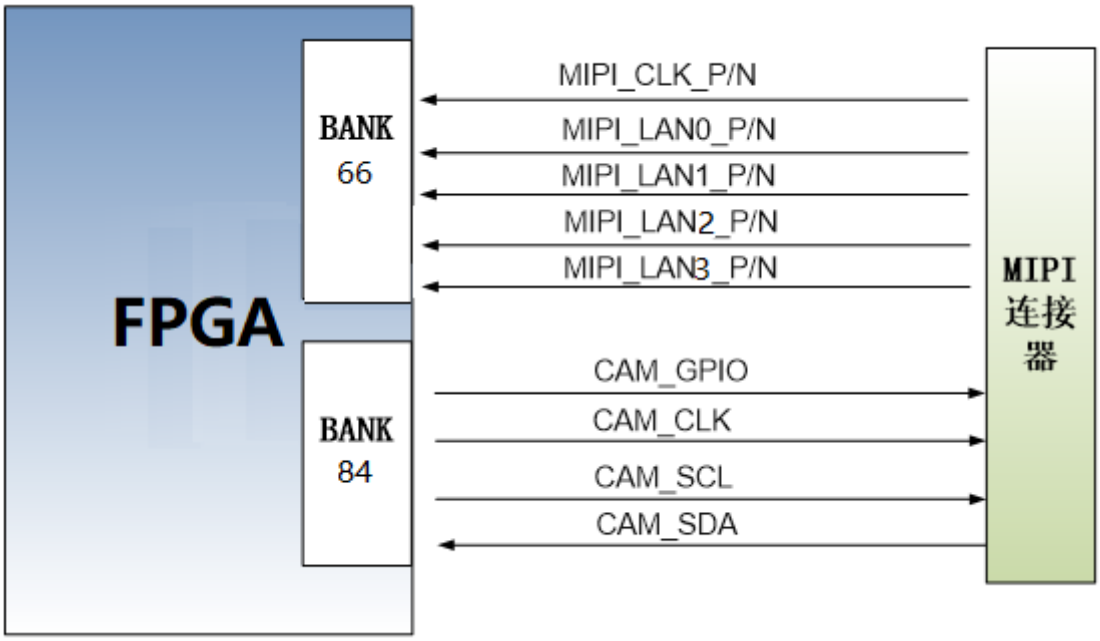

Figure 18: Schematic diagram of MIPI interface design

MIPI interface pin assignment:

Signal name	FPGA pin name	Pin number	Remark
MIPI_CLK_P	B66_L1_P	L18	MIPI Input Clock Positive
MIPI_CLK_N	B66_L1_N	K18	MIPI Input Clock Negative
MIPI_LAN0_P	B66_L5_P	K21	MIPI Input Data LANE0 Positive
MIPI_LAN0_N	B66_L5_N	J21	MIPI input data LANE0 negative
MIPI_LAN1_P	B66_L2_P	M20	MIPI Input Data LANE1 Positive
MIPI_LAN1_N	B66_L2_N	M21	MIPI Input Data LANE1 Negative
MIPI_LAN2_P	B66_L3_P	J19	MIPI Input Data LANE2 Positive
MIPI_LAN2_N	B66_L3_N	J20	MIPI input data LANE2 negative
MIPI_LAN3_P	B66_L4_P	M19	MIPI input data LANE3 positive
MIPI_LAN3_N	B66_L4_N	L19	MIPI input data LANE3 negative
MIPI_CLK	B84_L10_P	W14	Clock input for the camera
MIPI_GPIO	B84_L10_N	W15	GPIO control of the camera
MIPI_I2C_SCL	B84_L8_N	AB14	I2C clock for the camera
MIPI_I2C_SDA	B84_L8_P	AA14	I2C data for the camera

Table 15: MIPI interface pin assignment

Part 3.6: USB To Serial Port

The AXKU3 base board is equipped with an Uart to USB interface for system debugging. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface, which can be connected to the USB port of the upper PC with a USB cable for separate power supply of the module and serial port data communication.

The schematic diagram of the USB Uart circuit design is shown in the following figure:

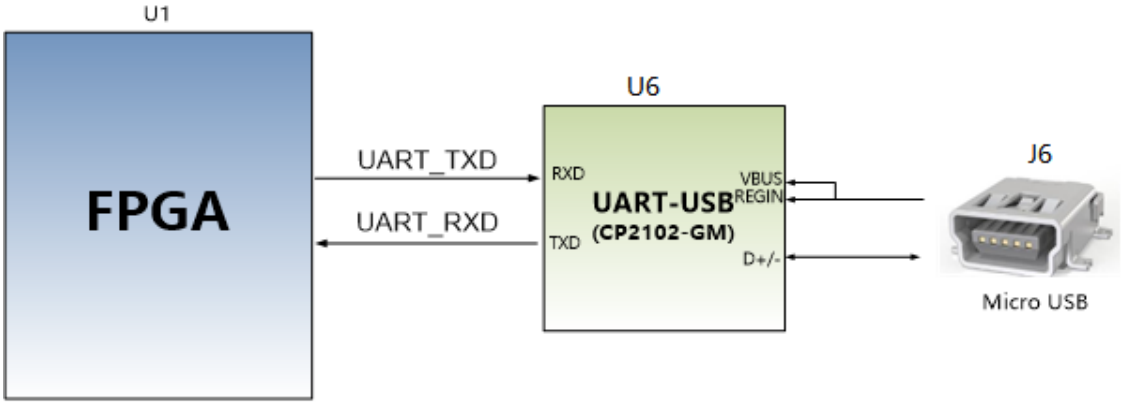

Figure 19: Schematic diagram of USB to serial port

USB to Serial FPGA pin assignment:

Signal name	FPGA pin name	Pin number	Remark
UART_RXD	B84_L3_N	AE15	Uart Data Input
UART_TXD	B84_L3_P	AD15	Uart Data Output

Table 16: USB to Serial FPGA pin assignment

Part 3.7: SD Card Slot

The AXKU3 base board includes a Micro type of SD card interface to provide user access to SD card memory for user data files. The SDIO signal relates to the IO signal of the FPGA, supports the SPI mode and the SD mode, and the SD card used is a MicroSD card. The schematic diagram of FPGA and SD card connector is shown in Figure 20 below.

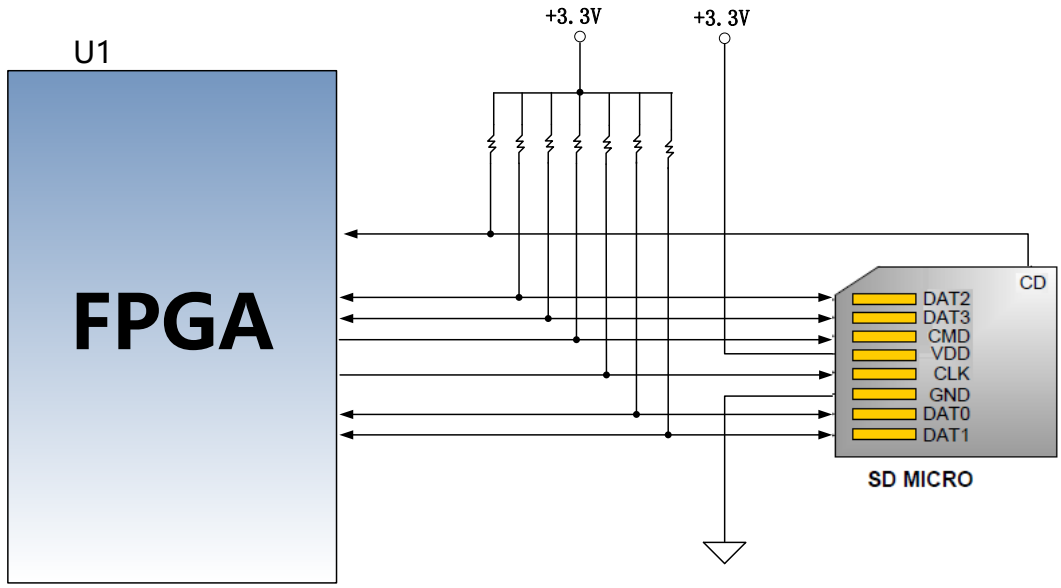

Figure 20: Schematic Diagram of SD Card Slot

SD card slot pin assignment:

Signal name	FPGA pin name	Pin number	Remark
SD_CD	B84_L4_N	AD14	SD chip select signal
SD_CLK	B84_L11_P	Y13	SD clock signal
SD_CMD	B84_L11_N	AA13	SD command signal
SD_D0	B84_L12_N	W13	SD Data 0
SD_D1	B84_L12_P	W12	SD Data 1
SD_D2	B84_L1_N	AF15	SD Data 2
SD_D3	B84_L1_P	AF14	SD Data 3

Table 17: SD card slot pin assignment

Part 3.8: 40 Pin Extension Port

A 40-pin expansion port J8 with a standard pitch of 2.54 mm is reserved on the base board, which is used to connect each module of Alinx, or the external circuit designed by the user. The expansion port has 40 signals, including 1 channel of 5V power supply, 2 channels of 3.3V power supply, 3 channels of ground and 34 channels of IO port. The IO of the expansion port is connected to the IO of the FPGA, and the default is 3.3V.

The pins of the J8 expansion port FPGA are assigned as follows:

J8 pin	Signal name	Pin number	J8 pin	Signal name	Pin number
1	GND	-	2	+5V	-
3	IO1_1N	A10	4	IO1_1P	B10
5	IO1_2N	B11	6	IO1_2P	C11
7	IO1_3N	E10	8	IO1_3P	E11
9	IO1_4N	A9	10	IO1_4P	B9
11	IO1_5N	D10	12	IO1_5P	D11
13	IO1_6N	C9	14	IO1_6P	D9
15	IO1_7N	F9	16	IO1_7P	F10
17	IO1_8N	G9	18	IO1_8P	G10

19	IO1_9N	H9	20	IO1_9P	J9
21	IO1_10N	J10	22	IO1_10P	J11
23	IO1_11N	G11	24	IO1_11P	H11
25	IO1_12N	K9	26	IO1_12P	K10
27	IO1_13N	B12	28	IO1_13P	C12
29	IO1_14N	E12	30	IO1_14P	E13
31	IO1_15N	F12	32	IO1_15P	G12
33	IO1_16N	A12	34	IO1_16P	A13
35	IO1_17N	D13	36	IO1_17P	D14
37	GND	-	38	GND	-
39	+3.3V	-	40	+3.3V	-

Table 18: Pins of the J8 expansion port

Part 3.9: Keys and LED Light

The AXKU3 base board has seven LEDs, one power indicator, two serial communication indicators, and four user LEDs. When the development board is powered on, the power indicator will light up; the four LEDs are connected to the IO of the FPGA, and the user can control the on and off through the program. When the IO voltage connected to the user LED is high, the user LED will light up, and when the IO voltage is low, the user LED will be off. In addition, there are four user keys on the board. The default key signal is high. When the key is pressed, the key level is low. Schematic diagram of hardware connection of user LED light and key is shown in Figure 21:

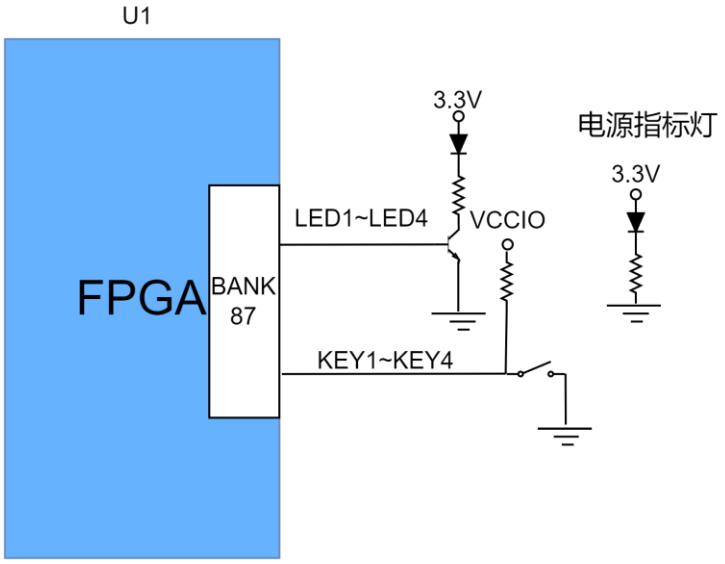

Figure 21: Schematic diagram of hardware connection of user LED light and key

Pin assignments for user LED light and key:

Signal name	FPGA pin name	Pin number	Remark
KEY1	B87_L4_N	J14	User key 1
KEY2	B87_L4_P	J15	User key 2
KEY3	B87_L2_P	J13	User key 3
KEY4	B87_L2_N	H13	User key 4
LED1	B87_L1_P	J12	User LED 1 light

LED2	B87_L3_P	H14	User LED 2 light
LED3	B87_L6_N	F13	User LED3 light
LED4	B87_L1_N	H12	User LED4 light

Table 19: Pin assignments for user LED light and key

Part 3.10: JTAG Debugging Interface

A 10-PIN JTAG interface is reserved on the AXKU3 base board for downloading FPGA programs or solidifying programs to FLASH. To avoid the damage to the FPGA chip caused by live plugging, we add a protection diode on the JTAG signal to ensure that the voltage of the signal is within the acceptable range of the FPGA, to avoid the damage to the chip.

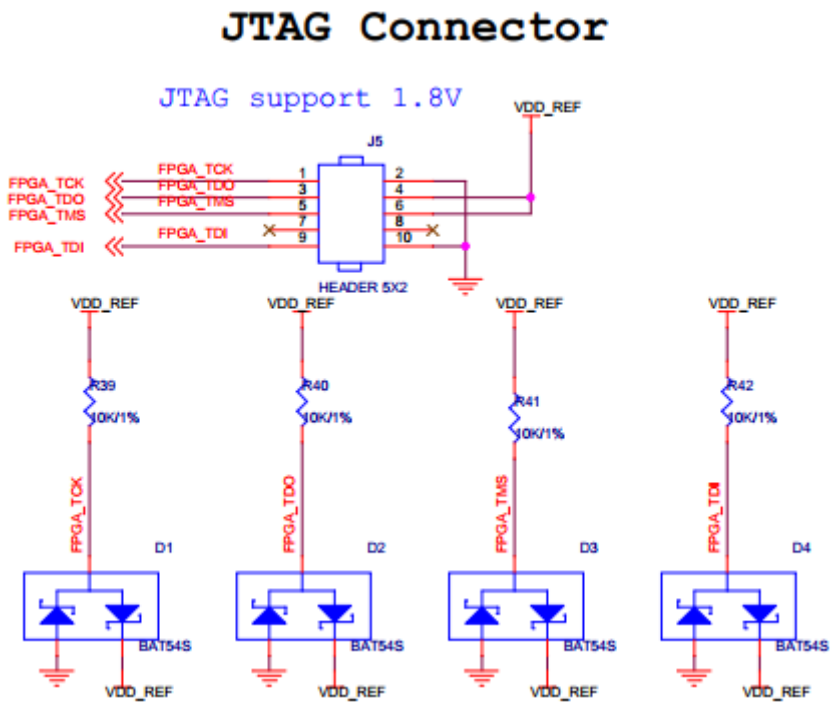

Figure 22: JTAG Interface Part in Schematic Diagram

Part 3.11: Power Source

The power input voltage of the development board is DC12V, which can supply power to the board through the PCIE slot or external +12V power supply. Please use the power supply provided by the development board when supplying power from the external power supply. Do not use the power supply of other specifications to avoid damaging the development board. The external input power supply on the base board is output through a voltage protection chip, and the DC/DC power supply chips ETA8156, ETA1471 and SGM61163 are respectively converted into three power supplies of +5V, +V_ADJ and +3.3V. The +3.3V output at the same time is the voltage required by each FPGA BANK of the multiple LDO output JTAG.

The power supply design diagram on the board is shown in Figure 23 below:

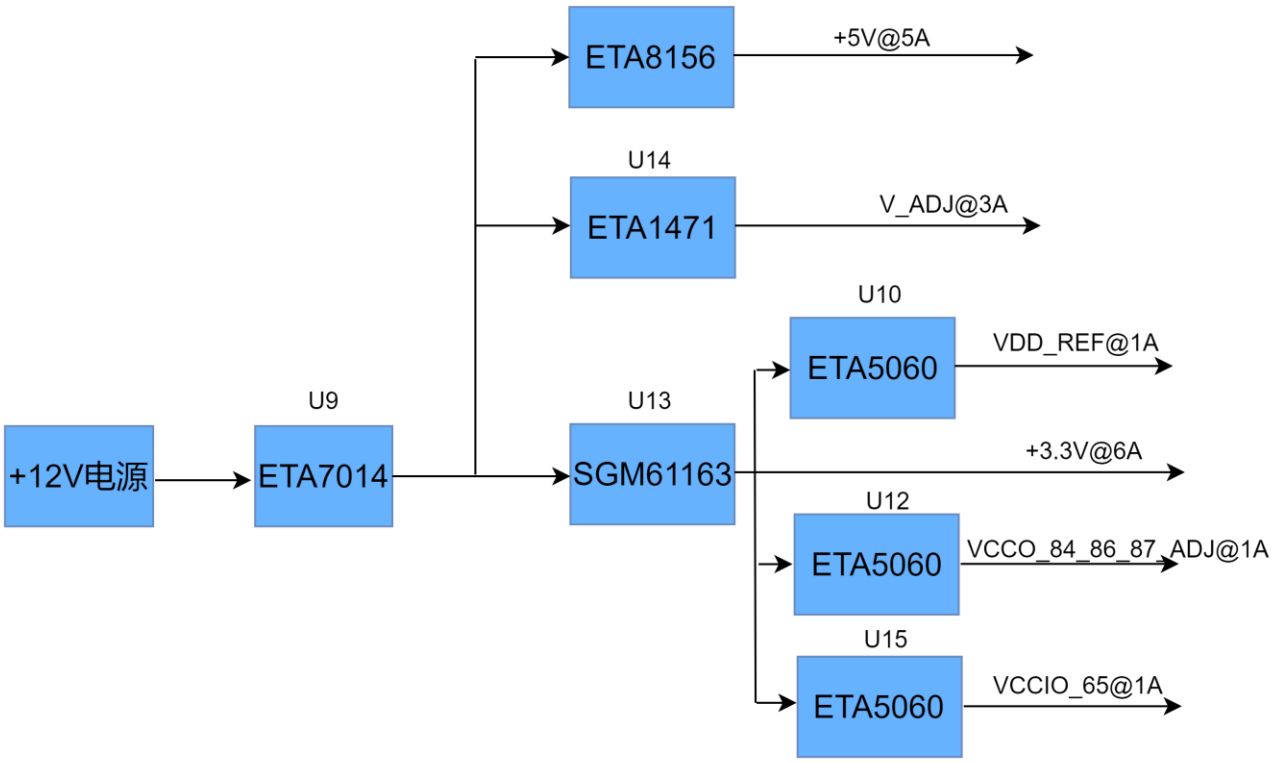

Figure 23: Power interface part in the schematic diagram

The function of each power distribution:

Power source	Function
+5.0V	Power supply of expansion module
V_ADJ	FPGA BANK voltage
+3.3V	Backplane peripheral power supply
VDD_REF	JTAG Power Supply
VCCIO_65	FPGA BANK voltage
VCCO_84_86_87_ADJ	FPGA BANK voltage

Table 20: function of each power distribution

Part 3.12: Structural Dimension Drawing

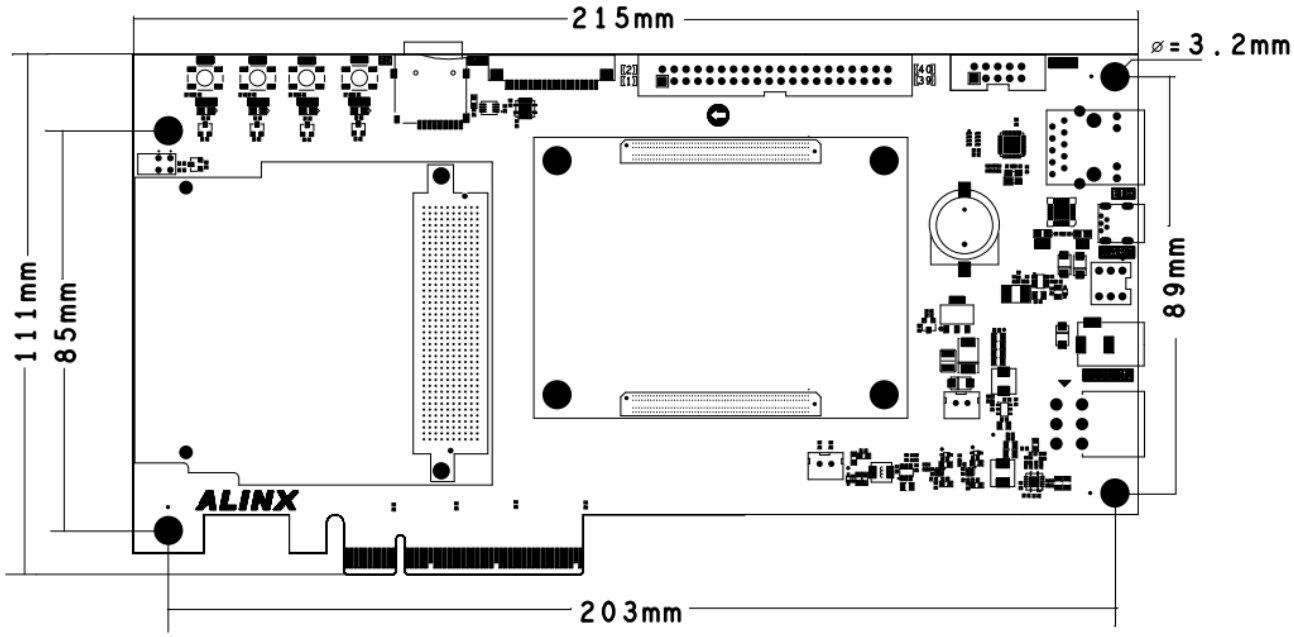

Figure 24: Top View of Structural Dimension Drawing