Kintex UltraScale+FPGA Development Board User Manual

AXKU5

ALINX

Version Record

Version	Modify Record
REV1.0	First Release

Table of Contents

Based on Xilinx FPGA Kintex Ultrascale+ development platform, development board (model: AXKU5) is officially released by Alinx Electronic Technology (Shanghai) Co., Ltd. To let you quickly understand this development platform, we have written this user manual.

This Kintex Ultrascale+ FPGA development platform adopts the core board plus expansion board mode, which is convenient for users to develop and utilize the core board. The core board uses Xilinx's Kintex Ultrascale+ chip xcku5pffvb676 solution, which is mounted with two 1GB high-speed DDR4 SDRAM chips and two 256Mb QSPI FLASH chips.

In the baseboard design, we have extended a wealth of peripheral interfaces for users, such as 1 PCIe3.0x8 interface, 1 FMC HPC interface, 1 Gigabit network interface, 1 MIPI input interface, 1 UART serial interface, 1 SD card interface, 1 40-pin expansion interface and so on. It can meet the user's various high-speed data exchange, video transmission processing and industrial control requirements, and is a "professional" FPGA development platform. It provides the possibility for high-speed data transmission and exchange, early validation and later application of data processing. We believe that such a product is very suitable for students, engineers and other groups engaged in FPGA development.、

Part 1: FPGA Development Board Introduction

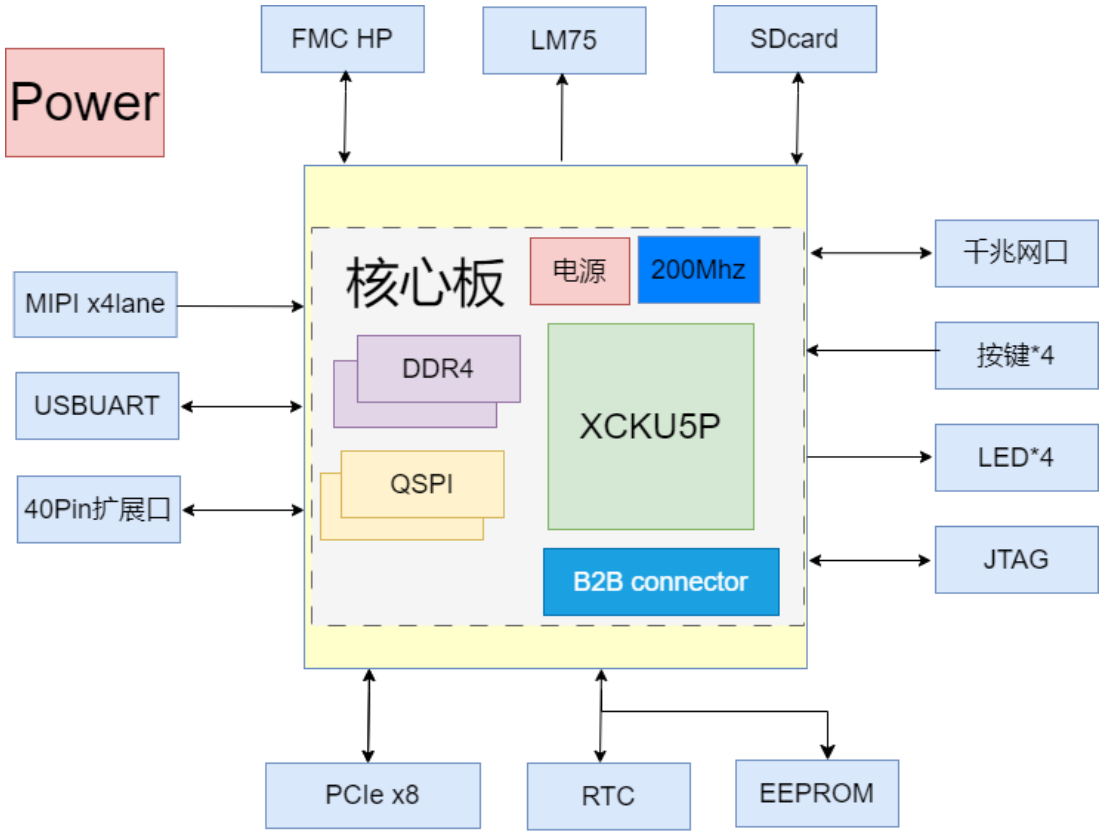
Here is a brief introduction to the functionality of the Kintex Ultrascale+ AXKU5 development platform.

The entire structure of the development board inherited our consistent SoM + expansion board model to design. The SoM and expansion board are connected using high-speed interboard connectors.

The core board is mainly composed of xcku5pffvb676 + 4 DDR4 + QSPI FLASH minimum system. Xilinx's Kintex Ultrascale+ series of chips, model xcku5pffvb676. Two DDR4 memory chips are connected to the HP port of the FPGA chip, each DDR4 capacity up to 1 GB, forming a 32-bit data bandwidth. Two 256Mb QSPI FLASH is used to statically store the FPGA chip's configuration file or other user data.

The carrier board provides a variety of external interfaces for the core board, including one PCIe3.0 x 8 port, one FMC HPC port, one Gigabit network port, one MIPI input port, one UART serial port, one SD card port, one 40-pin expansion port, some buttons and LEDs.

The following is the structure diagram of the whole development system:



Through this diagram, we can see the interfaces and functions that our development platform can contain.

- FPGA SoM Board

It consists of a minimum system of XCKU5P + 2 DDR4 + 2 QSPI FLASH, in addition, two crystal oscillators provide the clock, and two 200MHz crystal oscillators provide the FPGA logic and DDR control reference clock.

- PCIe3.0 x 8 interface

Support PCI Express 3.0 standard, provide standard PCIe x 8 high-speed data transmission interface, single channel communication rate up to 8GBaud.

- 1channel FMC HPC interface

The 8-channel high-speed transceiver in the FPGA is connected to the high-speed pin dedicated to FMC HPC, leading to 34 pairs of LA signal differential pairs and 2 pairs of clock signals of FMC, which can meet the high-speed signal transmission requirements, meet the FMC standard, and can be used for various FMC modules (HDMI input and output modules, high-speed AD modules, etc.).

- 1 Gigabit network port

Gigabit Ethernet interface chip adopts JL2121D Ethernet PHY chip to provide network communication services for users. The chip supports 10/100/1000 Mbps network transmission rate; Full duplex and adaptive.

- 1MIPI input interface

1-channel onboard MIPI lanex4 input port, with a maximum rate of 2.5Gb/s, is used to connect to the MIPI camera module.

- USB Uart interface

1 Uart to USB interface, used to communicate with the computer, convenient user debugging. The serial chip uses the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface uses the MINI USB interface.

- Micro SD card holder

1-channel Micro SD card used to store operating system images and file systems.

- 40 pin expansion port

A 40-pin 2.54mm pitch expansion port can be connected to various modules of black gold (binocular camera, TFT LCD screen, high-speed AD module, etc.). The expansion port contains one 5V power supply, two 3.3V power supplies, three ground power supplies, and 34 I/O ports.

- JTAG Debugging port

A 10-pin 2.54mm standard JTAG port for the download and debugging of FPGA programs, users can debug and download the FPGA system through XILINX downloader.

- LED light

7 LED leds, 3 on the core board, 7 on the base plate. 1 power indicator on the core board; 1 DONE configuration indicator and user indicator. The mainboard has one power indicator, four user indicators, and two serial port indicators.

- Button

4 user buttons on the baseboard.

Part 2: ACKU5 SoM Board

Part 2.1 FPGA Development Board Introduction

ACKU5 (SoM model, the same below) core board, FPGA chip is based on Xilinx FPGA Kintex Ultrascale+ main chip xcku5pffvb676 design. The SoM connects two DDR4 memory chips to the HP port of the FPGA to form 32-bit data bandwidth, and each DDR4 capacity is up to 1GB. The memory bandwidth on the HP side is up to 85Gb/s. In addition, the core board is also integrated with two 256MBit QSPI FLASH, used to start storage configuration and system files.

The SoM uses a board-to-board connector to expand 179 IO, and the level of the outgoing IO can be modified by replacing the LDO chip on the baseboard to meet the user's requirements of non-level interface; In addition, the SoM has been expanded to 16 pairs of high-speed transceiver interfaces. For users who need a lot of IO, this core board will be a good choice. In addition, the IO connection part, the wiring between the FPGA chip and the interface is isometric and differential processing, and the SoM size is only 80*60 (mm), which is very suitable for secondary development.

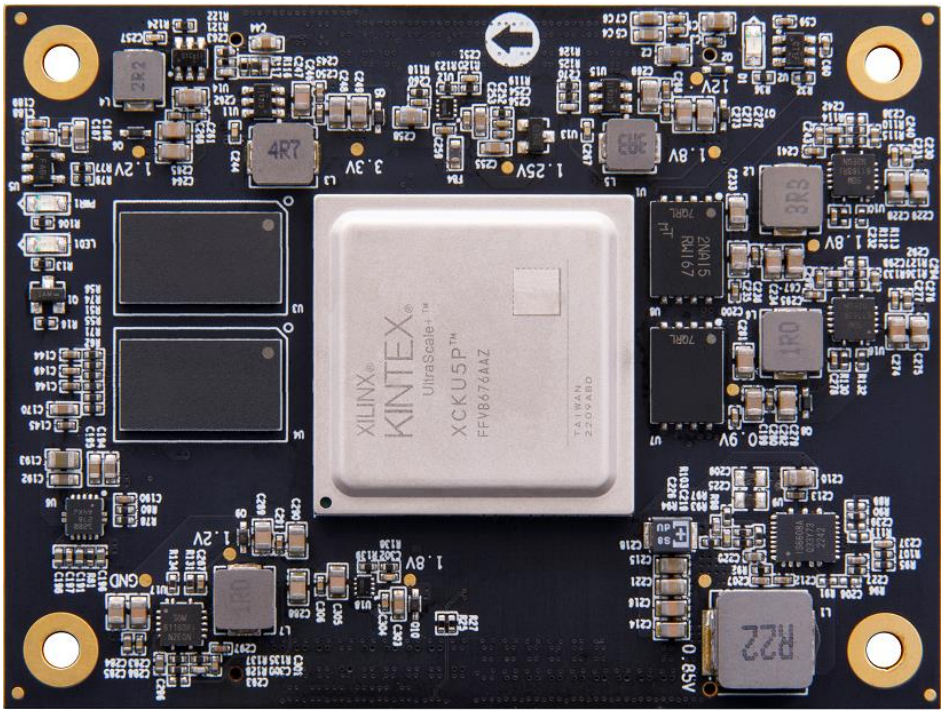


Figure 2-1-1 Front view of ACKU5 core board

Part 2.2 FPGA Chips

As mentioned above, the FPGA model we used is xcku5pffvb676, belonging to Xilinx Company's Kintex Ultrascale+ series products, speed class 6, temperature class industrial. This model is in FFVB676 package with 676 pins. The chip naming rules of Xilinx Kintex Ultrascale+ FPGA are as follows:

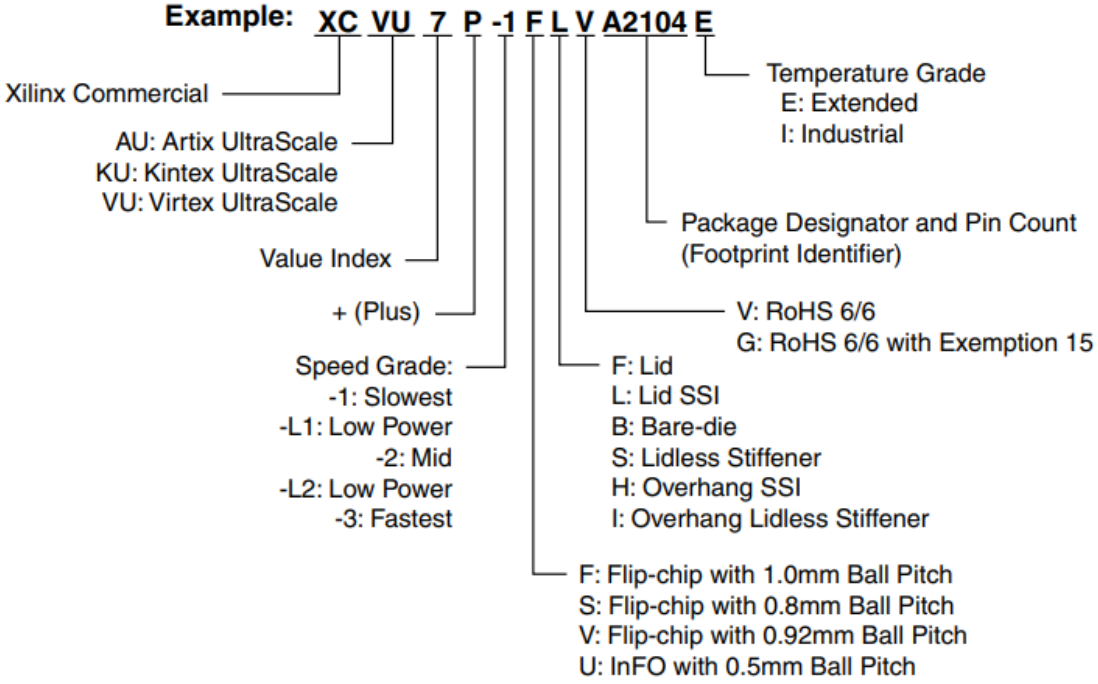


Figure 2-2-1 is the physical diagram of the FPGA chip used in the development board.

Figure 2-2-2 FPGA chip

The main parameters of the FPGA chip are as follows:

Name	Specific parameter
Logic Cells	475K
Flip-flop (FF)	433,920
LUTs	216,960
Total Block RAM	16.9Mb
DSP Slices	1824
CMTs	4
GTY/Gb/s	16/28.21
PCIe Gen3 x16	1
Speed Grade	-6
Temperature Grade	Industrial grade

Part 2.3 DDR4

The ACKU5 development board is equipped with two Micron 1GB DDR4 chips, model MT40A512M16LY-062E, connected to the HP end of the FPGA, composed of 32-bit data bus bandwidth and 2GB capacity. DDR4 SDRAM has a maximum operating data rate of 2666Mbps on the FPGA side, and the two-chip DDR4 memory system is directly connected to the memory interface of BANK 66 and R67. The DDR4 SDRAM configuration is shown in Table 2-3-1 below.

Position	Chip Model	Capacity	Factory
U3、U4	MT40A512M16LY-062E	512Mx 16bit	Micron

Table 2-3-1 DDR4 SDRAM Configuration

DDR4 hardware design needs to strictly consider signal integrity, we have fully considered the matching resistance/terminal resistance, line impedance control, line

isometric control in the circuit design and PCB design, to ensure the high-speed and stable operation of DDR4.

Figure 2-3-1 shows the hardware connection of DDR4 on the FPGA:

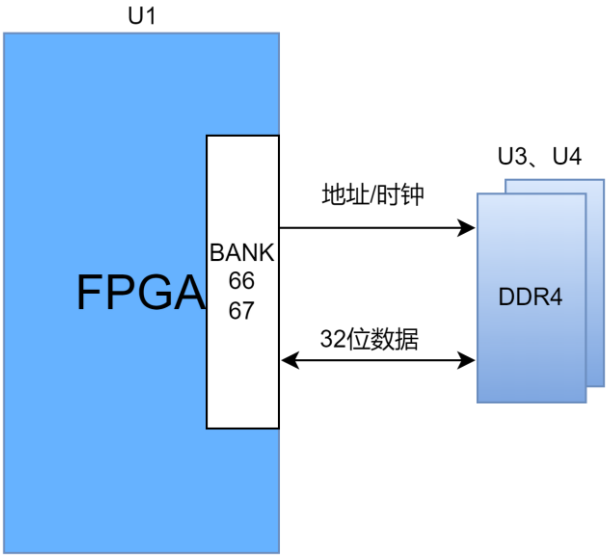
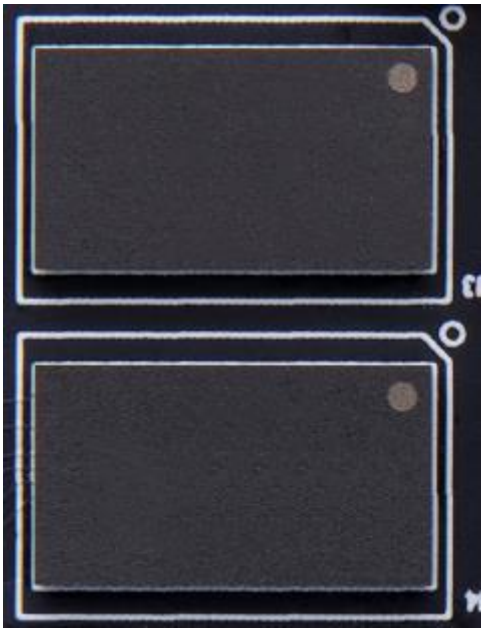


Figure 2-3-1 Schematic diagram of DDR4 DRAM

Figure 2-3-2 Photo of two DDR4 DRAM pieces of the development board



DDR4 SDRAM Pin assignment:

Signal Name	Pin No.
DDR4_D0	C16
DDR4_D1	G16
DDR4_D2	D15

DDR4_D3	G17
DDR4_D4	H17
DDR4_D5	H16
DDR4_D6	D16
DDR4_D7	E15
DDR4_D8	B19
DDR4_D9	C17
DDR4_D10	B20
DDR4_D11	B15
DDR4_D12	A19
DDR4_D13	A15
DDR4_D14	A20
DDR4_D15	B17
DDR4_D16	G20
DDR4_D17	D19
DDR4_D18	D20
DDR4_D19	F19
DDR4_D20	G21
DDR4_D21	E18
DDR4_D22	D18
DDR4_D23	F18
DDR4_D24	C23
DDR4_D25	C22
DDR4_D26	A24
DDR4_D27	B22
DDR4_D28	A25
DDR4_D29	D21
DDR4_D30	B24
DDR4_D31	E21
DDR4_DM0	G15
DDR4_DM1	C18
DDR4_DM2	H18
DDR4_DM3	A22
DDR4_DQS0_N	E17
DDR4_DQS0_P	E16

DDR4_DQS1_N	A18
DDR4_DQS1_P	A17
DDR4_DQS2_N	E20
DDR4_DQS2_P	F20
DDR4_DQS3_N	B21
DDR4_DQS3_P	C21
DDR4_A0	D26
DDR4_A1	D25
DDR4_A2	E26
DDR4_A3	C24
DDR4_A4	C26
DDR4_A5	F24
DDR4_A6	M26
DDR4_A7	B25
DDR4_A8	G26
DDR4_A9	B26
DDR4_A10	E25
DDR4_A11	H26
DDR4_A12	D23
DDR4_A13	F25
DDR4_ACT_B	J26
DDR4_BA0	M25
DDR4_BA1	F23
DDR4_BG0	K26
DDR4_CAS_B	E23
DDR4_CKE	L24
DDR4_CLK_N	G25
DDR4_CLK_P	G24
DDR4_CS_B	D24
DDR4_OTD	H24
DDR4_PAR	J25
DDR4_RAS_B	F22
DDR4_RST	L25
DDR4_WE_B	K25

Part 2.4 QSPI Flash

The SoM board is equipped with two 256MBit Quad-SPI FLASH chips, model MT25QU256ABA1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, in use, it can store FPGA configuration Bin files and other user data files. The specific models and related parameters of QSPI FLASH are shown in Table 2-4-1.

Table 2-4-1 QSPI Flash models and parameters

Position	Chip Model	Capacity	Factory
U7、U8	MT25QU256ABA1EW9	256Mbit	Micron

The QSPI FLASH is connected to the dedicated pins of the FPGA chip, where the clock pin is connected to the CCLK0 dedicated to BANK0, and the data pin is connected to BANK0 and BANK65 respectively. Figure 2-4-1 shows the connection diagram of QSPI Flash and FPGA chip.

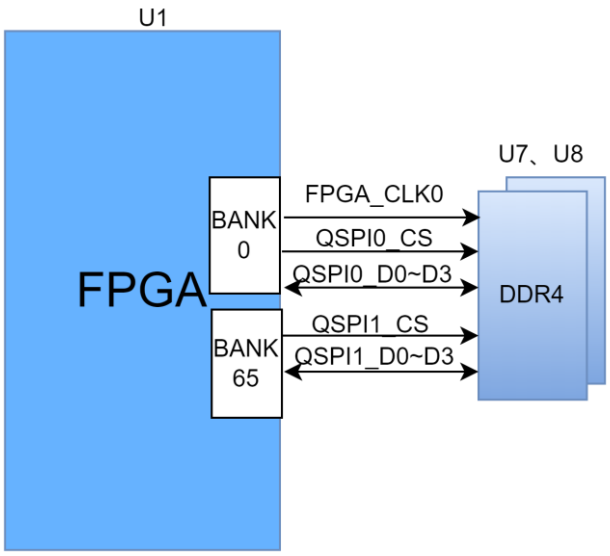


Figure 4-1 QSPI Flash Schematic

Configure chip pin assignment:

Signal Name	FPGA Pin No.
QSPI_CLK	Y11
QSPI0_CS	AA12
QSPI0_DQ0	AD11
QSPI0_DQ1	AC12
QSPI0_DQ2	AC11
QSPI0_DQ3	AE11

QSPI1_CS	U22
QSPI1_DQ0	N23
QSPI1_DQ1	P23
QSPI1_DQ2	R20
QSPI1_DQ3	R21

Part 2.5 Clock configuration

A 200Mhz 2-channel differential active clock is provided on the core board for the FPGA system. The differential clock source is provided for the FPGA logical part. The schematic diagram of the clock circuit design is shown in Figure 2-5-1 below:

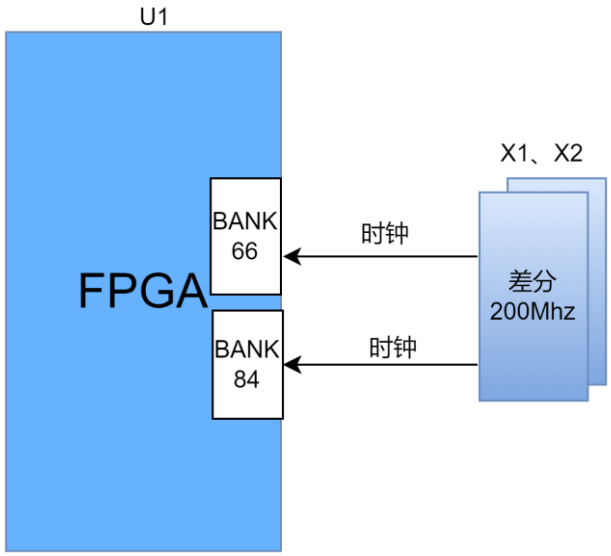


Figure 2-5-1 Clock source on the core board

FPGA system clock source

Two 200MHz differential crystal oscillators are provided on the board to provide reference clocks for the DDR4 controller and FPGA logic. The crystal output is connected to the global clock of the FPGA BANK66 and BANK84, which can be used to drive the DDR4 controller and user logic circuits within the FPGA. Figure 2-5-2 shows the schematic diagram of the clock source.

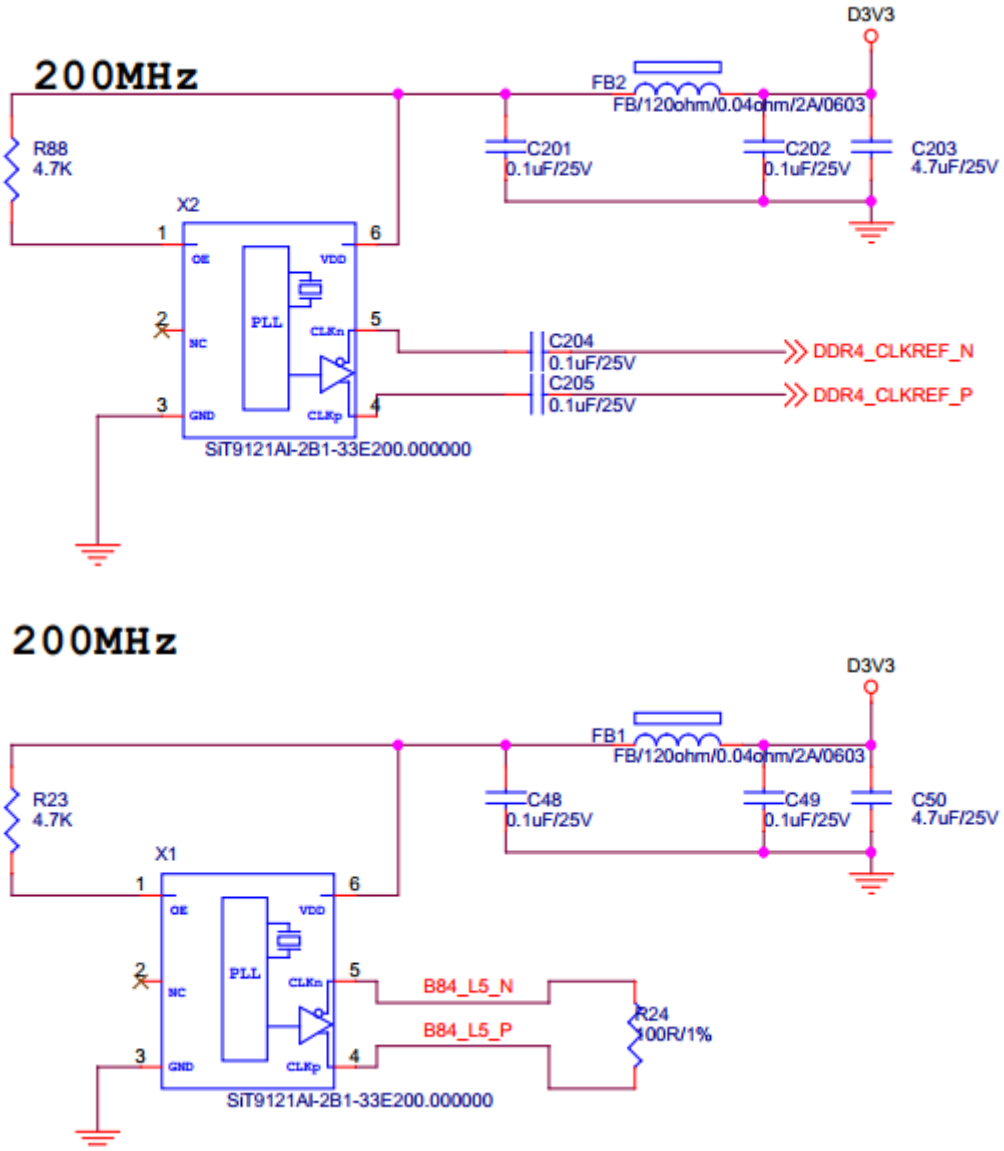


Figure 2-5-2 System clock source

Clock pin assignment:

Signal Name	FPGA Pin
B84_L5_P	AC13
B84_L5_N	AC14
DDR4_CLKREF_P	K22
DDR4_CLKREF_N	K23

Part 2.6 LED Light

The ACKU5 SoM board has three red LED lights, of which 1 is a power indicator

(PWR1), 1 is a configuration LED (D1), and a user indicator (LED1). The indicator light will light up when the core is powered on; When the FPGA is configured, the configuration LED lights up. User indicators can be used to customize function indicators. The schematic diagram of LED light hardware connection is shown in Figure 2-6-1:

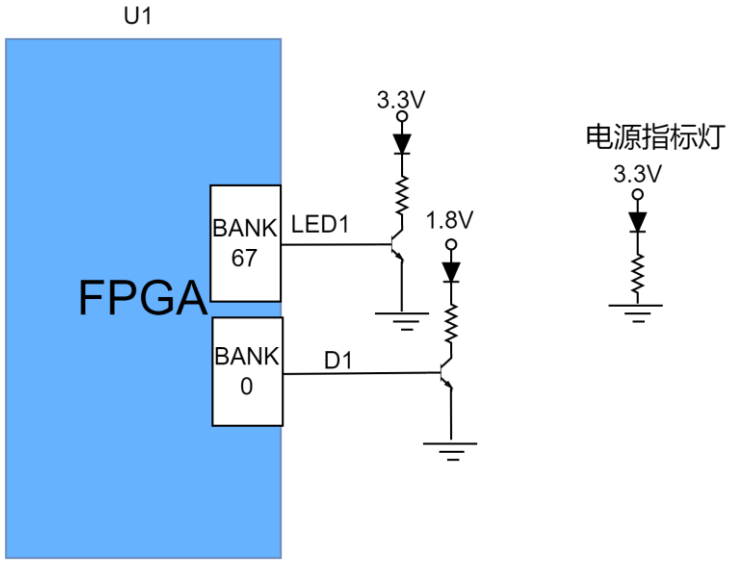


Figure 2-6-1 Schematic diagram of hardware connection of LED lights on the SoM board

Part 2.7 Power Supply

The power supply voltage of the ACKU5 SoM board is +12V, which is connected to the mainboard. The power supply design diagram on the board is shown in Figure 2-7-1 below:

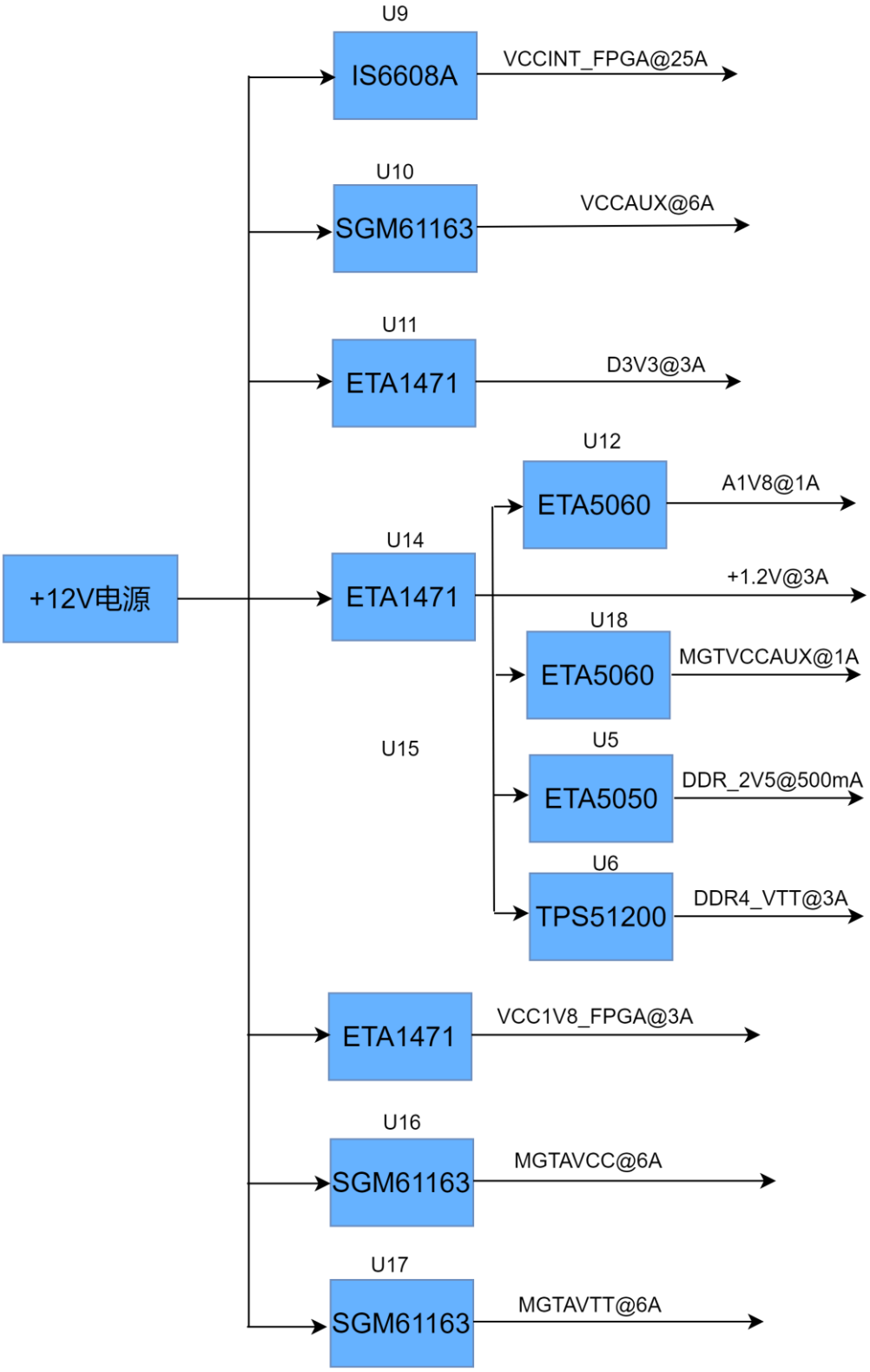


Figure 2-7-1 Schematic diagram of the power interface part

+12V generates FPGA core power supply through DCDC power chip IS6608, with output current up to 25A, which can meet the current requirements of core voltage. +12V power supply and then through 3 DCDC chips SGM61163 to generate VCCAUX,

MGTAVCC, MGTAVTT power supply to FPGA auxiliary power supply and high-speed transceiver power supply. At the same time, the +12V power supply is generated by the DCDC chip ETA1471 to generate +1.2V, VCC1V8_FPGA, D3V3 power supply to the BANK and peripherals of DDR4 and FPGA. In addition, D3V3 generates the auxiliary power supply of the high-speed transceiver and the ADC power supply of the FPGA through two LDO chips, ETA5060, +1.8V; The VTT and DDR2V5 voltages for DDR4 are generated by the TPS51200 and ETA5050.

Due to the requirements of the power-on sequence of the power supply of the FPGA, in the circuit design, we have designed in accordance with the power supply requirements of the chip to ensure the normal operation of the chip.

Part 2.8: Size Dimension

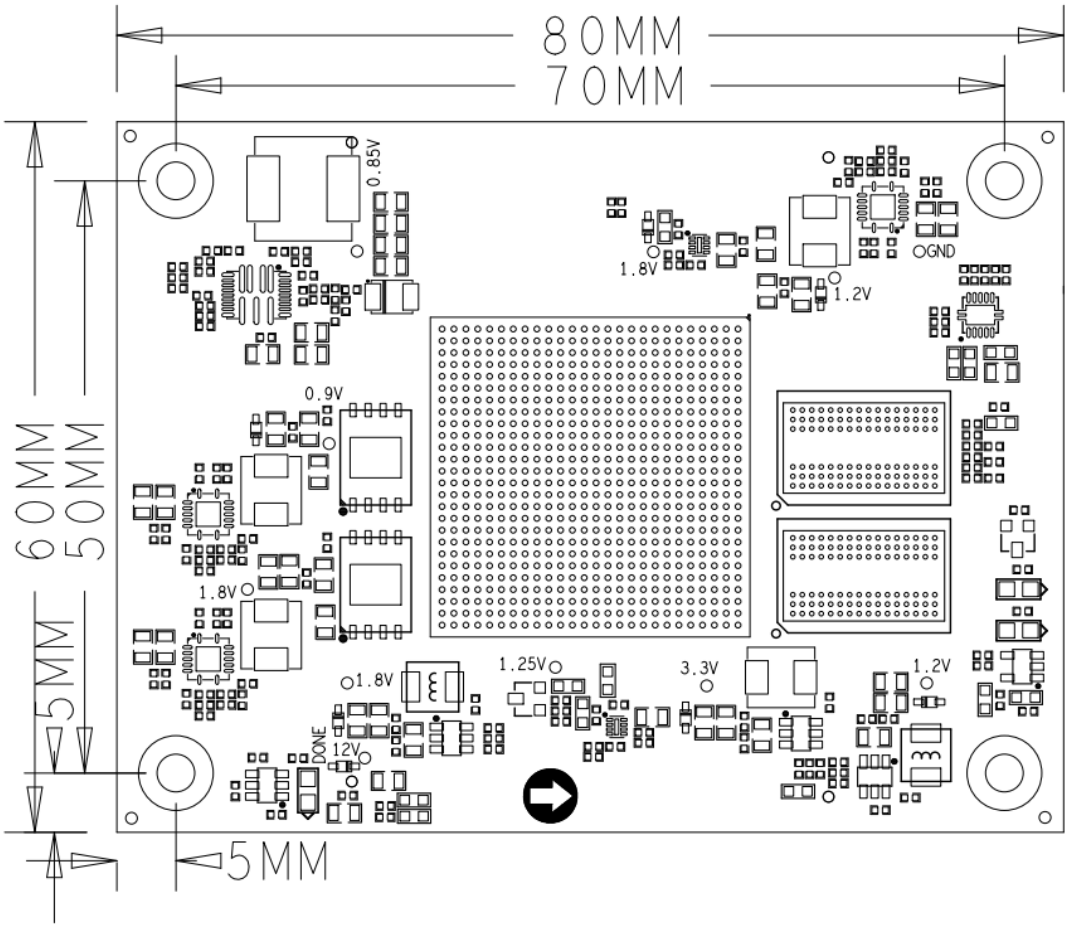


Figure 2-8-1 Top View

Part 2.9: Connector pin definition

The SoM board has two high-speed expansion ports, which are connected to the

baseboard using two 240Pin inter-board connectors (J1 to J2). The power supply of the SoM is input by the J2 connector.

J1 Pin assignment for connectors

J1Pin	Signal Name	FPGA Pin No.	J1Pin	Signal Name	FPGA Pin No.
A1	POWER_ALT	-	B1	POWER_SDA	-
A2	-	-	B2	POWER_SCL	-
A3	GND	-	B3	GND	-
A4	FPGA_TDI	AB12	B4	FPGA_TCK	AE12
A5	FPGA_TMS	AB10	B5	FPGA_TDO	Y10
A6	GND	-	B6	GND	-
A7	-	-	B7	-	-
A8	-	-	B8	-	-
A9	GND	-	B9	GND	-
A10	-	-	B10	-	-
A11	-	-	B11	-	-
A12	GND	-	B12	GND	-
A13	B87_L3_N	G14	B13	B87_L4_N	J14
A14	B87_L3_P	H14	B14	B87_L4_P	J15
A15	GND	-	B15	GND	-
A16	B87_L2_N	H13	B16	B87_L1_N	H12
A17	B87_L2_P	J13	B17	B87_L1_P	J12
A18	GND	-	B18	GND	-
A19	B87_L5_N	F12	B19	B87_L6_N	F13
A20	B87_L5_P	G12	B20	B87_L6_P	F14
A21	GND	-	B21	GND	-
A22	B87_L7_N	E12	B22	B87_L8_N	D13
A23	B87_L7_P	E13	B23	B87_L8_P	D14
A24	GND	-	B24	GND	-
A25	B87_L10_N	B12	B25	B87_L11_N	A12
A26	B87_L10_P	C12	B26	B87_L11_P	A13
A27	GND	-	B27	GND	-
A28	B87_L9_N	C13	B28	B87_L12_N	A14
A29	B87_L9_P	C14	B29	B87_L12_P	B14
A30	GND	-	B30	GND	-
A31	GND	-	B31	GND	-
A32	MGT226_CLK0_	P7	B32	MGT226_CLK1_P	M7

	P				
A33	MGT226_CLK0_N	P6	B33	MGT226_CLK1_N	M6
A34	GND	-	B34	GND	-
A35	MGT226_TX0_P	N5	B35	MGT226_RX0_P	M2
A36	MGT226_TX0_N	N4	B36	MGT226_RX0_N	M1
A37	GND	-	B37	GND	-
A38	MGT226_TX1_P	L5	B38	MGT226_RX1_P	K2
A39	MGT226_TX1_N	L4	B39	MGT226_RX1_N	K1
A40	GND	-	B40	GND	-
A41	MGT226_TX2_P	J5	B41	MGT226_RX2_P	H2
A42	MGT226_TX2_N	J4	B42	MGT226_RX2_N	H1
A43	GND	-	B43	GND	-
A44	MGT226_TX3_P	G5	B44	MGT226_RX3_P	F2
A45	MGT226_TX3_N	G4	B45	MGT226_RX3_N	F1
A46	GND	-	B46	GND	-
A47	MGT227_CLK1_P	H7	B47	MGT227_CLK0_P	K7
A48	MGT227_CLK1_N	H6	B48	MGT227_CLK0_N	K6
A49	GND	-	B49	GND	-
A50	MGT227_TX0_P	F7	B50	MGT227_RX0_P	D2
A51	MGT227_TX0_N	F6	B51	MGT227_RX0_N	D1
A52	GND	-	B52	GND	-
A53	MGT227_TX1_P	E5	B53	MGT227_RX1_P	C4
A54	MGT227_TX1_N	E4	B54	MGT227_RX1_N	C3
A55	GND	-	B55	GND	-
A56	MGT227_TX2_P	D7	B56	MGT227_RX2_P	B2
A57	MGT227_TX2_N	D6	B57	MGT227_RX2_N	B1
A58	GND	-	B58	GND	-
A59	MGT227_TX3_P	B7	B59	MGT227_RX3_P	A4
A60	MGT227_TX3_N	B6	B60	MGT227_RX3_N	A3

J1Pin	Signal Name	FPGA Pin No.	J1Pin	Signal Name	FPGA Pin No.
C1	MGT224_TX0_N	AF6	D1	MGT224_RX0_N	AF1
C2	MGT224_TX0_P	AF7	D2	MGT224_RX0_P	AF2
C3	GND	-	D3	GND	-
C4	MGT224_TX1_N	AE8	D4	MGT224_RX1_N	AE3

C5	MGT224_TX1_P	AE9	D5	MGT224_RX1_P	AE4
C6	GND	-	D6	GND	-
C7	MGT224_TX2_N	AD6	D7	MGT224_RX2_N	AD1
C8	MGT224_TX2_P	AD7	D8	MGT224_RX2_P	AD2
C9	GND	-	D9	GND	-
C10	MGT224_TX3_N	AC4	D10	MGT224_RX3_N	AB1
C11	MGT224_TX3_P	AC5	D11	MGT224_RX3_P	AB2
C12	GND	-	D12	GND	-
C13	MGT224_CLK1_N	Y6	D13	MGT224_CLK0_N	AB6
C14	MGT224_CLK1_P	Y7	D14	MGT224_CLK0_P	AB7
C15	GND	-	D15	GND	-
C16	MGT225_TX0_N	AA4	D16	MGT225_RX0_N	Y1
C17	MGT225_TX0_P	AA5	D17	MGT225_RX0_P	Y2
C18	GND	-	D18	GND	-
C19	MGT225_TX1_N	W4	D19	MGT225_RX1_N	V1
C20	MGT225_TX1_P	W5	D20	MGT225_RX1_P	V2
C21	GND	-	D21	GND	-
C22	MGT225_TX2_N	U4	D22	MGT225_RX2_N	T1
C23	MGT225_TX2_P	U5	D23	MGT225_RX2_P	T2
C24	GND	-	D24	GND	-
C25	MGT225_TX3_N	R4	D25	MGT225_RX3_N	P1
C26	MGT225_TX3_P	R5	D26	MGT225_RX3_P	P2
C27	GND	-	D27	GND	-
C28	MGT225_CLK1_N	T6	D28	MGT225_CLK0_N	V6
C29	MGT225_CLK1_P	T7	D29	MGT225_CLK0_P	V7
C30	GND	-	D30	GND	-
C31	GND	-	D31	GND	-
C32	-	-	D32	-	-
C33	-	-	D33	-	-
C34	GND	-	D34	GND	-
C35	-	-	D35	FPGA_VN_IN	R13
C36	-	-	D36	FPGA_VP_IN	P14
C37	GND	-	D37	GND	-
C38	GND	-	D38	GND	-
C39	B86_L2_N	J10	D39	B86_L4_N	G11
C40	B86_L2_P	J11	D40	B86_L4_P	H11
C41	GND	-	D41	GND	-
C42	B86_L3_N	H9	D42	B86_L1_N	K9

C43	B86_L3_P	J9	D43	B86_L1_P	K10
C44	GND	-	D44	GND	-
C45	B86_L9_N	C9	D45	B86_L5_N	G9
C46	B86_L9_P	D9	D46	B86_L5_P	G10
C47	GND	-	D47	GND	-
C48	B86_L6_N	F9	D48	B86_L10_N	A9
C49	B86_L6_P	F10	D49	B86_L10_P	B9
C50	GND	-	D50	GND	-
C51	B86_L7_N	E10	D51	B86_L8_N	D10
C52	B86_L7_P	E11	D52	B86_L8_P	D11
C53	GND	-	D53	GND	-
C54	B86_L11_N	A10	D54	B86_L12_N	B11
C55	B86_L11_P	B10	D55	B86_L12_P	C11
C56	GND	-	D56	GND	-
C57	-	-	D57	-	-
C58	-	-	D58	-	-
C59	-	-	D59	-	-
C60	-	-	D60	-	-

J2 Pin assignment for connectors

J2 Pin	Signal Name	FPGA Pin No.	J2 Pin	Signal Name	FPGA Pin No.
A1	+12V	-	B1	+12V	-
A2	-	-	B2	-	-
A3	GND	-	B3	GND	-
A4	VCCIO_65	P22,U23,Y24	B4	VCCIO_64	AA21,AB18,AD22
A5	-	-	B5	-	-
A6	GND	-	B6	GND	-
A7	GND	-	B7	GND	-
A8	-	-	B8	-	-
A9	-	-	B9	-	-
A10	GND	-	B10	GND	-
A11	B84_L2_N	AF13	B11	B84_L1_N	AF15
A12	B84_L2_P	AE13	B12	B84_L1_P	AF14
A13	GND	-	B13	GND	-
A14	B84_L9_N	Y16	B14	B84_L6_N	AB16
A15	B84_L9_P	W16	B15	B84_L6_P	AB15
A16	GND	-	B16	GND	-

A17	B64_L7_N	AF22	B17	B64_L8_N	AE23
A18	B64_L7_P	AE22	B18	B64_L8_P	AD23
A19	GND	-	B19	GND	-
A20	B64_L3_N	AF25	B20	B64_T2U	AE18
A21	B64_L3_P	AF24	B21	B64_T1U	AF20
A22	GND	-	B22	GND	-
A23	B64_L1_N	AE26	B23	B64_L11_N	AE21
A24	B64_L1_P	AE25	B24	B64_L11_P	AD21
A25	GND	-	B25	GND	-
A26	B64_L4_N	AD26	B26	B64_L5_N	AD25
A27	B64_L4_P	AC26	B27	B64_L5_P	AD24
A28	GND	-	B28	GND	-
A29	B64_L6_N	AC24	B29	B64_L9_N	AC23
A30	B64_L6_P	AB24	B30	B64_L9_P	AC22
A31	GND	-	B31	GND	-
A32	B64_L2_N	AB26	B32	B64_L10_N	AB22
A33	B64_L2_P	AB25	B33	B64_L10_P	AA22
A34	GND	-	B34	GND	-
A35	B64_T3U	AC16	B35	B64_L20_N	AB19
A36	B65_T1U	AA23	B36	B64_L20_P	AA19
A37	GND	-	B37	GND	-
A38	B65_L6_N	W20	B38	B65_L9_N	AA25
A39	B65_L6_P	W19	B39	B65_L9_P	AA24
A40	GND	-	B40	GND	-
A41	B65_L1_N	V19	B41	B65_L8_N	Y26
A42	B65_L1_P	U19	B42	B65_L8_P	Y25
A43	GND	-	B43	GND	-
A44	B65_L3_N	U20	B44	B65_L5_N	T23
A45	B65_L3_P	T20	B45	B65_L5_P	T22
A46	GND	-	B46	GND	-
A47	B66_L4_N	L19	B47	B65_L19_N	R23
A48	B66_L4_P	M19	B48	B65_L19_P	R22
A49	GND	-	B49	GND	-
A50	B66_L2_N	M21	B50	B65_L16_N	V26
A51	B66_L2_P	M20	B51	B65_L16_P	U26
A52	GND	-	B52	GND	-

A53	B66_L5_N	J21	B53	B65_T3U	T19
A54	B66_L5_P	K21	B54	-	-
A55	GND	-	B55	GND	-
A56	B66_L3_N	J20	B56	B65_L17_N	P26
A57	B66_L3_P	J19	B57	B65_L17_P	P25
A58	GND	-	B58	GND	-
A59	B66_L1_N	K18	B59	B65_L15_N	P24
A60	B66_L1_P	L18	B60	B65_L15_P	N24

J2 Pin	Signal Name	FPGA Pin No.	J2 Pin	Signal Name	FPGA Pin No.
C1	+12V	-	D1	+12V	-
C2	-	-	D2	-	-
C3	GND	-	D3	GND	-
C4	VCCAUX_PG	-	D4	FMC_HPC0_VREF_A_M2C	W18，V18
C5	-	-	D5	-	-
C6	GND	-	D6	GND	-
C7	GND	-	D7	GND	-
C8	B84_L11_N	AA13	D8	B84_L12_N	W13
C9	B84_L11_P	Y13	D9	B84_L12_P	W12
C10	GND	-	D10	GND	-
C11	B84_L3_N	AE15	D11	B84_L10_N	W15
C12	B84_L3_P	AD15	D12	B84_L10_P	W14
C13	GND	-	D13	GND	-
C14	B84_L4_N	AD14	D14	B84_L8_N	AB14
C15	B84_L4_P	AD13	D15	B84_L8_P	AA14
C16	GND	-	D16	GND	-
C17	B64_L17_N	AF17	D17	B84_L7_N	AA15
C18	B64_L17_P	AE17	D18	B84_L7_P	Y15
C19	GND	-	D19	GND	-
C20	B64_L15_N	AF19	D20	B64_L13_N	AE20
C21	B64_L15_P	AF18	D21	B64_L13_P	AD20
C22	GND	-	D22	GND	-
C23	B64_L16_N	AD18	D23	B64_L18_N	AE16
C24	B64_L16_P	AC18	D24	B64_L18_P	AD16
C25	GND	-	D25	GND	-

C26	B64_L14_N	AD19	D26	B64_L22_N	AC17
C27	B64_L14_P	AC19	D27	B64_L22_P	AB17
C28	GND	-	D28	GND	-
C29	B64_L12_N	AC21	D29	B64_L21_N	AB20
C30	B64_L12_P	AB21	D30	B64_L21_P	AA20
C31	GND	-	D31	GND	-
C32	B64_L24_N	AA18	D32	B64_L23_N	AA17
C33	B64_L24_P	Y18	D33	B64_L23_P	Y17
C34	GND	-	D34	GND	-
C35	-	-	D35	B64_L19_N	Y21
C36	-	-	D36	B64_L19_P	Y20
C37	GND	-	D37	GND	-
C38	-	-	D38	USER_DEF_CLOCK_P	J23
C39	-	-	D39	USER_DEF_CLOCK_N	J24
C40	GND	-	D40	GND	-
C41	B65_L10_N	W26	D41	B65_L12_N	W24
C42	B65_L10_P	W25	D42	B65_L12_P	V24
C43	GND	-	D43	GND	-
C44	B65_L11_N	W23	D44	B65_L7_N	Y23
C45	B65_L11_P	V23	D45	B65_L7_P	Y22
C46	GND	-	D46	GND	-
C47	B65_L4_N	V22	D47	B65_L23_N	P19
C48	B65_L4_P	V21	D48	B65_L23_P	N19
C49	GND	-	D49	GND	-
C50	B65_L20_N	P21	D50	B65_L24_N	N22
C51	B65_L20_P	P20	D51	B65_L24_P	N21
C52	GND	-	D52	GND	-
C53	B65_L14_N	U25	D53	B65_L13_N	U24
C54	B65_L14_P	T25	D54	B65_L13_P	T24
C55	GND	-	D55	GND	-
C56	B65_T2U	N26	D56	B65_L18_N	R26
C57	B65_L2_P	U21	D57	B65_L18_P	R25
C58	GND	-	D58	GND	-
C59	-	-	D59	-	-
C60	VCCO_84	AC15,Y24	D60	VCCO_86_87	E9,H10,E14,H25

Part 3: Expansion Board

Part 3.1: Introduction

Through the previous function introduction, we can understand the functions of the expansion board.

- PCIe3.0 x8 interface
- 1-channel Gigabit network port
- 1-channel FMC HPC port
- 1-channel MIPI input interface
- USB Uart interface
- Micro SD card holder
- 40 pin expansion port
- JTAG Debugging interface.
- LED lights
- KEYS

Part 3.2: PCIe slots

The AXKU5 expansion board has a PCIe x8 interface that supports the PCIe Gen3.0 protocol, and the 8-pair transceiver is connected to the golden finger of the PCIEx8 for data communication.

The receiving and sending signals of the PCIe interface are directly connected to the FPGA BANK224 and BANK225 transceivers, and the 8 TX signals and RX signals are connected to the FPGA transceiver in the way of differential signals, and the single-channel communication rate can be as high as 8G bit bandwidth.

The design diagram of the PCIe interface of the development board is shown in Figure 3-2-1, where the TX sending signal is connected in AC coupling mode.

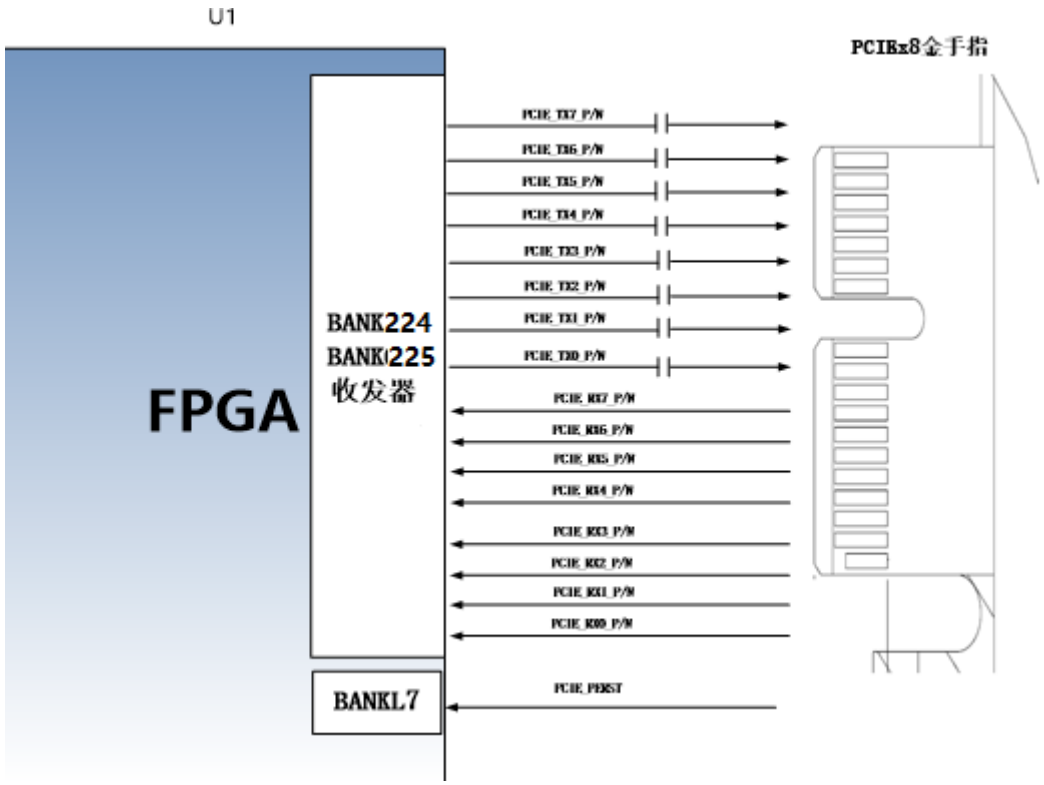


Figure 3-2-1 PCIe slot design

PCIe x8 interface FPGA Pin allocation is as follows:

Signal Name	FPGA Pin Name	Pin No.	Description
PCIE_RX0_P	MGT225_RX3_P	P2	PCIE Channel 0 Data reception P
PCIE_RX0_N	MGT225_RX3_N	P1	PCIE Channel 0 Data reception N
PCIE_RX1_P	MGT225_RX2_P	T2	PCIE Channel 1 Data reception P
PCIE_RX1_N	MGT225_RX2_N	T1	PCIE Channel Data reception N
PCIE_RX2_P	MGT225_RX1_P	V2	PCIE Channel 2 Data reception P
PCIE_RX2_N	MGT225_RX1_N	V1	PCIE Channel 2 Data reception N
PCIE_RX3_P	MGT225_RX0_P	Y2	PCIE Channel 3 Data reception P
PCIE_RX3_N	MGT225_RX0_N	Y1	PCIE Channel 3 Data reception N
PCIE_RX4_P	MGT224_RX3_P	AB2	PCIE Channel 4 Data reception P
PCIE_RX4_N	MGT224_RX3_N	AB1	PCIE Channel 4 Data reception N
PCIE_RX5_P	MGT224_RX2_P	AD2	PCIE Channel 5 Data reception P
PCIE_RX5_N	MGT224_RX2_N	AD1	PCIE Channel 5 Data reception N
PCIE_RX6_P	MGT224_RX1_P	AE4	PCIE Channel 6 Data reception P
PCIE_RX6_N	MGT224_RX1_N	AE3	PCIE Channel 6 Data reception N
PCIE_RX7_P	MGT224_RX0_P	AF2	PCIE Channel 7 Data reception P

PCIE_RX7_N	MGT224_RX0_N	AF1	PCIE Channel 7 Data reception N
PCIE_TX0_P	MGT225_TX3_P	R5	PCIE Channel 0 Data transmission P
PCIE_TX0_N	MGT225_TX3_N	R4	PCIE Channel 0 Data transmission N
PCIE_TX1_P	MGT225_TX2_P	U5	PCIE Channel 1 Data transmission P
PCIE_TX1_N	MGT225_TX2_N	U4	PCIE Channel 1 Data transmission N
PCIE_TX2_P	MGT225_TX1_P	W5	PCIE Channel 2 Data transmission P
PCIE_TX2_N	MGT225_TX1_N	W4	PCIE Channel 2 Data transmission N
PCIE_TX3_P	MGT225_TX0_P	AA5	PCIE Channel 3 Data transmission P
PCIE_TX3_N	MGT225_TX0_N	AA4	PCIE Channel 3 Data transmission N
PCIE_TX4_P	MGT224_TX3_P	AC5	PCIE Channel 4 Data transmission P
PCIE_TX4_N	MGT224_TX3_N	AC4	PCIE Channel 4 Data transmission N
PCIE_TX5_P	MGT224_TX2_P	AD7	PCIE Channel 5 Data transmission P
PCIE_TX5_N	MGT224_TX2_N	AD6	PCIE Channel 5 Data transmission N
PCIE_TX6_P	MGT224_TX1_P	AE9	PCIE Channel 6 Data transmission P
PCIE_TX6_N	MGT224_TX1_N	AE8	PCIE Channel 6 Data transmission N
PCIE_TX7_P	MGT224_TX0_P	AF7	PCIE Channel 7 Data transmission P
PCIE_TX7_N	MGT224_TX0_N	AF6	PCIE Channel 7 Data transmission N
PCIE_CLK_P	MGT225_CLK0_P	V7	PCIE Channel Reference clock P
PCIE_CLK_N	MGT225_CLK0_N	V6	PCIE Channel Reference clock N
FPGA_PCIE_PERST_N	B65_T3U	T19	PCIE Reset signal of the board

Part 3.3: Gigabit Ethernet Interface

There is one Gigabit Ethernet interface on AXKU5 development board. The GPHY chip uses JL21221D chip to provide users with network communication services. The Ethernet PHY chip is connected to the IO interface of the FPGA. The JL21221D chip supports 10/100/1000 Mbps network transmission rate and communicates with the FPGA through the RGMII interface. JL21221D chip supports MDI/MDX adaptation, various speed adaptation, Master/Slave adaptation, and supports MDIO bus for PHY register management.

When the JL21221D is powered on, it detects some specific IO level states to determine its own working mode. Table 3-2-1 describes the default Settings of the

GPHY chip after it is powered on.

Table 3-2-1 Default configuration values of PHY chip

Configuration Pin	Instructions	Configuration value
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	MDIO/MDC Mode PHY Address	PHY Address 001
RXD1_TXDLY	TX Clock 2ns delay	delay
RXD0_RXDLY	RX Clock 2ns delay	delay

When the network is connected to Gigabit Ethernet, the data transmission of the FPGA and PHY chip JL2121 is communicated through the RGMII bus, the transmission clock is 125Mhz, and the data is sampled on the rising edge and falling sample of the clock.

When the network is connected to 100 Gigabit Ethernet, the data transmission of the FPGA and PHY chip JL2121 is communicated through the RMII bus, and the transmission clock is 25Mhz. Data is sampled on the rising edge and falling samples of the clock.

Figure 3-3-1 shows the connection diagram between FPGA and Ethernet PHY chip:

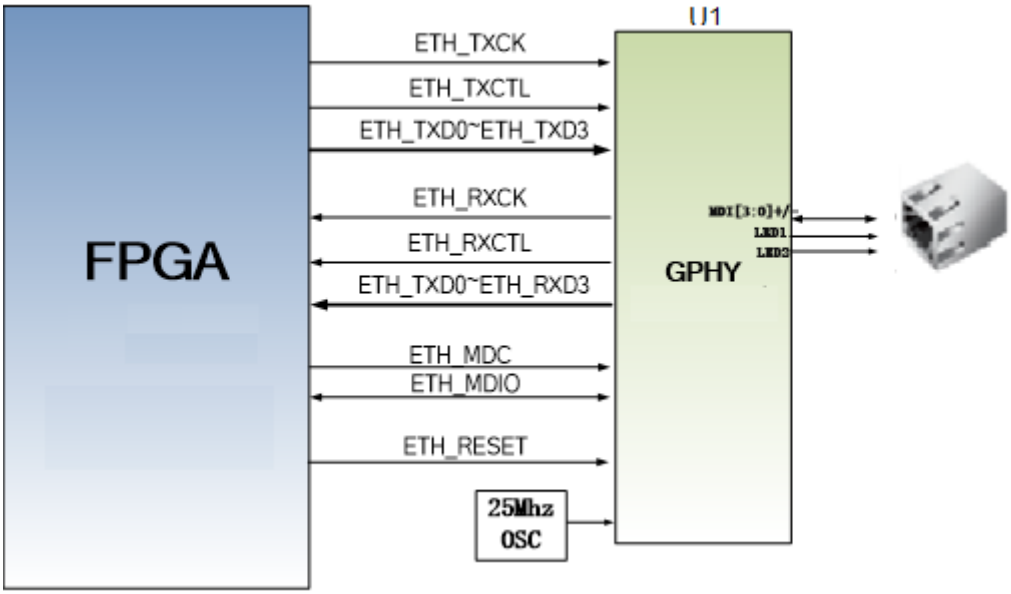


Figure 3-3-1 Schematic diagram of Gigabit network interface connection

Figure 3-3-2 shows the physical diagram of the Ethernet PHY chip

The FPGA pin assignment for an Ethernet PHY is as follows:

Signal Name	FPGA Pin No.	Description
ETH_MDC	N26	MDIO Management clock
ETH_MDIO	U19	MDIO Management data
ETH_RESET	N22	PHY chip reset
ETH_RXCK	U21	RGMII Receive clock
ETH_RXCTL	R23	Receive data valid signal
ETH_RXD0	V19	Receive data Bit0
ETH_RXD1	P20	Receive data Bit1
ETH_RXD2	P21	Receive data Bit2
ETH_RXD3	R22	Receive data Bit3
ETH_TXCK	R25	RGMII transmit clock
ETH_TXCTL	R26	Transmit enable signal
ETH_TXD0	V21	Transmit data bit0
ETH_TXD1	V22	Transmit data bit1
ETH_TXD2	N19	Transmit data bit2
ETH_TXD3	P19	Transmit data bit3

Part 3.4: FMC HPC Interface

The development board has 1 FMC HPC expansion port, which can be connected to XILINX or various FMC modules of our ALINX (HDMI input and output module, binocular camera module, high-speed AD module, etc.).

The FMC HPC expansion port contains 34 pairs of differential IO signals, respectively connected to the FPGA chip BANK64, BANK65, the level standard is 1.8V by default. 8 high-speed GTY transceiver signals are connected to FPGA chip BANK226, BANK227 IO.

The schematic diagram of the FPGA and FMC HPC connectors is shown in Figure 3-4-1:

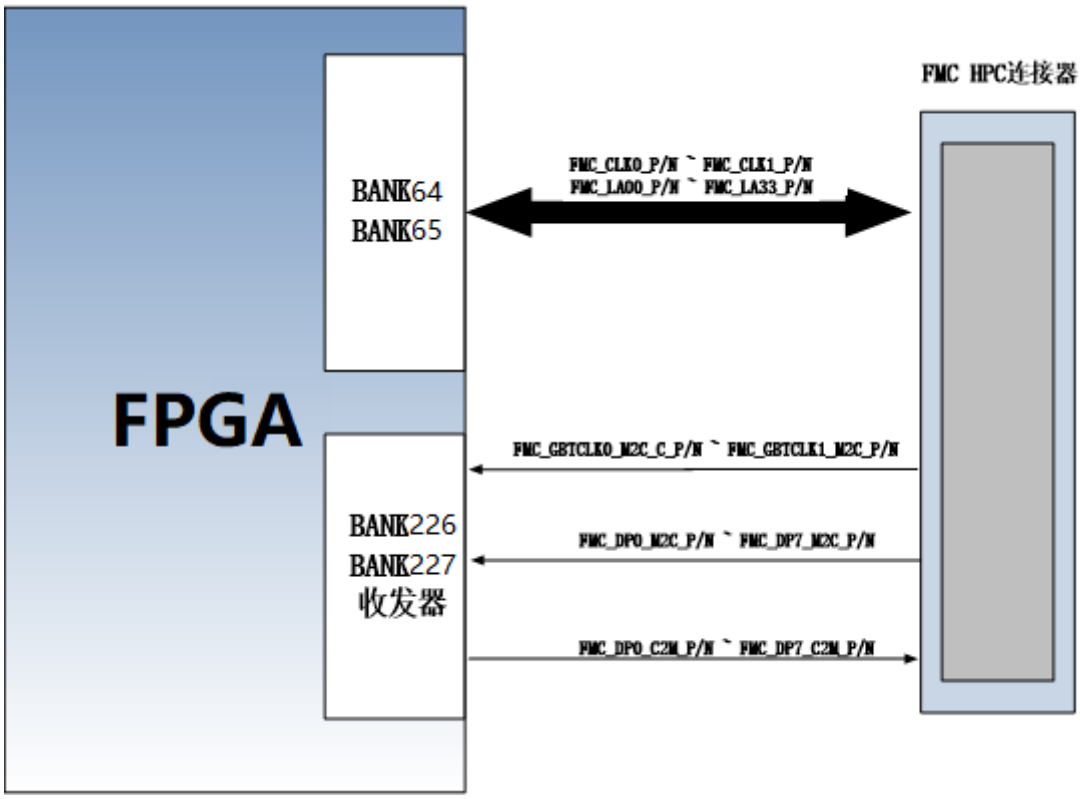


Figure 3-4-1 HPC FMC connection diagram

FMC HPC connector pins are assigned as follows:

Signal Name	FPGA Pin Name	FPGA Pin No.	备注
FMC_CLK0_N	B65_L12_N	W24	FMC 第 0 路输入参考时钟 N
FMC_CLK0_P	B65_L12_P	V24	FMC 0th input Reference clock P
FMC_CLK1_N	B64_L12_N	AC21	FMC 1st input Reference clock N
FMC_CLK1_P	B64_L12_P	AB21	FMC 1st input Reference clock P
FMC_LA00_CC_N	B65_L14_N	U25	FMC LA 0th Data（Clock）N
FMC_LA00_CC_P	B65_L14_P	T25	FMC LA 0th Data（Clock）P
FMC_LA01_CC_N	B65_L13_N	U24	FMC LA 1st Data（Clock）N
FMC_LA01_CC_P	B65_L13_P	T24	FMC LA 1st Data（Clock）P
FMC_LA02_N	B65_L17_N	P26	FMC LA 2nd Data N
FMC_LA02_P	B65_L17_P	P25	FMC LA 2nd Data P
FMC_LA03_N	B65_L5_N	T23	FMC LA 3rd Data N
FMC_LA03_P	B65_L5_P	T22	FMC LA 3rd Data P
FMC_LA04_N	B65_L16_N	V26	FMC LA 4th Data N
FMC_LA04_P	B65_L16_P	U26	FMC LA 4th Data P

FMC_LA05_N	B64_L24_N	AA18	FMC LA 5th Data N
FMC_LA05_P	B64_L24_P	Y18	FMC LA 5th Data P
FMC_LA06_N	B65_L10_N	W26	FMC LA 6th Data P
FMC_LA06_P	B65_L10_P	W25	FMC LA 6th Data P
FMC_LA07_N	B65_L9_N	AA25	FMC LA 7th Data N
FMC_LA07_P	B65_L9_P	AA24	FMC LA 7th Data P
FMC_LA08_N	B65_L11_N	W23	FMC LA 8th Data N
FMC_LA08_P	B65_L11_P	V23	FMC LA 8th Data P
FMC_LA09_N	B65_L8_N	Y26	FMC LA 9th Data N
FMC_LA09_P	B65_L8_P	Y25	FMC LA 9th Data P
FMC_LA10_N	B65_L15_N	P24	FMC LA 10th Data N
FMC_LA10_P	B65_L15_P	N24	FMC LA 10th Data P
FMC_LA11_N	B64_L10_N	AB22	FMC LA 11th Data N
FMC_LA11_P	B64_L10_P	AA22	FMC LA 11th Data P
FMC_LA12_N	B65_L7_N	Y23	FMC LA 12th Data N
FMC_LA12_P	B65_L7_P	Y22	FMC LA 12th Data P
FMC_LA13_N	B64_L9_N	AC23	FMC LA 13th Data N
FMC_LA13_P	B64_L9_P	AC22	FMC LA 13th Data P
FMC_LA14_N	B64_L7_N	AF22	FMC LA 14th Data N
FMC_LA14_P	B64_L7_P	AE22	FMC LA 14th Data P
FMC_LA15_N	B64_L11_N	AE21	FMC LA 15th Data N
FMC_LA15_P	B64_L11_P	AD21	FMC LA 15th Data P
FMC_LA16_N	B64_L8_N	AE23	FMC LA 16th Data N
FMC_LA16_P	B64_L8_P	AD23	FMC LA 16th Data P
FMC_LA17_CC_N	B64_L14_N	AD19	FMC LA 17th Data（Clock）N
FMC_LA17_CC_P	B64_L14_P	AC19	FMC LA 17th Data（Clock）P
FMC_LA18_CC_N	B64_L13_N	AE20	FMC LA 18th Data（Clock）N
FMC_LA18_CC_P	B64_L13_P	AD20	FMC LA 18th Data（Clock）P
FMC_LA19_N	B64_L18_N	AE16	FMC LA 19th Data N
FMC_LA19_P	B64_L18_P	AD16	FMC LA 19th Data P
FMC_LA20_N	B64_L16_N	AD18	FMC LA 20th Data N
FMC_LA20_P	B64_L16_P	AC18	FMC LA 20th Data P
FMC_LA21_N	B64_L20_N	AB19	FMC LA 21st Data N
FMC_LA21_P	B64_L20_P	AA19	FMC LA 21st Data P
FMC_LA22_N	B64_L21_N	AB20	FMC LA 22nd Data N
FMC_LA22_P	B64_L21_P	AA20	FMC LA 22nd Data P

FMC_LA23_N	B64_L23_N	AA17	FMC LA 23rd Data N
FMC_LA23_P	B64_L23_P	Y17	FMC LA 23rd Data P
FMC_LA24_N	B64_L15_N	AF19	FMC LA 24th Data N
FMC_LA24_P	B64_L15_P	AF18	FMC LA 24th Data P
FMC_LA25_N	B64_L6_N	AC24	FMC LA 25th Data N
FMC_LA25_P	B64_L6_P	AB24	FMC LA 25th Data P
FMC_LA26_N	B64_L19_N	Y21	FMC LA 26th Data N
FMC_LA26_P	B64_L19_P	Y20	FMC LA 26th Data P
FMC_LA27_N	B64_L22_N	AC17	FMC LA 27th Data N
FMC_LA27_P	B64_L22_P	AB17	FMC LA 27th Data P
FMC_LA28_N	B64_L17_N	AF17	FMC LA 28th Data N
FMC_LA28_P	B64_L17_P	AE17	FMC LA 28th Data P
FMC_LA29_N	B64_L1_N	AE26	FMC LA 29th Data N
FMC_LA29_P	B64_L1_P	AE25	FMC LA 29th Data P
FMC_LA30_N	B64_L5_N	AD25	FMC LA 30th Data N
FMC_LA30_P	B64_L5_P	AD24	FMC LA 30th Data P
FMC_LA31_N	B64_L2_N	AB26	FMC LA 31st Data N
FMC_LA31_P	B64_L2_P	AB25	FMC LA 31st Data P
FMC_LA32_N	B64_L4_N	AD26	FMC LA 32nd Data N
FMC_LA32_P	B64_L4_P	AC26	FMC LA 32nd Data P
FMC_LA33_N	B64_L3_N	AF25	FMC LA 33rd Data N
FMC_LA33_P	B64_L3_P	AF24	FMC LA 33rd Data P
FMC_SCL	B84_L6_P	AB15	FMC I2C Bus Clock
FMC_SDA	B84_L6_N	AB16	FMC I2C Bus Data
FMC_HPC_GBTCLK0_M2C_C_N	MGT226_CLK1_N	M6	Transceiver Reference clock 0 input P
FMC_HPC_GBTCLK0_M2C_C_P	MGT226_CLK1_P	M7	Transceiver Reference clock 0 input N
FMC_HPC_GBTCLK1_M2C_C_N	MGT227_CLK1_N	H6	Transceiver Reference clock 1 input P
FMC_HPC_GBTCLK1_M2C_C_P	MGT227_CLK1_P	H7	Transceiver Reference clock 1 input N
FMC_DP0_M2C_P	MGT226_RX0_P	M2	Transceiver data 0 input P
FMC_DP0_M2C_N	MGT226_RX0_N	M1	Transceiver data 0 input N
FMC_DP1_M2C_P	MGT226_RX1_P	K2	Transceiver data 1 input P
FMC_DP1_M2C_N	MGT226_RX1_N	K1	Transceiver data 1 input N
FMC_DP2_M2C_P	MGT226_RX2_P	H2	Transceiver data 2 input P
FMC_DP2_M2C_N	MGT226_RX2_N	H1	Transceiver data 2 input N
FMC_DP3_M2C_P	MGT226_RX3_P	F2	Transceiver data 3 input P
FMC_DP3_M2C_N	MGT226_RX3_N	F1	Transceiver data 3 input N

FMC_DP4_M2C_P	MGT227_RX0_P	D2	Transceiver data 4 input P
FMC_DP4_M2C_N	MGT227_RX0_N	D1	Transceiver data 4 input N
FMC_DP5_M2C_P	MGT227_RX1_P	C4	Transceiver data 5 input P
FMC_DP5_M2C_N	MGT227_RX1_N	C3	Transceiver data 5 input N
FMC_DP6_M2C_P	MGT227_RX3_P	A4	Transceiver data 6 input P
FMC_DP6_M2C_N	MGT227_RX3_N	A3	Transceiver data 6 input N
FMC_DP7_M2C_P	MGT227_RX2_P	B2	Transceiver data 7 input P
FMC_DP7_M2C_N	MGT227_RX2_N	B1	Transceiver data 7 input N
FMC_DP0_C2M_P	MGT226_TX0_P	N5	Transceiver data 0 output P
FMC_DP0_C2M_N	MGT226_TX0_N	N4	Transceiver data 0 output N
FMC_DP1_C2M_P	MGT226_TX1_P	L5	Transceiver data 1 output P
FMC_DP1_C2M_N	MGT226_TX1_N	L4	Transceiver data 1 output N
FMC_DP2_C2M_P	MGT226_TX2_P	J5	Transceiver data 2 output P
FMC_DP2_C2M_N	MGT226_TX2_N	J4	Transceiver data 2 output N
FMC_DP3_C2M_P	MGT226_TX3_P	G5	Transceiver data 3 output P
FMC_DP3_C2M_N	MGT226_TX3_N	G4	Transceiver data 3 output N
FMC_DP4_C2M_P	MGT227_TX0_P	F7	Transceiver data 4 output P
FMC_DP4_C2M_N	MGT227_TX0_N	F6	Transceiver data 4 output N
FMC_DP5_C2M_P	MGT227_TX1_P	E5	Transceiver data 5 output P
FMC_DP5_C2M_N	MGT227_TX1_N	E4	Transceiver data 5 output N
FMC_DP6_C2M_P	MGT227_TX3_P	B7	Transceiver data 6 output P
FMC_DP6_C2M_N	MGT227_TX3_N	B6	Transceiver data 6 output N
FMC_DP7_C2M_P	MGT227_TX2_P	D7	Transceiver data 7 output P
FMC_DP7_C2M_N	MGT227_TX2_N	D6	Transceiver data 7 output N

Part 3.5: MIPI Interface

There is a MIPI lanex4 camera input interface on the AXKU5 expansion board, which is connected to BANK66 and BANK84 of PGA. The connection design diagram is shown in Figure 3-5-1 below:

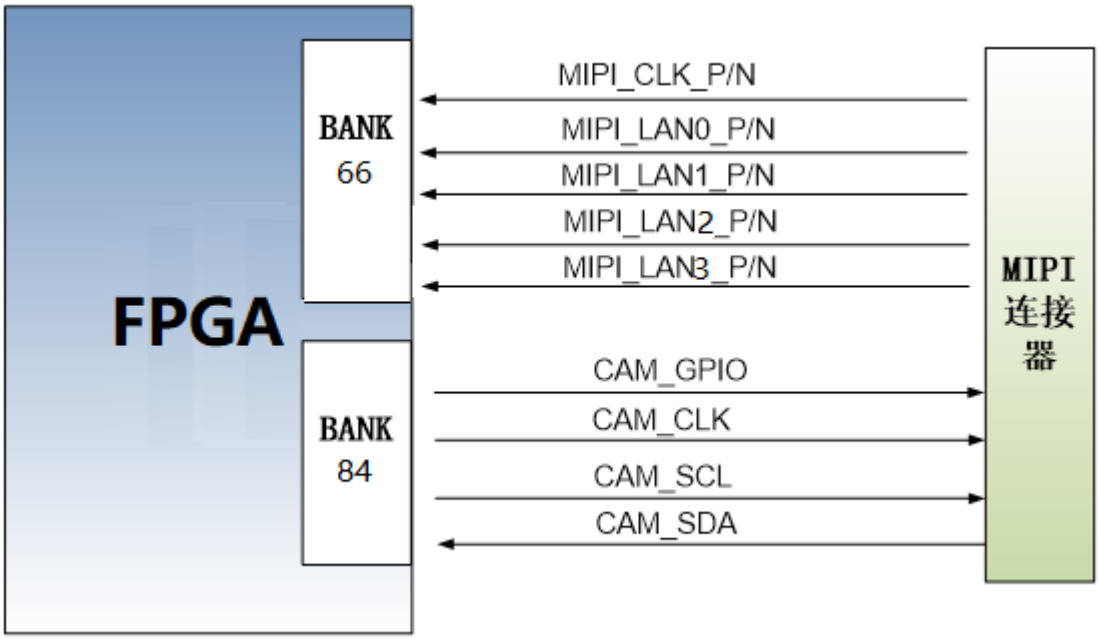


Figure 3-5-1 Schematic diagram of MIPI interface design

MIPI interface Pin assignment

Signal Name	ZYNQ pin name	ZYNQ pin No.	Description
MIPI_CLK_P	B66_L1_P	L18	MIPI Input clock P
MIPI_CLK_N	B66_L1_N	K18	MIPI Input clock N
MIPI_LAN0_P	B66_L5_P	K21	MIPI Input data LANE0 P
MIPI_LAN0_N	B66_L5_N	J21	MIPI Input data LANE0 N
MIPI_LAN1_P	B66_L2_P	M20	MIPI Input data LANE1 P
MIPI_LAN1_N	B66_L2_N	M21	MIPI Input data LANE1 N
MIPI_LAN2_P	B66_L3_P	J19	MIPI Input data LANE2 P
MIPI_LAN2_N	B66_L3_N	J20	MIPI Input data LANE2 N
MIPI_LAN3_P	B66_L4_P	M19	MIPI Input data LANE3 P
MIPI_LAN3_N	B66_L4_N	L19	MIPI Input data LANE3 N
MIPI_CLK	B84_L10_P	W14	Camera clock input
MIPI_GPIO	B84_L10_N	W15	Camera GPIO Control
MIPI_I2C_SCL	B84_L8_N	AB14	Camera I2C Clock
MIPI_I2C_SDA	B84_L8_P	AA14	Camera I2C Data

Part 3.6: USB to Serial Port

The AXKU5 expansion board is equipped with a Uart to USB interface for system debugging. The conversion chip adopts the USB-UAR chip of Silicon Labs CP2102GM, and the USB interface adopts the MINI USB interface, which can be connected to the

USB port of the upper PC with a USB cable for separate power supply of the core board and serial data communication.

The schematic diagram of USB Uart circuit design is shown in the following figure:

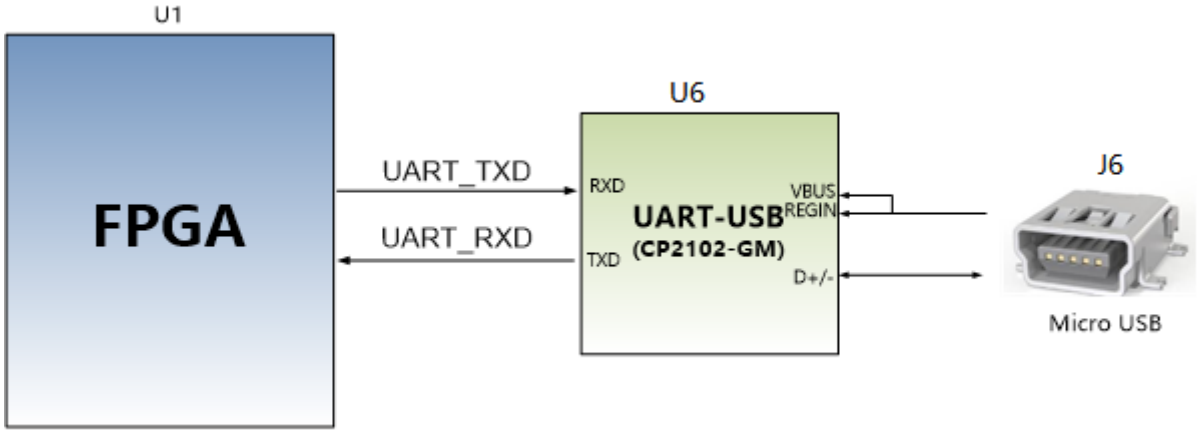


Figure 3-6-1 USB to serial port diagram

USB Serial Port FPGA Pin assignment:

Signal Name	FPGA pin name	Pin No.	Description
UART_RXD	B84_L3_N	AE15	Uart Data input
UART_TXD	B84_L3_P	AD15	Uart Data output

Part 3.7: SD Card Slot

The AXKU5 carrier board includes a Micro SD card interface in order to provide user's access to SD card memory for user data files. The SDIO signal is connected to the IO signal of the FPGA, supports SPI mode and SD mode, and uses a MicroSD card. The schematic diagram of the FPGA and SD card connectors is shown in Figure 3-7-1 below.

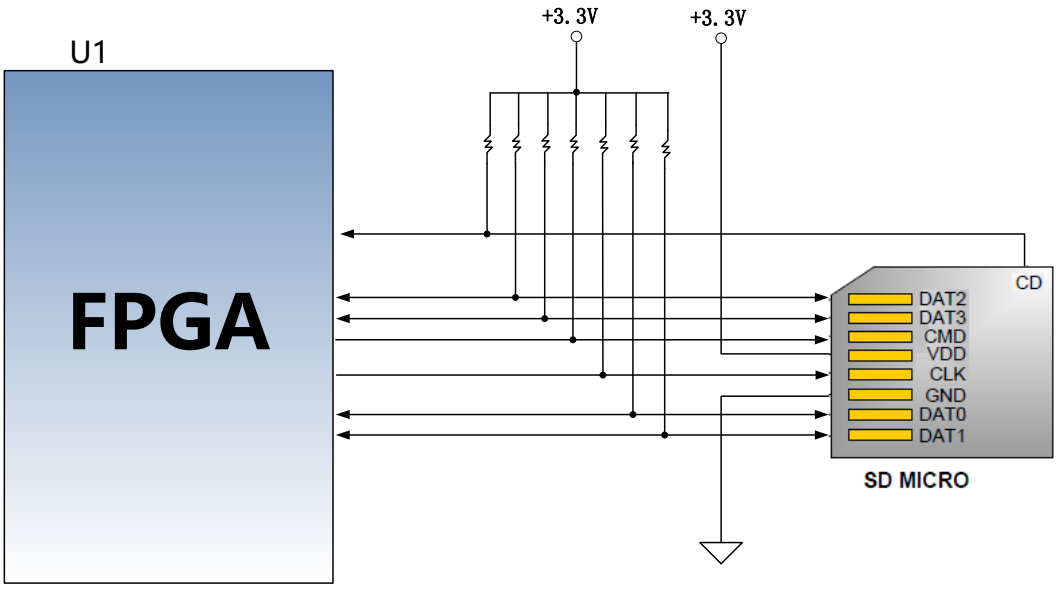


Figure 3-7-1 Schematic diagram of the SD card slot

SD Card Slot Pin Allocation

Signal Name	FPGA Pin Name	Pin No.	Description
SD_CD	B84_L4_N	AD14	SD Slice selection signal
SD_CLK	B84_L11_P	Y13	SD Clock signal
SD_CMD	B84_L11_N	AA13	SD Command signal
SD_D0	B84_L12_N	W13	SD Data 0
SD_D1	B84_L12_P	W12	SD Data 1
SD_D2	B84_L1_N	AF15	SD Data 2
SD_D3	B84_L1_P	AF14	SD Data 3

Part 3.8: 40 Pin Expansion port

The carrier board reserves a 40-pin expansion port J8 with 2.54mm standard pitch, which is used to connect each module of black gold or the external circuit designed by the user. The expansion port has 40 signals, including 1 5V power supply, 2 3.3V power supply, 3 ground channels, and 34 IO ports. The IO of the expansion port connects to the IO of the FPGA. The default value is 3.3V.

The pin assignment of the J8 expansion FPGA is as follows:

J8 Pin	Signal Name	Pin No.	J8 Pin	Signal Name	Pin No.
1	GND	-	2	+5V	-
3	IO1_1N	A10	4	IO1_1P	B10

5	IO1_2N	B11	6	IO1_2P	C11
7	IO1_3N	E10	8	IO1_3P	E11
9	IO1_4N	A9	10	IO1_4P	B9
11	IO1_5N	D10	12	IO1_5P	D11
13	IO1_6N	C9	14	IO1_6P	D9
15	IO1_7N	F9	16	IO1_7P	F10
17	IO1_8N	G9	18	IO1_8P	G10
19	IO1_9N	H9	20	IO1_9P	J9
21	IO1_10N	J10	22	IO1_10P	J11
23	IO1_11N	G11	24	IO1_11P	H11
25	IO1_12N	K9	26	IO1_12P	K10
27	IO1_13N	B12	28	IO1_13P	C12
29	IO1_14N	E12	30	IO1_14P	E13
31	IO1_15N	F12	32	IO1_15P	G12
33	IO1_16N	A12	34	IO1_16P	A13
35	IO1_17N	D13	36	IO1_17P	D14
37	GND	-	38	GND	-
39	+3.3V	-	40	+3.3V	-

Part 3.9: Keys and LED Lights

The carrier board of AXKU5 has 7 LED and 1 power indicator; 2 serial communication indicators, 4 user LED lights. When the development board is powered on, the power indicator will light up; The 4 LED lights are connected to the IO of the FPGA, and the user can control the on and off through the program. When the IO voltage of the connected user LED lamp is high, the user LED lamp will be on, and when the connected IO voltage is low, the user LED will be off. In addition, there are 4 user keys on the board, the default key signal is high, and the key level is low when the key is pressed. The hardware connection diagram of user LED lights and keys is shown in Figure 3-9-1:

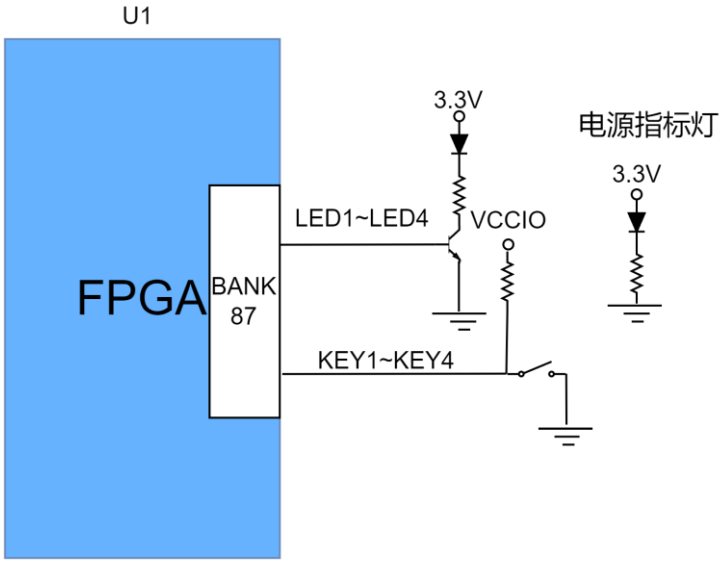


Figure 3-9-1 Schematic diagram of hardware connection of user LED lights and keys

User LED lights and pin allocation of keys

Signal Name	FPGA Pin Name	Pin No.	Description
KEY1	B87_L4_N	J14	User key 1
KEY2	B87_L4_P	J15	User key 2
KEY3	B87_L2_P	J13	User key 3
KEY4	B87_L2_N	H13	User key 4
LED1	B87_L1_P	J12	User LED1 Light
LED2	B87_L3_P	H14	User LED2 Light
LED3	B87_L6_N	F13	User LED3 Light
LED4	B87_L1_N	H12	User LED4 Light

Part 3.10: JTAG Debugging port.

A 10PIN JTAG interface is reserved on the AXKU5 backboard for downloading FPGA programs or curing programs to FLASH. In order to avoid the damage to the FPGA chip caused by live plugging, we add a protection diode to the JTAG signal to ensure that the voltage of the signal is in the range accepted by the FPGA.

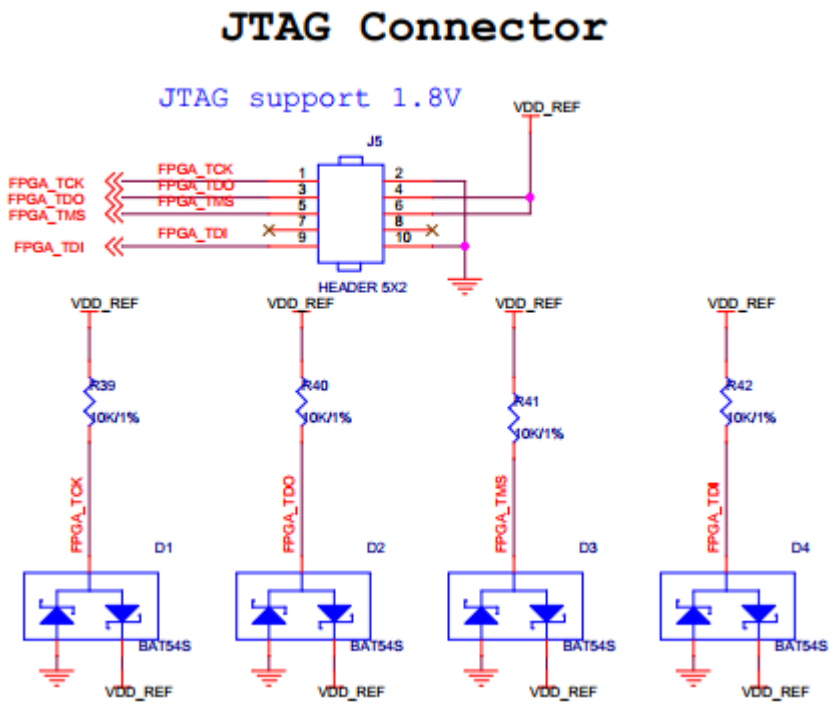


Figure 3-10-1 schematic diagram JTAG interface part

Part 3.11: Power Supply.

The input voltage power of the development board is 12V DC. You can supply power to the development board through the PCIE slot or external +12V power supply. Use the own power supply with the development board for external power supply. Do not use other power supplies to avoid damage to the development board. The external input power supply on the carrier board is protected by 1-way voltage chip, and the DC/DC power supply chips ETA8156, ETA1471 and SGM61163 are converted into +5V, +V_ADJ and +3.3V three-way power supplies respectively. At the same time, the +3.3V output provides the voltage required by the multiple LDO output JTAG FPGA BANK.

The power supply design diagram on the board is shown in Figure 3-11-1 below:

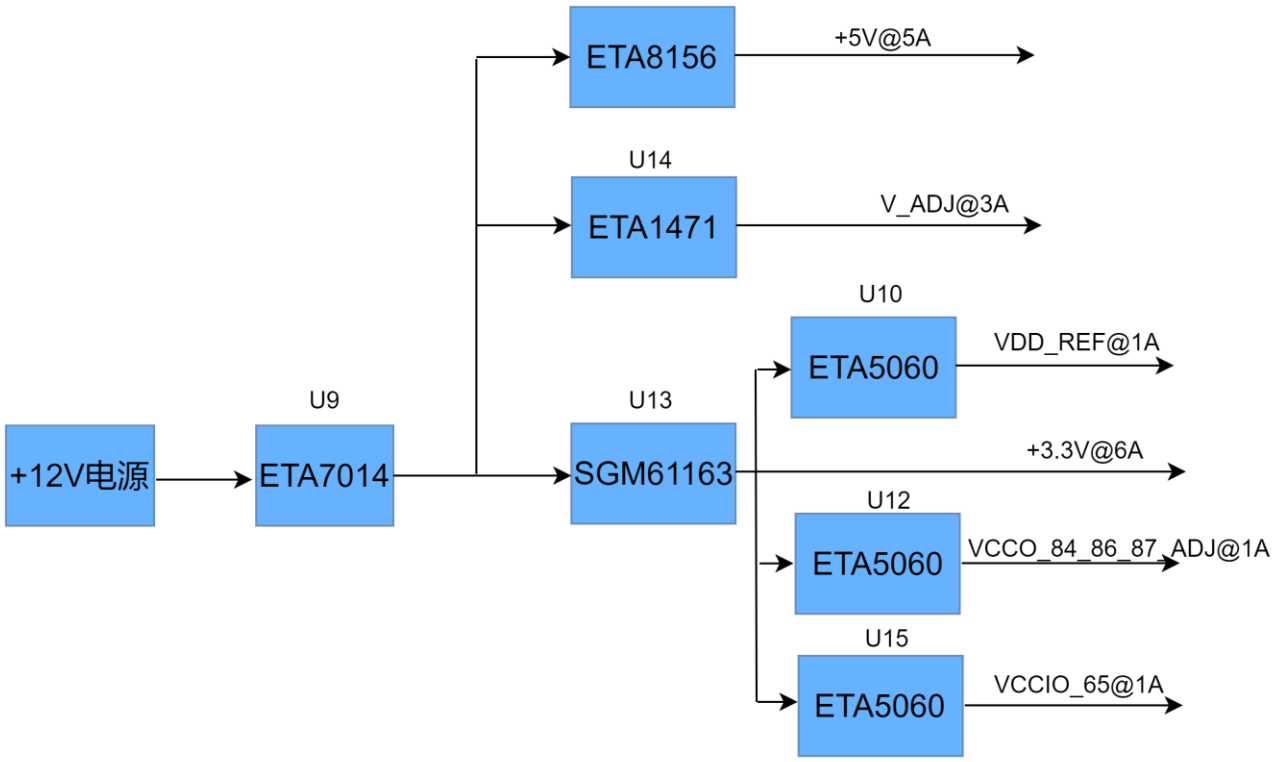


Figure 3-11-1 Schematic diagram of the power interface

The following table describes the power distribution functions:

Power supply	Function
+5.0V	Power supply for the expansion module
V_ADJ	FPGA BANK Voltage
+3.3V	Carrier board peripheral power supply
VDD_REF	JTAG power supply
VCCIO_65	FPGA BANK Voltage
VCCO_84_86_87_ADJ	FPGA BANK Voltage

Part 3.12: Structure Dimension drawing

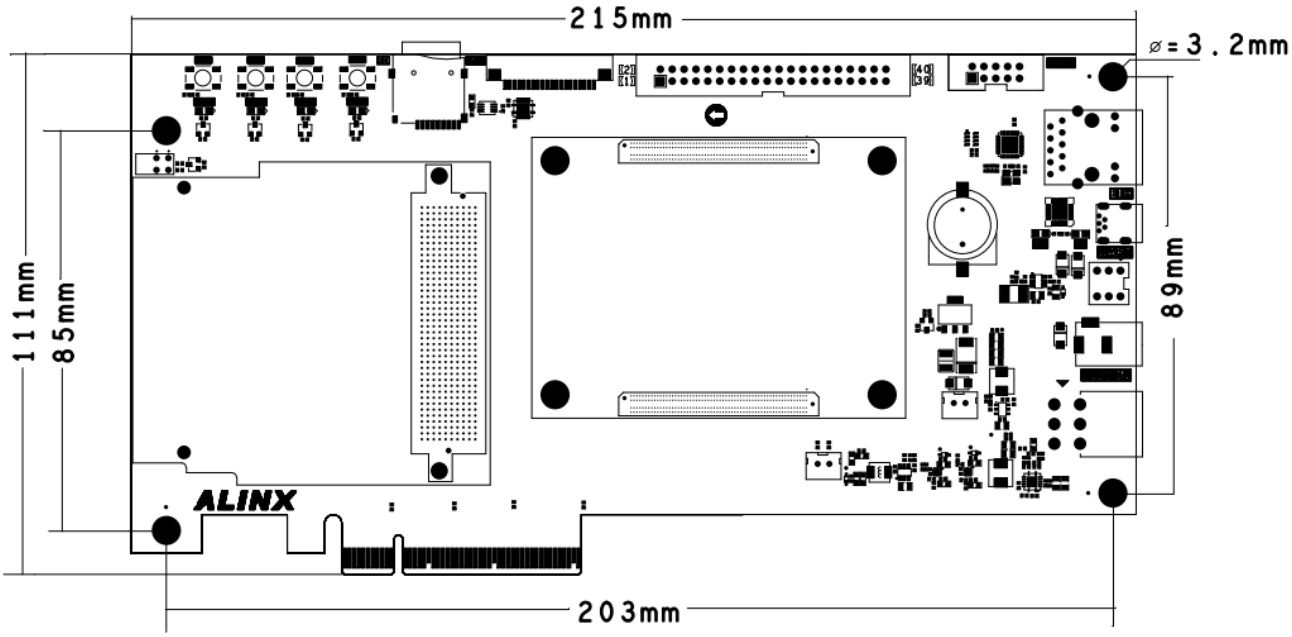


Figure 3-12-1 Top View