Xilinx FPGA

AXVU13F

Development Board

User Manual

ALINX

Document Revision Record:

Version	Time	Description
1.0	2024/6/5	Initial Release

Contents

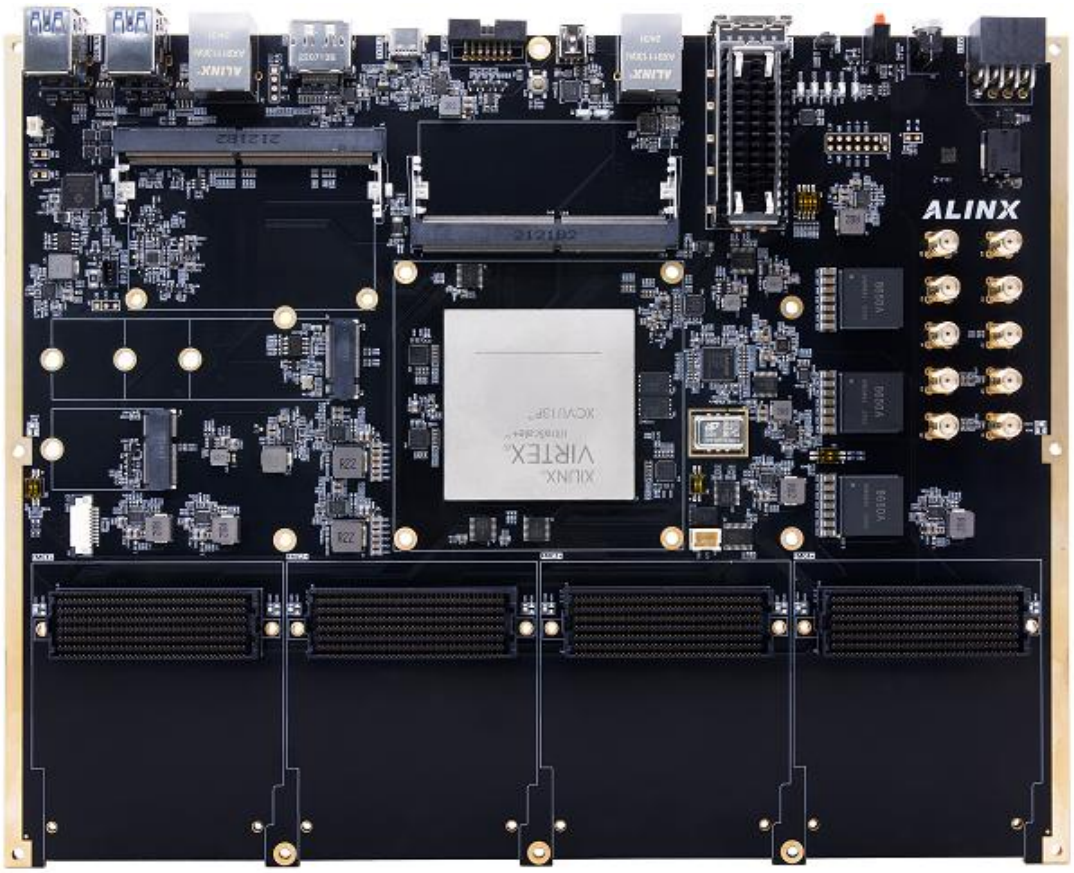
1 Overview

1.1 General

1.1.1 Introduction

The Alinx AXVU13F development platform is a high-performance system that integrates Xilinx FPGA Virtex UltraScale+ chip (XCVU13P-FHGB2104) with the Jetson Orin NX 8GB GPU module. It is engineered to meet a wide range of user requirements, including high-speed data exchange, data storage, video transmission and processing, deep learning, artificial intelligence, and industrial control.

The use of AXVU13F facilitates both the early-stage verification and later-stage application of high-speed data transfer and processing. AXVU13F is ideally suited for education, engineers, and other professionals engaged in FPGA and GPU development.



1.2 Features

- FPGA System:
  - SODIMM memory interface supporting up to 32GB
  - 1 x 2Gb QSPI FLASH chip
  - 4 x FMC+ interfaces
  - 1 x QSFP28 100G optical fiber interface
  - 6 x SMA interfaces
  - 1 x Gigabit Ethernet interface
  - 1 x UART interface
  - 6 x IO expansion interfaces
- NVIDIA ORIN
  - 1 x Gigabit Ethernet interface
  - 1 x USB3.0 Type-C interface
  - 4 x USB3.0 interfaces
  - 1 x M.2 SSD interface
  - 1 x M.2 WIFI/BT interface

2 Block Diagram

This section provides a functional introduction to the Virtex Ultrascale+ AXVU13F development platform.

The AXVU13F primarily integrates an FPGA system and an NVIDIA Orin module, interconnected via a **PCIe 2.0 x4** interface. The FPGA side utilizes the Xilinx Virtex Ultrascale+ series chip, model **XCVU13P-2FHGB2104I**. It supports a 72-bit SODIMM interface with a capacity of up to 32GB and is equipped with two 1Gb QSPI FLASH chips for static storage of FPGA configuration files or other user data. The NVIDIA Orin module side features multiple interfaces suitable for AI algorithms and high-performance computing applications.

The development platform provides a variety of interfaces, including 4 FMC+ interfaces, 1 QSFP28 100G optical fiber interface, 6 SMA interfaces, 2 Gigabit Ethernet interfaces, 1 UART interface, 6 IO expansion interfaces, 1 USB3.0 Type-C interface, 4 USB3.0 interfaces, 1 M.2 SSD interface, 1 M.2 WIFI/BT interface etc.

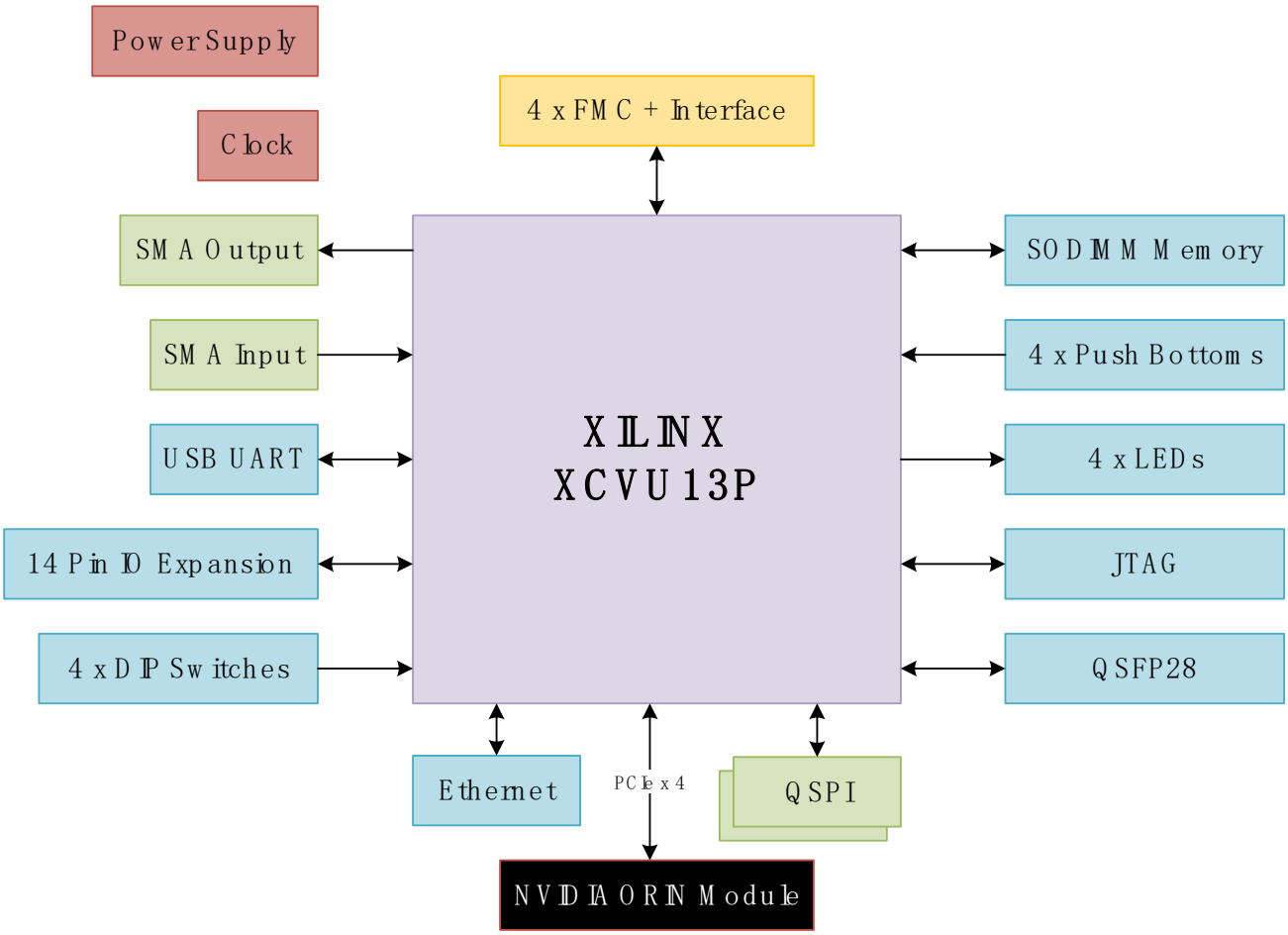


Figure 2: Schematic diagram of the development system

FPGA-Side Interfaces

- **FPGA Minimal System:**
  Comprises the XCVU13P-2FHGB2104I, a SODIMM interface, and QSPI FLASH. The board also features a high-precision, temperature-compensated crystal oscillator and a programmable clock source, providing reference clocks for the FPGA logic, SODIMM controller, and high-speed transceivers.

- **DDR4 Interface**
  Features a 260-pin DDR4 SODIMM slot, supporting a 72-bit data width and memory capacities of up to 32GB.

- **FPGA to NVIDIA ORIN PCIe Interconnect**
  Supports a PCI Express 3.0 x4 standard interface, with a per-lane communication rate of up to 8 GBaud.

- **4x FMC+ Interfaces:**
  - A total of 68 high-speed transceivers from the FPGA are routed to four FMC+ connectors. These ports comply with the FMC+ standard and are compatible with various FMC+ and FMC modules.
  - FMC1+: Provides 34 LA differential pairs, 2 clock pairs, 24 HA differential pairs, and 20 high-speed transceiver pairs.
  - FMC2+: Provides 34 LA differential pairs, 2 clock pairs, 24 HA differential pairs, and 16 high-speed transceiver pairs.
  - FMC3+: Provides 34 LA differential pairs, 2 clock pairs, and 16 high-speed transceiver pairs.
  - FMC4+: Provides 34 LA differential pairs, 2 clock pairs, and 16 high-speed transceiver pairs.
  - These interfaces meet high-speed signal transmission requirements, are compliant with the FMC+ standard, and are compatible with various FMC+ and FMC modules.

- **Gigabit Ethernet Interface:**
  Features one 10/100/1000 Mbps Ethernet RJ45 port for data exchange with a computer or other network devices.

- **QSFP28 100G Optical Interface:**
  Provides one QSFP28 port supporting an aggregate data rate of 100 Gbps (4 lanes operating at 25 Gbps each).

- **SMA Input/Output Interface:**
  Includes two SMA differential pairs (input/output) connected to the FPGA's HPIO pins, suitable for validating customer-provided differential signals.

- **4-Position DIP Switch:**
  An onboard 4-position DIP switch is available for simple user input or configuration settings.

- **USB-to-UART Interface:**
  Features one USB-to-UART bridge using a Silicon Labs **CP2102GM** chip to facilitate user debugging and communication with a host computer. The physical connector is a Mini-USB port.

- **Expansion Header:**
  An onboard 14-pin expansion header with a 2.54mm pitch provides access to 6 of the FPGA's HPIO pins for customer testing purposes.

- **JTAG Debug Port**
  One 14-pin, 2.00mm pitch standard JTAG header is provided for downloading and debugging the FPGA program. Users can debug and program the FPGA system using a Xilinx downloader/cable.

- **LED Indicators**
  The board includes 8 LEDs in total: one DONE configuration indicator, one power indicator, four user-configurable indicators, and two serial port (UART) indicators.

- **JTAG Debug Port**
  One 14-pin, 2.00mm pitch standard JTAG header is provided for downloading and debugging the FPGA program. Users can debug and program the FPGA system using a Xilinx downloader/cable.

- **LED Indicators**
  The board includes 8 LEDs in total: one DONE configuration indicator, one power indicator, four user-configurable indicators, and two serial port (UART) indicators.

- **Push-button**
  One user-configurable push-button is available.

NVIDIA ORIN Module Interfaces

- **DP Output Interface**
  One standard DisplayPort output is provided for video and image display, supporting resolutions up to 4K@30Hz or 1080P@60Hz. It is connected to the NVIDIA ORIN module via PCIe.

- **USB 3.0 Interface**
  The board features four USB 3.0 HOST ports (Type-A) for connecting external peripherals like a mouse, keyboard, or USB drive. Additionally, there is one USB 3.0 Type-C port connected to the NVIDIA ORIN module, which supports HOST, SLAVE, and OTG modes with data transfer speeds up to 5.0 Gb/s.

- **M.2 Interface**
  - **One M.2 Key-M slot:** Used for connecting an NVMe SSD. It is connected to the NVIDIA ORIN module via a PCIe x2 interface and supports communication speeds up to 5 Gbps.
  - **One M.2 Key-E slot:** Used for connecting a Wi-Fi/Bluetooth module. It is connected to the NVIDIA ORIN module via a PCIe x1 interface and supports communication speeds up to 5 Gbps.

- **Gigabit Ethernet Interface**
  One 10/100/1000 Mbps Ethernet RJ45 port is available for data exchange with a computer or other network devices.

3 FPGA Chip

3.1 Naming Convention

The FPGA model used in this product is XCVU13P-2FHGB2104I, which belongs to the Xilinx Virtex Ultrascale+ series. It has a speed grade of 2 and an industrial temperature grade. This model comes in the FHGB2104 package with 2104 pins.

The naming convention for Xilinx Virtex Ultrascale+ FPGAs is as Figure 3.

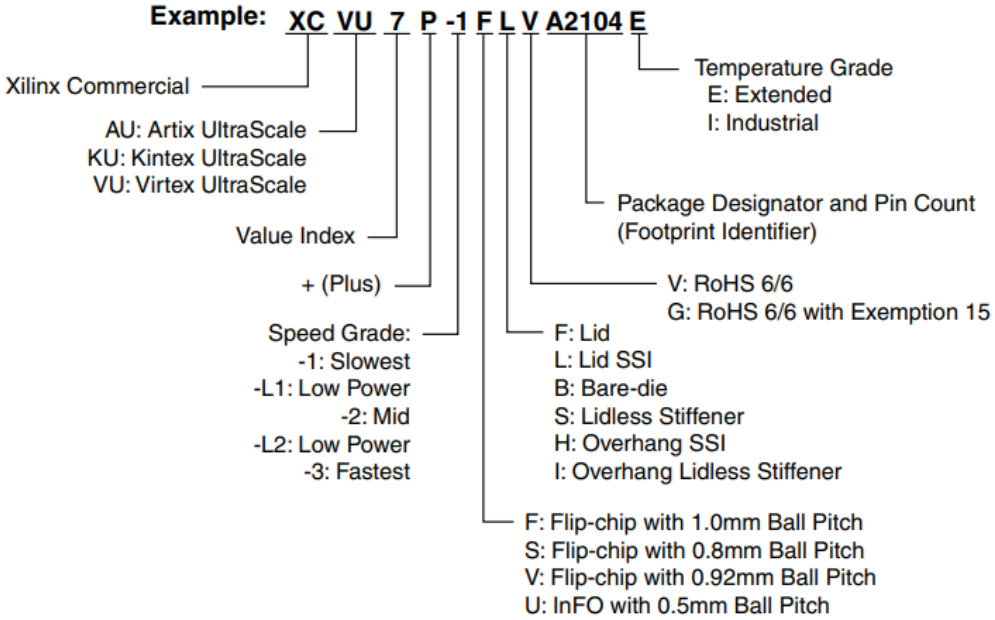


Figure 3: Naming convention for Xilinx Virtex Ultrascale+ FPGAs

3.2 Main Parameters of the FPGA Chip

FPGA Resource Specifications	Parameters
Logic Cells	3780K
Registers (FF)	3456K
LUTs	1728K
Total Block RAM	94.5Mb
Ultra RAM	360Mb
DSP Slices	12,288
CMTs	16
GTY/Gb/s	76/28.21Gb
PCIe Gen3 x16	4
Speed Grade	-2
Temperature Grade	Industrial Level

Table 1: Main parameters

4 DDR4 DRAM

The AXVU13F development board is equipped with a DDR4 SODIMM memory slot that supports various module capacities, including 8GB, 16GB, and 32GB. It is recommended to use memory models that have been previously tested by our team. The interface supports a data bus width of up to 72 bits.

The maximum operating data rate on the FPGA side is 2666 Mbps. The SODIMM interface is connected to the memory interfaces of BANK 61, 62, and 63.
The specific configuration of the DDR4 SDRAM is shown in Table 2 below.

Position Number	Chip Type	Capacity
J3	SODIMM	(8/16/32)GB

Table 2: DDR4 SDRAM configuration

4.1 Schematic Diagram

DDR4 hardware design requires stringent consideration of signal integrity. In circuit design and PCB design phases, we have thoroughly addressed impedance matching/termination resistance, trace impedance control, and equal length trace control to ensure stable and high-speed operation of DDR4.

The hardware connection method of the DDR4 DRAM at the FPGA end is shown in Figure 4:

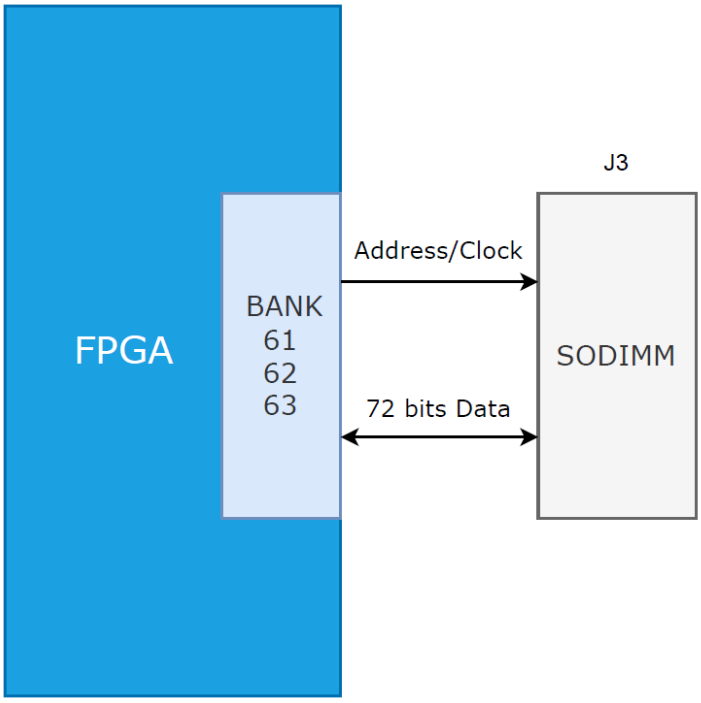


Figure 4: DDR4 DRAM schematic diagram

Figure 5 shows the physical object of the development board's SODIMM interface.

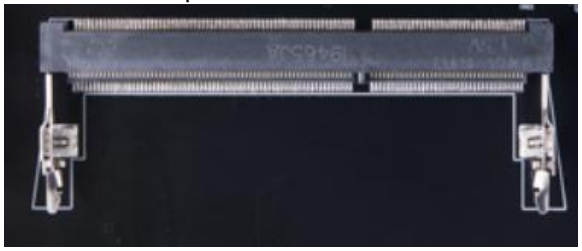


Figure 5: SODIMM interface

4.2 SODIMM Interface FPGA PIN Assignment

Signal Name	PIN Number
PL_DDR4_DQ0	AW34
PL_DDR4_DQ1	AW33
PL_DDR4_DQ2	AY36
PL_DDR4_DQ3	BA33
PL_DDR4_DQ4	AV33
PL_DDR4_DQ5	AY33
PL_DDR4_DQ6	AY35
PL_DDR4_DQ7	AV34
PL_DDR4_DQ8	AL32
PL_DDR4_DQ9	AM34
PL_DDR4_DQ10	AP33
PL_DDR4_DQ11	AM32
PL_DDR4_DQ12	AL34
PL_DDR4_DQ13	AN34
PL_DDR4_DQ14	AP34
PL_DDR4_DQ15	AR33
PL_DDR4_DQ16	BD39
PL_DDR4_DQ17	BE38
PL_DDR4_DQ18	BB38
PL_DDR4_DQ19	BF38
PL_DDR4_DQ20	BF37
PL_DDR4_DQ21	BC39
PL_DDR4_DQ22	BC38
PL_DDR4_DQ23	BE37
PL_DDR4_DQ24	BE36
PL_DDR4_DQ25	BD36
PL_DDR4_DQ26	BB35
PL_DDR4_DQ27	BE35
PL_DDR4_DQ28	BA35
PL_DDR4_DQ29	BB36
PL_DDR4_DQ30	BC36
PL_DDR4_DQ31	BD35
PL_DDR4_DQ32	BB31
PL_DDR4_DQ33	BA30
PL_DDR4_DQ34	AY30
PL_DDR4_DQ35	BA29
PL_DDR4_DQ36	AY32

PL_DDR4_DQ37	BB30
PL_DDR4_DQ38	AY31
PL_DDR4_DQ39	BB29
PL_DDR4_DQ40	BD29
PL_DDR4_DQ41	BE32
PL_DDR4_DQ42	BD33
PL_DDR4_DQ43	BE30
PL_DDR4_DQ44	BE31
PL_DDR4_DQ45	BE33
PL_DDR4_DQ46	BC29
PL_DDR4_DQ47	BF30
PL_DDR4_DQ48	AP30
PL_DDR4_DQ49	AP29
PL_DDR4_DQ50	AL30
PL_DDR4_DQ51	AM31
PL_DDR4_DQ52	AN31
PL_DDR4_DQ53	AR30
PL_DDR4_DQ54	AN29
PL_DDR4_DQ55	AL29
PL_DDR4_DQ56	AU32
PL_DDR4_DQ57	AW31
PL_DDR4_DQ58	AU30
PL_DDR4_DQ59	AT30
PL_DDR4_DQ60	AV32
PL_DDR4_DQ61	AV31
PL_DDR4_DQ62	AU31
PL_DDR4_DQ63	AT29
PL_DDR4_DQ64	Y33
PL_DDR4_DQ65	AB34
PL_DDR4_DQ66	Y32
PL_DDR4_DQ67	Y30
PL_DDR4_DQ68	W34
PL_DDR4_DQ69	W33
PL_DDR4_DQ70	AA34
PL_DDR4_DQ71	W30
C1_DDR4_CLKREF_N	AF33
C1_DDR4_CLKREF_P	AF32
PL_DDR4_A0	AC33
PL_DDR4_A1	AG29
PL_DDR4_A2	AJ29

PL_DDR4_A3	AG32
PL_DDR4_A4	AK28
PL_DDR4_A5	AJ30
PL_DDR4_A6	AG31
PL_DDR4_A7	AH31
PL_DDR4_A8	AG30
PL_DDR4_A9	AH32
PL_DDR4_A10	AJ27
PL_DDR4_A11	AJ31
PL_DDR4_A12	AF34
PL_DDR4_A13	AF30
PL_DDR4_ACT_B	AK31
PL_DDR4_ALERT_B	AK32
PL_DDR4_BA0	AH28
PL_DDR4_BA1	AC32
PL_DDR4_BG0	AH34
PL_DDR4_BG1	AH33
PL_DDR4_CAS_B	AH29
PL_DDR4_CKE0	AJ33
PL_DDR4_CKE1	AG34
PL_DDR4_CLK0_N	AE32
PL_DDR4_CLK0_P	AE31
PL_DDR4_CLK1_N	AE33
PL_DDR4_CLK1_P	AD33
PL_DDR4_CS0_B	AC31
PL_DDR4_CS1_B	AD31
PL_DDR4_DM0	BA34
PL_DDR4_DM1	AT33
PL_DDR4_DM2	BF39
PL_DDR4_DM3	BC34
PL_DDR4_DM4	BC31
PL_DDR4_DM5	BF32
PL_DDR4_DM6	AP31
PL_DDR4_DM7	AW29
PL_DDR4_DM8	AA32
PL_DDR4_DQS0_N	AW36
PL_DDR4_DQS0_P	AW35
PL_DDR4_DQS1_N	AN33
PL_DDR4_DQS1_P	AN32
PL_DDR4_DQS2_N	BE40

PL_DDR4_DQS2_P	BD40
PL_DDR4_DQS3_N	BC37
PL_DDR4_DQS3_P	BB37
PL_DDR4_DQS4_N	BB32
PL_DDR4_DQS4_P	BA32
PL_DDR4_DQS5_N	BD31
PL_DDR4_DQS5_P	BD30
PL_DDR4_DQS6_N	AM30
PL_DDR4_DQS6_P	AM29
PL_DDR4_DQS7_N	AV29
PL_DDR4_DQS7_P	AU29
PL_DDR4_DQS8_N	Y31
PL_DDR4_DQS8_P	W31
PL_DDR4_ODT0	AB32
PL_DDR4_ODT1	AD30
PL_DDR4_PARITY	AK27
PL_DDR4_RAS_B	AJ28
PL_DDR4_RST	AJ34
PL_DDR4_SCL_LS	AT14
PL_DDR4_SDA_LS	AT13
PL_DDR4_WE_B	AE30

Table 3: SODIMM Interface FPGA Pin Assignment

5 QSPI Flash

5.1 Type and Parameter

The module is equipped with 2 pieces of 1GBit Quad-SPI FLASH chips, model MT25QU01GBBB1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used to store FPGA configuration Bin files as well as other user data files.

The specific model and related parameters of the QSPI FLASH are listed in Table 2.

Position Number	Chip Type	Capacity	Manufacturers
U10; U11	MT25QU01GBBB1EW9	1Gbit	Micron

Table 4: QSPI Flash type and parameter.

5.2 Schematic Diagram

The QSPI FLASH is connected to dedicated pins on the FPGA chip. The clock pin is connected to CCLK0 of the dedicated BANK0, while the data pins are connected to BANK0 and BANK65 respectively.

Figure 6 illustrates the connection diagram between the QSPI Flash and the FPGA chip.

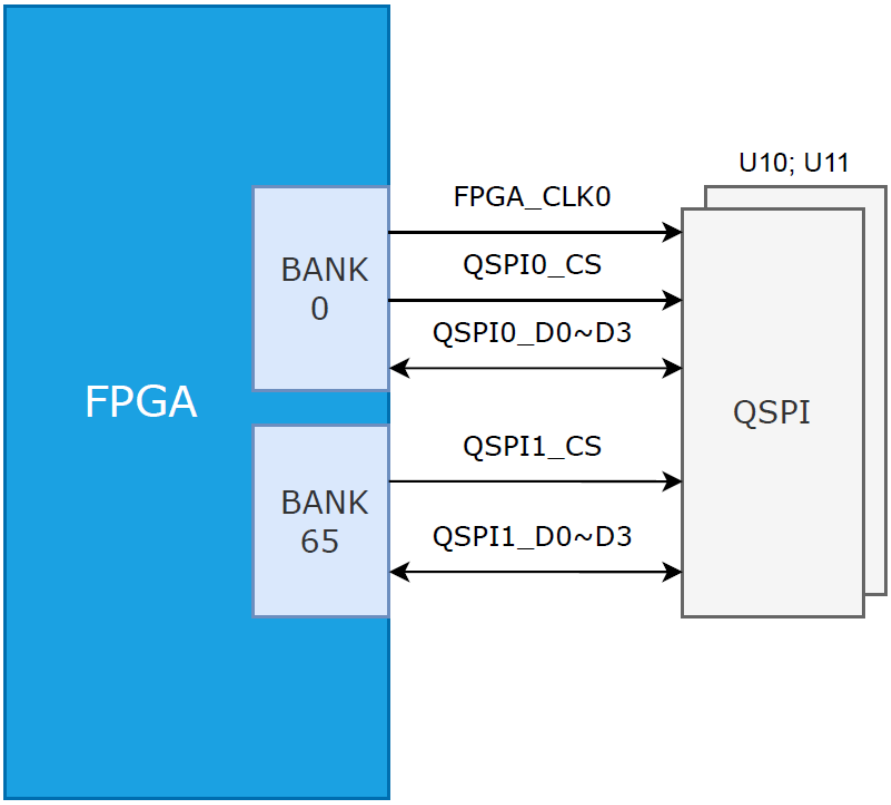


Figure 6: QSPI Flash schematic diagram

5.3 Configure Chip PIN Assignment

Signal Name	PIN Number
QSPI_CLK	AG13
QSPI0_CS	AG12
QSPI0_DQ0	AK12
QSPI0_DQ1	AJ12
QSPI0_DQ2	AL12
QSPI0_DQ3	AH12
QSPI1_CS	BF27
QSPI1_DQ0	AM26
QSPI1_DQ1	AN26
QSPI1_DQ2	AL25
QSPI1_DQ3	AM25

Table 3: Configure chip PIN assignment

6 Clock Configuration

6.1 FPGA System Clock Source

The board is equipped with two 200MHz differential crystal oscillators, which can provide reference clocks for the SODIMM controller and FPGA logic. The oscillator outputs are connected to the global clocks of FPGA BANK63 and BANK69, which can be used to drive the DDR4 controller and user logic circuits within the FPGA.

The schematic of this clock source is shown in Figure 7.

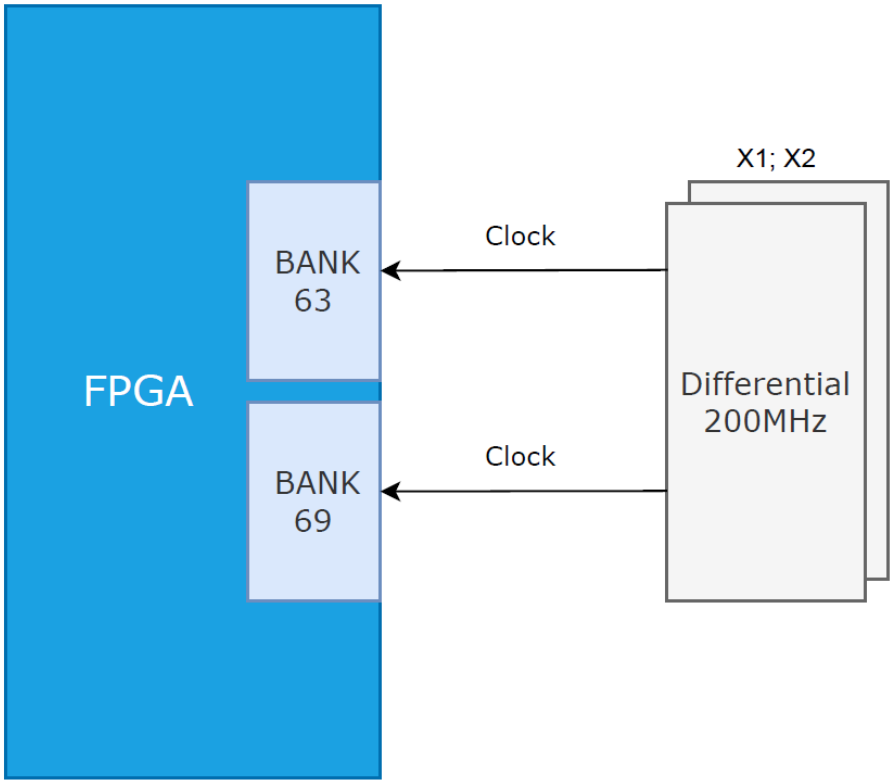


Figure 7: System clock source

6.2 Clock PIN Assignment

Signal Name	PIN Number
BADJ_CLK1_N	AW18
BADJ_CLK1_P	AV18
C1_DDR4_CLKREF_N	AF33
C1_DDR4_CLKREF_P	AF32

Table 4: Clock PIN Assignment

High-Speed Transceiver GTY Clock

The board is equipped with a high-precision, low-jitter, temperature-stabilized programmable multi-output clock source, which has 14 clock channels. This clock source can provide reference clocks for each channel of the high-speed transceiver GTY, meeting the clock requirements of the transceivers.

7 PCIe Interface

7.1 Design Diagram

On the AXVU13F board, there is a communication interface with the Jetson Orin NX 8GB GPU module, which supports the PCIe Gen3.0 protocol and uses a PCIe x4 lane interconnect model for data communication.

The GPU module's PCIe interface transmit and receive signals are directly connected to the FPGA BANK224 transceivers. The 4 lanes of TX signals and RX signals are all connected to the FPGA's transceivers as differential signals. The single-channel communication rate can reach up to 8G Baud bandwidth.

The design schematic of the development board's PCIe interface is shown in Figure 8, where the TX transmit signals are connected using AC coupling mode.

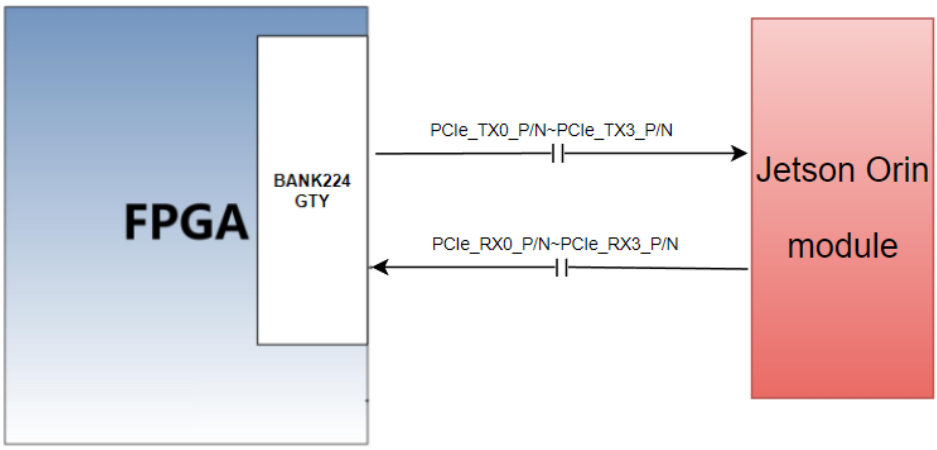


Figure 8: PCIe Interface design diagram

6.2 PCIe x4 Interface FPGA PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
PCIE_RX0_P	MGTYRXP3_224	AV2	PCIE channel 0 receive P
PCIE_RX0_N	MGTYRXN3_224	AV1	PCIE channel 0 receive N
PCIE_RX1_P	MGTYRXP2_224	AW4	PCIE channel 1 receive P
PCIE_RX1_N	MGTYRXN2_224	AW3	PCIE channel 1 receive N
PCIE_RX2_P	MGTYRXP1_224	BA2	PCIE channel 2 receive P
PCIE_RX2_N	MGTYRXN1_224	BA1	PCIE channel 2 receive N
PCIE_RX3_P	MGTYRXP0_224	BC2	PCIE channel 3 receive P
PCIE_RX3_N	MGTYRXN0_224	BC1	PCIE channel 3 receive N
PCIE_TX0_P	MGTYTXP3_224	AV7	PCIE channel 0 transmit P
PCIE_TX0_N	MGTYTXN3_224	AV6	PCIE channel 0 transmit N
PCIE_TX1_P	MGTYTXP2_224	BB5	PCIE channel 1 transmit P
PCIE_TX1_N	MGTYTXN2_224	BB4	PCIE channel 1 transmit N
PCIE_TX2_P	MGTYTXP1_224	BD5	PCIE channel 2 transmit P
PCIE_TX2_N	MGTYTXN1_224	BD4	PCIE channel 2 transmit N
PCIE_TX3_P	MGTYTXP0_224	BF5	PCIE channel 3 transmit P
PCIE_TX3_N	MGTYTXP3_224	AV7	PCIE channel 3 transmit N
PCIE_CLK0_P	MGTREFCLK0P_224	AW9	PCIE channel reference CLK P
PCIE_CLK0_N	MGTREFCLK0N_224	AW8	PCIE channel reference CLK N
FPGA_PCIE_PERST_n	IO_T3U_N12_PERSTN0_65	AR26	PCIE reset signal

Table 5: PCIe x4 Interface FPGA PIN assignment

7 FMC & Interface

7.1 FMC1 + (J9) Schematic Diagram

The AXVU13F is equipped with four FMC+ expansion connectors, identified as FMC1+ (J9), FMC2+ (J8), FMC3+ (J7), and FMC4+ (J23)[1]. These ports support external FMC+ and FMC modules from Xilinx or Alinx series, including modules for HDMI input/output, stereo cameras, high-speed AD converters, and more.

The FMC1+ expansion connector provides 34 LA differential pairs, 2 clock pairs, and 24 HA differential pairs, which are connected to BANK64, BANK66, and BANK67 of the FPGA. The default I/O voltage standard for these banks is 1.8V. Additionally, 20 high-speed GTY transceiver lanes route to the I/O of FPGA BANKs 124, 125, 126, 127, and 128.

The schematic diagram of the connection between the FPGA and the FMC1+ connector is shown in Figure 9.

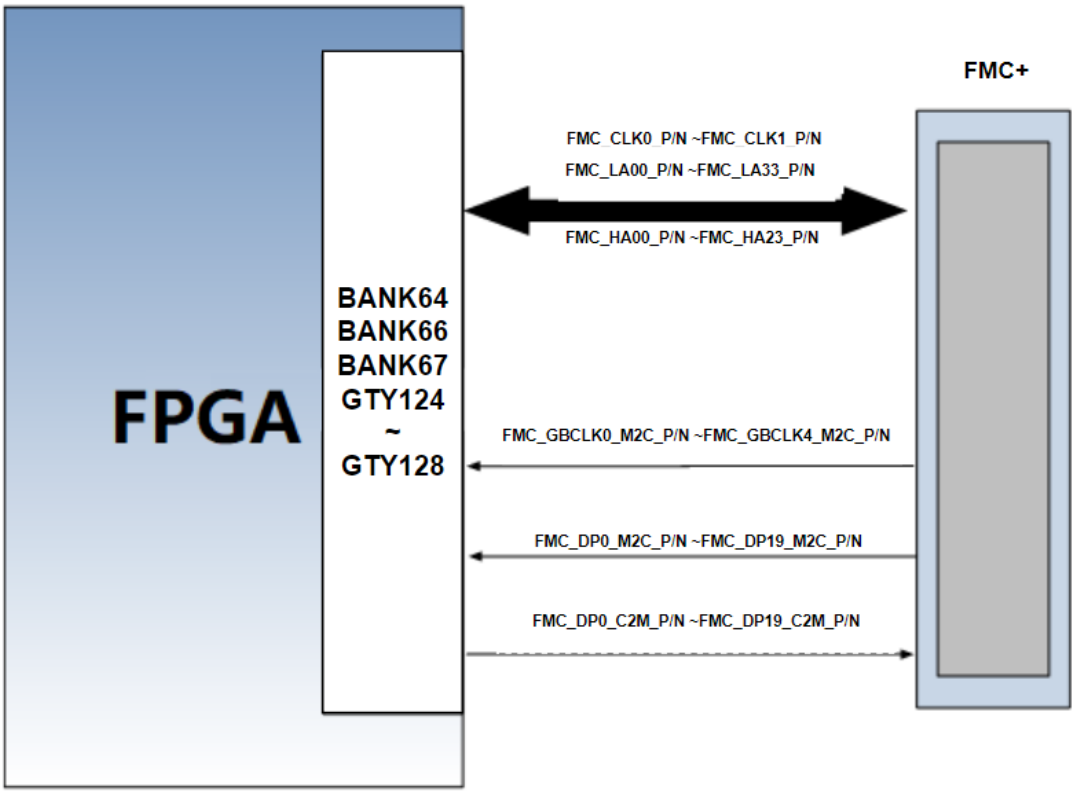


Figure 9: FMC1 + (J9) Schematic diagram

7.2 FMC1 + (J9) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC1_CLK0_N	IO_L12N_T1U_N11_GC_67	BA13	FMC channel 0 input reference CLK N
FMC1_CLK0_P	IO_L12P_T1U_N10_GC_67	AY13	FMC channel 0 input reference CLK P
FMC1_CLK1_N	IO_L12N_T1U_N11_GC_66	AW19	FMC channel 1 input reference CLK N
FMC1_CLK1_P	IO_L12P_T1U_N10_GC_66	AV19	FMC channel 1 input reference CLK P
FMC1_LA00_CC_N	IO_L14N_T2L_N3_GC_67	AW15	FMC LA channel 0 data (CLK) N
FMC1_LA00_CC_P	IO_L14P_T2L_N2_GC_67	AW16	FMC LA channel 0 data (CLK) P
FMC1_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_67	AW13	FMC LA channel 1 data (CLK) N
FMC1_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_67	AW14	FMC LA channel 1 data (CLK) P
FMC1_LA02_N	IO_L17N_T2U_N9_AD10N_67	AU15	FMC LA channel 2 data N
FMC1_LA02_P	IO_L17P_T2U_N8_AD10P_67	AT15	FMC LA channel 2 data P
FMC1_LA03_N	IO_L6N_T0U_N11_AD6N_67	BC13	FMC LA channel 3 data N
FMC1_LA03_P	IO_L6P_T0U_N10_AD6P_67	BC14	FMC LA channel 3 data P
FMC1_LA04_N	IO_L16N_T2U_N7_QBC_AD3N_67	AV14	FMC LA channel 4 data N
FMC1_LA04_P	IO_L16P_T2U_N6_QBC_AD3P_67	AU14	FMC LA channel 4 data P
FMC1_LA05_N	IO_L15N_T2L_N5_AD11N_67	AV13	FMC LA channel 5 data N
FMC1_LA05_P	IO_L15P_T2L_N4_AD11P_67	AU13	FMC LA channel 5 data P
FMC1_LA06_N	IO_L4N_T0U_N7_DBC_AD7N_67	BE13	FMC LA channel 6 data P
FMC1_LA06_P	IO_L4P_T0U_N6_DBC_AD7P_67	BD13	FMC LA channel 6 data P
FMC1_LA07_N	IO_L3N_T0L_N5_AD15N_67	BE16	FMC LA channel 7 data N
FMC1_LA07_P	IO_L3P_T0L_N4_AD15P_67	BD16	FMC LA channel 7 data P
FMC1_LA08_N	IO_L2N_T0L_N3_67	BF15	FMC LA channel 8 data N
FMC1_LA08_P	IO_L2P_T0L_N2_67	BE15	FMC LA channel 8 data P
FMC1_LA09_N	IO_L5N_T0U_N9_AD14N_67	BD14	FMC LA channel 9 data N
FMC1_LA09_P	IO_L5P_T0U_N8_AD14P_67	BD15	FMC LA channel 9 data P
FMC1_LA10_N	IO_L7N_T1L_N1_QBC_AD13N_67	BB12	FMC LA channel 10 data N
FMC1_LA10_P	IO_L7P_T1L_N0_QBC_AD13P_67	BA12	FMC LA channel 10 data P
FMC1_LA11_N	IO_L20N_T3L_N3_AD1N_67	AP14	FMC LA channel 11 data N
FMC1_LA11_P	IO_L20P_T3L_N2_AD1P_67	AP15	FMC LA channel 11 data P
FMC1_LA12_N	IO_L1N_T0L_N1_DBC_67	BF13	FMC LA channel 12 data N
FMC1_LA12_P	IO_L1P_T0L_N0_DBC_67	BF14	FMC LA channel 12 data P
FMC1_LA13_N	IO_L22N_T3U_N7_DBC_AD0N_67	AR13	FMC LA channel 13 data N
FMC1_LA13_P	IO_L22P_T3U_N6_DBC_AD0P_67	AP13	FMC LA channel 13 data P
FMC1_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_67	AR15	FMC LA channel 14 data N
FMC1_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_67	AR16	FMC LA channel 14 data P
FMC1_LA15_N	IO_L23N_T3U_N9_67	AM15	FMC LA channel 15 data N
FMC1_LA15_P	IO_L23P_T3U_N8_67	AL15	FMC LA channel 15 data P
FMC1_LA16_N	IO_L21N_T3L_N5_AD8N_67	AN13	FMC LA channel 16 data N
FMC1_LA16_P	IO_L21P_T3L_N4_AD8P_67	AN14	FMC LA channel 16 data P
FMC1_LA17_CC_N	IO_L14N_T2L_N3_GC_66	AU20	FMC LA channel 17 data (CLK) N

FMC1_LA17_CC_N	IO_L14N_T2L_N3_GC_74	F23	FMC LA channel 17 data (CLK) P
FMC1_LA17_CC_P	IO_L14P_T2L_N2_GC_66	AT20	FMC LA channel 18 data (CLK) N
FMC1_LA17_CC_P	IO_L14P_T2L_N2_GC_74	F24	FMC LA channel 18 data (CLK) P
FMC1_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_66	AU19	FMC LA channel 19 data N
FMC1_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_74	G24	FMC LA channel 19 data P
FMC1_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_66	AT19	FMC LA channel 20 data N
FMC1_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_74	G25	FMC LA channel 20 data P
FMC1_LA19_N	IO_L10N_T1U_N7_QBC_AD4N_66	AW21	FMC LA channel 21 data N
FMC1_LA19_N	IO_L10N_T1U_N7_QBC_AD4N_74	J25	FMC LA channel 21 data P
FMC1_LA19_P	IO_L10P_T1U_N6_QBC_AD4P_66	AV21	FMC LA channel 22 data N
FMC1_LA19_P	IO_L10P_T1U_N6_QBC_AD4P_74	K25	FMC LA channel 22 data P
FMC1_LA20_N	IO_L15N_T2L_N5_AD11N_66	AU17	FMC LA channel 23 data N
FMC1_LA20_N	IO_L15N_T2L_N5_AD11N_74	F22	FMC LA channel 23 data P
FMC1_LA20_P	IO_L15P_T2L_N4_AD11P_66	AT18	FMC LA channel 24 data N
FMC1_LA20_P	IO_L15P_T2L_N4_AD11P_74	G22	FMC LA channel 24 data P
FMC1_LA21_N	IO_L4N_T0U_N7_DBC_AD7N_74	N24	FMC LA channel 25 data N
FMC1_LA21_N	IO_L5N_T0U_N9_AD14N_66	BC17	FMC LA channel 25 data P
FMC1_LA21_P	IO_L4P_T0U_N6_DBC_AD7P_74	P24	FMC LA channel 26 data N
FMC1_LA21_P	IO_L5P_T0U_N8_AD14P_66	BB17	FMC LA channel 26 data P
FMC1_LA22_N	IO_L3N_T0L_N5_AD15N_74	N23	FMC LA channel 27 data N
FMC1_LA22_N	IO_L4N_T0U_N7_DBC_AD7N_66	BD19	FMC LA channel 27 data P
FMC1_LA22_P	IO_L3P_T0L_N4_AD15P_74	P23	FMC LA channel 28 data N
FMC1_LA22_P	IO_L4P_T0U_N6_DBC_AD7P_66	BC19	FMC LA channel 28 data P
FMC1_LA23_N	IO_L2N_T0L_N3_74	M22	FMC LA channel 29 data N
FMC1_LA23_N	IO_L3N_T0L_N5_AD15N_66	BE18	FMC LA channel 29 data P
FMC1_LA23_P	IO_L2P_T0L_N2_74	N22	FMC LA channel 30 data N
FMC1_LA23_P	IO_L3P_T0L_N4_AD15P_66	BD18	FMC LA channel 30 data P
FMC1_LA24_N	IO_L16N_T2U_N7_QBC_AD3N_66	AT17	FMC LA channel 31 data N
FMC1_LA24_N	IO_L16N_T2U_N7_QBC_AD3N_74	E22	FMC LA channel 31 data P
FMC1_LA24_P	IO_L16P_T2U_N6_QBC_AD3P_66	AR17	FMC LA channel 32 data N
FMC1_LA24_P	IO_L16P_T2U_N6_QBC_AD3P_74	E23	FMC LA channel 32 data P
FMC1_LA25_N	IO_L18N_T2U_N11_AD2N_74	D25	FMC LA channel 33 data N
FMC1_LA25_N	IO_L9N_T1L_N5_AD12N_66	AY20	FMC LA channel 33 data P
FMC1_SCL	IO_T2U_N12_66	AU21	FMC I2C bus CLK
FMC1_SDA	IO_T1U_N12_67	BB16	FMC I2C bus data
FMC1_HA00_CC_N	IO_L14N_T2L_N3_GC_64	AW24	FMC HA channel 0 data (CLK) N
FMC1_HA00_CC_P	IO_L14P_T2L_N2_GC_64	AV24	FMC HA channel 0 data (CLK) P
FMC1_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_64	AW23	FMC HA channel 1 data (CLK) N
FMC1_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_64	AV23	FMC HA channel 1 data (CLK) P
FMC1_HA02_N	IO_L7N_T1L_N1_QBC_AD13N_64	BB20	FMC HA channel 2 data N
FMC1_HA02_P	IO_L7P_T1L_N0_QBC_AD13P_64	BA20	FMC HA channel 2 data P

FMC1_HA03_N	IO_L5N_T0U_N9_AD14N_64	BE21	FMC HA channel 3 data N
FMC1_HA03_P	IO_L5P_T0U_N8_AD14P_64	BD21	FMC HA channel 3 data N
FMC1_HA04_N	IO_L2N_T0L_N3_64	BE23	FMC HA channel 4 data N
FMC1_HA04_P	IO_L2P_T0L_N2_64	BD23	FMC HA channel 4 data P
FMC1_HA05_N	IO_L4N_T0U_N7_DBC_AD7N_64	BF22	FMC HA channel 5 data N
FMC1_HA05_P	IO_L4P_T0U_N6_DBC_AD7P_64	BE22	FMC HA channel 5 data P
FMC1_HA06_N	IO_L3N_T0L_N5_AD15N_64	BD24	FMC HA channel 6 data N
FMC1_HA06_P	IO_L3P_T0L_N4_AD15P_64	BC24	FMC HA channel 6 data P
FMC1_HA07_N	IO_L1N_T0L_N1_DBC_64	BF23	FMC HA channel 7 data N
FMC1_HA07_P	IO_L1P_T0L_N0_DBC_64	BF24	FMC HA channel 7 data P
FMC1_HA08_N	IO_L6N_T0U_N11_AD6N_64	BE20	FMC HA channel 8 data N
FMC1_HA08_P	IO_L6P_T0U_N10_AD6P_64	BD20	FMC HA channel 8 data P
FMC1_HA09_N	IO_L15N_T2L_N5_AD11N_64	AV22	FMC HA channel 9 data N
FMC1_HA09_P	IO_L15P_T2L_N4_AD11P_64	AU22	FMC HA channel 9 data P
FMC1_HA10_N	IO_L16N_T2U_N7_QBC_AD3N_64	AT22	FMC HA channel 10 data N
FMC1_HA10_P	IO_L16P_T2U_N6_QBC_AD3P_64	AR22	FMC HA channel 10 data P
FMC1_HA11_N	IO_L17N_T2U_N9_AD10N_64	AT23	FMC HA channel 11 data N
FMC1_HA11_P	IO_L17P_T2U_N8_AD10P_64	AR23	FMC HA channel 11 data P
FMC1_HA12_N	IO_L18N_T2U_N11_AD2N_64	AU24	FMC HA channel 12 data N
FMC1_HA12_P	IO_L18P_T2U_N10_AD2P_64	AT24	FMC HA channel 12 data P
FMC1_HA13_N	IO_L10N_T1U_N7_QBC_AD4N_64	BB24	FMC HA channel 13 data N
FMC1_HA13_P	IO_L10P_T1U_N6_QBC_AD4P_64	BA24	FMC HA channel 13 data P
FMC1_HA14_N	IO_L20N_T3L_N3_AD1N_64	AP23	FMC HA channel 14 data N
FMC1_HA14_P	IO_L20P_T3L_N2_AD1P_64	AN23	FMC HA channel 14 data P
FMC1_HA15_N	IO_L8N_T1L_N3_AD5N_64	BC21	FMC HA channel 15 data N
FMC1_HA15_P	IO_L8P_T1L_N2_AD5P_64	BB21	FMC HA channel 15 data P
FMC1_HA16_N	IO_L9N_T1L_N5_AD12N_64	BC22	FMC HA channel 16 data N
FMC1_HA16_P	IO_L9P_T1L_N4_AD12P_64	BB22	FMC HA channel 16 data P
FMC1_HA17_CC_N	IO_L12N_T1U_N11_GC_64	BA23	FMC HA channel 17 data (CLK) N
FMC1_HA17_CC_P	IO_L12P_T1U_N10_GC_64	AY23	FMC HA channel 17 data (CLK) P
FMC1_HA18_N	IO_L22N_T3U_N7_DBC_AD0N_64	AM24	FMC HA channel 18 data N
FMC1_HA18_P	IO_L22P_T3U_N6_DBC_AD0P_64	AL24	FMC HA channel 18 data P
FMC1_HA19_N	IO_L11N_T1U_N9_GC_64	BA22	FMC HA channel 19 data N
FMC1_HA19_P	IO_L11P_T1U_N8_GC_64	AY22	FMC HA channel 19 data P
FMC1_HA20_N	IO_L21N_T3L_N5_AD8N_64	AP24	FMC HA channel 20 data N
FMC1_HA20_P	IO_L21P_T3L_N4_AD8P_64	AN24	FMC HA channel 20 data P
FMC1_HA21_N	IO_L19N_T3L_N1_DBC_AD9N_64	AN21	FMC HA channel 21 data N
FMC1_HA21_P	IO_L19P_T3L_N0_DBC_AD9P_64	AN22	FMC HA channel 21 data P
FMC1_HA22_N	IO_L23N_T3U_N9_64	AM22	FMC HA channel 22 data N
FMC1_HA22_P	IO_L23P_T3U_N8_64	AL22	FMC HA channel 22 data P
FMC1_HA23_N	IO_L24N_T3U_N11_64	AM21	FMC HA channel 23 data N

FMC1_HA23_P	IO_L24P_T3U_N10_64	AL21	FMC HA channel 23 data P
FMC1_DP0_M2C_P	MGTYRXP0_124	BC45	Transceiver data 0 input P
FMC1_DP0_M2C_N	MGTYRXN0_124	BC46	Transceiver data 0 input N
FMC1_DP1_M2C_P	MGTYRXP1_124	BA45	Transceiver data 1 input P
FMC1_DP1_M2C_N	MGTYRXN1_124	BA46	Transceiver data 1 input N
FMC1_DP2_M2C_P	MGTYRXP2_124	AW45	Transceiver data 2 input P
FMC1_DP2_M2C_N	MGTYRXN2_124	AW46	Transceiver data 2 input N
FMC1_DP3_M2C_P	MGTYRXP3_124	AV43	Transceiver data 3 input P
FMC1_DP3_M2C_N	MGTYRXN3_124	AV44	Transceiver data 3 input N
FMC1_DP4_M2C_P	MGTYRXP1_127	AH43	Transceiver data 4 input P
FMC1_DP4_M2C_N	MGTYRXN1_127	AH44	Transceiver data 4 input N
FMC1_DP5_M2C_P	MGTYRXP3_127	AF43	Transceiver data 5 input P
FMC1_DP5_M2C_N	MGTYRXN3_127	AF44	Transceiver data 5 input N
FMC1_DP6_M2C_P	MGTYRXP2_127	AG45	Transceiver data 6 input P
FMC1_DP6_M2C_N	MGTYRXN2_127	AG46	Transceiver data 6 input N
FMC1_DP7_M2C_P	MGTYRXP0_127	AJ45	Transceiver data 7 input P
FMC1_DP7_M2C_N	MGTYRXN0_127	AJ46	Transceiver data 7 input N
FMC1_DP8_M2C_P	MGTYRXP2_125	AR45	Transceiver data 8 input P
FMC1_DP8_M2C_N	MGTYRXN2_125	AR46	Transceiver data 8 input N
FMC1_DP9_M2C_P	MGTYRXP1_125	AT43	Transceiver data 9 input P
FMC1_DP9_M2C_N	MGTYRXN1_125	AT44	Transceiver data 9 input N
FMC1_DP10_M2C_P	MGTYRXP0_125	AU45	Transceiver data 10 input P
FMC1_DP10_M2C_N	MGTYRXN0_125	AU46	Transceiver data 10 input N
FMC1_DP11_M2C_P	MGTYRXP3_125	AP43	Transceiver data 11 input P
FMC1_DP11_M2C_N	MGTYRXN3_125	AP44	Transceiver data 11 input N
FMC1_DP12_M2C_P	MGTYRXP0_126	AN45	Transceiver data 12 input P
FMC1_DP12_M2C_N	MGTYRXN0_126	AN46	Transceiver data 12 input N
FMC1_DP13_M2C_P	MGTYRXP1_126	AM43	Transceiver data 13 input P
FMC1_DP13_M2C_N	MGTYRXN1_126	AM44	Transceiver data 13 input N
FMC1_DP14_M2C_P	MGTYRXP2_126	AL45	Transceiver data 14 input P
FMC1_DP14_M2C_N	MGTYRXN2_126	AL46	Transceiver data 14 input N
FMC1_DP15_M2C_P	MGTYRXP3_126	AK43	Transceiver data 15 input P
FMC1_DP15_M2C_N	MGTYRXN3_126	AK44	Transceiver data 15 input N
FMC1_DP16_M2C_P	MGTYRXP0_128	AE45	Transceiver data 16 input P
FMC1_DP16_M2C_N	MGTYRXN0_128	AE46	Transceiver data 16 input N
FMC1_DP17_M2C_P	MGTYRXP1_128	AD43	Transceiver data 17 input P
FMC1_DP17_M2C_N	MGTYRXN1_128	AD44	Transceiver data 17 input N
FMC1_DP18_M2C_P	MGTYRXP2_128	AC45	Transceiver data 18 input P
FMC1_DP18_M2C_N	MGTYRXN2_128	AC46	Transceiver data 18 input N
FMC1_DP19_M2C_P	MGTYRXP3_128	AB43	Transceiver data 19 input P
FMC1_DP19_M2C_N	MGTYRXN3_128	AB44	Transceiver data 19 input N

FMC1_DP0_C2M_P	MGTYTXP0_124	BF42	Transceiver data 0 output P
FMC1_DP0_C2M_N	MGTYTXN0_124	BF43	Transceiver data 0 output N
FMC1_DP1_C2M_P	MGTYTXP1_124	BD42	Transceiver data 1 output P
FMC1_DP1_C2M_N	MGTYTXN1_124	BD43	Transceiver data 1 output N
FMC1_DP2_C2M_P	MGTYTXP2_124	BB42	Transceiver data 2 output P
FMC1_DP2_C2M_N	MGTYTXN2_124	BB43	Transceiver data 2 output N
FMC1_DP3_C2M_P	MGTYTXP3_124	AW40	Transceiver data 3 output P
FMC1_DP3_C2M_N	MGTYTXN3_124	AW41	Transceiver data 3 output N
FMC1_DP4_C2M_P	MGTYTXP1_127	AH38	Transceiver data 4 output P
FMC1_DP4_C2M_N	MGTYTXN1_127	AH39	Transceiver data 4 output N
FMC1_DP5_C2M_P	MGTYTXP3_127	AF38	Transceiver data 5 output P
FMC1_DP5_C2M_N	MGTYTXN3_127	AF39	Transceiver data 5 output N
FMC1_DP6_C2M_P	MGTYTXP2_127	AG40	Transceiver data 6 output P
FMC1_DP6_C2M_N	MGTYTXN2_127	AG41	Transceiver data 6 output N
FMC1_DP7_C2M_P	MGTYTXP0_127	AJ40	Transceiver data 7 output P
FMC1_DP7_C2M_N	MGTYTXN0_127	AJ41	Transceiver data 7 output N
FMC1_DP8_C2M_P	MGTYTXP2_125	AR40	Transceiver data 8 output P
FMC1_DP8_C2M_N	MGTYTXN2_125	AR41	Transceiver data 8 output N
FMC1_DP9_C2M_P	MGTYTXP1_125	AT38	Transceiver data 9 output P
FMC1_DP9_C2M_N	MGTYTXN1_125	AT39	Transceiver data 9 output N
FMC1_DP10_C2M_P	MGTYTXP0_125	AU40	Transceiver data 10 output P
FMC1_DP10_C2M_N	MGTYTXN0_125	AU41	Transceiver data 10 output N
FMC1_DP11_C2M_P	MGTYTXP3_125	AP38	Transceiver data 11 output P
FMC1_DP11_C2M_N	MGTYTXN3_125	AP39	Transceiver data 11 output N
FMC1_DP12_C2M_P	MGTYTXP0_126	AN40	Transceiver data 12 output P
FMC1_DP12_C2M_N	MGTYTXN0_126	AN41	Transceiver data 12 output N
FMC1_DP13_C2M_P	MGTYTXP1_126	AM38	Transceiver data 13 output P
FMC1_DP13_C2M_N	MGTYTXN1_126	AM39	Transceiver data 13 output N
FMC1_DP14_C2M_P	MGTYTXP2_126	AL40	Transceiver data 14 output P
FMC1_DP14_C2M_N	MGTYTXN2_126	AL41	Transceiver data 14 output N
FMC1_DP15_C2M_P	MGTYTXP3_126	AK38	Transceiver data 15 output P
FMC1_DP15_C2M_N	MGTYTXN3_126	AK39	Transceiver data 15 output N
FMC1_DP16_C2M_P	MGTYTXP0_128	AE40	Transceiver data 16 output P
FMC1_DP16_C2M_N	MGTYTXN0_128	AE41	Transceiver data 16 output N
FMC1_DP17_C2M_P	MGTYTXP1_128	AD38	Transceiver data 17 output P
FMC1_DP17_C2M_N	MGTYTXN1_128	AD39	Transceiver data 17 output N
FMC1_DP18_C2M_P	MGTYTXP2_128	AC40	Transceiver data 18 output P
FMC1_DP18_C2M_N	MGTYTXN2_128	AC41	Transceiver data 18 output N
FMC1_DP19_C2M_P	MGTYTXP3_128	AB38	Transceiver data 19 output P
FMC1_DP19_C2M_N	MGTYTXN3_128	AB39	Transceiver data 19 output N
FMC1_GBT1_0_M2C_C_N	MGTREFCLK1N_127	AJ37	Transceiver reference CLK 1 input N

FMC1_GBT1_0_M2C_C_P	MGTREFCLK1P_127	AJ36	Transceiver reference CLK 1 input P
FMC1_GBT1_1_M2C_C_N	MGTREFCLK1N_124	AY39	Transceiver reference CLK 1 input N
FMC1_GBT1_1_M2C_C_P	MGTREFCLK1P_124	AY38	Transceiver reference CLK 1 input P
FMC1_GBT1_2_M2C_C_N	MGTREFCLK1N_125	AU37	Transceiver reference CLK 1 input N
FMC1_GBT1_2_M2C_C_P	MGTREFCLK1P_125	AU36	Transceiver reference CLK 1 input P
FMC1_GBT1_3_M2C_C_N	MGTREFCLK1N_126	AN37	Transceiver reference CLK 1 input N
FMC1_GBT1_3_M2C_C_P	MGTREFCLK1P_126	AN36	Transceiver reference CLK 1 input P
FMC1_GBT1_4_M2C_C_N	MGTREFCLK1N_128	AE37	Transceiver reference CLK 1 input N
FMC1_GBT1_4_M2C_C_P	MGTREFCLK1P_128	AE36	Transceiver reference CLK 1 input P
FMC1_GBT0_0_M2C_C_N	MGTREFCLK0N_124	BA41	Transceiver reference CLK 0 input N
FMC1_GBT0_0_M2C_C_P	MGTREFCLK0P_124	BA40	Transceiver reference CLK 0 input P
FMC1_GBTCLK2_M2C_C_N	MGTREFCLK0N_125	AV39	Transceiver reference CLK 0 input N
FMC1_GBTCLK2_M2C_C_P	MGTREFCLK0P_125	AV38	Transceiver reference CLK 0 input P
FMC1_GBTCLK3_M2C_C_N	MGTREFCLK0N_126	AR37	Transceiver reference CLK 0 input N
FMC1_GBTCLK3_M2C_C_P	MGTREFCLK0P_126	AR36	Transceiver reference CLK 0 input P
FMC1_GBTCLK4_M2C_C_N	MGTREFCLK0N_128	AG37	Transceiver reference CLK 0 input N
FMC1_GBTCLK4_M2C_C_P	MGTREFCLK0P_128	AG36	Transceiver reference CLK 0 input P
FMC1_H_PRSNT_M2C_B	IO_L7P_T1L_N0_QBC_AD13P_66	AY17	Reset pin
FMC1_L_PRSNT_M2C_B	IO_L8P_T1L_N2_AD5P_67	AY12	Reset pin
FMC1_PG_C2M	IO_L8N_T1L_N3_AD5N_67	AY11	Power status pin
FMC1_PG_M2C	IO_T1U_N12_66	AV17	Power status pin
FMC1_REFCLK_C2M_N	IO_L9N_T1L_N5_AD12N_67	AY15	reference CLK 1 output N
FMC1_REFCLK_C2M_P	IO_L9P_T1L_N4_AD12P_67	AY16	reference CLK 1 output P
FMC1_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_67	BA14	reference CLK 1 input N
FMC1_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_67	BA15	reference CLK 1 input P
FMC1_SYNC_C2M_N	IO_L10N_T1U_N7_QBC_AD4N_67	BB14	C2M SYNC output N
FMC1_SYNC_C2M_P	IO_L10P_T1U_N6_QBC_AD4P_67	BB15	C2M SYNC output P
FMC1_SYNC_M2C_N	IO_L18N_T2U_N11_AD2N_67	AV16	M2C SYNC input N
FMC1_SYNC_M2C_P	IO_L18P_T2U_N10_AD2P_67	AU16	M2C SYNC input P
FMC1_GBT0_1_M2C_C_N	MGTREFCLK0N_127	AL37	reference CLK 0 input N
FMC1_GBT0_1_M2C_C_P	MGTREFCLK0P_127	AL36	reference CLK 0 input P

Table 6: FMC1 + (J9) Connector PIN assignment

7.3 FMC2 + (J8) Schematic Diagram

The FMC2+ expansion port includes 34 LA differential pairs, 2 clock pairs, and 24 HA signals, which are connected to BANK65, BANK69, and BANK70 of the FPGA. The default I/O voltage standard is 1.8V. Additionally, 16 high-speed GTY transceiver channels are connected to the I/O of the FPGA's BANK129, BANK130, BANK131, and BANK133.

The schematic diagram for the FPGA and the FMC2+ connector is shown in Figure 2-6-2 below:
Figure 10 shows the schematic diagram of the connection between the FPGA and the FMC2+ connector.

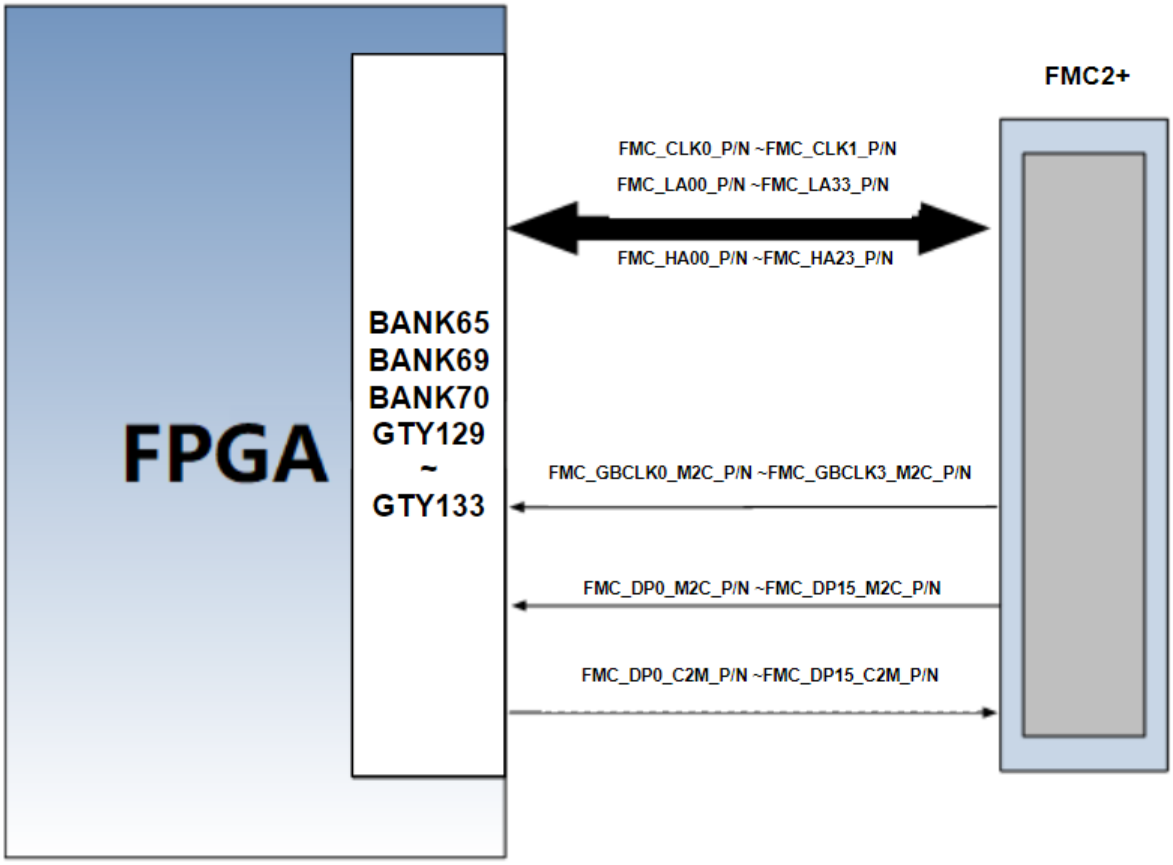


Figure 10: HPC FMC2+ (J8) schematic diagram

7.4 FMC2 + (J8) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC2_CLK0_M2C_N	IO_L11N_T1U_N9_GC_69	N31	FMC channel 0 reference CLK N
FMC2_CLK0_M2C_P	IO_L11P_T1U_N8_GC_69	P31	FMC channel 0 reference CLK P
FMC2_CLK1_M2C_N	IO_L12N_T1U_N11_GC_A09_D25_65	AY28	FMC channel 1 reference CLK N
FMC2_CLK1_M2C_P	IO_L12P_T1U_N10_GC_A08_D24_65	AW28	FMC channel 1 reference CLK P
FMC2_LA00_CC_N	IO_L14N_T2L_N3_GC_69	K32	FMC LA channel 0 data (CLK) N
FMC2_LA00_CC_P	IO_L14P_T2L_N2_GC_69	L32	FMC LA channel 0 data (CLK) P
FMC2_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_69	M32	FMC LA channel 1 data (CLK) N
FMC2_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_69	M31	FMC LA channel 1 data (CLK) P
FMC2_LA02_N	IO_L15N_T2L_N5_AD11N_69	L30	FMC LA channel 2 data N
FMC2_LA02_P	IO_L15P_T2L_N4_AD11P_69	M30	FMC LA channel 2 data P
FMC2_LA03_N	IO_L6N_T0U_N11_AD6N_69	T30	FMC LA channel 3 data N
FMC2_LA03_P	IO_L6P_T0U_N10_AD6P_69	U30	FMC LA channel 3 data P
FMC2_LA04_N	IO_L17N_T2U_N9_AD10N_69	J31	FMC LA channel 4 data N
FMC2_LA04_P	IO_L17P_T2U_N8_AD10P_69	K31	FMC LA channel 4 data P
FMC2_LA05_N	IO_L16N_T2U_N7_QBC_AD3N_69	J30	FMC LA channel 5 data N
FMC2_LA05_P	IO_L16P_T2U_N6_QBC_AD3P_69	K30	FMC LA channel 5 data P
FMC2_LA06_N	IO_L2N_T0L_N3_69	R33	FMC LA channel 6 data P
FMC2_LA06_P	IO_L2P_T0L_N2_69	T33	FMC LA channel 6 data P
FMC2_LA07_N	IO_L5N_T0U_N9_AD14N_69	U31	FMC LA channel 7 data N
FMC2_LA07_P	IO_L5P_T0U_N8_AD14P_69	V31	FMC LA channel 7 data P
FMC2_LA08_N	IO_L4N_T0U_N7_DBC_AD7N_69	V33	FMC LA channel 8 data N
FMC2_LA08_P	IO_L4P_T0U_N6_DBC_AD7P_69	V32	FMC LA channel 8 data P
FMC2_LA09_N	IO_L3N_T0L_N5_AD15N_69	T32	FMC LA channel 9 data N
FMC2_LA09_P	IO_L3P_T0L_N4_AD15P_69	U32	FMC LA channel 9 data P
FMC2_LA10_N	IO_L18N_T2U_N11_AD2N_69	K33	FMC LA channel 10 data N
FMC2_LA10_P	IO_L18P_T2U_N10_AD2P_69	L33	FMC LA channel 10 data P
FMC2_LA11_N	IO_L22N_T3U_N7_DBC_AD0N_69	H33	FMC LA channel 11 data N
FMC2_LA11_P	IO_L22P_T3U_N6_DBC_AD0P_69	J33	FMC LA channel 11 data P
FMC2_LA12_N	IO_L1N_T0L_N1_DBC_69	T34	FMC LA channel 12 data N
FMC2_LA12_P	IO_L1P_T0L_N0_DBC_69	U34	FMC LA channel 12 data P
FMC2_LA13_N	IO_L20N_T3L_N3_AD1N_69	G31	FMC LA channel 13 data N
FMC2_LA13_P	IO_L20P_T3L_N2_AD1P_69	H31	FMC LA channel 13 data P
FMC2_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_69	F30	FMC LA channel 14 data N
FMC2_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_69	G30	FMC LA channel 14 data P
FMC2_LA15_N	IO_L21N_T3L_N5_AD8N_69	G32	FMC LA channel 15 data N
FMC2_LA15_P	IO_L21P_T3L_N4_AD8P_69	H32	FMC LA channel 15 data P
FMC2_LA16_N	IO_L23N_T3U_N9_69	E32	FMC LA channel 16 data N
FMC2_LA16_P	IO_L23P_T3U_N8_69	F32	FMC LA channel 16 data P
FMC2_LA17_CC_N	IO_L14N_T2L_N3_GC_A05_D21_65	AV28	FMC LA channel 17 data (CLK) N

FMC2_LA17_CC_P	IO_L14P_T2L_N2_GC_A04_D20_65	AV27	FMC LA channel 17 data (CLK) P
FMC2_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	AW26	FMC LA channel 18 data (CLK) N
FMC2_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	AV26	FMC LA channel 18 data (CLK) P
FMC2_LA19_N	IO_L6N_T0U_N11_AD6N_A21_65	BC27	FMC LA channel 19 data N
FMC2_LA19_P	IO_L6P_T0U_N10_AD6P_A20_65	BC26	FMC LA channel 19 data P
FMC2_LA20_N	IO_L15N_T2L_N5_AD11N_A03_D19_65	AU27	FMC LA channel 20 data N
FMC2_LA20_P	IO_L15P_T2L_N4_AD11P_A02_D18_65	AU26	FMC LA channel 20 data P
FMC2_LA21_N	IO_L8N_T1L_N3_AD5N_A17_65	BB27	FMC LA channel 21 data N
FMC2_LA21_P	IO_L8P_T1L_N2_AD5P_A16_65	BB26	FMC LA channel 21data P
FMC2_LA22_N	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	AY25	FMC LA channel 22 data N
FMC2_LA22_P	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	AW25	FMC LA channel 22 data P
FMC2_LA23_N	IO_L11N_T1U_N9_GC_A11_D27_65	AY27	FMC LA channel 23 data N
FMC2_LA23_P	IO_L11P_T1U_N8_GC_A10_D26_65	AY26	FMC LA channel 23 data P
FMC2_LA24_N	IO_L17N_T2U_N9_AD10N_D15_65	AT27	FMC LA channel 24 data N
FMC2_LA24_P	IO_L17P_T2U_N8_AD10P_D14_65	AR27	FMC LA channel 24 data P
FMC2_LA25_N	IO_L18N_T2U_N11_AD2N_D13_65	AT28	FMC LA channel 25 data N
FMC2_LA25_P	IO_L18P_T2U_N10_AD2P_D12_65	AR28	FMC LA channel 25 data P
FMC2_LA26_N	IO_L7N_T1L_N1_QBC_AD13N_A19_65	BB25	FMC LA channel 26 data N
FMC2_LA26_P	IO_L7P_T1L_N0_QBC_AD13P_A18_65	BA25	FMC LA channel 26 data P
FMC2_LA27_N	IO_L9N_T1L_N5_AD12N_A15_D31_65	BA28	FMC LA channel 27 data N
FMC2_LA27_P	IO_L9P_T1L_N4_AD12P_A14_D30_65	BA27	FMC LA channel 27 data P
FMC2_LA28_N	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	AT25	FMC LA channel 28 data N
FMC2_LA28_P	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	AR25	FMC LA channel 28 data P
FMC2_LA29_N	IO_L3N_T0L_N5_AD15N_A27_65	BE28	FMC LA channel 29 data N
FMC2_LA29_P	IO_L3P_T0L_N4_AD15P_A26_65	BD28	FMC LA channel 29 data P
FMC2_LA30_N	IO_L24N_T3U_N11_DOUT_CSO_B_65	AL28	FMC LA channel 30 data N
FMC2_LA30_P	IO_L24P_T3U_N10_EMCCLK_65	AL27	FMC LA channel 30 data P
FMC2_LA31_N	IO_L20N_T3L_N3_AD1N_D09_65	AP28	FMC LA channel 31 data N
FMC2_LA31_P	IO_L20P_T3L_N2_AD1P_D08_65	AN28	FMC LA channel 31 data P
FMC2_LA32_N	IO_L19N_T3L_N1_DBC_AD9N_D11_65	AP26	FMC LA channel 32 data N
FMC2_LA32_P	IO_L19P_T3L_N0_DBC_AD9P_D10_65	AP25	FMC LA channel 32 data P
FMC2_LA33_N	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65	AN27	FMC LA channel 33 data N
FMC2_LA33_P	IO_L23P_T3U_N8_I2C_SCLK_65	AM27	FMC LA channel 33 data P
FMC2_SCL	IO_T3U_N12_69	E31	FMC I2C bus CLK
FMC2_SDA	IO_T1U_N12_69	P33	FMC I2C bus data
FMC2_HA00_CC_N	IO_L14N_T2L_N3_GC_70	D36	FMC HA channel 0 data (CLK) N
FMC2_HA00_CC_P	IO_L14P_T2L_N2_GC_70	E36	FMC HA channel 0 data (CLK) P
FMC2_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_70	C37	FMC HA channel 1 data (CLK) N
FMC2_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_70	C36	FMC HA channel 1 data (CLK) P
FMC2_HA02_N	IO_L18N_T2U_N11_AD2N_70	D35	FMC HA channel 2 data N
FMC2_HA02_P	IO_L18P_T2U_N10_AD2P_70	E35	FMC HA channel 2 data P

FMC2_HA03_N	IO_L3N_T0L_N5_AD15N_70	J36	FMC HA channel 3 data N
FMC2_HA03_P	IO_L3P_T0L_N4_AD15P_70	J35	FMC HA channel 3 data N
FMC2_HA04_N	IO_L2N_T0L_N3_70	F37	FMC HA channel 4 data N
FMC2_HA04_P	IO_L2P_T0L_N2_70	G37	FMC HA channel 4 data P
FMC2_HA05_N	IO_L4N_T0U_N7_DBC_AD7N_70	G36	FMC HA channel 5 data N
FMC2_HA05_P	IO_L4P_T0U_N6_DBC_AD7P_70	H36	FMC HA channel 5 data P
FMC2_HA06_N	IO_L5N_T0U_N9_AD14N_70	G34	FMC HA channel 6 data N
FMC2_HA06_P	IO_L5P_T0U_N8_AD14P_70	H34	FMC HA channel 6 data P
FMC2_HA07_N	IO_L1N_T0L_N1_DBC_70	H38	FMC HA channel 7 data N
FMC2_HA07_P	IO_L1P_T0L_N0_DBC_70	H37	FMC HA channel 7 data P
FMC2_HA08_N	IO_L21N_T3L_N5_AD8N_70	C33	FMC HA channel 8 data N
FMC2_HA08_P	IO_L21P_T3L_N4_AD8P_70	D33	FMC HA channel 8 data P
FMC2_HA09_N	IO_L16N_T2U_N7_QBC_AD3N_70	B37	FMC HA channel 9 data N
FMC2_HA09_P	IO_L16P_T2U_N6_QBC_AD3P_70	B36	FMC HA channel 9 data P
FMC2_HA10_N	IO_L17N_T2U_N9_AD10N_70	A35	FMC HA channel 10 data N
FMC2_HA10_P	IO_L17P_T2U_N8_AD10P_70	B35	FMC HA channel 10 data P
FMC2_HA11_N	IO_L15N_T2L_N5_AD11N_70	A38	FMC HA channel 11 data N
FMC2_HA11_P	IO_L15P_T2L_N4_AD11P_70	A37	FMC HA channel 11 data P
FMC2_HA12_N	IO_L20N_T3L_N3_AD1N_70	C34	FMC HA channel 12 data N
FMC2_HA12_P	IO_L20P_T3L_N2_AD1P_70	D34	FMC HA channel 12 data P
FMC2_HA13_N	IO_L6N_T0U_N11_AD6N_70	F35	FMC HA channel 13 data N
FMC2_HA13_P	IO_L6P_T0U_N10_AD6P_70	F34	FMC HA channel 13 data P
FMC2_HA14_N	IO_L8N_T1L_N3_AD5N_70	D39	FMC HA channel 14 data N
FMC2_HA14_P	IO_L8P_T1L_N2_AD5P_70	E39	FMC HA channel 14 data P
FMC2_HA15_N	IO_L23N_T3U_N9_70	B32	FMC HA channel 15 data N
FMC2_HA15_P	IO_L23P_T3U_N8_70	C32	FMC HA channel 15 data P
FMC2_HA16_N	IO_L19N_T3L_N1_DBC_AD9N_70	A34	FMC HA channel 16 data N
FMC2_HA16_P	IO_L19P_T3L_N0_DBC_AD9P_70	B34	FMC HA channel 16 data P
FMC2_HA17_CC_N	IO_L12N_T1U_N11_GC_70	C39	FMC HA channel 17 data (CLK) N
FMC2_HA17_CC_P	IO_L12P_T1U_N10_GC_70	C38	FMC HA channel 17 data (CLK) P
FMC2_HA18_N	IO_L7N_T1L_N1_QBC_AD13N_70	D40	FMC HA channel 18 data N
FMC2_HA18_P	IO_L7P_T1L_N0_QBC_AD13P_70	E40	FMC HA channel 18 data P
FMC2_HA19_N	IO_L24N_T3U_N11_70	C31	FMC HA channel 19 data N
FMC2_HA19_P	IO_L24P_T3U_N10_70	D31	FMC HA channel 19 data P
FMC2_HA20_N	IO_L22N_T3U_N7_DBC_AD0N_70	A33	FMC HA channel 20 data N
FMC2_HA20_P	IO_L22P_T3U_N6_DBC_AD0P_70	A32	FMC HA channel 20 data P
FMC2_HA21_N	IO_L11N_T1U_N9_GC_70	D38	FMC HA channel 21 data N
FMC2_HA21_P	IO_L11P_T1U_N8_GC_70	E38	FMC HA channel 21 data P
FMC2_HA22_N	IO_L9N_T1L_N5_AD12N_70	A40	FMC HA channel 22 data N
FMC2_HA22_P	IO_L9P_T1L_N4_AD12P_70	B40	FMC HA channel 22 data P
FMC2_HA23_N	IO_L10N_T1U_N7_QBC_AD4N_70	A39	FMC HA channel 23 data N

FMC2_HA23_P	IO_L10P_T1U_N6_QBC_AD4P_70	B39	FMC HA channel 23 data P
FMC2_DP0_M2C_P	MGTYRXP0_129	AA45	Transceiver data 0 input P
FMC2_DP0_M2C_N	MGTYRXN0_129	AA46	Transceiver data 0 input N
FMC2_DP1_M2C_P	MGTYRXP3_129	V43	Transceiver data 1 input P
FMC2_DP1_M2C_N	MGTYRXN3_129	V44	Transceiver data 1 input N
FMC2_DP2_M2C_P	MGTYRXP2_129	W45	Transceiver data 2 input P
FMC2_DP2_M2C_N	MGTYRXN2_129	W46	Transceiver data 2 input N
FMC2_DP3_M2C_P	MGTYRXP1_129	Y43	Transceiver data 3 input P
FMC2_DP3_M2C_N	MGTYRXN1_129	Y44	Transceiver data 3 input N
FMC2_DP4_M2C_P	MGTYRXP2_133	F45	Transceiver data 4 input P
FMC2_DP4_M2C_N	MGTYRXN2_133	F46	Transceiver data 4 input N
FMC2_DP5_M2C_P	MGTYRXP0_133	J45	Transceiver data 5 input P
FMC2_DP5_M2C_N	MGTYRXN0_133	J46	Transceiver data 5 input N
FMC2_DP6_M2C_P	MGTYRXP1_133	H43	Transceiver data 6 input P
FMC2_DP6_M2C_N	MGTYRXN1_133	H44	Transceiver data 6 input N
FMC2_DP7_M2C_P	MGTYRXP3_133	D45	Transceiver data 7 input P
FMC2_DP7_M2C_N	MGTYRXN3_133	D46	Transceiver data 7 input N
FMC2_DP8_M2C_P	MGTYRXP2_130	R45	Transceiver data 8 input P
FMC2_DP8_M2C_N	MGTYRXN2_130	R46	Transceiver data 8 input N
FMC2_DP9_M2C_P	MGTYRXP0_130	U45	Transceiver data 9 input P
FMC2_DP9_M2C_N	MGTYRXN0_130	U46	Transceiver data 9 input N
FMC2_DP10_M2C_P	MGTYRXP1_130	T43	Transceiver data 10 input P
FMC2_DP10_M2C_N	MGTYRXN1_130	T44	Transceiver data 10 input N
FMC2_DP11_M2C_P	MGTYRXP3_130	P43	Transceiver data 11 input P
FMC2_DP11_M2C_N	MGTYRXN3_130	P44	Transceiver data 11 input N
FMC2_DP12_M2C_P	MGTYRXP0_131	N45	Transceiver data 12 input P
FMC2_DP12_M2C_N	MGTYRXN0_131	N46	Transceiver data 12 input N
FMC2_DP13_M2C_P	MGTYRXP1_131	M43	Transceiver data 13 input P
FMC2_DP13_M2C_N	MGTYRXN1_131	M44	Transceiver data 13 input N
FMC2_DP14_M2C_P	MGTYRXP2_131	L45	Transceiver data 14 input P
FMC2_DP14_M2C_N	MGTYRXN2_131	L46	Transceiver data 14 input N
FMC2_DP15_M2C_P	MGTYRXP3_131	K43	Transceiver data 15 input P
FMC2_DP15_M2C_N	MGTYRXN3_131	K44	Transceiver data 15 input N
FMC2_DP0_C2M_P	MGTYTXP0_129	AA40	Transceiver data 0 output P
FMC2_DP0_C2M_N	MGTYTXN0_129	AA41	Transceiver data 0 output N
FMC2_DP1_C2M_P	MGTYTXP3_129	V38	Transceiver data 1 output P
FMC2_DP1_C2M_N	MGTYTXN3_129	V39	Transceiver data 1 output N
FMC2_DP2_C2M_P	MGTYTXP2_129	W40	Transceiver data 2 output P
FMC2_DP2_C2M_N	MGTYTXN2_129	W41	Transceiver data 2 output N
FMC2_DP3_C2M_P	MGTYTXP1_129	Y38	Transceiver data 3 output P
FMC2_DP3_C2M_N	MGTYTXN1_129	Y39	Transceiver data 3 output N

FMC2_DP4_C2M_P	MGTYTXP2_133	C42	Transceiver data 4 output P
FMC2_DP4_C2M_N	MGTYTXN2_133	C43	Transceiver data 4 output N
FMC2_DP5_C2M_P	MGTYTXP0_133	G40	Transceiver data 5 output P
FMC2_DP5_C2M_N	MGTYTXN0_133	G41	Transceiver data 5 output N
FMC2_DP6_C2M_P	MGTYTXP1_133	E42	Transceiver data 6 output P
FMC2_DP6_C2M_N	MGTYTXN1_133	E43	Transceiver data 6 output N
FMC2_DP7_C2M_P	MGTYTXP3_133	A42	Transceiver data 7 output P
FMC2_DP7_C2M_N	MGTYTXN3_133	A43	Transceiver data 7 output N
FMC2_DP8_C2M_P	MGTYTXP2_130	R40	Transceiver data 8 output P
FMC2_DP8_C2M_N	MGTYTXN2_130	R41	Transceiver data 8 output N
FMC2_DP9_C2M_P	MGTYTXP0_130	U40	Transceiver data 9 output P
FMC2_DP9_C2M_N	MGTYTXN0_130	U41	Transceiver data 9 output N
FMC2_DP10_C2M_P	MGTYTXP1_130	T38	Transceiver data 10 output P
FMC2_DP10_C2M_N	MGTYTXN1_130	T39	Transceiver data 10 output N
FMC2_DP11_C2M_P	MGTYTXP3_130	P38	Transceiver data 11 output P
FMC2_DP11_C2M_N	MGTYTXN3_130	P39	Transceiver data 11 output N
FMC2_DP12_C2M_P	MGTYTXP0_131	N40	Transceiver data 12 output P
FMC2_DP12_C2M_N	MGTYTXN0_131	N41	Transceiver data 12 output N
FMC2_DP13_C2M_P	MGTYTXP1_131	M38	Transceiver data 13 output P
FMC2_DP13_C2M_N	MGTYTXN1_131	M39	Transceiver data 13 output N
FMC2_DP14_C2M_P	MGTYTXP2_131	L40	Transceiver data 14 output P
FMC2_DP14_C2M_N	MGTYTXN2_131	L41	Transceiver data 14 output N
FMC2_DP15_C2M_P	MGTYTXP3_131	J40	Transceiver data 15 output P
FMC2_DP15_C2M_N	MGTYTXN3_131	J41	Transceiver data 15 output N
FMC2_GBT1_0_M2C_C_N	MGTREFCLK1N_129	AA37	Transceiver reference CLK1 input N
FMC2_GBT1_0_M2C_C_P	MGTREFCLK1P_129	AA36	Transceiver reference CLK1 input P
FMC2_GBT1_1_M2C_C_N	MGTREFCLK1N_133	K39	Transceiver reference CLK1 input N
FMC2_GBT1_1_M2C_C_P	MGTREFCLK1P_133	K38	Transceiver reference CLK1 input P
FMC2_GBT1_2_M2C_C_N	MGTREFCLK1N_130	U37	Transceiver reference CLK1 input N
FMC2_GBT1_2_M2C_C_P	MGTREFCLK1P_130	U36	Transceiver reference CLK1 input P
FMC2_GBT1_3_M2C_C_N	MGTREFCLK1N_131	N37	Transceiver reference CLK1 input N
FMC2_GBT1_3_M2C_C_P	MGTREFCLK1P_131	N36	Transceiver reference CLK1 input P
FMC2_GBT0_0_M2C_C_N	MGTREFCLK0N_129	AC37	Transceiver reference CLK0 input N
FMC2_GBT0_0_M2C_C_P	MGTREFCLK0P_129	AC36	Transceiver reference CLK0 input P
FMC2_GBTCLK2_M2C_C_N	MGTREFCLK0N_130	W37	Transceiver reference CLK0 input N
FMC2_GBTCLK2_M2C_C_P	MGTREFCLK0P_130	W36	Transceiver reference CLK0 input P
FMC2_GBTCLK3_M2C_C_N	MGTREFCLK0N_131	R37	Transceiver reference CLK0 input N
FMC2_GBTCLK3_M2C_C_P	MGTREFCLK0P_131	R36	Transceiver reference CLK0 input P
FMC2_H_PRSNT_M2C_B	IO_T3U_N12_70	B31	Reset PIN
FMC2_L_PRSNT_M2C_B	IO_T2U_N12_69	K34	Reset PIN
FMC2_PG_C2M	IO_L9N_T1L_N5_AD12N_69	N34	Power statues PIN

FMC2_PG_M2C	IO_L9P_T1L_N4_AD12P_69	P34	Power statues PIN
FMC2_REFCLK_C2M_N	IO_L8N_T1L_N3_AD5N_69	R32	reference CLK1 output N
FMC2_REFCLK_C2M_P	IO_L8P_T1L_N2_AD5P_69	R31	reference CLK1 output P
FMC2_REFCLK_M2C_N	IO_L12N_T1U_N11_GC_69	N33	reference CLK1 input N
FMC2_REFCLK_M2C_P	IO_L12P_T1U_N10_GC_69	N32	reference CLK1 input P
FMC2_SYNC_C2M_N	IO_L24N_T3U_N11_69	E33	C2M SYNC output N
FMC2_SYNC_C2M_P	IO_L24P_T3U_N10_69	F33	C2M SYNC output P
FMC2_SYNC_M2C_N	IO_L7N_T1L_N1_QBC_AD13N_69	P30	M2C SYNC input N
FMC2_SYNC_M2C_P	IO_L7P_T1L_N0_QBC_AD13P_69	R30	M2C SYNC input P
FMC2_GBT0_1_M2C_C_N	MGTREFCLK0N_133	L37	reference CLK0 input N
FMC2_GBT0_1_M2C_C_P	MGTREFCLK0P_133	L36	reference CLK0 input P

Table 7: FMC2 + (J8) Connector PIN assignment

7.5 FMC3 + (J7) Schematic Diagram

The port provides 34 LA differential pairs and 2 clock pairs, which are connected to BANK71 and BANK74 of the FPGA. The default I/O voltage standard for these signals is 1.8V. Additionally, 16 high-speed GTY transceiver channels are connected to the I/O of the FPGA's BANK228 through BANK233.

Figure 11 shows the schematic diagram of the connection between the FPGA and the FMC3+ connector.

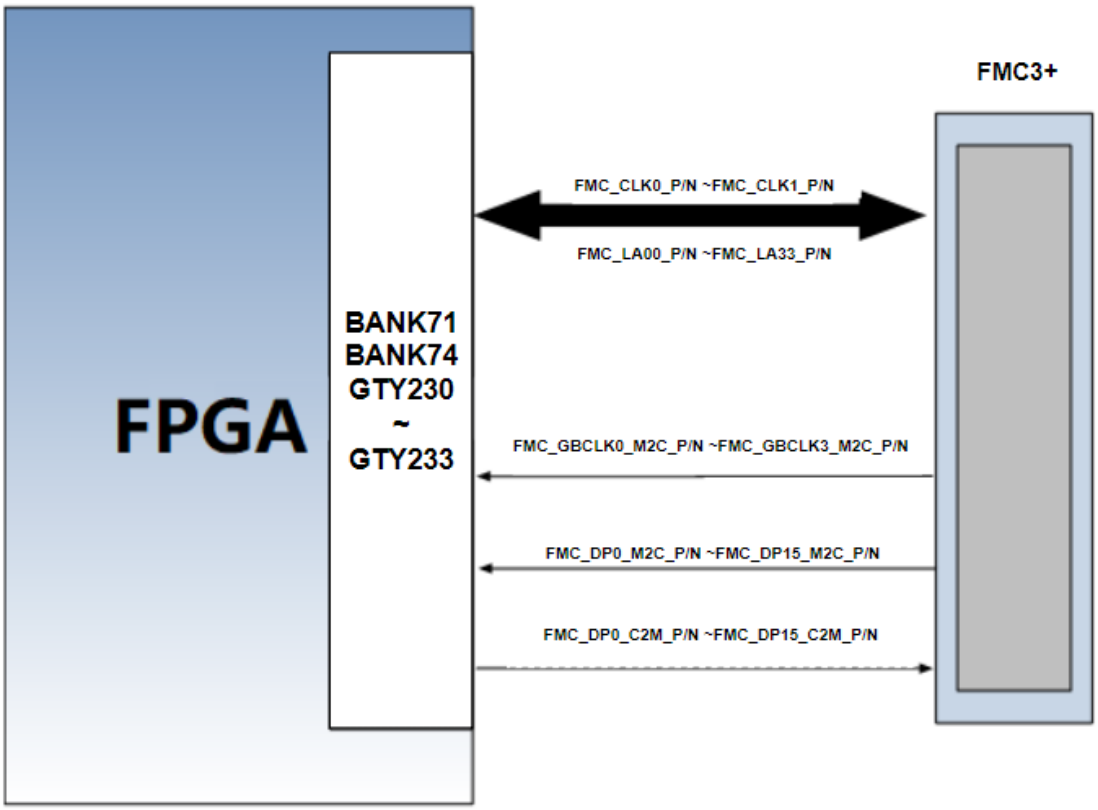


Figure 11: FMC3 + (J7) schematic diagram

7.6 FMC3 + (J7) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC3_CLK0_N	IO_L12N_T1U_N11_GC_71	J29	FMC channel 0 input reference CLK N
FMC3_CLK0_P	IO_L12P_T1U_N10_GC_71	J28	FMC channel 0 input reference CLK P
FMC3_CLK1_N	IO_L11N_T1U_N9_GC_74	H23	FMC channel 1 input reference CLK N
FMC3_CLK1_P	IO_L11P_T1U_N8_GC_74	J23	FMC channel 1 input reference CLK P
FMC3_LA00_CC_N	IO_L14N_T2L_N3_GC_71	G27	FMC LA channel 0 data (CLK) N
FMC3_LA00_CC_P	IO_L14P_T2L_N2_GC_71	G26	FMC LA channel 0 data (CLK) P
FMC3_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_71	H26	FMC LA channel 1 data (CLK) N
FMC3_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_71	J26	FMC LA channel 1 data (CLK) P
FMC3_LA02_N	IO_L15N_T2L_N5_AD11N_71	G29	FMC LA channel 2 data N
FMC3_LA02_P	IO_L15P_T2L_N4_AD11P_71	H29	FMC LA channel 2 data P
FMC3_LA03_N	IO_L24N_T3U_N11_71	A30	FMC LA channel 3 data N
FMC3_LA03_P	IO_L24P_T3U_N10_71	B30	FMC LA channel 3 data P
FMC3_LA04_N	IO_L16N_T2U_N7_QBC_AD3N_71	F29	FMC LA channel 4 data N
FMC3_LA04_P	IO_L16P_T2U_N6_QBC_AD3P_71	F28	FMC LA channel 4 data P
FMC3_LA05_N	IO_L17N_T2U_N9_AD10N_71	E27	FMC LA channel 5 data N
FMC3_LA05_P	IO_L17P_T2U_N8_AD10P_71	F27	FMC LA channel 5 data P
FMC3_LA06_N	IO_L4N_T0U_N7_DBC_AD7N_71	N29	FMC LA channel 6 data P
FMC3_LA06_P	IO_L4P_T0U_N6_DBC_AD7P_71	P29	FMC LA channel 6 data P
FMC3_LA07_N	IO_L2N_T0L_N3_71	R27	FMC LA channel 7 data N
FMC3_LA07_P	IO_L2P_T0L_N2_71	T27	FMC LA channel 7 data P
FMC3_LA08_N	IO_L5N_T0U_N9_AD14N_71	N28	FMC LA channel 8 data N
FMC3_LA08_P	IO_L5P_T0U_N8_AD14P_71	P28	FMC LA channel 8 data P
FMC3_LA09_N	IO_L3N_T0L_N5_AD15N_71	R26	FMC LA channel 9 data N
FMC3_LA09_P	IO_L3P_T0L_N4_AD15P_71	T26	FMC LA channel 9 data P
FMC3_LA10_N	IO_L18N_T2U_N11_AD2N_71	D28	FMC LA channel 10 data N
FMC3_LA10_P	IO_L18P_T2U_N10_AD2P_71	E28	FMC LA channel 10 data P
FMC3_LA11_N	IO_L23N_T3U_N9_71	A29	FMC LA channel 11 data N
FMC3_LA11_P	IO_L23P_T3U_N8_71	B29	FMC LA channel 11 data P
FMC3_LA12_N	IO_L1N_T0L_N1_DBC_71	R28	FMC LA channel 12 data N
FMC3_LA12_P	IO_L1P_T0L_N0_DBC_71	T28	FMC LA channel 12 data P
FMC3_LA13_N	IO_L22N_T3U_N7_DBC_AD0N_71	A28	FMC LA channel 13 data N
FMC3_LA13_P	IO_L22P_T3U_N6_DBC_AD0P_71	A27	FMC LA channel 13 data P
FMC3_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_71	B27	FMC LA channel 14 data N
FMC3_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_71	C27	FMC LA channel 14 data P
FMC3_LA15_N	IO_L21N_T3L_N5_AD8N_71	D30	FMC LA channel 15 data N
FMC3_LA15_P	IO_L21P_T3L_N4_AD8P_71	E30	FMC LA channel 15 data P
FMC3_LA16_N	IO_L20N_T3L_N3_AD1N_71	C29	FMC LA channel 16 data N
FMC3_LA16_P	IO_L20P_T3L_N2_AD1P_71	D29	FMC LA channel 16 data P
FMC3_LA17_CC_N	IO_L14N_T2L_N3_GC_74	F23	FMC LA channel 17 data (CLK) N

FMC3_LA17_CC_P	IO_L14P_T2L_N2_GC_74	F24	FMC LA channel 17 data (CLK) P
FMC3_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_74	G24	FMC LA channel 18 data (CLK) N
FMC3_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_74	G25	FMC LA channel 18 data (CLK) P
FMC3_LA19_N	IO_L10N_T1U_N7_QBC_AD4N_74	J25	FMC LA channel 19 data N
FMC3_LA19_P	IO_L10P_T1U_N6_QBC_AD4P_74	K25	FMC LA channel 19 data P
FMC3_LA20_N	IO_L15N_T2L_N5_AD11N_74	F22	FMC LA channel 20 data N
FMC3_LA20_P	IO_L15P_T2L_N4_AD11P_74	G22	FMC LA channel 20 data P
FMC3_LA21_N	IO_L4N_T0U_N7_DBC_AD7N_74	N24	FMC LA channel 21 data N
FMC3_LA21_P	IO_L4P_T0U_N6_DBC_AD7P_74	P24	FMC LA channel 21 data P
FMC3_LA22_N	IO_L3N_T0L_N5_AD15N_74	N23	FMC LA channel 22 data N
FMC3_LA22_P	IO_L3P_T0L_N4_AD15P_74	P23	FMC LA channel 22 data P
FMC3_LA23_N	IO_L2N_T0L_N3_74	M22	FMC LA channel 23 data N
FMC3_LA23_P	IO_L2P_T0L_N2_74	N22	FMC LA channel 23 data P
FMC3_LA24_N	IO_L16N_T2U_N7_QBC_AD3N_74	E22	FMC LA channel 24 data N
FMC3_LA24_P	IO_L16P_T2U_N6_QBC_AD3P_74	E23	FMC LA channel 24 data P
FMC3_LA25_N	IO_L18N_T2U_N11_AD2N_74	D25	FMC LA channel 25 data N
FMC3_LA25_P	IO_L18P_T2U_N10_AD2P_74	E25	FMC LA channel 25 data P
FMC3_LA26_N	IO_L1N_T0L_N1_DBC_74	P21	FMC LA channel 26 data N
FMC3_LA26_P	IO_L1P_T0L_N0_DBC_74	R21	FMC LA channel 26 data P
FMC3_LA27_N	IO_L5N_T0U_N9_AD14N_74	M24	FMC LA channel 27 data N
FMC3_LA27_P	IO_L5P_T0U_N8_AD14P_74	M25	FMC LA channel 27 data P
FMC3_LA28_N	IO_L17N_T2U_N9_AD10N_74	D23	FMC LA channel 28 data N
FMC3_LA28_P	IO_L17P_T2U_N8_AD10P_74	D24	FMC LA channel 28 data P
FMC3_LA29_N	IO_L19N_T3L_N1_DBC_AD9N_74	B22	FMC LA channel 29 data N
FMC3_LA29_P	IO_L19P_T3L_N0_DBC_AD9P_74	C22	FMC LA channel 29 data P
FMC3_LA30_N	IO_L21N_T3L_N5_AD8N_74	B26	FMC LA channel 30 data N
FMC3_LA30_P	IO_L21P_T3L_N4_AD8P_74	C26	FMC LA channel 30 data P
FMC3_LA31_N	IO_L23N_T3U_N9_74	A24	FMC LA channel 31 data N
FMC3_LA31_P	IO_L23P_T3U_N8_74	B24	FMC LA channel 31 data P
FMC3_LA32_N	IO_L20N_T3L_N3_AD1N_74	C23	FMC LA channel 32 data N
FMC3_LA32_P	IO_L20P_T3L_N2_AD1P_74	C24	FMC LA channel 32 data P
FMC3_LA33_N	IO_L22N_T3U_N7_DBC_AD0N_74	A22	FMC LA channel 33 data N
FMC3_LA33_P	IO_L22P_T3U_N6_DBC_AD0P_74	A23	FMC LA channel 33 data P
FMC3_SCL	IO_L24P_T3U_N10_74	B25	FMC I2C bus CLK
FMC3_SDA	IO_L24N_T3U_N11_74	A25	FMC I2C bus data
FMC3_DP0_M2C_P	MGTYRXP2_233	C4	Transceiver data 0 input P
FMC3_DP0_M2C_N	MGTYRXN2_233	C3	Transceiver data 0 input N
FMC3_DP1_M2C_P	MGTYRXP1_233	D2	Transceiver data 1 input P
FMC3_DP1_M2C_N	MGTYRXN1_233	D1	Transceiver data 1 input N
FMC3_DP2_M2C_P	MGTYRXP0_233	E4	Transceiver data 2 input P
FMC3_DP2_M2C_N	MGTYRXN0_233	E3	Transceiver data 2 input N

FMC3_DP3_M2C_P	MGTYRXP3_233	A5	Transceiver data 3 input P
FMC3_DP3_M2C_N	MGTYRXN3_233	A4	Transceiver data 3 input N
FMC3_DP4_M2C_P	MGTYRXP0_230	U4	Transceiver data 4 input P
FMC3_DP4_M2C_N	MGTYRXN0_230	U3	Transceiver data 4 input N
FMC3_DP5_M2C_P	MGTYRXP2_230	R4	Transceiver data 5 input P
FMC3_DP5_M2C_N	MGTYRXN2_230	R3	Transceiver data 5 input N
FMC3_DP6_M2C_P	MGTYRXP1_230	T2	Transceiver data 6 input P
FMC3_DP6_M2C_N	MGTYRXN1_230	T1	Transceiver data 6 input N
FMC3_DP7_M2C_P	MGTYRXP3_230	P2	Transceiver data 7 input P
FMC3_DP7_M2C_N	MGTYRXN3_230	P1	Transceiver data 7 input N
FMC3_DP8_M2C_P	MGTYRXP1_232	H2	Transceiver data 8 input P
FMC3_DP8_M2C_N	MGTYRXN1_232	H1	Transceiver data 8 input N
FMC3_DP9_M2C_P	MGTYRXP3_232	F2	Transceiver data 9 input P
FMC3_DP9_M2C_N	MGTYRXN3_232	F1	Transceiver data 9 input N
FMC3_DP10_M2C_P	MGTYRXP2_232	G4	Transceiver data 10 input P
FMC3_DP10_M2C_N	MGTYRXN2_232	G3	Transceiver data 10 input N
FMC3_DP11_M2C_P	MGTYRXP0_232	J4	Transceiver data 11 input P
FMC3_DP11_M2C_N	MGTYRXN0_232	J3	Transceiver data 11 input N
FMC3_DP12_M2C_P	MGTYRXP3_231	K2	Transceiver data 12 input P
FMC3_DP12_M2C_N	MGTYRXN3_231	K1	Transceiver data 12 input N
FMC3_DP13_M2C_P	MGTYRXP2_231	L4	Transceiver data 13 input P
FMC3_DP13_M2C_N	MGTYRXN2_231	L3	Transceiver data 13 input N
FMC3_DP14_M2C_P	MGTYRXP1_231	M2	Transceiver data 14 input P
FMC3_DP14_M2C_N	MGTYRXN1_231	M1	Transceiver data 14 input N
FMC3_DP15_M2C_P	MGTYRXP0_231	N4	Transceiver data 15 input P
FMC3_DP15_M2C_N	MGTYRXN0_231	N3	Transceiver data 15 input N
FMC3_DP0_C2M_P	MGTYTXP2_233	C9	Transceiver data 0 output P
FMC3_DP0_C2M_N	MGTYTXN2_233	C8	Transceiver data 0 output N
FMC3_DP1_C2M_P	MGTYTXP1_233	D7	Transceiver data 1 output P
FMC3_DP1_C2M_N	MGTYTXN1_233	D6	Transceiver data 1 output N
FMC3_DP2_C2M_P	MGTYTXP0_233	E9	Transceiver data 2 output P
FMC3_DP2_C2M_N	MGTYTXN0_233	E8	Transceiver data 2 output N
FMC3_DP3_C2M_P	MGTYTXP3_233	A9	Transceiver data 3 output P
FMC3_DP3_C2M_N	MGTYTXN3_233	A8	Transceiver data 3 output N
FMC3_DP4_C2M_P	MGTYTXP0_230	U9	Transceiver data 4 output P
FMC3_DP4_C2M_N	MGTYTXN0_230	U8	Transceiver data 4 output N
FMC3_DP5_C2M_P	MGTYTXP2_230	R9	Transceiver data 5 output P
FMC3_DP5_C2M_N	MGTYTXN2_230	R8	Transceiver data 5 output N
FMC3_DP6_C2M_P	MGTYTXP1_230	T7	Transceiver data 6 output P
FMC3_DP6_C2M_N	MGTYTXN1_230	T6	Transceiver data 6 output N
FMC3_DP7_C2M_P	MGTYTXP3_230	P7	Transceiver data 7 output P

FMC3_DP7_C2M_N	MGTYTXN3_230	P6	Transceiver data 7 output N
FMC3_DP8_C2M_P	MGTYTXP1_232	H7	Transceiver data 8 output P
FMC3_DP8_C2M_N	MGTYTXN1_232	H6	Transceiver data 8 output N
FMC3_DP9_C2M_P	MGTYTXP3_232	F7	Transceiver data 9 output P
FMC3_DP9_C2M_N	MGTYTXN3_232	F6	Transceiver data 9 output N
FMC3_DP10_C2M_P	MGTYTXP2_232	G9	Transceiver data 10 output P
FMC3_DP10_C2M_N	MGTYTXN2_232	G8	Transceiver data 10 output N
FMC3_DP11_C2M_P	MGTYTXP0_232	J9	Transceiver data 11 output P
FMC3_DP11_C2M_N	MGTYTXN0_232	J8	Transceiver data 11 output N
FMC3_DP12_C2M_P	MGTYTXP3_231	K7	Transceiver data 12 output P
FMC3_DP12_C2M_N	MGTYTXN3_231	K6	Transceiver data 12 output N
FMC3_DP13_C2M_P	MGTYTXP2_231	L9	Transceiver data 13 output P
FMC3_DP13_C2M_N	MGTYTXN2_231	L8	Transceiver data 13 output N
FMC3_DP14_C2M_P	MGTYTXP1_231	M7	Transceiver data 14 output P
FMC3_DP14_C2M_N	MGTYTXN1_231	M6	Transceiver data 14 output N
FMC3_DP15_C2M_P	MGTYTXP0_231	N9	Transceiver data 15 output P
FMC3_DP15_C2M_N	MGTYTXN0_231	N8	Transceiver data 15 output N
FMC3_GBT1_0_M2C_C_N	MGTREFCLK1N_232	F10	Transceiver reference CLK 1 input N
FMC3_GBT1_0_M2C_C_P	MGTREFCLK1P_232	F11	Transceiver reference CLK 1 input P
FMC3_GBT1_1_M2C_C_N	MGTREFCLK1N_233	B10	Transceiver reference CLK 1 input N
FMC3_GBT1_1_M2C_C_P	MGTREFCLK1P_233	B11	Transceiver reference CLK 1 input P
FMC3_GBT1_2_M2C_C_N	MGTREFCLK1N_230	P10	Transceiver reference CLK 1 input N
FMC3_GBT1_2_M2C_C_P	MGTREFCLK1P_230	P11	Transceiver reference CLK 1 input P
FMC3_GBT1_3_M2C_C_N	MGTREFCLK1N_231	K10	Transceiver reference CLK 1 input N
FMC3_GBT1_3_M2C_C_P	MGTREFCLK1P_231	K11	Transceiver reference CLK 1 input P
FMC3_GBT0_0_M2C_C_N	MGTREFCLK0N_233	D10	Transceiver reference CLK 0 input N
FMC3_GBT0_0_M2C_C_P	MGTREFCLK0P_233	D11	Transceiver reference CLK 0 input P
FMC3_GBTCLK2_M2C_C_N	MGTREFCLK0N_232	H10	Transceiver reference CLK 0 input N
FMC3_GBTCLK2_M2C_C_P	MGTREFCLK0P_232	H11	Transceiver reference CLK 0 input P
FMC3_GBTCLK3_M2C_C_N	MGTREFCLK0N_231	M10	Transceiver reference CLK 0 input N
FMC3_GBTCLK3_M2C_C_P	MGTREFCLK0P_231	M11	Transceiver reference CLK 0 input P
FMC3_H_PRSNT_M2C_B	IO_T3U_N12_74	D26	Reset PIN
FMC3_L_PRSNT_M2C_B	IO_T3U_N12_71	C28	Reset PIN
FMC3_PG_C2M	IO_T2U_N12_74	F25	Power statues PIN
FMC3_PG_M2C	IO_T2U_N12_71	E26	Power statues PIN
FMC3_REFCLK_C2M_N	IO_L8N_T1L_N3_AD5N_71	K28	Reference CLK 1 output N
FMC3_REFCLK_C2M_P	IO_L8P_T1L_N2_AD5P_71	L28	Reference CLK 1 output P
FMC3_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_71	H28	Reference CLK 1 input N
FMC3_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_71	H27	Reference CLK 1 input P
FMC3_SYNC_C2M_N	IO_L7N_T1L_N1_QBC_AD13N_71	L29	C2M SYNC output N
FMC3_SYNC_C2M_P	IO_L7P_T1L_N0_QBC_AD13P_71	M29	C2M SYNC output P

FMC3_SYNC_M2C_N	IO_L10N_T1U_N7_QBC_AD4N_71	K27	M2C SYNC input N
FMC3_SYNC_M2C_P	IO_L10P_T1U_N6_QBC_AD4P_71	K26	M2C SYNC input P
FMC3_GBT0_1_M2C_C_N	MGTREFCLK0N_230	T10	Transceiver reference CLK 0 input N
FMC3_GBT0_1_M2C_C_P	MGTREFCLK0P_230	T11	Transceiver reference CLK 0 input P

Table 8: FMC3 + (J7) Connector PIN assignment

7.7 FMC4 + (J23) Schematic Diagram

The port provides 34 LA differential pairs and 2 clock pairs, which are connected to BANK71 and BANK72 of the FPGA. The default I/O voltage standard for these signals is 1.8V. Additionally, 16 high-speed GTY transceiver channels are connected to the I/O of the FPGA's BANK225 through BANK228.

Figure 12 shows the schematic diagram of the connection between the FPGA and the FMC4+ connector.

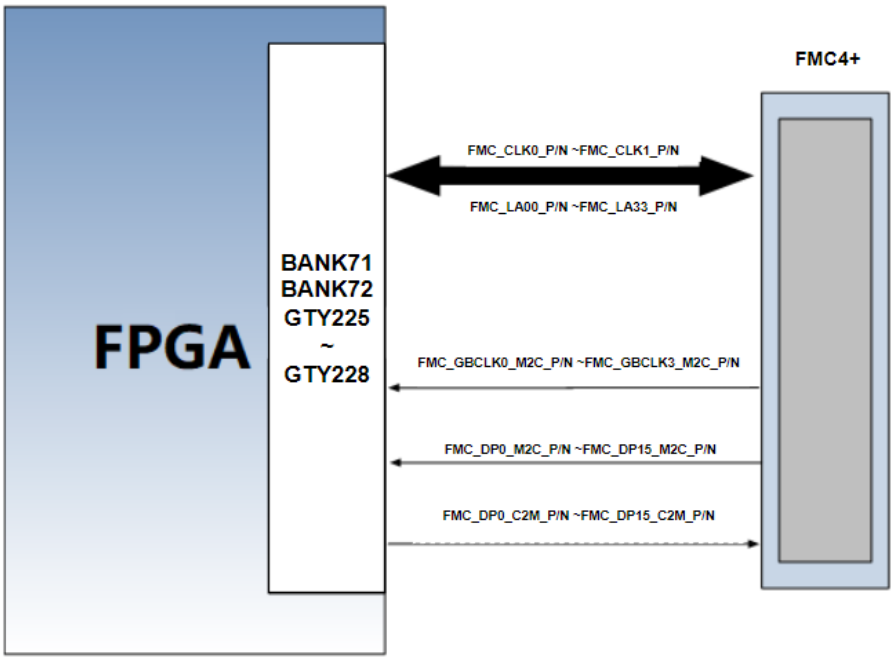


Figure 12: FMC4 + (J23) schematic diagram

7.8 FMC4 + (J23) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC4_CLK0_N	IO_L12N_T1U_N11_GC_73	J19	FMC Channel 0 Input Reference CLK N
FMC4_CLK0_P	IO_L12P_T1U_N10_GC_73	J20	FMC Channel 0 Input Reference CLK P
FMC4_CLK1_N	IO_L12N_T1U_N11_GC_72	J15	FMC Channel 1 Input Reference CLK N
FMC4_CLK1_P	IO_L12P_T1U_N10_GC_72	J16	FMC Channel 1 Input Reference CLK P
FMC4_LA00_CC_N	IO_L14N_T2L_N3_GC_73	G19	FMC LA Channel 0 Data (CLK) N
FMC4_LA00_CC_P	IO_L14P_T2L_N2_GC_73	G20	FMC LA Channel 0 Data (CLK) P
FMC4_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_73	H18	FMC LA Channel 1 Data (CLK) N
FMC4_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_73	H19	FMC LA Channel 1 Data (CLK) P
FMC4_LA02_N	IO_L17N_T2U_N9_AD10N_73	E20	FMC LA Channel 2 Data N
FMC4_LA02_P	IO_L17P_T2U_N8_AD10P_73	E21	FMC LA Channel 2 Data P
FMC4_LA03_N	IO_L10N_T1U_N7_QBC_AD4N_73	H21	FMC LA Channel 3 Data N
FMC4_LA03_P	IO_L10P_T1U_N6_QBC_AD4P_73	J21	FMC LA Channel 3 Data P
FMC4_LA04_N	IO_L15N_T2L_N5_AD11N_73	F19	FMC LA Channel 4 Data N
FMC4_LA04_P	IO_L15P_T2L_N4_AD11P_73	F20	FMC LA Channel 4 Data P
FMC4_LA05_N	IO_L16N_T2U_N7_QBC_AD3N_73	E17	FMC LA Channel 5 Data N
FMC4_LA05_P	IO_L16P_T2U_N6_QBC_AD3P_73	E18	FMC LA Channel 5 Data P
FMC4_LA06_N	IO_L21N_T3L_N5_AD8N_73	B21	FMC LA Channel 6 Data N
FMC4_LA06_P	IO_L21P_T3L_N4_AD8P_73	C21	FMC LA Channel 6 Data P
FMC4_LA07_N	IO_L23N_T3U_N9_73	A19	FMC LA Channel 7 Data N
FMC4_LA07_P	IO_L23P_T3U_N8_73	B19	FMC LA Channel 7 Data P
FMC4_LA08_N	IO_L20N_T3L_N3_AD1N_73	D20	FMC LA Channel 8 Data N
FMC4_LA08_P	IO_L20P_T3L_N2_AD1P_73	D21	FMC LA Channel 8 Data P
FMC4_LA09_N	IO_L22N_T3U_N7_DBC_AD0N_73	C18	FMC LA Channel 9 Data N
FMC4_LA09_P	IO_L22P_T3U_N6_DBC_AD0P_73	D18	FMC LA Channel 9 Data P
FMC4_LA10_N	IO_L18N_T2U_N11_AD2N_73	F17	FMC LA Channel 10 Data N
FMC4_LA10_P	IO_L18P_T2U_N10_AD2P_73	F18	FMC LA Channel 10 Data P
FMC4_LA11_N	IO_L5N_T0U_N9_AD14N_73	P20	FMC LA Channel 11 Data N
FMC4_LA11_P	IO_L5P_T0U_N8_AD14P_73	R20	FMC LA Channel 11 Data P
FMC4_LA12_N	IO_L19N_T3L_N1_DBC_AD9N_73	C19	FMC LA Channel 12 Data N
FMC4_LA12_P	IO_L19P_T3L_N0_DBC_AD9P_73	D19	FMC LA Channel 12 Data P
FMC4_LA13_N	IO_L2N_T0L_N3_73	N18	FMC LA Channel 13 Data N

FMC4_LA13_P	IO_L2P_T0L_N2_73	P18	FMC LA Channel 13 Data P
FMC4_LA14_N	IO_L1N_T0L_N1_DBC_73	M17	FMC LA Channel 14 Data N
FMC4_LA14_P	IO_L1P_T0L_N0_DBC_73	N17	FMC LA Channel 14 Data P
FMC4_LA15_N	IO_L3N_T0L_N5_AD15N_73	M19	FMC LA Channel 15 Data N
FMC4_LA15_P	IO_L3P_T0L_N4_AD15P_73	M20	FMC LA Channel 15 Data P
FMC4_LA16_N	IO_L4N_T0U_N7_DBC_AD7N_73	N19	FMC LA Channel 16 Data N
FMC4_LA16_P	IO_L4P_T0U_N6_DBC_AD7P_73	P19	FMC LA Channel 16 Data P
FMC4_LA17_CC_N	IO_L14N_T2L_N3_GC_72	F15	FMC LA Channel 17 Data (CLK) N
FMC4_LA17_CC_P	IO_L14P_T2L_N2_GC_72	G15	FMC LA Channel 17 Data (CLK) P
FMC4_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_72	F14	FMC LA Channel 18 Data (CLK) N
FMC4_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_72	G14	FMC LA Channel 18 Data (CLK) P
FMC4_LA19_N	IO_L11N_T1U_N9_GC_72	H14	FMC LA Channel 19 Data N
FMC4_LA19_P	IO_L11P_T1U_N8_GC_72	J14	FMC LA Channel 19 Data P
FMC4_LA20_N	IO_L16N_T2U_N7_QBC_AD3N_72	G16	FMC LA Channel 20 Data N
FMC4_LA20_P	IO_L16P_T2U_N6_QBC_AD3P_72	G17	FMC LA Channel 20 Data P
FMC4_LA21_N	IO_L5N_T0U_N9_AD14N_72	L14	FMC LA Channel 21 Data N
FMC4_LA21_P	IO_L5P_T0U_N8_AD14P_72	M14	FMC LA Channel 21 Data P
FMC4_LA22_N	IO_L3N_T0L_N5_AD15N_72	P15	FMC LA Channel 22 Data N
FMC4_LA22_P	IO_L3P_T0L_N4_AD15P_72	R15	FMC LA Channel 22 Data P
FMC4_LA23_N	IO_L4N_T0U_N7_DBC_AD7N_72	P16	FMC LA Channel 23 Data N
FMC4_LA23_P	IO_L4P_T0U_N6_DBC_AD7P_72	R16	FMC LA Channel 23 Data P
FMC4_LA24_N	IO_L17N_T2U_N9_AD10N_72	D15	FMC LA Channel 24 Data N
FMC4_LA24_P	IO_L17P_T2U_N8_AD10P_72	E15	FMC LA Channel 24 Data P
FMC4_LA25_N	IO_L9N_T1L_N5_AD12N_72	H13	FMC LA Channel 25 Data N
FMC4_LA25_P	IO_L9P_T1L_N4_AD12P_72	J13	FMC LA Channel 25 Data P
FMC4_LA26_N	IO_L1N_T0L_N1_DBC_72	N13	FMC LA Channel 26 Data N
FMC4_LA26_P	IO_L1P_T0L_N0_DBC_72	P13	FMC LA Channel 26 Data P
FMC4_LA27_N	IO_L2N_T0L_N3_72	N14	FMC LA Channel 27 Data N
FMC4_LA27_P	IO_L2P_T0L_N2_72	P14	FMC LA Channel 27 Data P
FMC4_LA28_N	IO_L15N_T2L_N5_AD11N_72	E13	FMC LA Channel 28 Data N
FMC4_LA28_P	IO_L15P_T2L_N4_AD11P_72	F13	FMC LA Channel 28 Data P
FMC4_LA29_N	IO_L19N_T3L_N1_DBC_AD9N_72	C13	FMC LA Channel 29 Data N
FMC4_LA29_P	IO_L19P_T3L_N0_DBC_AD9P_72	D13	FMC LA Channel 29 Data P
FMC4_LA30_N	IO_L21N_T3L_N5_AD8N_72	A13	FMC LA Channel 30 Data N
FMC4_LA30_P	IO_L21P_T3L_N4_AD8P_72	A14	FMC LA Channel 30 Data P
FMC4_LA31_N	IO_L20N_T3L_N3_AD1N_72	B14	FMC LA Channel 31 Data N
FMC4_LA31_P	IO_L20P_T3L_N2_AD1P_72	C14	FMC LA Channel 31 Data P
FMC4_LA32_N	IO_L23N_T3U_N9_72	B16	FMC LA Channel 32 Data N

FMC4_LA32_P	IO_L23P_T3U_N8_72	C16	FMC LA Channel 32 Data P
FMC4_LA33_N	IO_L22N_T3U_N7_DBC_AD0N_72	A15	FMC LA Channel 33 Data N
FMC4_LA33_P	IO_L22P_T3U_N6_DBC_AD0P_72	B15	FMC LA Channel 33 Data P
FMC4_SCL	IO_L24P_T3U_N10_73	B20	FMC I2C Bus CLK
FMC4_SDA	IO_T3U_N12_73	A18	FMC I2C Bus Data
FMC4_DP0_M2C_P	MGTYRXP2_228	AC4	Transceiver Data 0 Input P
FMC4_DP0_M2C_N	MGTYRXN2_228	AC3	Transceiver Data 0 Input N
FMC4_DP1_M2C_P	MGTYRXP0_228	AE4	Transceiver Data 1 Input P
FMC4_DP1_M2C_N	MGTYRXN0_228	AE3	Transceiver Data 1 Input N
FMC4_DP2_M2C_P	MGTYRXP1_228	AD2	Transceiver Data 2 Input P
FMC4_DP2_M2C_N	MGTYRXN1_228	AD1	Transceiver Data 2 Input N
FMC4_DP3_M2C_P	MGTYRXP3_228	AB2	Transceiver Data 3 Input P
FMC4_DP3_M2C_N	MGTYRXN3_228	AB1	Transceiver Data 3 Input N
FMC4_DP4_M2C_P	MGTYRXP2_225	AR4	Transceiver Data 4 Input P
FMC4_DP4_M2C_N	MGTYRXN2_225	AR3	Transceiver Data 4 Input N
FMC4_DP5_M2C_P	MGTYRXP1_225	AT2	Transceiver Data 5 Input P
FMC4_DP5_M2C_N	MGTYRXN1_225	AT1	Transceiver Data 5 Input N
FMC4_DP6_M2C_P	MGTYRXP0_225	AU4	Transceiver Data 6 Input P
FMC4_DP6_M2C_N	MGTYRXN0_225	AU3	Transceiver Data 6 Input N
FMC4_DP7_M2C_P	MGTYRXP3_225	AP2	Transceiver Data 7 Input P
FMC4_DP7_M2C_N	MGTYRXN3_225	AP1	Transceiver Data 7 Input N
FMC4_DP8_M2C_P	MGTYRXP1_227	AH2	Transceiver Data 8 Input P
FMC4_DP8_M2C_N	MGTYRXN1_227	AH1	Transceiver Data 8 Input N
FMC4_DP9_M2C_P	MGTYRXP3_227	AF2	Transceiver Data 9 Input P
FMC4_DP9_M2C_N	MGTYRXN3_227	AF1	Transceiver Data 9 Input N
FMC4_DP10_M2C_P	MGTYRXP2_227	AG4	Transceiver Data 10 Input P
FMC4_DP10_M2C_N	MGTYRXN2_227	AG3	Transceiver Data 10 Input N
FMC4_DP11_M2C_P	MGTYRXP0_227	AJ4	Transceiver Data 11 Input P
FMC4_DP11_M2C_N	MGTYRXN0_227	AJ3	Transceiver Data 11 Input N
FMC4_DP12_M2C_P	MGTYRXP3_226	AK2	Transceiver Data 12 Input P
FMC4_DP12_M2C_N	MGTYRXN3_226	AK1	Transceiver Data 12 Input N
FMC4_DP13_M2C_P	MGTYRXP2_226	AL4	Transceiver Data 13 Input P

FMC4_DP13_M2C_N	MGTYRXN2_226	AL3	Transceiver Data 13 Input N
FMC4_DP14_M2C_P	MGTYRXP1_226	AM2	Transceiver Data 14 Input P
FMC4_DP14_M2C_N	MGTYRXN1_226	AM1	Transceiver Data 14 Input N
FMC4_DP15_M2C_P	MGTYRXP0_226	AN4	Transceiver Data 15 Input P
FMC4_DP15_M2C_N	MGTYRXN0_226	AN3	Transceiver Data 15 Input N
FMC4_DP0_C2M_P	MGTYTXP2_228	AC9	Transceiver Data 0 Output P
FMC4_DP0_C2M_N	MGTYTXN2_228	AC8	Transceiver Data 0 Output N
FMC4_DP1_C2M_P	MGTYTXP0_228	AE9	Transceiver Data 1 Output P
FMC4_DP1_C2M_N	MGTYTXN0_228	AE8	Transceiver Data 1 Output N
FMC4_DP2_C2M_P	MGTYTXP1_228	AD7	Transceiver Data 2 Output P
FMC4_DP2_C2M_N	MGTYTXN1_228	AD6	Transceiver Data 2 Output N
FMC4_DP3_C2M_P	MGTYTXP3_228	AB7	Transceiver Data 3 Output P
FMC4_DP3_C2M_N	MGTYTXN3_228	AB6	Transceiver Data 3 Output N
FMC4_DP4_C2M_P	MGTYTXP2_225	AR9	Transceiver Data 4 Output P
FMC4_DP4_C2M_N	MGTYTXN2_225	AR8	Transceiver Data 4 Output N
FMC4_DP5_C2M_P	MGTYTXP1_225	AT7	Transceiver Data 5 Output P
FMC4_DP5_C2M_N	MGTYTXN1_225	AT6	Transceiver Data 5 Output N
FMC4_DP6_C2M_P	MGTYTXP0_225	AU9	Transceiver Data 6 Output P
FMC4_DP6_C2M_N	MGTYTXN0_225	AU8	Transceiver Data 6 Output N
FMC4_DP7_C2M_P	MGTYTXP3_225	AP7	Transceiver Data 7 Output P
FMC4_DP7_C2M_N	MGTYTXN3_225	AP6	Transceiver Data 7 Output N
FMC4_DP8_C2M_P	MGTYTXP1_227	AH7	Transceiver Data 8 Output P
FMC4_DP8_C2M_N	MGTYTXN1_227	AH6	Transceiver Data 8 Output N
FMC4_DP9_C2M_P	MGTYTXP3_227	AF7	Transceiver Data 9 Output P
FMC4_DP9_C2M_N	MGTYTXN3_227	AF6	Transceiver Data 9 Output N
FMC4_DP10_C2M_P	MGTYTXP2_227	AG9	Transceiver Data 10 Output P
FMC4_DP10_C2M_N	MGTYTXN2_227	AG8	Transceiver Data 10 Output N
FMC4_DP11_C2M_P	MGTYTXP0_227	AJ9	Transceiver Data 11 Output P
FMC4_DP11_C2M_N	MGTYTXN0_227	AJ8	Transceiver Data 11 Output N
FMC4_DP12_C2M_P	MGTYTXP3_226	AK7	Transceiver Data 12 Output P
FMC4_DP12_C2M_N	MGTYTXN3_226	AK6	Transceiver Data 12 Output N
FMC4_DP13_C2M_P	MGTYTXP2_226	AL9	Transceiver Data 13 Output P

FMC4_DP13_C2M_N	MGTYTXN2_226	AL8	Transceiver Data 13 Output N
FMC4_DP14_C2M_P	MGTYTXP1_226	AM7	Transceiver Data 14 Output P
FMC4_DP14_C2M_N	MGTYTXN1_226	AM6	Transceiver Data 14 Output N
FMC4_DP15_C2M_P	MGTYTXP0_226	AN9	Transceiver Data 15 Output P
FMC4_DP15_C2M_N	MGTYTXN0_226	AN8	Transceiver Data 15 Output N
FMC4_GBT1_0_M2C_C_N	MGTREFCLK1N_226	AK10	Transceiver Reference CLK 1 Input N
FMC4_GBT1_0_M2C_C_P	MGTREFCLK1P_226	AK11	Transceiver Reference CLK 1 Input P
FMC4_GBT1_1_M2C_C_N	MGTREFCLK1N_225	AP10	Transceiver Reference CLK 1 Input N
FMC4_GBT1_1_M2C_C_P	MGTREFCLK1P_225	AP11	Transceiver Reference CLK 1 Input P
FMC4_GBT1_2_M2C_C_N	MGTREFCLK1N_227	AF10	Transceiver Reference CLK 1 Input N
FMC4_GBT1_2_M2C_C_P	MGTREFCLK1P_227	AF11	Transceiver Reference CLK 1 Input P
FMC4_GBT1_3_M2C_C_N	MGTREFCLK1N_228	AB10	Transceiver Reference CLK 1 Input N
FMC4_GBT1_3_M2C_C_P	MGTREFCLK1P_228	AB11	Transceiver Reference CLK 1 Input P
FMC4_GBT0_0_M2C_C_N	MGTREFCLK0N_228	AD10	Transceiver Reference CLK 0 Input N
FMC4_GBT0_0_M2C_C_P	MGTREFCLK0P_228	AD11	Transceiver Reference CLK 0 Input P
FMC4_GBTCLK2_M2C_C_N	MGTREFCLK0N_227	AH10	Transceiver Reference CLK 0 Input N
FMC4_GBTCLK2_M2C_C_P	MGTREFCLK0P_227	AH11	Transceiver Reference CLK 0 Input P
FMC4_GBTCLK3_M2C_C_N	MGTREFCLK0N_226	AM10	Transceiver Reference CLK 0 Input N
FMC4_GBTCLK3_M2C_C_P	MGTREFCLK0P_226	AM11	Transceiver Reference CLK 0 Input P
FMC4_H_PRSNT_M2C_B	IO_L6N_T0U_N11_AD6N_73	M21	Reset Pin
FMC4_L_PRSNT_M2C_B	IO_L24N_T3U_N11_73	A20	Reset Pin
FMC4_PG_C2M	IO_T2U_N12_73	G21	Power Status Pin
FMC4_PG_M2C	IO_T1U_N12_73	K21	Power Status Pin
FMC4_REFCLK_C2M_N	IO_L8N_T1L_N3_AD5N_73	L18	Reference CLK 1 Output N
FMC4_REFCLK_C2M_P	IO_L8P_T1L_N2_AD5P_73	L19	Reference CLK 1 Output P
FMC4_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_73	J18	Reference CLK 1 Input N
FMC4_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_73	K18	Reference CLK 1 Input P
FMC4_SYNC_C2M_N	IO_L7N_T1L_N1_QBC_AD13N_73	K17	C2M SYNC Output N
FMC4_SYNC_C2M_P	IO_L7P_T1L_N0_QBC_AD13P_73	L17	C2M SYNC Output P
FMC4_SYNC_M2C_N	IO_L9N_T1L_N5_AD12N_73	K20	M2C SYNC Input N
FMC4_SYNC_M2C_P	IO_L9P_T1L_N4_AD12P_73	L20	M2C SYNC Input P
FMC4_GBT0_1_M2C_C_N	MGTREFCLK0N_225	AT10	Transceiver Reference CLK 0 Input N

FMC4_GBT0_1_M2C_C_P	MGTREFCLK0P_225	AT11	Transceiver Reference CLK 0 Input P

Table 9: FMC4 + (J23) Connector PIN assignment

8 USB Serial Converter

8.1 Schematic Diagram

The AXVU13F expansion board is equipped with a USB-to-UART interface for system debugging. The interface utilizes a Silicon Labs **CP2102GM** USB-to-UART bridge chip and features a Mini-USB connector. Using a single USB cable, it can be connected to a PC's USB port to provide both standalone power to the core board and serial data communication.

Figure 13 shows the schematic diagram of the USB UART circuit design.

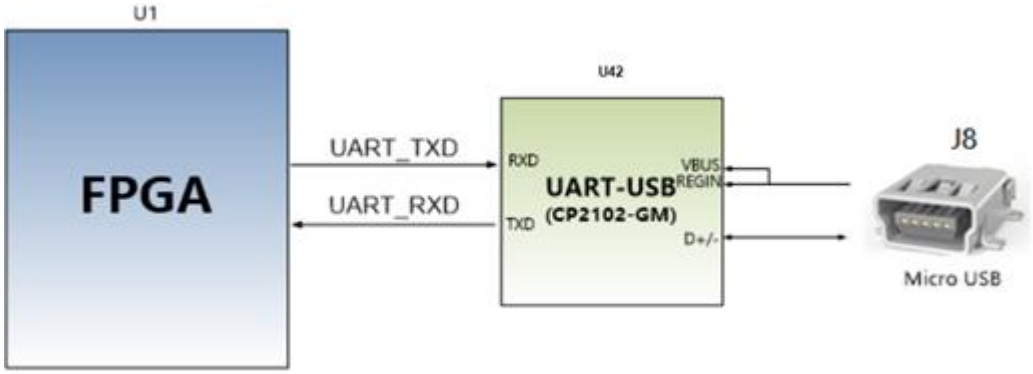


Figure 13: USB serial converter schematic diagram

8.2 USB Serial Converter PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
UART_RX_LS	IO_L5N_T0U_N9_AD14N_A23_65	BF25	UART data input
UART_TX_LS	IO_L5P_T0U_N8_AD14P_A22_65	BE25	UART data output

Table 10: USB Serial Converter PIN Assignment

9 Gigabit Ethernet Interface

9.1 PHY Chip Definition & FPGA Connection

The board provides network communication services via a JL21221D Ethernet PHY chip, which is connected to the I/O interface of the FPGA.

The JL21221D chip supports 10/100/1000 Mbps network transmission rates and communicates with the FPGA through an RGMII interface. The chip's features include Auto MDI/MDIX, auto-negotiation for various speeds, Master/Slave auto-negotiation, and support for PHY register management via the MDIO bus.

Upon power-on, the JL21221D detects the logic levels of specific I/O pins to determine its operating mode. Table 2-8-1 describes the default configuration settings of the GPHY chip after power-on.

Table 11 shows the PHY chip default configuration.

Pin configuration	Description	Configuration
RXD3_ADR0 RXC_ADR1 RXCTL_ADR2	PHY Address in MDIO/MDC mode	PHY Address is set to 001
RXD1_TXDLY	2ns delay on the TX clock	Delay Enabled
RXD0_RXDLY	2ns delay on the RX clock	Delay Enabled

Table 11: PHY Chip Default Configuration

9.2 Connectivity

When connected to Gigabit Ethernet: Data transmission between the FPGA and the JL2121 PHY chip occurs via the RGMII bus. The transmission clock is 125 MHz, and data is sampled on both the rising and falling edges of the clock.

When connected to Fast Ethernet (100Mbps) : Data transmission between the FPGA and the JL2121 PHY chip occurs via the RMII bus. The transmission clock is 25 MHz, and data is sampled on both the rising and falling edges of the clock.

Figure 14 shows the schematic diagram of the connection between the FPGA and the Ethernet PHY chip.

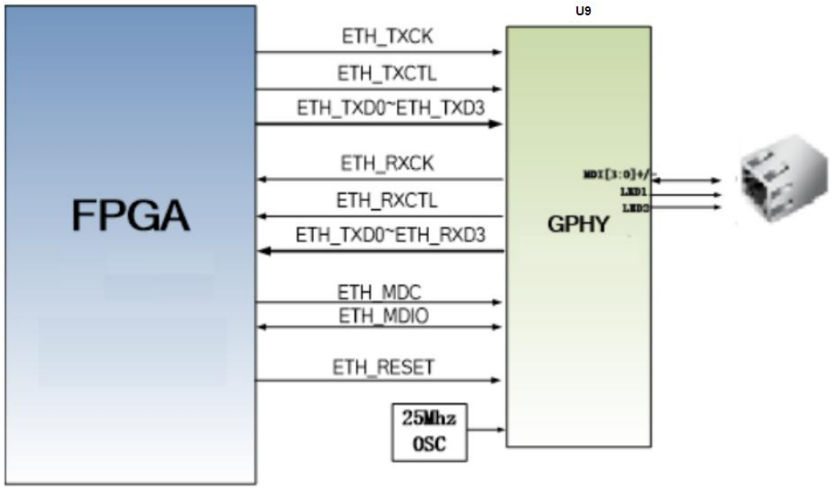


Figure 14: Gigabit Ethernet Interface Connection Schematic

Figure 15 shows the photo of the actual Ethernet PHY chip.

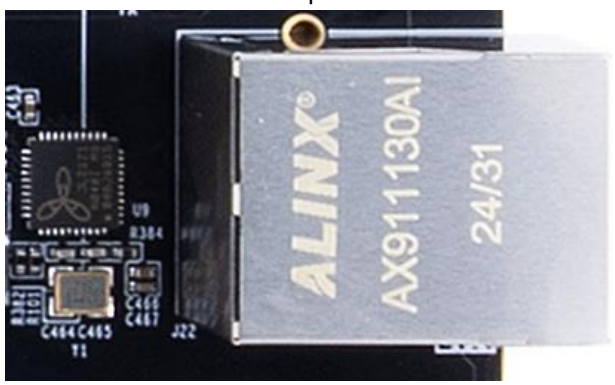


Figure 15: Photo of the Ethernet PHY Chip

The FPGA pin assignment for the Ethernet PHY is as follows:

Signal Name	FPGA PIN Name	Remark
ETH_MDC	BE12	MDIO Management CLK
ETH_MDIO	BF12	MDIO Management data
ETH_RESET	BD11	PHY Chip Reset
ETH_RXCK	BA9	RGMII Receive CLK
ETH_RXCTL	BA8	Receive data valid
ETH_RXD0	BD8	Receive data Bit0
ETH_RXD1	BD9	Receive data Bit1
ETH_RXD2	BE8	Receive data Bit2
ETH_RXD3	BC11	Receive data Bit3
ETH_TXCK	BF9	RGMII transmit CLK
ETH_TXCTL	BE10	Transmit enable
ETH_TXD0	BC12	Transmit data Bit0

ETH_TXD1	BF10	Transmit data Bit1
ETH_TXD2	BE11	Transmit data Bit2
ETH_TXD3	BF8	Transmit data Bit3

Table 12: Ethernet PHY FPGA Pin Configuration

10 Optical Interface

10.1 Optical Interface Schematic

The board features one QSFP28 optical interface, allowing users to insert a QSFP optical module for data communication (purchase separately). The interface connects to 4 RX/TX pairs of the GTY transceivers in BANK229, providing four independent transmit and receive channels. Each channel can operate at 25 Gbps over 100 meters of OM4 Multi-Mode Fiber (MMF), for an aggregate data rate of 100 Gbps. The two reference clocks are supplied by a crystal oscillator and an SC6301 clock chip.

The schematic diagram of the FPGA and optical interface design is shown in the figure below.

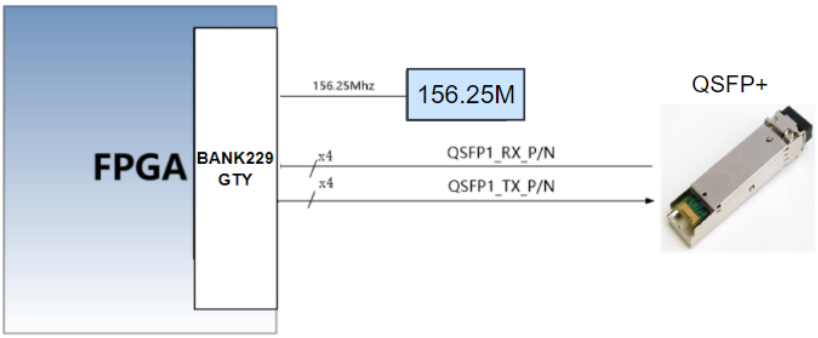


Figure 16: Optic Schematic Diagram

The FPGA pin assignment for the optical fiber interface is as follows:

Signal Name	FPGA PIN Name	FPGA PIN number	Remark
QSFP1_RX1_N	MGTYRXN0_229	AA3	Optical module 1 data receive N 1
QSFP1_RX1_P	MGTYRXP0_229	AA4	Optical module 1 data receive P 1
QSFP1_RX2_N	MGTYRXN1_229	Y1	Optical module 1 data receive N 2
QSFP1_RX2_P	MGTYRXP1_229	Y2	Optical module 1 data receive P 2
QSFP1_RX3_N	MGTYRXN2_229	W3	Optical module 1 data receive N 3
QSFP1_RX3_P	MGTYRXP2_229	W4	Optical module 1 data receive P 3
QSFP1_RX4_N	MGTYRXN3_229	V1	Optical module 1 data receive N 4
QSFP1_RX4_P	MGTYRXP3_229	V2	Optical module 1 data receive P 4
QSFP1_TX1_N	MGTYTXN0_229	AA8	Optical module 1 data transmit N 1
QSFP1_TX1_P	MGTYTXP0_229	AA9	Optical module 1 data transmit P 1
QSFP1_TX2_N	MGTYTXN1_229	Y6	Optical module 1 data transmit N 2

QSFP1_TX2_P	MGTYTXP1_229	Y7	Optical module 1 data transmit P 2
QSFP1_TX3_N	MGTYTXN2_229	W8	Optical module 1 data transmit N 3
QSFP1_TX3_P	MGTYTXP2_229	W9	Optical module 1 data transmit P 3
QSFP1_TX4_N	MGTYTXN3_229	V6	Optical module 1 data transmit N 4
QSFP1_TX4_P	MGTYTXP3_229	V7	Optical module 1 data transmit P 4
MGT229_CLK0_N	MGTREFCLK0N_229	Y10	BANK229 reference CLK 0 N
MGT229_CLK0_P	MGTREFCLK0P_229	Y11	BANK229 reference CLK 0 P
MGT229_CLK1_N	MGTREFCLK1N_229	V10	BANK229 reference CLK 1 N
MGT229_CLK1_P	MGTREFCLK1P_229	V11	BANK229 reference CLK 1 P
QSFP1_INTL	IO_L6N_T0U_N11_AD6N_72	M16	Interrupt signal, Active low
QSFP1_LPMODE	IO_L8P_T1L_N2_AD5P_72	K16	Optical module LP mode
QSFP1_MODPRSL	IO_L6P_T0U_N10_AD6P_72	N16	Optical module presence detects, active low
QSFP1_MODSELL	IO_T1U_N12_72	L15	Mode select, I2C active low
QSFP1_RESETL	IO_L8N_T1L_N3_AD5N_72	K15	Reset signal, active low
QSFP1_SCL	IO_L7P_T1L_N0_QBC_AD13P_72	L13	Optical module I2C CLK
QSFP1_SDA	IO_L10N_T1U_N7_QBC_AD4N_72	H16	Optical module I2C data

Table 13: Optic Interface Pin Configuration

11 IO Expansion Interface

11.1 Expansion Interface Schematic

The AXVU13F features a 14-pin IO expansion interface with a 2.54mm pitch, exposing 6 IO signals. By default, these are not soldered. The pin definitions are as follows:

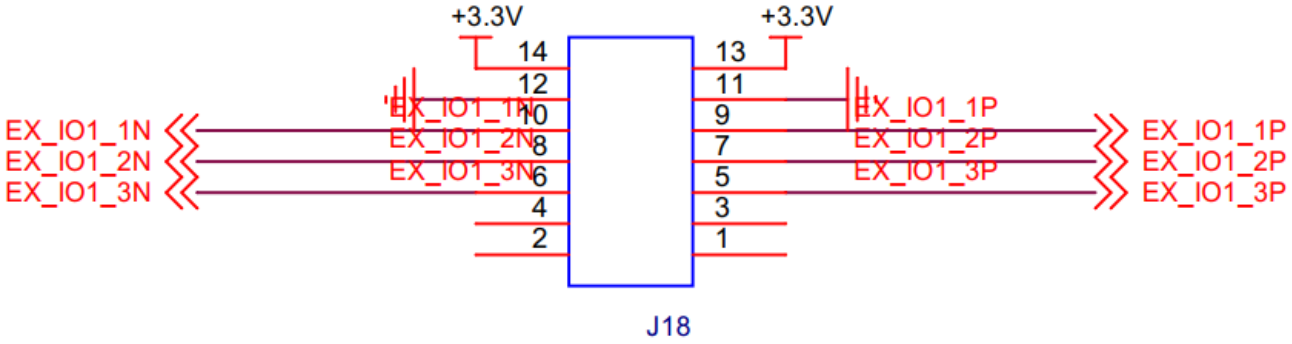


Figure 17: Expansion Interface Schematic

11.2 Expansion Interface PIN Assignment

Expansion port PIN	Signal Name	PIN #	Comments
1	NC	-	-
2	NC	-	-
3	NC	-	-
4	NC	-	-
5	EX_IO1_3P	BE7	Data
6	EX_IO1_3N	BF7	Data
7	EX_IO1_2P	BC8	Data
8	EX_IO1_2N	BC7	Data
9	EX_IO1_1P	BA7	Data
10	EX_IO1_1N	BB7	Data
11	GND	-	GND
12	GND	-	GND
13	+3.3V	-	3.3V
14	+3.3V	-	3.3V

Table 14: Expansion Interface PIN Assignment

12 SMA Interface

The board is equipped with two SMA interfaces; one can serve as a differential input, and the other can serve as a differential output. These are connected to the HPIO pins of the FPGA and can be used for the verification of customer differential signal input and output.

The FPGA pin assignments are as follows:

Signal Name	PIN Name	PIN #	Comments
CLKOUT_P	IO_L8P_T1L_N2_AD5P_68	BB11	SMA data receive positive
CLKOUT_N	IO_L8N_T1L_N3_AD5N_68	BB10	SMA data receive negative
CLKIN_P	IO_L11P_T1U_N8_GC_68	BB9	SMA data input positive
CLKIN_N	IO_L11N_T1U_N9_GC_68	BC9	SMA data input negative

Table 15: SMA Interface PIN Assignment

13 Keys & LED

13.1 Schematics

The AXVU13F baseboard has a total of 8 light-emitting diodes (LEDs):

- 1x Power Indicator: Lights up when the development board is powered on.
- 1x Configuration DONE Indicator
- 2x Serial Port Communication Indicators
- 4x User LEDs: These are connected to the FPGA's I/O pins and can be controlled through user programming. The LEDs are active-high; they light up when the corresponding I/O voltage is high and turn off when the voltage is low.

Additionally, there is one user push-button on the board. The button is active-low; its default signal level is high, and the level goes low when the button is pressed.
The schematic diagram for the hardware connection of the user LEDs and the push-button is shown in Figure 18 below:

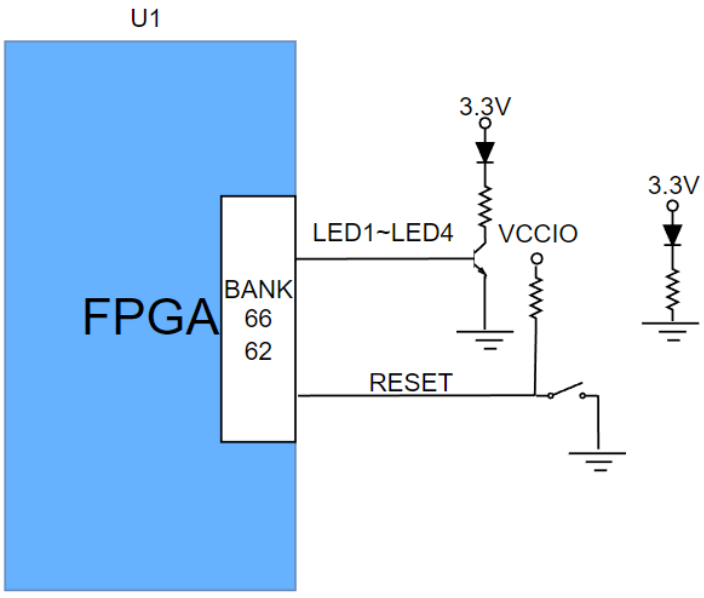


Figure 18: Buttons and LEDs schematic diagram

13.2 User Keys & LED pin assessment:

Signal Name	FPGA PIN Name	PIN #	Comments
RESET	IO_T1U_N12_62	BF35	User button
LED1	IO_L7N_T1L_N1_QBC_AD13N_66	BA17	User LED1
LED2	IO_L8N_T1L_N3_AD5N_66	BA18	User LED2
LED3	IO_L6N_T0U_N11_AD6N_66	BC18	User LED3
LED4	IO_L6P_T0U_N10_AD6P_66	BB19	User LED4

Table 16: Buttons and LEDs PIN assignment

14 JTAG Debug Port

A 14-pin JTAG interface is reserved on the AXVU13F base board for downloading FPGA programs or programming them into FLASH. To prevent damage to the FPGA chip due to hot swapping, we have added protection diodes to the JTAG signals to ensure that the voltage remains within the acceptable range for the FPGA, avoiding chip damage.

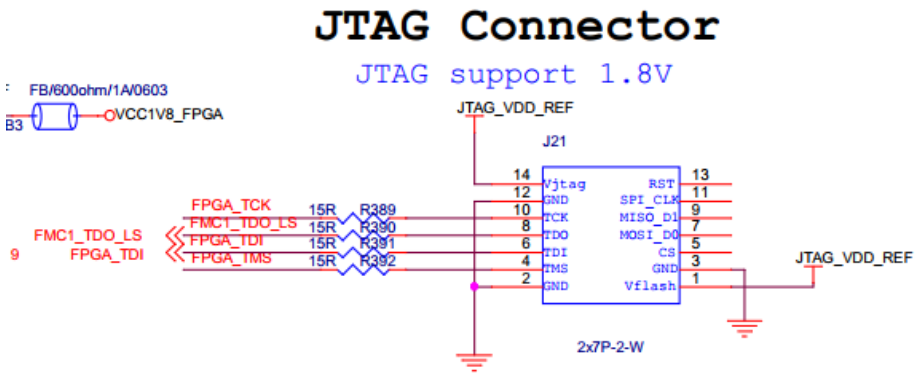


Figure 19: JTAG debug port schematic

15 Power

15.1 Power Design Schematic Diagram

The development board's input voltage is 12V DC, which can be supplied via an external +12V power source through the 8-pin J10 interface. To prevent damage, please use the power supply unit provided with the board and do not use power supplies with other specifications.

The 12V input is used by a DC-DC module to generate the main FPGA core power, with an output current of up to 150A to meet the core's current requirements. The +12V supply also powers other DC-DC converters: the SGM61163 generates VCCAUX, while the IS6608A generates the MGTAVCC and MGTAVTT supplies for the FPGA's auxiliary functions and high-speed transceivers.

The DC-DC converters ETA1471, SGM61163, and IS66066 are used to generate the +1.2V, VCC1V8_FPGA, and +3.3V rails, which power the DDR4 memory, FPGA banks, and other peripherals. Additionally, the +3.3V rail powers two ETA5060 LDO chips to generate the +1.8V auxiliary supply for the high-speed transceivers and the FPGA's ADC. The VTT and +2.5V supplies for the DDR4 memory are generated by the TPS51200 and ETA5050.

Furthermore, the IS66066 also provides power to the three FMC+ interfaces and other peripherals.

The power design block diagram on the board is as follows:

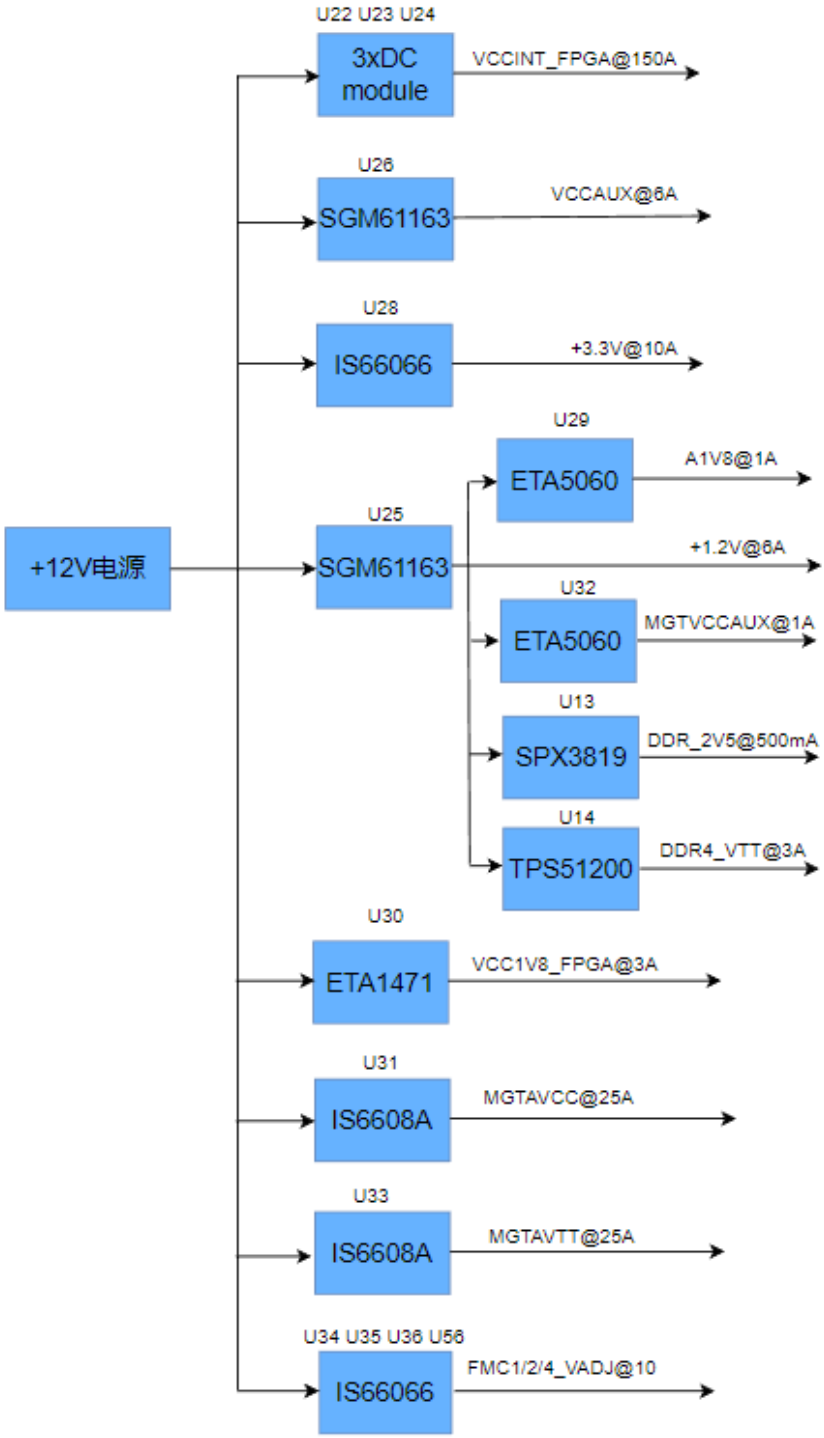


Figure20: Power supply interface schematic diagram

15.2 Power Distribution Functions Table

Power Supply	Function
VCCINT_FPGA@150A	FPGA Core power supply
VCCAUX@6A	FPGA Auxiliary power supply
MGTVCCAUX@1A	GTY support power
MGTAVCC@25A	FPGA GTY power supply

MGTAVTT@25A	FPGA GTY power supply
VCC1V8_FPGA@3A	FPGA BANK Voltage and Peripherals
+1.2V@6A	SODIMM & BANK voltage
FMC1_VADJ@10A	FMC1+ Regulation voltage
FMC2_VADJ@10A	FMC2+ Regulation voltage
FMC3_VADJ@10A	FMC3+ Regulation voltage
FMC3_VADJ@10A	FMC4+ Regulation voltage
FMC4_VADJ@10A	FPGA Peripherals voltage
+3.3V@10A	DDR4 VTT voltage
DDR4_VTT@3A	DDR4 supply voltage

Table 17: Power distribution functions table

16 Structural Dimensional

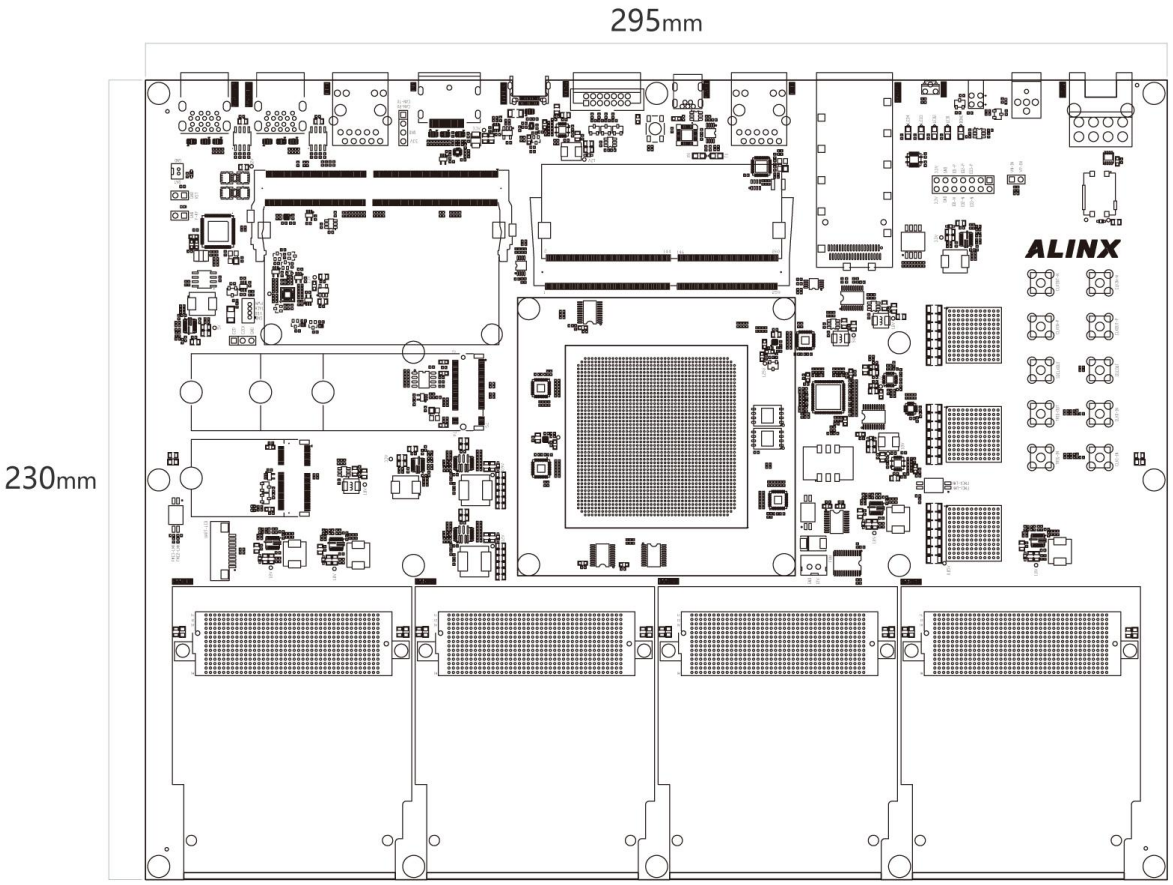


Figure 21: Top view structural dimensional

ORIN System

17 NVIDIA ORIN

This development board includes a SO-DIMM connector for the NVIDIA ORIN module. The board utilizes the NVIDIA Jetson Orin NX 8GB module, which, despite its small form factor, delivers up to 70 TOPS of AI performance.

The module is supported by the same AI software and cloud-native workflows used on other NVIDIA platforms. It provides the performance and power efficiency that enterprises need to build autonomous machines at the edge, while the powerful Jetson software stack allows for a faster time-to-market. This makes it an ideal choice for learning and developing AI and robotics.

Model is shown as below:

Figure 22: Top view of the ORIN Module

Jetson Orin NX Specifications shown as follows:

	Jetson AGX Orin series				Jetson Orin NX series	
	Jetson AGX Orin Developer Kit	Jetson AGX Orin 64GB	Jetson AGX Orin Industrial	Jetson AGX Orin 32GB	Jetson Orin NX 16GB	Jetson Orin NX 8GB
AI Performance	275 TOPS		248 TOPs	200 TOPS	157 TOPS	117 TOPS
GPU	2048-core NVIDIA Ampere architecture GPU with 64 Tensor Cores			1792-core NVIDIA Ampere c GPU with 56 Tensor Cores	1024-core NVIDIA Ampere architecture GPU with 32 Tensor Cores	
GPU Max Frequency	1.3 GHz		1.2 GHz	930 MHz	1173MHz	1173MHz
CPU	12-core Arm® Cortex®-A78AE v8.2 64-bit CPU 3MB L2 + 6MB L3			8-core Arm® Cortex®-A78AE v8.2 64-bit CPU 2MB L2 + 4MB L3	8-core Arm® Cortex®-A78AE v8.2 64-bit CPU 2MB L2 + 4MB L3	6-core Arm® Cortex®-A78AE v8.2 64-bit CPU 1.5MB L2 + 4MB L3
CPU Max Frequency	2.2 GHz		2.0 GHz	2.2 GHz	2 GHz	
DL Accelerator	2x NVDLA v2					1x NVDLA v2
DLA Max Frequency	1.6 GHz		1.4 GHz		1.23 GHz	
Vision Accelerator	1x PVA v2					
Safety Cluster Engine	-					-
Memory	64GB 256-bit LPDDR5 204.8GB/s		64GB 256-bit LPDDR5 (+ ECC) 204.8GB/s	32GB 256-bit LPDDR5 204.8GB/s	16GB 128-bit LPDDR5 102.4GB/s	8GB 128-bit LPDDR5 102.4GB/s
Storage	64GB eMMC 5.1				- (Supports external NVMe)	
Video Encode	2x 4K60 (H.265) 4x 4K30 (H.265) 8x 1080p60 (H.265) 16x 1080p30 (H.265)		1x 4K60 (H.265) 3x 4K30 (H.265) 7x 1080p60 (H.265) 15x 1080p30 (H.265)	1x 4K60 (H.265) 3x 4K30 (H.265) 6x 1080p60 (H.265) 12x 1080p30 (H.265)		

Video Decode	1x 8K30 (H.265) 3x 4K60 (H.265) 7x 4K30 (H.265) 11x 1080p60 (H.265) 22x 1080p30 (H.265)	1x 8K30 (H.265) 3x 4K60 (H.265) 7x 4K30 (H.265) 11x 1080p60 (H.265) 23x 1080p30 (H.265)	1x 8K30 (H.265) 2x 4K60 (H.265) 4x 4K30 (H.265) 9x 1080p60 (H.265) 18x 1080p30 (H.265)		
CSI Camera	16-lane MIPI CSI-2 connector	Up to 6 cameras (16 via virtual channels) 16 lanes MIPI CSI-2 D-PHY 2.1 (up to 40Gbps) | C-PHY 2.0 (up to 164Gbps)		Up to 4 cameras (8 via virtual channels***) 8 lanes MIPI CSI-2 D-PHY 2.1 (up to 20Gbps)	
PCIe*	x16 PCIe slot supporting x8 PCIe Gen4 M.2 Key M slot with x4 PCIe Gen4 M.2 Key E slot with x1 PCIe Gen4	Up to 2 x8 + 1 x4 + 2 x1 (PCIe Gen4, Root Port, & Endpoint)		1 x4 + 3 x1 (PCIe Gen4, Root Port, & Endpoint)	
USB*	USB Type-C connector: 2x USB 3.2 Gen2 USB Type-A connector: 2x USB 3.2 Gen2, 2x USB 3.2 Gen1 USB Micro-B connector: USB 2.0	3x USB 3.2 Gen2 (10 Gbps) 4x USB 2.0		3x USB 3.2 Gen2 (10 Gbps) 3x USB 2.0	
Networking*	RJ45 connector with up to 10 GbE	1x GbE 1x 10GbE		1x GbE	
Display	1x DisplayPort 1.4a (+MST) connector	1x 8K60 multi-mode DP 1.4a (+MST)/eDP 1.4a/HDMI 2.1		1x 8K30 multi-mode DP 1.4a (+MST)/eDP 1.4a/HDMI 2.1	
Other I/O	40-pin header (UART, SPI, I2S, I2C, CAN, PWM, DMIC, GPIO) 12-pin automation header 10-pin audio panel header 10-pin JTAG header 4-pin fan header 2-pin RTC batter backup connector microSD slot DC power jack Power, Force Recovery, and Reset buttons	4x UART, 3x SPI, 4x I2S, 8x I2C, 2x CAN, PWM, DMIC & DSPK, GPIOs		3x UART, 2x SPI, 2x I2S, 4x I2C, 1x CAN, DMIC & DSPK, PWM, GPIOs	
Power	15W - 60W	15W-75W	15W - 40W	10W - 15W - 25W - 40W	10W - 15W - 25W - 40W
Mechanical	110mm x 110mm x 71.65mm (Height includes feet, carrier board, module, and thermal solution)	100mm x 87mm 699-pin Molex Mirror Mezz Connector Integrated Thermal Transfer Plate		69.6mm x 45mm 260-pin SO-DIMM connector	

Figure 23: Specs of the ORIN Module

18 M.2 SSD Interface

18.1 Schematics

The ORIN system provides one M.2 interface compliant with the **PCIe Gen4 x2** standard, which is used for connecting an NVMe Solid-State Drive (SSD). The ORIN's data and system files are stored on this SSD.

The M.2 interface uses an **M-key** slot. It supports **PCIe-based NVMe SSDs only** and does not support SATA-based SSDs. Users must choose a PCIe-type NVMe SSD for this interface.

The design schematic for the M.2 interface is shown below:

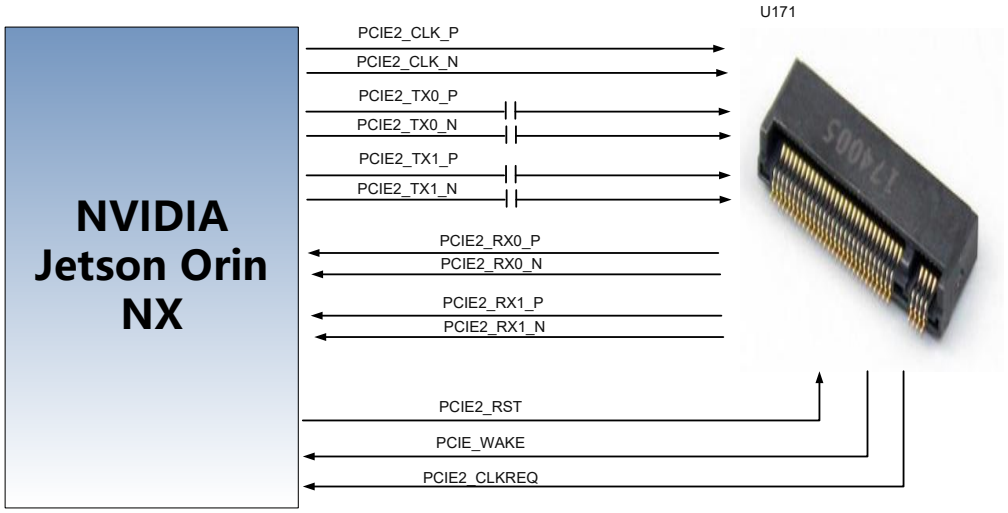


Figure 24: M.2 SSD Interface

18.2 M.2 SSD Interface

M.2 SSD interface pin assignment:

40	PCIE2_RX0_N	PCIe 2 Receive 0– (PCIe Ctrl #7 Lane 0)	Input	PCIe PHY
42	PCIE2_RX0_P	PCIe 2 Receive 0+ (PCIe Ctrl #7 Lane 0)	Input	PCIe PHY
46	PCIE2_TX0_N	PCIe 2 Transmit 0– (PCIe Ctrl #7 Lane 0)	Output	PCIe PHY
48	PCIE2_TX0_P	PCIe 2 Transmit 0+ (PCIe Ctrl #7 Lane 0)	Output	PCIe PHY
58	PCIE2_RX1_N (PCIE3_RX0_N)	PCIe 2 Receive 1– (PCIe Ctrl #7 Lane 1) or PCIe 3 Receive 0– (PCIe Ctrl #9 Lane 0)	Input	PCIe PHY
60	PCIE2_RX1_P (PCIE3_RX0_P)	PCIe 2 Receive 1+ (PCIe Ctrl #7 Lane 1) or PCIe 3 Receive 0+ (PCIe Ctrl #9 Lane 0)	Input	PCIe PHY
64	PCIE2_TX1_N (PCIE3_TX0_N)	PCIe 2 Transmit 1– (PCIe Ctrl #7 Lane 1) or PCIe 3 Transmit 0– (PCIe Ctrl #9 Lane 0)	Output	PCIe PHY
66	PCIE2_TX1_P (PCIE3_TX0_P)	PCIe 2 Transmit 1+ (PCIe Ctrl #7 Lane 1) or PCIe 3 Transmit 0+ (PCIe Ctrl #9 Lane 0)	Output	PCIe PHY
52	PCIE2_CLK_N	PCIe 2 Reference Clock– (PCIe Ctrl #7)	Output	PCIe PHY
54	PCIE2_CLK_P	PCIe 2 Reference Clock+ (PCIe Ctrl #7)	Output	PCIe PHY
219	PCIE2_RST*	PCIe 2 Reset (PCIe Ctrl #7). 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain 3.3V
221	PCIE2_CLKREQ*	PCIe 2 Clock Request (PCIe Ctrl #7). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain 3.3V

Table 18: M.2 SSD Pin Assignment Table

19 M.2 Wi-Fi/BT Interface

19.1 schematic

The AXVU13F development board has one M.2 **Key-E** connector, which is reserved for connecting a Wi-Fi/BT module. The interface includes **PCIe x1**, **USB 2.0**, **UART**, **I2S**, and **I2C** signals. Figure 25 shows the interface connection diagram.

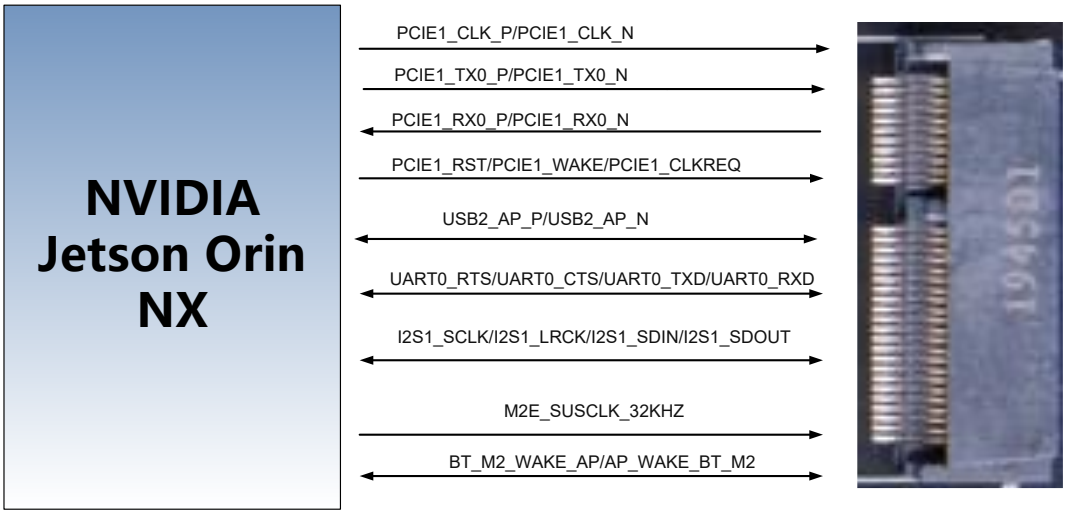


Figure 25: M.2 WIFI/BT Interface

19.2 M.2 WIFI/BT Pin Assignment

Pin #	Signal Name	Description	Direction	Pin Type
99	UART0_TXD	UART #0 Transmit	Output	CMOS – 1.8V
101	UART0_RXD	UART #0 Receive	Input	CMOS – 1.8V
103	UART0_RTS*	UART #0 Request to Send	Output	CMOS – 1.8V
105	UART0_CTS*	UART #0 Clear to Send	Input	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V
167	PCIE1_RX0_N	PCIe 1 Receive 0– (PCIe Ctrl #1 Lane 0)	Input	PCIe PHY
169	PCIE1_RX0_P	PCIe 1 Receive 0+ (PCIe Ctrl #1 Lane 0)	Input	PCIe PHY
172	PCIE1_TX0_N	PCIe 1 Transmit 0– (PCIe Ctrl #1 Lane 0)	Output	PCIe PHY
174	PCIE1_TX0_P	PCIe 1 Transmit 0+ (PCIe Ctrl #1 Lane 0)	Output	PCIe PHY
183	PCIE1_RST*	PCIe 1 Reset (PCIe Ctrl #1). 4.7kΩ pull-up to 3.3V on the module.	Output	Open Drain 3.3V
182	PCIE1_CLKREQ*	PCIe 1 Clock Request (PCIe Ctrl #1). 47kΩ pull-up to 3.3V on the module.	Bidir	Open Drain 3.3V
173	PCIE1_CLK_N	PCIe 1 Reference Clock– (PCIe Ctrl #1)	Output	PCIe PHY
175	PCIE1_CLK_P	PCIe 1 Reference Clock+ (PCIe Ctrl #1)	Output	PCIe PHY

121	USB2_D_N	USB 2.0 Port 2 Data–	Bidir	USB PHY
123	USB2_D_P	USB 2.0 Port 2 Data+	Bidir	USB PHY

Table 19: M.2 WIFI/BT Pin Assignment

20 DP Display Interface

Jetson Orin NX module supports DP video output. The development board features one DisplayPort output interface connected to the Jetson Orin NX module for video and image display. The interface supports the **VESA DisplayPort V1.2** and **eDP V1.4** output standards.

The DisplayPort interface pin assignment is as follows:

Jetson SODIMM Signal Name	Jetson Orin NX Function	PIN # Top Odd
DP1_TXD0_N	DP1_TXD0_N	63
DP1_TXD0_P	DP1_TXD0_P	65
GND	GND	67
DP1_TXD1_N	DP1_TXD1_N	69
DP1_TXD1_P	DP1_TXD1_P	71
GND	GND	73
DP1_TXD2_N	DP1_TXD2_N	75
DP1_TXD2_P	DP1_TXD2_P	77
GND	GND	79
DP1_TXD3_N	DP1_TXD3_N	81
DP1_TXD3_P	DP1_TXD3_P	83

Table 20: DP Display Interface Pin Assignment

21 USB 3.0 Interface

21.1 Schematic

The USB0 interface of the NVIDIA Jetson Orin NX module is expanded into four **USB 3.0** Host ports (Type-A) via a **GL3523T** HUB chip. Additionally, the USB1 interface is designed as a **USB 3.0 Type-C** port, which supports Host, Slave, and OTG modes with data transfer speeds up to **5.0 Gbps**.

A schematic of the USB 3.0 connections is shown in Figure 26:

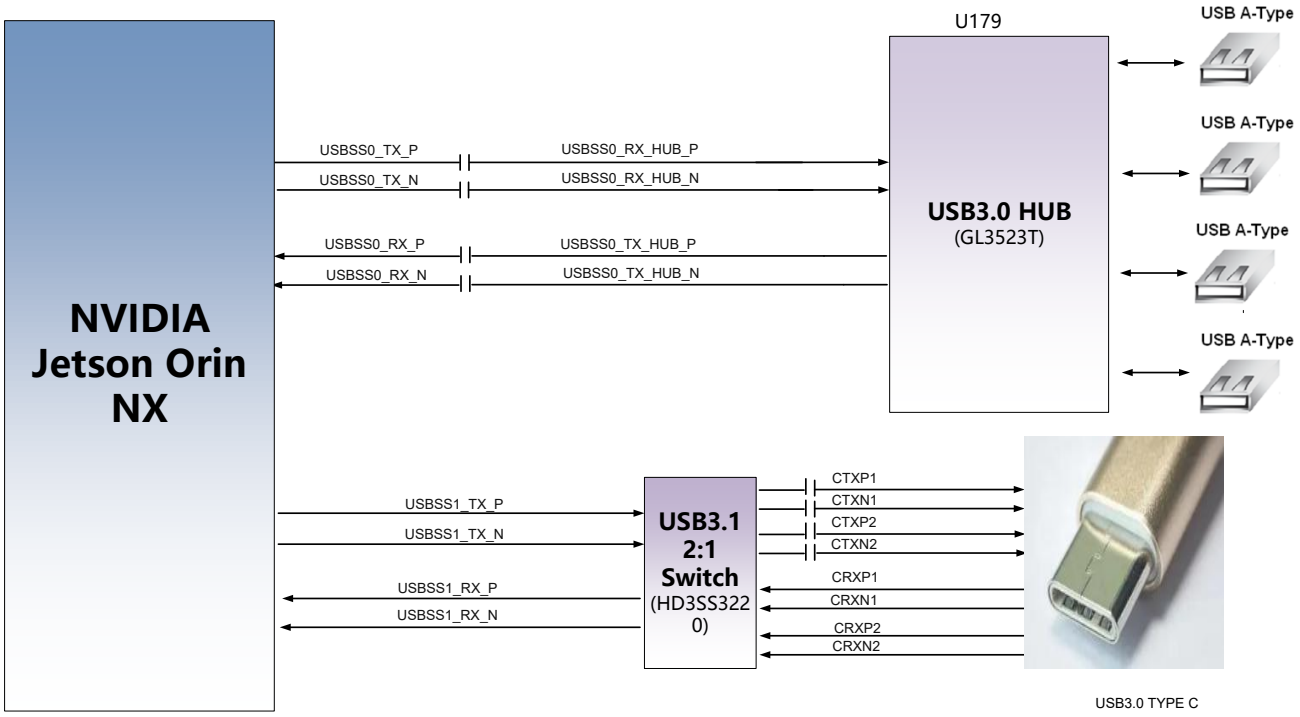


Figure 26: USB 3.0 Interface

21.2 USB Pin Assignment

Pin #	Signal Name	Description	Direction	Pin Type
161	USBSS0_RX_N	USB SS Receive– (USB 3.2 Port #0)	Input	USB SS PHY
163	USBSS0_RX_P	USB SS Receive+ (USB 3.2 Port #0)	Input	USB SS PHY
166	USBSS0_TX_N	USB SS Transmit– (USB 3.2 Port #0)	Output	USB SS PHY
168	USBSS0_TX_P	USB SS Transmit+ (USB 3.2 Port #0)	Output	USB SS PHY
39	USBSS1_RX_N	USB SS Receive– (USB 3.2 Port #1)	Input	USB SS PHY
41	USBSS1_RX_P	USB SS Receive+ (USB 3.2 Port #1)	Input	USB SS PHY
45	USBSS1_TX_N	USB SS Transmit– (USB 3.2 Port #1)	Output	USB SS PHY
47	USBSS1_TX_P	USB SS Transmit+ (USB 3.2 Port #1)	Output	USB SS PHY
51	USBSS2_RX_N	USB SS Receive– (USB 3.2 Port #2)	Input	USB SS PHY
53	USBSS2_RX_P	USB SS Receive+ (USB 3.2 Port #2)	Input	USB SS PHY
57	USBSS2_TX_N	USB SS Transmit– (USB 3.2 Port #2)	Output	USB SS PHY
59	USBSS2_TX_P	USB SS Transmit+ (USB 3.2 Port #2)	Output	USB SS PHY

Table 21: USB Pin Assignment

22 Gigabit Ethernet Interface

22.1 Schematic

The NVIDIA Jetson Orin NX module provides one Gigabit Ethernet interface. The MDI signals from the module are connected directly to the RJ45 connector.

Figure 27 shows the Ethernet connection diagram:

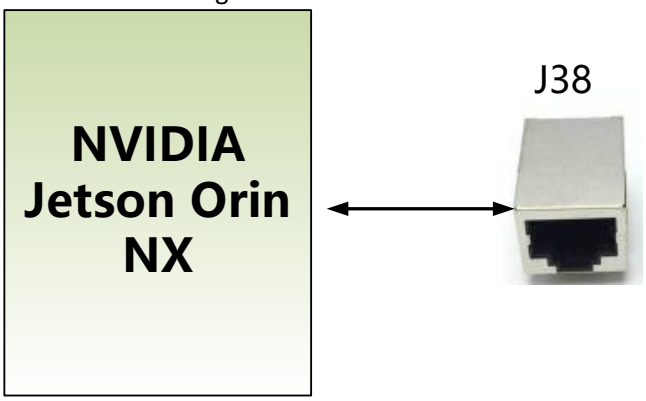


Figure 27: USB 3.0 Interface

22.2 NVIDIA Jetson Orin NX Gigabit Ethernet Pin Assignment

Pin #	Signal Name	Description	Direction	Pin Type
184	GBE_MDI0_N	GbE Transformer Data 0–	Bidir	MDI
186	GBE_MDI0_P	GbE Transformer Data 0+	Bidir	MDI
190	GBE_MDI1_N	GbE Transformer Data 1–	Bidir	MDI
192	GBE_MDI1_P	GbE Transformer Data 1+	Bidir	MDI
196	GBE_MDI2_N	GbE Transformer Data 2–	Bidir	MDI
198	GBE_MDI2_P	GbE Transformer Data 2+	Bidir	MDI
202	GBE_MDI3_N	GbE Transformer Data 3–	Bidir	MDI
204	GBE_MDI3_P	GbE Transformer Data 3+	Bidir	MDI
188	GBE_LED_LINK	Ethernet Link LED (Green)	Output	-
194	GBE_LED_ACT	Ethernet Activity LED (Yellow)	Output	-

Table 22: Jetson Orin NX Gigabit Ethernet Pin Assignment

23 EEPROM

The board features a **24AA04 I/SN** EEPROM chip with a capacity of **4Kbit**. It communicates with the NVIDIA Jetson Orin NX module via the **I2C** bus.

The pin assignment for communication between the EEPROM and the NVIDIA Jetson Orin NX module is as follows:

Pin #	Signal Name	Description	Direction	Pin Type
232	I2C2_SCL	General I2C 2 Clock. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V
234	I2C2_SDA	General I2C 2 Data. 2.2kΩ pull-up to 1.8V on the module.	Bidir	Open Drain – 1.8V

Table 23: Pin Configuration

24 Power Supply

The power supply system for the NVIDIA Jetson Orin NX module is as follows: the VDD_CVM supply provides power to the Orin NX module itself, while other circuits provide power for the various peripherals on the ORIN system board.

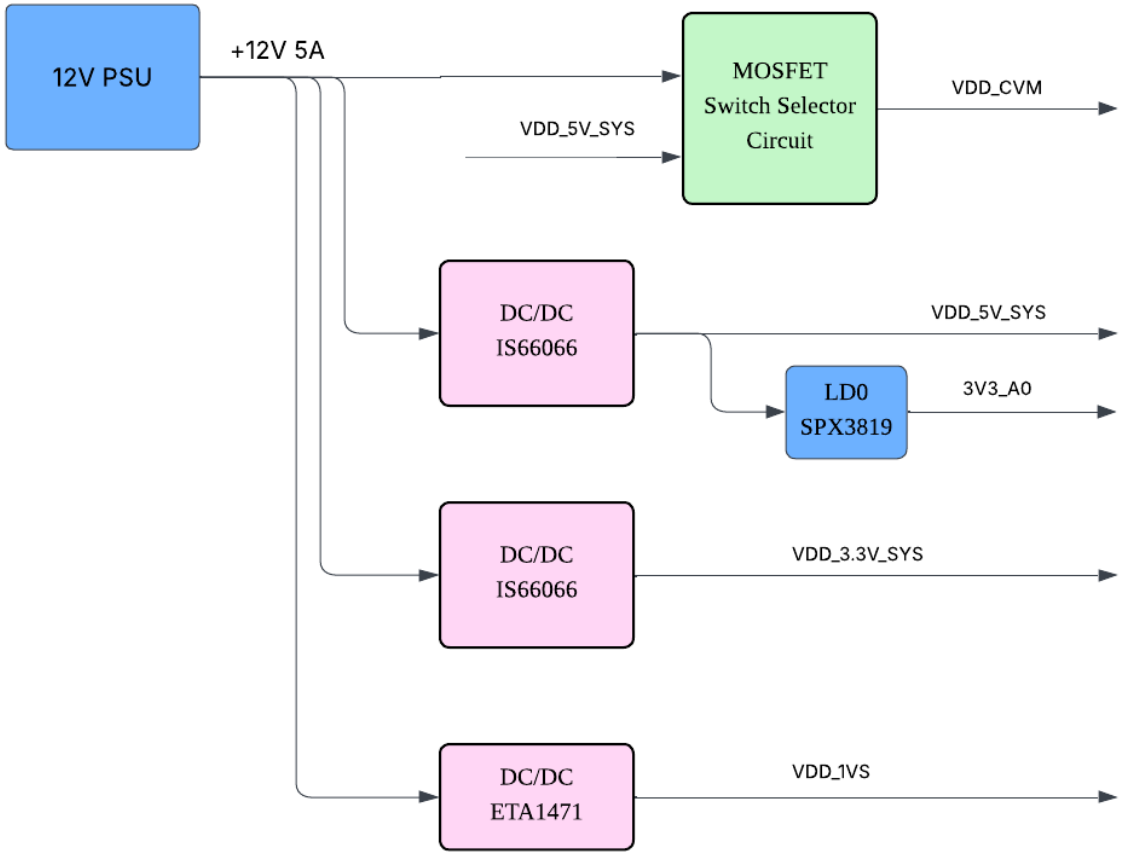


Figure 28: Orin NX Power Supply Diagram

A MOSFET switching circuit, as shown in Figure 29, uses the MODULE_ID pin from the Orin NX module to determine whether to output 12V or +5V.

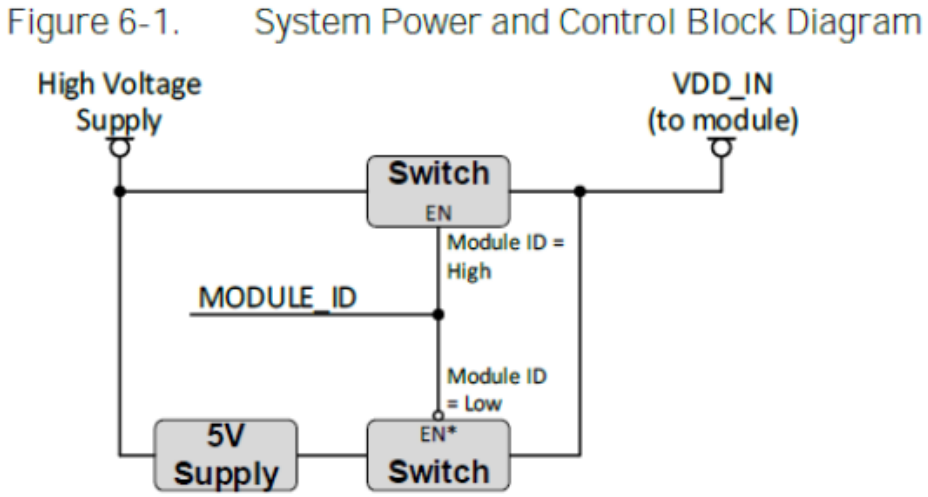


Figure 29: Power Switching Diagram

The baseboard is designed with a programmable "POWER LOGIC" chip that controls the power-on sequence for the Orin NX module and its peripherals. After the board receives power, pressing the Power button causes the Power Logic to output a high POWER_EN signal, which powers on the Orin NX module. Once the Orin NX module has finished booting, it outputs a high SYS_RESET signal, which in turn enables the power supplies for the peripherals on the baseboard.

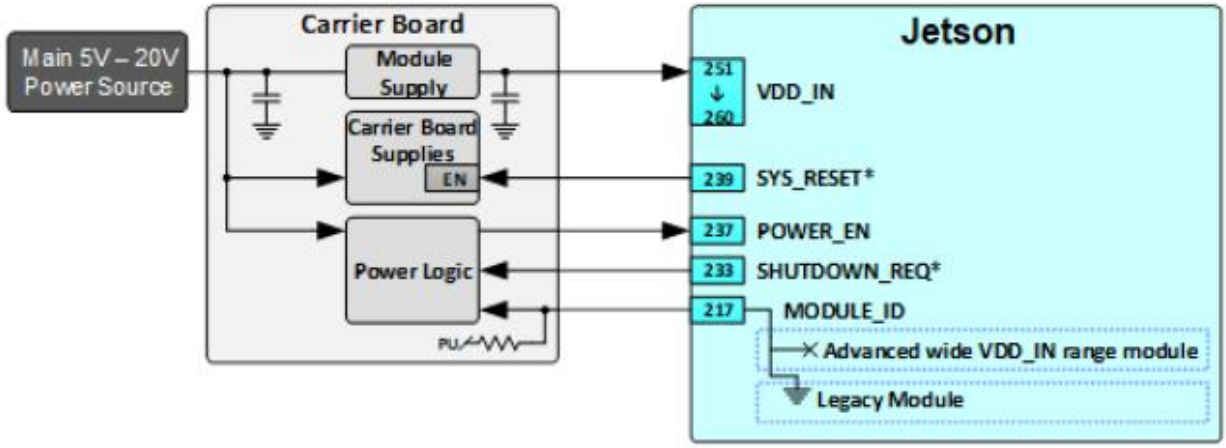


Figure 30: System Power and Control Block Diagram

Figure 6-4. Power Up Sequence with Power Button

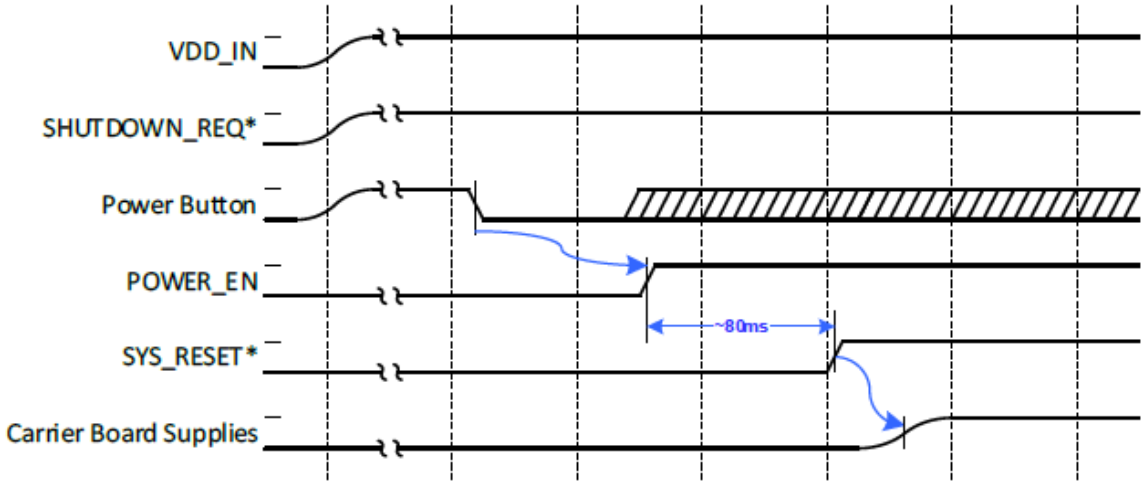


Figure 31: Power Up Sequence with Power Button

25 Power Button

The AXVU13F development board has one power switch, which is a momentary push-button with an integrated LED. The button's signal is connected to the SLEEP/WAKE pin of the NVIDIA Jetson Orin NX, allowing users to control the board's power-on and power-off states.

- **To Power On:** Press the power button once to start the system.
- **To Power Off:** Press and hold the power button for more than 10 seconds to shut down the power.