Xilinx FPGA

AXVU13P Development Board

User Manual

ALINX

Document Revision Record:

Version	Time	Description
1.0	2024/6/5	Initial Release

Contents

Overview

Alinx Electronic Limited has released the AXVU13P Development Platform based on the Xilinx Virtex Ultrascale+ FPGA. Virtex Ultrascale+ FPGA Development Platform adopts an all-in-one board design, utilizing the Xilinx Virtex Ultrascale+ chip model XCVU13PFHGB2104 as its main solution.

It features a SODIMM memory slot supporting up to 16GB, three FMC+ interfaces, and is equipped with a 2Gb QSPI FLASH chip. Additionally, the platform extends a rich set of peripheral interfaces for users, including one PCIe 3.0 x16 interface, one SMA input, one SMA output, one UART serial interface, DIP switches, and IO expansion interfaces among others.

This platform meets various user needs such as high-speed data exchange, data acceleration, industrial control, and validation of complex algorithm models, making it a "Professional-Grade" FPGA Development Board.

Figure 1: AXVU13P Development Board

1 Block Diagram

The AXVU13P is mainly composed of a minimal system featuring the XCVU13P-2FHGB2104I FPGA, a SODIMM interface with up to 16GB capacity, and two 1Gb QSPI FLASH units. It uses the Xilinx Virtex Ultrascale+ series chip, model XCVU13P-2FHGB2104I.

The SODIMM interface supports 16GB with a 72-bit data path, while the two QSPI FLASH units are used for static storage of FPGA configuration files or other user data. The platform includes one PCIe 3.0 x16 interface, three FMC+ interfaces, one SMA input, one SMA output, one UART serial interface, and one 14-pin IO expansion interface, along with various DIP switches, buttons, and LEDs.

Figure 2 shows the structure of the entire development system:

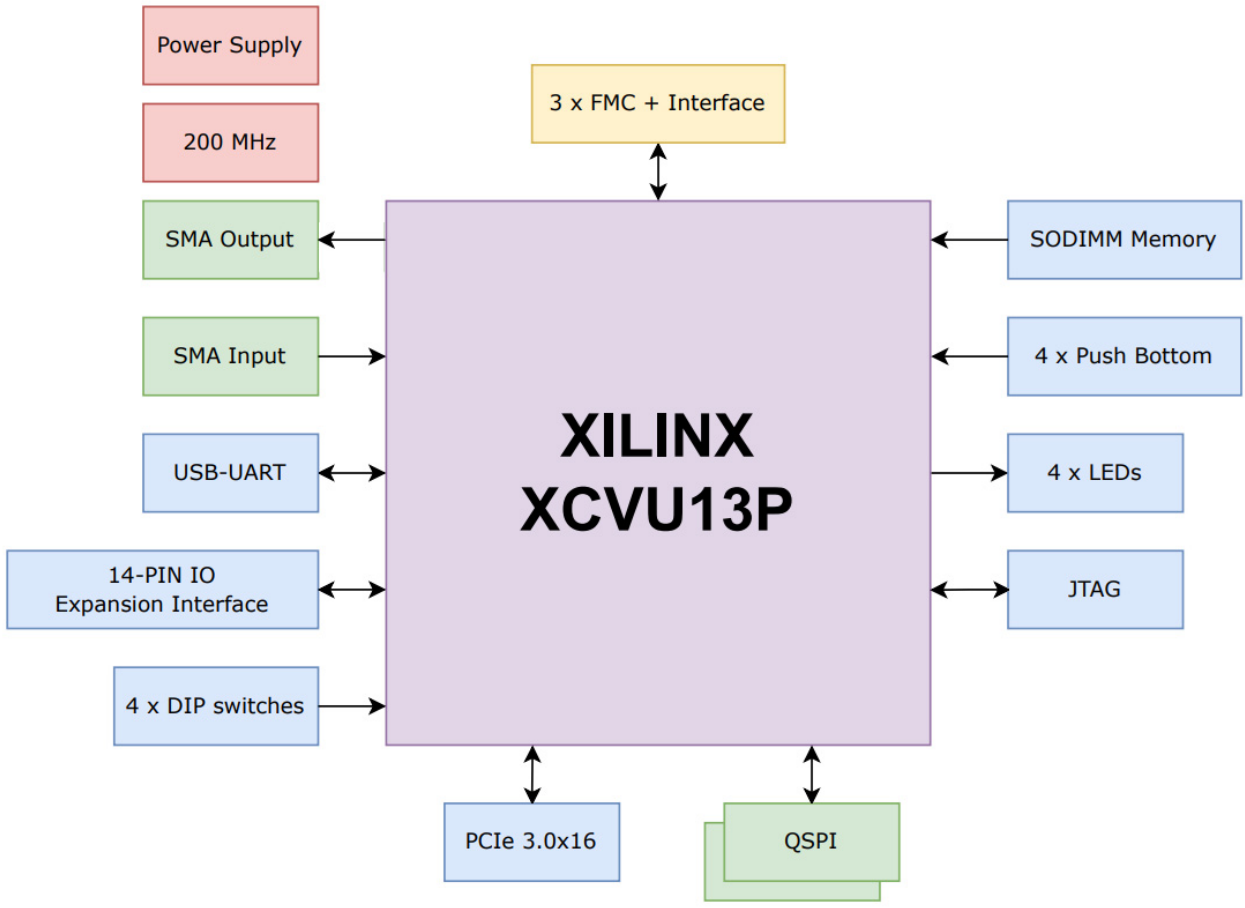

Figure 2: Schematic diagram of the development system

FPGA Minimal System:

Comprises the XCVU13P-2FHGB2104I, a SODIMM interface, and QSPI FLASH. The board also features a high-precision, temperature-compensated crystal oscillator and a programmable clock source, providing reference clocks for the FPGA logic, SODIMM controller, and high-speed transceivers.

DDR4 Interface:

Includes one 260-pin DDR4 SODIMM memory slot with a 72-bit data path, supporting up to 16GB in capacity.

PCIe 3.0 x16 Interface:

Supports the PCI Express 3.0 standard, providing a standard PCIe x16 high-speed data transfer interface with a single-channel communication rate up to 8 GBaud.

3 FMC+ Interfaces:

The 56 high-speed transceivers in the FPGA are connected to three FMC+ dedicated high-speed pins.

- FMC1+ connector exposes 34 pairs of LA differential signals, 2 pairs of clock signals, 24 pairs of HA signals, and 20 pairs of high-speed transceivers.
- FMC2+ connector exposes 34 pairs of LA differential signals, 2 pairs of clock signals, 24 pairs of HA signals, and 16 pairs of high-speed transceivers.
- FMC3+ connector exposes 34 pairs of LA differential signals, 2 pairs of clock signals, 24 pairs of HA signals, 22 pairs of HB signals, and 24 pairs of high-speed transceivers.

These interfaces meet high-speed signal transmission requirements, are compliant with the FMC+ standard, and are compatible with various FMC+ and FMC modules.

SMA Input/Output Interface:

One SMA differential input/output interface is connected to the FPGA's HPIO pins, facilitating customer differential signal input and output verification.

4-Bit DIP Switches:

For simple input verification by the customer.

USB UART Interface:

One UART-to-USB interface for communication with a computer, aiding in user debugging. The serial chip used is the Silicon Labs CP2102GM USB-UART chip, with a MINI USB connector.

Expansion Port:

Features a 14-pin, 2.54mm pitch expansion interface, bringing out 10 HPIO pins of the FPGA for customer testing.

JTAG Debug Port:

One 14-pin, 2.00mm standard JTAG port for downloading and debugging FPGA programs, allowing users to program and debug the FPGA system with a XILINX programmer.

LEDs:

Includes 8 LEDs: 1 DONE configuration indicator, 1 power indicator, 4 user LEDs, and 2 UART indicator LEDs.

Buttons:

One user button.

2 FPGA Chip

2.1 Naming Convention

The FPGA model used in this product is XCVU13P-2FHGB2104I, which belongs to the Xilinx Virtex Ultrascale+ series. It has a speed grade of 2 and an industrial temperature grade. This model comes in the FHGB2104 package with 2104 pins.

The naming convention for Xilinx Virtex Ultrascale+ FPGAs is as Figure 3.

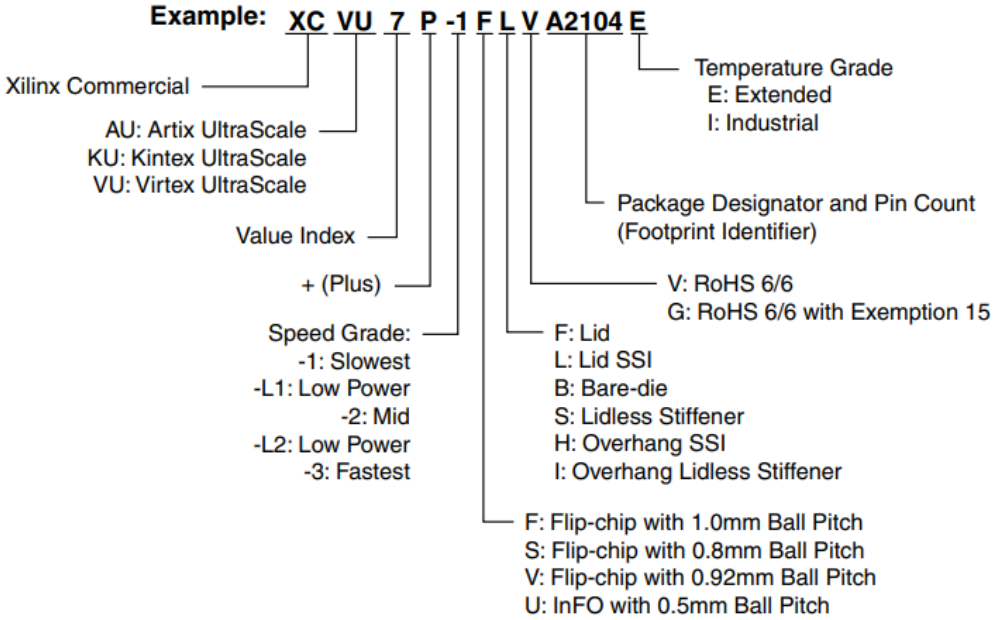

Figure 3: Naming convention for Xilinx Virtex Ultrascale+ FPGAs

2.2 Main Parameters of the FPGA Chip

FPGA Resource Specifications	Parameters
Logic Cells	3780K
Registers (FF)	3456K
LUTs	1728K
Total Block RAM	94.5Mb
Ultra RAM	360Mb
DSP Slices	12,288
CMTs	16
GTY/Gb/s	76/28.21Gb
PCIe Gen3 x16	4
Speed Grade	-2
Temperature Grade	Industrial Level

Table 1: Main parameters

3 DDR4 DRAM

3.1 Type and Parameter

The AXVU13P development board is equipped with a SODIMM memory module interface that supports DDR4, accommodating various capacities such as 8GB and 16GB, and we recommend using the models we have tested. It supports a data bus width of up to 72 bits. On the FPGA side, the maximum operational data rate is 2666 Mbps. The SODIMM interface is connected to the memory interfaces of BANK 61, 62, and 63.

The specific configuration of the DDR4 SDRAM is shown in Table 2 below.

Position Number	Chip Type	Capacity
J3	SODIMM	(8/16/32)GB

Table 2: DDR4 SDRAM configuration

3.2 Schematic Diagram

DDR4 hardware design requires stringent consideration of signal integrity. In circuit design and PCB design phases, we have thoroughly addressed impedance matching/termination resistance, trace impedance control, and equal length trace control to ensure stable and high-speed operation of DDR4.

The hardware connection method of the DDR4 DRAM at the FPGA end is shown in Figure 4:

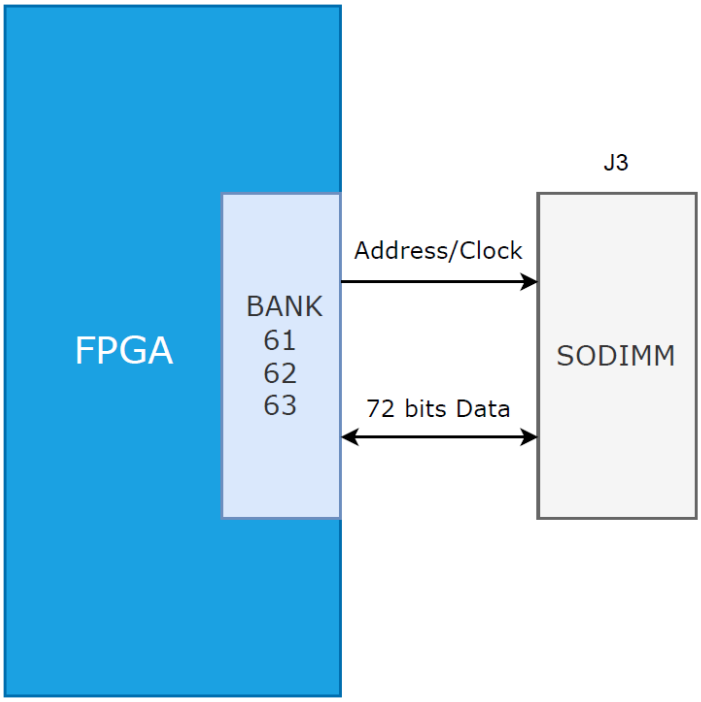

Figure 4: DDR4 DRAM schematic diagram

Figure 5 shows the physical object of the development board's SODIMM interface.

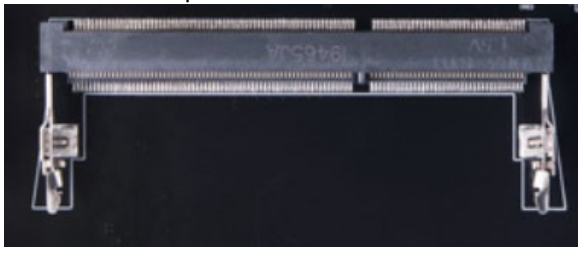

Figure 5: SODIMM interface

3.3 SODIMM Interface FPGA PIN Assignment

Signal Name	PIN Number
PL_DDR4_DQ0	AW34
PL_DDR4_DQ1	AW33
PL_DDR4_DQ2	AY36
PL_DDR4_DQ3	BA33
PL_DDR4_DQ4	AV33
PL_DDR4_DQ5	AY33
PL_DDR4_DQ6	AY35
PL_DDR4_DQ7	AV34
PL_DDR4_DQ8	AL32
PL_DDR4_DQ9	AM34
PL_DDR4_DQ10	AP33
PL_DDR4_DQ11	AM32
PL_DDR4_DQ12	AL34
PL_DDR4_DQ13	AN34
PL_DDR4_DQ14	AP34
PL_DDR4_DQ15	AR33
PL_DDR4_DQ16	BD39
PL_DDR4_DQ17	BE38
PL_DDR4_DQ18	BB38
PL_DDR4_DQ19	BF38
PL_DDR4_DQ20	BF37
PL_DDR4_DQ21	BC39
PL_DDR4_DQ22	BC38
PL_DDR4_DQ23	BE37
PL_DDR4_DQ24	BE36
PL_DDR4_DQ25	BD36
PL_DDR4_DQ26	BB35
PL_DDR4_DQ27	BE35
PL_DDR4_DQ28	BA35
PL_DDR4_DQ29	BB36
PL_DDR4_DQ30	BC36
PL_DDR4_DQ31	BD35
PL_DDR4_DQ32	BB31
PL_DDR4_DQ33	BA30
PL_DDR4_DQ34	AY30
PL_DDR4_DQ35	BA29
PL_DDR4_DQ36	AY32

PL_DDR4_DQ37	BB30
PL_DDR4_DQ38	AY31
PL_DDR4_DQ39	BB29
PL_DDR4_DQ40	BD29
PL_DDR4_DQ41	BE32
PL_DDR4_DQ42	BD33
PL_DDR4_DQ43	BE30
PL_DDR4_DQ44	BE31
PL_DDR4_DQ45	BE33
PL_DDR4_DQ46	BC29
PL_DDR4_DQ47	BF30
PL_DDR4_DQ48	AP30
PL_DDR4_DQ49	AP29
PL_DDR4_DQ50	AL30
PL_DDR4_DQ51	AM31
PL_DDR4_DQ52	AN31
PL_DDR4_DQ53	AR30
PL_DDR4_DQ54	AN29
PL_DDR4_DQ55	AL29
PL_DDR4_DQ56	AU32
PL_DDR4_DQ57	AW31
PL_DDR4_DQ58	AU30
PL_DDR4_DQ59	AT30
PL_DDR4_DQ60	AV32
PL_DDR4_DQ61	AV31
PL_DDR4_DQ62	AU31
PL_DDR4_DQ63	AT29
PL_DDR4_DQ64	Y33
PL_DDR4_DQ65	AB34
PL_DDR4_DQ66	Y32
PL_DDR4_DQ67	Y30
PL_DDR4_DQ68	W34
PL_DDR4_DQ69	W33
PL_DDR4_DQ70	AA34
PL_DDR4_DQ71	W30
C1_DDR4_CLKREF_N	AF33
C1_DDR4_CLKREF_P	AF32
PL_DDR4_A0	AC33
PL_DDR4_A1	AG29
PL_DDR4_A2	AJ29

PL_DDR4_A3	AG32
PL_DDR4_A4	AK28
PL_DDR4_A5	AJ30
PL_DDR4_A6	AG31
PL_DDR4_A7	AH31
PL_DDR4_A8	AG30
PL_DDR4_A9	AH32
PL_DDR4_A10	AJ27
PL_DDR4_A11	AJ31
PL_DDR4_A12	AF34
PL_DDR4_A13	AF30
PL_DDR4_ACT_B	AK31
PL_DDR4_ALERT_B	AK32
PL_DDR4_BA0	AH28
PL_DDR4_BA1	AC32
PL_DDR4_BG0	AH34
PL_DDR4_BG1	AH33
PL_DDR4_CAS_B	AH29
PL_DDR4_CKE0	AJ33
PL_DDR4_CKE1	AG34
PL_DDR4_CLK0_N	AE32
PL_DDR4_CLK0_P	AE31
PL_DDR4_CLK1_N	AE33
PL_DDR4_CLK1_P	AD33
PL_DDR4_CS0_B	AC31
PL_DDR4_CS1_B	AD31
PL_DDR4_DM0	BA34
PL_DDR4_DM1	AT33
PL_DDR4_DM2	BF39
PL_DDR4_DM3	BC34
PL_DDR4_DM4	BC31
PL_DDR4_DM5	BF32
PL_DDR4_DM6	AP31
PL_DDR4_DM7	AW29
PL_DDR4_DM8	AA32
PL_DDR4_DQS0_N	AW36
PL_DDR4_DQS0_P	AW35
PL_DDR4_DQS1_N	AN33
PL_DDR4_DQS1_P	AN32
PL_DDR4_DQS2_N	BE40

PL_DDR4_DQS2_P	BD40
PL_DDR4_DQS3_N	BC37
PL_DDR4_DQS3_P	BB37
PL_DDR4_DQS4_N	BB32
PL_DDR4_DQS4_P	BA32
PL_DDR4_DQS5_N	BD31
PL_DDR4_DQS5_P	BD30
PL_DDR4_DQS6_N	AM30
PL_DDR4_DQS6_P	AM29
PL_DDR4_DQS7_N	AV29
PL_DDR4_DQS7_P	AU29
PL_DDR4_DQS8_N	Y31
PL_DDR4_DQS8_P	W31
PL_DDR4_ODT0	AB32
PL_DDR4_ODT1	AD30
PL_DDR4_PARITY	AK27
PL_DDR4_RAS_B	AJ28
PL_DDR4_RST	AJ34
PL_DDR4_SCL_LS	AT14
PL_DDR4_SDA_LS	AT13
PL_DDR4_WE_B	AE30

Table 3: SODIMM Interface FPGA Pin Assignment

4 QSPI Flash

4.1 Type and Parameter

The module is equipped with 2 pieces of 1GBit Quad-SPI FLASH chips, model MT25QU01GBBB1EW9, which uses the 1.8V CMOS voltage standard. Due to the non-volatile nature of QSPI FLASH, it can be used to store FPGA configuration Bin files as well as other user data files.

The specific model and related parameters of the QSPI FLASH are listed in Table 2.

Position Number	Chip Type	Capacity	Manufacturers
U10; U11	MT25QU01GBBB1EW9	1Gbit	Micron

Table 4: QSPI Flash type and parameter.

4.2 Schematic Diagram

The QSPI FLASH is connected to dedicated pins on the FPGA chip. The clock pin is connected to CCLK0 of the dedicated BANK0, while the data pins are connected to BANK0 and BANK65 respectively.

Figure 6 illustrates the connection diagram between the QSPI Flash and the FPGA chip.

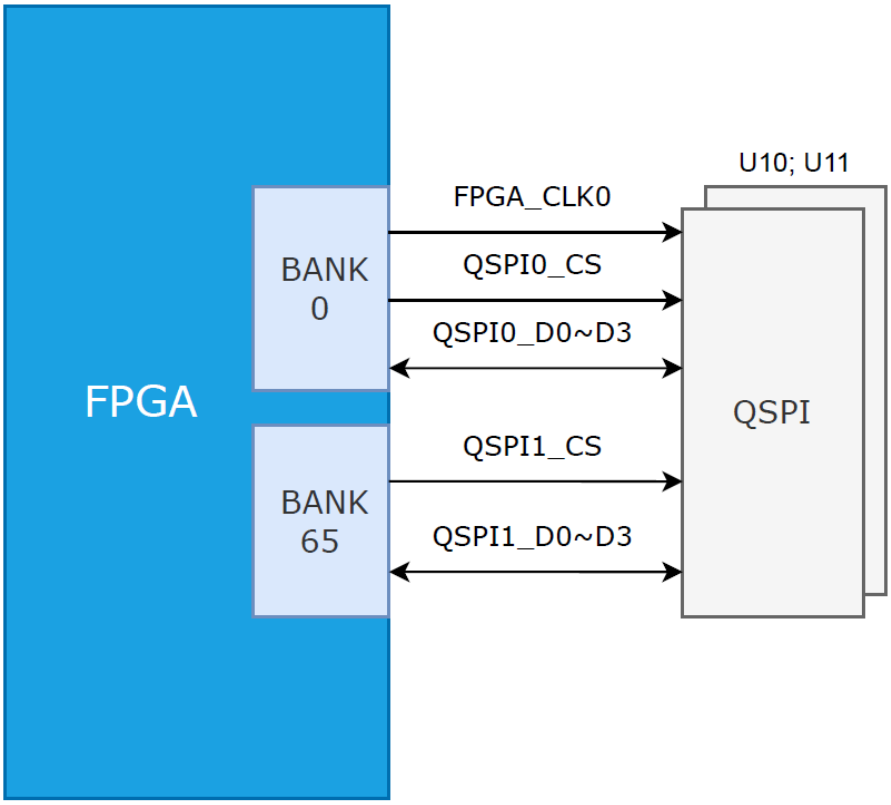

Figure 6: QSPI Flash schematic diagram

4.3 Configure Chip PIN Assignment

Signal Name	PIN Number
QSPI_CLK	AG13
QSPI0_CS	AG12
QSPI0_DQ0	AK12
QSPI0_DQ1	AJ12
QSPI0_DQ2	AL12
QSPI0_DQ3	AH12
QSPI1_CS	BF27
QSPI1_DQ0	AM26
QSPI1_DQ1	AN26
QSPI1_DQ2	AL25
QSPI1_DQ3	AM25

Table 3: Configure chip PIN assignment

5 Clock Configuration

5.1 FPGA System Clock Source

The board is equipped with two 200MHz differential crystal oscillators, which can provide reference clocks for the SODIMM controller and FPGA logic. The oscillator outputs are connected to the global clocks of FPGA BANK63 and BANK69, which can be used to drive the DDR4 controller and user logic circuits within the FPGA.

The schematic of this clock source is shown in Figure 7.

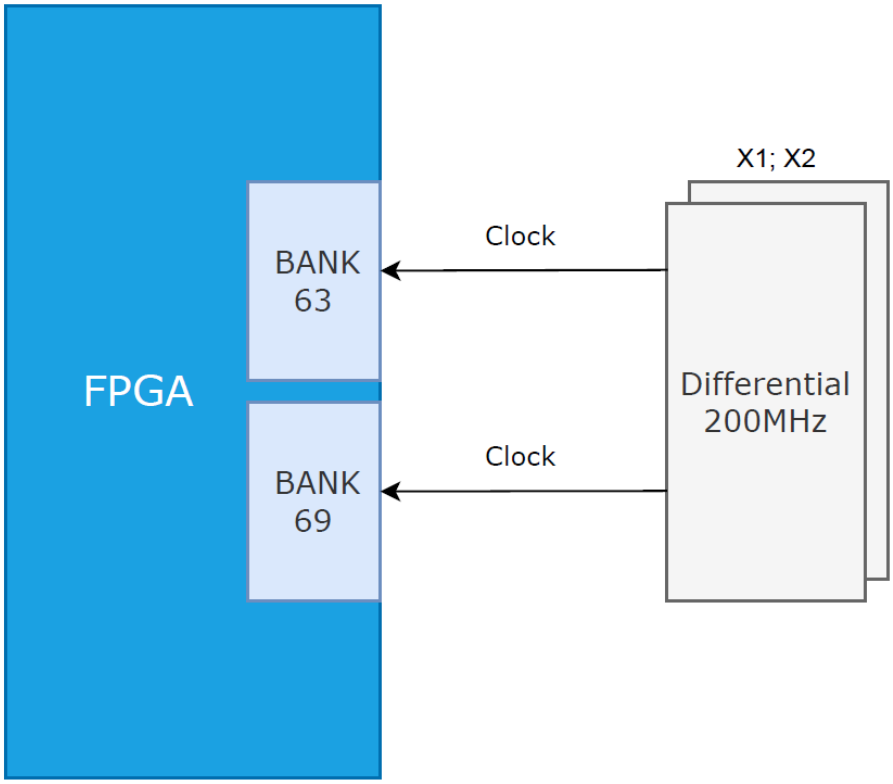

Figure 7: System clock source

5.2 Clock PIN Assignment

Signal Name	PIN Number
BADJ_CLK1_N	AW18
BADJ_CLK1_P	AV18
C1_DDR4_CLKREF_N	AF33
C1_DDR4_CLKREF_P	AF32

Table 4: Clock PIN Assignment

5.3 High-Speed Transceiver GTY Clock

The board is equipped with a high-precision, low-jitter, temperature-stabilized programmable multi-output clock source, which has 14 clock channels. This clock source can provide reference clocks for each channel of the high-speed transceiver GTY, meeting the clock requirements of the transceivers.

6 PCIe Interface

6.1 Design Diagram

The AXVU13P expansion board features a PCIe x16 interface that supports the PCIe Gen3.0 protocol. It has 16 transceivers connected to the PCIe x16 for data communication.

The transmission and receive signals of the PCIe interface are directly connected to the transceivers of FPGA BANK224~227. The 16 channels of TX signals and RX signals are all connected to the FPGA's transceivers in differential signal mode, with a single-channel communication rate reaching up to 8G bit bandwidth.

The design schematic of the development board's PCIe interface is shown in Figure 8, where the TX transmit signals are connected using AC coupling mode.

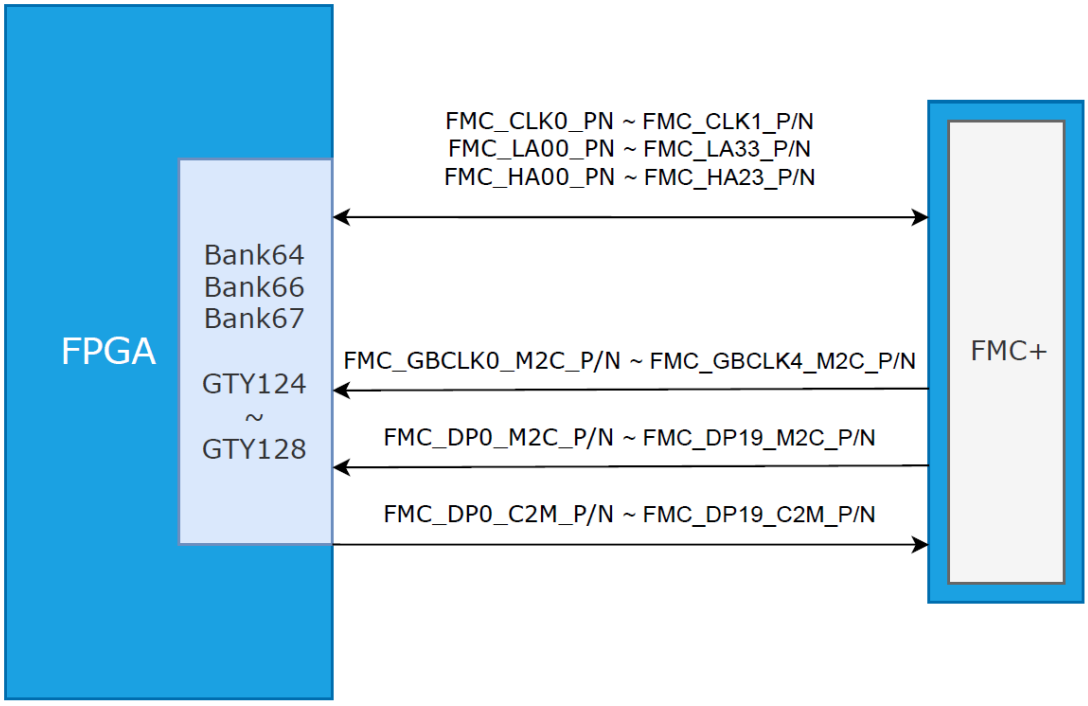

Figure 8: PCIe Interface design diagram

6.2 PCIe x16 Interface FPGA PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
PCIe_RX0_P	MGTYRXP3_227	AF2	PCIe channel 0 data receive positive
PCIe_RX0_N	MGTYRXN3_227	AF1	PCIe channel 0 data receive negative
PCIe_RX1_P	MGTYRXP2_227	AG4	PCIe channel 1 data receive positive
PCIe_RX1_N	MGTYRXN2_227	AG3	PCIe channel 1 data receive negative
PCIe_RX2_P	MGTYRXP1_227	AH2	PCIe channel 2 data receive positive
PCIe_RX2_N	MGTYRXN1_227	AH1	PCIe channel 2 data receive negative
PCIe_RX3_P	MGTYRXP0_227	AJ4	PCIe channel 3 data receive positive
PCIe_RX3_N	MGTYRXN0_227	AJ3	PCIe channel 3 data receive negative
PCIe_RX4_P	MGTYRXP3_226	AK2	PCIe channel 4 data receive positive
PCIe_RX4_N	MGTYRXN3_226	AK1	PCIe channel 4 data receive negative
PCIe_RX5_P	MGTYRXP2_226	AL4	PCIe channel 5 data receive positive
PCIe_RX5_N	MGTYRXN2_226	AL3	PCIe channel 5 data receive negative
PCIe_RX6_P	MGTYRXP1_226	AM2	PCIe channel 6 data receive positive
PCIe_RX6_N	MGTYRXN1_226	AM1	PCIe channel 6 data receive negative
PCIe_RX7_P	MGTYRXP0_226	AN4	PCIe channel 7 data receive positive
PCIe_RX7_N	MGTYRXN0_226	AN3	PCIe channel 7 data receive negative
PCIe_RX8_P	MGTYRXP3_225	AP2	PCIe channel 8 data transmission positive
PCIe_RX8_N	MGTYRXN3_225	AP1	PCIe channel 8 data transmission negative
PCIe_RX9_P	MGTYRXP2_225	AR4	PCIe channel 9 data transmission positive
PCIe_RX9_N	MGTYRXN2_225	AR3	PCIe channel 9 data transmission negative
PCIe_RX10_P	MGTYRXP1_225	AT2	PCIe channel 10 data transmission positive
PCIe_RX10_N	MGTYRXN1_225	AT1	PCIe channel 10 data transmission negative
PCIe_RX11_P	MGTYRXP0_225	AU4	PCIe channel 11 data transmission positive
PCIe_RX11_N	MGTYRXN0_225	AU3	PCIe channel 11 data transmission negative
PCIe_RX12_P	MGTYRXP3_224	AV2	PCIe channel 12 data transmission positive
PCIe_RX12_N	MGTYRXN3_224	AV1	PCIe channel 12 data transmission negative
PCIe_RX13_P	MGTYRXP2_224	AW4	PCIe channel 13 data transmission positive
PCIe_RX13_N	MGTYRXN2_224	AW3	PCIe channel 13 data transmission negative
PCIe_RX14_P	MGTYRXP1_224	BA2	PCIe channel 14 data transmission positive
PCIe_RX14_N	MGTYRXN1_224	BA1	PCIe channel 14 data transmission negative
PCIe_RX15_P	MGTYRXP0_224	BC2	PCIe channel 15 data transmission positive
PCIe_RX15_N	MGTYRXN0_224	BC1	PCIe channel 15 data transmission negative
PCIe_TX0_P	MGTYTXP3_227	AF7	PCIe channel 0 data transmission positive
PCIe_TX0_N	MGTYTXN3_227	AF6	PCIe channel 0 data transmission negative
PCIe_TX1_P	MGTYTXP2_227	AG9	PCIe channel 1 data transmission positive
PCIe_TX1_N	MGTYTXN2_227	AG8	PCIe channel 1 data transmission negative
PCIe_TX2_P	MGTYTXP1_227	AH7	PCIe channel 2 data transmission positive
PCIe_TX2_N	MGTYTXN1_227	AH6	PCIe channel 2 data transmission negative
PCIe_TX3_P	MGTYTXP0_227	AJ9	PCIe channel 3 data transmission positive

PCIe_TX3_N	MGTYTXN0_227	AJ8	PCIe channel 3 data transmission negative
PCIe_TX4_P	MGTYTXP3_226	AK7	PCIe channel 4 data transmission positive
PCIe_TX4_N	MGTYTXN3_226	AK6	PCIe channel 4 data transmission negative
PCIe_TX5_P	MGTYTXP2_226	AL9	PCIe channel 5 data transmission positive
PCIe_TX5_N	MGTYTXN2_226	AL8	PCIe channel 5 data transmission negative
PCIe_TX6_P	MGTYTXP1_226	AM7	PCIe channel 6 data transmission positive
PCIe_TX6_N	MGTYTXN1_226	AM6	PCIe channel 6 data transmission negative
PCIe_TX7_P	MGTYTXP0_226	AN9	PCIe channel 7 data transmission positive
PCIe_TX7_N	MGTYTXN0_226	AN8	PCIe channel 7 data transmission negative
PCIe_TX8_P	MGTYTXP3_225	AP7	PCIe channel 8 data transmission positive
PCIe_TX8_N	MGTYTXN3_225	AP6	PCIe channel 8 data transmission negative
PCIe_TX9_P	MGTYTXP2_225	AR9	PCIe channel 9 data transmission positive
PCIe_TX9_N	MGTYTXN2_225	AR8	PCIe channel 9 data transmission negative
PCIe_TX10_P	MGTYTXP1_225	AT7	PCIe channel 10 data transmission positive
PCIe_TX10_N	MGTYTXN1_225	AT6	PCIe channel 10 data transmission negative
PCIe_TX11_P	MGTYTXP0_225	AU9	PCIe channel 11 data transmission positive
PCIe_TX11_N	MGTYTXN0_225	AU8	PCIe channel 11 data transmission negative
PCIe_TX12_P	MGTYTXP3_224	AV7	PCIe channel 12 data transmission positive
PCIe_TX12_N	MGTYTXN3_224	AV6	PCIe channel 12 data transmission negative
PCIe_TX13_P	MGTYTXP2_224	BB5	PCIe channel 13 data transmission positive
PCIe_TX13_N	MGTYTXN2_224	BB4	PCIe channel 13 data transmission negative
PCIe_TX14_P	MGTYTXP1_224	BD5	PCIe channel 14 data transmission positive
PCIe_TX14_N	MGTYTXN1_224	BD4	PCIe channel 14 data transmission negative
PCIe_TX15_P	MGTYTXP0_224	BF5	PCIe channel 15 data transmission positive
PCIe_TX15_N	MGTYTXN0_224	BF4	PCIe channel 15 data transmission negative
PCIe_CLK1_P	MGTREFCLK0P_225	AT11	PCIe channel reference CLK positive
PCIe_CLK1_N	MGTREFCLK0N_225	AT10	PCIe channel reference CLK negative
PCIe_CLK2_P	MGTREFCLK0P_227	AH11	PCIe channel reference CLK positive
PCIe_CLK2_N	MGTREFCLK0N_227	AH10	PCIe channel reference CLK negative
FPGA_PCIe_PERST_n	IO_T3U_N12_PERSTN0_65	AR26	PCIe Reset Signal

Table 5: PCIe x16 Interface FPGA PIN assignment

7 FMC & Interface

7.1 FMC1 + (J9) Schematic Diagram

The development board features three FMC+ expansion ports, specifically FMC1+ (J9), FMC2+ (J8), and FMC3+ (J7). These ports can connect to various FMC+ and FMC modules from XILINX or our Alinx, including HDMI input/output modules, stereo camera modules, and high-speed AD modules, among others.

The FMC1+ port includes 34 pairs of LA differential signals, 2 pairs of clock signals, and 24 pairs of HA signals, which are connected to the FPGA chip's BANK64, BANK66, and BANK67 respectively, with a default voltage standard of 1.8V. Additionally, 20 high-speed GTY transceiver signals are connected to the IO of the FPGA chip's BANK124, BANK125, BANK126, BANK127, and BANK128.

The schematic diagram of the connection between the FPGA and the FMC1+ connector is shown in Figure 9.

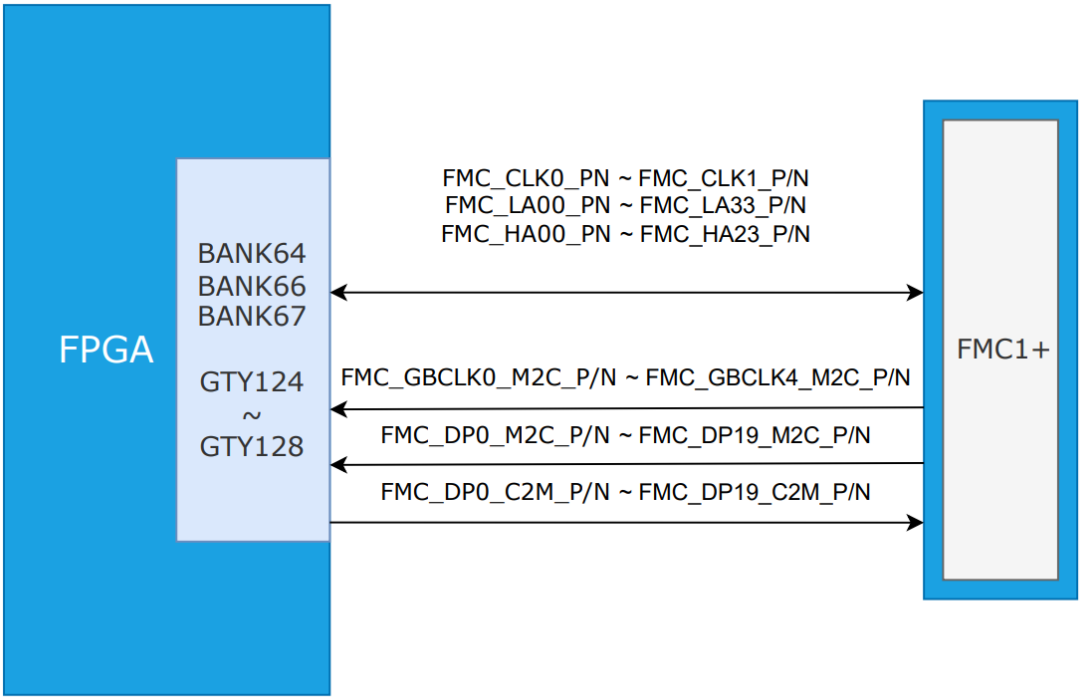

Figure 9: FMC1 + (J9) Schematic diagram

7.2 FMC1 + (J9) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC1_CLK0_N	IO_L12N_T1U_N11_GC_67	BA13	FMC channel 0 input reference CLK N
FMC1_CLK0_P	IO_L12P_T1U_N10_GC_67	AY13	FMC channel 0 input reference CLK P
FMC1_CLK1_N	IO_L12N_T1U_N11_GC_66	AW19	FMC channel 1 input reference CLK N
FMC1_CLK1_P	IO_L12P_T1U_N10_GC_66	AV19	FMC channel 1 input reference CLK P
FMC1_LA00_CC_N	IO_L14N_T2L_N3_GC_67	AW15	FMC LA channel 0 data (CLK) N
FMC1_LA00_CC_P	IO_L14P_T2L_N2_GC_67	AW16	FMC LA channel 0 data (CLK) P
FMC1_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_67	AW13	FMC LA channel 1 data (CLK) N
FMC1_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_67	AW14	FMC LA channel 1 data (CLK) P
FMC1_LA02_N	IO_L16N_T2U_N7_QBC_AD3N_67	AV14	FMC LA channel 2 data N
FMC1_LA02_P	IO_L16P_T2U_N6_QBC_AD3P_67	AU14	FMC LA channel 2 data P
FMC1_LA03_N	IO_L6N_T0U_N11_AD6N_67	BC13	FMC LA channel 3 data N
FMC1_LA03_P	IO_L6P_T0U_N10_AD6P_67	BC14	FMC LA channel 3 data P
FMC1_LA04_N	IO_L15N_T2L_N5_AD11N_67	AV13	FMC LA channel 4 data N
FMC1_LA04_P	IO_L15P_T2L_N4_AD11P_67	AU13	FMC LA channel 4 data P
FMC1_LA05_N	IO_L17N_T2U_N9_AD10N_67	AU15	FMC LA channel 5 data N
FMC1_LA05_P	IO_L17P_T2U_N8_AD10P_67	AT15	FMC LA channel 5 data P
FMC1_LA06_N	IO_L4N_T0U_N7_DBC_AD7N_67	BE13	FMC LA channel 6 data P
FMC1_LA06_P	IO_L4P_T0U_N6_DBC_AD7P_67	BD13	FMC LA channel 6 data P
FMC1_LA07_N	IO_L3N_T0L_N5_AD15N_67	BE16	FMC LA channel 7 data N
FMC1_LA07_P	IO_L3P_T0L_N4_AD15P_67	BD16	FMC LA channel 7 data P
FMC1_LA08_N	IO_L2N_T0L_N3_67	BF15	FMC LA channel 8 data N
FMC1_LA08_P	IO_L2P_T0L_N2_67	BE15	FMC LA channel 8 data P
FMC1_LA09_N	IO_L5N_T0U_N9_AD14N_67	BD14	FMC LA channel 9 data N
FMC1_LA09_P	IO_L5P_T0U_N8_AD14P_67	BD15	FMC LA channel 9 data P
FMC1_LA10_N	IO_L10N_T1U_N7_QBC_AD4N_67	BB14	FMC LA channel 10 data N
FMC1_LA10_P	IO_L10P_T1U_N6_QBC_AD4P_67	BB15	FMC LA channel 10 data P
FMC1_LA11_N	IO_L20N_T3L_N3_AD1N_67	AP14	FMC LA channel 11 data N
FMC1_LA11_P	IO_L20P_T3L_N2_AD1P_67	AP15	FMC LA channel 11 data P
FMC1_LA12_N	IO_L1N_T0L_N1_DBC_67	BF13	FMC LA channel 12 data N
FMC1_LA12_P	IO_L1P_T0L_N0_DBC_67	BF14	FMC LA channel 12 data P
FMC1_LA13_N	IO_L22N_T3U_N7_DBC_AD0N_67	AR13	FMC LA channel 13 data N
FMC1_LA13_P	IO_L22P_T3U_N6_DBC_AD0P_67	AP13	FMC LA channel 13 data P
FMC1_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_67	AR15	FMC LA channel 14 data N
FMC1_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_67	AR16	FMC LA channel 14 data P
FMC1_LA15_N	IO_L23N_T3U_N9_67	AM15	FMC LA channel 15 data N
FMC1_LA15_P	IO_L23P_T3U_N8_67	AL15	FMC LA channel 15 data P
FMC1_LA16_N	IO_L21N_T3L_N5_AD8N_67	AN13	FMC LA channel 16 data N
FMC1_LA16_P	IO_L21P_T3L_N4_AD8P_67	AN14	FMC LA channel 16 data P
FMC1_LA17_CC_N	IO_L14N_T2L_N3_GC_66	AU20	FMC LA channel 17 data (CLK) N

FMC1_LA17_CC_P	IO_L14P_T2L_N2_GC_66	AT20	FMC LA channel 17 data (CLK) P
FMC1_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_66	AU19	FMC LA channel 18 data (CLK) N
FMC1_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_66	AT19	FMC LA channel 18 data (CLK) P
FMC1_LA19_N	IO_L7N_T1L_N1_QBC_AD13N_66	BA17	FMC LA channel 19 data N
FMC1_LA19_P	IO_L7P_T1L_N0_QBC_AD13P_66	AY17	FMC LA channel 19 data P
FMC1_LA20_N	IO_L15N_T2L_N5_AD11N_66	AU17	FMC LA channel 20 data N
FMC1_LA20_P	IO_L15P_T2L_N4_AD11P_66	AT18	FMC LA channel 20 data P
FMC1_LA21_N	IO_L4N_T0U_N7_DBC_AD7N_66	BD19	FMC LA channel 21 data N
FMC1_LA21_P	IO_L4P_T0U_N6_DBC_AD7P_66	BC19	FMC LA channel 21 data P
FMC1_LA22_N	IO_L2N_T0L_N3_66	BF18	FMC LA channel 22 data N
FMC1_LA22_P	IO_L2P_T0L_N2_66	BF19	FMC LA channel 22 data P
FMC1_LA23_N	IO_L3N_T0L_N5_AD15N_66	BE18	FMC LA channel 23 data N
FMC1_LA23_P	IO_L3P_T0L_N4_AD15P_66	BD18	FMC LA channel 23 data P
FMC1_LA24_N	IO_L16N_T2U_N7_QBC_AD3N_66	AT17	FMC LA channel 24 data N
FMC1_LA24_P	IO_L16P_T2U_N6_QBC_AD3P_66	AR17	FMC LA channel 24 data P
FMC1_LA25_N	IO_L9N_T1L_N5_AD12N_66	AY20	FMC LA channel 25 data N
FMC1_LA25_P	IO_L9P_T1L_N4_AD12P_66	AW20	FMC LA channel 25 data P
FMC1_LA26_N	IO_L1N_T0L_N1_DBC_66	BF17	FMC LA channel 26 data N
FMC1_LA26_P	IO_L1P_T0L_N0_DBC_66	BE17	FMC LA channel 26 data P
FMC1_LA27_N	IO_L5N_T0U_N9_AD14N_66	BC17	FMC LA channel 27 data N
FMC1_LA27_P	IO_L5P_T0U_N8_AD14P_66	BB17	FMC LA channel 27 data P
FMC1_LA28_N	IO_L17N_T2U_N9_AD10N_66	AR18	FMC LA channel 28 data N
FMC1_LA28_P	IO_L17P_T2U_N8_AD10P_66	AP18	FMC LA channel 28 data P
FMC1_LA29_N	IO_L19N_T3L_N1_DBC_AD9N_66	AN17	FMC LA channel 29 data N
FMC1_LA29_P	IO_L19P_T3L_N0_DBC_AD9P_66	AN18	FMC LA channel 29 data P
FMC1_LA30_N	IO_L20N_T3L_N3_AD1N_66	AP19	FMC LA channel 30 data N
FMC1_LA30_P	IO_L20P_T3L_N2_AD1P_66	AN19	FMC LA channel 30 data P
FMC1_LA31_N	IO_L23N_T3U_N9_66	AM19	FMC LA channel 31 data N
FMC1_LA31_P	IO_L23P_T3U_N8_66	AL19	FMC LA channel 31 data P
FMC1_LA32_N	IO_L22N_T3U_N7_DBC_AD0N_66	AM17	FMC LA channel 32 data N
FMC1_LA32_P	IO_L22P_T3U_N6_DBC_AD0P_66	AL17	FMC LA channel 32 data P
FMC1_LA33_N	IO_L21N_T3L_N5_AD8N_66	AN16	FMC LA channel 33 data N
FMC1_LA33_P	IO_L21P_T3L_N4_AD8P_66	AM16	FMC LA channel 33 data P
FMC1_SCL	IO_L8P_T1L_N2_AD5P_67	AY12	FMC I2C bus CLK
FMC1_SDA	IO_L8N_T1L_N3_AD5N_67	AY11	FMC I2C bus data
FMC1_HA00_CC_N	IO_L14N_T2L_N3_GC_64	AW24	FMC HA channel 0 data (CLK) N
FMC1_HA00_CC_P	IO_L14P_T2L_N2_GC_64	AV24	FMC HA channel 0 data (CLK) P
FMC1_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_64	AW23	FMC HA channel 1 data (CLK) N
FMC1_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_64	AV23	FMC HA channel 1 data (CLK) P
FMC1_HA02_N	IO_L7N_T1L_N1_QBC_AD13N_64	BB20	FMC HA channel 2 data N
FMC1_HA02_P	IO_L7P_T1L_N0_QBC_AD13P_64	BA20	FMC HA channel 2 data P

FMC1_HA03_N	IO_L5N_T0U_N9_AD14N_64	BE21	FMC HA channel 3 data N
FMC1_HA03_P	IO_L5P_T0U_N8_AD14P_64	BD21	FMC HA channel 3 data N
FMC1_HA04_N	IO_L2N_T0L_N3_64	BE23	FMC HA channel 4 data N
FMC1_HA04_P	IO_L2P_T0L_N2_64	BD23	FMC HA channel 4 data P
FMC1_HA05_N	IO_L4N_T0U_N7_DBC_AD7N_64	BF22	FMC HA channel 5 data N
FMC1_HA05_P	IO_L4P_T0U_N6_DBC_AD7P_64	BE22	FMC HA channel 5 data P
FMC1_HA06_N	IO_L3N_T0L_N5_AD15N_64	BD24	FMC HA channel 6 data N
FMC1_HA06_P	IO_L3P_T0L_N4_AD15P_64	BC24	FMC HA channel 6 data P
FMC1_HA07_N	IO_L1N_T0L_N1_DBC_64	BF23	FMC HA channel 7 data N
FMC1_HA07_P	IO_L1P_T0L_N0_DBC_64	BF24	FMC HA channel 7 data P
FMC1_HA08_N	IO_L6N_T0U_N11_AD6N_64	BE20	FMC HA channel 8 data N
FMC1_HA08_P	IO_L6P_T0U_N10_AD6P_64	BD20	FMC HA channel 8 data P
FMC1_HA09_N	IO_L15N_T2L_N5_AD11N_64	AV22	FMC HA channel 9 data N
FMC1_HA09_P	IO_L15P_T2L_N4_AD11P_64	AU22	FMC HA channel 9 data P
FMC1_HA10_N	IO_L16N_T2U_N7_QBC_AD3N_64	AT22	FMC HA channel 10 data N
FMC1_HA10_P	IO_L16P_T2U_N6_QBC_AD3P_64	AR22	FMC HA channel 10 data P
FMC1_HA11_N	IO_L17N_T2U_N9_AD10N_64	AT23	FMC HA channel 11 data N
FMC1_HA11_P	IO_L17P_T2U_N8_AD10P_64	AR23	FMC HA channel 11 data P
FMC1_HA12_N	IO_L18N_T2U_N11_AD2N_64	AU24	FMC HA channel 12 data N
FMC1_HA12_P	IO_L18P_T2U_N10_AD2P_64	AT24	FMC HA channel 12 data P
FMC1_HA13_N	IO_L10N_T1U_N7_QBC_AD4N_64	BB24	FMC HA channel 13 data N
FMC1_HA13_P	IO_L10P_T1U_N6_QBC_AD4P_64	BA24	FMC HA channel 13 data P
FMC1_HA14_N	IO_L21N_T3L_N5_AD8N_64	AP24	FMC HA channel 14 data N
FMC1_HA14_P	IO_L21P_T3L_N4_AD8P_64	AN24	FMC HA channel 14 data P
FMC1_HA15_N	IO_L8N_T1L_N3_AD5N_64	BC21	FMC HA channel 15 data N
FMC1_HA15_P	IO_L8P_T1L_N2_AD5P_64	BB21	FMC HA channel 15 data P
FMC1_HA16_N	IO_L9N_T1L_N5_AD12N_64	BC22	FMC HA channel 16 data N
FMC1_HA16_P	IO_L9P_T1L_N4_AD12P_64	BB22	FMC HA channel 16 data P
FMC1_HA17_CC_N	IO_L12N_T1U_N11_GC_64	BA23	FMC HA channel 17 data (CLK) N
FMC1_HA17_CC_P	IO_L12P_T1U_N10_GC_64	AY23	FMC HA channel 17 data (CLK) P
FMC1_HA18_N	IO_L20N_T3L_N3_AD1N_64	AP23	FMC HA channel 18 data N
FMC1_HA18_P	IO_L20P_T3L_N2_AD1P_64	AN23	FMC HA channel 18 data P
FMC1_HA19_N	IO_L11N_T1U_N9_GC_64	BA22	FMC HA channel 19 data N
FMC1_HA19_P	IO_L11P_T1U_N8_GC_64	AY22	FMC HA channel 19 data P
FMC1_HA20_N	IO_L22N_T3U_N7_DBC_AD0N_64	AM24	FMC HA channel 20 data N
FMC1_HA20_P	IO_L22P_T3U_N6_DBC_AD0P_64	AL24	FMC HA channel 20 data P
FMC1_HA21_N	IO_L19N_T3L_N1_DBC_AD9N_64	AN21	FMC HA channel 21 data N
FMC1_HA21_P	IO_L19P_T3L_N0_DBC_AD9P_64	AN22	FMC HA channel 21 data P
FMC1_HA22_N	IO_L23N_T3U_N9_64	AM22	FMC HA channel 22 data N
FMC1_HA22_P	IO_L23P_T3U_N8_64	AL22	FMC HA channel 22 data P
FMC1_HA23_N	IO_L24N_T3U_N11_64	AM21	FMC HA channel 23 data N

FMC1_HA23_P	IO_L24P_T3U_N10_64	AL21	FMC HA channel 23 data P
FMC1_DP0_M2C_P	MGTYRXP0_124	BC45	Transceiver data 0 input P
FMC1_DP0_M2C_N	MGTYRXN0_124	BC46	Transceiver data 0 input N
FMC1_DP1_M2C_P	MGTYRXP1_124	BA45	Transceiver data 1 input P
FMC1_DP1_M2C_N	MGTYRXN1_124	BA46	Transceiver data 1 input N
FMC1_DP2_M2C_P	MGTYRXP2_124	AW45	Transceiver data 2 input P
FMC1_DP2_M2C_N	MGTYRXN2_124	AW46	Transceiver data 2 input N
FMC1_DP3_M2C_P	MGTYRXP3_124	AV43	Transceiver data 3 input P
FMC1_DP3_M2C_N	MGTYRXN3_124	AV44	Transceiver data 3 input N
FMC1_DP4_M2C_P	MGTYRXP1_127	AH43	Transceiver data 4 input P
FMC1_DP4_M2C_N	MGTYRXN1_127	AH44	Transceiver data 4 input N
FMC1_DP5_M2C_P	MGTYRXP3_127	AF43	Transceiver data 5 input P
FMC1_DP5_M2C_N	MGTYRXN3_127	AF44	Transceiver data 5 input N
FMC1_DP6_M2C_P	MGTYRXP2_127	AG45	Transceiver data 6 input P
FMC1_DP6_M2C_N	MGTYRXN2_127	AG46	Transceiver data 6 input N
FMC1_DP7_M2C_P	MGTYRXP0_127	AJ45	Transceiver data 7 input P
FMC1_DP7_M2C_N	MGTYRXN0_127	AJ46	Transceiver data 7 input N
FMC1_DP8_M2C_P	MGTYRXP2_125	AR45	Transceiver data 8 input P
FMC1_DP8_M2C_N	MGTYRXN2_125	AR46	Transceiver data 8 input N
FMC1_DP9_M2C_P	MGTYRXP1_125	AT43	Transceiver data 9 input P
FMC1_DP9_M2C_N	MGTYRXN1_125	AT44	Transceiver data 9 input N
FMC1_DP10_M2C_P	MGTYRXP0_125	AU45	Transceiver data 10 input P
FMC1_DP10_M2C_N	MGTYRXN0_125	AU46	Transceiver data 10 input N
FMC1_DP11_M2C_P	MGTYRXP3_125	AP43	Transceiver data 11 input P
FMC1_DP11_M2C_N	MGTYRXN3_125	AP44	Transceiver data 11 input N
FMC1_DP12_M2C_P	MGTYRXP0_126	AN45	Transceiver data 12 input P
FMC1_DP12_M2C_N	MGTYRXN0_126	AN46	Transceiver data 12 input N
FMC1_DP13_M2C_P	MGTYRXP1_126	AM43	Transceiver data 13 input P
FMC1_DP13_M2C_N	MGTYRXN1_126	AM44	Transceiver data 13 input N
FMC1_DP14_M2C_P	MGTYRXP2_126	AL45	Transceiver data 14 input P
FMC1_DP14_M2C_N	MGTYRXN2_126	AL46	Transceiver data 14 input N
FMC1_DP15_M2C_P	MGTYRXP3_126	AK43	Transceiver data 15 input P
FMC1_DP15_M2C_N	MGTYRXN3_126	AK44	Transceiver data 15 input N
FMC1_DP16_M2C_P	MGTYRXP0_128	AE45	Transceiver data 16 input P
FMC1_DP16_M2C_N	MGTYRXN0_128	AE46	Transceiver data 16 input N
FMC1_DP17_M2C_P	MGTYRXP1_128	AD43	Transceiver data 17 input P
FMC1_DP17_M2C_N	MGTYRXN1_128	AD44	Transceiver data 17 input N
FMC1_DP18_M2C_P	MGTYRXP2_128	AC45	Transceiver data 18 input P
FMC1_DP18_M2C_N	MGTYRXN2_128	AC46	Transceiver data 18 input N
FMC1_DP19_M2C_P	MGTYRXP3_128	AB43	Transceiver data 19 input P
FMC1_DP19_M2C_N	MGTYRXN3_128	AB44	Transceiver data 19 input N

FMC1_DP0_C2M_P	MGTYTXP0_124	BF42	Transceiver data 0 output P
FMC1_DP0_C2M_N	MGTYTXN0_124	BF43	Transceiver data 0 output N
FMC1_DP1_C2M_P	MGTYTXP1_124	BD42	Transceiver data 1 output P
FMC1_DP1_C2M_N	MGTYTXN1_124	BD43	Transceiver data 1 output N
FMC1_DP2_C2M_P	MGTYTXP2_124	BB42	Transceiver data 2 output P
FMC1_DP2_C2M_N	MGTYTXN2_124	BB43	Transceiver data 2 output N
FMC1_DP3_C2M_P	MGTYTXP3_124	AW40	Transceiver data 3 output P
FMC1_DP3_C2M_N	MGTYTXN3_124	AW41	Transceiver data 3 output N
FMC1_DP4_C2M_P	MGTYTXP1_127	AH38	Transceiver data 4 output P
FMC1_DP4_C2M_N	MGTYTXN1_127	AH39	Transceiver data 4 output N
FMC1_DP5_C2M_P	MGTYTXP3_127	AF38	Transceiver data 5 output P
FMC1_DP5_C2M_N	MGTYTXN3_127	AF39	Transceiver data 5 output N
FMC1_DP6_C2M_P	MGTYTXP2_127	AG40	Transceiver data 6 output P
FMC1_DP6_C2M_N	MGTYTXN2_127	AG41	Transceiver data 6 output N
FMC1_DP7_C2M_P	MGTYTXP0_127	AJ40	Transceiver data 7 output P
FMC1_DP7_C2M_N	MGTYTXN0_127	AJ41	Transceiver data 7 output N
FMC1_DP8_C2M_P	MGTYTXP2_125	AR40	Transceiver data 8 output P
FMC1_DP8_C2M_N	MGTYTXN2_125	AR41	Transceiver data 8 output N
FMC1_DP9_C2M_P	MGTYTXP1_125	AT38	Transceiver data 9 output P
FMC1_DP9_C2M_N	MGTYTXN1_125	AT39	Transceiver data 9 output N
FMC1_DP10_C2M_P	MGTYTXP0_125	AU40	Transceiver data 10 output P
FMC1_DP10_C2M_N	MGTYTXN0_125	AU41	Transceiver data 10 output N
FMC1_DP11_C2M_P	MGTYTXP3_125	AP38	Transceiver data 11 output P
FMC1_DP11_C2M_N	MGTYTXN3_125	AP39	Transceiver data 11 output N
FMC1_DP12_C2M_P	MGTYTXP0_126	AN40	Transceiver data 12 output P
FMC1_DP12_C2M_N	MGTYTXN0_126	AN41	Transceiver data 12 output N
FMC1_DP13_C2M_P	MGTYTXP1_126	AM38	Transceiver data 13 output P
FMC1_DP13_C2M_N	MGTYTXN1_126	AM39	Transceiver data 13 output N
FMC1_DP14_C2M_P	MGTYTXP2_126	AL40	Transceiver data 14 output P
FMC1_DP14_C2M_N	MGTYTXN2_126	AL41	Transceiver data 14 output N
FMC1_DP15_C2M_P	MGTYTXP3_126	AK38	Transceiver data 15 output P
FMC1_DP15_C2M_N	MGTYTXN3_126	AK39	Transceiver data 15 output N
FMC1_DP16_C2M_P	MGTYTXP0_128	AE40	Transceiver data 16 output P
FMC1_DP16_C2M_N	MGTYTXN0_128	AE41	Transceiver data 16 output N
FMC1_DP17_C2M_P	MGTYTXP1_128	AD38	Transceiver data 17 output P
FMC1_DP17_C2M_N	MGTYTXN1_128	AD39	Transceiver data 17 output N
FMC1_DP18_C2M_P	MGTYTXP2_128	AC40	Transceiver data 18 output P
FMC1_DP18_C2M_N	MGTYTXN2_128	AC41	Transceiver data 18 output N
FMC1_DP19_C2M_P	MGTYTXP3_128	AB38	Transceiver data 19 output P
FMC1_DP19_C2M_N	MGTYTXN3_128	AB39	Transceiver data 19 output N
FMC1_GBT1_0_M2C_C_N	MGTREFCLK1N_127	AJ37	Transceiver reference CLK 1 input N

FMC1_GBT1_0_M2C_C_P	MGTREFCLK1P_127	AJ36	Transceiver reference CLK 1 input P
FMC1_GBT1_1_M2C_C_N	MGTREFCLK1N_124	AY39	Transceiver reference CLK 1 input N
FMC1_GBT1_1_M2C_C_P	MGTREFCLK1P_124	AY38	Transceiver reference CLK 1 input P
FMC1_GBT1_2_M2C_C_N	MGTREFCLK1N_125	AU37	Transceiver reference CLK 1 input N
FMC1_GBT1_2_M2C_C_P	MGTREFCLK1P_125	AU36	Transceiver reference CLK 1 input P
FMC1_GBT1_3_M2C_C_N	MGTREFCLK1N_126	AN37	Transceiver reference CLK 1 input N
FMC1_GBT1_3_M2C_C_P	MGTREFCLK1P_126	AN36	Transceiver reference CLK 1 input P
FMC1_GBT1_4_M2C_C_N	MGTREFCLK1N_128	AE37	Transceiver reference CLK 1 input N
FMC1_GBT1_4_M2C_C_P	MGTREFCLK1P_128	AE36	Transceiver reference CLK 1 input P
FMC1_GBT0_0_M2C_C_N	MGTREFCLK0N_124	BA41	Transceiver reference CLK 0 input N
FMC1_GBT0_0_M2C_C_P	MGTREFCLK0P_124	BA40	Transceiver reference CLK 0 input P
FMC1_GBTCLK2_M2C_C_N	MGTREFCLK0N_125	AV39	Transceiver reference CLK 0 input N
FMC1_GBTCLK2_M2C_C_P	MGTREFCLK0P_125	AV38	Transceiver reference CLK 0 input P
FMC1_GBTCLK3_M2C_C_N	MGTREFCLK0N_126	AR37	Transceiver reference CLK 0 input N
FMC1_GBTCLK3_M2C_C_P	MGTREFCLK0P_126	AR36	Transceiver reference CLK 0 input P
FMC1_GBTCLK4_M2C_C_N	MGTREFCLK0N_128	AG37	Transceiver reference CLK 0 input N
FMC1_GBTCLK4_M2C_C_P	MGTREFCLK0P_128	AG36	Transceiver reference CLK 0 input P
FMC1_H_PRSNT_M2C_B	IO_L7P_T1L_N0_QBC_AD13P_67	BA12	Reset PIN
FMC1_L_PRSNT_M2C_B	IO_T1U_N12_67	BB16	Reset PIN
FMC1_PG_C2M	IO_L7N_T1L_N1_QBC_AD13N_67	BB12	Power status PIN
FMC1_PG_M2C	IO_T1U_N12_66	AV17	Power status PIN
FMC1_REFCLK_C2M_N	IO_L18N_T2U_N11_AD2N_67	AV16	Reference CLK 1 output N
FMC1_REFCLK_C2M_P	IO_L18P_T2U_N10_AD2P_67	AU16	Reference CLK 1 output P
FMC1_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_67	BA14	Reference CLK 1 input N
FMC1_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_67	BA15	Reference CLK 1 input P
FMC1_SYNC_C2M_N	IO_L24N_T3U_N11_67	AM14	C2M SYNC output N
FMC1_SYNC_C2M_P	IO_L24P_T3U_N10_67	AL14	C2M SYNC output P
FMC1_SYNC_M2C_N	IO_L9N_T1L_N5_AD12N_67	AY15	M2C SYNC input N
FMC1_SYNC_M2C_P	IO_L9P_T1L_N4_AD12P_67	AY16	M2C SYNC input P
FMC1_GBT0_1_M2C_C_N	MGTREFCLK0N_127	AL37	Reference CLK 0 input N
FMC1_GBT0_1_M2C_C_P	MGTREFCLK0P_127	AL36	Reference CLK 0 input P

Table 6: FMC1 + (J9) Connector PIN assignment

7.3 FMC2 + (J8) Schematic Diagram

The FMC2 + expansion port includes 34 pairs of LA differential signals, 2 pairs of clock signals, and 24 pairs of HA signals, which are connected to the FPGA chip's BANK65, BANK69, and BANK70 respectively, with a default voltage standard of 1.8V. Additionally, 16 high-speed GTY transceiver signals are connected to the IO of the FPGA chip's BANK129, BANK130, BANK131, and BANK133.

Figure 10 shows the schematic diagram of the connection between the FPGA and the FMC2+ connector.

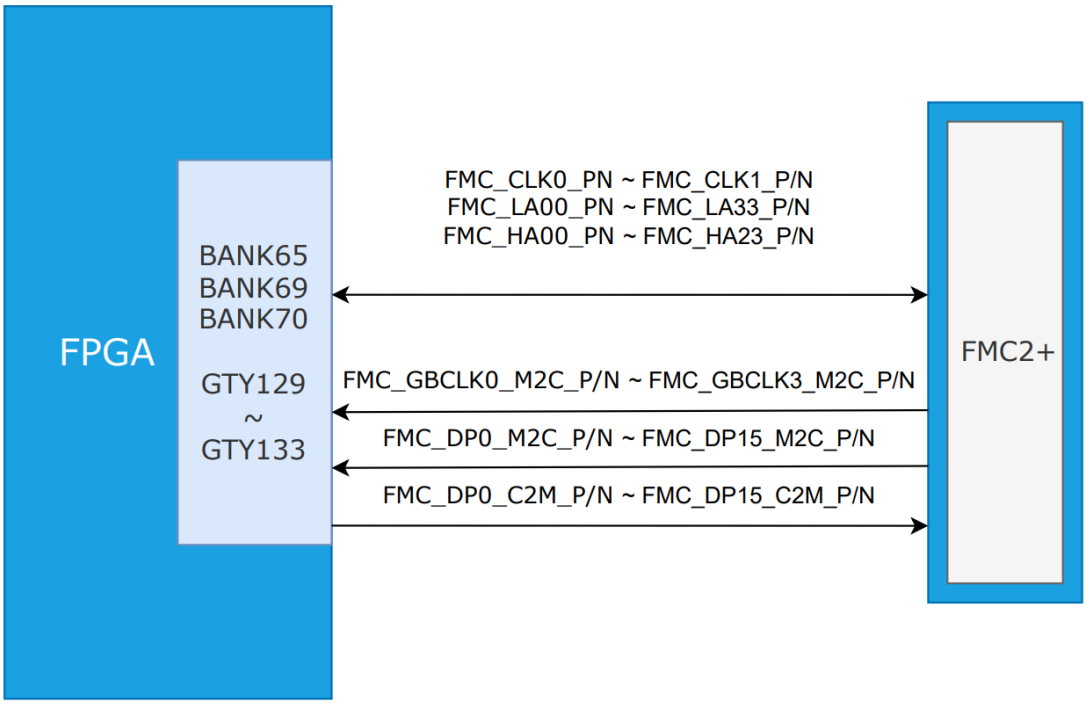

Figure 10: HPC FMC2+ (J8) schematic diagram

7.4 FMC2 + (J8) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC2_CLK0_M2C_N	IO_L12N_T1U_N11_GC_69	N33	FMC channel 0 input reference CLK N
FMC2_CLK0_M2C_P	IO_L12P_T1U_N10_GC_69	N32	FMC channel 0 input reference CLK P
FMC2_CLK1_M2C_N	IO_L12N_T1U_N11_GC_A09_D25_65	AY28	FMC channel 1 input reference CLK N
FMC2_CLK1_M2C_P	IO_L12P_T1U_N10_GC_A08_D24_65	AW28	FMC channel 1 input reference CLK P
FMC2_LA00_CC_N	IO_L14N_T2L_N3_GC_69	K32	FMC LA channel 0 data (CLK) N
FMC2_LA00_CC_P	IO_L14P_T2L_N2_GC_69	L32	FMC LA channel 0 data (CLK) P
FMC2_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_69	M32	FMC LA channel 1 data (CLK) N
FMC2_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_69	M31	FMC LA channel 1 data (CLK) P
FMC2_LA02_N	IO_L15N_T2L_N5_AD11N_69	L30	FMC LA channel 2 data N
FMC2_LA02_P	IO_L15P_T2L_N4_AD11P_69	M30	FMC LA channel 2 data P
FMC2_LA03_N	IO_L6N_T0U_N11_AD6N_69	T30	FMC LA channel 3 data N
FMC2_LA03_P	IO_L6P_T0U_N10_AD6P_69	U30	FMC LA channel 3 data P
FMC2_LA04_N	IO_L17N_T2U_N9_AD10N_69	J31	FMC LA channel 4 data N
FMC2_LA04_P	IO_L17P_T2U_N8_AD10P_69	K31	FMC LA channel 4 data P
FMC2_LA05_N	IO_L16N_T2U_N7_QBC_AD3N_69	J30	FMC LA channel 5 data N
FMC2_LA05_P	IO_L16P_T2U_N6_QBC_AD3P_69	K30	FMC LA channel 5 data P
FMC2_LA06_N	IO_L2N_T0L_N3_69	R33	FMC LA channel 6 data P
FMC2_LA06_P	IO_L2P_T0L_N2_69	T33	FMC LA channel 6 data P
FMC2_LA07_N	IO_L5N_T0U_N9_AD14N_69	U31	FMC LA channel 7 data N
FMC2_LA07_P	IO_L5P_T0U_N8_AD14P_69	V31	FMC LA channel 7 data P
FMC2_LA08_N	IO_L4N_T0U_N7_DBC_AD7N_69	V33	FMC LA channel 8 data N
FMC2_LA08_P	IO_L4P_T0U_N6_DBC_AD7P_69	V32	FMC LA channel 8 data P
FMC2_LA09_N	IO_L3N_T0L_N5_AD15N_69	T32	FMC LA channel 9 data N
FMC2_LA09_P	IO_L3P_T0L_N4_AD15P_69	U32	FMC LA channel 9 data P
FMC2_LA10_N	IO_L8N_T1L_N3_AD5N_69	R32	FMC LA channel 10 data N
FMC2_LA10_P	IO_L8P_T1L_N2_AD5P_69	R31	FMC LA channel 10 data P
FMC2_LA11_N	IO_L22N_T3U_N7_DBC_AD0N_69	H33	FMC LA channel 11 data N
FMC2_LA11_P	IO_L22P_T3U_N6_DBC_AD0P_69	J33	FMC LA channel 11 data P
FMC2_LA12_N	IO_L1N_T0L_N1_DBC_69	T34	FMC LA channel 12 data N
FMC2_LA12_P	IO_L1P_T0L_N0_DBC_69	U34	FMC LA channel 12 data P
FMC2_LA13_N	IO_L20N_T3L_N3_AD1N_69	G31	FMC LA channel 13 data N
FMC2_LA13_P	IO_L20P_T3L_N2_AD1P_69	H31	FMC LA channel 13 data P
FMC2_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_69	F30	FMC LA channel 14 data N
FMC2_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_69	G30	FMC LA channel 14 data P
FMC2_LA15_N	IO_L21N_T3L_N5_AD8N_69	G32	FMC LA channel 15 data N
FMC2_LA15_P	IO_L21P_T3L_N4_AD8P_69	H32	FMC LA channel 15 data P
FMC2_LA16_N	IO_L23N_T3U_N9_69	E32	FMC LA channel 16 data N
FMC2_LA16_P	IO_L23P_T3U_N8_69	F32	FMC LA channel 16 data P
FMC2_LA17_CC_N	IO_L14N_T2L_N3_GC_A05_D21_65	AV28	FMC LA channel 17 data (CLK) N

FMC2_LA17_CC_P	IO_L14P_T2L_N2_GC_A04_D20_65	AV27	FMC LA channel 17 data (CLK) P
FMC2_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_A07_D23_65	AW26	FMC LA channel 18 data (CLK) N
FMC2_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_A06_D22_65	AV26	FMC LA channel 18 data (CLK) P
FMC2_LA19_N	IO_L6N_T0U_N11_AD6N_A21_65	BC27	FMC LA channel 19 data N
FMC2_LA19_P	IO_L6P_T0U_N10_AD6P_A20_65	BC26	FMC LA channel 19 data P
FMC2_LA20_N	IO_L15N_T2L_N5_AD11N_A03_D19_65	AU27	FMC LA channel 20 data N
FMC2_LA20_P	IO_L15P_T2L_N4_AD11P_A02_D18_65	AU26	FMC LA channel 20 data P
FMC2_LA21_N	IO_L8N_T1L_N3_AD5N_A17_65	BB27	FMC LA channel 21 data N
FMC2_LA21_P	IO_L8P_T1L_N2_AD5P_A16_65	BB26	FMC LA channel 21 data P
FMC2_LA22_N	IO_L10N_T1U_N7_QBC_AD4N_A13_D29_65	AY25	FMC LA channel 22 data N
FMC2_LA22_P	IO_L10P_T1U_N6_QBC_AD4P_A12_D28_65	AW25	FMC LA channel 22 data P
FMC2_LA23_N	IO_L11N_T1U_N9_GC_A11_D27_65	AY27	FMC LA channel 23 data N
FMC2_LA23_P	IO_L11P_T1U_N8_GC_A10_D26_65	AY26	FMC LA channel 23 data P
FMC2_LA24_N	IO_L17N_T2U_N9_AD10N_D15_65	AT27	FMC LA channel 24 data N
FMC2_LA24_P	IO_L17P_T2U_N8_AD10P_D14_65	AR27	FMC LA channel 24 data P
FMC2_LA25_N	IO_L3N_T0L_N5_AD15N_A27_65	BE28	FMC LA channel 25 data N
FMC2_LA25_P	IO_L3P_T0L_N4_AD15P_A26_65	BD28	FMC LA channel 25 data P
FMC2_LA26_N	IO_L7N_T1L_N1_QBC_AD13N_A19_65	BB25	FMC LA channel 26 data N
FMC2_LA26_P	IO_L7P_T1L_N0_QBC_AD13P_A18_65	BA25	FMC LA channel 26 data P
FMC2_LA27_N	IO_L9N_T1L_N5_AD12N_A15_D31_65	BA28	FMC LA channel 27 data N
FMC2_LA27_P	IO_L9P_T1L_N4_AD12P_A14_D30_65	BA27	FMC LA channel 27 data P
FMC2_LA28_N	IO_L16N_T2U_N7_QBC_AD3N_A01_D17_65	AT25	FMC LA channel 28 data N
FMC2_LA28_P	IO_L16P_T2U_N6_QBC_AD3P_A00_D16_65	AR25	FMC LA channel 28 data P
FMC2_LA29_N	IO_L18N_T2U_N11_AD2N_D13_65	AT28	FMC LA channel 29 data N
FMC2_LA29_P	IO_L18P_T2U_N10_AD2P_D12_65	AR28	FMC LA channel 29 data P
FMC2_LA30_N	IO_L19N_T3L_N1_DBC_AD9N_D11_65	AP26	FMC LA channel 30 data N
FMC2_LA30_P	IO_L19P_T3L_N0_DBC_AD9P_D10_65	AP25	FMC LA channel 30 data P
FMC2_LA31_N	IO_L20N_T3L_N3_AD1N_D09_65	AP28	FMC LA channel 31 data N
FMC2_LA31_P	IO_L20P_T3L_N2_AD1P_D08_65	AN28	FMC LA channel 31 data P
FMC2_LA32_N	IO_L24N_T3U_N11_DOUT_CSO_B_65	AL28	FMC LA channel 32 data N
FMC2_LA32_P	IO_L24P_T3U_N10_EMCCLK_65	AL27	FMC LA channel 32 data P
FMC2_LA33_N	IO_L23N_T3U_N9_PERSTN1_I2C_SDA_65	AN27	FMC LA channel 33 data N
FMC2_LA33_P	IO_L23P_T3U_N8_I2C_SCLK_65	AM27	FMC LA channel 33 data P
FMC2_SCL	IO_T3U_N12_69	E31	FMC I2C bus CLK
FMC2_SDA	IO_T2U_N12_69	K34	FMC I2C bus data
FMC2_HA00_CC_N	IO_L14N_T2L_N3_GC_70	D36	FMC HA channel 0 data (CLK) N
FMC2_HA00_CC_P	IO_L14P_T2L_N2_GC_70	E36	FMC HA channel 0 data (CLK) P
FMC2_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_70	C37	FMC HA channel 1 data (CLK) N
FMC2_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_70	C36	FMC HA channel 1 data (CLK) P
FMC2_HA02_N	IO_L18N_T2U_N11_AD2N_70	D35	FMC HA channel 2 data N
FMC2_HA02_P	IO_L18P_T2U_N10_AD2P_70	E35	FMC HA channel 2 data P

FMC2_HA03_N	IO_L4N_T0U_N7_DBC_AD7N_70	G36	FMC HA channel 3 data N
FMC2_HA03_P	IO_L4P_T0U_N6_DBC_AD7P_70	H36	FMC HA channel 3 data N
FMC2_HA04_N	IO_L2N_T0L_N3_70	F37	FMC HA channel 4 data N
FMC2_HA04_P	IO_L2P_T0L_N2_70	G37	FMC HA channel 4 data P
FMC2_HA05_N	IO_L5N_T0U_N9_AD14N_70	G34	FMC HA channel 5 data N
FMC2_HA05_P	IO_L5P_T0U_N8_AD14P_70	H34	FMC HA channel 5 data P
FMC2_HA06_N	IO_L3N_T0L_N5_AD15N_70	J36	FMC HA channel 6 data N
FMC2_HA06_P	IO_L3P_T0L_N4_AD15P_70	J35	FMC HA channel 6 data P
FMC2_HA07_N	IO_L1N_T0L_N1_DBC_70	H38	FMC HA channel 7 data N
FMC2_HA07_P	IO_L1P_T0L_N0_DBC_70	H37	FMC HA channel 7 data P
FMC2_HA08_N	IO_L21N_T3L_N5_AD8N_70	C33	FMC HA channel 8 data N
FMC2_HA08_P	IO_L21P_T3L_N4_AD8P_70	D33	FMC HA channel 8 data P
FMC2_HA09_N	IO_L15N_T2L_N5_AD11N_70	A38	FMC HA channel 9 data N
FMC2_HA09_P	IO_L15P_T2L_N4_AD11P_70	A37	FMC HA channel 9 data P
FMC2_HA10_N	IO_L17N_T2U_N9_AD10N_70	A35	FMC HA channel 10 data N
FMC2_HA10_P	IO_L17P_T2U_N8_AD10P_70	B35	FMC HA channel 10 data P
FMC2_HA11_N	IO_L16N_T2U_N7_QBC_AD3N_70	B37	FMC HA channel 11 data N
FMC2_HA11_P	IO_L16P_T2U_N6_QBC_AD3P_70	B36	FMC HA channel 11 data P
FMC2_HA12_N	IO_L20N_T3L_N3_AD1N_70	C34	FMC HA channel 12 data N
FMC2_HA12_P	IO_L20P_T3L_N2_AD1P_70	D34	FMC HA channel 12 data P
FMC2_HA13_N	IO_L6N_T0U_N11_AD6N_70	F35	FMC HA channel 13 data N
FMC2_HA13_P	IO_L6P_T0U_N10_AD6P_70	F34	FMC HA channel 13 data P
FMC2_HA14_N	IO_L7N_T1L_N1_QBC_AD13N_70	D40	FMC HA channel 14 data N
FMC2_HA14_P	IO_L7P_T1L_N0_QBC_AD13P_70	E40	FMC HA channel 14 data P
FMC2_HA15_N	IO_L23N_T3U_N9_70	B32	FMC HA channel 15 data N
FMC2_HA15_P	IO_L23P_T3U_N8_70	C32	FMC HA channel 15 data P
FMC2_HA16_N	IO_L19N_T3L_N1_DBC_AD9N_70	A34	FMC HA channel 16 data N
FMC2_HA16_P	IO_L19P_T3L_N0_DBC_AD9P_70	B34	FMC HA channel 16 data P
FMC2_HA17_CC_N	IO_L12N_T1U_N11_GC_70	C39	FMC HA channel 17 data (CLK) N
FMC2_HA17_CC_P	IO_L12P_T1U_N10_GC_70	C38	FMC HA channel 17 data (CLK) P
FMC2_HA18_N	IO_L8N_T1L_N3_AD5N_70	D39	FMC HA channel 18 data N
FMC2_HA18_P	IO_L8P_T1L_N2_AD5P_70	E39	FMC HA channel 18 data P
FMC2_HA19_N	IO_L24N_T3U_N11_70	C31	FMC HA channel 19 data N
FMC2_HA19_P	IO_L24P_T3U_N10_70	D31	FMC HA channel 19 data P
FMC2_HA20_N	IO_L22N_T3U_N7_DBC_AD0N_70	A33	FMC HA channel 20 data N
FMC2_HA20_P	IO_L22P_T3U_N6_DBC_AD0P_70	A32	FMC HA channel 20 data P
FMC2_HA21_N	IO_L11N_T1U_N9_GC_70	D38	FMC HA channel 21 data N
FMC2_HA21_P	IO_L11P_T1U_N8_GC_70	E38	FMC HA channel 21 data P
FMC2_HA22_N	IO_L9N_T1L_N5_AD12N_70	A40	FMC HA channel 22 data N
FMC2_HA22_P	IO_L9P_T1L_N4_AD12P_70	B40	FMC HA channel 22 data P
FMC2_HA23_N	IO_L10N_T1U_N7_QBC_AD4N_70	A39	FMC HA channel 23 data N

FMC2_HA23_P	IO_L10P_T1U_N6_QBC_AD4P_70	B39	FMC HA channel 23 data P
FMC2_DP0_M2C_P	MGTYRXP0_129	AA45	Transceiver data 0 input P
FMC2_DP0_M2C_N	MGTYRXN0_129	AA46	Transceiver data 0 input N
FMC2_DP1_M2C_P	MGTYRXP3_129	V43	Transceiver data 1 input P
FMC2_DP1_M2C_N	MGTYRXN3_129	V44	Transceiver data 1 input N
FMC2_DP2_M2C_P	MGTYRXP2_129	W45	Transceiver data 2 input P
FMC2_DP2_M2C_N	MGTYRXN2_129	W46	Transceiver data 2 input N
FMC2_DP3_M2C_P	MGTYRXP1_129	Y43	Transceiver data 3 input P
FMC2_DP3_M2C_N	MGTYRXN1_129	Y44	Transceiver data 3 input N
FMC2_DP4_M2C_P	MGTYRXP2_133	F45	Transceiver data 4 input P
FMC2_DP4_M2C_N	MGTYRXN2_133	F46	Transceiver data 4 input N
FMC2_DP5_M2C_P	MGTYRXP0_133	J45	Transceiver data 5 input P
FMC2_DP5_M2C_N	MGTYRXN0_133	J46	Transceiver data 5 input N
FMC2_DP6_M2C_P	MGTYRXP1_133	H43	Transceiver data 6 input P
FMC2_DP6_M2C_N	MGTYRXN1_133	H44	Transceiver data 6 input N
FMC2_DP7_M2C_P	MGTYRXP3_133	D45	Transceiver data 7 input P
FMC2_DP7_M2C_N	MGTYRXN3_133	D46	Transceiver data 7 input N
FMC2_DP8_M2C_P	MGTYRXP2_130	R45	Transceiver data 8 input P
FMC2_DP8_M2C_N	MGTYRXN2_130	R46	Transceiver data 8 input N
FMC2_DP9_M2C_P	MGTYRXP0_130	U45	Transceiver data 9 input P
FMC2_DP9_M2C_N	MGTYRXN0_130	U46	Transceiver data 9 input N
FMC2_DP10_M2C_P	MGTYRXP1_130	T43	Transceiver data 10 input P
FMC2_DP10_M2C_N	MGTYRXN1_130	T44	Transceiver data 10 input N
FMC2_DP11_M2C_P	MGTYRXP3_130	P43	Transceiver data 11 input P
FMC2_DP11_M2C_N	MGTYRXN3_130	P44	Transceiver data 11 input N
FMC2_DP12_M2C_P	MGTYRXP0_131	N45	Transceiver data 12 input P
FMC2_DP12_M2C_N	MGTYRXN0_131	N46	Transceiver data 12 input N
FMC2_DP13_M2C_P	MGTYRXP1_131	M43	Transceiver data 13 input P
FMC2_DP13_M2C_N	MGTYRXN1_131	M44	Transceiver data 13 input N
FMC2_DP14_M2C_P	MGTYRXP2_131	L45	Transceiver data 14 input P
FMC2_DP14_M2C_N	MGTYRXN2_131	L46	Transceiver data 14 input N
FMC2_DP15_M2C_P	MGTYRXP3_131	K43	Transceiver data 15 input P
FMC2_DP15_M2C_N	MGTYRXN3_131	K44	Transceiver data 15 input N
FMC2_DP0_C2M_P	MGTYTXP0_129	AA40	Transceiver data 0 output P
FMC2_DP0_C2M_N	MGTYTXN0_129	AA41	Transceiver data 0 output N
FMC2_DP1_C2M_P	MGTYTXP3_129	V38	Transceiver data 1 output P
FMC2_DP1_C2M_N	MGTYTXN3_129	V39	Transceiver data 1 output N
FMC2_DP2_C2M_P	MGTYTXP2_129	W40	Transceiver data 2 output P
FMC2_DP2_C2M_N	MGTYTXN2_129	W41	Transceiver data 2 output N
FMC2_DP3_C2M_P	MGTYTXP1_129	Y38	Transceiver data 3 output P
FMC2_DP3_C2M_N	MGTYTXN1_129	Y39	Transceiver data 3 output N

FMC2_DP4_C2M_P	MGTYTXP2_133	C42	Transceiver data 4 output P
FMC2_DP4_C2M_N	MGTYTXN2_133	C43	Transceiver data 4 output N
FMC2_DP5_C2M_P	MGTYTXP0_133	G40	Transceiver data 5 output P
FMC2_DP5_C2M_N	MGTYTXN0_133	G41	Transceiver data 5 output N
FMC2_DP6_C2M_P	MGTYTXP1_133	E42	Transceiver data 6 output P
FMC2_DP6_C2M_N	MGTYTXN1_133	E43	Transceiver data 6 output N
FMC2_DP7_C2M_P	MGTYTXP3_133	A42	Transceiver data 7 output P
FMC2_DP7_C2M_N	MGTYTXN3_133	A43	Transceiver data 7 output N
FMC2_DP8_C2M_P	MGTYTXP2_130	R40	Transceiver data 8 output P
FMC2_DP8_C2M_N	MGTYTXN2_130	R41	Transceiver data 8 output N
FMC2_DP9_C2M_P	MGTYTXP0_130	U40	Transceiver data 9 output P
FMC2_DP9_C2M_N	MGTYTXN0_130	U41	Transceiver data 9 output N
FMC2_DP10_C2M_P	MGTYTXP1_130	T38	Transceiver data 10 output P
FMC2_DP10_C2M_N	MGTYTXN1_130	T39	Transceiver data 10 output N
FMC2_DP11_C2M_P	MGTYTXP3_130	P38	Transceiver data 11 output P
FMC2_DP11_C2M_N	MGTYTXN3_130	P39	Transceiver data 11 output N
FMC2_DP12_C2M_P	MGTYTXP0_131	N40	Transceiver data 12 output P
FMC2_DP12_C2M_N	MGTYTXN0_131	N41	Transceiver data 12 output N
FMC2_DP13_C2M_P	MGTYTXP1_131	M38	Transceiver data 13 output P
FMC2_DP13_C2M_N	MGTYTXN1_131	M39	Transceiver data 13 output N
FMC2_DP14_C2M_P	MGTYTXP2_131	L40	Transceiver data 14 output P
FMC2_DP14_C2M_N	MGTYTXN2_131	L41	Transceiver data 14 output N
FMC2_DP15_C2M_P	MGTYTXP3_131	J40	Transceiver data 15 output P
FMC2_DP15_C2M_N	MGTYTXN3_131	J41	Transceiver data 15 output N
FMC2_GBT1_0_M2C_C_N	MGTREFCLK1N_129	AA37	Transceiver reference CLK 1 input N
FMC2_GBT1_0_M2C_C_P	MGTREFCLK1P_129	AA36	Transceiver reference CLK 1 input P
FMC2_GBT1_1_M2C_C_N	MGTREFCLK1N_133	K39	Transceiver reference CLK 1 input N
FMC2_GBT1_1_M2C_C_P	MGTREFCLK1P_133	K38	Transceiver reference CLK 1 input P
FMC2_GBT1_2_M2C_C_N	MGTREFCLK1N_130	U37	Transceiver reference CLK 1 input N
FMC2_GBT1_2_M2C_C_P	MGTREFCLK1P_130	U36	Transceiver reference CLK 1 input P
FMC2_GBT1_3_M2C_C_N	MGTREFCLK1N_131	N37	Transceiver reference CLK 1 input N
FMC2_GBT1_3_M2C_C_P	MGTREFCLK1P_131	N36	Transceiver reference CLK 1 input P
FMC2_GBT0_0_M2C_C_N	MGTREFCLK0N_129	AC37	Transceiver reference CLK 0 input N
FMC2_GBT0_0_M2C_C_P	MGTREFCLK0P_129	AC36	Transceiver reference CLK 0 input P
FMC2_GBTCLK2_M2C_C_N	MGTREFCLK0N_130	W37	Transceiver reference CLK 0 input N
FMC2_GBTCLK2_M2C_C_P	MGTREFCLK0P_130	W36	Transceiver reference CLK 0 input P
FMC2_GBTCLK3_M2C_C_N	MGTREFCLK0N_131	R37	Transceiver reference CLK 0 input N
FMC2_GBTCLK3_M2C_C_P	MGTREFCLK0P_131	R36	Transceiver reference CLK 0 input P
FMC2_H_PRSNT_M2C_B	IO_T1U_N12_69	P33	Reset PIN
FMC2_L_PRSNT_M2C_B	IO_T3U_N12_70	B31	Reset PIN
FMC2_PG_C2M	IO_L9N_T1L_N5_AD12N_69	N34	Power status PIN

FMC2_PG_M2C	IO_L9P_T1L_N4_AD12P_69	P34	Power status PIN
FMC2_REFCLK_C2M_N	IO_L18N_T2U_N11_AD2N_69	K33	Reference CLK 1 output N
FMC2_REFCLK_C2M_P	IO_L18P_T2U_N10_AD2P_69	L33	Reference CLK 1 output P
FMC2_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_69	N31	Reference CLK 1 input N
FMC2_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_69	P31	Reference CLK 1 input P
FMC2_SYNC_C2M_N	IO_L24N_T3U_N11_69	E33	C2M SYNC output N
FMC2_SYNC_C2M_P	IO_L24P_T3U_N10_69	F33	C2M SYNC output P
FMC2_SYNC_M2C_N	IO_L7N_T1L_N1_QBC_AD13N_69	P30	M2C SYNC input N
FMC2_SYNC_M2C_P	IO_L7P_T1L_N0_QBC_AD13P_69	R30	M2C SYNC input P
FMC2_GBT0_1_M2C_C_N	MGTREFCLK0N_133	L37	Reference CLK 0 input N
FMC2_GBT0_1_M2C_C_P	MGTREFCLK0P_133	L36	Reference CLK 0 input P

Table 7: FMC2 + (J8) Connector PIN assignment

7.5 FMC3 + (J7) Schematic Diagram

The FMC3+ expansion port includes 34 pairs of LA differential signals, 2 pairs of clock signals, 24 pairs of HA signals, and 22 pairs of HB signals, which are connected to the FPGA chip's BANK71, BANK72, BANK73, and BANK74 respectively; the default voltage standard is 1.8V. Additionally, 24 high-speed GTY transceiver signals are connected to the IO of the FPGA chip's BANK228 through BANK233.

Figure 11 shows the schematic diagram of the connection between the FPGA and the FMC3+ connector.

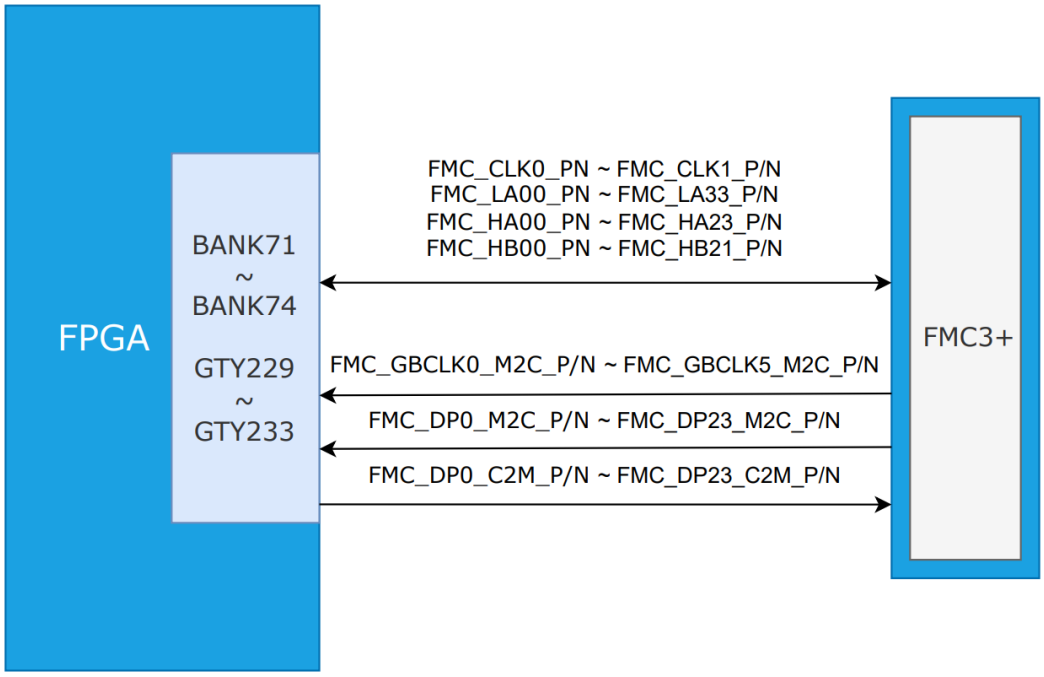

Figure 11: FMC3 + (J7) schematic diagram

7.6 FMC3 + (J7) Connector PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
FMC3_CLK0_N	IO_L12N_T1U_N11_GC_71	J29	FMC channel 0 input reference CLK N
FMC3_CLK0_P	IO_L12P_T1U_N10_GC_71	J28	FMC channel 0 input reference CLK P
FMC3_CLK1_N	IO_L12N_T1U_N11_GC_74	H24	FMC channel 1 input reference CLK N
FMC3_CLK1_P	IO_L12P_T1U_N10_GC_74	J24	FMC channel 1 input reference CLK P
FMC3_LA00_CC_N	IO_L14N_T2L_N3_GC_71	G27	FMC LA channel 0 data (CLK) N
FMC3_LA00_CC_P	IO_L14P_T2L_N2_GC_71	G26	FMC LA channel 0 data (CLK) P
FMC3_LA01_CC_N	IO_L13N_T2L_N1_GC_QBC_71	H26	FMC LA channel 1 data (CLK) N
FMC3_LA01_CC_P	IO_L13P_T2L_N0_GC_QBC_71	J26	FMC LA channel 1 data (CLK) P
FMC3_LA02_N	IO_L15N_T2L_N5_AD11N_71	G29	FMC LA channel 2 data N
FMC3_LA02_P	IO_L15P_T2L_N4_AD11P_71	H29	FMC LA channel 2 data P
FMC3_LA03_N	IO_L18N_T2U_N11_AD2N_71	D28	FMC LA channel 3 data N
FMC3_LA03_P	IO_L18P_T2U_N10_AD2P_71	E28	FMC LA channel 3 data P
FMC3_LA04_N	IO_L16N_T2U_N7_QBC_AD3N_71	F29	FMC LA channel 4 data N
FMC3_LA04_P	IO_L16P_T2U_N6_QBC_AD3P_71	F28	FMC LA channel 4 data P
FMC3_LA05_N	IO_L17N_T2U_N9_AD10N_71	E27	FMC LA channel 5 data N
FMC3_LA05_P	IO_L17P_T2U_N8_AD10P_71	F27	FMC LA channel 5 data P
FMC3_LA06_N	IO_L2N_T0L_N3_71	R27	FMC LA channel 6 data P
FMC3_LA06_P	IO_L2P_T0L_N2_71	T27	FMC LA channel 6 data P
FMC3_LA07_N	IO_L5N_T0U_N9_AD14N_71	N28	FMC LA channel 7 data N
FMC3_LA07_P	IO_L5P_T0U_N8_AD14P_71	P28	FMC LA channel 7 data P
FMC3_LA08_N	IO_L4N_T0U_N7_DBC_AD7N_71	N29	FMC LA channel 8 data N
FMC3_LA08_P	IO_L4P_T0U_N6_DBC_AD7P_71	P29	FMC LA channel 8 data P
FMC3_LA09_N	IO_L3N_T0L_N5_AD15N_71	R26	FMC LA channel 9 data N
FMC3_LA09_P	IO_L3P_T0L_N4_AD15P_71	T26	FMC LA channel 9 data P
FMC3_LA10_N	IO_L24N_T3U_N11_71	A30	FMC LA channel 10 data N
FMC3_LA10_P	IO_L24P_T3U_N10_71	B30	FMC LA channel 10 data P
FMC3_LA11_N	IO_L21N_T3L_N5_AD8N_71	D30	FMC LA channel 11 data N
FMC3_LA11_P	IO_L21P_T3L_N4_AD8P_71	E30	FMC LA channel 11 data P
FMC3_LA12_N	IO_L1N_T0L_N1_DBC_71	R28	FMC LA channel 12 data N
FMC3_LA12_P	IO_L1P_T0L_N0_DBC_71	T28	FMC LA channel 12 data P
FMC3_LA13_N	IO_L22N_T3U_N7_DBC_AD0N_71	A28	FMC LA channel 13 data N
FMC3_LA13_P	IO_L22P_T3U_N6_DBC_AD0P_71	A27	FMC LA channel 13 data P
FMC3_LA14_N	IO_L19N_T3L_N1_DBC_AD9N_71	B27	FMC LA channel 14 data N
FMC3_LA14_P	IO_L19P_T3L_N0_DBC_AD9P_71	C27	FMC LA channel 14 data P
FMC3_LA15_N	IO_L20N_T3L_N3_AD1N_71	C29	FMC LA channel 15 data N
FMC3_LA15_P	IO_L20P_T3L_N2_AD1P_71	D29	FMC LA channel 15 data P
FMC3_LA16_N	IO_L23N_T3U_N9_71	A29	FMC LA channel 16 data N
FMC3_LA16_P	IO_L23P_T3U_N8_71	B29	FMC LA channel 16 data P
FMC3_LA17_CC_N	IO_L14N_T2L_N3_GC_74	F23	FMC LA channel 17 data (CLK) N

FMC3_LA17_CC_P	IO_L14P_T2L_N2_GC_74	F24	FMC LA channel 17 data (CLK) P
FMC3_LA18_CC_N	IO_L13N_T2L_N1_GC_QBC_74	G24	FMC LA channel 18 data (CLK) N
FMC3_LA18_CC_P	IO_L13P_T2L_N0_GC_QBC_74	G25	FMC LA channel 18 data (CLK) P
FMC3_LA19_N	IO_L6N_T0U_N11_AD6N_74	P25	FMC LA channel 19 data N
FMC3_LA19_P	IO_L6P_T0U_N10_AD6P_74	R25	FMC LA channel 19 data P
FMC3_LA20_N	IO_L17N_T2U_N9_AD10N_74	D23	FMC LA channel 20 data N
FMC3_LA20_P	IO_L17P_T2U_N8_AD10P_74	D24	FMC LA channel 20 data P
FMC3_LA21_N	IO_L5N_T0U_N9_AD14N_74	M24	FMC LA channel 21 data N
FMC3_LA21_P	IO_L5P_T0U_N8_AD14P_74	M25	FMC LA channel 21 data P
FMC3_LA22_N	IO_L4N_T0U_N7_DBC_AD7N_74	N24	FMC LA channel 22 data N
FMC3_LA22_P	IO_L4P_T0U_N6_DBC_AD7P_74	P24	FMC LA channel 22 data P
FMC3_LA23_N	IO_L3N_T0L_N5_AD15N_74	N23	FMC LA channel 23 data N
FMC3_LA23_P	IO_L3P_T0L_N4_AD15P_74	P23	FMC LA channel 23 data P
FMC3_LA24_N	IO_L16N_T2U_N7_QBC_AD3N_74	E22	FMC LA channel 24 data N
FMC3_LA24_P	IO_L16P_T2U_N6_QBC_AD3P_74	E23	FMC LA channel 24 data P
FMC3_LA25_N	IO_L7N_T1L_N1_QBC_AD13N_74	L24	FMC LA channel 25 data N
FMC3_LA25_P	IO_L7P_T1L_N0_QBC_AD13P_74	L25	FMC LA channel 25 data P
FMC3_LA26_N	IO_L1N_T0L_N1_DBC_74	P21	FMC LA channel 26 data N
FMC3_LA26_P	IO_L1P_T0L_N0_DBC_74	R21	FMC LA channel 26 data P
FMC3_LA27_N	IO_L2N_T0L_N3_74	M22	FMC LA channel 27 data N
FMC3_LA27_P	IO_L2P_T0L_N2_74	N22	FMC LA channel 27 data P
FMC3_LA28_N	IO_L15N_T2L_N5_AD11N_74	F22	FMC LA channel 28 data N
FMC3_LA28_P	IO_L15P_T2L_N4_AD11P_74	G22	FMC LA channel 28 data P
FMC3_LA29_N	IO_L19N_T3L_N1_DBC_AD9N_74	B22	FMC LA channel 29 data N
FMC3_LA29_P	IO_L19P_T3L_N0_DBC_AD9P_74	C22	FMC LA channel 29 data P
FMC3_LA30_N	IO_L23N_T3U_N9_74	A24	FMC LA channel 30 data N
FMC3_LA30_P	IO_L23P_T3U_N8_74	B24	FMC LA channel 30 data P
FMC3_LA31_N	IO_L22N_T3U_N7_DBC_AD0N_74	A22	FMC LA channel 31 data N
FMC3_LA31_P	IO_L22P_T3U_N6_DBC_AD0P_74	A23	FMC LA channel 31 data P
FMC3_LA32_N	IO_L21N_T3L_N5_AD8N_74	B26	FMC LA channel 32 data N
FMC3_LA32_P	IO_L21P_T3L_N4_AD8P_74	C26	FMC LA channel 32 data P
FMC3_LA33_N	IO_L20N_T3L_N3_AD1N_74	C23	FMC LA channel 33 data N
FMC3_LA33_P	IO_L20P_T3L_N2_AD1P_74	C24	FMC LA channel 33 data P
FMC3_SCL	IO_L18N_T2U_N11_AD2N_74	D25	FMC I2C bus CLK
FMC3_SDA	IO_L24P_T3U_N10_74	B25	FMC I2C bus data
FMC3_HA00_CC_N	IO_L14N_T2L_N3_GC_73	G19	FMC HA channel 0 data (CLK) N
FMC3_HA00_CC_P	IO_L14P_T2L_N2_GC_73	G20	FMC HA channel 0 data (CLK) P
FMC3_HA01_CC_N	IO_L13N_T2L_N1_GC_QBC_73	H18	FMC HA channel 1 data (CLK) N
FMC3_HA01_CC_P	IO_L13P_T2L_N0_GC_QBC_73	H19	FMC HA channel 1 data (CLK) P
FMC3_HA02_N	IO_L20N_T3L_N3_AD1N_73	D20	FMC HA channel 2 data N
FMC3_HA02_P	IO_L20P_T3L_N2_AD1P_73	D21	FMC HA channel 2 data P

FMC3_HA03_N	IO_L2N_T0L_N3_73	N18	FMC HA channel 3 data N
FMC3_HA03_P	IO_L2P_T0L_N2_73	P18	FMC HA channel 3 data N
FMC3_HA04_N	IO_L4N_T0U_N7_DBC_AD7N_73	N19	FMC HA channel 4 data N
FMC3_HA04_P	IO_L4P_T0U_N6_DBC_AD7P_73	P19	FMC HA channel 4 data P
FMC3_HA05_N	IO_L5N_T0U_N9_AD14N_73	P20	FMC HA channel 5 data N
FMC3_HA05_P	IO_L5P_T0U_N8_AD14P_73	R20	FMC HA channel 5 data P
FMC3_HA06_N	IO_L3N_T0L_N5_AD15N_73	M19	FMC HA channel 6 data N
FMC3_HA06_P	IO_L3P_T0L_N4_AD15P_73	M20	FMC HA channel 6 data P
FMC3_HA07_N	IO_L1N_T0L_N1_DBC_73	M17	FMC HA channel 7 data N
FMC3_HA07_P	IO_L1P_T0L_N0_DBC_73	N17	FMC HA channel 7 data P
FMC3_HA08_N	IO_L9N_T1L_N5_AD12N_73	K20	FMC HA channel 8 data N
FMC3_HA08_P	IO_L9P_T1L_N4_AD12P_73	L20	FMC HA channel 8 data P
FMC3_HA09_N	IO_L15N_T2L_N5_AD11N_73	F19	FMC HA channel 9 data N
FMC3_HA09_P	IO_L15P_T2L_N4_AD11P_73	F20	FMC HA channel 9 data P
FMC3_HA10_N	IO_L16N_T2U_N7_QBC_AD3N_73	E17	FMC HA channel 10 data N
FMC3_HA10_P	IO_L16P_T2U_N6_QBC_AD3P_73	E18	FMC HA channel 10 data P
FMC3_HA11_N	IO_L17N_T2U_N9_AD10N_73	E20	FMC HA channel 11 data N
FMC3_HA11_P	IO_L17P_T2U_N8_AD10P_73	E21	FMC HA channel 11 data P
FMC3_HA12_N	IO_L10N_T1U_N7_QBC_AD4N_73	H21	FMC HA channel 12 data N
FMC3_HA12_P	IO_L10P_T1U_N6_QBC_AD4P_73	J21	FMC HA channel 12 data P
FMC3_HA13_N	IO_L11N_T1U_N9_GC_73	J18	FMC HA channel 13 data N
FMC3_HA13_P	IO_L11P_T1U_N8_GC_73	K18	FMC HA channel 13 data P
FMC3_HA14_N	IO_L8N_T1L_N3_AD5N_73	L18	FMC HA channel 14 data N
FMC3_HA14_P	IO_L8P_T1L_N2_AD5P_73	L19	FMC HA channel 14 data P
FMC3_HA15_N	IO_L19N_T3L_N1_DBC_AD9N_73	C19	FMC HA channel 15 data N
FMC3_HA15_P	IO_L19P_T3L_N0_DBC_AD9P_73	D19	FMC HA channel 15 data P
FMC3_HA16_N	IO_L22N_T3U_N7_DBC_AD0N_73	C18	FMC HA channel 16 data N
FMC3_HA16_P	IO_L22P_T3U_N6_DBC_AD0P_73	D18	FMC HA channel 16 data P
FMC3_HA17_CC_N	IO_L12N_T1U_N11_GC_73	J19	FMC HA channel 17 data (CLK) N
FMC3_HA17_CC_P	IO_L12P_T1U_N10_GC_73	J20	FMC HA channel 17 data (CLK) P
FMC3_HA18_N	IO_L21N_T3L_N5_AD8N_73	B21	FMC HA channel 18 data N
FMC3_HA18_P	IO_L21P_T3L_N4_AD8P_73	C21	FMC HA channel 18 data P
FMC3_HA19_N	IO_L23N_T3U_N9_73	A19	FMC HA channel 19 data N
FMC3_HA19_P	IO_L23P_T3U_N8_73	B19	FMC HA channel 19 data P
FMC3_HA20_N	IO_L24N_T3U_N11_73	A20	FMC HA channel 20 data N
FMC3_HA20_P	IO_L24P_T3U_N10_73	B20	FMC HA channel 20 data P
FMC3_HA21_N	IO_L6N_T0U_N11_AD6N_73	M21	FMC HA channel 21 data N
FMC3_HA21_P	IO_L6P_T0U_N10_AD6P_73	N21	FMC HA channel 21 data P
FMC3_HA22_N	IO_L18N_T2U_N11_AD2N_73	F17	FMC HA channel 22 data N
FMC3_HA22_P	IO_L18P_T2U_N10_AD2P_73	F18	FMC HA channel 22 data P
FMC3_HA23_N	IO_L7N_T1L_N1_QBC_AD13N_73	K17	FMC HA channel 23 data N

FMC3_HA23_P	IO_L7P_T1L_N0_QBC_AD13P_73	L17	FMC HA channel 23 data P
FMC3_HB00_CC_N	IO_L13N_T2L_N1_GC_QBC_72	F14	FMC HB channel 0 data (CLK) N
FMC3_HB00_CC_P	IO_L13P_T2L_N0_GC_QBC_72	G14	FMC HB channel 0 data (CLK) P
FMC3_HB01_N	IO_L15N_T2L_N5_AD11N_72	E13	FMC HB channel 1 data (CLK) N
FMC3_HB01_P	IO_L15P_T2L_N4_AD11P_72	F13	FMC HB channel 1 data (CLK) P
FMC3_HB02_N	IO_L16N_T2U_N7_QBC_AD3N_72	G16	FMC HB channel 2 data N
FMC3_HB02_P	IO_L16P_T2U_N6_QBC_AD3P_72	G17	FMC HB channel 2 data P
FMC3_HB03_N	IO_L14N_T2L_N3_GC_72	F15	FMC HB channel 3 data N
FMC3_HB03_P	IO_L14P_T2L_N2_GC_72	G15	FMC HB channel 3 data N
FMC3_HB04_N	IO_L17N_T2U_N9_AD10N_72	D15	FMC HB channel 4 data N
FMC3_HB04_P	IO_L17P_T2U_N8_AD10P_72	E15	FMC HB channel 4 data P
FMC3_HB05_N	IO_L10N_T1U_N7_QBC_AD4N_72	H16	FMC HB channel 5 data N
FMC3_HB05_P	IO_L10P_T1U_N6_QBC_AD4P_72	H17	FMC HB channel 5 data P
FMC3_HB06_CC_N	IO_L11N_T1U_N9_GC_72	H14	FMC HB channel 6 data N
FMC3_HB06_CC_P	IO_L11P_T1U_N8_GC_72	J14	FMC HB channel 6 data P
FMC3_HB07_N	IO_L9N_T1L_N5_AD12N_72	H13	FMC HB channel 7 data N
FMC3_HB07_P	IO_L9P_T1L_N4_AD12P_72	J13	FMC HB channel 7 data P
FMC3_HB08_N	IO_L8N_T1L_N3_AD5N_72	K15	FMC HB channel 8 data N
FMC3_HB08_P	IO_L8P_T1L_N2_AD5P_72	K16	FMC HB channel 8 data P
FMC3_HB09_N	IO_L7N_T1L_N1_QBC_AD13N_72	K13	FMC HB channel 9 data N
FMC3_HB09_P	IO_L7P_T1L_N0_QBC_AD13P_72	L13	FMC HB channel 9 data P
FMC3_HB10_N	IO_L22N_T3U_N7_DBC_AD0N_72	A15	FMC HB channel 10 data N
FMC3_HB10_P	IO_L22P_T3U_N6_DBC_AD0P_72	B15	FMC HB channel 10 data P
FMC3_HB11_N	IO_L1N_T0L_N1_DBC_72	N13	FMC HB channel 11 data N
FMC3_HB11_P	IO_L1P_T0L_N0_DBC_72	P13	FMC HB channel 11 data P
FMC3_HB12_N	IO_L6N_T0U_N11_AD6N_72	M16	FMC HB channel 12 data N
FMC3_HB12_P	IO_L6P_T0U_N10_AD6P_72	N16	FMC HB channel 12 data P
FMC3_HB13_N	IO_L18N_T2U_N11_AD2N_72	D16	FMC HB channel 13 data N
FMC3_HB13_P	IO_L18P_T2U_N10_AD2P_72	E16	FMC HB channel 13 data P
FMC3_HB14_N	IO_L23N_T3U_N9_72	B16	FMC HB channel 14 data N
FMC3_HB14_P	IO_L23P_T3U_N8_72	C16	FMC HB channel 14 data P
FMC3_HB15_N	IO_L24N_T3U_N11_72	A17	FMC HB channel 15 data N
FMC3_HB15_P	IO_L24P_T3U_N10_72	B17	FMC HB channel 15 data P
FMC3_HB16_N	IO_L4N_T0U_N7_DBC_AD7N_72	P16	FMC HB channel 16 data N
FMC3_HB16_P	IO_L4P_T0U_N6_DBC_AD7P_72	R16	FMC HB channel 16 data P
FMC3_HB17_CC_N	IO_L12N_T1U_N11_GC_72	J15	FMC HB channel 17 data (CLK) N
FMC3_HB17_CC_P	IO_L12P_T1U_N10_GC_72	J16	FMC HB channel 17 data (CLK) P
FMC3_HB18_N	IO_L21N_T3L_N5_AD8N_72	A13	FMC HB channel 18 data N
FMC3_HB18_P	IO_L21P_T3L_N4_AD8P_72	A14	FMC HB channel 18 data P
FMC3_HB19_N	IO_L2N_T0L_N3_72	N14	FMC HB channel 19 data N
FMC3_HB19_P	IO_L2P_T0L_N2_72	P14	FMC HB channel 19 data P

FMC3_HB20_N	IO_L3N_T0L_N5_AD15N_72	P15	FMC HB channel 20 data N
FMC3_HB20_P	IO_L3P_T0L_N4_AD15P_72	R15	FMC HB channel 20 data P
FMC3_HB21_N	IO_L5N_T0U_N9_AD14N_72	L14	FMC HB channel 21 data N
FMC3_HB21_P	IO_L5P_T0U_N8_AD14P_72	M14	FMC HB channel 21 data P
FMC3_DP0_M2C_P	MGTYRXP1_228	AD2	Transceiver data 0 input P
FMC3_DP0_M2C_N	MGTYRXN1_228	AD1	Transceiver data 0 input N
FMC3_DP1_M2C_P	MGTYRXP0_228	AE4	Transceiver data 1 input P
FMC3_DP1_M2C_N	MGTYRXN0_228	AE3	Transceiver data 1 input N
FMC3_DP2_M2C_P	MGTYRXP2_228	AC4	Transceiver data 2 input P
FMC3_DP2_M2C_N	MGTYRXN2_228	AC3	Transceiver data 2 input N
FMC3_DP3_M2C_P	MGTYRXP3_228	AB2	Transceiver data 3 input P
FMC3_DP3_M2C_N	MGTYRXN3_228	AB1	Transceiver data 3 input N
FMC3_DP4_M2C_P	MGTYRXP1_232	H2	Transceiver data 4 input P
FMC3_DP4_M2C_N	MGTYRXN1_232	H1	Transceiver data 4 input N
FMC3_DP5_M2C_P	MGTYRXP3_232	F2	Transceiver data 5 input P
FMC3_DP5_M2C_N	MGTYRXN3_232	F1	Transceiver data 5 input N
FMC3_DP6_M2C_P	MGTYRXP2_232	G4	Transceiver data 6 input P
FMC3_DP6_M2C_N	MGTYRXN2_232	G3	Transceiver data 6 input N
FMC3_DP7_M2C_P	MGTYRXP0_232	J4	Transceiver data 7 input P
FMC3_DP7_M2C_N	MGTYRXN0_232	J3	Transceiver data 7 input N
FMC3_DP8_M2C_P	MGTYRXP0_230	U4	Transceiver data 8 input P
FMC3_DP8_M2C_N	MGTYRXN0_230	U3	Transceiver data 8 input N
FMC3_DP9_M2C_P	MGTYRXP1_230	T2	Transceiver data 9 input P
FMC3_DP9_M2C_N	MGTYRXN1_230	T1	Transceiver data 9 input N
FMC3_DP10_M2C_P	MGTYRXP2_230	R4	Transceiver data 10 input P
FMC3_DP10_M2C_N	MGTYRXN2_230	R3	Transceiver data 10 input N
FMC3_DP11_M2C_P	MGTYRXP3_230	P2	Transceiver data 11 input P
FMC3_DP11_M2C_N	MGTYRXN3_230	P1	Transceiver data 11 input N
FMC3_DP12_M2C_P	MGTYRXP0_231	N4	Transceiver data 12 input P
FMC3_DP12_M2C_N	MGTYRXN0_231	N3	Transceiver data 12 input N
FMC3_DP13_M2C_P	MGTYRXP1_231	M2	Transceiver data 13 input P
FMC3_DP13_M2C_N	MGTYRXN1_231	M1	Transceiver data 13 input N
FMC3_DP14_M2C_P	MGTYRXP2_231	L4	Transceiver data 14 input P
FMC3_DP14_M2C_N	MGTYRXN2_231	L3	Transceiver data 14 input N
FMC3_DP15_M2C_P	MGTYRXP3_231	K2	Transceiver data 15 input P
FMC3_DP15_M2C_N	MGTYRXN3_231	K1	Transceiver data 15 input N
FMC3_DP16_M2C_P	MGTYRXP3_233	A5	Transceiver data 16 input P
FMC3_DP16_M2C_N	MGTYRXN3_233	A4	Transceiver data 16 input N
FMC3_DP17_M2C_P	MGTYRXP2_233	C4	Transceiver data 17 input P
FMC3_DP17_M2C_N	MGTYRXN2_233	C3	Transceiver data 17 input N
FMC3_DP18_M2C_P	MGTYRXP0_233	E4	Transceiver data 18 input P

FMC3_DP18_M2C_N	MGTYRXN0_233	E3	Transceiver data 18 input N
FMC3_DP19_M2C_P	MGTYRXP1_233	D2	Transceiver data 19 input P
FMC3_DP19_M2C_N	MGTYRXN1_233	D1	Transceiver data 19 input N
FMC3_DP20_M2C_P	MGTYRXP0_229	AA4	Transceiver data 20 input P
FMC3_DP20_M2C_N	MGTYRXN0_229	AA3	Transceiver data 20 input N
FMC3_DP21_M2C_P	MGTYRXP1_229	Y2	Transceiver data 21 input P
FMC3_DP21_M2C_N	MGTYRXN1_229	Y1	Transceiver data 21 input N
FMC3_DP22_M2C_P	MGTYRXP2_229	W4	Transceiver data 22 input P
FMC3_DP22_M2C_N	MGTYRXN2_229	W3	Transceiver data 22 input N
FMC3_DP23_M2C_P	MGTYRXP3_229	V2	Transceiver data 23 input P
FMC3_DP23_M2C_N	MGTYRXN3_229	V1	Transceiver data 23 input N
FMC3_DP0_C2M_P	MGTYTXP1_228	AD7	Transceiver data 0 output P
FMC3_DP0_C2M_N	MGTYTXN1_228	AD6	Transceiver data 0 output N
FMC3_DP1_C2M_P	MGTYTXP0_228	AE9	Transceiver data 1 output P
FMC3_DP1_C2M_N	MGTYTXN0_228	AE8	Transceiver data 1 output N
FMC3_DP2_C2M_P	MGTYTXP2_228	AC9	Transceiver data 2 output P
FMC3_DP2_C2M_N	MGTYTXN2_228	AC8	Transceiver data 2 output N
FMC3_DP3_C2M_P	MGTYTXP3_228	AB7	Transceiver data 3 output P
FMC3_DP3_C2M_N	MGTYTXN3_228	AB6	Transceiver data 3 output N
FMC3_DP4_C2M_P	MGTYTXP1_232	H7	Transceiver data 4 output P
FMC3_DP4_C2M_N	MGTYTXN1_232	H6	Transceiver data 4 output N
FMC3_DP5_C2M_P	MGTYTXP3_232	F7	Transceiver data 5 output P
FMC3_DP5_C2M_N	MGTYTXN3_232	F6	Transceiver data 5 output N
FMC3_DP6_C2M_P	MGTYTXP2_232	G9	Transceiver data 6 output P
FMC3_DP6_C2M_N	MGTYTXN2_232	G8	Transceiver data 6 output N
FMC3_DP7_C2M_P	MGTYTXP0_232	J9	Transceiver data 7 output P
FMC3_DP7_C2M_N	MGTYTXN0_232	J8	Transceiver data 7 output N
FMC3_DP8_C2M_P	MGTYTXP0_230	U9	Transceiver data 8 output P
FMC3_DP8_C2M_N	MGTYTXN0_230	U8	Transceiver data 8 output N
FMC3_DP9_C2M_P	MGTYTXP1_230	T7	Transceiver data 9 output P
FMC3_DP9_C2M_N	MGTYTXN1_230	T6	Transceiver data 9 output N
FMC3_DP10_C2M_P	MGTYTXP2_230	R9	Transceiver data 10 output P
FMC3_DP10_C2M_N	MGTYTXN2_230	R8	Transceiver data 10 output N
FMC3_DP11_C2M_P	MGTYTXP3_230	P7	Transceiver data 11 output P
FMC3_DP11_C2M_N	MGTYTXN3_230	P6	Transceiver data 11 output N
FMC3_DP12_C2M_P	MGTYTXP0_231	N9	Transceiver data 12 output P
FMC3_DP12_C2M_N	MGTYTXN0_231	N8	Transceiver data 12 output N
FMC3_DP13_C2M_P	MGTYTXP1_231	M7	Transceiver data 13 output P
FMC3_DP13_C2M_N	MGTYTXN1_231	M6	Transceiver data 13 output N
FMC3_DP14_C2M_P	MGTYTXP2_231	L9	Transceiver data 14 output P
FMC3_DP14_C2M_N	MGTYTXN2_231	L8	Transceiver data 14 output N

FMC3_DP15_C2M_P	MGTYTXP3_231	K7	Transceiver data 15 output P
FMC3_DP15_C2M_N	MGTYTXN3_231	K6	Transceiver data 15 output N
FMC3_DP16_C2M_P	MGTYTXP3_233	A9	Transceiver data 16 output P
FMC3_DP16_C2M_N	MGTYTXN3_233	A8	Transceiver data 16 output N
FMC3_DP17_C2M_P	MGTYTXP2_233	C9	Transceiver data 17 output P
FMC3_DP17_C2M_N	MGTYTXN2_233	C8	Transceiver data 17 output N
FMC3_DP18_C2M_P	MGTYTXP0_233	E9	Transceiver data 18 output P
FMC3_DP18_C2M_N	MGTYTXN0_233	E8	Transceiver data 18 output N
FMC3_DP19_C2M_P	MGTYTXP1_233	D7	Transceiver data 19 output P
FMC3_DP19_C2M_N	MGTYTXN1_233	D6	Transceiver data 19 output N
FMC3_DP20_C2M_P	MGTYTXP0_229	AA9	Transceiver data 20 output P
FMC3_DP20_C2M_N	MGTYTXN0_229	AA8	Transceiver data 20 output N
FMC3_DP21_C2M_P	MGTYTXP1_229	Y7	Transceiver data 21 output P
FMC3_DP21_C2M_N	MGTYTXN1_229	Y6	Transceiver data 21 output N
FMC3_DP22_C2M_P	MGTYTXP2_229	W9	Transceiver data 22 output P
FMC3_DP22_C2M_N	MGTYTXN2_229	W8	Transceiver data 22 output N
FMC3_DP23_C2M_P	MGTYTXP3_229	V7	Transceiver data 23 output P
FMC3_DP23_C2M_N	MGTYTXN3_229	V6	Transceiver data 23 output N
FMC3_GBT1_0_M2C_C_N	MGTREFCLK1N_232	F10	Transceiver reference CLK 1 input N
FMC3_GBT1_0_M2C_C_P	MGTREFCLK1P_232	F11	Transceiver reference CLK 1 input P
FMC3_GBT1_1_M2C_C_N	MGTREFCLK1N_228	AB10	Transceiver reference CLK 1 input N
FMC3_GBT1_1_M2C_C_P	MGTREFCLK1P_228	AB11	Transceiver reference CLK 1 input P
FMC3_GBT1_2_M2C_C_N	MGTREFCLK1N_230	P10	Transceiver reference CLK 1 input N
FMC3_GBT1_2_M2C_C_P	MGTREFCLK1P_230	P11	Transceiver reference CLK 1 input P
FMC3_GBT1_3_M2C_C_N	MGTREFCLK1N_231	K10	Transceiver reference CLK 1 input N
FMC3_GBT1_3_M2C_C_P	MGTREFCLK1P_231	K11	Transceiver reference CLK 1 input P
FMC3_GBT1_4_M2C_C_N	MGTREFCLK1N_233	B10	Transceiver reference CLK 1 input N
FMC3_GBT1_4_M2C_C_P	MGTREFCLK1P_233	B11	Transceiver reference CLK 1 input P
FMC3_GBT1_5_M2C_C_N	MGTREFCLK1N_229	V10	Transceiver reference CLK 1 input N
FMC3_GBT1_5_M2C_C_P	MGTREFCLK1P_229	V11	Transceiver reference CLK 1 input P
FMC3_GBT0_0_M2C_C_N	MGTREFCLK0N_228	AD10	Transceiver reference CLK 0 input N
FMC3_GBT0_0_M2C_C_P	MGTREFCLK0P_228	AD11	Transceiver reference CLK 0 input P
FMC3_GBTCLK2_M2C_C_N	MGTREFCLK0N_230	T10	Transceiver reference CLK 0 input N
FMC3_GBTCLK2_M2C_C_P	MGTREFCLK0P_230	T11	Transceiver reference CLK 0 input P
FMC3_GBTCLK3_M2C_C_N	MGTREFCLK0N_231	M10	Transceiver reference CLK 0 input N
FMC3_GBTCLK3_M2C_C_P	MGTREFCLK0P_231	M11	Transceiver reference CLK 0 input P
FMC3_GBTCLK4_M2C_C_N	MGTREFCLK0N_233	D10	Transceiver reference CLK 0 input N
FMC3_GBTCLK4_M2C_C_P	MGTREFCLK0P_233	D11	Transceiver reference CLK 0 input P
FMC3_GBTCLK5_M2C_C_N	MGTREFCLK0N_229	Y10	Transceiver reference CLK 0 input N
FMC3_GBTCLK5_M2C_C_P	MGTREFCLK0P_229	Y11	Transceiver reference CLK 0 input P
FMC3_H_PRSNT_M2C_B	IO_T2U_N12_74	F25	Reset PIN

FMC3_L_PRSNT_M2C_B	IO_T3U_N12_74	D26	Reset PIN
FMC3_PG_C2M	IO_L24N_T3U_N11_74	A25	Power statues PIN
FMC3_PG_M2C	IO_T3U_N12_71	C28	Power statues PIN
FMC3_REFCLK_C2M_N	IO_L10N_T1U_N7_QBC_AD4N_71	K28	Reference CLK 1 output N
FMC3_REFCLK_C2M_P	IO_L10P_T1U_N6_QBC_AD4P_71	L28	Reference CLK 1 output P
FMC3_REFCLK_M2C_N	IO_L11N_T1U_N9_GC_71	H28	Reference CLK 1 input N
FMC3_REFCLK_M2C_P	IO_L11P_T1U_N8_GC_71	H27	Reference CLK 1 input P
FMC3_SYNC_C2M_N	IO_L8N_T1L_N3_AD5N_71	K27	C2M SYNC output N
FMC3_SYNC_C2M_P	IO_L8P_T1L_N2_AD5P_71	K26	C2M SYNC output P
FMC3_SYNC_M2C_N	IO_L9N_T1L_N5_AD12N_71	L27	M2C SYNC input N
FMC3_SYNC_M2C_P	IO_L9P_T1L_N4_AD12P_71	M27	M2C SYNC input P
FMC3_GBT0_1_M2C_C_N	MGTREFCLK0N_232	H10	M2C SYNC input N
FMC3_GBT0_1_M2C_C_P	MGTREFCLK0P_232	H11	M2C SYNC input P

Table 8: FMC3 + (J7) Connector PIN assignment

8 USB Serial Converter

8.1 Schematic Diagram

The AXVU13P expansion board is equipped with a UART to USB interface for system debugging. The conversion chip used is the Silicon Labs CP2102GM USB-UART chip. The USB interface is a MINI USB type, allowing it to be connected to a PC's USB port with a single USB cable for separate power supply to the SoM and serial data communication.

Figure 12 shows the schematic diagram of the USB UART circuit design.

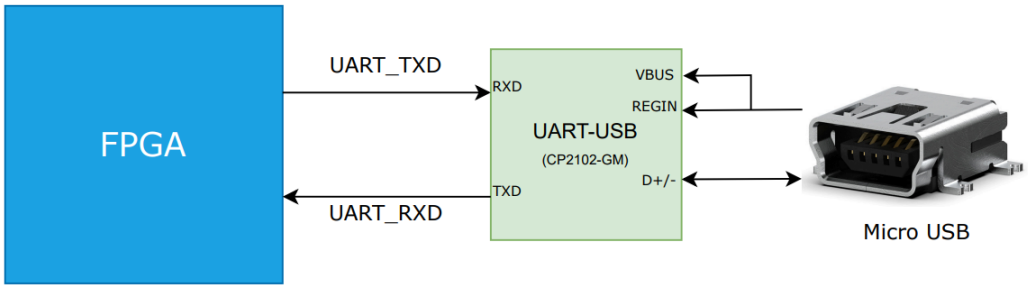

Figure 12: USB serial converter schematic diagram

8.2 USB Serial Converter PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
UART_RXD_LS	IO_L5N_T0U_N9_AD14N_A23_65	BF25	UART data input
UART_TXD_LS	IO_L5P_T0U_N8_AD14P_A22_65	BE25	UART data output

Table 9: USB Serial Converter PIN Assignment

9 IO Expansion Interface

9.1 Expansion Interface Schematic

The AXVU13P features a 14-pin IO expansion interface with a 2.54mm pitch, exposing 10 IO signals. By default, these are not soldered. The pin definitions are as follows:

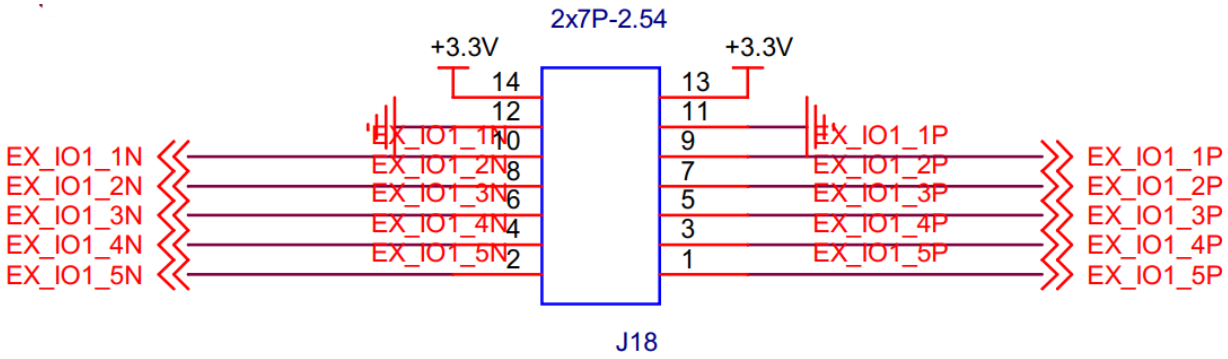

Figure 13: Expansion Interface Schematic

9.2 Expansion Interface PIN Assignment

Expansion port PIN	Signal Name	PIN #	Comments
1	EX_IO1_5P	BC8	Data
2	EX_IO1_5N	BC7	Data
3	EX_IO1_4P	BD9	Data
4	EX_IO1_4N	BD8	Data
5	EX_IO1_3P	BA7	Data
6	EX_IO1_3N	BB7	Data
7	EX_IO1_2P	BC12	Data
8	EX_IO1_2N	BC11	Data
9	EX_IO1_1P	BB11	Data
10	EX_IO1_1N	BB10	Data
11	GND	-	Ground
12	GND	-	Ground
13	+3.3V	-	3.3V
14	+3.3V	-	3.3V

Table 10: Expansion Interface PIN Assignment

10 SMA Interface

The board is equipped with two SMA interfaces; one can serve as a differential input, and the other can serve as a differential output. These are connected to the HPIO pins of the FPGA and can be used for the verification of customer differential signal input and output.

The FPGA pin assignments are as follows:

Signal Name	PIN Name	PIN #	Comments
CLKOUT_P	B68_L12_P	BA9	SMA data receive positive
CLKOUT_N	B68_L12_N	BA8	SMA data receive negative
CLKIN_P	B68_L11_P	BB9	SMA data input positive
CLKIN_N	B68_L11_N	BC9	SMA data input negative

Table 11: SMA Interface PIN Assignment

11 JTAG Debug Port

A 14-pin JTAG interface is reserved on the AXVU13P base board for downloading FPGA programs or programming them into FLASH. To prevent damage to the FPGA chip due to hot swapping, we have added protection diodes to the JTAG signals to ensure that the voltage remains within the acceptable range for the FPGA, thus avoiding chip damage.

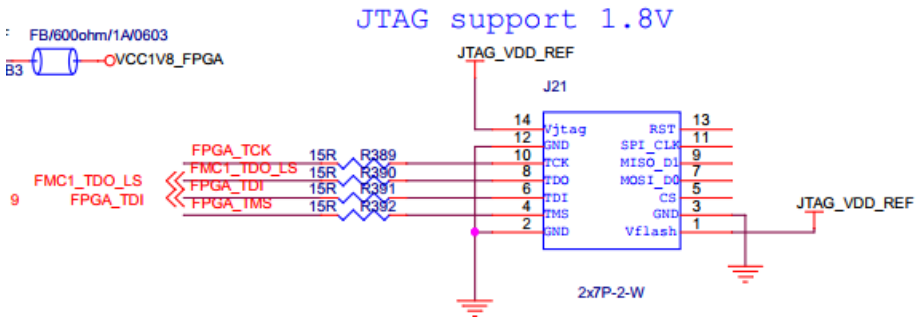

Figure 14: JTAG debug port schematic

12 Buttons and LEDs

12.1 Schematic Diagram

The AXVU13P base board features 8 light-emitting diodes (LEDs), including 1 power indicator light, 1 configuration completion indicator, 2 UART communication indicator lights, and 4 user LEDs. When the development board is powered on, the power indicator light illuminates. The 4 user LEDs are connected to the FPGA's IO pins, allowing users to control their on/off state through software. When the voltage on the IO pin connected to a user LED is high, the LED lights up; when the IO voltage is low, the LED turns off.

Additionally, there is one user button on the board, with the default button signal being high; when the button is pressed, the level becomes low.

The hardware connection diagram for the user LEDs and button is shown in Figure 14:

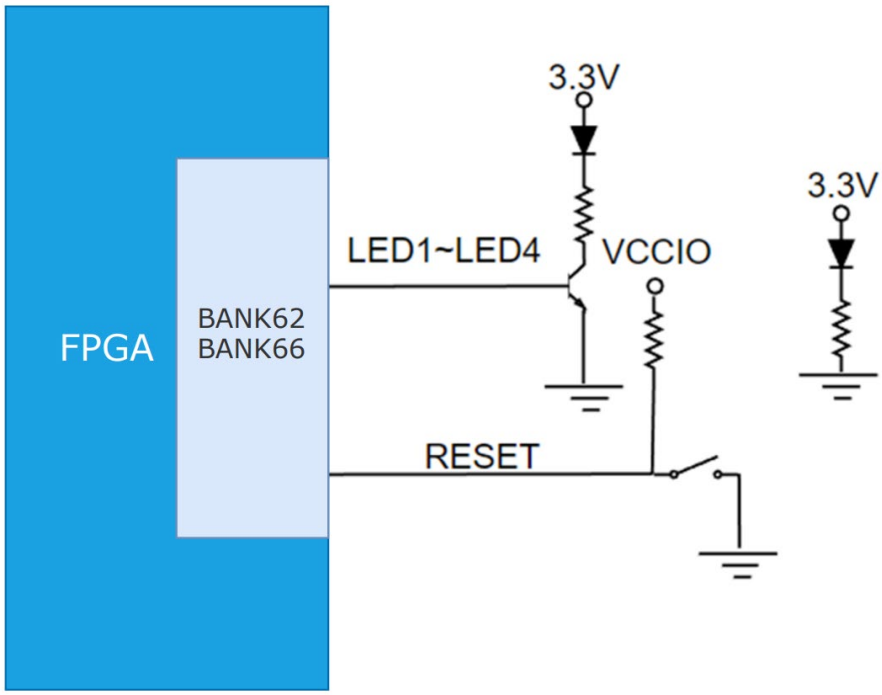

Figure 15: Buttons and LEDs schematic diagram

12.2 Buttons and LEDs PIN Assignment

Signal Name	FPGA PIN Name	PIN #	Comments
RESET	IO_T1U_N12_62	BF35	User button
LED1	IO_L6N_T0U_N11_AD6N_66	BC18	User LED1
LED2	IO_L6P_T0U_N10_AD6P_66	BB19	User LED2
LED3	IO_L10P_T1U_N6_QBC_AD4P_66	AV21	User LED3
LED4	IO_L10N_T1U_N7_QBC_AD4N_66	AW21	User LED4

Table 12: Buttons and LEDs PIN assignment

13 Power

13.1 Power Design Schematic Diagram

The input voltage for the development board is DC12V, which can be supplied either through a PCIe slot or an external +12V power source. When using an external power supply, please use the power supply that comes with the development board; do not use power supplies of different specifications to avoid damaging the board. The 12V input is converted by a DCDC module to produce the FPGA core power, with an output current as high as 150A, meeting the current demand for the core voltage.

The +12V power then goes through other DCDC chips: SGM61163 to generate VCCAUX, IS6608A to generate MGTAVCC, and MGTAVTT for powering the FPGA's auxiliary power and high-speed transceivers. DCDC chips ETA1471, SGM61163, and IS66066 produce +1.2V, VCC1V8_FPGA, and +3.3V to supply power to DDR4, FPGA banks, and peripherals. Additionally, D3V3 generates supplementary power for high-speed transceivers and the FPGA's ADC power source at +1.8V through two LDO chips ETA5060. The VTT and DDR2V5 voltages for DDR4 are generated by TPS51200 and ETA5050. Power is also provided to the three FMC+ interfaces and other peripherals through IS66066.

The power design block diagram on the board is as follows:

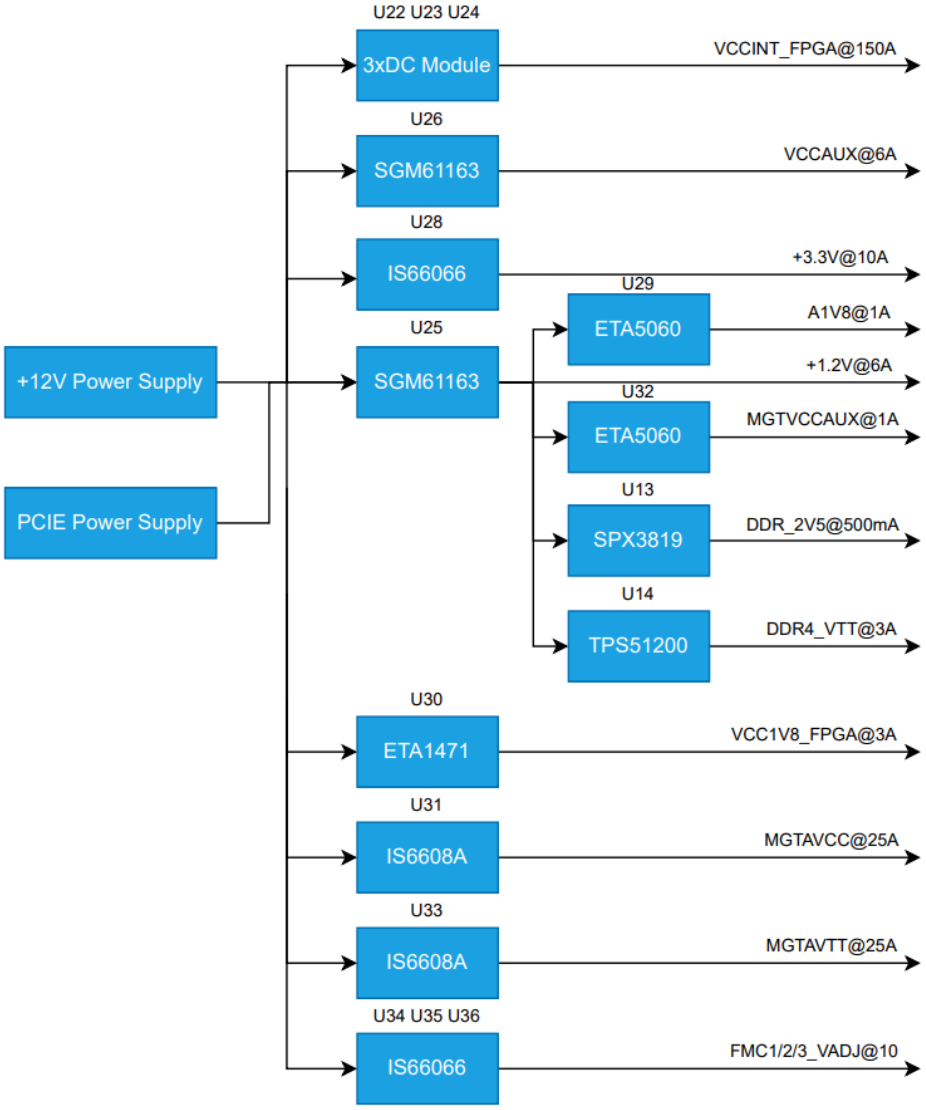

Figure16: Power supply interface schematic diagram

13.2 Power Distribution Functions Table

Power Supply	Function
VCCINT_FPGA@150A	FPGA Core power supply
VCCAUX@6A	FPGA Auxiliary power supply
MGTVCCAUX@1A	GTY support power
MGTAVCC@25A	FPGA GTY power supply
MGTAVTT@25A	FPGA GTY power supply
VCC1V8_FPGA@3A	FPGA BANK Voltage and Peripherals
+1.2V@6A	SODIMM & BANK voltage
FMC1_VADJ@10A	FMC1+ Regulation voltage
FMC2_VADJ@10A	FMC2+ Regulation voltage
FMC3_VADJ@10A	FMC3+ Regulation voltage
+3.3V@10A	FPGA Peripherals voltage
DDR4_VTT@3A	DDR4 VTT voltage
DDR_2V5@500mA	DDR4 supply voltage

Table 12: Power distribution functions table

14 Structural Dimensional

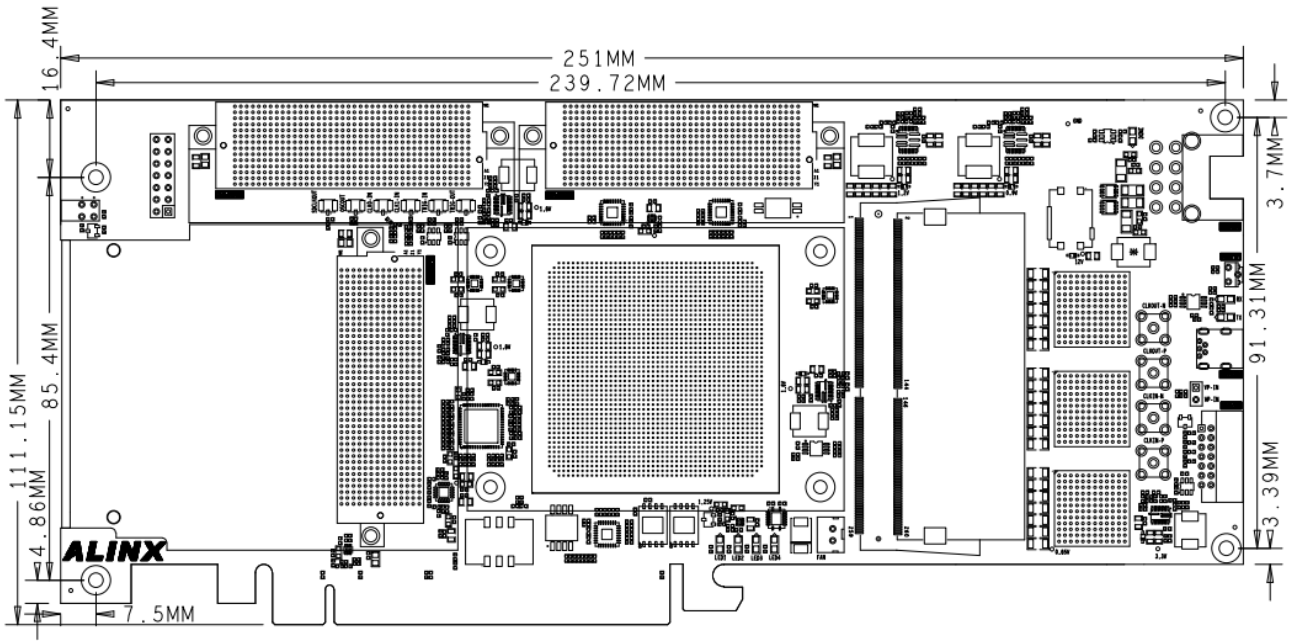

Figure 17: Top view structural dimensional