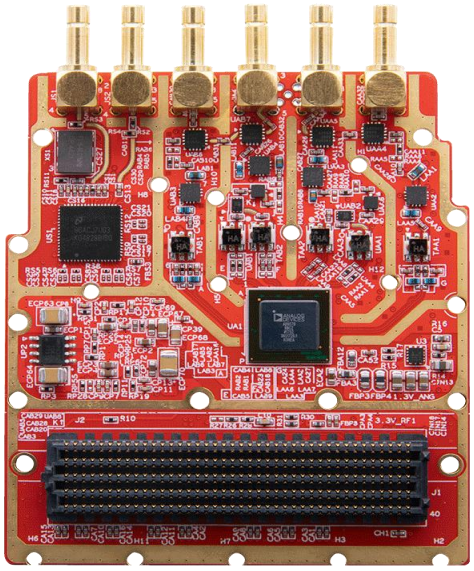
FMC Wideband RF Transceiver ADRV9009 based



Introduction：

FH9000 is a high-performance, broadband, and highly integrated RF sub card based on the VITA57.1FMC architecture.

The FH9000 uses ADI's RF agile transceiver ADRV9009 as its processing core, which can cover the 75MHz~6GHz frequency band and integrate dual channel transceiver links. The maximum real-time bandwidth for sending is 450MHz, and the maximum bandwidth for receiving is 200MHz. Compared to previous generation products,AD9009 has larger bandwidth, better sensitivity, dynamic range, and IP3 performance.FH9000 is more suitable for application on general software radio platforms.

We5G provides FPGA reference code for FH9000, allowing users to easily modify the RF working status through SDK software. We5G also provides JESD204B reference design, allowing users to quickly verify and integrate the system.

Main Features：

- ✓ AD9009
- ✓ Tuning range：75MHz-6GHz
- ✓ 16bit ADC & 14bitDAC
- ✓ Supports half duplex, full duplex, TDD/FDD mode
- ✓ RF impedance matching 50Ω
- ✓ Maximum RX bandwidth: ： 200MHz
- ✓ Maximum ORX observation channel bandwidth：450MHz
- ✓ Maximum TX synthetic bandwidth：450MHz
- ✓ Integrated power amplifier （ 14dB@2GHz ）, supporting a maximum transmission power of 10dBm output
- ✓ Support for internal or external reference clocks
- ✓ JESD204B digital interface

Application Scenario：

3G,4G and 5G macrocell base stations
FDD and TDD active antenna systems
Microwave, nonline of sight (NLOS) backhaul systemsElectronic warfare
Massive MIMO
Phased array radar
Military communications
Portable test equipment

System Structure：

The RF front-end includes components such as power amplifiers, antenna switches, balun, etc., which enhances the practicality of the device. The main differences between FH9000 and ADI's AD9009 development board are as follows：

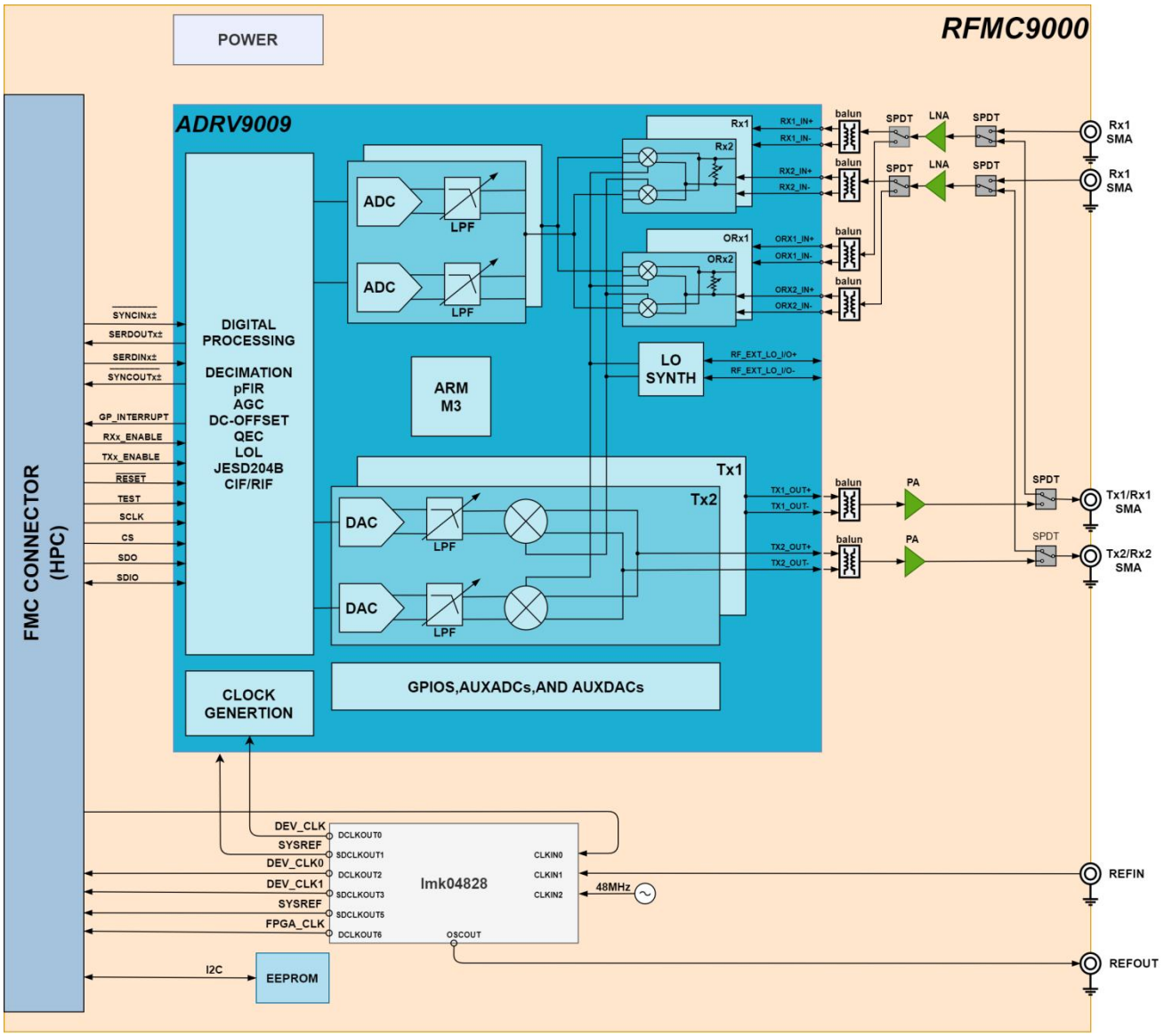
- ✓ Transmitting terminal add PA
- ✓ Support maximum transmission power of 10dBm
- ✓ Receiving terminal, add LNA
- ✓ Support external link gain of 15dB(300MHz-6GHz)
- ✓ Support TDD and FDD mode switching with On board dual antenna switch
- ✓ IO control ns level switching speed

✓ High isolation, single switch 40dB isolation ORX channel and RX channel add switches, and you can choose to use RX channel or ORX channel for Reception.

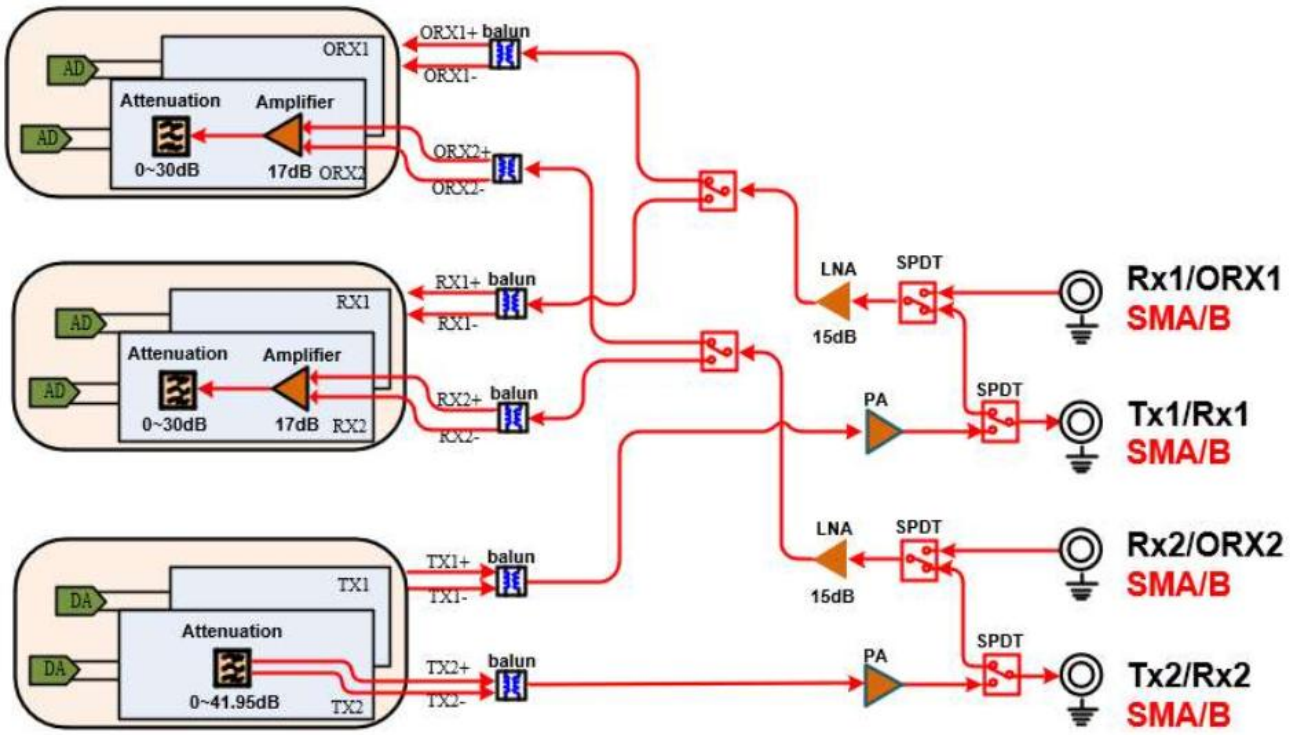
✓ Flexible reference clock, variable reference achieved through TI clock chip (LMK04828)

✓ Can support dynamic JESD204B sampling clock rate

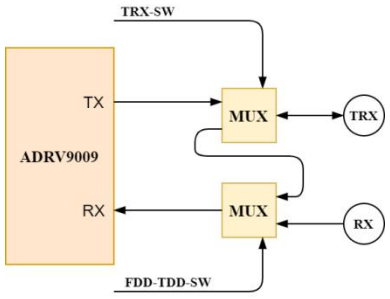
Function Frame



RF front-end link

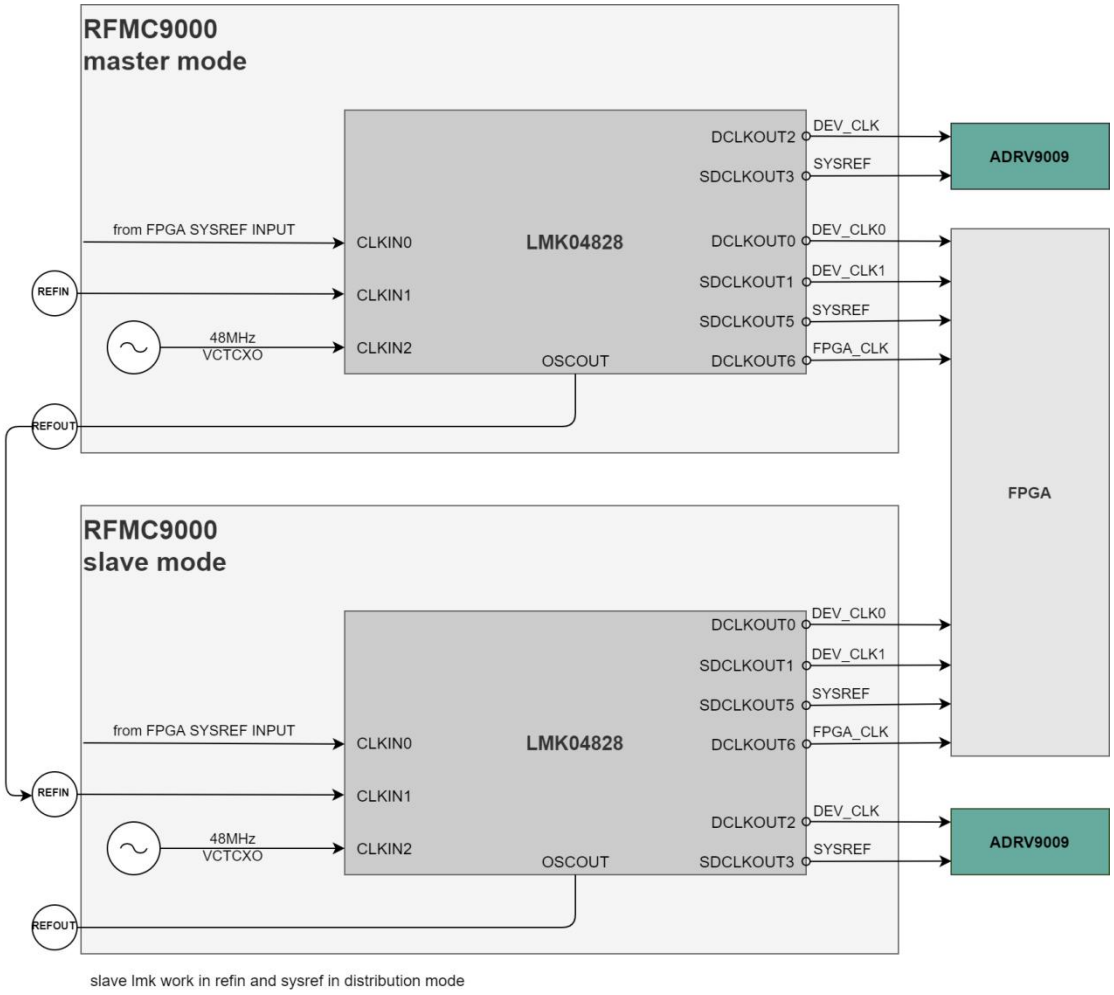


RF Switch for switch of receiving and dispatching



Name	1	0
TRX-SW	TX->TRX	TRX->MUX2
FDD-TDD-SW	RX<-RX	MUX1->RX

Clock cascade allocation link



slave lmk work in refin and sysref in distribution mode

Front Panel

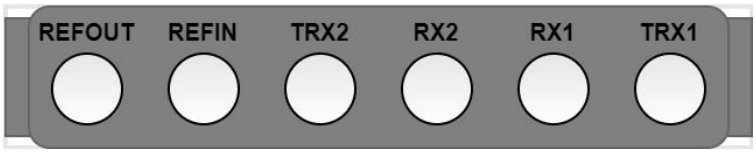


Figure 1 Definition of RFMC7000 Module Front Panel

No.	Items	Remark
1	TRX1	DAC Output channel 1（Can also be configured as RX1）
2	RX1	ADC Input channel 1（RX1/ORX1）
3	RX2	ADC Input channel 2（RX2/ORX2）
4	TRX2	DAC Output channel 2（Can also be configured asRX2）
5	REFIN	Reference Clock Input
6	REFOUT	Reference Clock Output

The index of Radio Frequency：

	No.	Items	Specifications	Remark
Tx	1	Frequency	75~6000MHz	
	2	Interface	SMB	
	3	Bandwidth	Up to 450 MHz	Tx real-time bandwidth, tunable
	4	Transmission Power	17dBm	75~6000MHz, CW
	5	EVM	<0.7%	
	6	Gain Control Range	32dB	
	7	Gain Step	0.05dB	
	8	ACLR	< -64dBc	@0dBm output
	9	Spurious	60dBc	
	10	SSB Suppression	65dBc	
	11	LO Suppression	70dBc	
	12	DAC Sample Rate (max)	122.88MS/s	Up to 245.76MS/s
	13	DAC Resolution	14bits	
Rx	1	Frequency	75~6000MHz	
	2	Interface	SMB	
	3	Bandwidth	8 to 200 MHz	real-time bandwidth, tunable
	4	Sensitivity:	-93dBm@20MHz	Noise Figure<3dB
	5	EVM	<1.2%	@-30dBm input
	6	Gain Control Range	61.5dB	Including 30dB of ADRV9009 inside
	7	Gain Step	0.5dB	
	8	Rx Alias Band Rejection	80dB	Due to digital filters
	9	Noise Figure	<3dB	Maximum RX gain
	10	IIP3 (@ typ NF)	-25dBm	
	11	ADC Sample Rate (max)	122.88MS/s	Up to153.6MS/s
	12	ADC Resolution	16bits	
	13	ADC Wideband SFDR	78dBc	
	1	Voltage	3.3V& 12V	
	2	ON/OFF TIME	<6uS	TDD model
	3	Duplexing Model	TDD/FDD	
	4	Power Consumptions	<6W	

Figure 2 FMC interface definition

Signal Name	FMC Pin Name	FMC Pin	Direction	Remark
ADRV9009 Signal of Chips				
FPGA_REF_CLK0_N	GBTCLK0_M2C_N	D5	Output	JESD204B Reference Clock LVDS
FPGA_REF_CLK0_P	GBTCLK0_M2C_P	D4	Output	JESD204B Reference Clock LVDS
FPGA_REF_CLK1_N	GBTCLK1_M2C_N	B21	Output	JESD204B Reference Clock LVDS
FPGA_REF_CLK1_P	GBTCLK1_M2C_P	B20	Output	JESD204B Reference Clock LVDS
FPGA_SYSREF_N	LA23_N	D21	Output	JESD204B SYSREF LVDS
FPGA_SYSREF_P	LA23_P	D20	Output	JESD204B SYSREF LVDS
SERDIN0_N	DP0_C2M_N	C3	Input	JESD204B DAC CML
SERDIN0_P	DP0_C2M_P	C2	Input	JESD204B DAC CML
SERDIN1_N	DP1_C2M_N	A23	Input	JESD204B DAC CML
SERDIN1_P	DP1_C2M_P	A22	Input	JESD204B DAC CML
SERDIN2_N	DP2_C2M_N	A27	Input	JESD204B DAC CML
SERDIN2_P	DP2_C2M_P	A26	Input	JESD204B DAC CML
SERDIN3_N	DP3_C2M_N	A31	Input	JESD204B DAC CML
SERDIN3_P	DP3_C2M_P	A30	Input	JESD204B DAC CML
SERDOUT0_N	DP0_M2C_N	C7	Output	JESD204B ADC CML
SERDOUT0_P	DP0_M2C_P	C6	Output	JESD204B ADC CML
SERDOUT1_N	DP1_M2C_N	A3	Output	JESD204B ADC CML
SERDOUT1_P	DP1_M2C_P	A2	Output	JESD204B ADC CML
SERDOUT2_N	DP2_M2C_N	A7	Output	JESD204B ADC CML
SERDOUT2_P	DP2_M2C_P	A6	Output	JESD204B ADC CML
SERDOUT3_N	DP3_M2C_N	A11	Output	JESD204B ADC CML
SERDOUT3_P	DP3_M2C_P	A10	Output	JESD204B ADC CML
SYNCINB0_N	LA03_N	G10	Input	JESD204B SYNC LVDS
SYNCINB0_P	LA03_P	G9	Input	JESD204B SYNC LVDS
SYNCINB1_N	LA25_N	G28	Input	JESD204B SYNC LVDS
SYNCINB1_P	LA25_P	G27	Input	JESD204B SYNC LVDS
SYNCOUTB0_N	LA32_N	H38	Output	JESD204B SYNC LVDS
SYNCOUTB0_P	LA32_P	H37	Output	JESD204B SYNC LVDS
TX1_ENABLE	LA13_P	D17	Input	ADRV9009 Send Enable
TX2_ENABLE	LA14_P	C18	Input	ADRV9009 Send Enable
RX1_ENABLE	LA13_N	D18	Input	ADRV9009 Receive Enable
RX2_ENABLE	LA14_N	C19	Input	ADRV9009 Receive Enable
TEST	LA05_P	D11	Input	ADRV9009 TEST
GP_INTERRUPT	LA04_N	H11	Output	ADRV9009 Interrupt

RESETB	LA04_P	H10	Input	ADRV9009 Reset
AD9371_SPI_CLK	LA07_P	H13	Input	ADRV9009 SPI
AD9371_SPI_CS	LA09_P	D14	Input	ADRV9009 SPI
AD9371_SPI_MISO	LA08_P	G12	Output	ADRV9009 SPI
AD9371_SPI_MOSI	LA07_N	H14	Input	ADRV9009 SPI
GPIO_0	LA15_P	H19	Two-way	ADRV9009 GPIO
GPIO_1	LA15_N	H20	Two-way	ADRV9009 GPIO
GPIO_2	LA16_P	G18	Two-way	ADRV9009 GPIO
GPIO_3	LA16_N	G19	Two-way	ADRV9009 GPIO
GPIO_4	LA21_P	H25	Two-way	ADRV9009 GPIO
GPIO_5	LA21_N	H26	Two-way	ADRV9009 GPIO
GPIO_6	LA18_P_CC	C22	Two-way	ADRV9009 GPIO
GPIO_7	LA18_N_CC	C23	Two-way	ADRV9009 GPIO
GPIO_8	LA22_N	G25	Two-way	ADRV9009 GPIO
GPIO_9	LA19_P	H22	Two-way	ADRV9009 GPIO
GPIO_10	LA19_N	H23	Two-way	ADRV9009 GPIO
GPIO_11	LA20_P	G21	Two-way	ADRV9009 GPIO
GPIO_12	LA20_N	G22	Two-way	ADRV9009 GPIO
GPIO_13	LA29_N	G31	Two-way	ADRV9009 GPIO
GPIO_14	LA29_P	G30	Two-way	ADRV9009 GPIO
GPIO_15	LA22_P	G24	Two-way	ADRV9009 GPIO
GPIO_16	LA12_N	G16	Two-way	ADRV9009 GPIO
GPIO_17	LA12_P	G15	Two-way	ADRV9009 GPIO
GPIO_18	LA05_N	D12	Two-way	ADRV9009 GPIO
FH9000 Additional signal				
GPIO_SCL	SCL	C30	Input	EEPROM SCL
GPIO_SDA	SDA	C31	Two-way	EEPROM SDA
LMK_RESET	LA30_N	H35	Input	Clock Chip Reset Signal
LMK_SPI_CS	LA28_N	H32	Input	Clock Chip SPI Enable
LMK_SPI_MISO	LA26_P	D26	Input	Clock Chip SPI Data
LMK_SPI_MOSI	LA27_P	C26	Input	Clock Chip SPI Data
LMK_SPI_SCLK	LA27_N	C27	Input	Clock Chip SPI Clock
LMK_SYNC	LA11_N	H17	Output	Clock Chip Synchronization Signal
LMK_CLKIN_SEL0	LA10_N	C15	Input	Clock Chip Reference Input Selection
LMK_CLKIN_SEL1	LA10_P	C14	Input	Clock Chip Reference Input Selection
FPGA_GC_CLK_N	CLK0_M2C_N	H5	Output	Clock Chip DCLKOUT6*
FPGA_GC_CLK_P	CLK0_M2C_P	H4	Output	Clock Chip DCLKOUT6
REF_CLK_C2M_N	CLK1_M2C_N	G3	Input	Clock Chip CLKIN0

REF_CLK_C2M_P	CLK1_M2C_P	G2	Input	Clock Chip CLKIN0*
FDDTDD_SW1	LA00_P_CC	G6	Input	RF switch duplex switching
TRX_SW1	LA00_N_CC	G7	Input	RF switch duplex switching
FDDTDD_SW2	LA06_P	C10	Input	RF switch duplex switching
TRX_SW2	LA06_N	C11	Input	RF switch duplex switching
TX_BANDSEL_A	LA24_N	G3	Input	RF RX/ORX switching
TX_BANDSEL_B	LA24_P	G2	Input	RF RX/ORX switching

All single ended signal levels range from 1.8V~2.5V

FMC Power Supply：

The expansion module requires three types of power supply：

12V： 1A

3.3V: 1A

VADJ：1A 1.8V~2.5V

FH9000 Dimension：