FMC 4-channels high-speed AD module FL2514 User Manual

Rev 1.0

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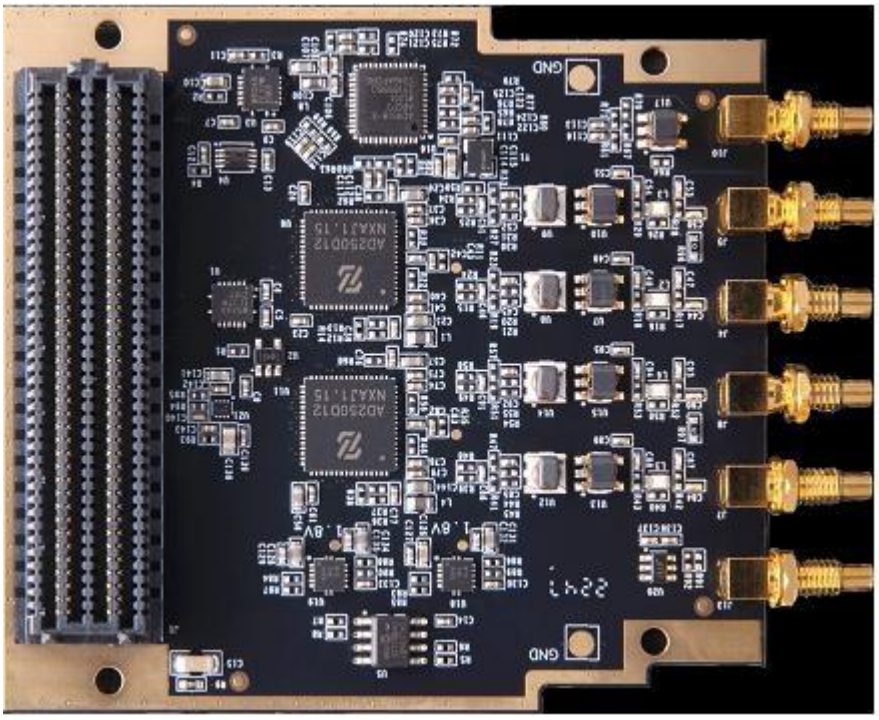
1. Introduction of FL2514 Module

Alinx FMC high-speed AD module FL9613 is a 4-channels 250MSPS, 14-bit analog to digital module. Its AD conversion adopts two ZGAD250D14 chips from Zynalog Semiconductor Co., Ltd, each of which supports 2-channels AD inputs. Therefore, the two ZGAD250D14 chips support a total of 4-channels AD inputs. The voltage range of the analog signal input is 1.5 V P-P, and the interface is SSMC.

FL2514 supports external trigger signal input and is also an SSMC interface; The clock mode supports internal reference clock input and external reference clock input, and the clock selection can be configured through the SPI bus.

The electrical and mechanical design of FL2514 is based on the FMC standard (ANSI/VITA 57.1), which is a standard LPC FMC interface used to connect FPGA development boards. The FMC connector model is ASP_ 134604_ 01.

The picture of the FL2514 module is as follows:

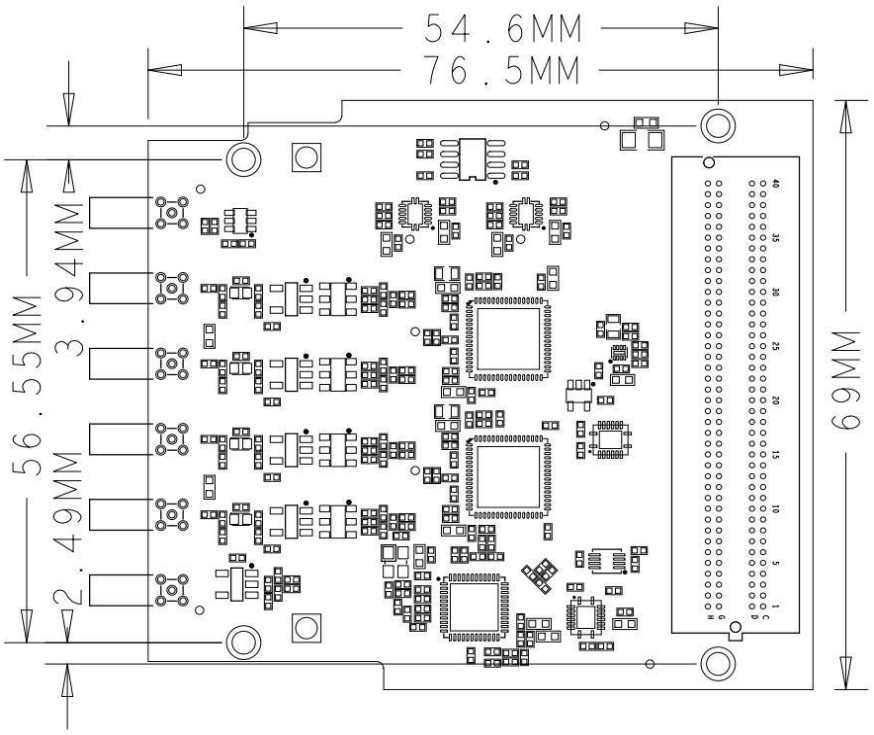


1.1 Parameters of FL2514 Module

The following are the detailed parameters of the FL2514 high-speed AD module:

- AD conversion chip: 2 ZGAD250D14
- AD conversion channel: 4 channels
- AD sampling rate: 250MSPS
- AD sampling data bits: 14
- AD analog signal input range: 1.5V P-P
- AD input impedance: 50 ohms
- Analog signal input interface: SSMC interface
- External clock input: 1 channel
- External trigger signal input: 1 channel
- Digital interface level standard: LVDS level
- Configuration interface: SPI interface
- Working temperature: -40°~85°

1.2 Structure diagram of FL2514 module



Size and dimension of FL2514 module

1.3 Installation and Usage Requirements

The FL2514 module must be used with the development board with the FMC interface, and the FMC of the development board must comply with the FMC standard (ANSI/VITA57.1). The development board provides DC 3.3V, DC 12V, DC VADJ power supplies for the module through FMC connector. The voltage range of the VADJ allowed by the module is 1.65V~3.3V. Considering the LVDS data communication of the FPGA development board, it is generally recommended that the VADJ operate at a voltage of +2.5V or 1.8V.

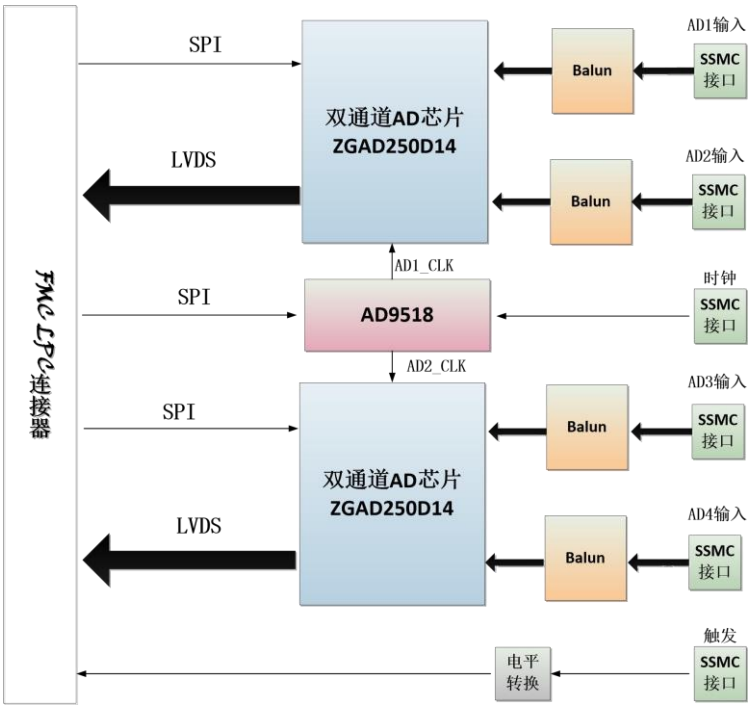
When installing the board, the operator must protect the accuracy. Do not touch the board components directly without electrostatic protection.

The output data of FL2514 module is LVDS signal, the control signal and trigger signal of the board are LVCMOS signals, and the voltage standard depends on the power supply voltage of VADJ.

2. Functions of FL2514 Module

2.1 Schematic Diagram of FL2514

The schematic diagram of FL2514 module is as follows:

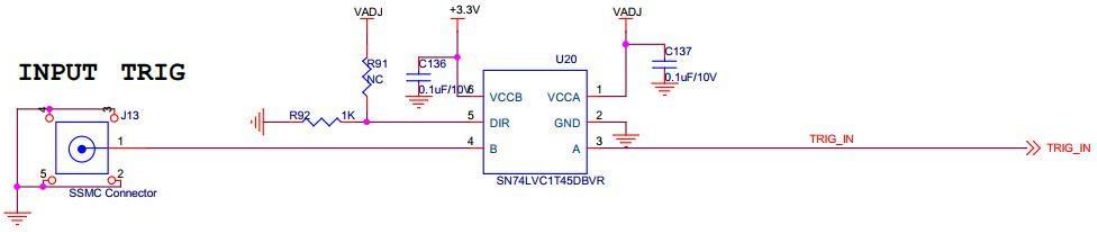


For the specific circuit reference design of ZGAD250D14, please refer to the chip manual.

2.1 Input Interface Description

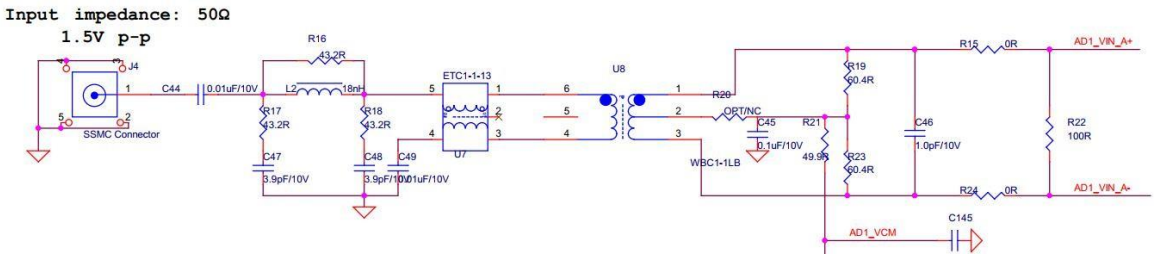
2.1.1 External trigger input interface

The external trigger input supports LVTTL / LVCMOS 3.3V level input mode, which is converted to VADJ level by level conversion chip on board and connected to FMC connector pin.



2.1.2 AD input interface

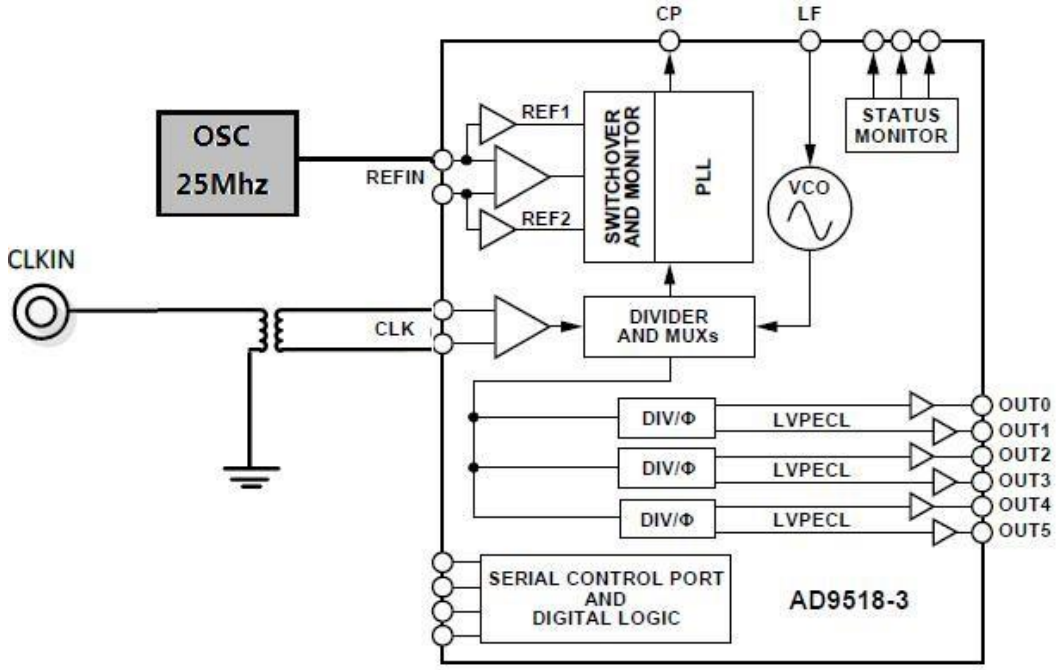
The FL2514 is designed with AC coupled inputs, with a maximum input signal of 300Mhz, input impedance of 50 ohms, and analog signal range of 1.5Vp-p.



2.1.3 Clock input

The on-board clock generation module adopts ADI company’ s AD9518-3 chip and uses the internal VCO. The frequency range of VCO is 1.55G~2.25G. The internal clock and the external reference clock are switched programmatically; The clock module configuration is achieved through the SPI bus connected to the FMC.

The internal reference clock is welded with 25M crystal oscillator by default and connected to REF1 pin of the AD9518; The external reference clock is converted by a transformer into a differential and connected to the CLK+- pin.



2.2 FMC Interface Description

The FMC interface of the FL2514 module is a standard LPC. The following only lists the signal definition of the power supply on the FMC interface and AD chip interface, but the GND signal is not listed. For details, pls refer to the schematic diagram.

Pin Number	Signal Name	Description
C35	+12V	12V power input
C37	+12V	12V power input
D32	+3.3V	3.3V power input
G19	AD1_AD2_MOSI	AD1、AD2 Register configuration input serial port
D20	AD1_CS	AD1 chip selection
G7	AD1_CLKOUT-	AD1's A-channel LVDS data clock output -N.
G6	AD1_CLKOUT+	AD1's A-channel LVDS data clock output -P.
G13	AD1_DA_0_1-	AD1's A-channel LVDS data bits 0 and 1 output -N.
G12	AD1_DA_0_1+	AD1's A-channel LVDS data bits 0 and 1 output -P.
D15	AD1_DA_2_3-	AD1's A-channel LVDS data bits 2 and 3 output -N.
D14	AD1_DA_2_3+	AD1's A-channel LVDS data bits 2 and 3 output -P.
G16	AD1_DA_4_5-	AD1's A-channel LVDS data bits 4 and 5 output -N.
G15	AD1_DA_4_5+	AD1's A-channel LVDS data bits 4 and 5 output -P.
D18	AD1_DA_6_7-	AD1's A-channel LVDS data bits 6 and 7 output -N.
D17	AD1_DA_6_7+	AD1's A-channel LVDS data bits 6 and 7 output -P.
H17	AD1_DA_8_9-	AD1's A-channel LVDS data bits 8 and 9 output -N.
H16	AD1_DA_8_9+	AD1's A-channel LVDS data bits 8 and 9 output -P.
C19	AD1_DA_10_11-	AD1's A-channel LVDS data bits 10 and 11 output -N.
C18	AD1_DA_10_11+	AD1's A-channel LVDS data bits 10 and 11 output -P.
G22	AD1_DA_12_13-	AD1's A-channel LVDS data bits 12 and 13 output -N.
G21	AD1_DA_12_13+	AD1's A-channel LVDS data bits 12 and 13 output -P.
H8	AD1_DB_0_1-	AD1's B-channel LVDS data bits 0 and 1 output -N.
H7	AD1_DB_0_1+	AD1's B-channel LVDS data bits 0 and 1 output -P.
C11	AD1_DB_2_3-	AD1's B-channel LVDS data bits 2 and 3 output -N.
C10	AD1_DB_2_3+	AD1's B-channel LVDS data bits 2 and 3 output -P.
D12	AD1_DB_4_5-	AD1's B-channel LVDS data bits 4 and 5 output -N.
D11	AD1_DB_4_5+	AD1's B-channel LVDS data bits 4 and 5 output -P.
H11	AD1_DB_6_7-	AD1's B-channel LVDS data bits 6 and 7 output -N.
H10	AD1_DB_6_7+	AD1's B-channel LVDS data bits 6 and 7 output -P.
G10	AD1_DB_8_9-	AD1's B-channel LVDS data bits 8 and 9 output -N.
G9	AD1_DB_8_9+	AD1's B-channel LVDS data bits 8 and 9 output -P.
C15	AD1_DB_10_11-	AD1's B-channel LVDS data bits 10 and 11 output -N.
C14	AD1_DB_10_11+	AD1's B-channel LVDS data bits 10 and 11 output -P.
H14	AD1_DB_12_13-	AD1's B-channel LVDS data bits 12 and 13 output -N.

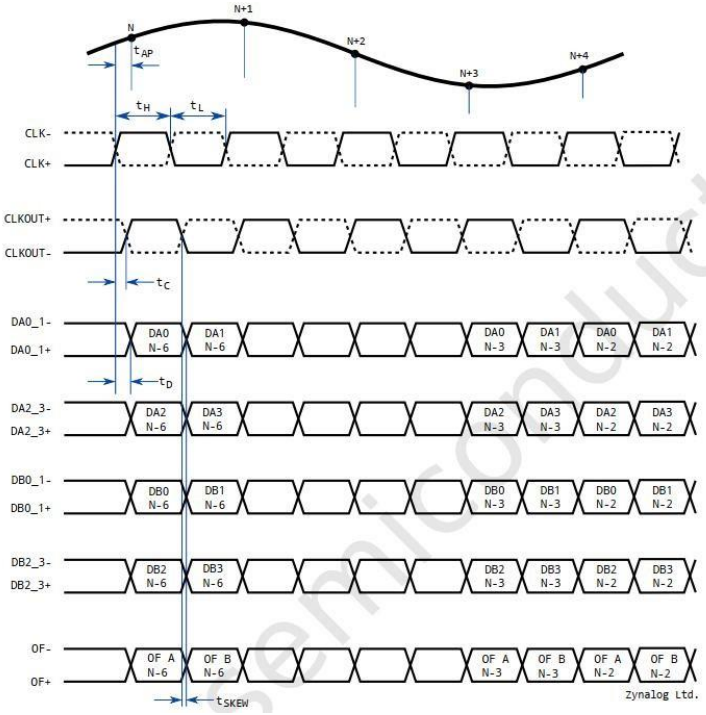
H13	AD1_DB_12_13+	AD1's B-channel LVDS data bits 12 and 13 output -P.
D9	AD1_OR-	The input range of the AD1 channel exceeds the indication -N.
D8	AD1_OR+	The input range of the AD1 channel exceeds the indication -P.
H19	AD2_CS	AD2 chip SPI communication chip selection signal
C23	AD2_CLKOUT-	AD2's A-channel LVDS data clock output -N.
C22	AD2_CLKOUT+	AD2's A-channel LVDS data clock output -P.
G28	AD2_DA_0_1-	AD2's A-channel LVDS data bits 0 and 1 output -N.
G27	AD2_DA_0_1+	AD2's A-channel LVDS data bits 0 and 1 output -P.
G31	AD2_DA_2_3-	AD2's A-channel LVDS data bits 2 and 3 output -N.
G30	AD2_DA_2_3+	AD2's A-channel LVDS data bits 2 and 3 output -P.
H32	AD2_DA_4_5-	AD2's A-channel LVDS data bits 4 and 5 output -N.
H31	AD2_DA_4_5+	AD2's A-channel LVDS data bits 4 and 5 output -P.
G34	AD2_DA_6_7-	AD2's A-channel LVDS data bits 6 and 7 output -N.
G33	AD2_DA_6_7+	AD2's A-channel LVDS data bits 6 and 7 output -P.
H35	AD2_DA_8_9-	AD2's A-channel LVDS data bits 8 and 9 output -N.
H34	AD2_DA_8_9+	AD2's A-channel LVDS data bits 8 and 9 output -P.
G37	AD2_DA_10_11-	AD2's A-channel LVDS data bits 10 and 11 output -N.
G36	AD2_DA_10_11+	AD2's A-channel LVDS data bits 10 and 11 output -P.
H38	AD2_DA_12_13-	AD2's A-channel LVDS data bits 12 and 13 output -N.
H37	AD2_DA_12_13+	AD2's A-channel LVDS data bits 12 and 13 output -P.
D24	AD2_DB_0_1-	AD2's B-channel LVDS data bits 0 and 1 output -N.
D23	AD2_DB_0_1+	AD2's B-channel LVDS data bits 0 and 1 output -P.
H23	AD2_DB_2_3-	AD2's B-channel LVDS data bits 2 and 3 output -N.
H22	AD2_DB_2_3+	AD2's B-channel LVDS data bits 2 and 3 output -P.
C27	AD2_DB_4_5-	AD2's B-channel LVDS data bits 4 and 5 output -N.
C26	AD2_DB_4_5+	AD2's B-channel LVDS data bits 4 and 5 output -P.
G25	AD2_DB_6_7-	AD2's B-channel LVDS data bits 6 and 7 output -N.
G24	AD2_DB_6_7+	AD2's B-channel LVDS data bits 6 and 7 output -P.
H26	AD2_DB_8_9-	AD2's B-channel LVDS data bits 8 and 9 output -N.
H25	AD2_DB_8_9+	AD2's B-channel LVDS data bits 8 and 9 output -P.
D27	AD2_DB_10_11-	AD2's B-channel LVDS data bits 10 and 11 output -N.
D26	AD2_DB_10_11+	AD2's B-channel LVDS data bits 10 and 11 output -P.
H29	AD2_DB_12_13-	AD2's B-channel LVDS data bits 12 and 13 output -N.
H28	AD2_DB_12_13+	AD2's B-channel LVDS data bits 12 and 13 output -P.

H20	AD2_OR	The input range of the AD2 channel exceeds the indication
G3	CLK_CS	SPI communication chip selection signal of clock chip
G2	CLK_SCLK	SPI communication clock signal of clock chip and AD
G18	CLK_SDIO	SPI communication data two-way signal of clock chip
H5	FPGA_CLK-	FPGA reference clock input -N
H4	FPGA_CLK+	FPGA reference clock input -P
C34	GA0	EEPROM address bit 0 bit
D35	GA1	EEPROM address bit 1 bit
C30	SCL	EEPROM I2C clock
C31	SDA	EEPROM I2C data
D21	TRIG_IN	Trigger input signal
G39	VADJ	VADJ power input
H40	VADJ	VADJ power input

3. AD Sampling Timing and Design

3.1 FL2514 Digital Output Timing

The digital output of the ZGAD250D14 dual-channel AD is configured in LVDS output mode. Two channels (A and B) share a pair of differential clock signals and six pairs of differential data signals, and double data rate DDR sampling is performed. The AD data output is shown in the following figure.

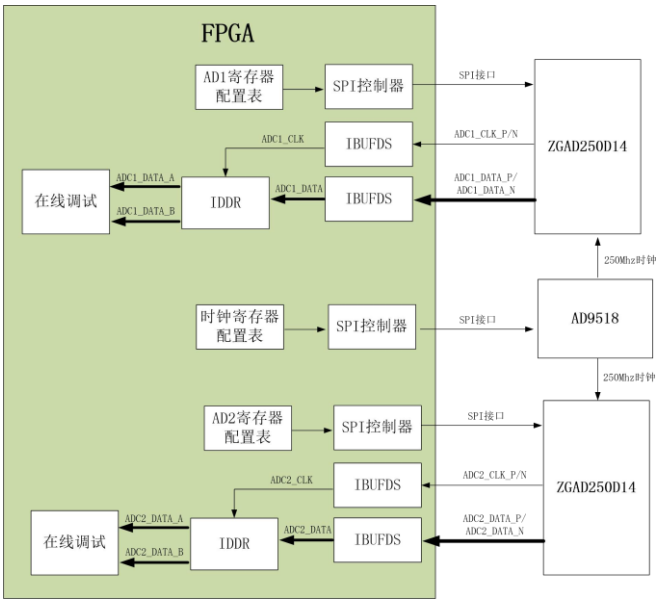


3.2 FL2514 Program Design

We offer routines for AD acquisition and display of the development board. In this routine, the differential LVDS clock signal and differential LVDS data signal input by two ZGAD250D14 chips are converted into single-ended signals respectively through the differential to single-ended module. The 14-bit data is then converted into 14-bit data in channel A and 14-bit data in channel B through the IDDR module. The 14-bit data of channel A and channel B is observed through online debugging.

After power-on, the register of clock chip AD9518 needs to be configured through SPI interface first, so that the 250Mhz differential clock is output to the ZGAD250D14 chip. In addition, the register of the ZGAD250D14 should be configured through the SPI interface.

The functional diagram of FPGA AD test is as follows:



The following is a simple functional introduction to the main modules used in the FPGA program:

1. ad2512_lut_config.v

ZGAD250D14 chip register configuration table. The chip involves the configuration of 5 registers. For specific configuration parameters, pls refer to the program Settings. The following is a description of register functions.

Register 0x00 is the reset register.

地址 (HEX)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	初始值	备注
0x00	RESET	X	X	X	X	X	X	X	0x00	只写
bit7	RESET 软件复位位。写入 0 禁用; 写入 1= 软件复位。复位完成后, 该位自动设置回 0。									
bit6-0	未使用。									

Register 0x01 is the power-off register.

地址 (HEX)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	初始值	备注
0x01	X	X	X	X	SLEEP	LP	PDB	0	0x00	读写
bit7:4	未使用。读回为 0。									
bit3	SLEEP, 休眠位，0= 正常工作模式; 1= 关断整个芯片。									
bit2	Low Power, 低功耗位，0= 正常工作模式; 1= 两个通道均为低功耗模式。									
bit1	Power Down B, 通道 B 关断位, 0 = 正常工作模式; 1= 关断通道 B。通道 A 正常运行。									
bit0	写入 0，写入 1 禁用。									

Register 0x02 is timing register.

地址 (HEX)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	初始值	备注
0x02	X	X	X	X	CINV	CPH1	CPH0	DCS	0x00	读写

bit7:4	未使用。读回为 0。
bit3	CLKOUT inverse, 输出时钟反转位。 0= 正常 CLKOUT 极性 (如图 6所示); 1= 反向 CLKOUT 极性。
bit2:1	CLKOUT PHASE1:CLKOUT PHASE0 输出时钟相位延迟位 00 = 无 CLKOUT 延迟 (如图 6所示) 01 = CLKOUT+/CLKOUT–延迟 45°(时钟周期 • 1/8) 10 = CLKOUT+/CLKOUT–延迟 90°(时钟周期 • 1/4) 11 = CLKOUT+/CLKOUT–延迟 135°(时钟周期 • 3/8) 注意: 如果使用 CLKOUT 相位延迟功能, 则还必须打开时钟占空比稳定器。
bit0	Duty Cycle Stabilizer, 时钟占空比稳定器位。 0 = 时钟占空比稳定器关闭 1 = 时钟占空比稳定器开启

Register 0x03 is an output mode register.

地址 (HEX)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	初始值	备注
0x03	X	X	X	ILVDS2	ILVDS1	ILVDS0	TON	OFF	0x00	读写

bit7:5	未使用。读回为 0。
bit4:2	ILVDS2:ILVDS0 LVDS 输出电流位 000 = 3.5mA LVDS 输出驱动电流 001 = 4.0mA LVDS 输出驱动电流 010 = 4.5mA LVDS 输出驱动电流 011 = 未使用 100 =3.0mA LVDS 输出驱动电流 101 =2.5mA LVDS 输出驱动电流 110 =2.1mA LVDS 输出驱动电流 111 = 1.75mA LVDS 输出驱动电流
bit1	TERMINATION ON, LVDS 内部终端使能位 0 = 内部终端关闭 1 = 内部终端开启。LVDS 输出驱动电流等于 ILVDS2:ILVDS0 设置的电流的 2 倍
bit0	OUTPUT OFF, 数字输出控制位 0 = 启用数字输出 1 = 数字输出被禁用 (高阻抗)

Register 0x04 is data format register.

地址 (HEX)	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	初始值	备注
0x04	TEST2	TEST1	TEST0	ABP	0	TON	RAND	2SC	0x00	读写

bit7:5	OUTTEST2:OUTTEST0 数字输出测试模式位 000 = 所有数字输出 = 0 001 = 所有数字输出 = 1 010 = 交替输出模式。OF, D11-D0 在 0000000000000 和 1111111111111 之间交替 100 = 棋盘格输出模式。OF, D11-D0 在 1010101010101 和 0101010101010 之间交替 注 1: 不使用其他位组合。 注 2: 通道 A 和通道 B 的码型可能不同步。
bit4	ABP 交替位极性模式控制位 0 = 交替位极性模式关闭 1 = 交替位极性模式开启。奇数位 D1,D3,D5...D11 极性反转。
bit3	必须设置为 0
bit2	TEST ON, 启用数字输出测试模式 (输出模式由位 7:5 设置) 0 = 正常模式 1 = 启用数字输出测试模式
bit1	RAND 数据输出随机发生器模式控制位 0 = 随机发生器模式关闭 1 = 随机发生器模式开启
bit0	Twos Complement Mode 补码模式控制位 0 = 偏移二进制数据格式 (Offset Binary Output) 1 = 二进制补码数据格式 (Twos Complement Mode)

2. ad9518_lut_config.v

AD9518 register configuration table. Pls refer to the chip manual for details because there have many registers configured here.

1) spi_config.v

This module configures the AD9518 register by calling the SPI communication module.

2) spi_8bit_config.v

This module configures the ZGAD250D14 register by calling the SPI communication module.

3) top.v

In addition to instantiating the above submodules, the "top" module also implements the following functions:

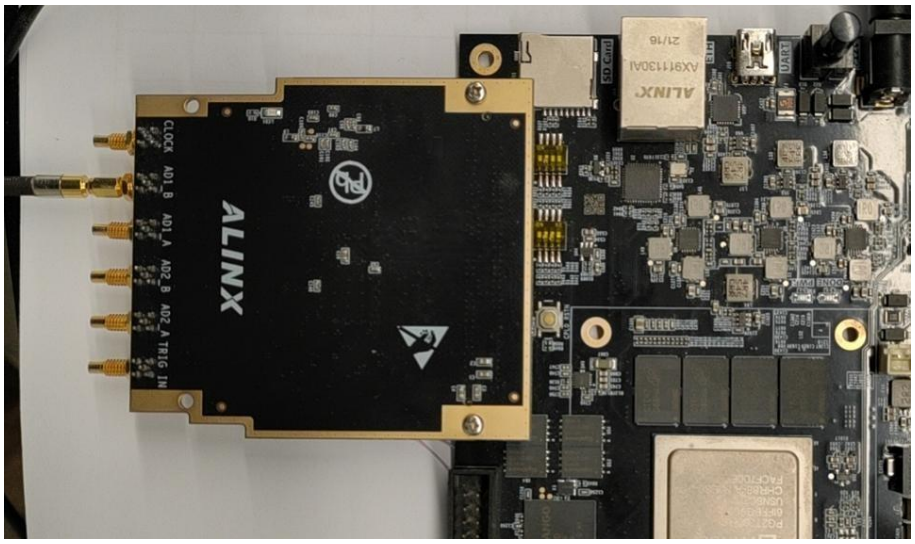
- The IBUFDS primitive is invoked to convert LVDS differential clock signal and data signal into single-ended clock and single-ended data.
- The IDDR primitive is invoked to convert the double-edge data of A and B channels into single-edge data of A and B channels.

3. xdc constraint file

The xdc constraint file defines the pins for communication between the two AD chips and the clock chips.

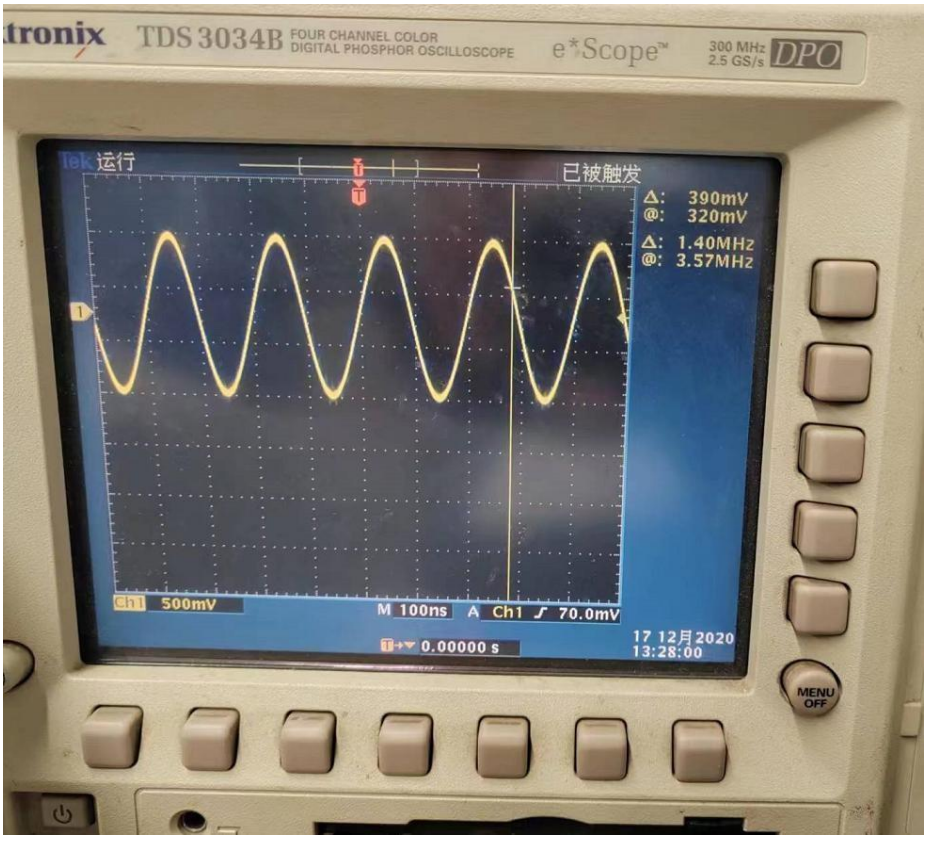
4. Hardware Connection and Testing

The hardware connection between the FL2514 module and the FPGA development board is very simple, as long as the FMC interface and the FMC interface of the development board can be inserted, and then fixed with screws. We use a signal generator to generate analog signals connected to the SMC interface of the AD1_B channel. The following is the hardware connection diagram of the FMC interface of the AXP390 development board and FL2514:

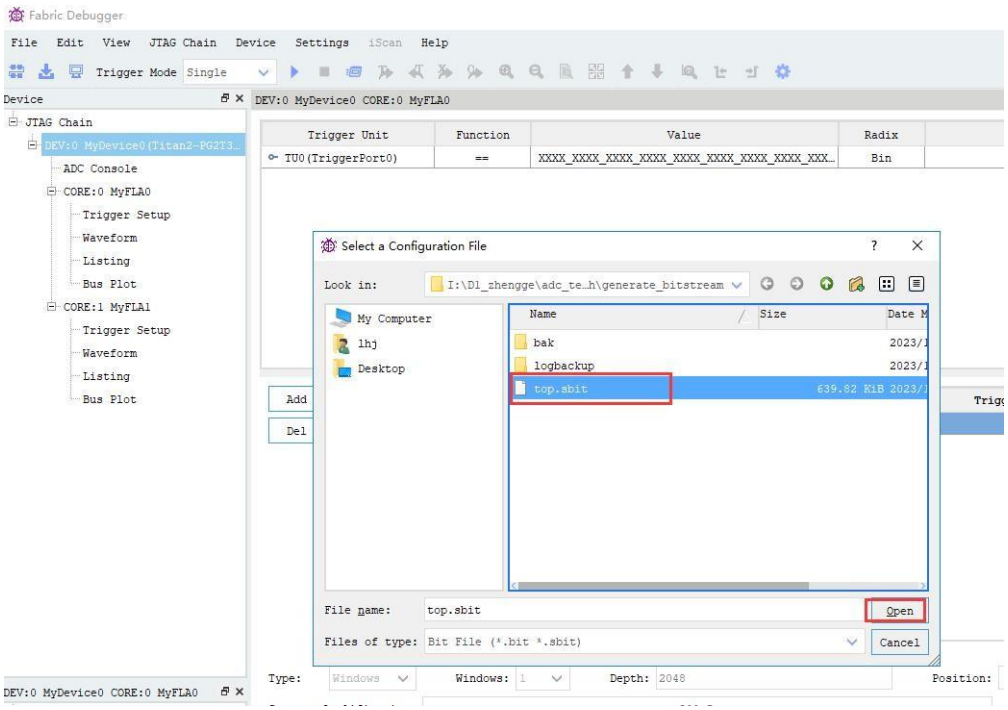


When the development board is powered on, the signal generator generates 1 channel positive selected wave, the frequency is 5Mhz, the internal resistance of the signal generator is set at 50 ohms, and the amplitude peak-to-peak value is 1.5 Vp-p.

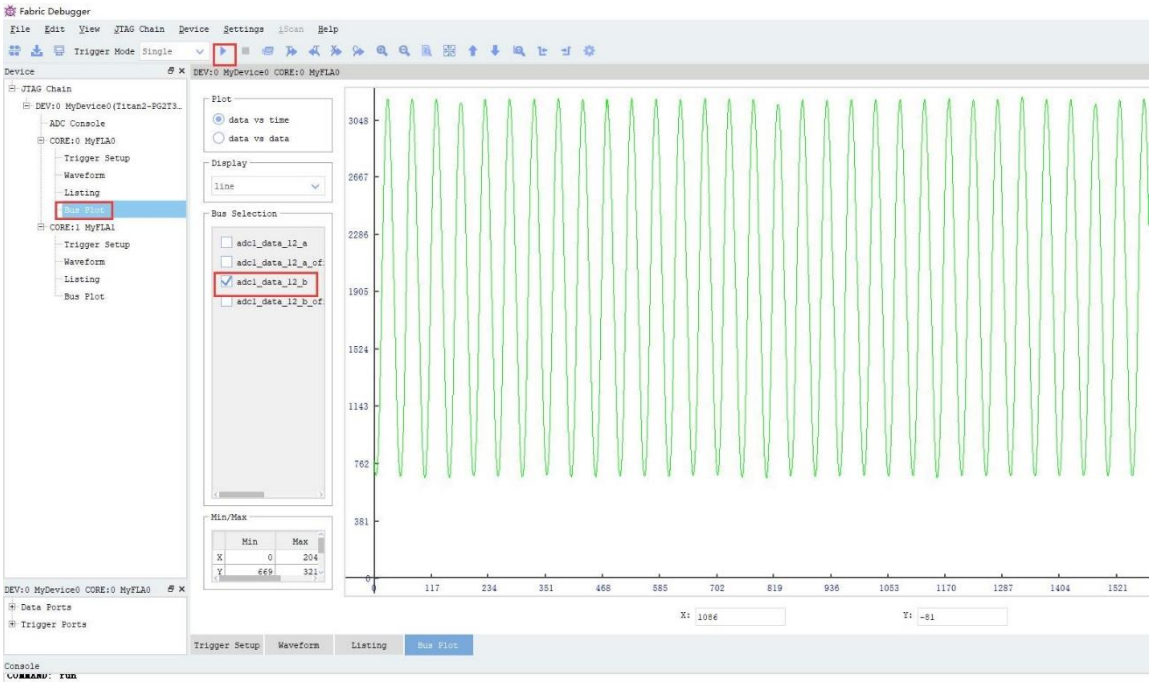
The waveform measured by the AD input signal oscilloscope is as follows:



Then download the program in the co-creator development software PDS.



Click the "Run" button in the online debugging interface and you can see the observed data waveform as shown in the figure below:



The FL2514 DEMO program of Xilinx FPGA board is also provided.