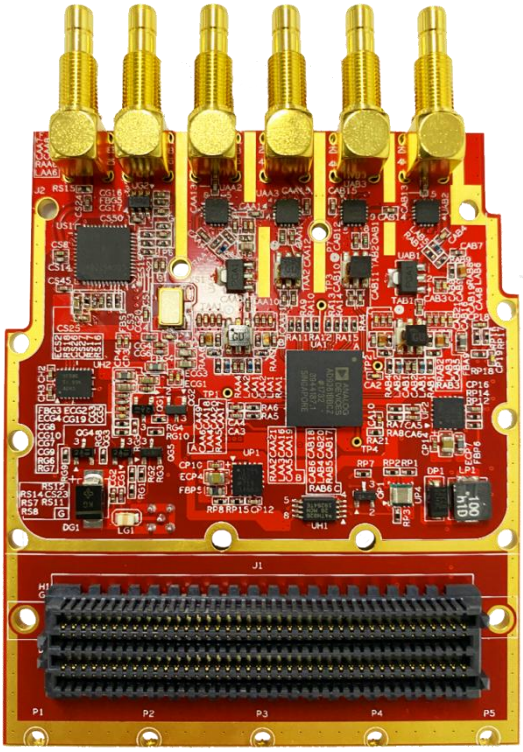
1. Main Features:



- ✓ AD9361
- ✓ 70MHz-6GHz
- ✓ 12bit ADC & 12bitADC
- ✓ Support half-duplex full-duplex, TDD/FDD mode
- ✓ RF impedance matching 50Ω
- ✓ RX maximum 56MHz real-time bandwidth
- ✓ TX maximum 56MHz real-time bandwidth
- ✓ Integrated power amplifier (14dB@2GHz), support transmit power up to 10dBm output
- ✓ Support internal or external reference clocks
- ✓ Parallel digital interface
- ✓ Equipped with GPS module, provide reference clock and pulse synchronization signal through GPS

2. Application Scenarios:

- ✓ 3G/4G micro and macro base stations (BTS)
- ✓ FDD and TDD active antenna systems
- ✓ Portable test equipment

3. Introduction:

The FL6000 highly integrated RF module can cover the 70MHz~6GHz band, and integrates a dual-channel transceiver link. The maximum transmit real-time bandwidth is 56MHz, and the maximum receive bandwidth is 56MHz. Compared with traditional RF front-end, the AD9361 can have advantages of low power-consumption, small dimension and so on, and can guarantee sensitivity and dynamic range performance. FL6000 is suitable for general software radio platforms.

V3 TECHNOLOGY provides FL6000 FPGA reference code, so that users can easily modify the RF working state through the SDK software.

4. System Structure:

The RF front end includes power amplifier, antenna switch, balun and other components to improve the practicability of the device. The main differences between FL6000 and ADI's AD9361 development board are as follows:

- ✓ Transmit end, increase PA
  - ■ Supports a maximum transmit power of 10dBm
- ✓ On-board dual antenna switch, supports TDD and FDD mode switching
  - ■ IO controls the NS-level switching speed
  - ■ High isolation, individual switch 40dB isolation

✓ Flexible reference clock with variable reference through TI clock chip (CDCM6028)

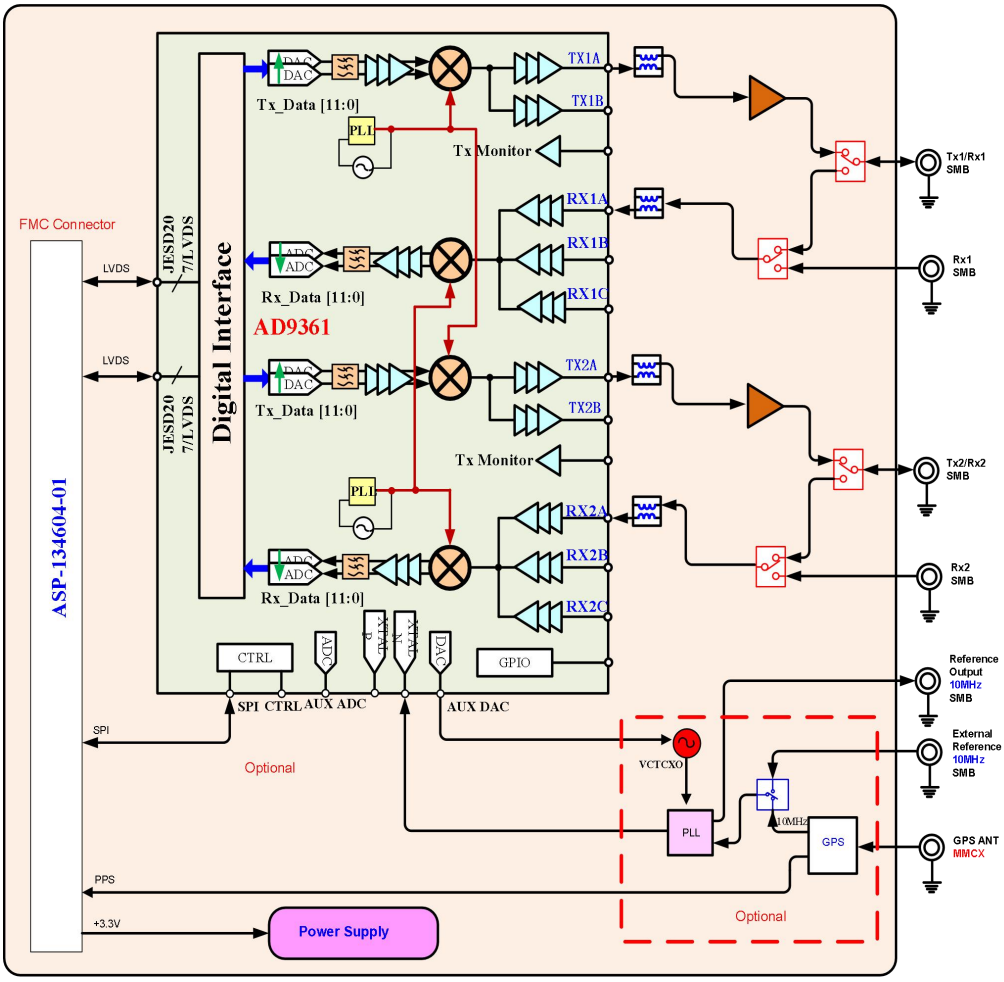
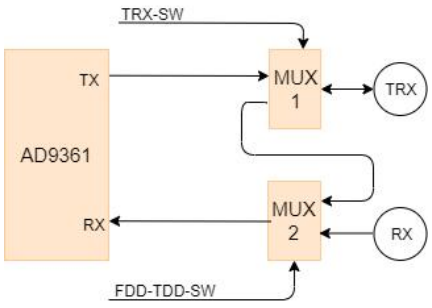
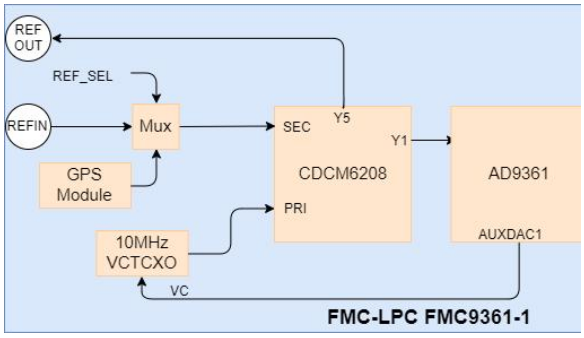


Figure 1: Overall block diagram



Name	1	0
TRX-SW	TX->TRX	TRX->MUX2
FDD-TDD-SW	RX<-RX	MUX1->RX

Figure 2: RF switch



Name	1	0
REF_SEL	REFIN	GPS module

Figure 3: Clock allocation link

5. RF Index:

Table 1: RF Index

	No.	Items	Specifications	Remark
Tx	1	Frequency	70~6000MHz	
	2	Interface	SMB	
	3	Bandwidth	Up to56 MHz	Tx real-time bandwidth, tunable
	4	Transmission Power	10dBm	2500MHz, CW
	5	EVM	<2%	
	6	Gain Control Range	89dB	
	7	Gain Step	0.25dB	
	8	ACLR	< -45dBc	@10dBm output
	9	Spurious	TBD	
	10	SSB Suppression	35dBc	
	11	LO Suppression	45dBc	
	12	DAC Sample Rate (max)	61.44MS/s	
	13	DAC Resolution	12bits	
Rx	1	Frequency	70~6000MHz	
	2	Interface	SMB	
	3	Bandwidth	Up to56 MHz	real-time bandwidth, tunable
	4	Sensitivity:	-90dBm@20MHz	
	5	EVM	<1.5%	
	6	Gain Control Range	>60dB	
	7	Gain Step	1dB	
	8	Noise Figure	<6dB	Maximum RX gain
	9	IIP3 (@ typ NF)	-15dBm	
	10	ADC Sample Rate (max)	61.44MS/s	
	11	ADC Resolution	12bits	
	1	Voltage	3.3V& 12V	
	2	ON/OFF TIME	<6uS	TDD model
	3	Duplexing Model	TDD/FDD	
	4	Power Consumptions	<3W	

6 Pin List:

Table 2 Pin List

Signal Name	FMC Pin Name	FMC Pin	Direction	Description
AD9361 Chip Signal				
CLOCKOUT	LA20_N	G22	Output	Configurable clock output
CTRL_IN0	LA26_P	D26	Output	Configurable control signals
CTRL_IN1	LA22_N	G25	Output	Configurable control signals
CTRL_IN2	LA21_P	H25	Output	Configurable control signals
CTRL_IN3	LA25_P	G27	Output	Configurable control signals
CTRL_OUT0	LA25_N	G28	Input	Configurable control signals
CTRL_OUT1	LA24_N	H29	Input	Configurable control signals
CTRL_OUT2	LA21_N	H26	Input	Configurable control signals
CTRL_OUT3	LA22_P	G24	Input	Configurable control signals
CTRL_OUT4	LA23_N	D24	Input	Configurable control signals
CTRL_OUT5	LA24_P	H28	Input	Configurable control signals
CTRL_OUT6	LA26_N	D27	Input	Configurable control signals
CTRL_OUT7	LA16_N	G19	Input	Configurable control signals
EN_AGC	LA16_P	G18	Input	AGC enable control
ENABLE	LA19_N	H23	Input	TDD switch control
RESETB	LA23_P	D23	Input	Low level reset
TXNRX	LA17_N_CC	D21	Input	TDD switch control
SPI_CLK	LA18_N_CC	C23	Input	SPI bus clock
SPI_CS#	LA19_P	H22	Input	SPI bus chip select
SPI_MISO	LA20_P	G21	Input	SPI bus data
SPI_MOSI	LA18_P_CC	C22	Output	SPI bus data
SYNC_IN	LA17_P_CC	D20	Input	Synchronous trigger signal
RX_CLK_N	CLK0_M2C_N	H5	Output LVDS	Data clock
RX_CLK_P	CLK0_M2C_P	H4	Output LVDS	Data clock
RX_FRAME_N	LA06_N	C11	Output LVDS	Data frame synchronization
RX_FRAME_P	LA06_P	C10	Output LVDS	Data frame synchronization
RXD_N0	LA08_N	G13	Output LVDS	Data
RXD_N1	LA10_N	C15	Output LVDS	Data
RXD_N2	LA04_N	H11	Output LVDS	Data
RXD_N3	LA03_N	G10	Output LVDS	Data
RXD_N4	LA05_N	D12	Output LVDS	Data
RXD_N5	LA02_N	H8	Output LVDS	Data

RXD_P0	LA08_P	G12	Output LVDS	Data
RXD_P1	LA10_P	C14	Output LVDS	Data
RXD_P2	LA04_P	H10	Output LVDS	Data
RXD_P3	LA03_P	G9	Output LVDS	Data
RXD_P4	LA05_P	D11	Output LVDS	Data
RXD_P5	LA02_P	H7	Output LVDS	Data
FB_CLK_N	CLK1_M2C_N	G3	Input LVDS	Data loop clock
FB_CLK_P	CLK1_M2C_P	G2	Input LVDS	Data loop clock
TX_FRAME_N	LA07_N	H14	Input LVDS	Data frame synchronization
TX_FRAME_P	LA07_P	H13	Input LVDS	Data frame synchronization
TXD_N0	LA12_N	G16	Input LVDS	Data
TXD_N1	LA11_N	H17	Input LVDS	Data
TXD_N2	LA13_N	D18	Input LVDS	Data
TXD_N3	LA14_N	C19	Input LVDS	Data
TXD_N4	LA15_N	H20	Input LVDS	Data
TXD_N5	LA09_N	D15	Input LVDS	Data
TXD_P0	LA12_P	G15	Input LVDS	Data
TXD_P1	LA11_P	H16	Input LVDS	Data
TXD_P2	LA13_P	D17	Input LVDS	Data
TXD_P3	LA14_P	C18	Input LVDS	Data
TXD_P4	LA15_P	H19	Input LVDS	Data
TXD_P5	LA09_P	D14	Input LVDS	Data
FL6000 Additional Signal				
CDCM_SPI_CLK	LA29_N	G31	Input	CDCM6208 SPI configuration bus
CDCM_SPI_CS	LA30_P	H34	Input	CDCM6208 SPI configuration bus
CDCM_SPI_MISO	LA31_N	G34	Input	CDCM6208 SPI configuration bus
CDCM_SPI_MOSI	LA30_N	H35	Output	CDCM6208 SPI configuration bus
CDCM_SYNC	LA33_P	G36	Input	CDCM6208 synchronous trigger
GPIO_SCL	SCL	C30	Bi-direction	I2C eeprom AT24CM01
GPIO_SDA	SDA	C31	Bi-direction	I2C eeprom AT24CM01
PPS_1SR	LA32_N	H38	Output	1pps of GPS module
REF_SELECT	LA29_P	G30	Input	1=external reference，0=internal GPS module reference
REF_SELECT2	LA31_P	G33	Input	0=internal VCTCXO crystal oscillator，1=external reference or GPS
FDDTDD_SW	LA28_N	H32	Input	RF switch duplex switching
TRX_SW	LA27_N	C27	Input	RF switch duplex switching

TXD_GPSR	LA32_P	H37	Output	GPS module UART
RXD_GPSR	LA33_N	G37	Input	GPS module UART

All single-ended signal levels range from 1.8V to 2.5V.

7. FMC Power Supply:

The expansion module requires three power supplies:

12V： 1A

3.3V: 1A

VADJ：1A 1.8V~2.5V

8. FL6000 Dimension Drawing:

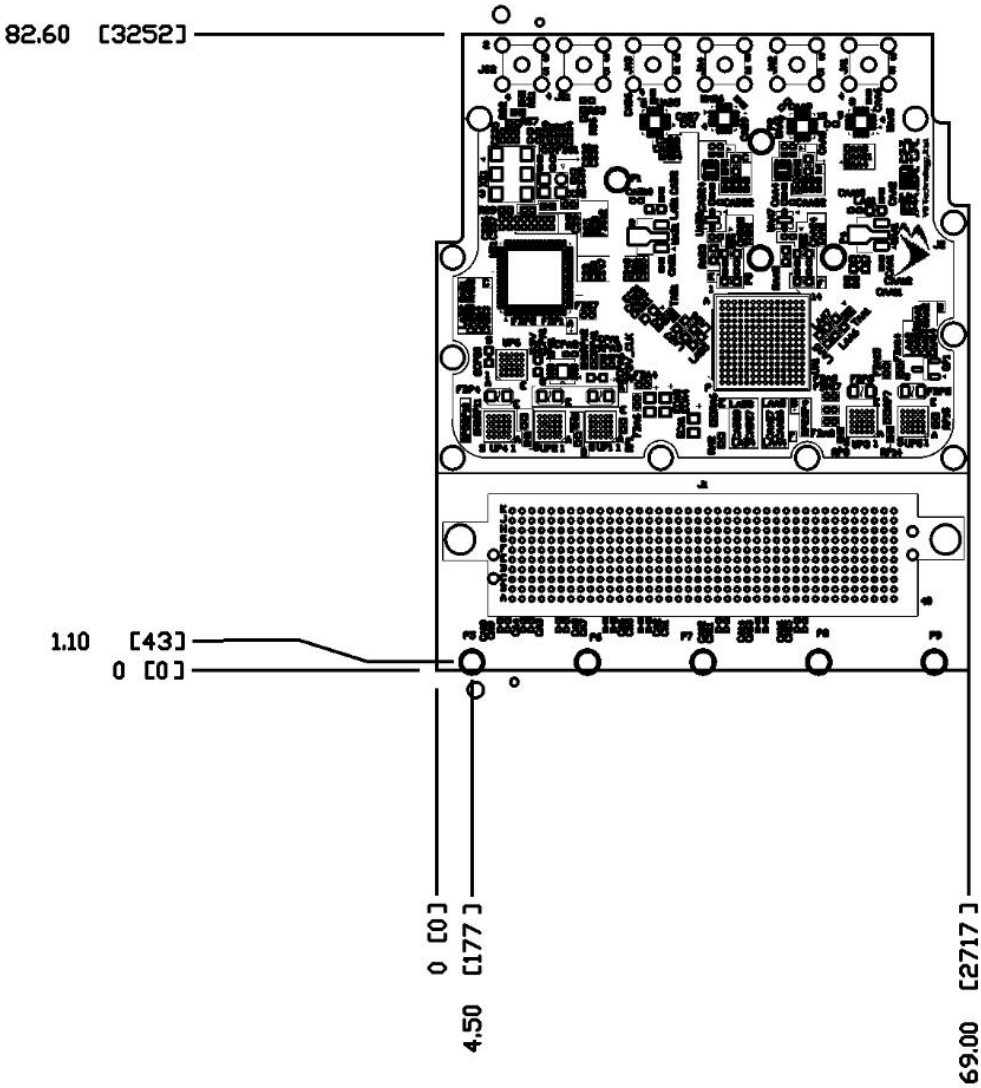


Figure 4: FMC Subboard Diagram

9. FL6000 Physical Drawing:

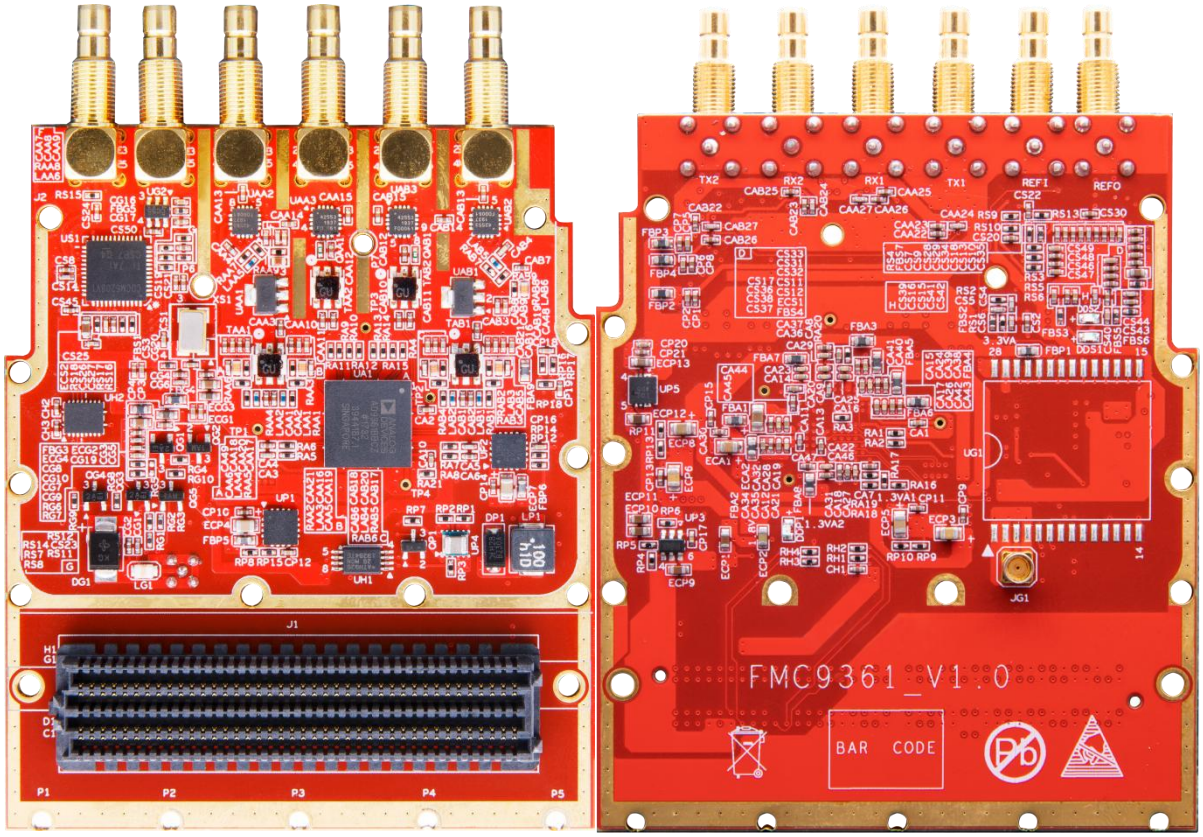


Figure 5: Physical Drawing

10. FL6000 Typical Index Testing:

Table 3: P1dB Output Power

Frequency Point (MHz)	Attenuation Value (mdB) txatt	Output Power (dBm)
500	8e3	13.1
1000	8e3	12.6
1500	6e3	12.1
2000	5e3	12.9
2500	5e3	12
3000	4e3	6.8
3500	2e3	7.5
4000	2e3	10.4
4500	2e3	10.2
5000	2e3	9.4
5500	2e3	6.3
5800	2e3	4.7

Table 4: Receive 5dB Gain P1dB Input Power

Frequency Point (MHz)	P1dB Input (dBm)
500	-10.8
1000	-11.2
1500	-12.1
2000	-11.8
2500	-7
3000	-2.4
3500	2.2
4000	7.2
4500	-3.1
5000	-3.4
5500	-2.5

Table 5: Receive 70dB Gain P1dB Input Power

Frequency Point (MHz)	P1dB Input (dBm)
500	-65.8
1000	-66.2
1500	-67.1
2000	-66.8
2500	-67
3000	-62.4
3500	-62.3
4000	-57.8
4500	-53.1
5000	-53.4
5500	-58.8

Table 6: Sensitivity

Frequency Point (MHz)	Sensitivity (dBm)
500	-85.8
1000	-88.2
1500	-87.1
2000	-86.8
2500	-87
3000	-84.4
3500	-84.3
4000	-81.8
4500	-81.1
5000	-82.4
5500	-83.8

Note: The bandwidth is 30.72MHz, the carrier-to-noise ratio (CNR) threshold is 3.5dB, and the Y520_50 receive gain rx_gain=71.

Table 7: Phase Noise

Y520_50	200MHz	400M	1000M	2000M	2500M	3000M	3800M	4500M	5000M	5500M
100Hz	-86	-82	-75	-71	-68	-66	-63	63	-62	-61
1KHz	-103	-99	-92	-86	-85	-82	-81	-80	-79	-78
10KHz	-105	-102	-95	-89	-88	-85	-84	-82	-81	-80
100KHz	-115	-112	-106	-99	-99	-95	-94	-92	-91	-90
1MHz	-132	-130	-127	-123	-115	-116	-118	-113	-114	-112