Four Channel DA Output FL9781 User Manual

Rev1.0

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Version Record

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Rev 1.0	2024/4/17	Kathy Xia	First Release

Table of Contents

Part 1: Introduction of FMC FL9781 Module

ALINX FL9781 is a 4-channel high-speed DA module. Each DA is a 14-bit digital-to-analog signal with a conversion rate of 500MSPS. Two AD9781 chips of Analog Devices are used for DA conversion of the FMC module. Each AD9781 chip supports two DA outputs, so the two AD9781 chips support four DA outputs in total. The voltage range of analog signal output is -350mV ~ +350mV, and the interface is SSMC.

FL9781 supports external trigger signal input and SSMC interface; clock mode supports internal reference clock input, external reference clock input, and clock selection can be configured through SPI bus.

The electrical and mechanical design of the FL9781 is based on the FMC standard (ANSI/VITA 57.1). It is a standard LPC FMC interface for connecting to an FPGA development board. The FMC connector model is ASP_134604_01.

Photo of FL9781 module is as follows:

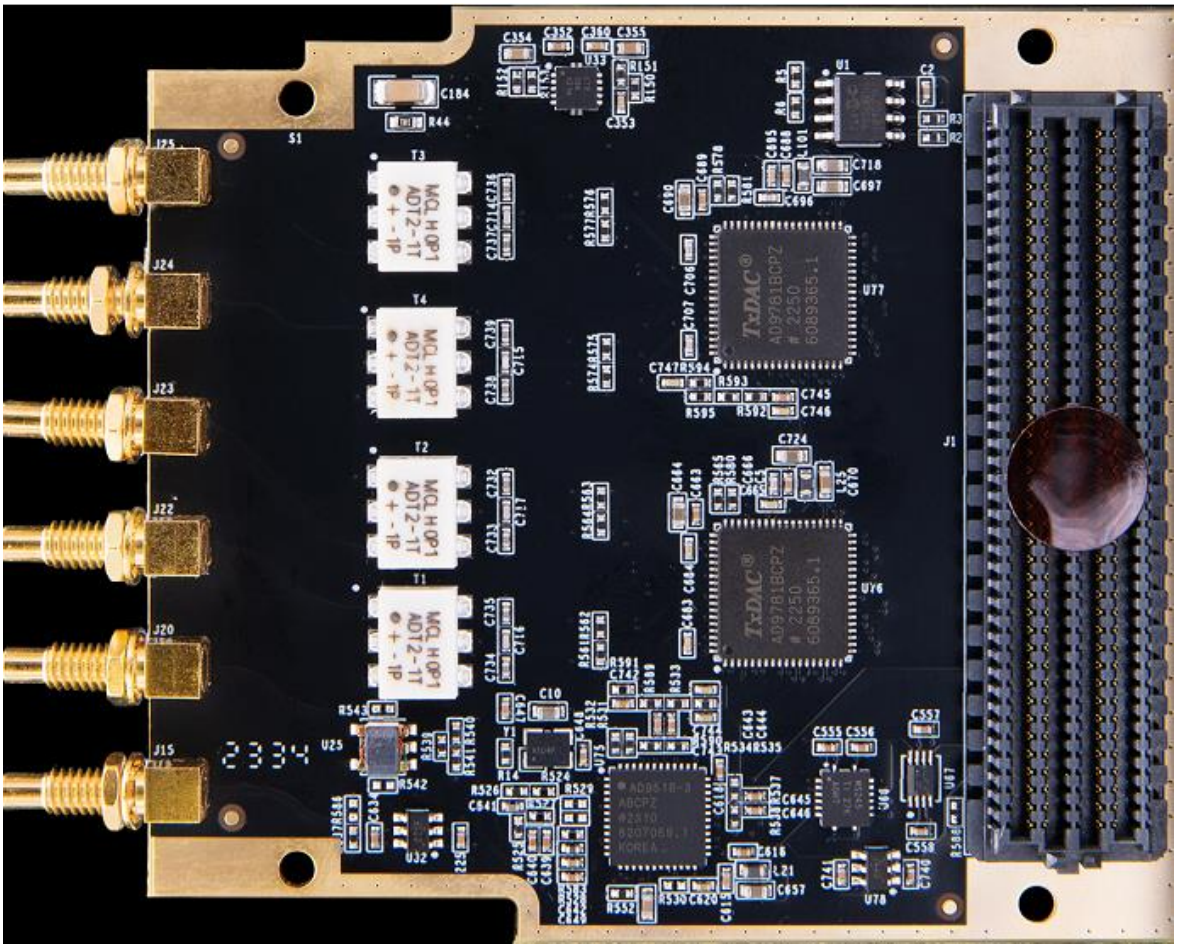

Figure 1: Physical drawing of FL9781 module

Part 1.1: Parameter Description of FMC FL9781 Module

The detailed parameters of the FL9781 high-speed DA module are as follows:

Analog output:

- Output coupling mode: AC coupling

- DA output channels: 4 channels, 14bit, 500MS/s update rate
- Output Impedance: 50 Ohm.
- Full-range output current: 8.66 mA ~ 31.66 mA (default 20 mA)
- Output amplitude range: -350mV ~ +350mV
- Analog signal output interface: SSMC interface

Clock/trigger:

- External clock input: 1 channel
- External trigger/sync signal: 1 input, 3.3V LVCMOS or LVTTL

FMC interface:

- Support for LPC or HPC
- Digital interface level standard: LVDS level 1.8V or 2.5V
- Configuration interface: SPI interface

Work environment:

- Working temperature: -40° ~ 85°
- Power consumption less than 6W

Part 1.2: FL9781 Block diagram of the module

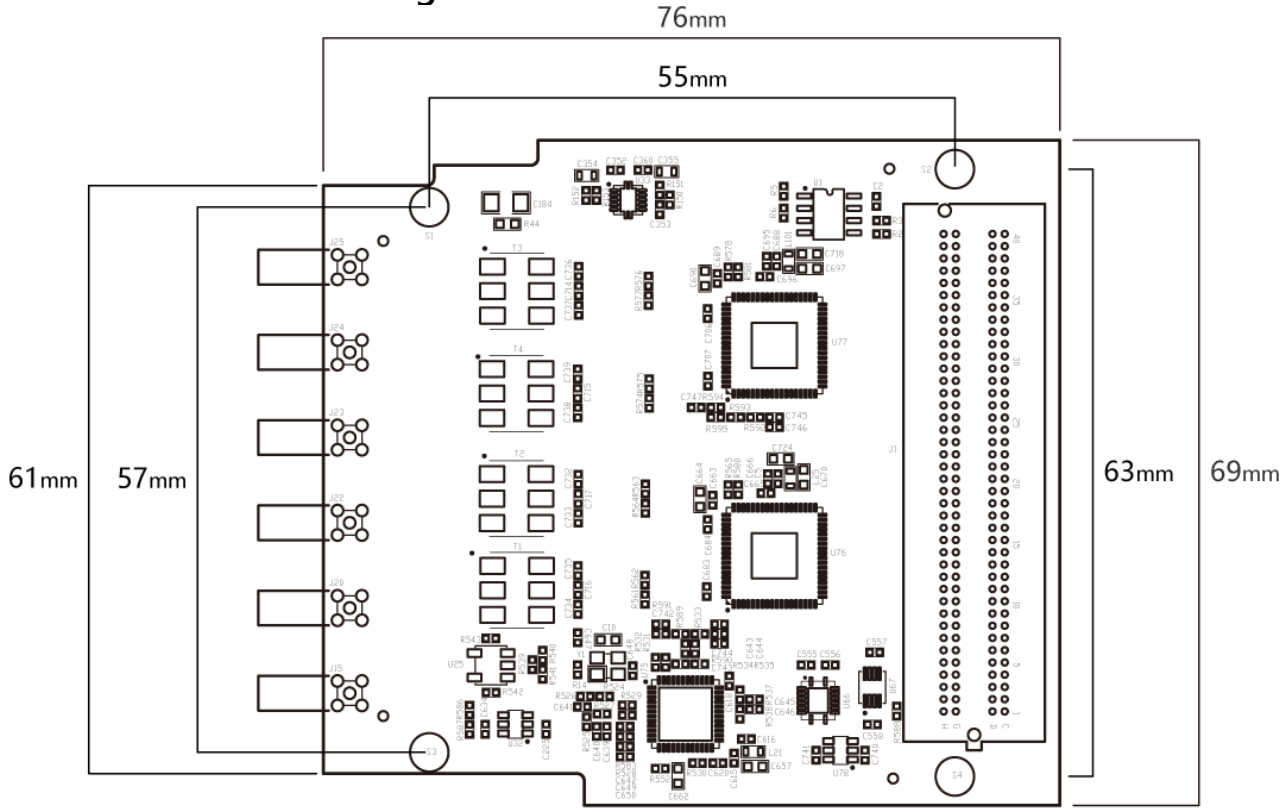

Figure 2: FL9781 High Speed DA Module Dimensional Diagram

Part 1.3: FL9781 Functional Block diagram of the module

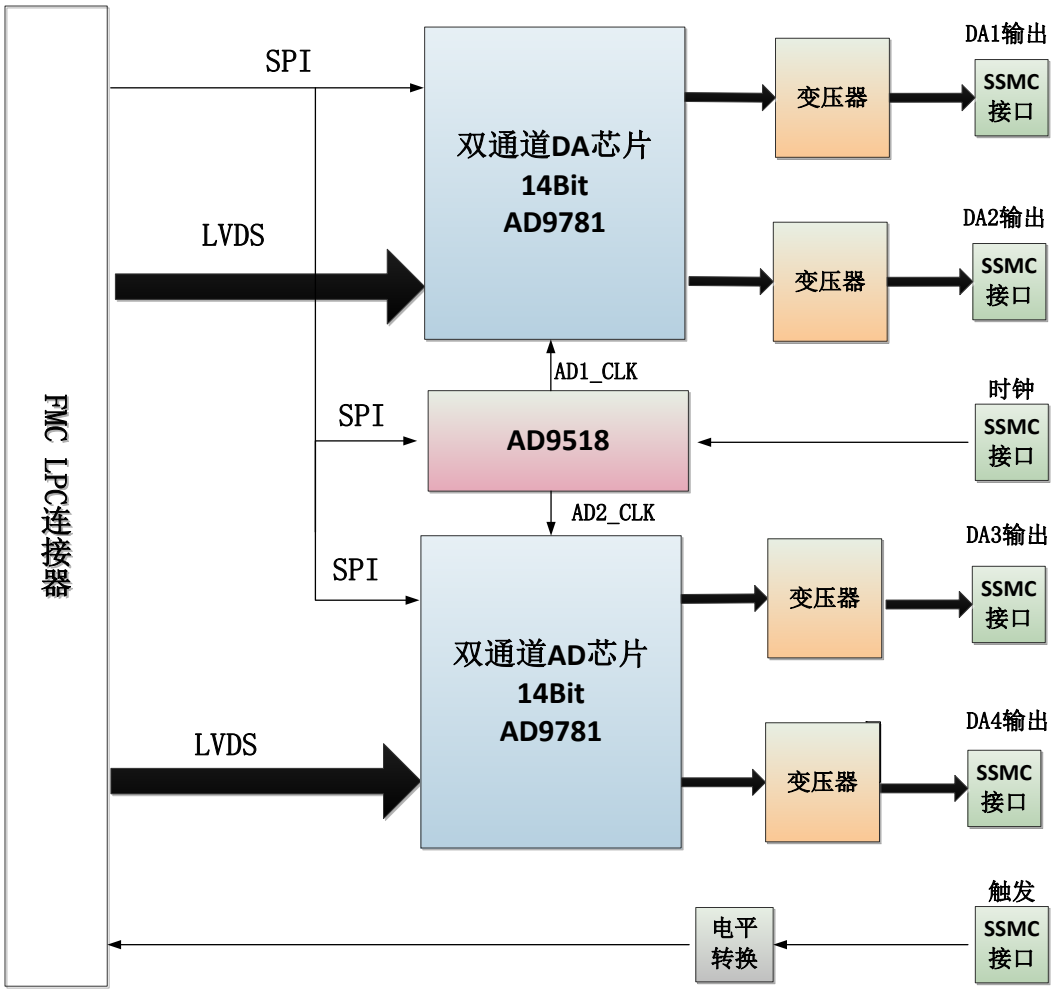

Figure 3: FL9781 Functional block diagram of the module

Please refer to the chip manual of AD9781 for the specific reference design of the circuit of AD9781.

Part 1.4: Interface Description

1) External trigger input interface

The external trigger input supports the LVTTL/LVCMOS 3.3V level input mode. After being converted into the VADJ level by the level conversion chip on the board, it is connected to the FMC connector pin and input to the FPGA chip.

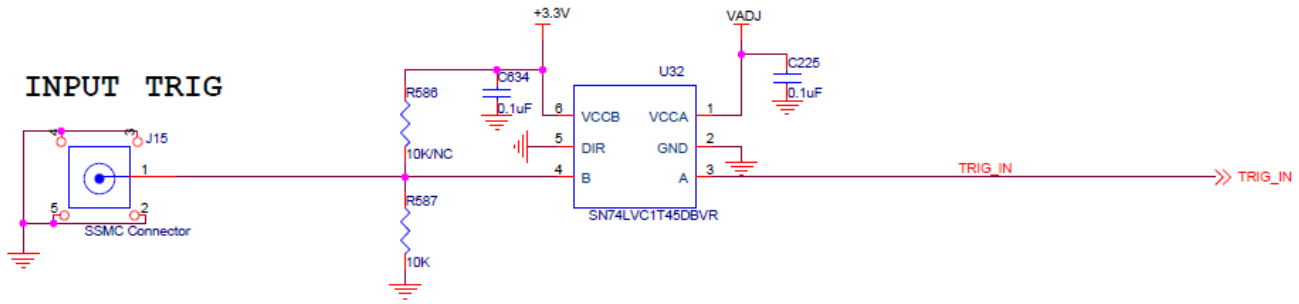

Figure 4: External trigger input interface

2) AD output interface

The output of the FL9613 is designed to be ac-coupled, using a center-tapped transformer as the output interface for the current-output DAC. Transformer coupling provides DC isolation between the DAC output and the final load, helping to suppress common-mode signals present at the DAC output. The maximum output signal is 300Mhz, the output impedance is 50 ohms, and the analog signal range is 0.7Vp-p.

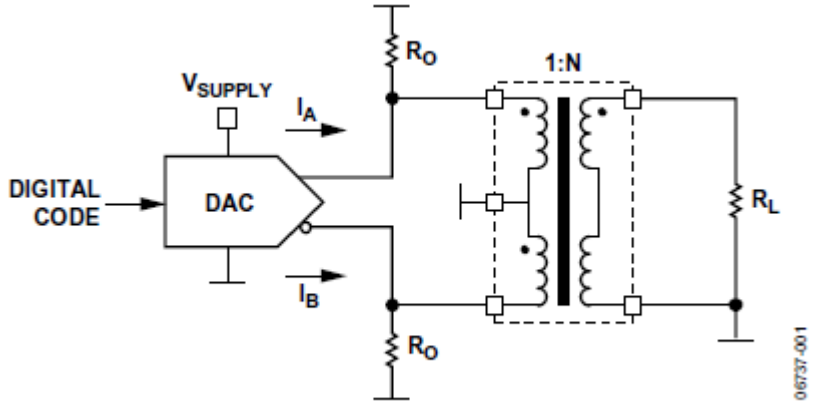

图1 带变压器耦合的平衡电流输出DAC

Figure 5: AD output interface

3) Clock input

The AD9518-3 chip of Analog Devices is selected as the on-board clock generation module, and the design uses an internal VCO with a frequency range of 1.75G ~ 2.25G. The internal clock and the external reference clock are switched by a program, and the clock module configuration is realized by connecting to the SPI bus of the FMC.

By default, the internal reference clock is connected to the REF1 pin of the AD9518 by soldering a 25M crystal oscillator, and the external reference clock is converted into a differential by a transformer and connected to the CLK+-pin.

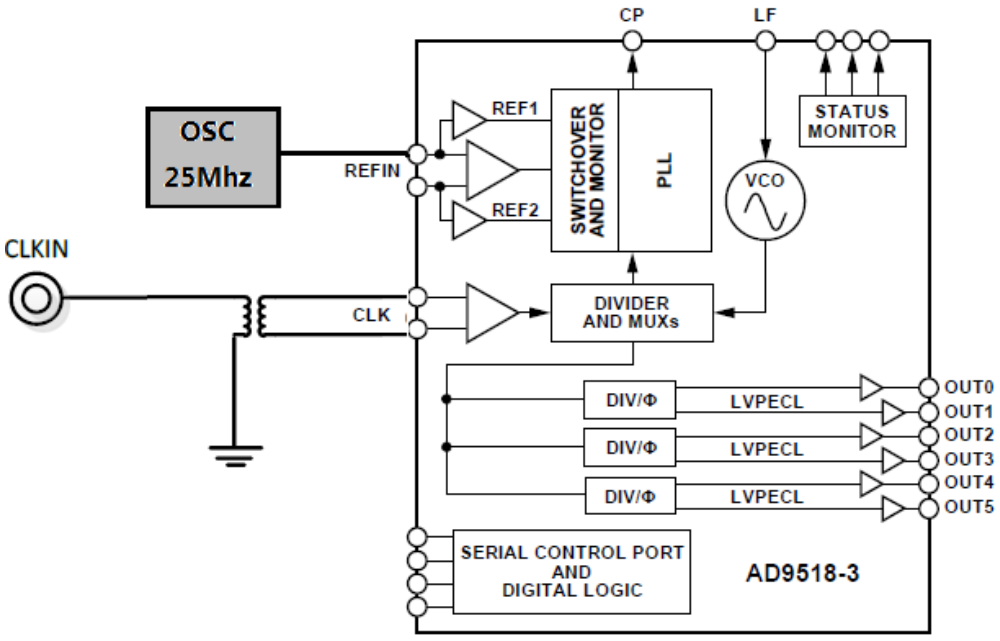

Figure 6: Clock input

Part 1.5: FMC Connector Interface Definition

The FMC interface of the FL9781 module is a standard LPC. Only the signal definitions of the power supply and the DA chip interface on the FMC interface are listed below, and the GND signal is not listed. For details, refer to the schematic diagram. The interfaces are defined as follows:

Pin Number	Signal Name	Description
C35	+12V	12 V power input
C37	+12V	12 V power input
D32	+3.3V	3.3 V Supply Input
D8	P1_DCI_P	Data Clock Output -P for LVDS for DA1 Channel (Align to Output Data)
D9	P1_DCI_N	Data Clock Output -N (Align with Output Data) for LVDS for DA1 Channel
G6	P1_DCO_P	Conversion Clock Input -P for LVDS for DA1 Channel
G7	P1_DCO_N	Conversion Clock Input for LVDS for DA1 Channel -N
G18	P1_D0_P	Data 0 Output -P for LVDS of DA1 Channel
G19	P1_D0_N	Data 0 Output for DA1 Channel LVDS-N
C18	P1_D1_P	Data 1 Output -P for LVDS for DA1 Channel
C19	P1_D1_N	Data 1 Output for LVDS for DA1 Channel -N
H19	P1_D2_P	Data 2 Output -P for LVDS for DA1 Channel
H20	P1_D2_N	Data 2 Output for LVDS for DA1 Channel-N
D17	P1_D3_P	Data 3 Output for DA1 Channel LVDS-P
D18	P1_D3_N	Data 3 Output for DA1 Channel LVDS-N
H16	P1_D4_P	Data 4 Output for DA1 Channel LVDS-P
H17	P1_D4_N	Data 4 Output for DA1 Channel LVDS-N
G15	P1_D5_P	Data 5 Output for DA1 Channel LVDS-P
G16	P1_D5_N	Data 5 Output for DA1 Channel LVDS-N
C14	P1_D6_P	Data 6 Output for DA1 Channel LVDS-P
C15	P1_D6_N	Data 6 Output for DA1 Channel LVDS-N
D14	P1_D7_P	Data 7 Output for DA1 Channel LVDS-P
D15	P1_D7_N	Data 7 Output for DA1 Channel LVDS-N
H13	P1_D8_P	Data 8 Output for LVDS of DA1 Channel -P
H14	P1_D8_N	Data 8 Output for DA1 Channel LVDS-N
G12	P1_D9_P	Data 9 Output for DA1 Channel LVDS-P
G13	P1_D9_N	Data 9 Output for DA1 Channel LVDS-N
D11	P1_D10_P	Data 10 Output for DA1 Channel LVDS-P
D12	P1_D10_N	Data 10 Output for DA1 Channel LVDS-N
H10	P1_D11_P	Data 11 Output for LVDS of DA1 Channel -P
H11	P1_D11_N	Data 11 Output for DA1 Channel LVDS-N
G9	P1_D12_P	Data 12 Output -P for LVDS of DA1 Channel
G10	P1_D12_N	Data 12 Output for DA1 Channel LVDS-N
C10	P1_D13_P	Data 13 Output for LVDS of DA1 Channel -P
C11	P1_D13_N	Data 13 Output for DA1 Channel LVDS-N
C22	P2_DCI_P	Data Clock Output -P for DA2 Channel LVDS (Align to Output Data)
C23	P2_DCI_N	Data Clock Output -N for DA2 Channel LVDS (Align with Output Data
D20	P2_DCO_P	Conversion Clock Input-P for LVDS for DA2 Channel
D21	P2_DCO_N	Conversion Clock Input for LVDS for DA2 Channel -N
H34	P2_D0_P	Data 0 Output -P for DA2 Channel LVDS
H35	P2_D0_N	Data 0 Output for DA2 Channel LVDS-N

H37	P2_D1_P	Data 1 Output -P for DA2 Channel LVDS
H38	P2_D1_N	Data 1 Output for DA2 Channel LVDS-N
G36	P2_D2_P	Data 2 Output for DA2 Channel LVDS-P
G37	P2_D2_N	Data 2 Output for DA2 Channel LVDS-N
G33	P2_D3_P	Data 3 Output for DA2 Channel LVDS-P
G34	P2_D3_N	Data 3 Output for DA2 Channel LVDS-N
H31	P2_D4_P	Data 4 Output for DA2 Channel LVDS-P
H32	P2_D4_N	Data 4 Output for DA2 Channel LVDS-N
G30	P2_D5_P	Data 5 Output for DA2 Channel LVDS-P
G31	P2_D5_N	Data 5 Output for DA2 Channel LVDS-N
C26	P2_D6_P	Data 6 Output for DA2 Channel LVDS-P
C27	P2_D6_N	Data 6 Output for DA2 Channel LVDS-N
H28	P2_D7_P	Data 7 Output for DA2 Channel LVDS-P
H29	P2_D7_N	Data 7 Output for DA2 Channel LVDS-N
G27	P2_D8_P	Data 8 Output for DA2 Channel LVDS-P
G28	P2_D8_N	Data 8 Output for DA2 Channel LVDS-N
D26	P2_D9_P	Data 9 Output for DA2 Channel LVDS-P
D27	P2_D9_N	Data 9 Output for DA2 Channel LVDS-N
H25	P2_D10_P	Data 10 Output for DA2 Channel LVDS-P
H26	P2_D10_N	Data 10 Output for DA2 Channel LVDS-N
G24	P2_D11_P	Data 11 Output for DA2 Channel LVDS-P
G25	P2_D11_N	Data 11 Output for DA2 Channel LVDS-N
D23	P2_D12_P	Data 12 Output -P for DA2 Channel LVDS
D24	P2_D12_N	Data 12 Output for DA2 Channel LVDS-N
H22	P2_D13_P	Data 13 Output for DA2 Channel LVDS-P
H23	P2_D13_N	Data 13 Output for DA2 Channel LVDS-N
G21	P1_SPI_CSB	SPI communication chip select signal of DA1 chip
G22	P2_SPI_CSB	SPI communication chip select signal of DA2 chip
G2	FMC_CLK_CS	SPI communication chip selection signal of clock chip
G3	FMC_SPI_CLK	SPI communication clock signal
H4	FMC_SPI_SDO	SPI communication data signal
H5	FMC_SPI_SDIO	SPI communication bidirectional data signal
H7	TRIG_IN	Trigger input signal
C34	GA0	EEPROM Address Bit 0 Bit
D35	GA1	EEPROM Address Bit 1 Bit
C30	SCL	I2C clock to EEPROM
C31	SDA	I2C data from EEPROM
G39	VADJ	VADJ Supply Input
H40	VADJ	VADJ Supply Input

Table 1: FMC Connector interface Definition

Part 2: Supported development boards

Many ALINX development boards have an FMC LPC interface or an HPC interface, and all development boards with an FMC interface support the FL9781 module. The FL9781 module routines are already available on the following development boards.

The development boards for porting programs are:

Number	Development board model	FMC connector
1	AX7325/AX7325B	J7
2	AX7350	J15
3	AX7450	J7
4	AXKU040	FMC2 (J6)
5	AXKU041	FMC2 (J2)
6	AXKU042	FMC2 (J13)
7	AXU4EV-P	J41
8	AXU5EV-P	J41
9	AXU9EG	J7
10	AXU15EG	J7
11	Z7-P	J13
12	Z19	FMC2 (J33)
13	Z19-P	FMC2 (J19)

Table 2: Development boards for porting programs

Part 3: Hardware connection and test

The hardware connection between the FL9781 module and the FPGA development board is very simple. Just plug the FMC interface into the FMC interface of the development board, and then fix it with screws. We use the SSMC to BNC line to connect to a DAC output to the oscilloscope. The following is the hardware connection diagram of Alinx Z19 Development Board (FMC2) and FL9781:

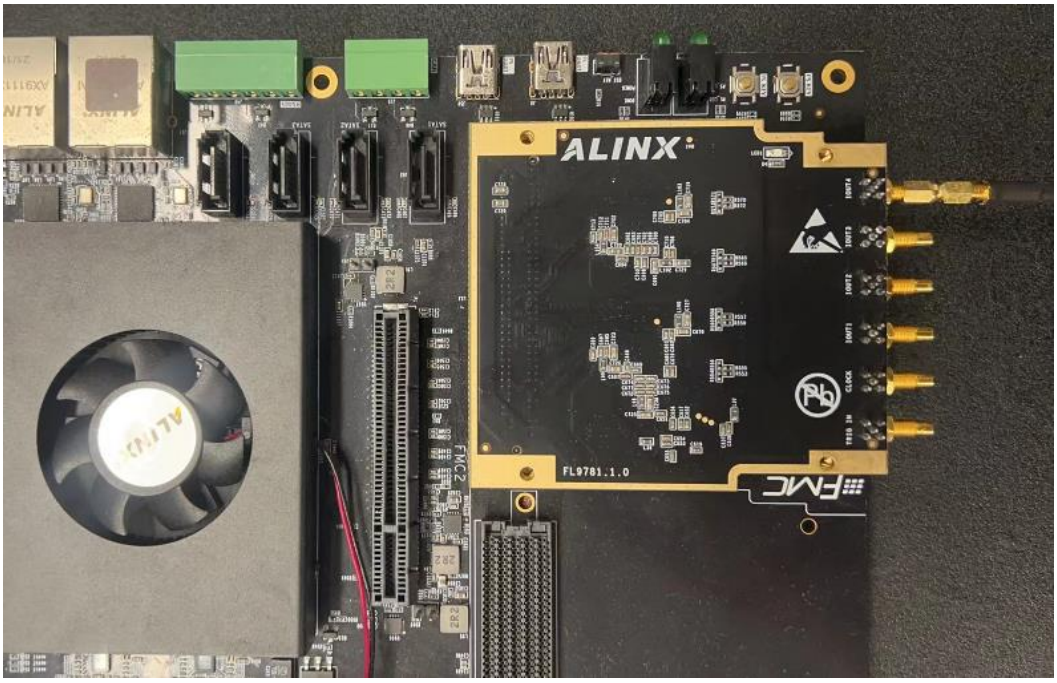

Figure 7: Z19 and FL9781

Power on the development board, connect JTAG, and download the bit test program from the Vivado software. The positive waveform of DA output can be seen in the oscilloscope.

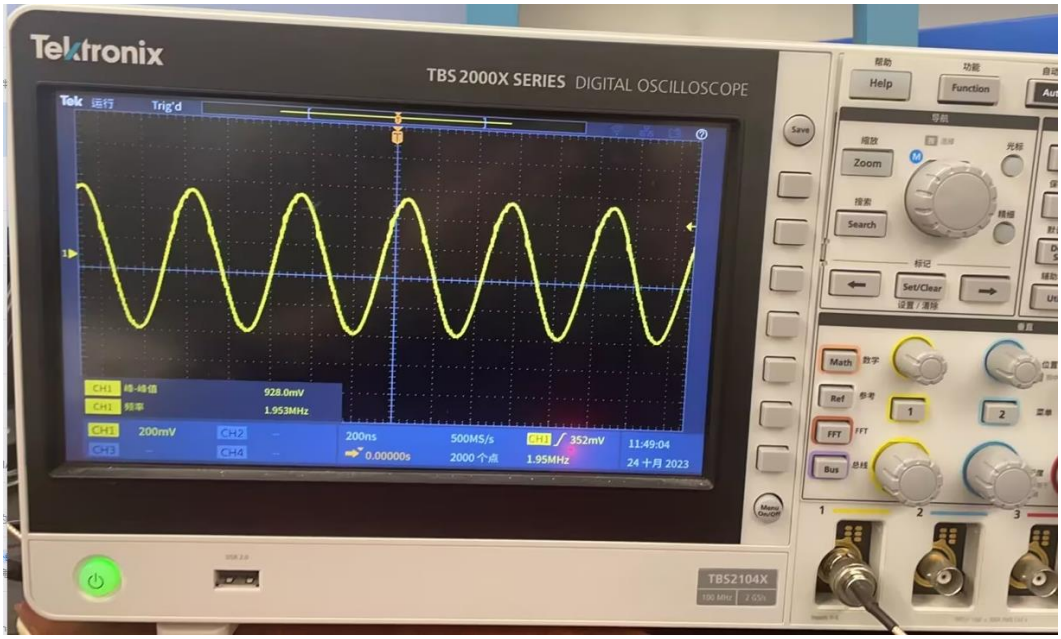

Figure 8: waveform of DA output