GRIDCHIP

GC3355 DATASHEET

GRIDCHIP
2013/11/28

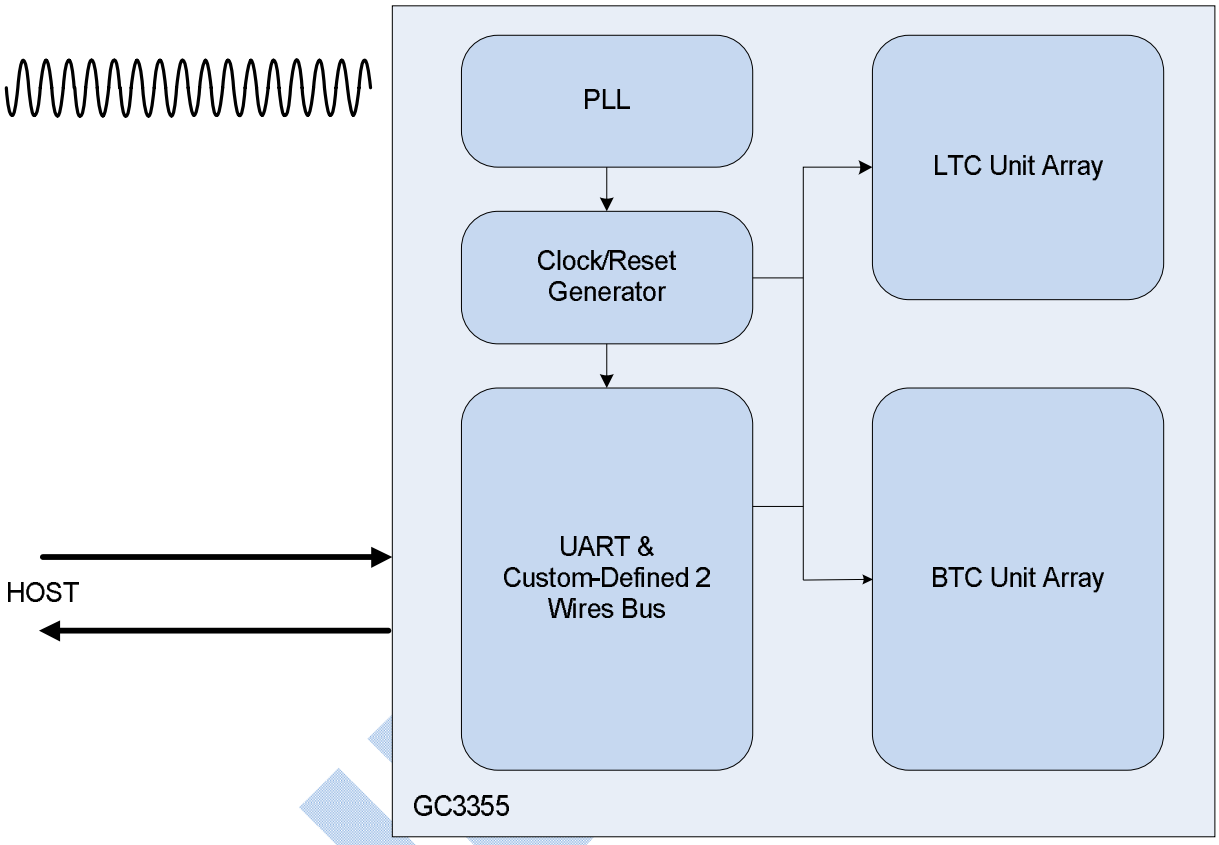
1 GENERAL DESCRIPTION

GC3355 is high performance and low power SHA256 processor designed by GRIDCHIP. With advanced technology and highly integrated design, GC3355 target to provide multiple function and low cost solution in SHA256 application fields.

Key feature:

- 160 BTC Units
- 4 LTC Units
- BTC mode up to 2.25G/s BTC Hash Rate, with 2.4W/GHash
- LTC mode up to 60K/s LTC Hash Rate
- Due-Coin mode up to 1.75G/s BTC Hash Rate + 60K/s LTC Hash Rate, or up to 2.25G/s BTC Hash Rate + 38K LTC Hash Rate
- Highly integrated with PLL and Pre-Calculation Engine
- Support dual configuration and report interface, UART and Custom-Defined 2-Wires Bus
- Support Crystal and Oscillator
- Fully adjustable clock frequency

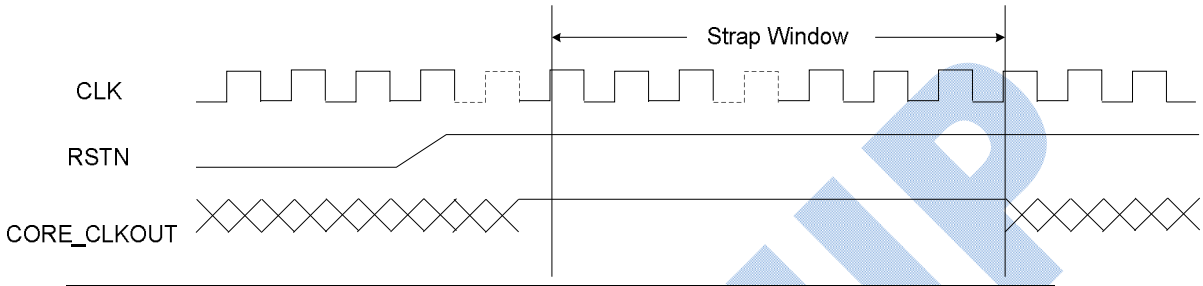
2 CHIP ARCHITECTURE



3 INTERFACE

3.1 Strap

GC3355 supports two type configuration and report interface: UART and Custom-defined 2-wires bus. There is a strap pin on CLKOUT to indicate which protocol should be used.



Strap Pin	Driver	Description
CORE_CLKOUT	PU/PD*	PD: GC3355 UART mode PU: GC3355 Custom-Defined 2 Wires Bus

*Note: PU/PD stands for pull up/pull down.

3.2 UART

The UART (Universal Asynchronous Receiver/Transmitter) provides serial communication capabilities. Serial data is transmitted and received at standard bit rates using the internal baud rate generator. UART is low cost asynchronous serial bus and have low pin counts to save cost. GC3355 is easy to program to support UART speed from 9600bps to 6.25Mbps and. The typical baud rate is 115200bps.

3.3 Custom-Defined 2-Wires Bus

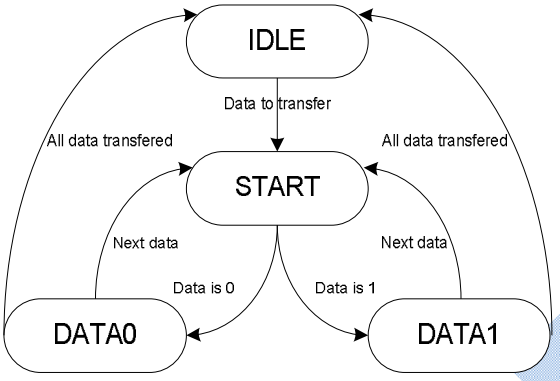
The protocol has 2 Asynchronous Wires to perform transaction: DATA_P and DATA_N. And there are 4 defined states:

IDLE: DATA_P=1 and DATA_N=1;

START: DATA_P=0 and DATA_N=0;

DATA0: DATA_P=0 and DATA_N Rise;

DATA1: DATA_P Rise and DATA_N=0;


IDLE
Data to transfer
All data transfered
All data transfered
START
Next data
Next data
Data is 0
Data is 1
DATA0
DATA1

4 DATA FORMAT

4.1 UART DATA FORMAT

The Data Format in UART mode is defined as below:

Prefix: 0x55AA, this marker indicate the start of new transaction.

Address: 16-bit address, Address combined with Prefix is named ADDR Cycle.

Nth DATA: The Nth 32-bit Data is named DATA Cycle. DATA Cycle includes 4 bytes and order is little endian. For example, the calculation result is 0x12345678; the sequence on UART is 0x78, 0x56, 0x34, and 0x12.

WAIT: Before start a new transaction, WAIT Cycle must be inserted. WAIT Cycle value is programmable register in UART and default wait time is UART receive 32 bits time (One DATA Cycle).

4.2 Custom-Defined 2-Wire Bus

The Data Format in this mode is simpler than UART mode. GC3355 have built-in Pre-Calculation Engine, HOST only need to configure GC3355's registers. The typical sequence is:

IDLE state is must be inserted between 2 transactions.

5 PIN ASSIGNMENT

5.1 Clock and Reset

Pin Number	Pin Name	Direction	Description
56	CORE_CLKOUT	OUT	Strap Pin; Internal Core Clock Divided by 50.
57	RSTN	IN	Chip Asynchronous Reset, Active low
11	XCLKIN	IN	Crystal or Oscillator Clock Input
12	XCLKOUT	OUT	Crystal or Oscillator Clock Output

5.2 Configuration and Report Interface

Pin Number	Pin Name	Direction	Description
16	CHIP_ID0	IN	Chip ID Bit 0, Stable Input
17	CHIP_ID1	IN	Chip ID Bit 1, Stable Input
18	CHIP_ID2	IN	Chip ID Bit 2, Stable Input
1	CFG_P	IN	UART RXD for BTC or DATA_P for Custom defined 2 Wire Bus for Configuration
2	CFG_N	IN	UART RXD for LTC or DATA_N for Custom defined 2 Wire Bus for Configuration
24	RPT_P	OUT OC*	UART TXD for BTC or DATA_P for Custom defined 2 Wire Bus for Report Open-Drain Mode by default
23	RPT_N	OUT OC*	UART TXD for LTC or DATA_N for Custom defined 2 Wire Bus for Report Open-Drain Mode by default
25	RPT_BUSYN	OUT OC*	BTC Unit is Busy, Active low Open-Drain Mode by default
47	LTC_EN	IN	Enable LTC function, Stable Input
48	LTC_BUSYN	OUT OC*	LTC Unit is Busy, Active low Open-Drain Mode by default

*Note: RPT_P, RPT_N, RPT_BUSYN and LTC_BUSYN are Open-Drain mode by default, external Pull up is needed on PCB in this mode. RPT_P, RPT_N, RPT_BUSYN and LTC_BUSYN also can be programmable to normal mode. Please refer to application note for detail.

5.3 Power and Ground

Pin Number	Pin Name	Direction	Description
7	VSSA_PLL	-	PLL Analog VSS
8	VDDA_PLL	-	PLL Analog VDD, 1.0V
9	VDD_PLL	-	PLL Digital VDD, 1.0V
10	VSS_PLL	-	PLL Digital VSS
49	OVDD0	-	IO VDD0, 3.3V
50	OVSS0	-	IO VSS0
32	OVDD1	-	IO VDD1, 3.3V
31	OVSS1	-	IO VSS0
3	DVDD	-	Digital VDD, 1.0V

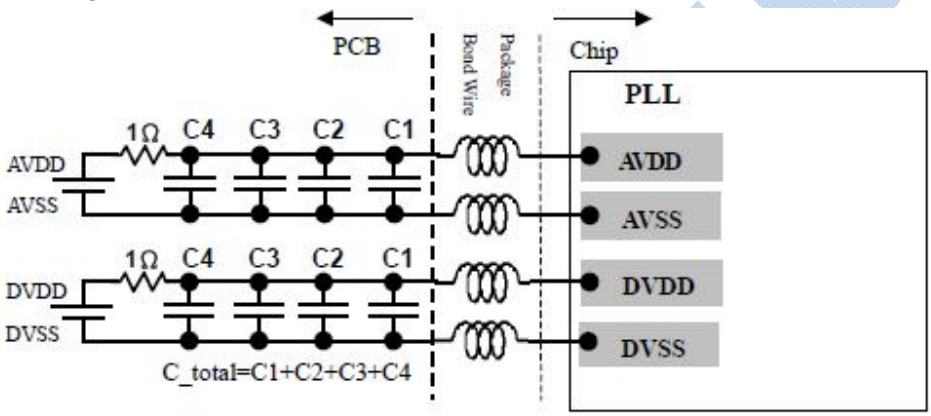
4	DVDD	-	Digital VDD, 1.0V
5	DVDD	-	Digital VDD, 1.0V
6	DVDD	-	Digital VDD, 1.0V
13	DVDD	-	Digital VDD, 1.0V
14	DVDD	-	Digital VDD, 1.0V
19	DVDD	-	Digital VDD, 1.0V
20	DVDD	-	Digital VDD, 1.0V
21	DVDD	-	Digital VDD, 1.0V
22	DVDD	-	Digital VDD, 1.0V
26	DVDD	-	Digital VDD, 1.0V
27	DVDD	-	Digital VDD, 1.0V
29	DVDD	-	Digital VDD, 1.0V
30	DVDD	-	Digital VDD, 1.0V
34	DVDD	-	Digital VDD, 1.0V
35	DVDD	-	Digital VDD, 1.0V
37	DVDD	-	Digital VDD, 1.0V
38	DVDD	-	Digital VDD, 1.0V
39	DVDD	-	Digital VDD, 1.0V
41	DVDD	-	Digital VDD, 1.0V
42	DVDD	-	Digital VDD, 1.0V
43	DVDD	-	Digital VDD, 1.0V
45	DVDD	-	Digital VDD, 1.0V
46	DVDD	-	Digital VDD, 1.0V
51	DVDD	-	Digital VDD, 1.0V
52	DVDD	-	Digital VDD, 1.0V
54	DVDD	-	Digital VDD, 1.0V
55	DVDD	-	Digital VDD, 1.0V
58	DVDD	-	Digital VDD, 1.0V
59	DVDD	-	Digital VDD, 1.0V
60	DVDD	-	Digital VDD, 1.0V
62	DVDD	-	Digital VDD, 1.0V
63	DVDD	-	Digital VDD, 1.0V
15	DVSS	-	Digital VSS
28	DVSS	-	Digital VSS
33	DVSS	-	Digital VSS
36	DVSS	-	Digital VSS
40	DVSS	-	Digital VSS
44	DVSS	-	Digital VSS
53	DVSS	-	Digital VSS
61	DVSS	-	Digital VSS
64	DVSS	-	Digital VSS

6 ELECTRICAL CHARACTERISTICS

6.1 Crystal and Oscillator

PARAMETER	MIN	TYP	MAX	UNIT
Clock Period		40		ns
Clock Frequency		25	50	MHz
Clock Duty Cycle	45	50	55	%
Clock Jitter			50	ps

6.2 PCB Board Design Recommendations



Recommendation of PLL PCB power supply filtering.

components must be implemented to meet the following requirement:

● For IR drop consideration, 1Ω resistor of the filter is recommended for loading PLL current only.

● Choose SMD ceramic high-frequency capacitors:

— Decide VCO maximum oscillating frequency (Fvco).

— Choose SMD ceramic high-frequency capacitors C1 which serial resonance frequency (SRF) is close to Fvco.

— Choose SMD ceramic high-frequency capacitors C2 and C3 by the relationship with C1. (C1, C2 and C3 must be the sameproduce series and dimension)

C2=2*C1, C3=2*C2

— Choose SMD ceramic high-frequency capacitors C4 by composing C_total to form a less than 100KHz pole of power supply filter.

Fc_filter=1/(2*pi*R*C_total) < 100KHz

● Total parasitic inductance, including of wire bond + Lead frame (or Flip Chip) + PCB trace length, should be as short as possible. The rule of thumb is less than 10 nH.

● All SMD ceramic high-frequency capacitors best be placed as close as to power and GND pins and shorten the current loop as short as possible.

● Use wide traces for power and ground path.

● Minimize the loop area from AVDD to AVSS and from DVDD to DVSS.

Besides, take care of layout to avoid coupling noise from adjacent digital signals or digital power traces.

Example:
Find maximum VCO oscillating frequency of PLL and choice capacitor from vender's datasheet.
(Fvco=1000MHz as example.)

Capacitor	SRF(MHz)	Capacitance (F)	Remark
C1	~1000	22p	Murata ERB21 series
C2	~800	43p	Murata ERB21 series
C3	~450	91p	Murata ERB21 series
C4	N.A.	2.2u	Murata GMR21-X7R series

Cx_total= 22p+43p+91p+2.2u
R=1 ohm
Fc_filter=1/(2*pi*R*Cx_total) =72.3KHz < 100KHz

6.3 Operation Condition

PARAMETER	MIN	TYP	MAX	UNIT
Core Supply Power	0.7	1.0	1.2	V
PLL Supply Power	0.9	1.0	1.1	V
IO Supply Power	2.5	3.3	3.6	V
Operating Temperature	-20	25	85	℃
DVDD Operation Current			5000	mA
Power Consumption			5000	mW

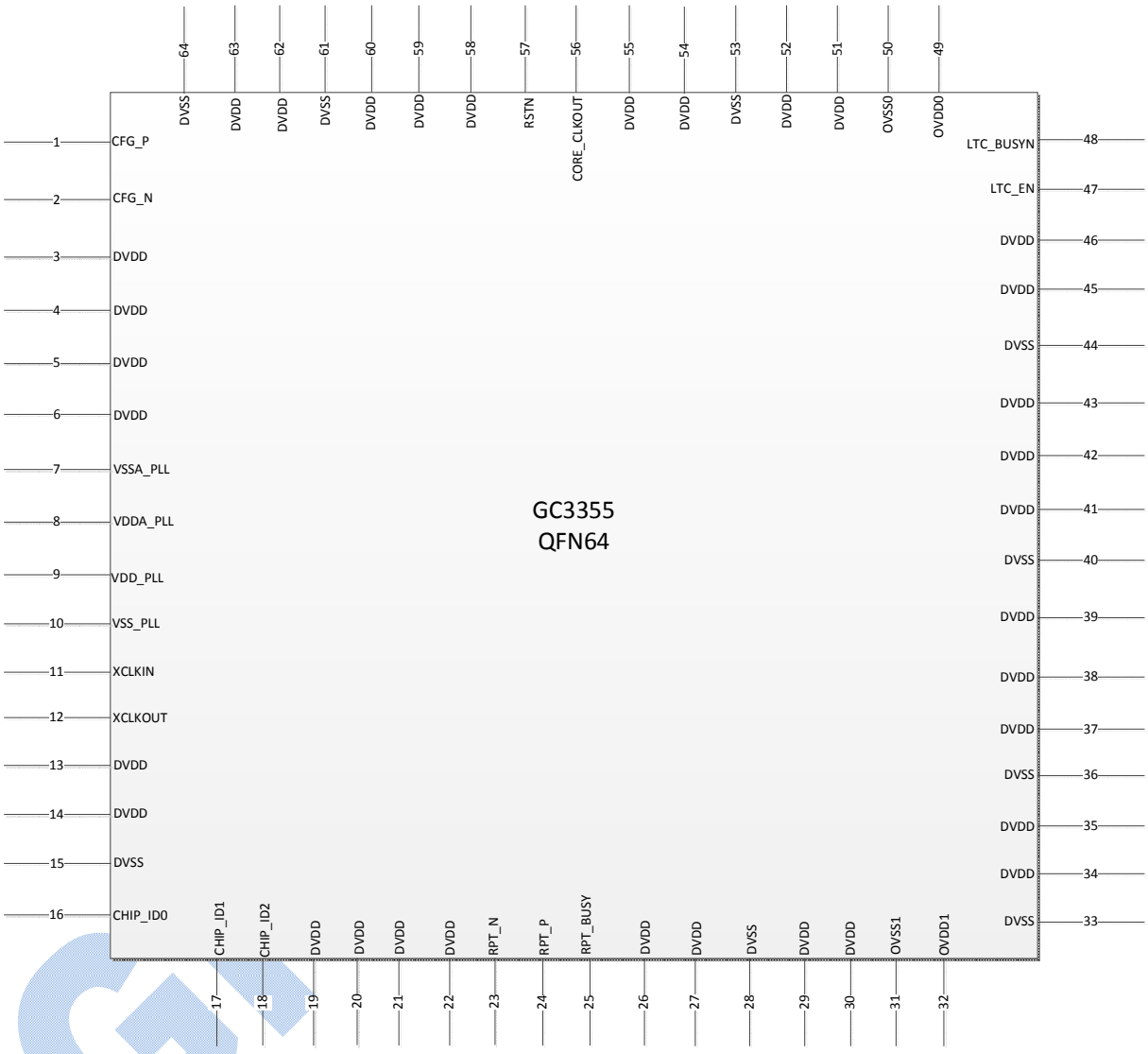
6.4 Power Consumption

The following is the power consumption under 1.0V DVDD condition (Unit: Watt). Gridchip will release more accurate power consumption data after mass production of ASIC Chip and Mining machine.

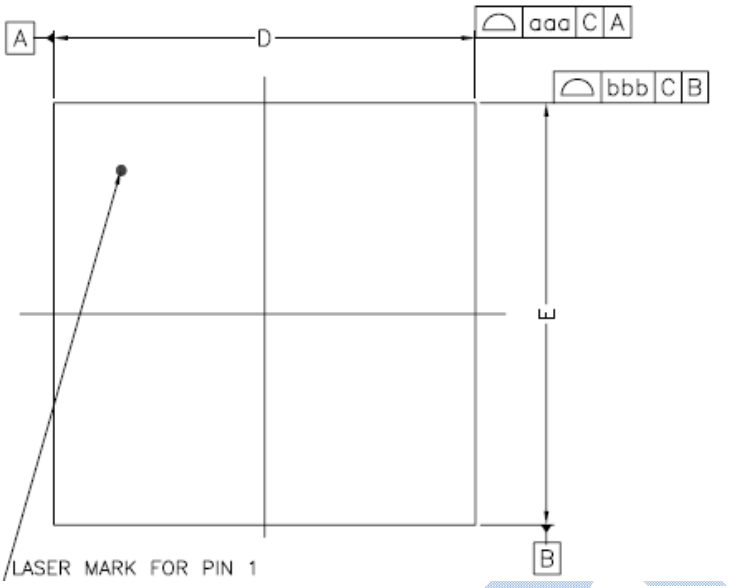
Freq(MHz)	BTC HashRate(G)	LTC HashRate(K)	Power of BTC Mode	Power of BTC+LTC Mode	Power of LTC Mode
400	1000	34.0	2.35	2.64	0.28
500	1250	42.6	2.92	3.27	0.33
550	1375	46.8	3.25	3.58	0.35
600	1500	51.1	3.49	3.90	0.39
650	1625	55.3	3.81	4.23	0.41
700	1750	59.6	4.20	4.56	0.44
750	1875		4.40	X	X
800	2000		4.70	X	X
850	2125		5.00	X	X
900	2250		5.30	X	X

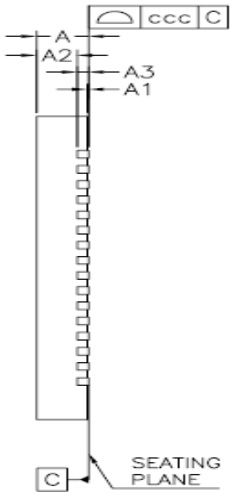
7 PACKAGE INFORMATION

7.1 Package Diagram

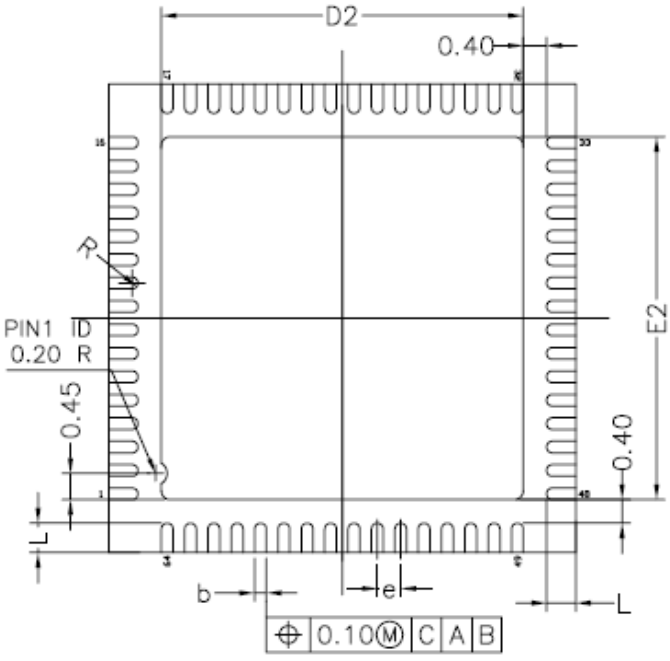


7.2 MECHENICAL CHARACTERISTICS





SIDE VIEW



BOTTOM VIEW

* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	8.00 bsc			0.315 bsc		
D2	6.10	6.20	6.30	0.240	0.244	0.248
E	8.00 bsc			0.315 bsc		
E2	6.10	6.20	6.30	0.240	0.244	0.248
L	0.45	0.50	0.55	0.018	0.020	0.022
e	0.40 bsc			0.016 bsc		
R	0.08	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

8 REVISION HISTORY

Revision	Data	Description
1.0	2013/11/28	Initial version.