

Nervous Systems (On Chip)

Martin A. Trefzer

martin.trefzer@york.ac.uk

Bio-inspired Systems and Technology Lab
School of Physics, Engineering and Technology

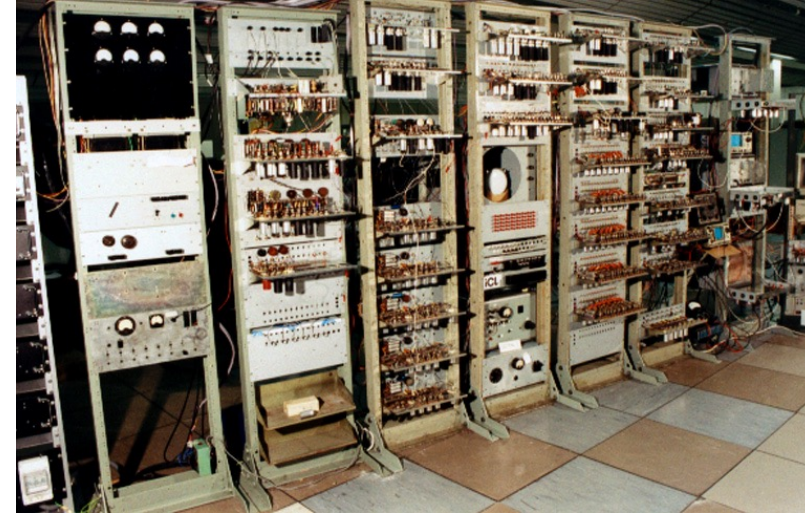
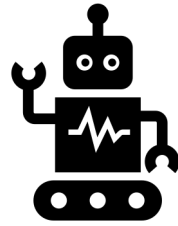


Traditional Computing Hardware

... JUST WHAT IS A COMPUTER ANYWAY?

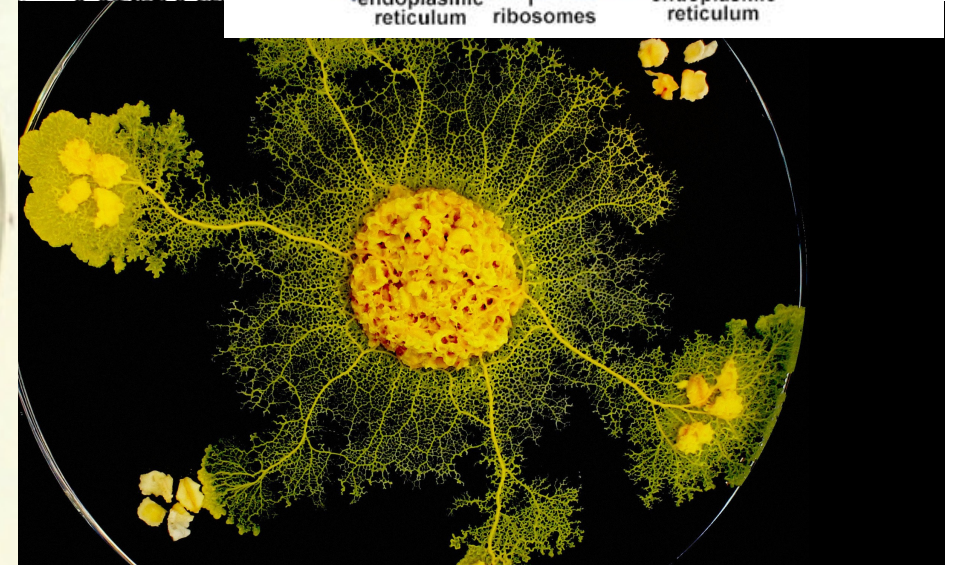
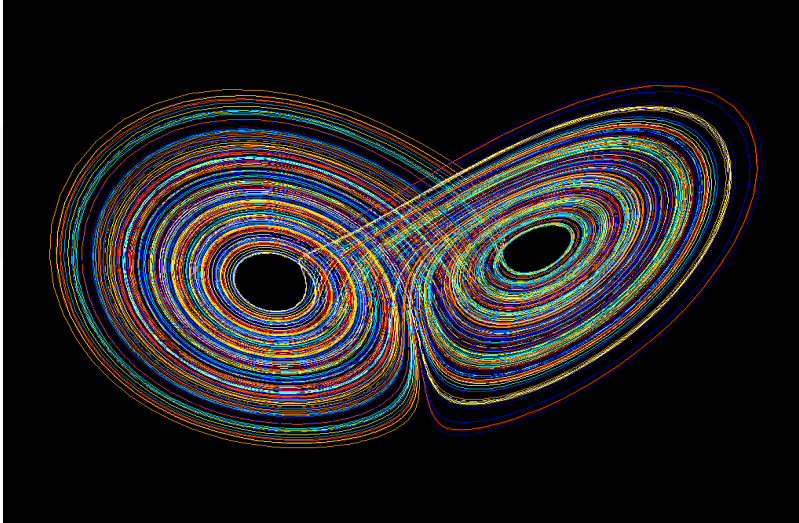
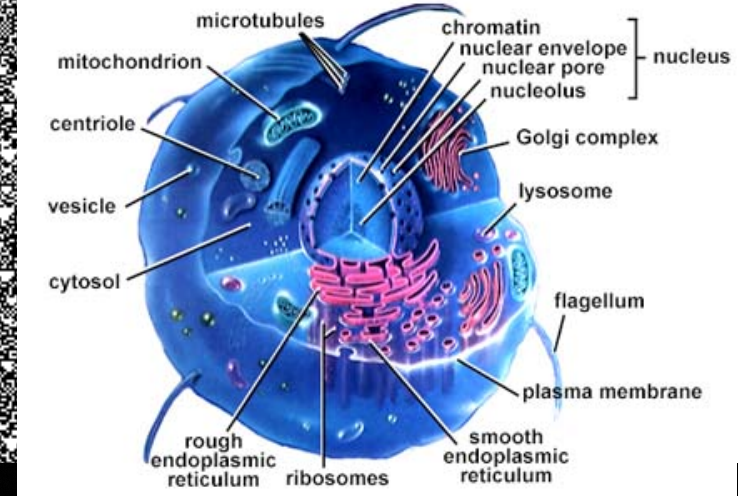
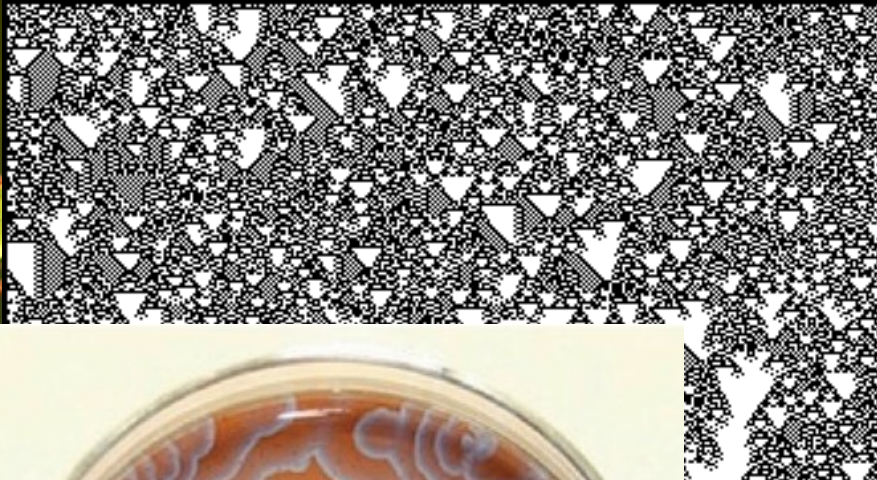


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Unconventional Computing Hardware

BIO- / PHYSICS / CHEMISTRY / NATURE INSPIRED



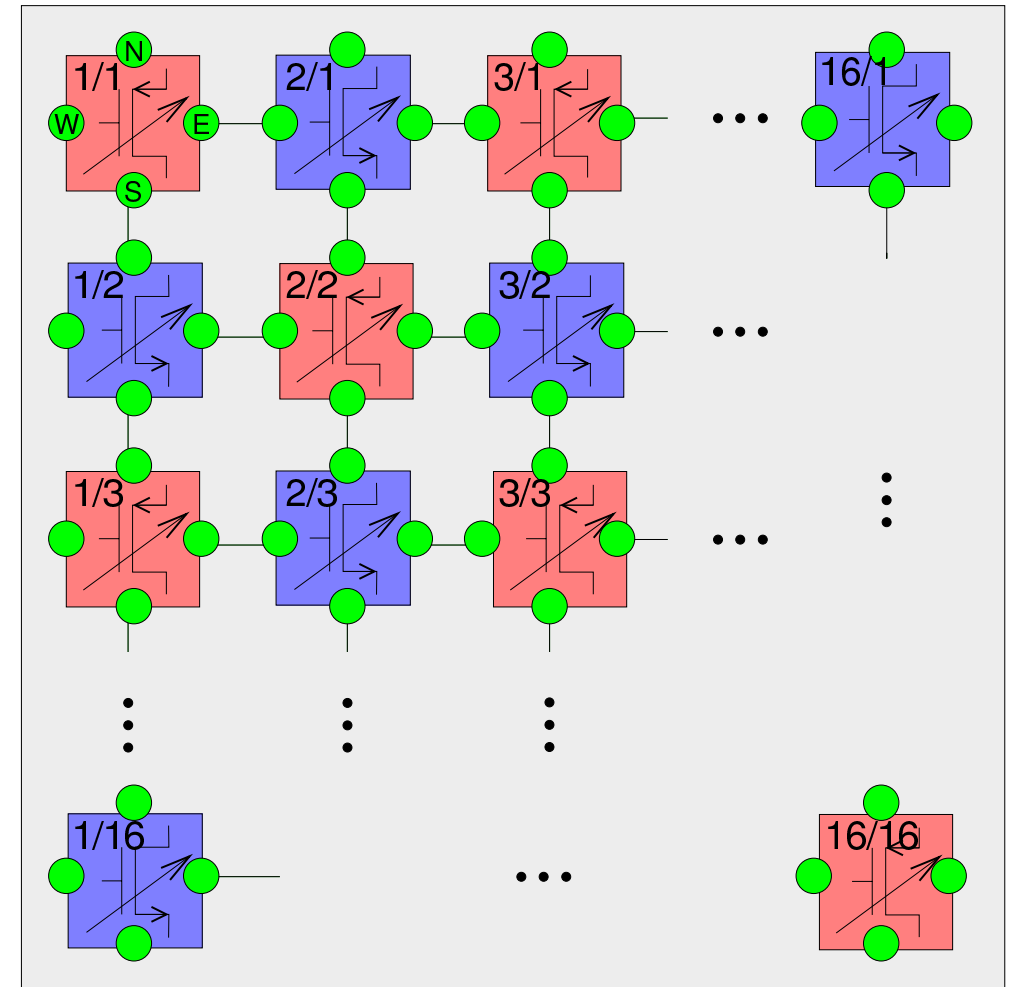
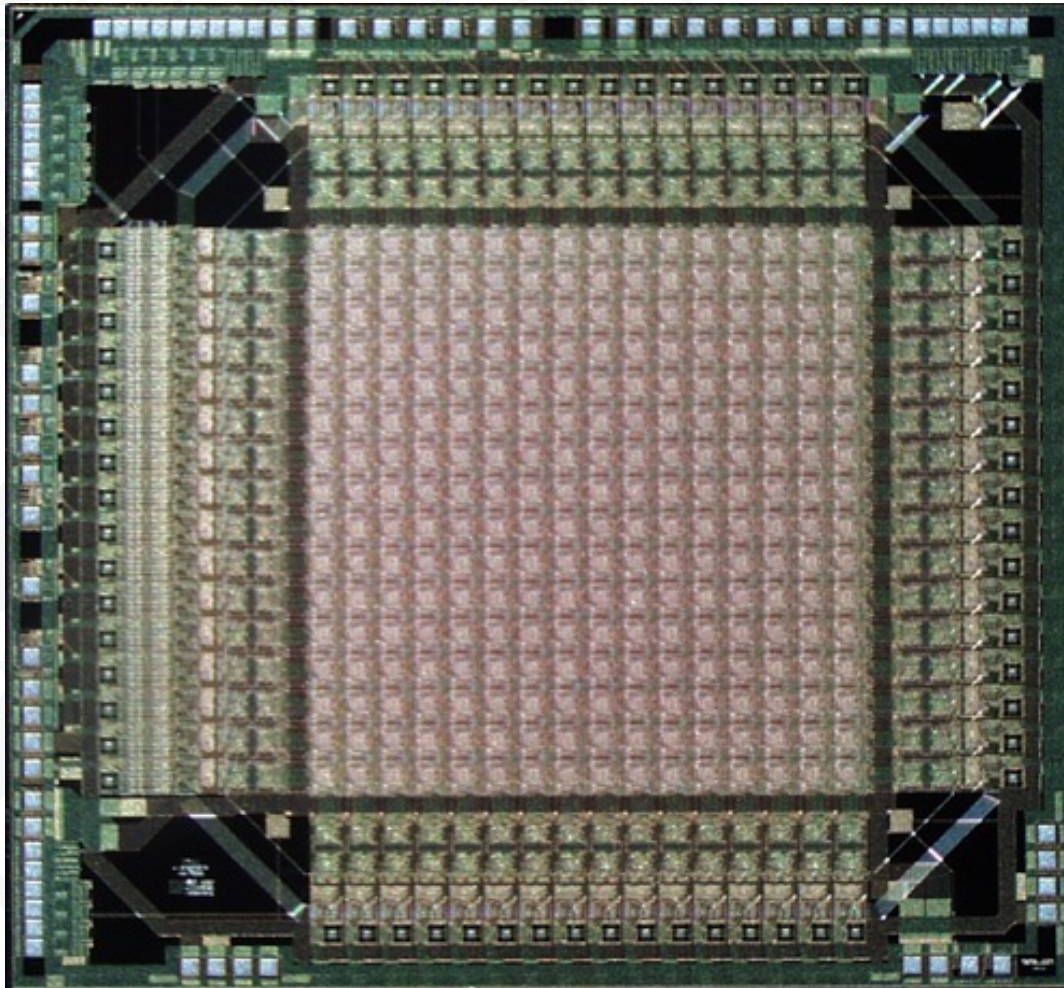
Bio-inspired Hardware

- Multi-**reconfigurable** systems
- **Evolutionary** hardware design
- Design optimisation
- Fault-tolerant systems
- Adaptive **neuromorphic** hardware

Silicon “Primordial Soup”

FIELD-PROGRAMMABLE TRANSISTOR ARRAY – FPTA

AMS
600nm



Computing Hardware

instantiation

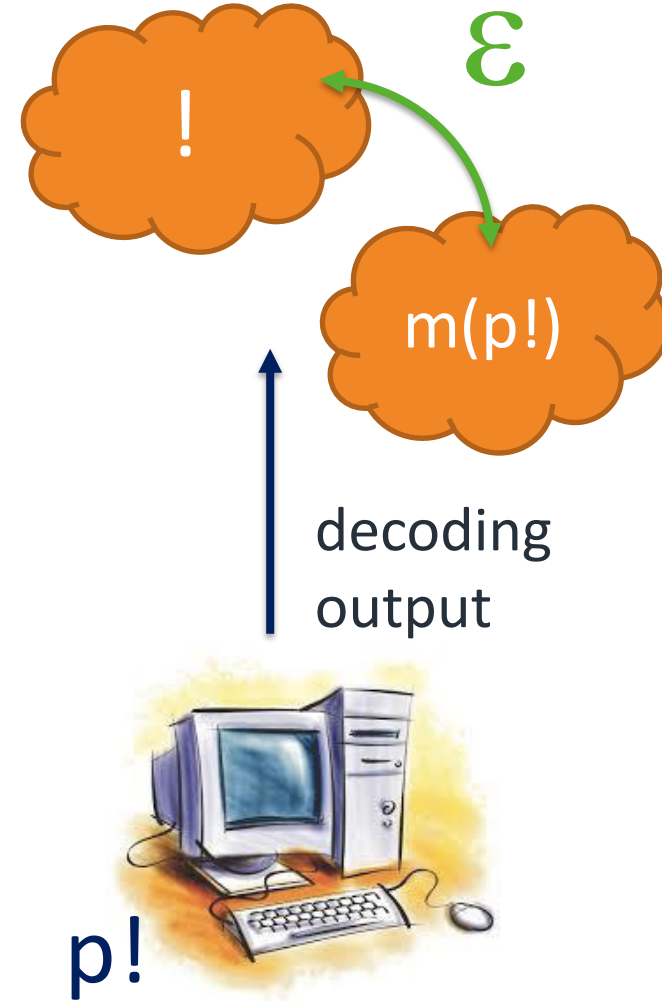


prediction
 $P(?) = ! - \epsilon$

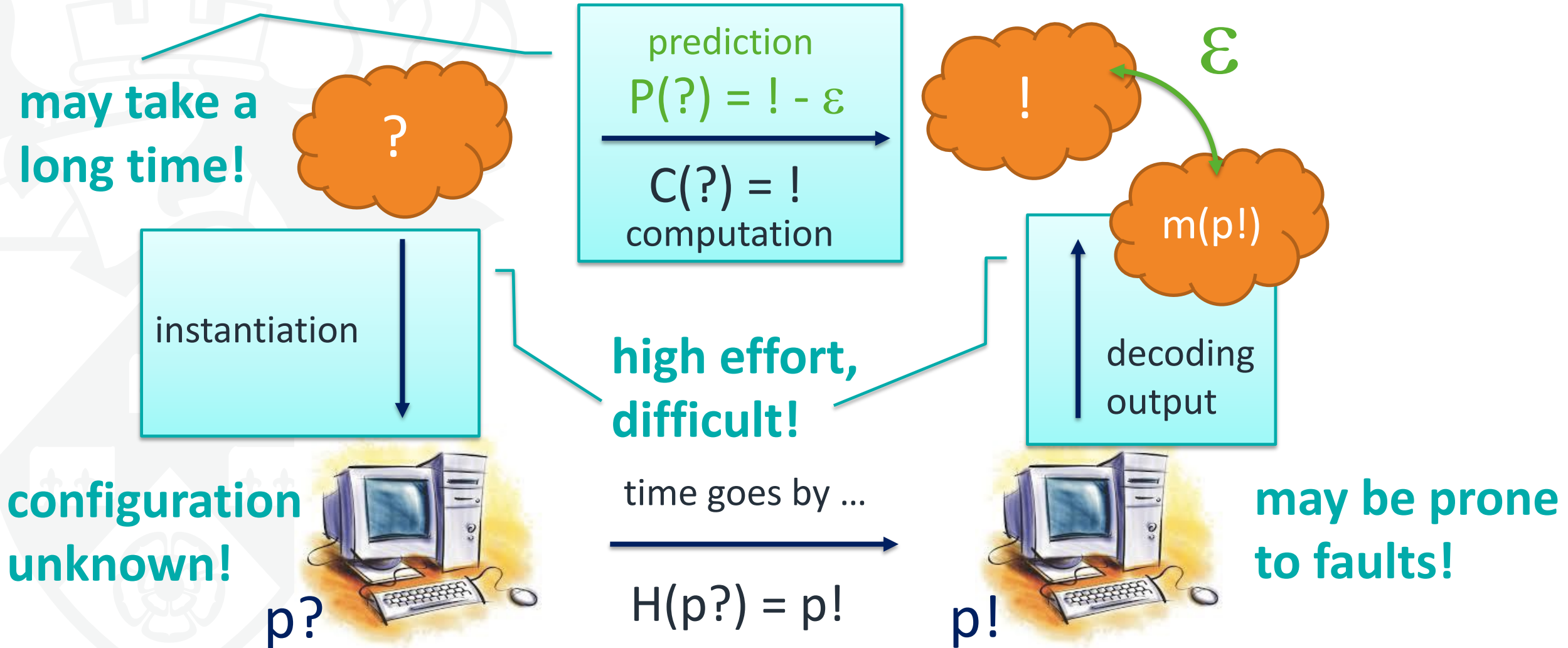
$C(?) = !$
computation

time goes by ...

$H(p?) = p!$

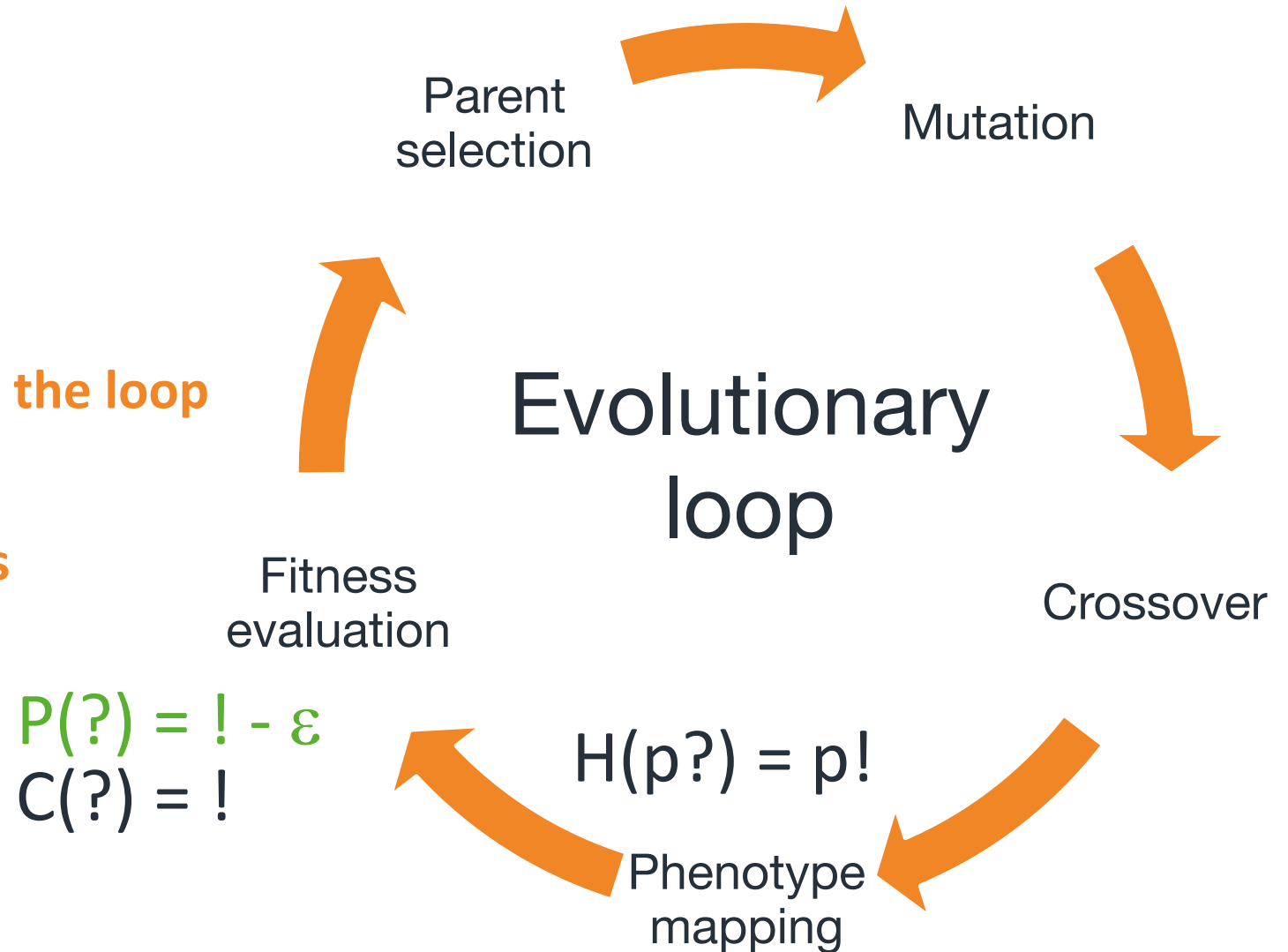


Computing Hardware



Evolutionary *Configurable* Hardware

- May take a long time!
 - automated optimisation
- High effort, difficult!
 - configurable hardware in the loop
- Prone to faults
 - robustness part of fitness
- Configuration unknown!
 - black box

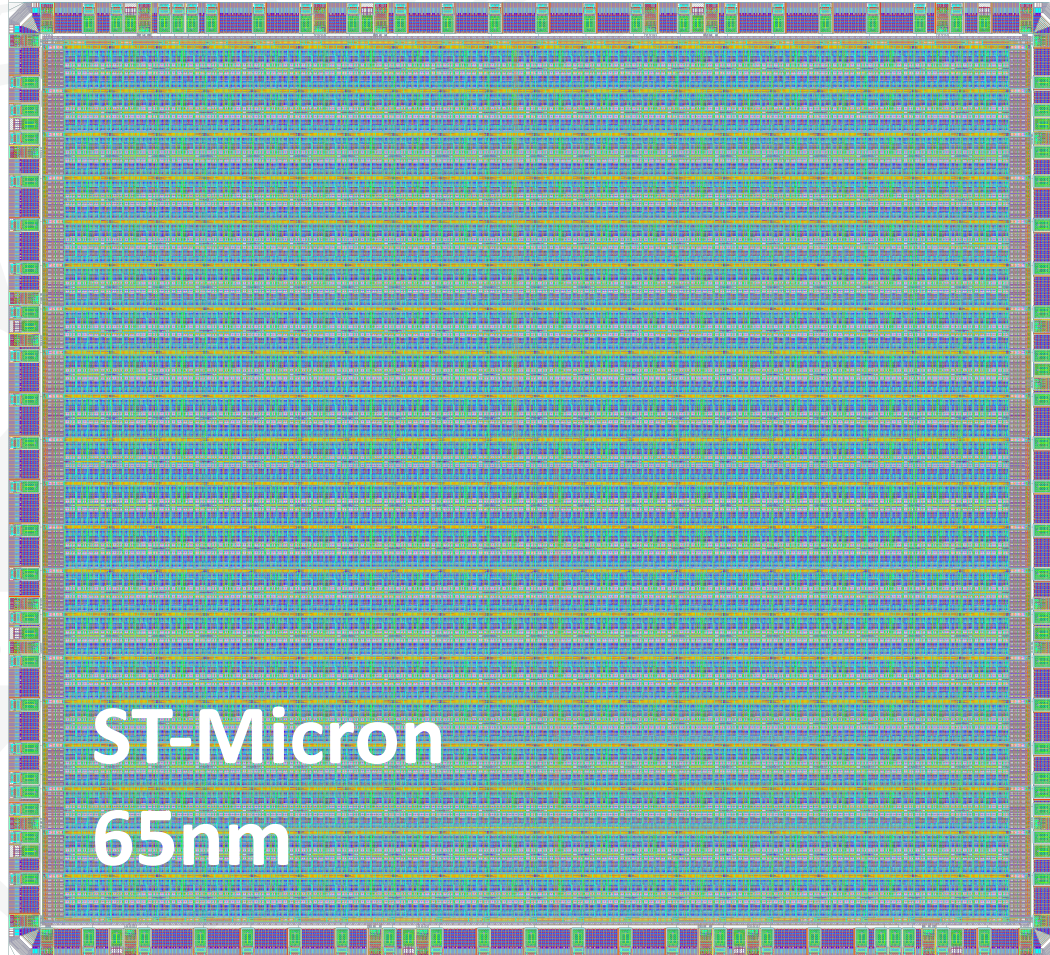


[illegible]

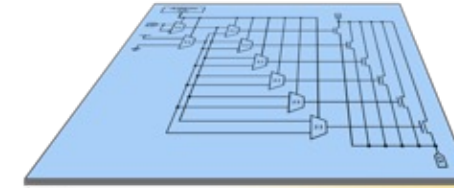
4:50

Multi-reconfigurable Hardware

PROGRAMMABLE ANALOGUE AND DIGITAL ARRAY – PANDA

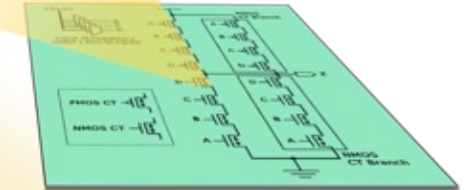


ST-Micron
65nm

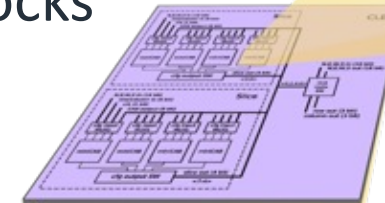


configurable
devices

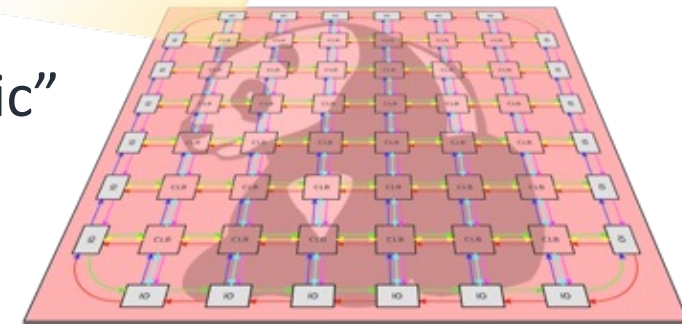
configurable
analogue
blocks



configurable
logic blocks



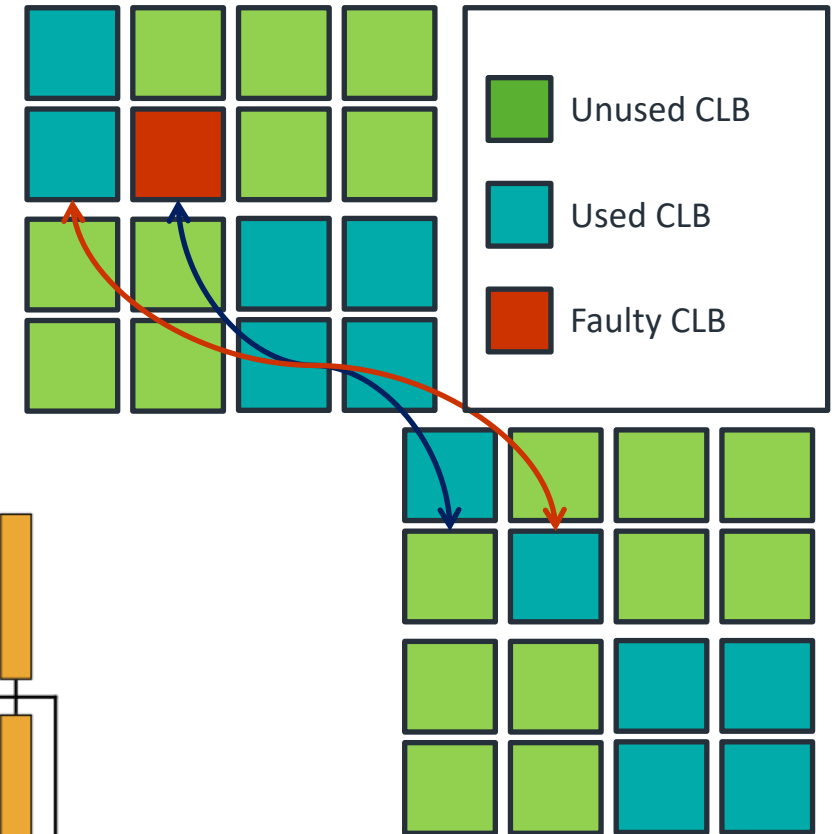
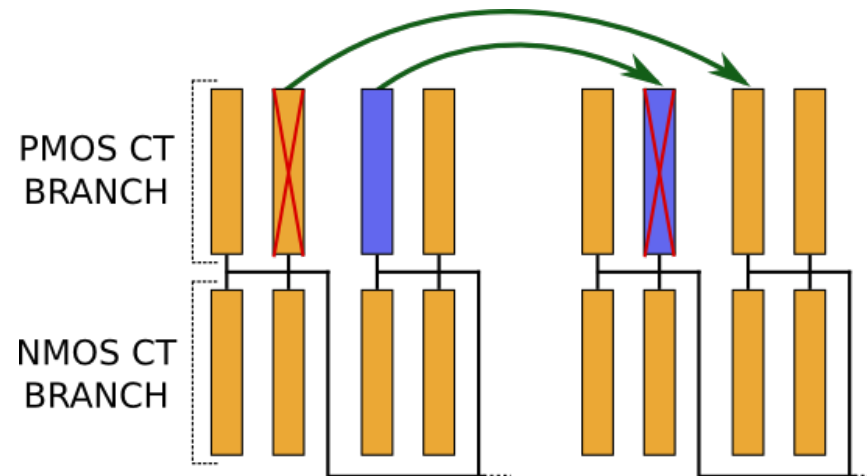
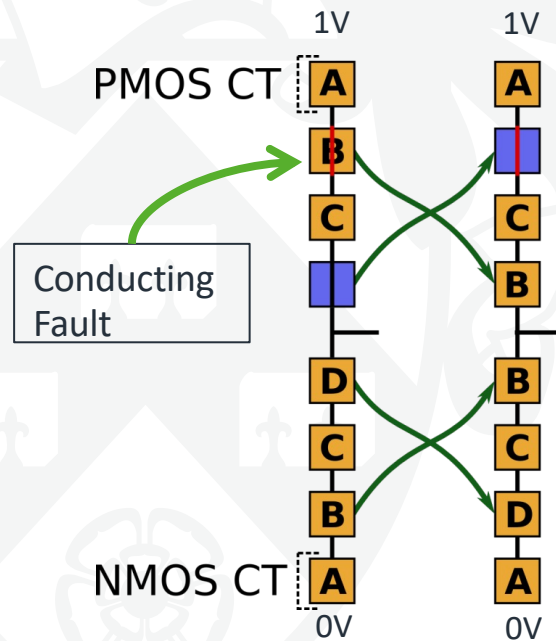
“Heterotic”
Adaptive
FPGA



Fault Tolerance

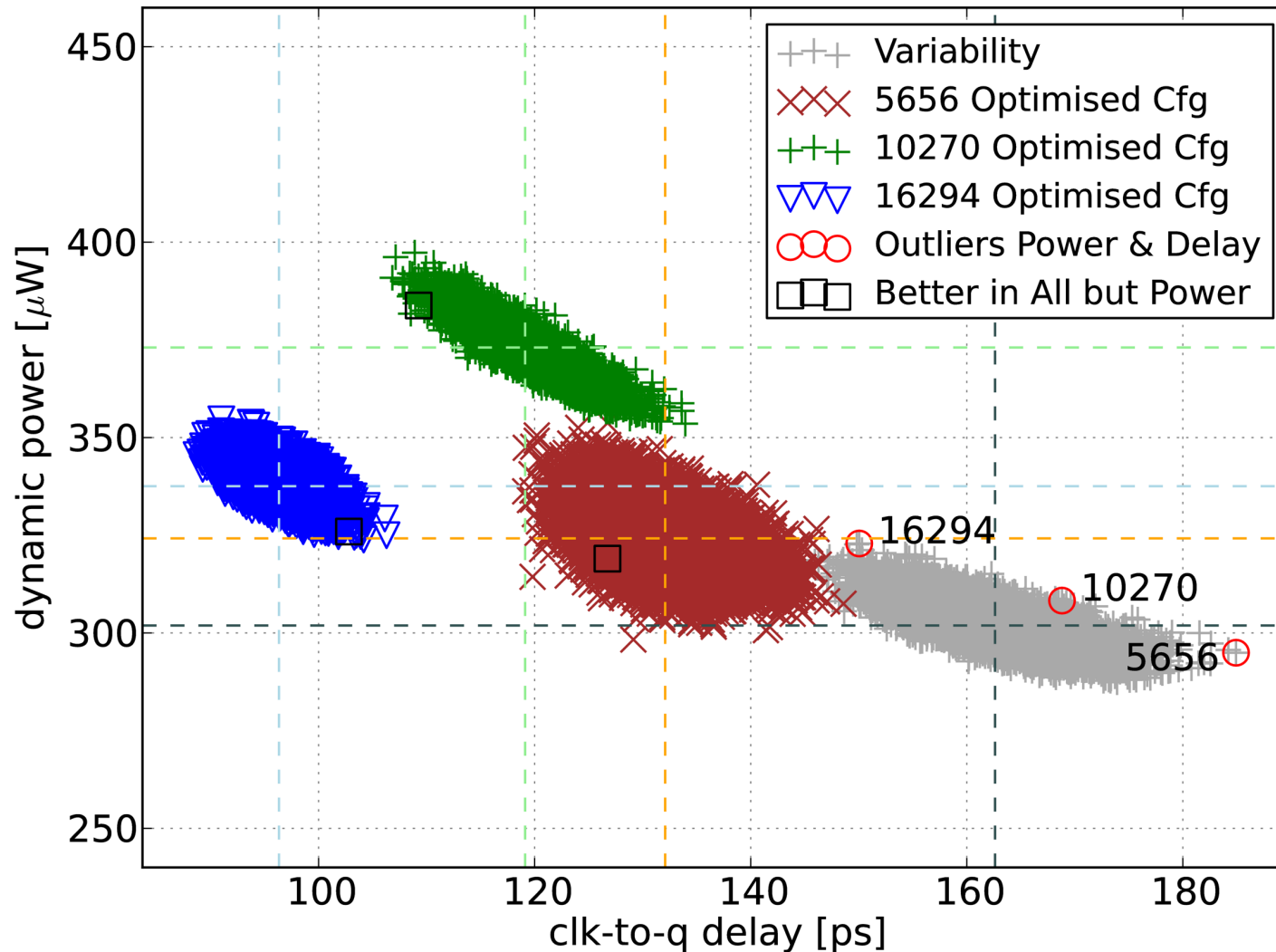
PROGRAMMABLE ANALOGUE AND DIGITAL ARRAY – PANDA

- Evolution of fast hierarchical repair strategies
- Swap CLBs, CABs, Branches, CTs



Variability Mitigation

PROGRAMMABLE ANALOGUE AND DIGITAL ARRAY – PANDA

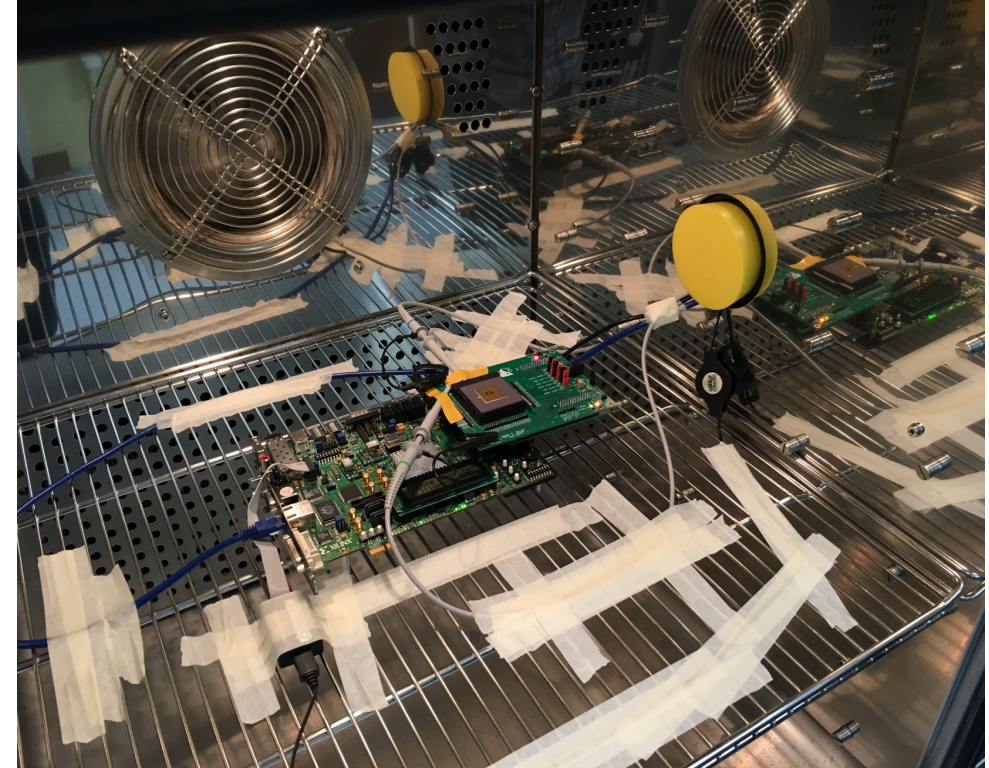
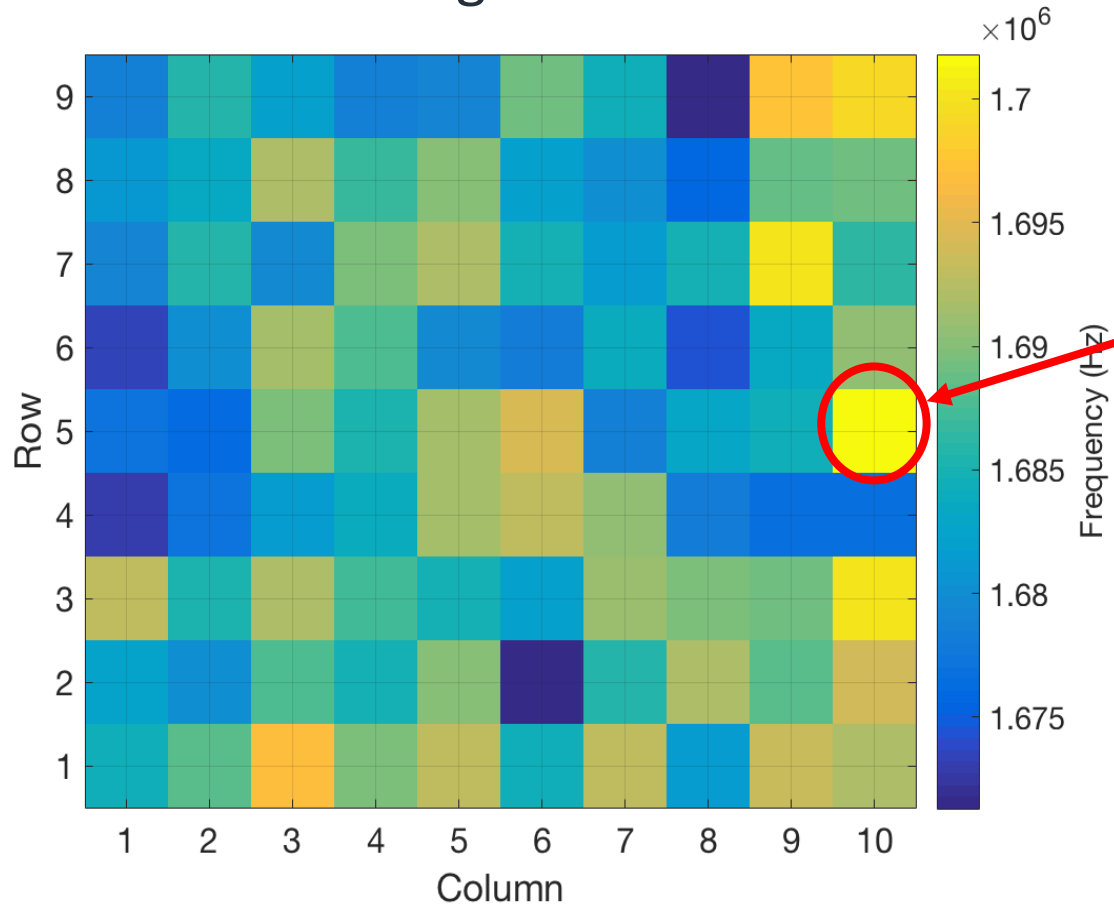


- Standard cell optimization
- Robustness against variability

Variability Mitigation

PROGRAMMABLE ANALOGUE AND DIGITAL ARRAY – PANDA

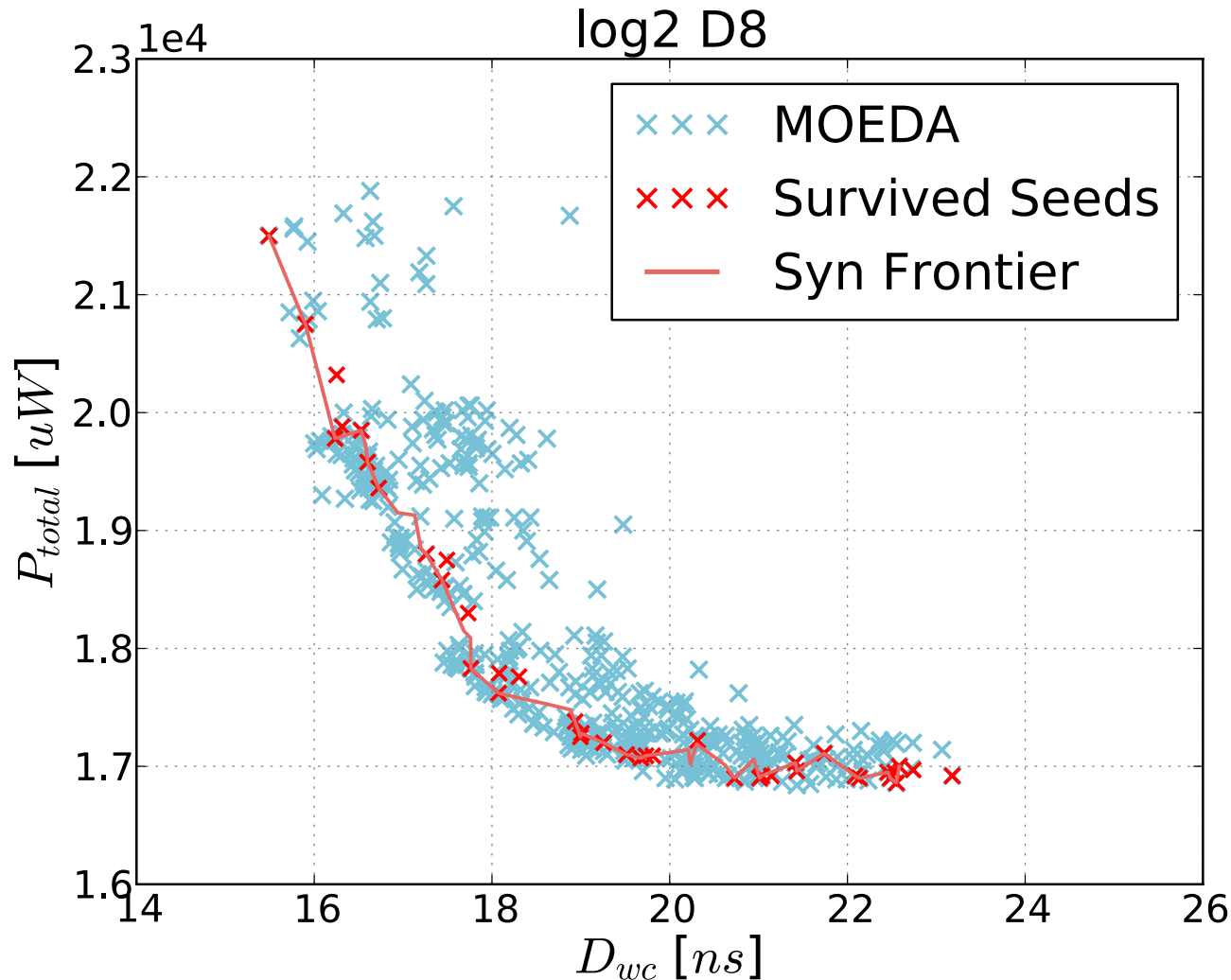
- Ring-oscillator frequency optimisation
- Substrate homogeneity



- Temperature-controlled setup

Cell Mapping in VLSI EDA Flow

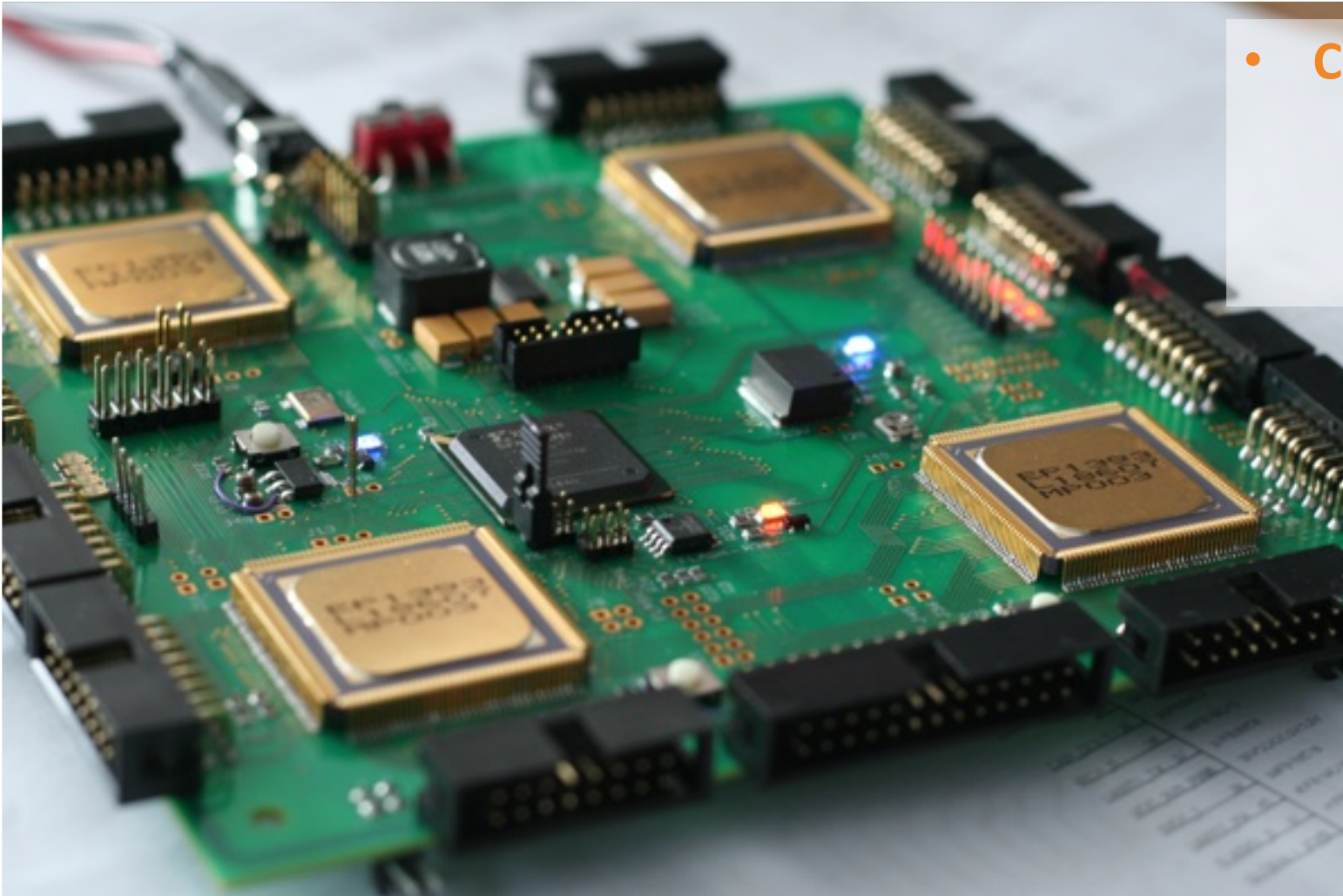
OPTIMISING DRIVE STRENGTH MAPPING IN INDUSTRIAL EDA FLOW



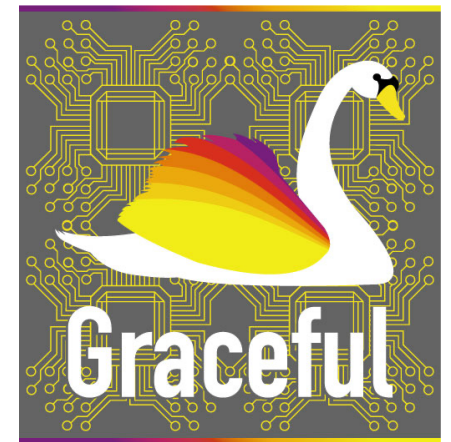
- Log2 Circuit
- 32k complex gates
- Multi-objective optimization for PPA

RTM of Many-core Systems

RUNTIME MANAGEMENT OF DISTRIBUTED SYSTEMS

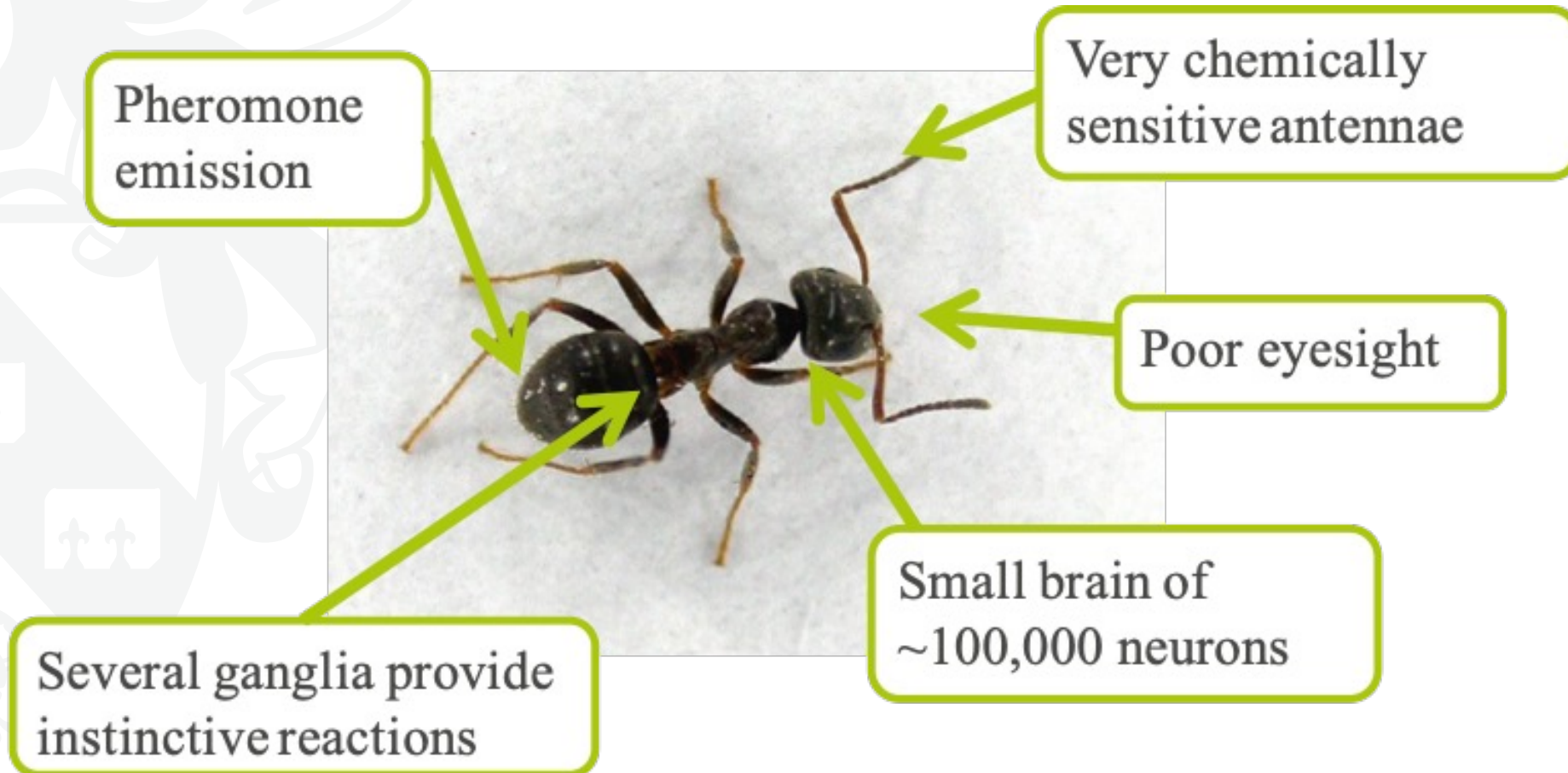


- **Custom-built many-core systems**
 - RISA (180nm TSMC)
 - Centurion (Xilinx Virtex-7)
 - Graceful (Xilinx ZYNQ-7020)



Social-insects Inspired Behaviour

RUNTIME OPTIMISATION, ONLINE LEARNING, FAULT TOLERANCE



Social-insects Inspired Behaviour

RUNTIME OPTIMISATION, ONLINE LEARNING, FAULT TOLERANCE



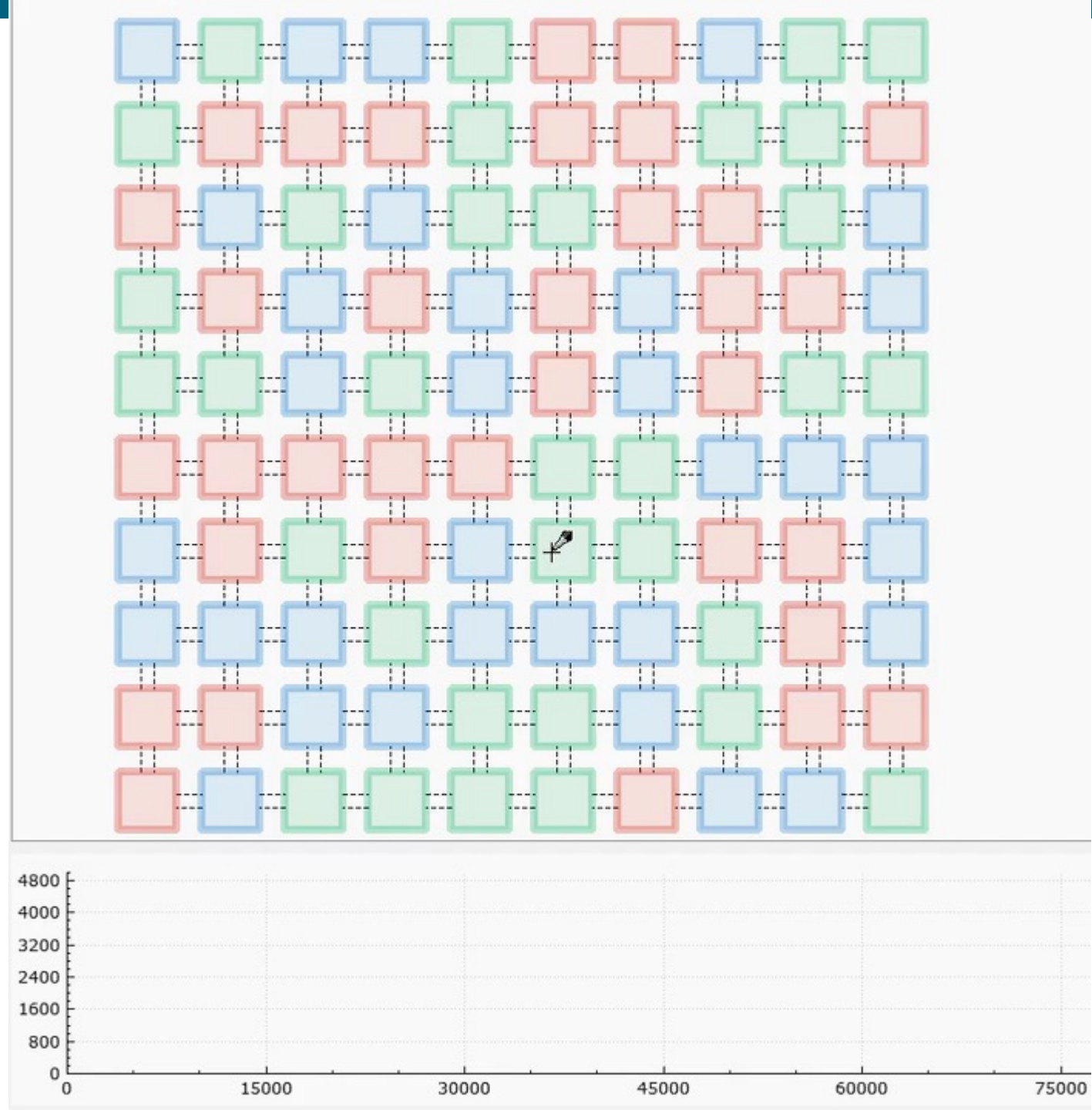
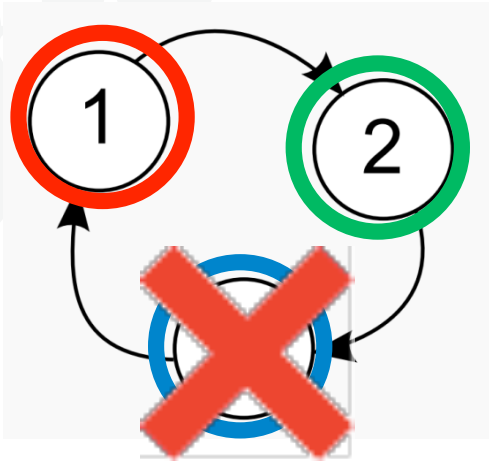
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Social insects- inspired Behaviour

ANT-INSPIRED RUNTIME MANAGEMENT
AND FAULT TOLERANCE
IN MANY-CORE SYSTEMS

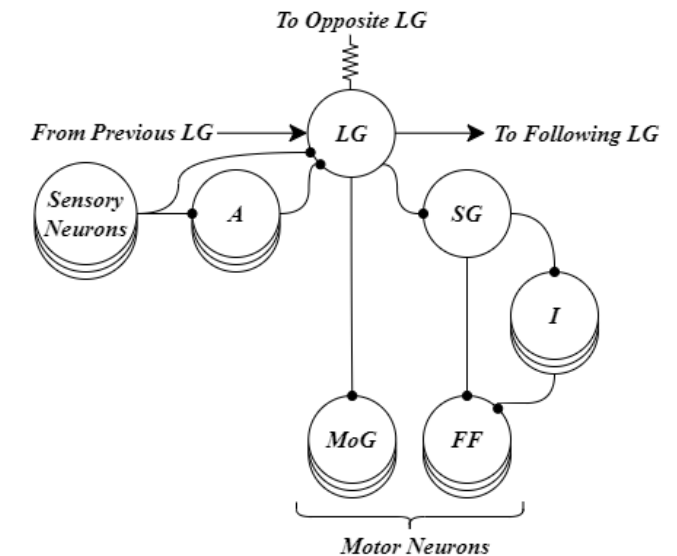
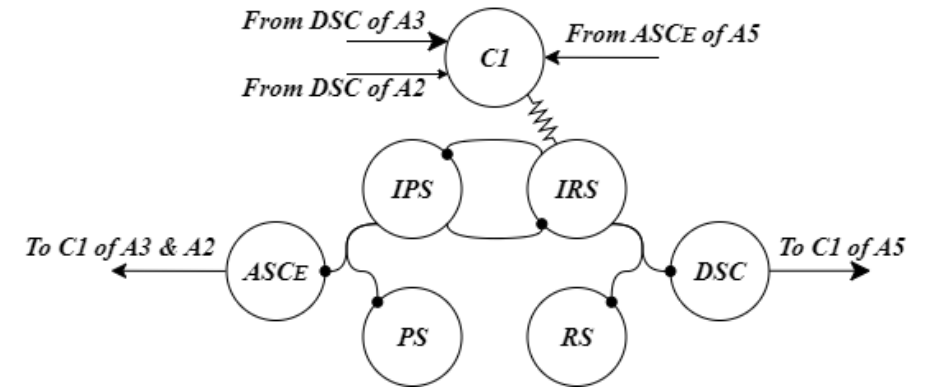
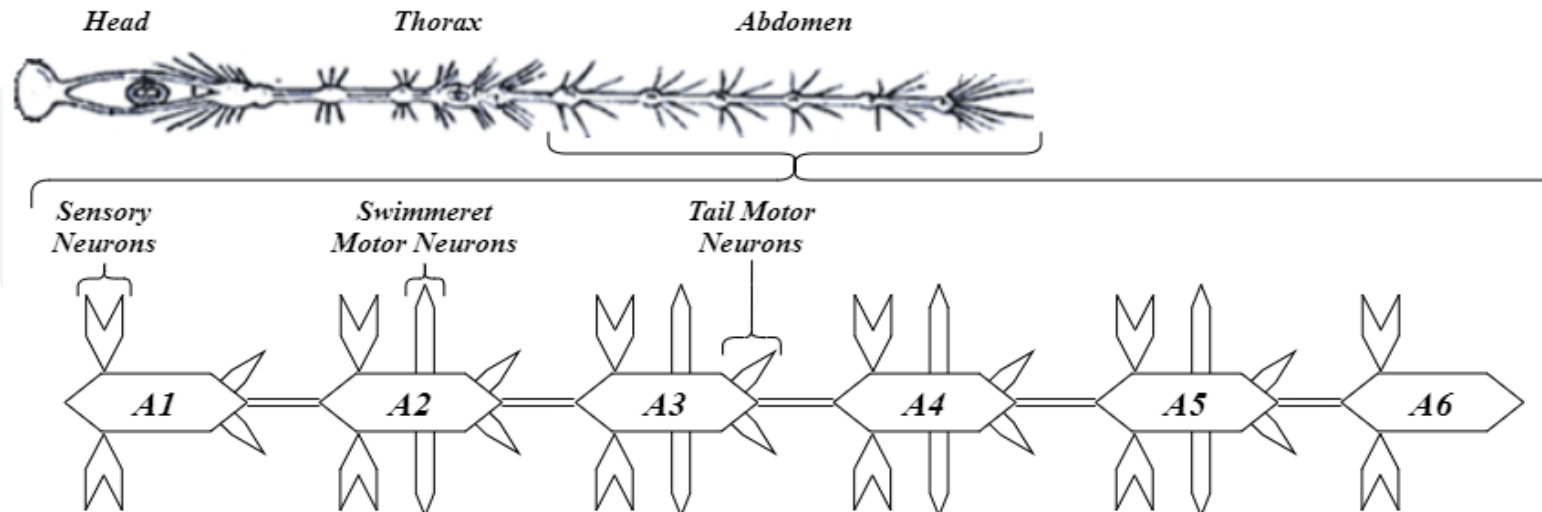
- Self-organization
- Distributed decision making
- Autonomous fault tolerance



Artificial Neural Microcircuits

NEURAL MICROCIRCUITS AS EMBEDDED “NERVOUS SYSTEM”

Crayfish tail reflex

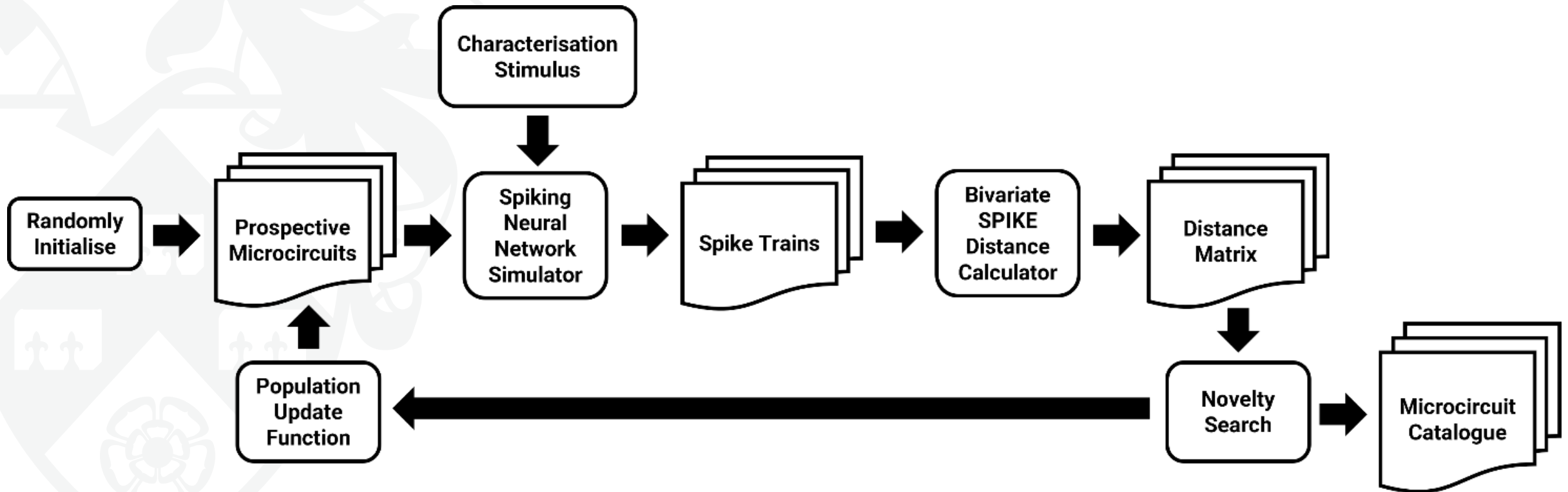


Making Neural Microcircuits

EVOLUTIONARY NOVELTY SEARCH AND TASK SEARCH



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Embedding Neural Microcircuits

NEORV32 RISC-IV CPU

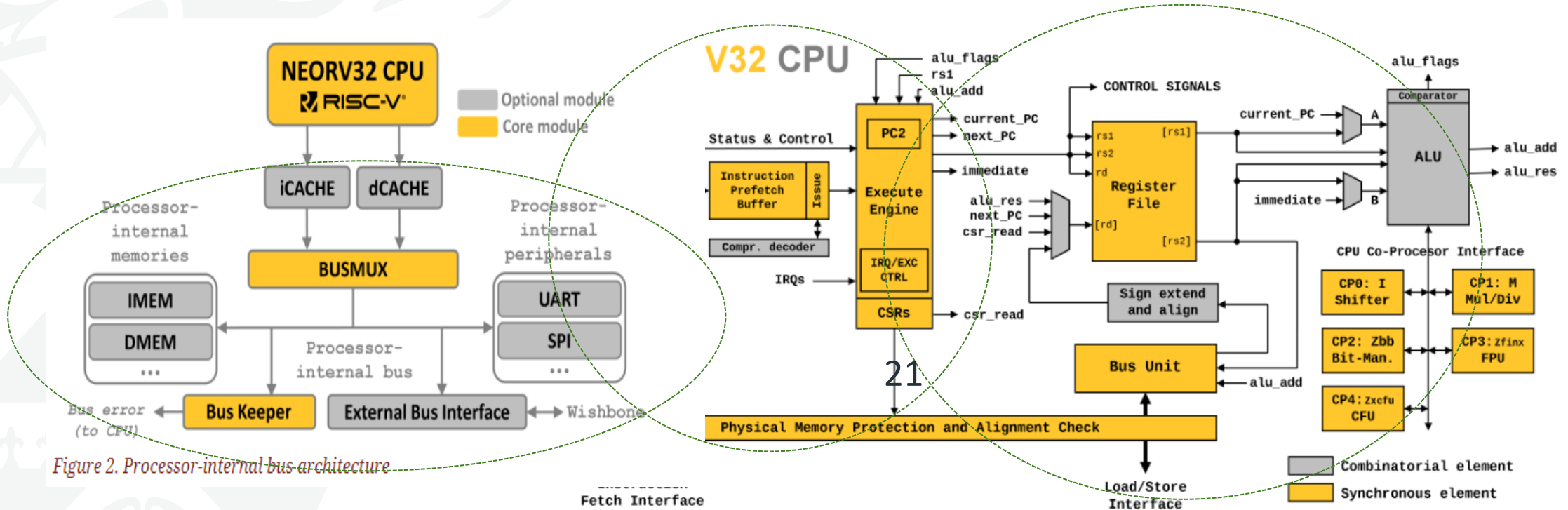


Figure 2. Processor-internal bus architecture

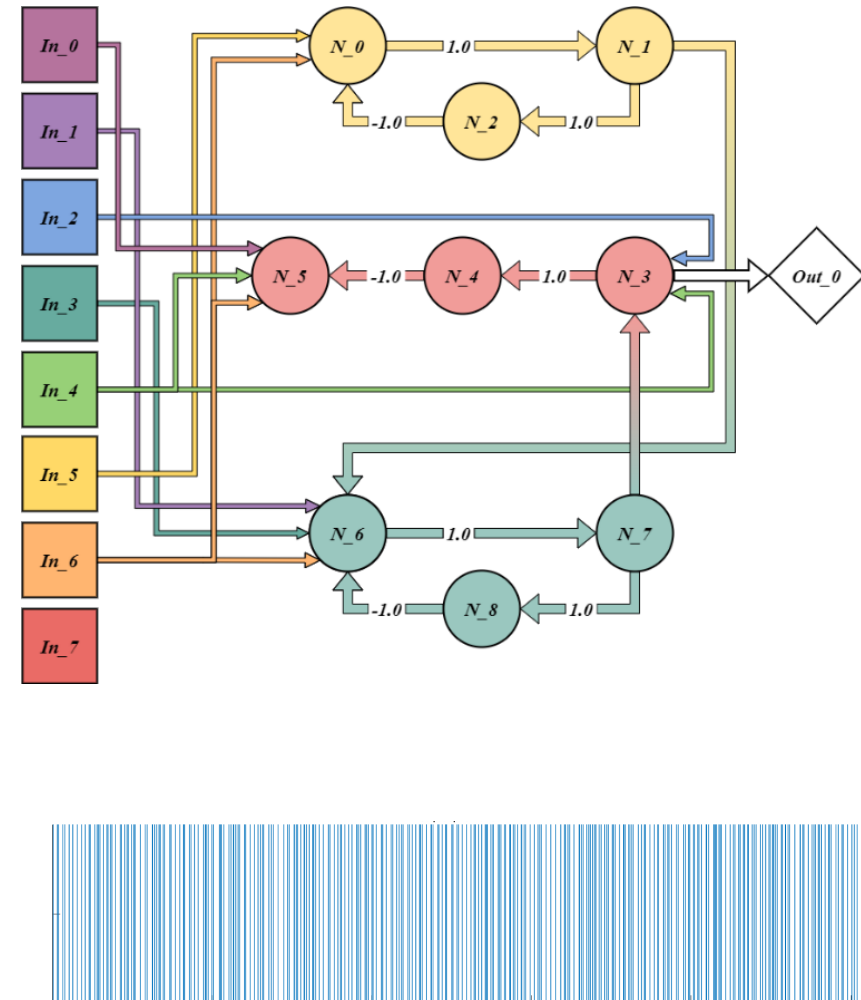
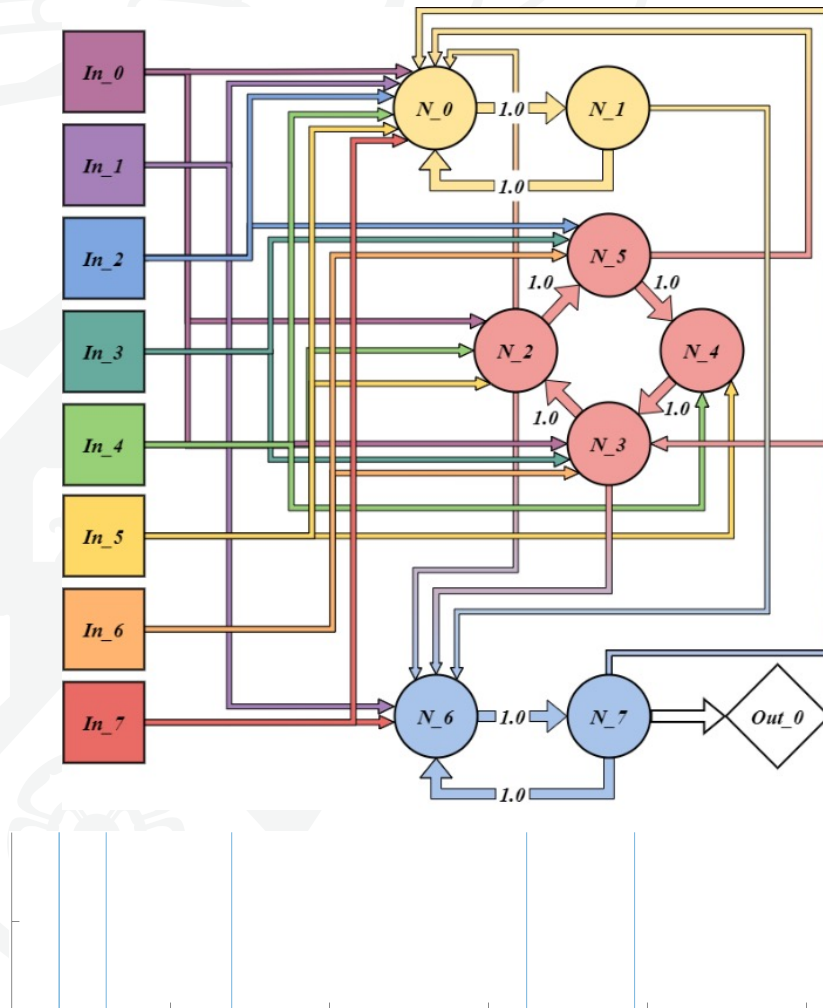
Location 1

Location 2

Location 3

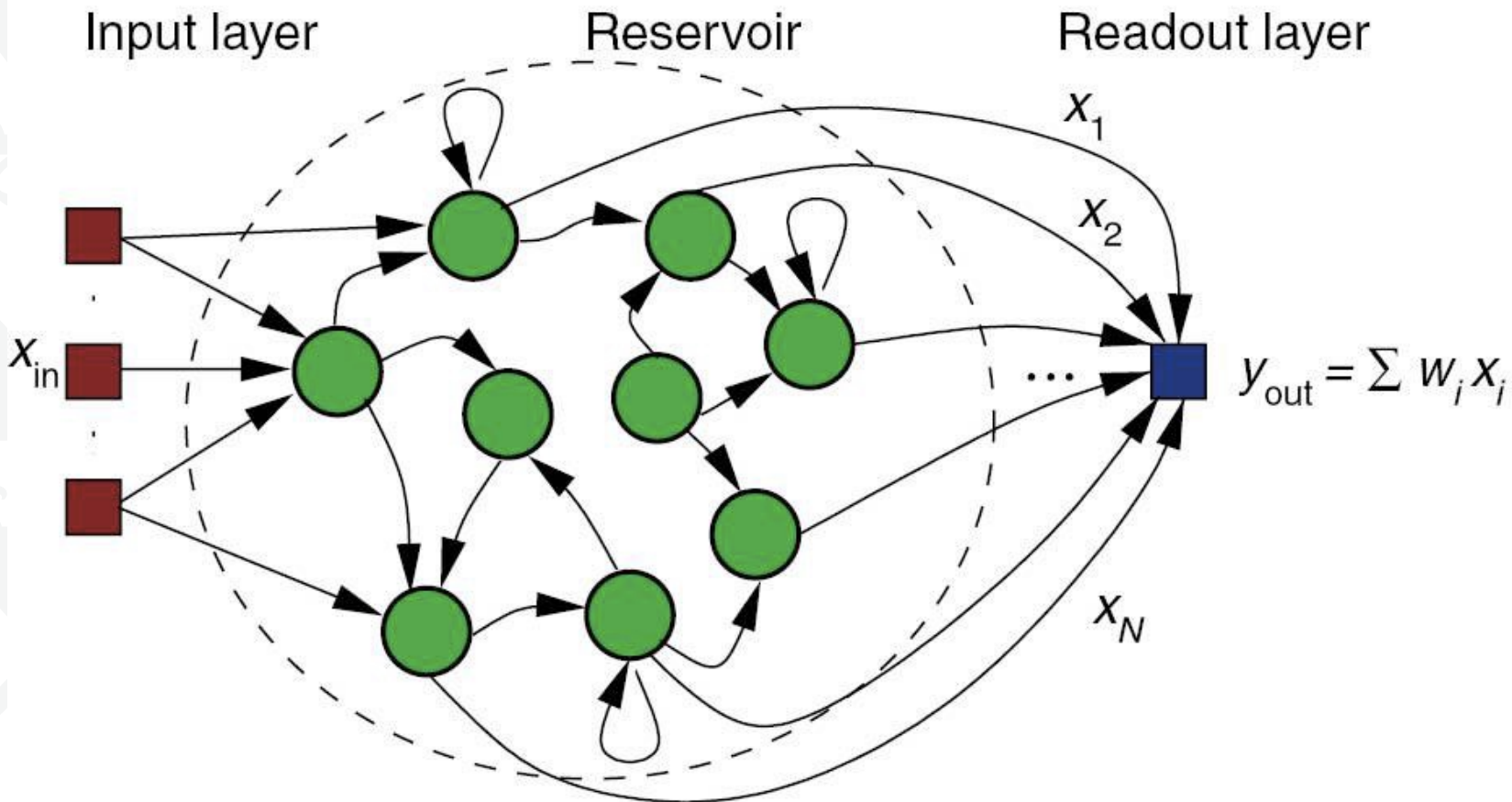
Neural Microcircuit Responses

RESPONDING TO “IRRADIATED” MEMORY / PROGRAMS



System-level Learning with SNNs

SPIKING NEURAL NETWORKS WITH RESERVOIR COMPUTING

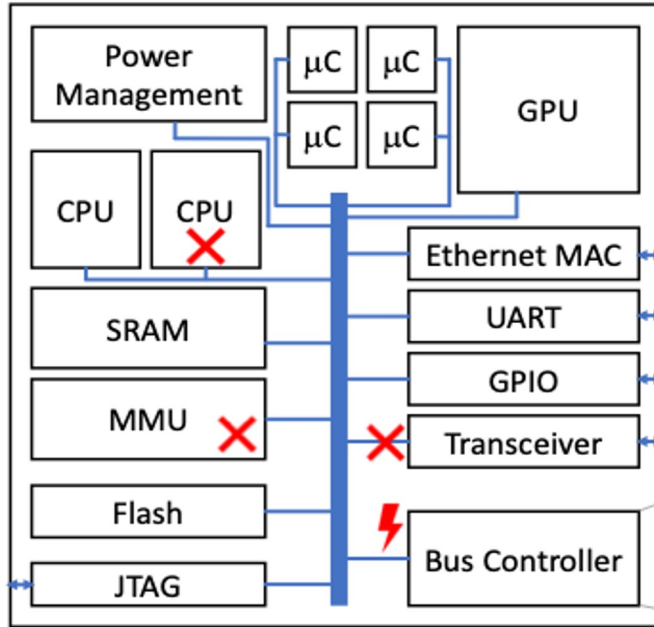


Nervous Systems On Chip

NEUROMORPHIC FAULT TOLERANT HW – LEARNING WHAT IS AN ANOMALY

System on Chip

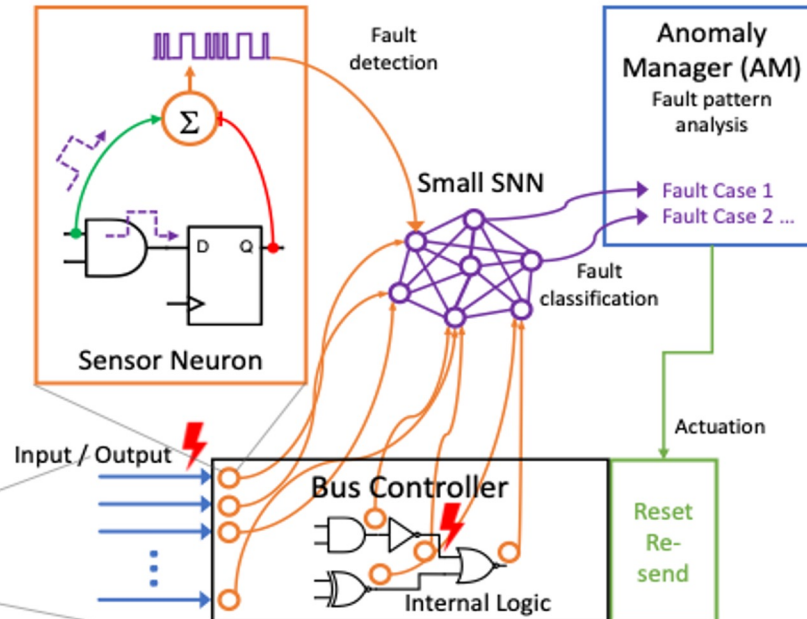
⚡ - Fault ✗ - Resulting Errors



WP1

Spiking Neurons / Small-world SNNs

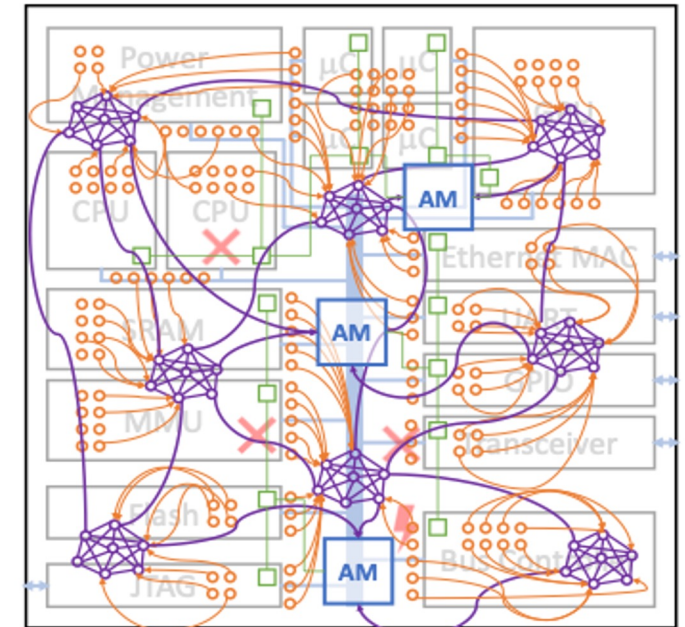
○ - Sensor Neuron ○ - Neuron □ - Actuator □ - Anomaly Manager



WP2

Nervous System on Chip

○+○+□+□ = Overlay Architecture



WP3 / WP4



Invertebrate cardiac control pathways



Crayfish startle pathways



Leech muscle control pathways



C. elegans



Leech



Lobster



Fruit fly



Ant



Honeybee



Zebrafish

Behavioural complexity of nervous systems



END