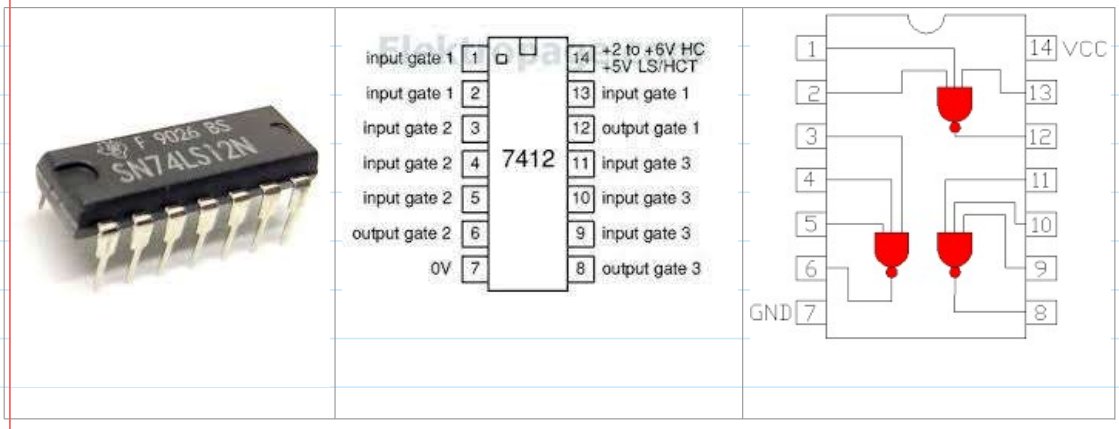
# Unit 5 Theory Part

26 August 2022 12:54

## Question Bank

1. What are the various steps to design digital system using CAD Tool/Define Digital Design flow.
2. Q what is differences between Simulation and Synthesis?
3. What is HDL?
4. What are the advantage of CAD Tool.
5. What are the various PLD in VLSI
6. What are the various style of design entry in the CAD Tool.

Digital technique, circuit and system is very important nowadays. The word digital is entered in every part of our life. So there is demand of more and more powerful digital system.
In the earlier chapter we have seen small and less complex digital system made by few GATE and Flipflop using MSI and LSI Chip.




We have discussed manual method of design digital system.

1. Simplification of Boolean expressions using Boolean algebraic theorems,
2. graphical method(K map),
3. Tabular method(QMC method)

These design (synthesis) methods is suitable for understanding the concepts of digital circuits, but these designs are relatively small in size and are not complex in today's context.

But in the todays context size and complexity of digital system is high, so not possible to design digital system using manual method.

So we have to adopt design methods which involve the use of computers, These methods are known as computer aided design (CAD) methods.

Development of various CAD tools have made it very convenient and easy to go through design process. CAD tools enable the designers to simulate the behavior of a design without its hardware implementation.
CAD tool are used to simulate the design and are also used to determine whether the obtained design meets the required specifications or not. If not, then appropriate modifications

The initial design idea has to go through several design stages before its hardware implementation is obtained.
At each stage of design process the designer evaluates and verifies the results of that design stage.
For the evaluation of the results of a design stage, the design is to be tested by applying test data (stimuli) at the input and finding the output and checking this output and verifying it against the original system specifications.
If there is any error then the design must be modified to eliminate the error. The modified design is again put to evaluation and verification. This process is repeated until there is no error in the designed system.

Now with the tremendous progress in semiconductor technology, we cannot think of designing powerful and efficient complex digital systems without use of CAD tools.

What are the advantage of CAD

1. Design complex logic circuits easier.
2. Many tasks in the design process are performed automatically by the CAD tools resulting in faster and efficient design.


What is HDL?

7. Hardware Description Language (HDL).
8. it have been developed for describing the structure and behavior of complex digital circuits.

What are two HDL for the design of Very High Speed Integrated Circuits (VHSIC)

1. VHDL (VHSIC Hardware Description Language)-first version of VHDL was IEEE standard 1076–1987, and

presently using IEEE 1076–2008.

2. Verilog was adopted in 1995 as IEEE standard 1364 (Verilog–95) and presently using IEEE standard 1364–2005.

==========

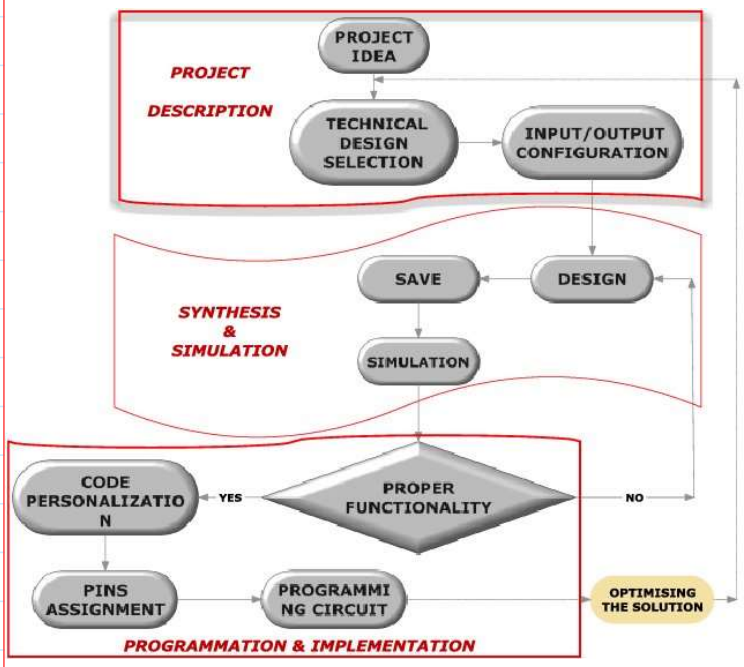
What is PLD in VLSI?|An IC that contains large numbers of gates, flip-flops, etc. that can be configured by the user to perform different functions is called a Programmable Logic Device (PLD).

types

1. Programmable Read Only Memory.
2. Programmable Array Logic.
3. Programmable Logic Array.
4. A Complex Programmable Logic Device (CPLD and FPGA)

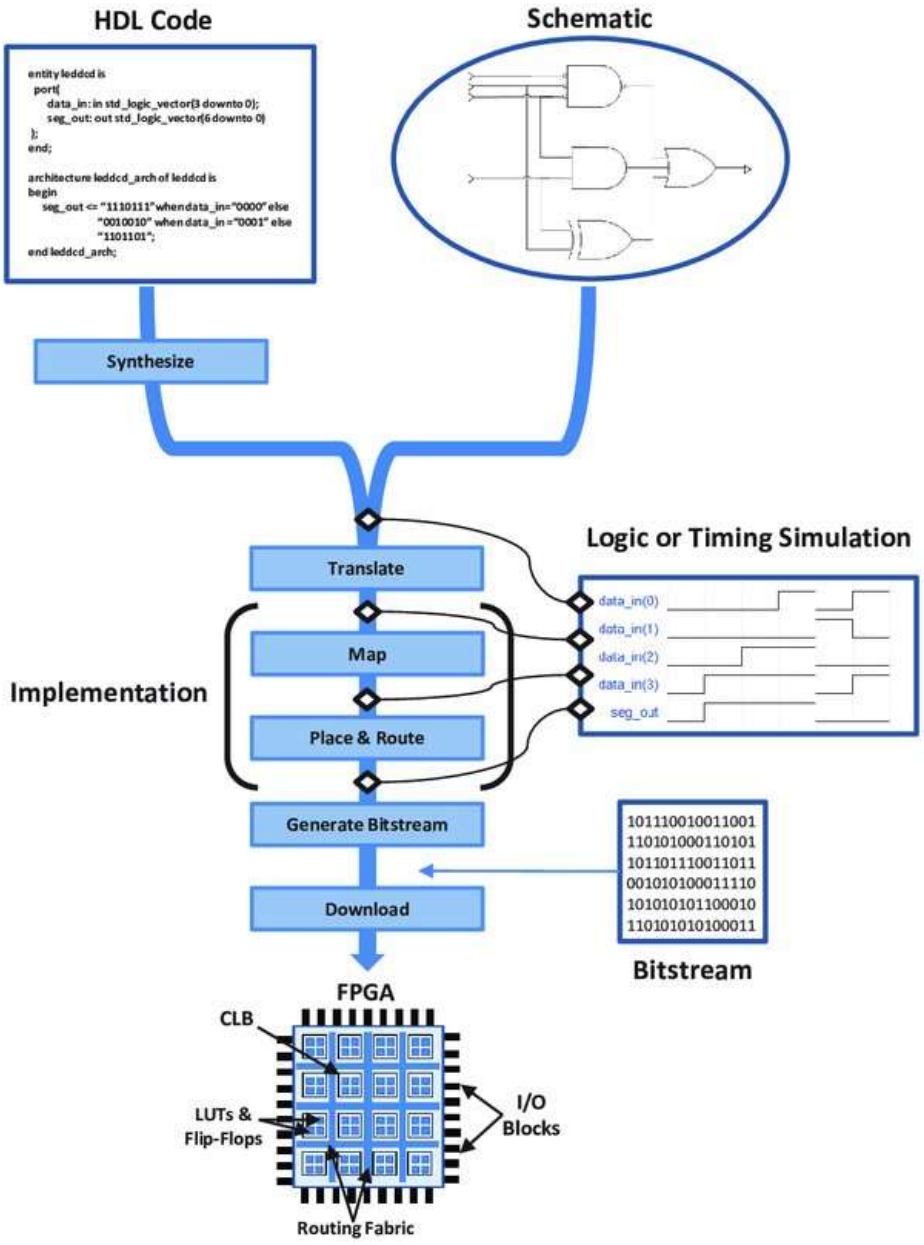


When design system must keep in mind which hard ware we will use to implement it.




The flowchart design of digital systems using programmable circuits.

From <https://www.researchgate.net/publication/236907914_Researching_strategies_for_optimizing_educational_technologies_by_offering_alternative_designs/figures?lo=1>

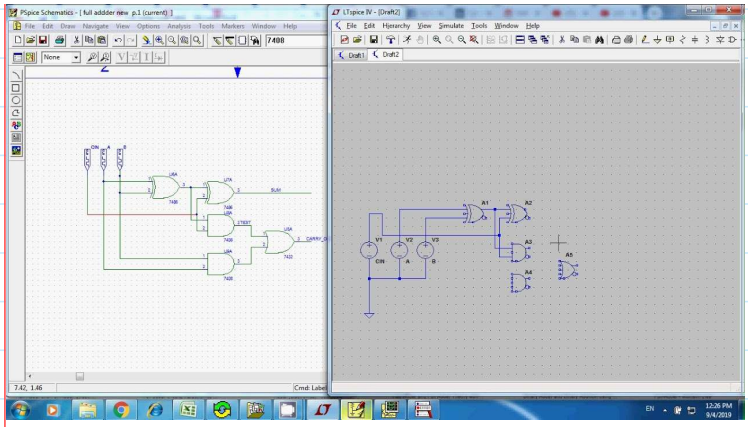



What are the various style of design entry in the CAD Tool.

1. Truth table
2. Schematic diagram
3. Hardware description language (HDL

Design Entry Using Truth Table- The truth table of a logic function or a timing waveforms diagram may be given to CAD tool to design digital system.
This method of design entry can be used when small number of variables in the design, this method is not suitable when number of variable are more.

3. Design Entry Using Schematic Capture The term schematic refers to a circuit diagram in which the circuit elements are represented by their graphical symbols and the connections between the circuit elements are drawn as lines.



The schematic tool provides a library of graphical symbols that represent gates of various types with different number of inputs.
Some of the commonly required circuits using these gates can be created by a designer and these can also be represented by graphical symbols.
This is a hierarchical design method and is, therefore, a convenient way of dealing with the complexities of larger circuits.

Design Entry Using Hardware Description Languages-
The two most commonly used hardware description languages (HDLs) in industry are: VHDL (Very High-Speed Integrated Circuits Hardware Description Language) and Verilog HDL.
Using a HDL, a logic circuit is represented in its code which is used for design entry. This method of design entry is the most commonly used method for the design of digital systems.
This method can be used for efficiently designing small as well as large systems.

The three design entry methods can be mixed in a system design for different subcircuits, for example, a schematic capture tool can be used in which a subcircuit in the schematic is described using VHDL.

==========

Define the term simulation and Synthesis?

Design are simulate to determine whether the obtained design meets the required specifications or not. If not, then appropriate modifications are made in the design and the verification of the modified design is repeated through simulation till the correct design is obtained.

Once the functionally correct design is obtained, logic synthesis and optimization CAD tools are used to obtain optimized logic expression to suit the target hardware technology to be used for implementing the design. Using these optimal logic expressions, physical design tool is used for obtaining gate level or transistor level design.

Synthesis is the process of transforming design entry information of the circuit into a set of logic equations.
Simulation- two types

- Functional Simulation- it is necessary to verify the circuit function of the designed circuit with the

expected function. For this purpose, a functional simulator CAD tool is used.(Prior to synthesis)

The output of the simulator, which is obtained either in the truth table form or as the timing diagram are examined to verify whether the designed circuit operates as required or not. If the output from the simulation process is not the desired output then the design is to be modified suitably. This process is repeated unless the functionally correct design is obtained.

- Timing Simulation-The functional simulation process assumes propagation delay is zero of the logic gates, which is not true for practical circuits. There is always some time needed for signals to propagate through logic gates, therefore, it is necessary to take care of propagation delays While designing digital circuits. For this purpose timing simulation is used, which simulates the actual propagation delays in the technology chosen for implementation of the design. The model to be used for timing simulation must take care of delays associated with the chip, microcells if the target device is a CPLD and logic cells for an FPGA target device, and the delays through the inter connection. Timing Simulator CAD tools are used for this.