


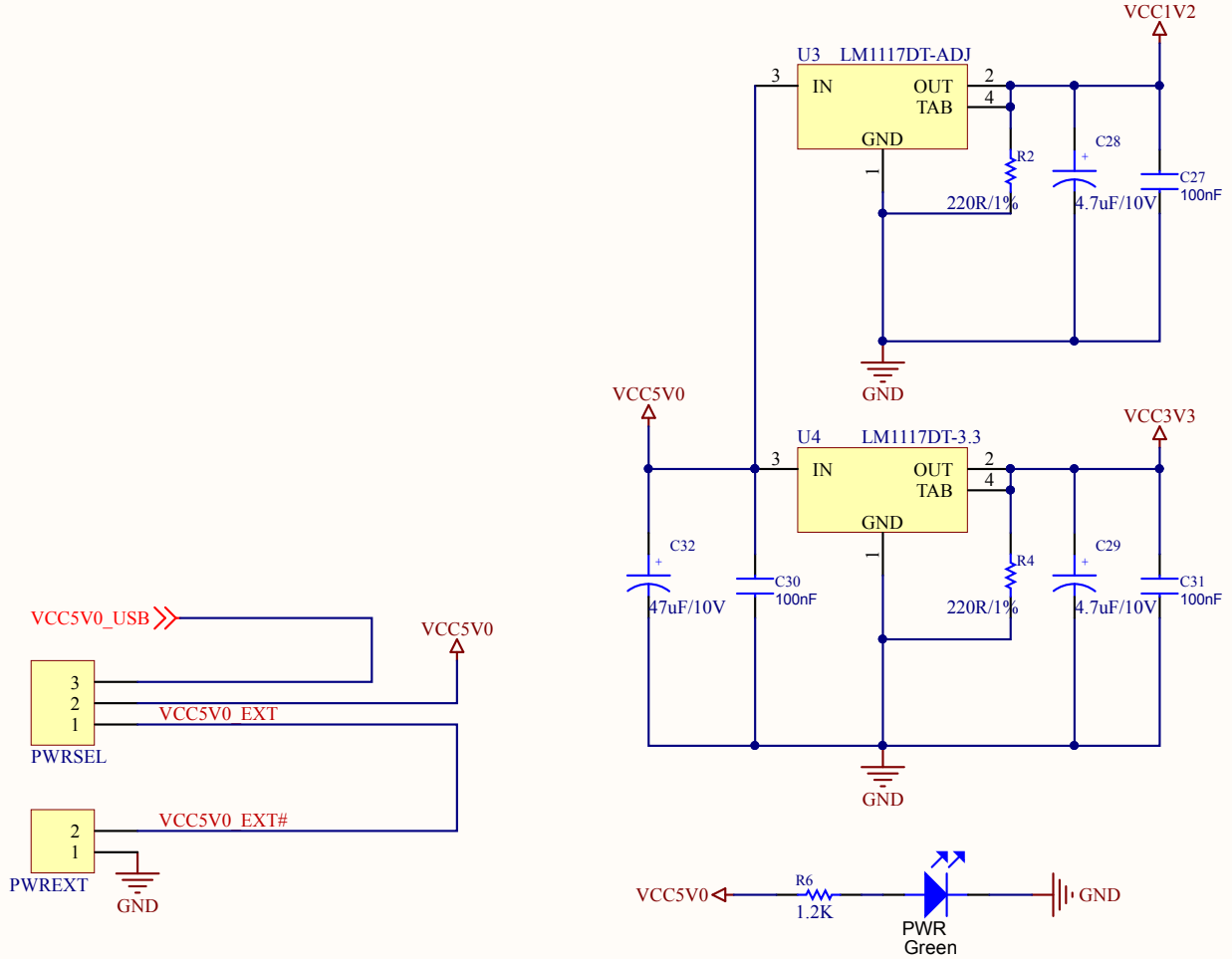
www.posedge.ir

Posedge-One SPARTAN-6 FPGA Development Board
Rev 1.2

SPARTAN-6 LX 9 FPGA
On-Board USB-JTAG Programmer
512 KB SRAM Memory
USB-FIFO Interface (Up to 10 MB/s transfer speed)
64 Mbit QSPI Flash
48 User I/O

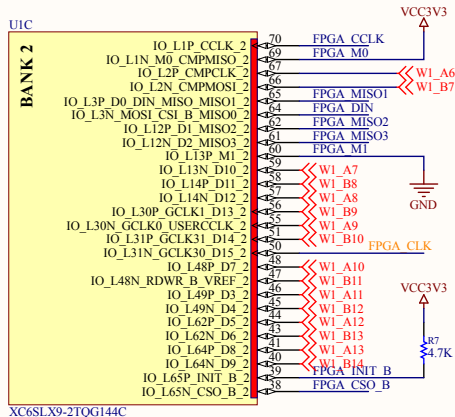
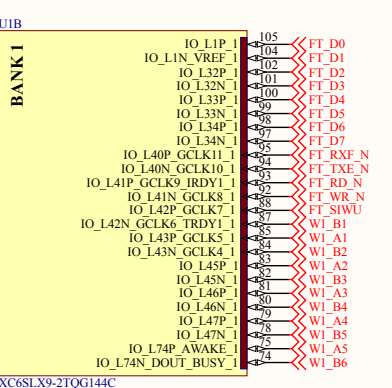
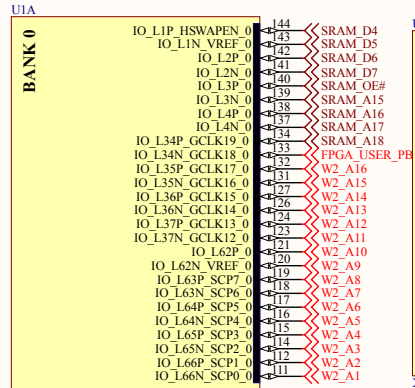
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POWER



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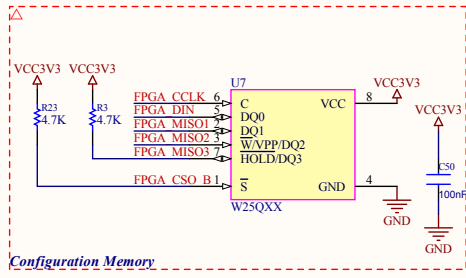
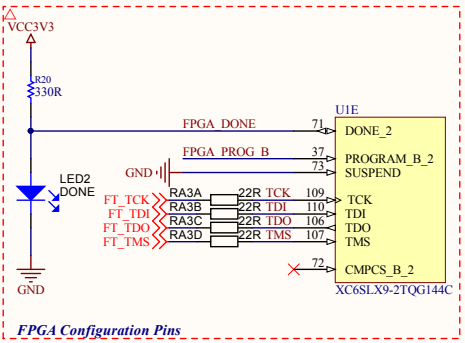
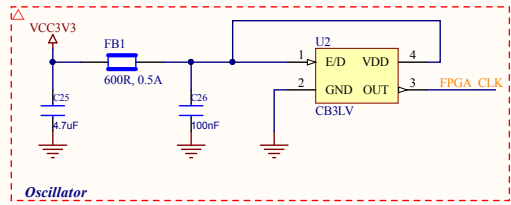
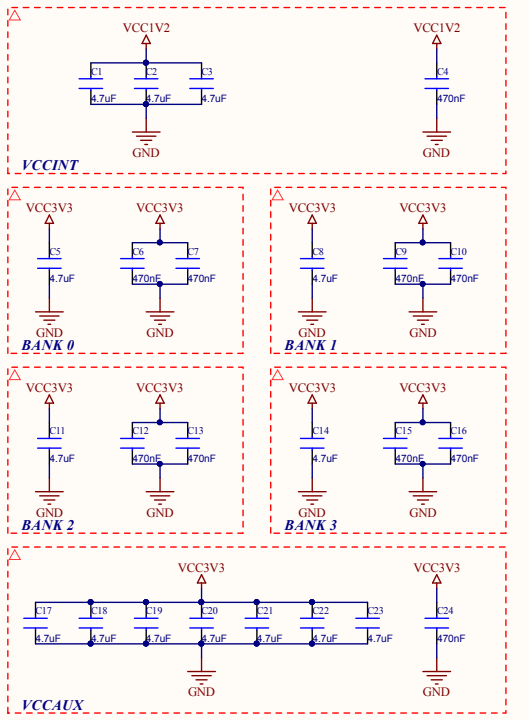
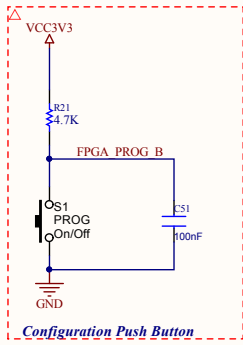
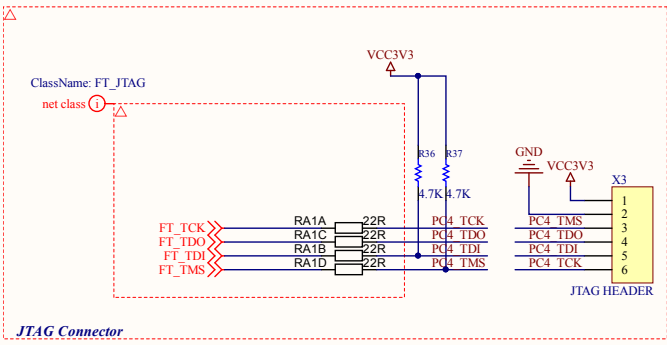
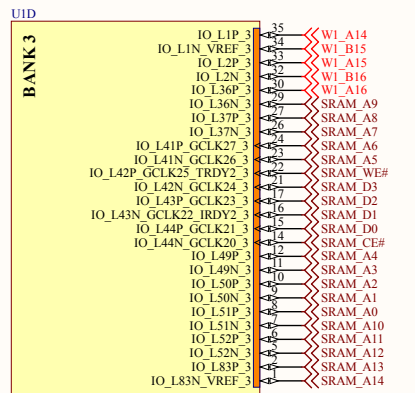
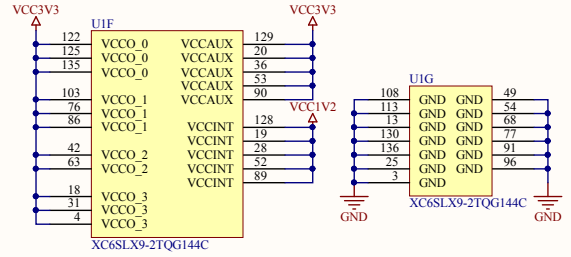
FPGA



Orange Nets are Clock pins which should be connected to GCLK pins

Blue Nets are config pins with fixed position

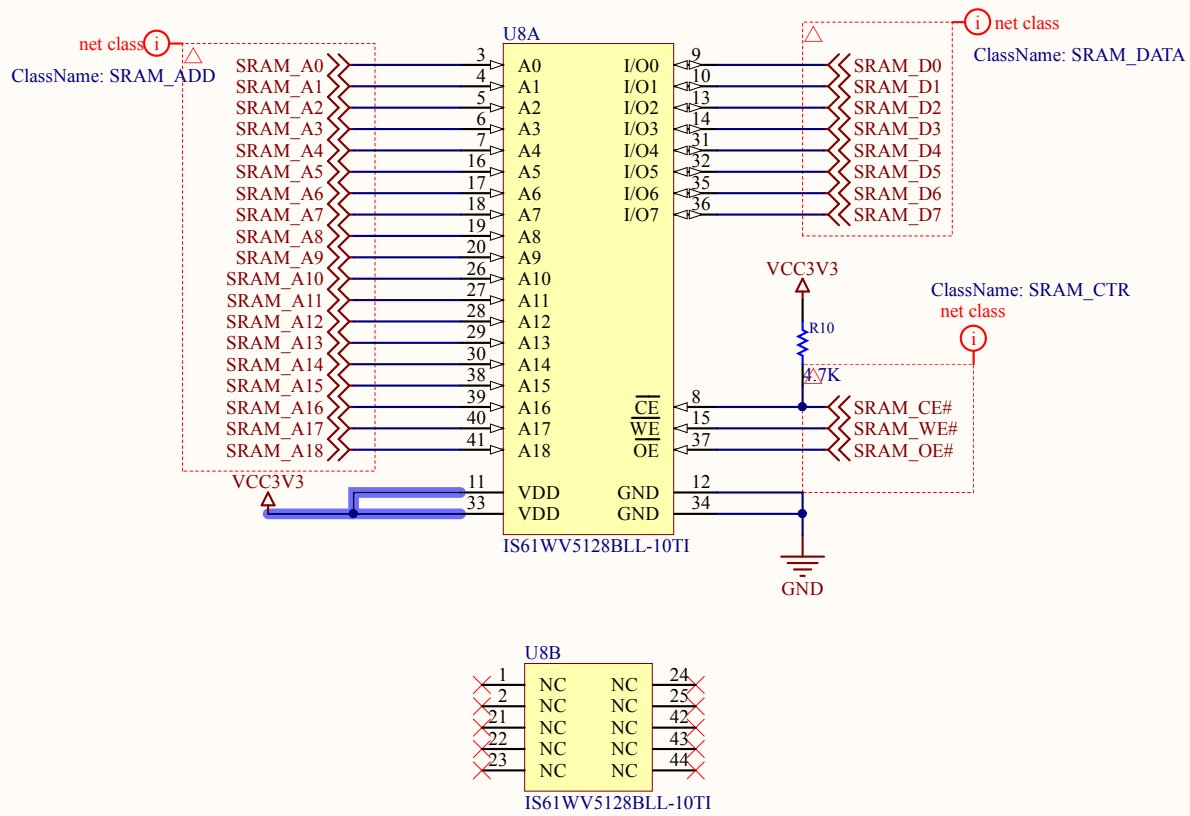
Red Nets are GPIO and could be place on any GPIO pin of the FPGA



Decoupling according to UG393



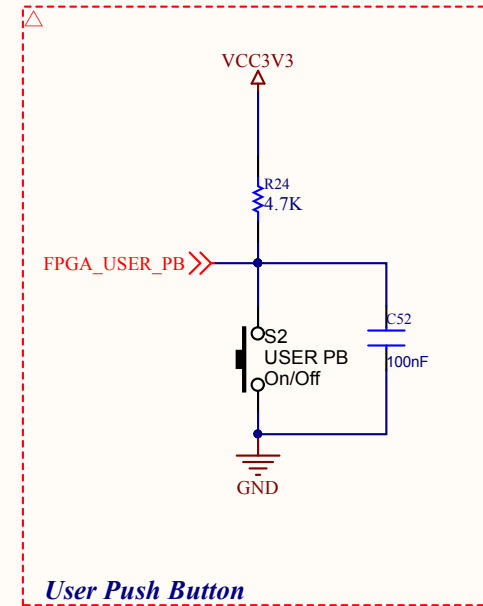
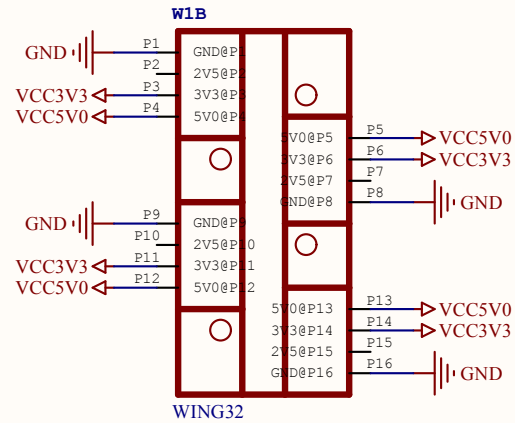
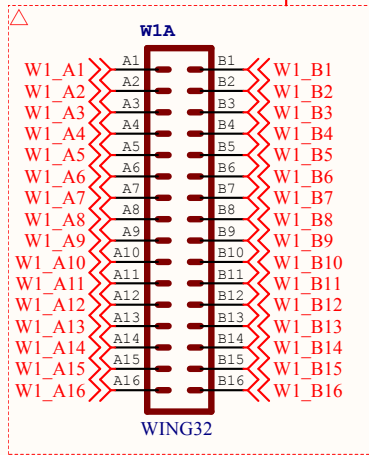
SRAM



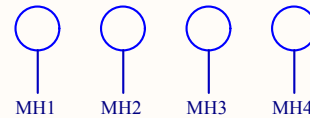
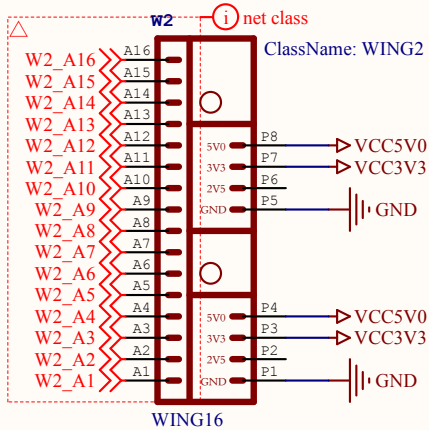
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GPIO

ClassName: WING1
net class



ClassName: WING2
net class



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USB-JTAG

