


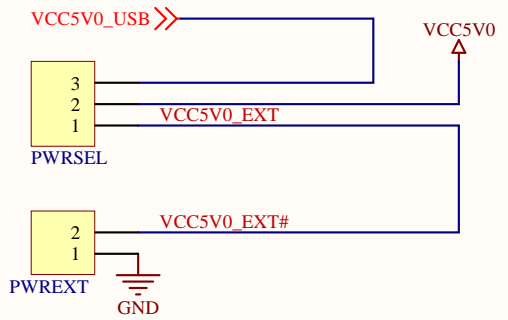
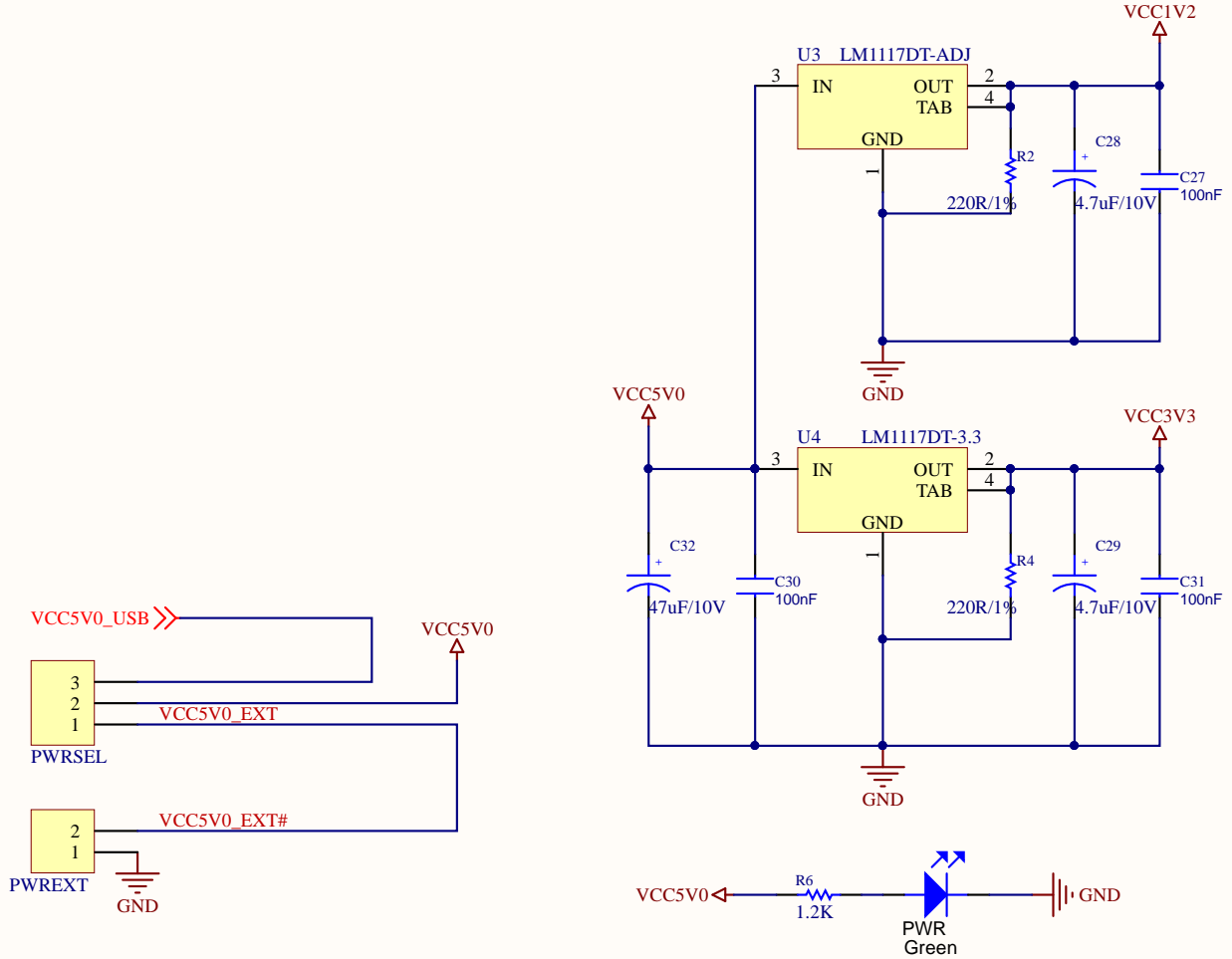
www.posedge.ir

Posedge-One SPARTAN-6 FPGA Development Board
Rev 1.3

SPARTAN-6 LX 9 FPGA
On-Board USB-JTAG Programmer
512 KB SRAM Memory
USB-FIFO Interface (Up to 10 MB/s transfer speed)
64 Mbit QSPI Flash
48 User I/O

Title <i>Posedge-One SPARTAN-6 Development Board</i>			<i>www.posedge.ir</i> <i>TORANJ Inc.</i>	
Size: <i>A</i>	Number:	Revision: <i>1.3</i>	<i>Isfahan Science and</i> <i>Technology Town, Isfahan</i>	
Date: <i>11/26/2016</i>	Sheet <i>1</i> of <i>6</i>		<i>IRAN</i>	

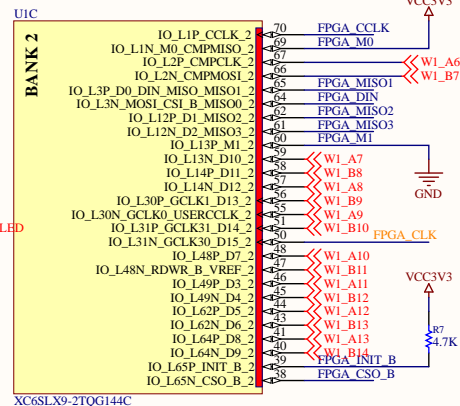
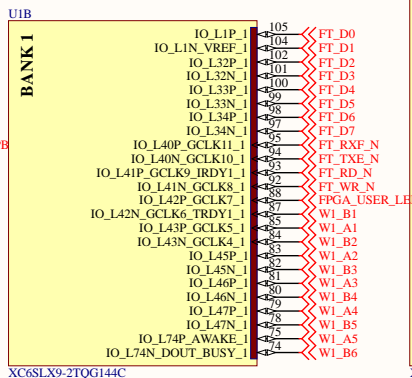
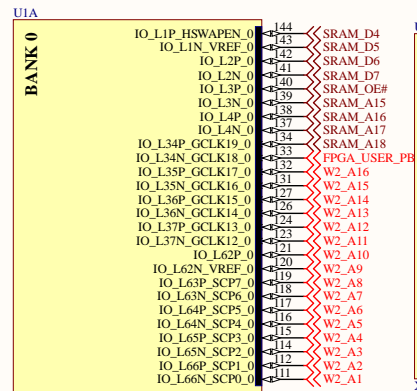
POWER



Title Posedge-One SPARTAN-6 Development Board		www.posedge.ir TORANJ Inc.	
Size: A	Number:	Revision: 1.3	
Date: 11/26/2016	Sheet 2 of 6		Isfahan Science and Technology Town, Isfahan IRAN



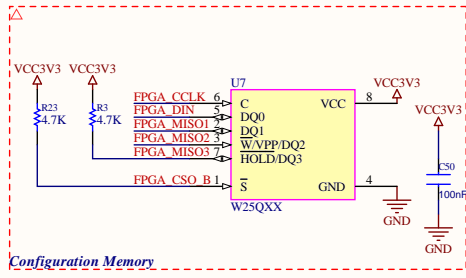
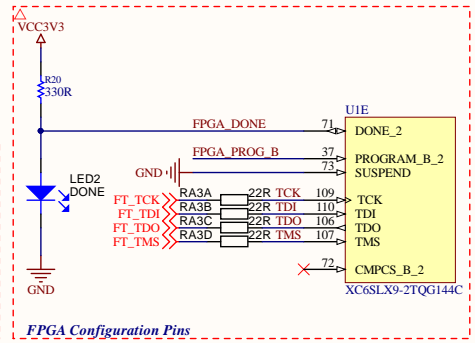
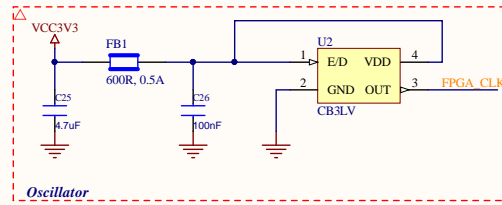
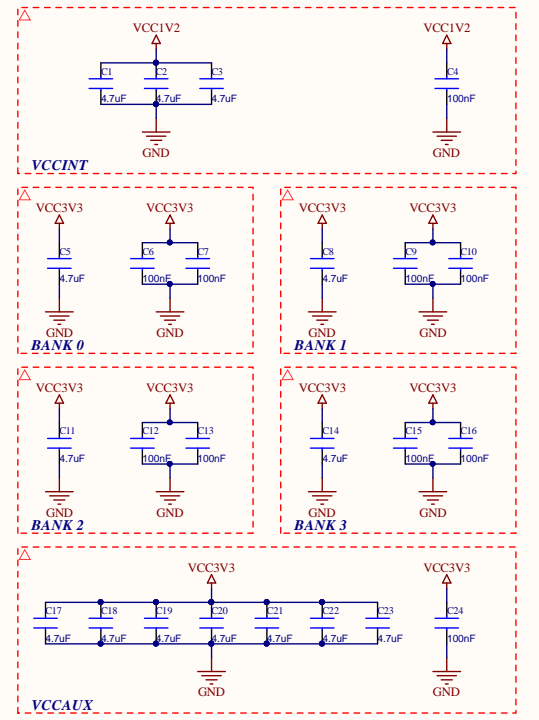
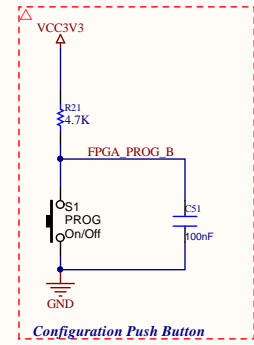
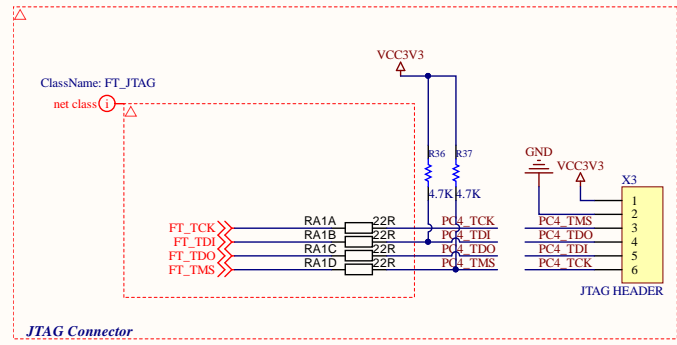
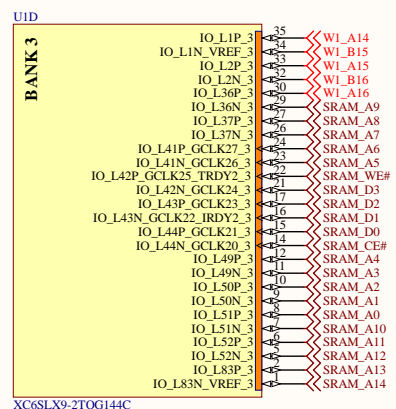
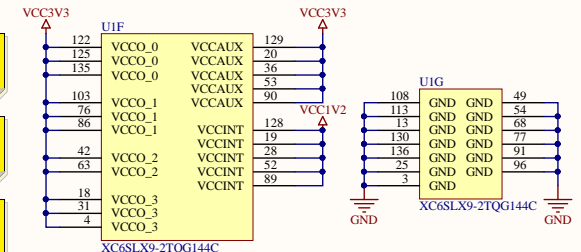
FPGA



Orange Nets are Clock pins which should be connected to GCLK pins

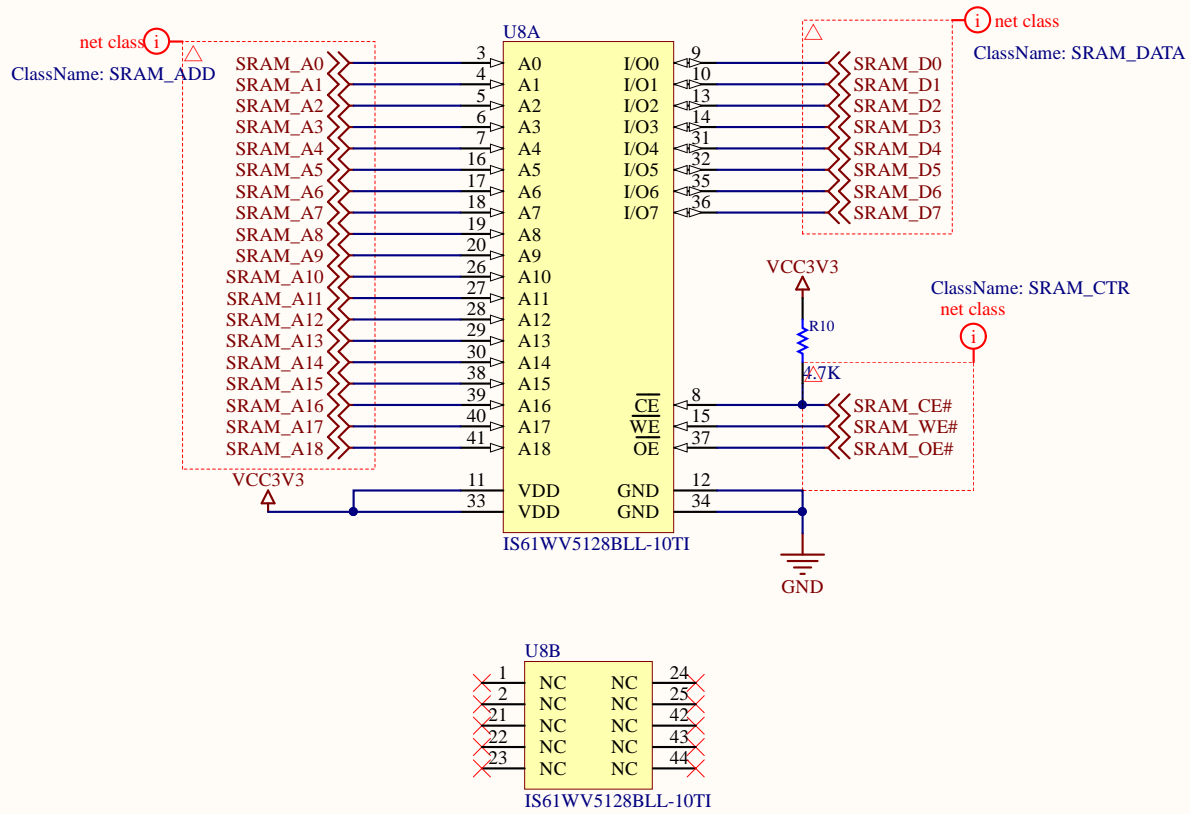
Blue Nets are config pins with fixed position

Red Nets are GPIO and could be place on any GPIO pin of the FPGA



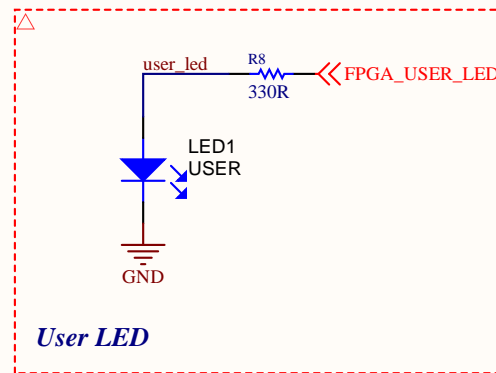
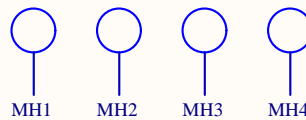
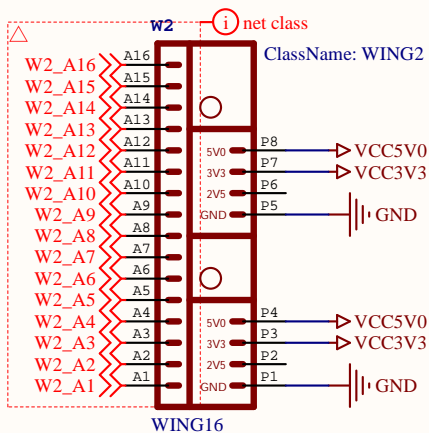
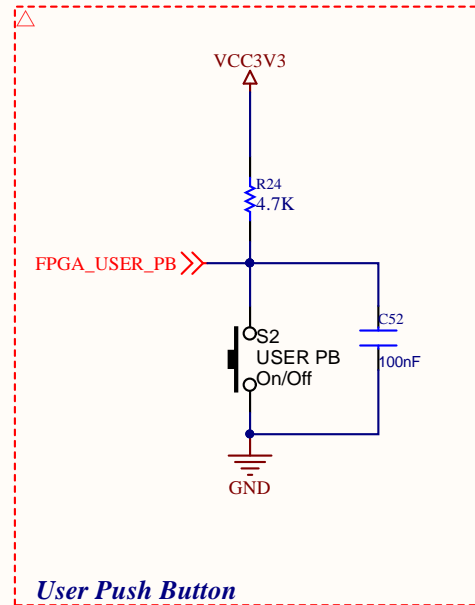
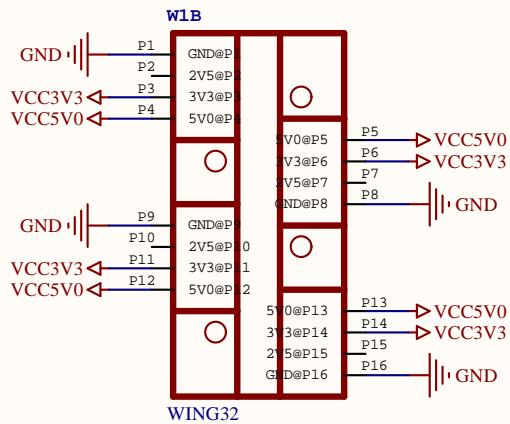
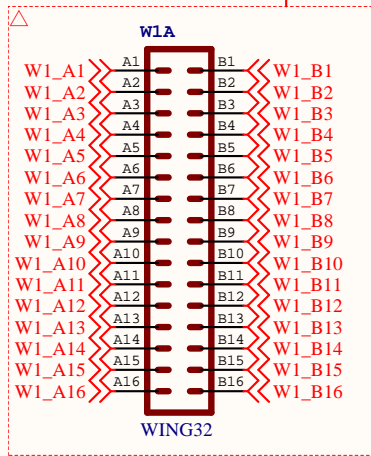
Decoupling according to UG393

SRAM



GPIO

ClassName: WING1
net class



USB-JTAG

