Design of an 8x8 SRAM Array in 65nm technology

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***Abstract*— The aim of this project is to build an 8-row by 8-bit SRAM memory array, using the 65nm CMOS technology. Using a 3-to-8 decoder, the SRAM array is accessed by a 3-bit address. The SRAM cells are designed to achieve lowest power consumption and suitable static noise margin, while operating at 100 MHz Read & Write cycles. The test-bench, the implementation, and the layout of the SRAM array and the decoder are done using software simulations through Cadence Virtuoso's Analog-Design Environment (ADE).**

***Index Terms*— Cadence, CMOS, Decoder, Layout, Static Noise Margin, SRAM.**

I. Introduction

Semiconductor memories have always been an essential part of any computer storage system. The regular demand for higher storage space with less power and less area has been the driving force for the development in this field, especially in random-access memories (RAMs), since they offer higher read and write speeds than other types of memories, Among the most common RAM types are the static RAMs (SRAMs) and dynamic RAMs (DRAMs).

In the proposed system, the 6T SRAM architecture is used. Even though SRAMs usually require larger area and are more expensive than DRAMs, they are much faster, compatible with CMOS technology, and don't require periodic-refreshing circuits to keep its data while power supply is on. In the following sections, the design & the testing process are explained in detail, with the results and conclusion presented in sections VI and VII, respectively.

II. System Overview

The SRAM array consists of 8 rows, each comprises 8 6T-SRAM cells. One SRAM cell represents 1 bit of data that could be read from, or written to. Each bit, or individual SRAM cell, is accessed by 2 complementary bit lines. The SRAM rows are accessed by a word line, that is activated using a 3-to-8 CMOS decoder. The inputs to the decoder are a 3-bit address that chooses which word line to activate, and an enable. The system operates at 100 MHz, in which the Read or Write information is obtained during half of the cycle, and a refresh operation occurs in the second half.

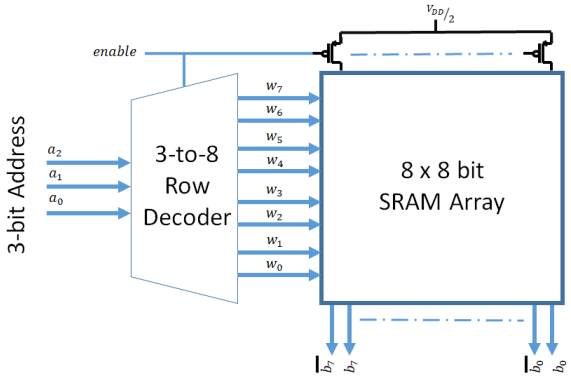


Fig. 1. SRAM array & Decoder block diagram

III. Static Random-Access Memory (SRAM)

A. Circuit

The basic block in the proposed SRAM array is the 6-transistor SRAM cell [1], as shown in Fig. 2. This circuit depends primarily on two back-to-back inverters to maintain the stored data. Transistors M5 and M6 are responsible of reading from the inverters or writing to them. During the Read operation, the bit lines are not driven by external sources, and the stored data is transferred to the bit lines as soon as the word line activates M5 and M6. In the Write operation, the bit lines are driven by a high and a low signal, that are passed by M5 and M6 to change the values of Q and Q-bar.

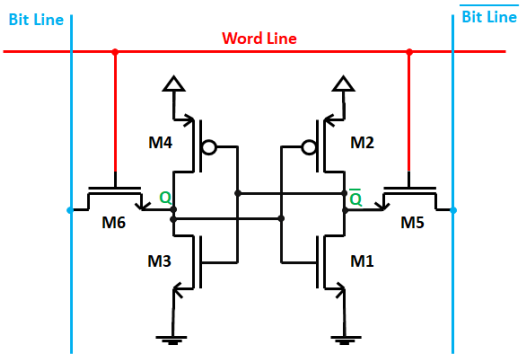


Fig. 2. SRAM array & Decoder block diagram

To ensure the cell works properly, where the data in the cell is not affected by whatever voltage is on the bit line during the Read operation, and where the pass-NMOS transistors are strong enough to pass the voltage on the bit lines onto the Q and Q-bar during the Write operation, the sizes of the transistors are chosen carefully according to the cell ratio and the pullup ratio, given by equations (1) and (2), respectively. Increasing the cell ratio gives a better Read operation, while decreasing the pullup ratio helps the Write operation.

$$Cell\ Ratio = \left(W_1/L_1\right) \Big/ \left(W_5/L_5\right) \quad (1)$$

$$Pullup\ Ratio = \left(W_4/L_4\right) \Big/ \left(W_6/L_6\right) \quad (2)$$

B. Static Noise Margin

The static noise margin (SNM) is a measure of the SRAM's stability in the presence of noise [2 – 4]. The test bench used to obtain the SNM is shown in Fig. 3 and 4, for the Read and Write operations, respectively.

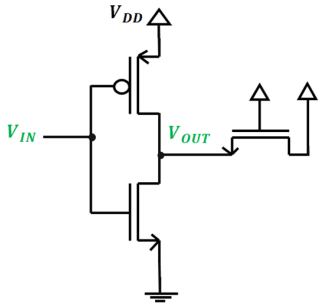


Fig. 3. Testbench for the Read SNM

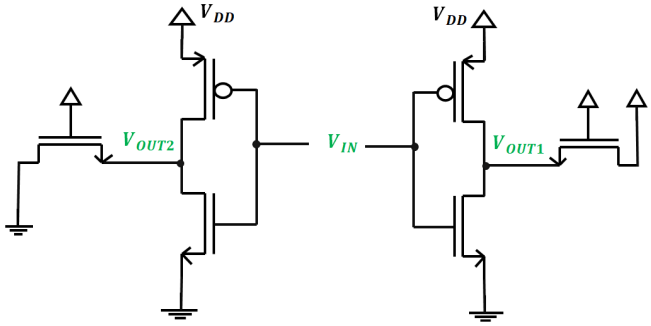


Fig. 4. Testbench for the Write SNM

To obtain the SNM value, the biggest square that can fit between the characteristic curves of the back-to-back inverters should be found. That is done by first finding the longest diagonal between the 2 curves, then using that diagonal to draw the square. The curves, shown in Fig. 5 and 6, are obtained at a supply voltage of 1 V for the Read and the Write operations in the DC analysis.

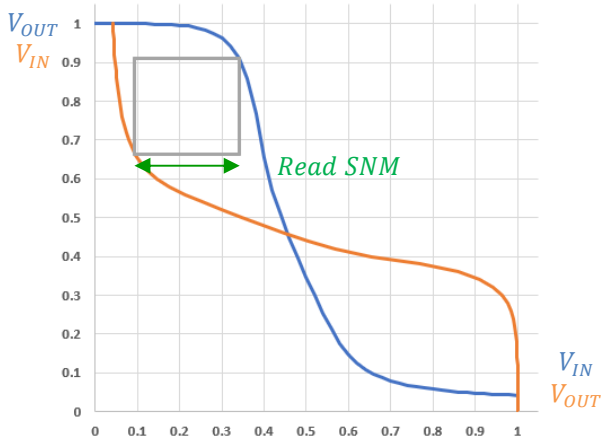


Fig. 5. Read Static Noise Margin

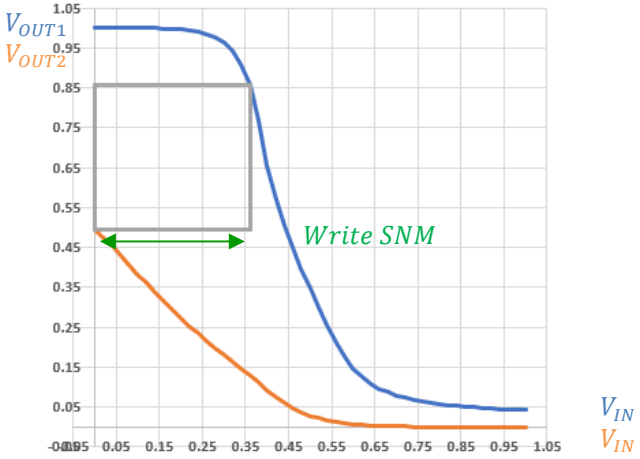


Fig. 6. Write Static Noise Margin

C. Transient Simulations

To test a single SRAM cell, the setup shown in Fig. 7 is used. Since each bit line is connected to 16 SRAM cell, a large capacitor representing these transistors need to be connected to each bit line. The enforcing voltage sources connected to the bit lines are only connected to the bit lines during the Write operation.

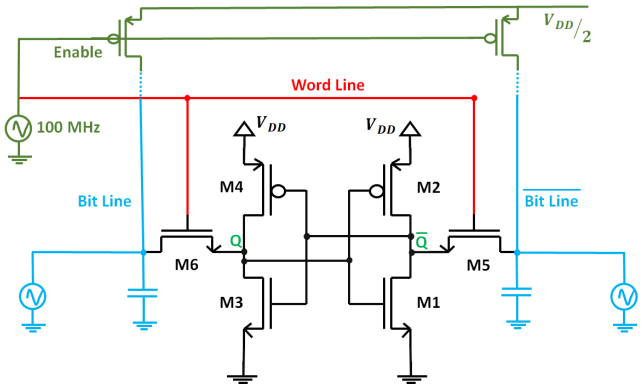


Fig. 7. Testbench for transient analysis

A 100 MHz source is used to drive both the word line and the refresh PMOS transistors. When the word line is high, the pass NMOS transistors transfer information from or to the SRAM cell. During the other half cycle (while the

word line is low), the SRAM cell is separated from the bit lines, and the bit lines are charged to half of V_{DD}. This is to improve the Write and Read operations. From the waveforms in Fig. 8 and 9, it is noticed that the values change due to the Read or the Write operations only when the word signal is high. In the Read operation, the bit line that goes to high only reaches to about 0.7 V and not V_{DD} since the pass transistor is an NMOS device that passes a weak 1. In the Write operation, the pull-up PMOS transistor of the back-to-back inverters is weak causing the stored 1 to be less than V_{DD}.

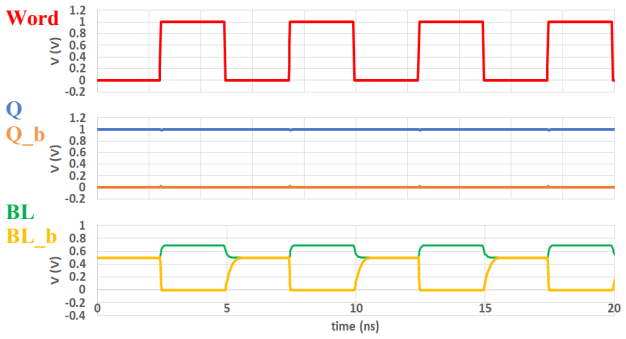


Fig. 8. Waveforms of the Read Operation

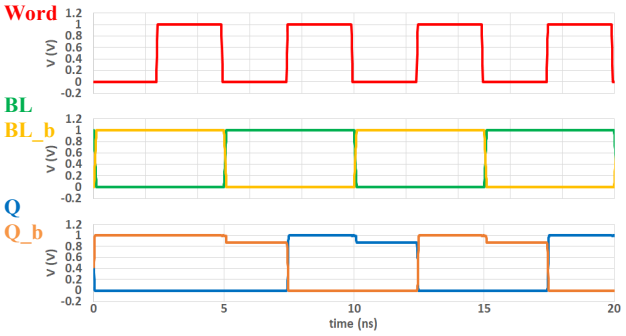


Fig. 9. Waveforms of the Write Operation

IV. Row Decoder

A. Circuit

The information in the SRAM array is accessed through the word lines. Each word line is connected to the output of a 3-to-8 decoder whose input is a 3-bit address. An extra input is used as an Enable signal, that enables the decoder for half of the 100 MHz cycle, and disables it during the second half where the bit lines are refreshed (pulled to $V_{DD}/_2$). The full circuit of the decoder is shown in Fig. 10 [5].

The gates used to build the decoder are simply static CMOS inverters and 4-input NANDs. 4-input NANDs are used since there are 3 inputs from the address and 1 from the enable. The transistors of the inverter are sized to give equal rise and fall times, and those of the NAND are sized such that the worst-case delay would equal the delay of the inverter.

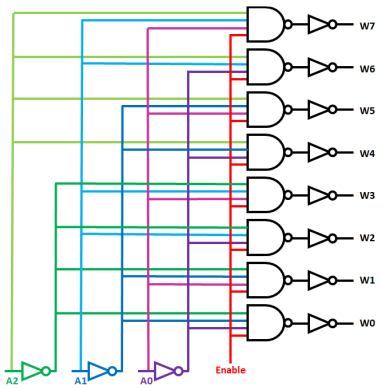


Fig. 10. 3-to-8 Decoder with enable circuit

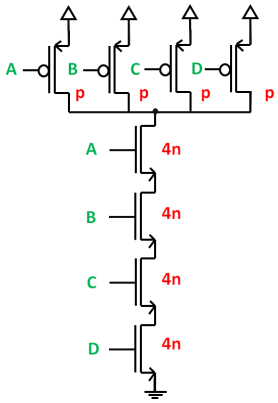


Fig. 11. 4-input static CMOS NAND gate

B. Transient Simulations

From the transient analysis of the decoder shown in Fig. 12, it is shown that only one output is high per address combination and only when the enable is high. This simulation is done after including the loading effects from the SRAM array word lines.

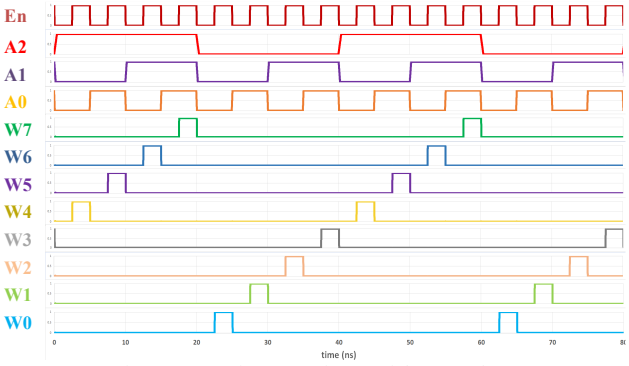


Fig. 12. Transient waveforms of the Decoder

V. Layout

The layout design process is done in a hierarchical fashion. Each block's layout is designed individually before integrating the whole system. The layout of the individual SRAM cell is shown in Fig. 13. Bit lines are represented by the metal-1 lines at the sides of the block, the power rails are placed at the top and the bottom of the cell to be easily joined to the adjacent cells, and the gate terminals

connected are connected using polySi (including the word lines).

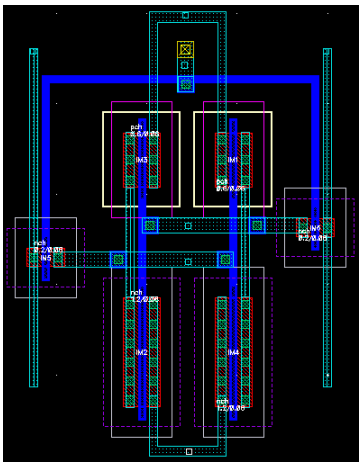
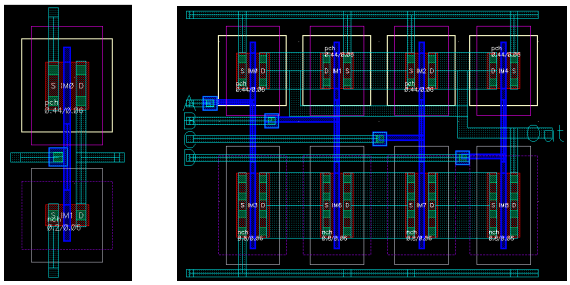


Fig. 13. SRAM Layout

For the decoder, the layout of the inverter and the NAND are designed first (Fig. 14(a) and 14(b)), then the whole decoder is put together, as shown in Fig. 15. By placing the power rails at the top and the bottom of the gates, every row (NAND and inverter pair) in the decoder is a vertical flip with respect to the row above and below it. This is to save area by having common V_{DD} and ground rails.



(a) (b)

Fig. 14. Layout of the static CMOS gates (a) inverter (b) NAND

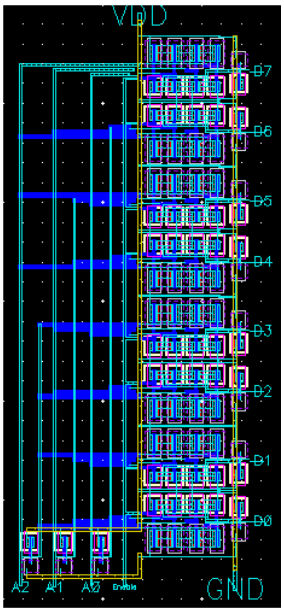


Fig. 15. Decoder Layout

Fig. 16 shows the layout of the whole SRAM array system. As what was done in the decoder layout, each SRAM row shares either a V_{DD} rail or a ground rail with the upper and the lower rows, by flipping every other row vertically. Bit lines for all columns are connected by metal-1, the word line of each row is implemented using metal-2, and the power rails of the whole system are connected using metal-3. The total area of the layout is 1883.08 μm^2.

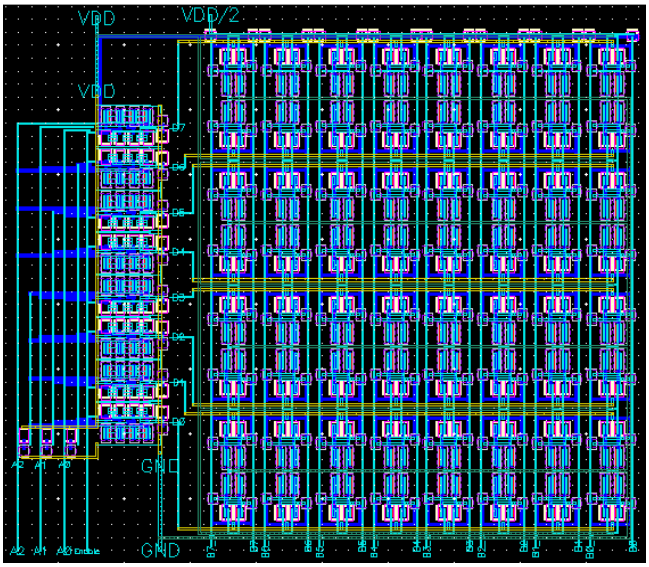


Fig. 16. Whole System Layout

VI. Final Results

The SRAM array system is built using TSMC 65nm CMOS technology, with a power supply of 1 V. Final system parameters obtained from the proposed design are shown in Table 1. From the DC characteristic curves of the SRAM cell, the SNM is found to be 0.246 V in Read operation and 0.361 V in Write operation.

The Read and the Write operations operate at a 100 MHz frequency. In the Write operation, the delay has been defined as the time from when the word line raises to half of V_{DD} till the time the Q transitions to half of V_{DD}. Since the bit lines are refreshed to half of V_{DD} in each cycle, the delay in the Read operation is found from when the word line raises to half of V_{DD} till the time when the bit line reaches its final value.

TABLE I
Final System Parameters

Parameter		Value
Technology		65nm CMOS
Supply Voltage (V_{DD})		1 V
Frequency (f)		100 MHz
Power Consumption (P)		109.72 uW
Static Noise Margin	Read	0.2461 V
	Write	0.3606 V
Delay	Read	53.2 ps
	Write	43.1 ps
Total Area (A)		40 um x 47.077 um = 1883.08 μm^2

VII. Conclusion

The presented work introduces the design and the layout of an 8x8 SRAM array with a 3-to-8 row decoder that is built using the TSMC 65 nm CMOS technology and operates at 100 MHz, with a power supply of 1V. The SRAM cell is designed to have a SNM of 0.246 V and a delay of 53.2 ps in Read operation, and a SNM of 0.360 V and a delay of 43.1 ps in Write mode. The total average power dissipation of the whole system is about 109.72 uW and the total area of the layout is 1883 μm^2.

Many improvements can be done on this system in future work, like increasing the storage capacity and operating at much higher frequencies. The system can also be expanded by including sense amplifiers to the bit line and its compliment, which is useful when the capacitance on the bit lines increase from adding more rows and the voltage read from the SRAM cell is weak.

References

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