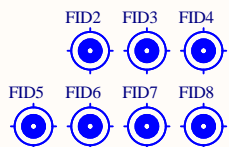
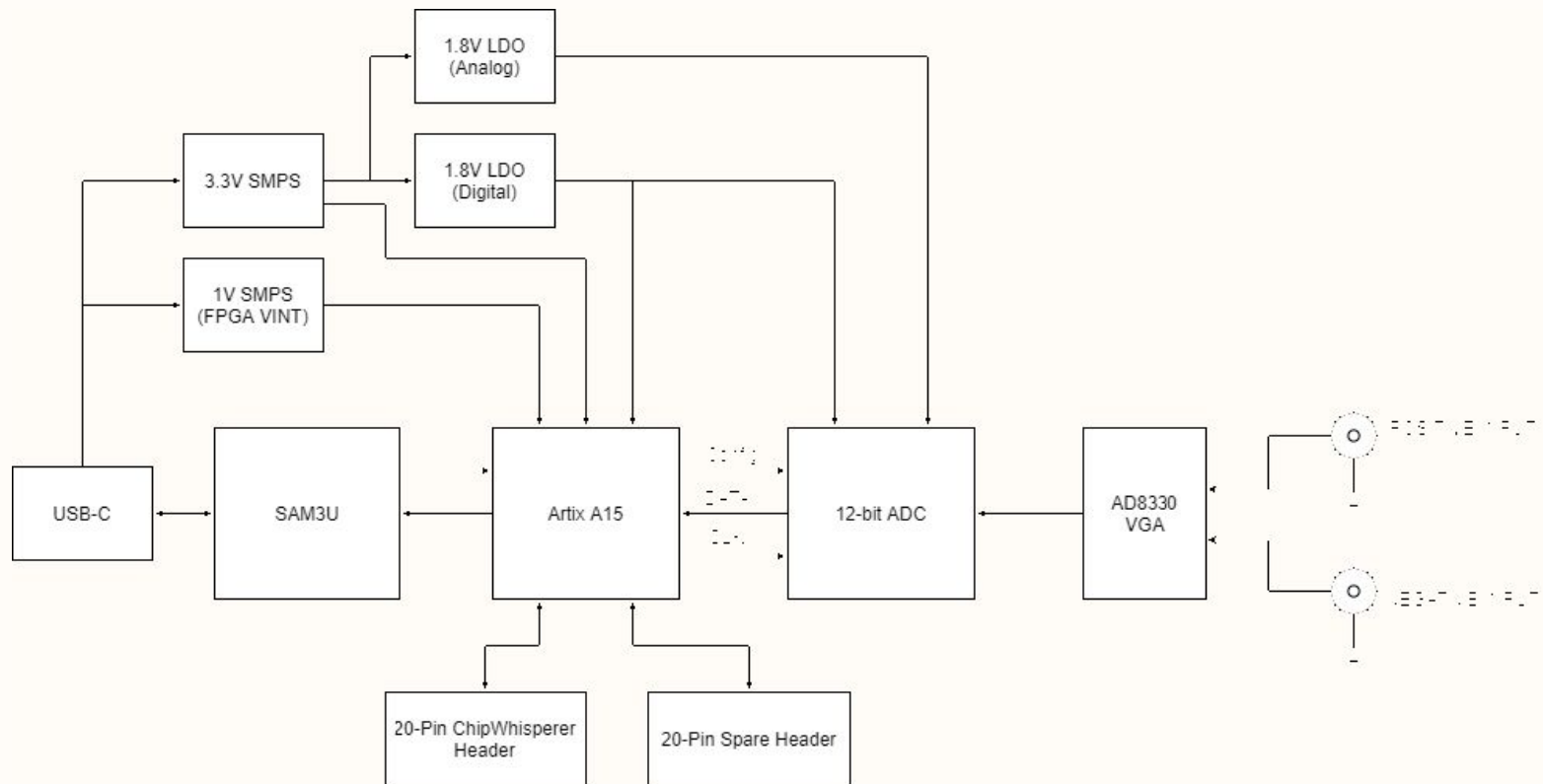


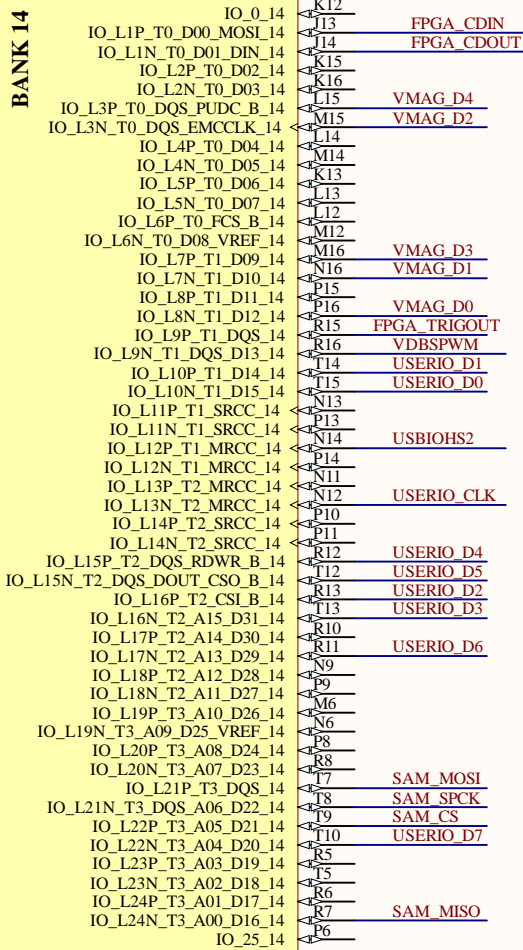


ChipWhisperer-Husky

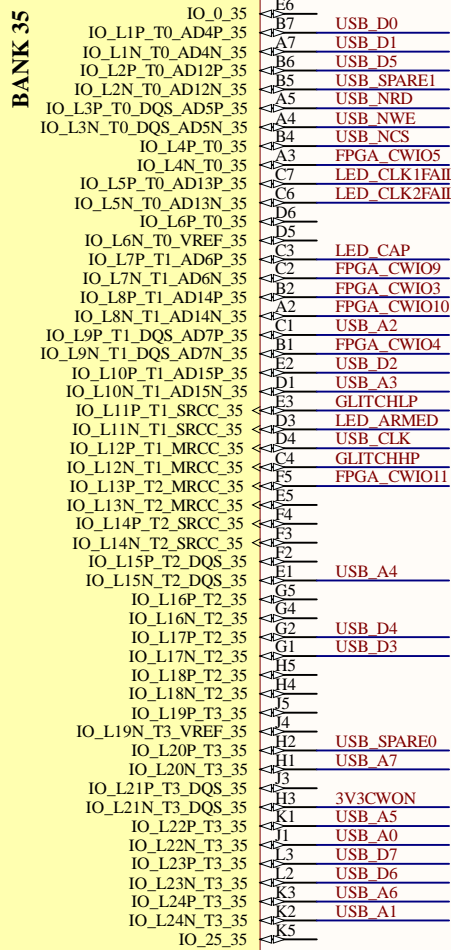


Title: Info & Block Diagram			 Approved: YES		
Rev: 03	Project: CW-Husky		License: TBD		
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File: cwh_frontpage.SchDoc			NewAE.com		

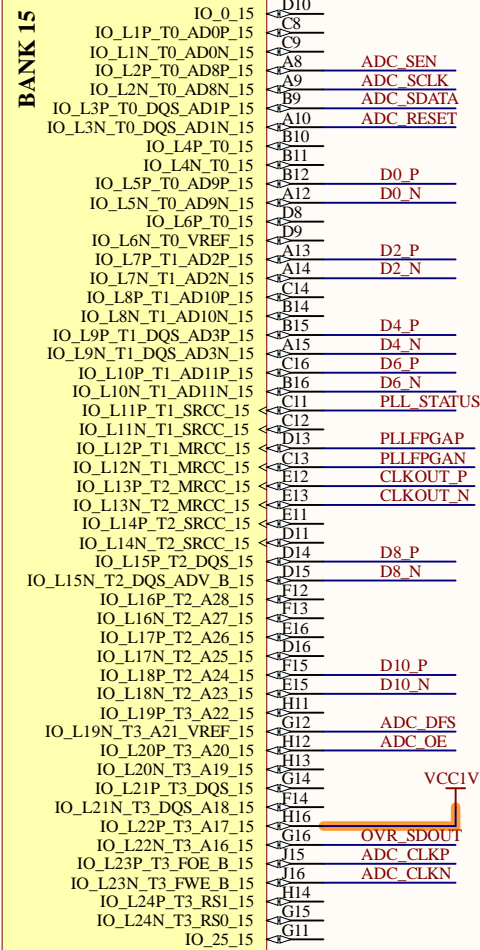
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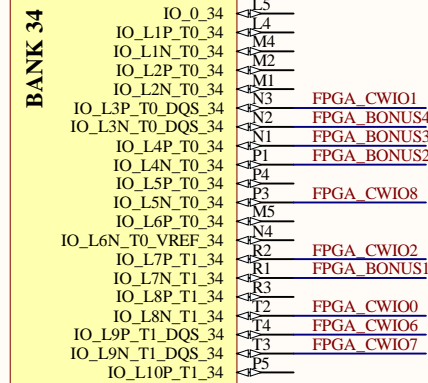
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U2B



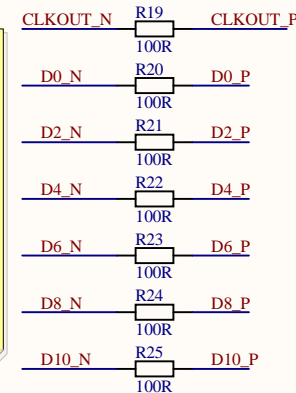
U2C



VCCIO=1.8V for this bank.

LVDS on A7 requires VCC=2.5, but ADC I/O is at 1.8V, so need to use VCC=1.8V. LVDS should work according to refs at VCCIO=1.8V, but it's marginal.

ADC supports LVCMOS18 in case LVDS doesn't work - depopulate LVDS term if required.

Title: **FPGA I/O**

Approved: YES



Rev: 03

Project: CW-Husky

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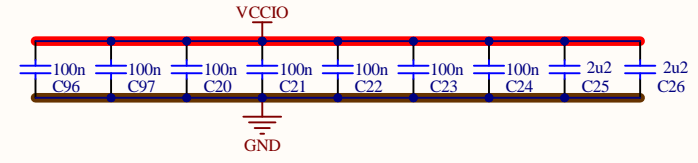
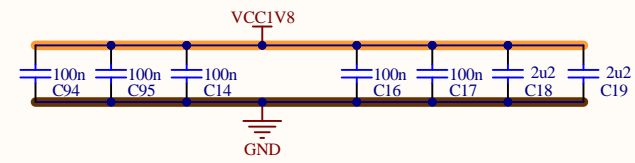
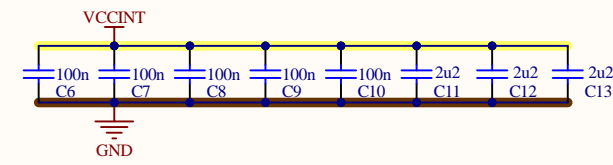
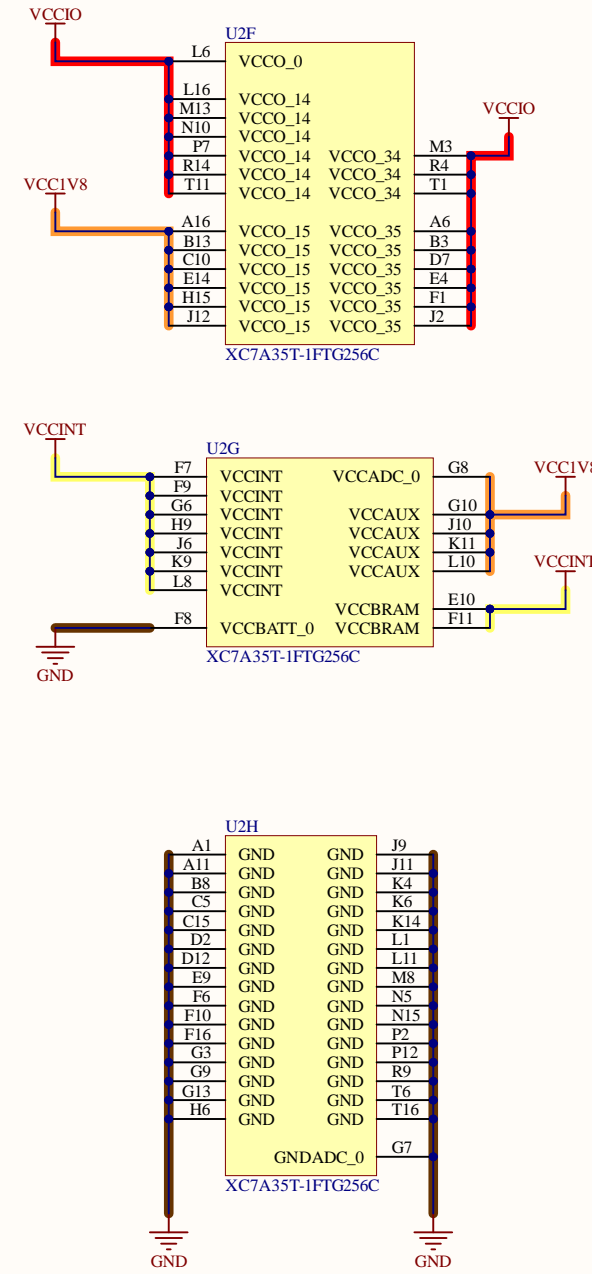
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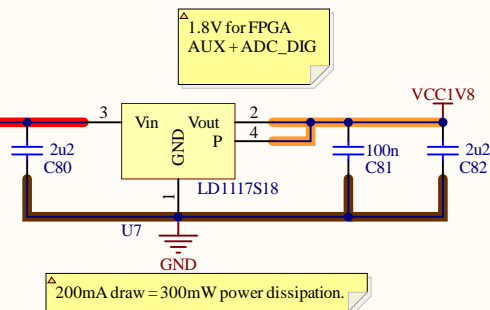
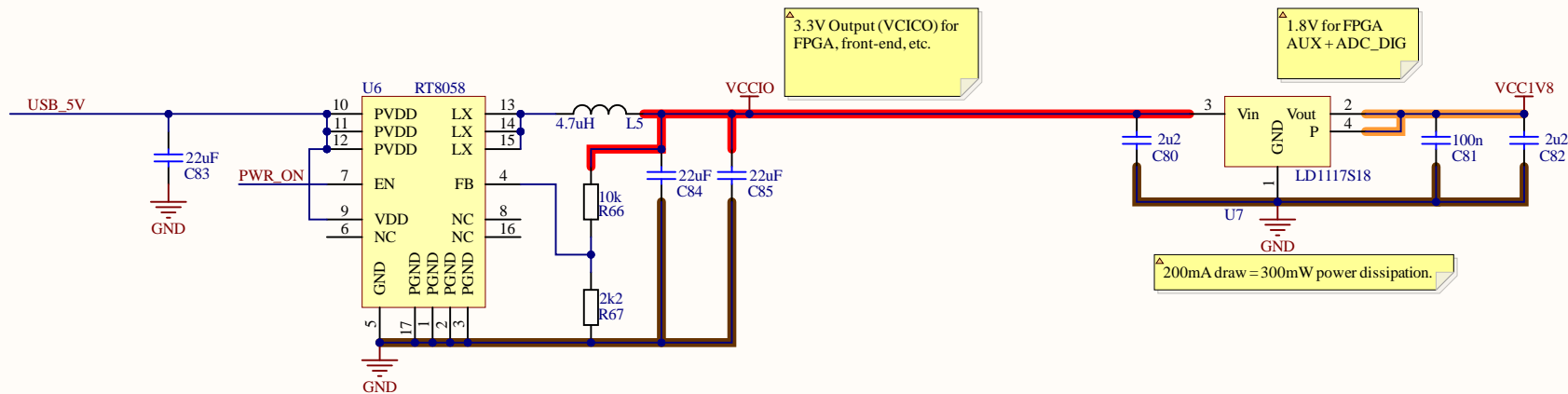
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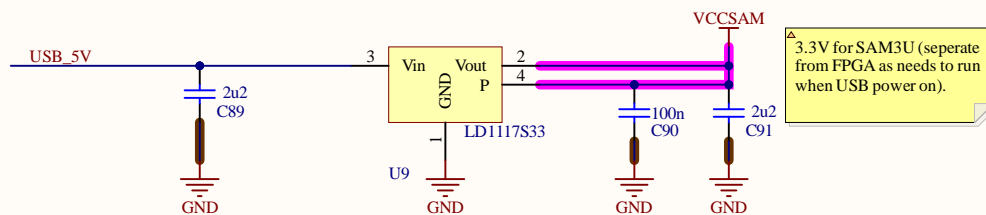
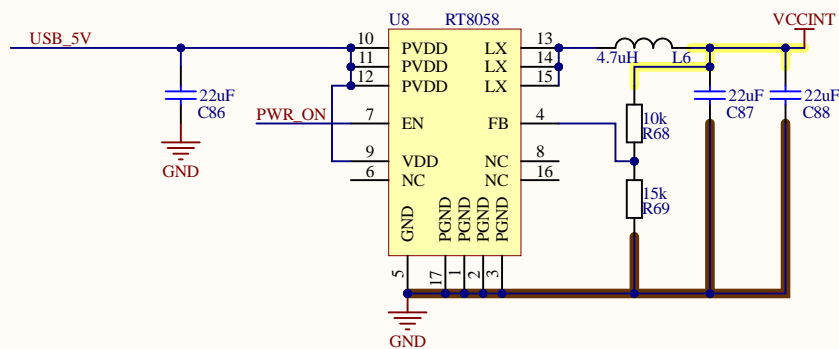
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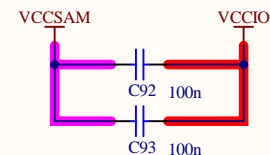


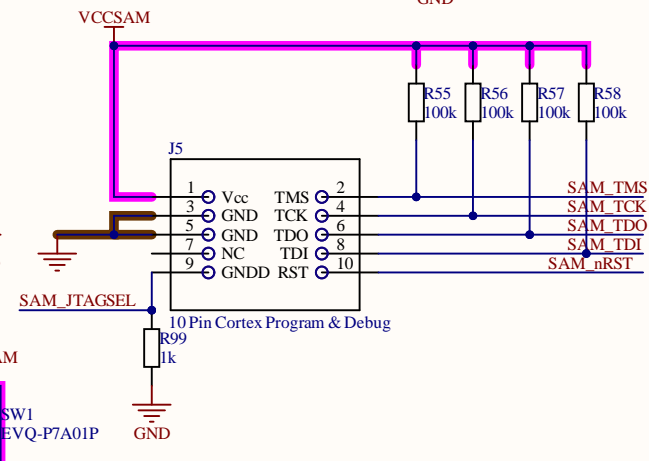
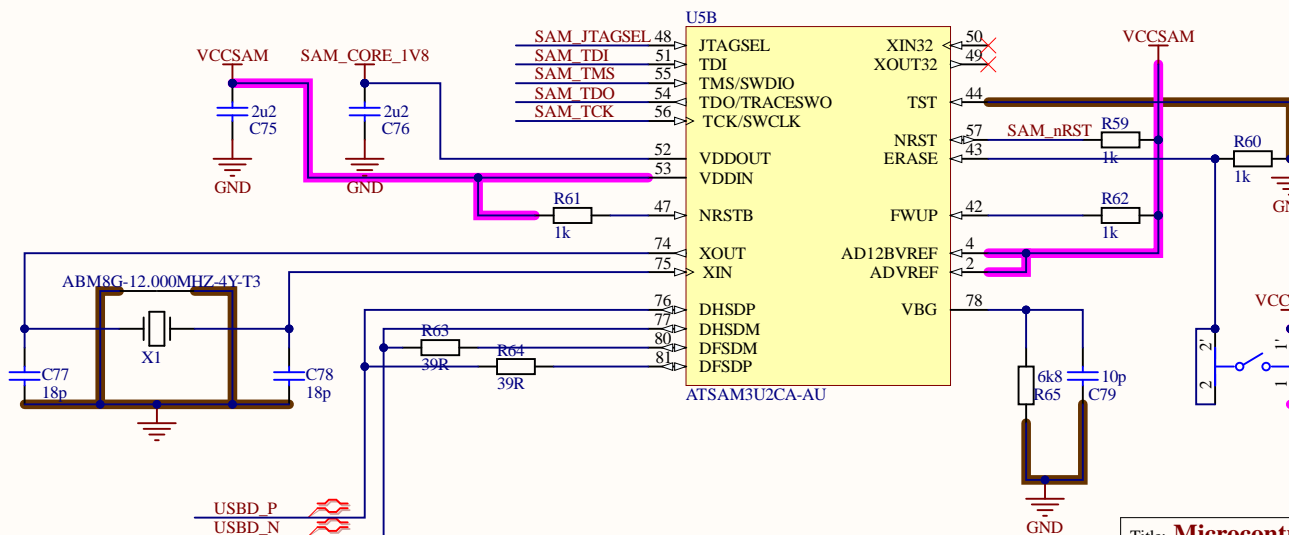
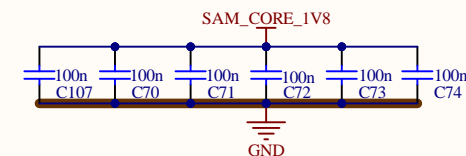
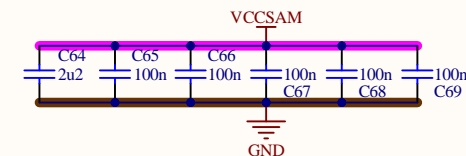
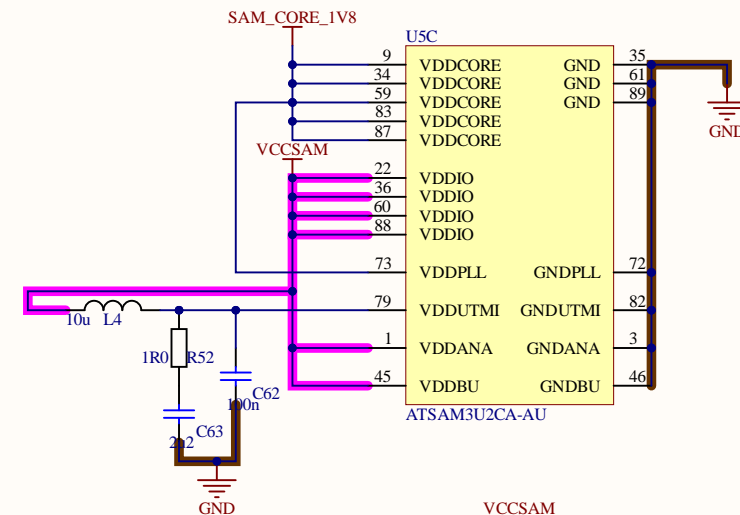
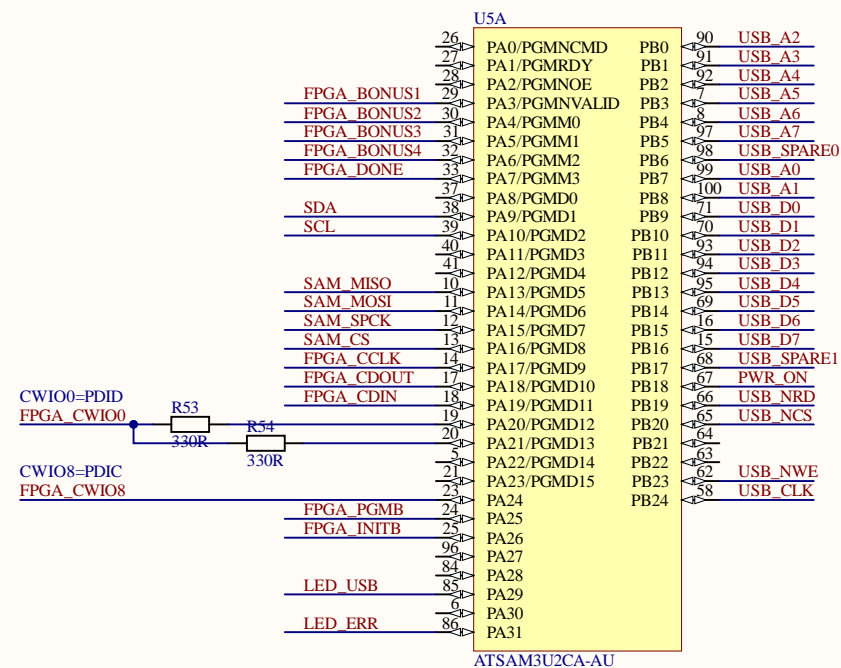


200mA draw = 300mW power dissipation.



NOTE: The power domains for SAM3U and FPGA on 3.3V are different. Need caps when crossing planes, as high-speed signals are forced to somewhat cross this plane :(
TODO - add as many as needed depending on routing.



Title: **Microcontroller**

Approved: YES

Rev: 03

Project: CW-Husky

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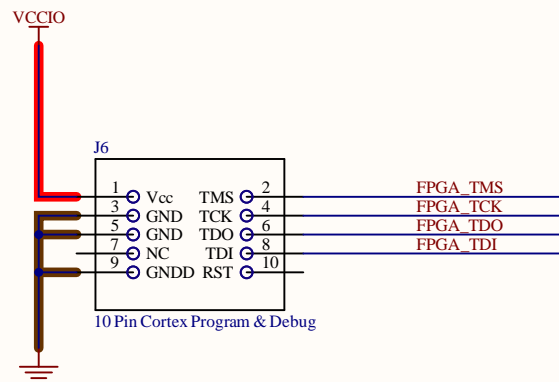
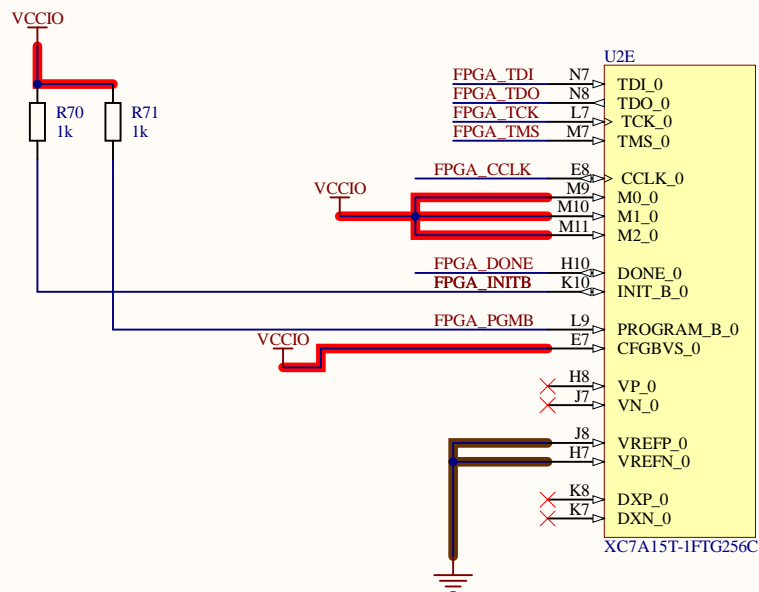
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Title: **FPGA Misc**

Approved: NO

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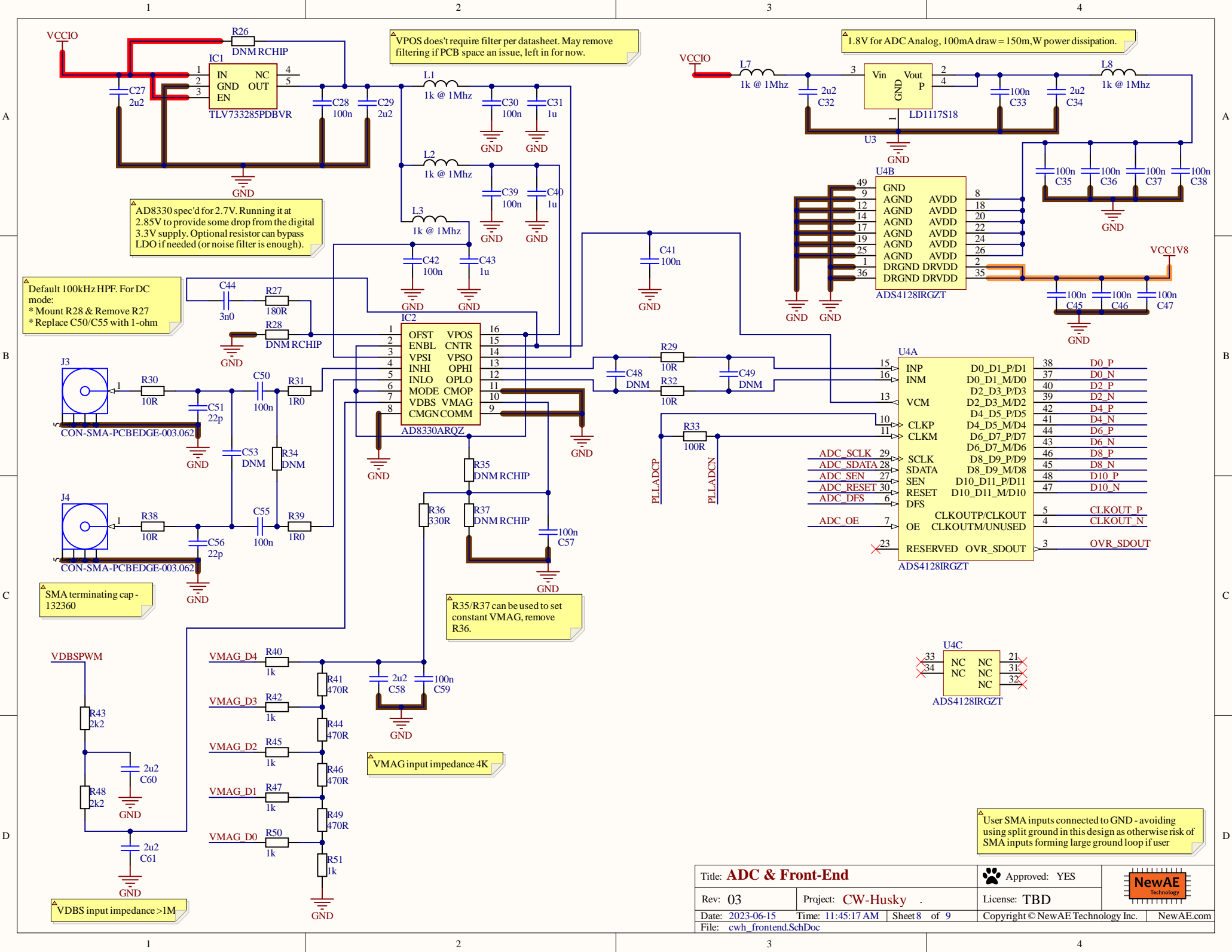
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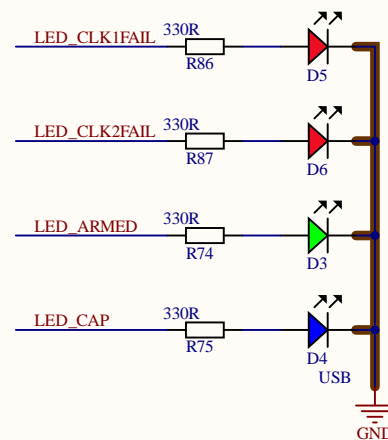
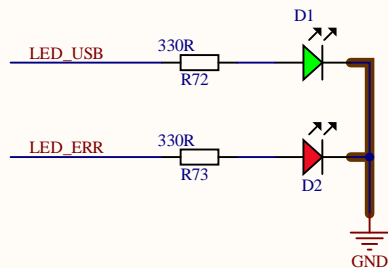
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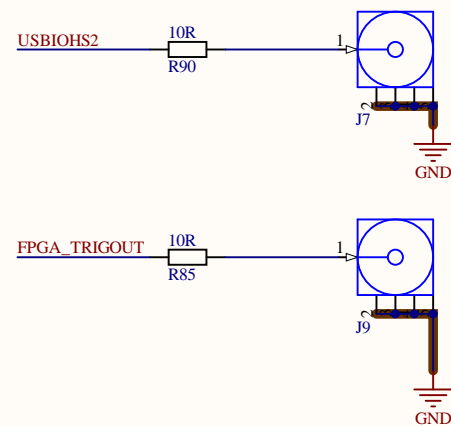
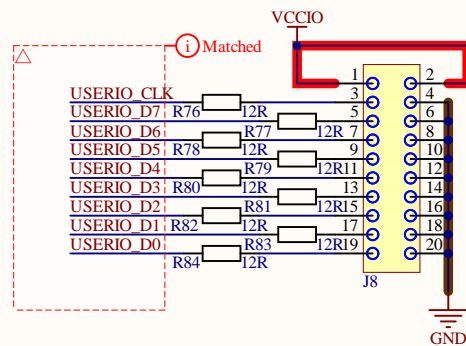
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Route to FPGA pins.
USERIO_CLK must go to
SRCC/MRCC pin, and _P pair.
Rest can go to any pins on same
bank as clock.



Title: **User I/O**

Rev: 03

Project: CW-Husky

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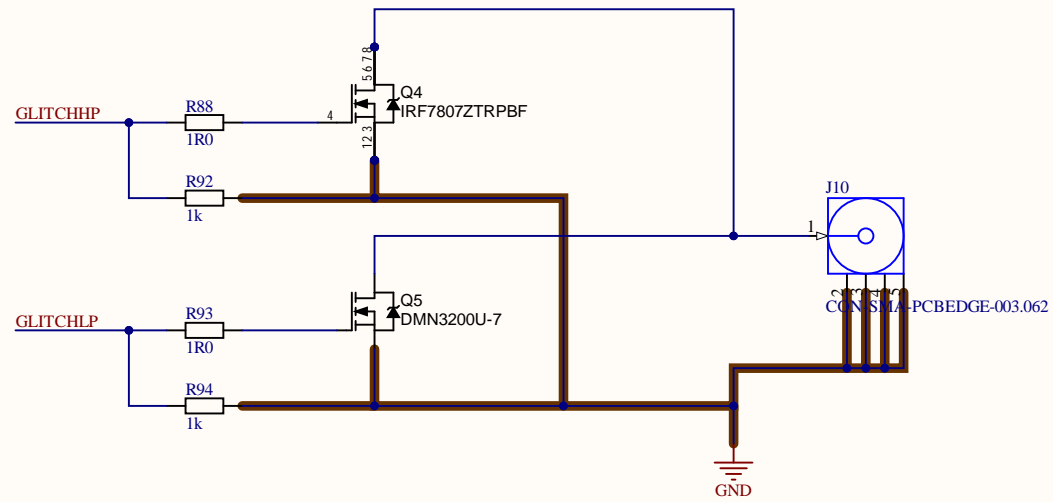
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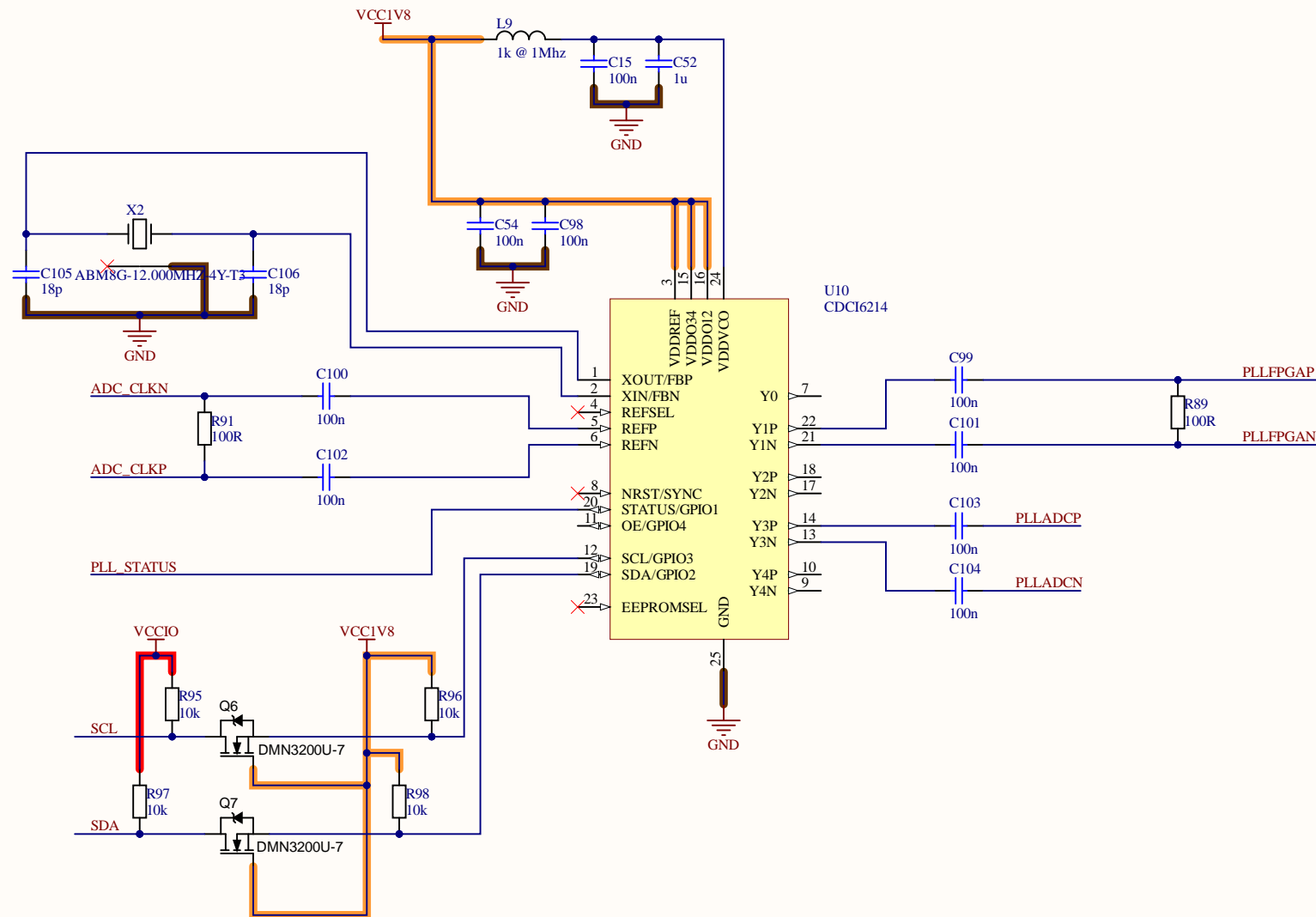
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See
<https://www.nxp.com/docs/en/application-note/AN10441.pdf>
 for level shifting details.

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