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Jaeduk Han (Jae-Duk Han, J. D. Han), Ph.D.

Curriculum Vitae

Research group website: https://niftylab.github.io/, Email: jdhan at hanyang.ac.kr,
Google scholar: https://scholar.google.com/citations?user=l3DrF84AAAAJ&hl=en

Research Interests

Ultra-high-speed (60+Gb/s) SERDES for electrical/optical communication systems for datacenter applications, High-speed TISAR ADCs, analog and mixed-signal (AMS) circuit design automation for advanced VLSI/SOC applications (<16nm FinFET CMOS), Environment-friendly LED lighting systems, Rapid-prototyping hardware for bio-electronic systems.

Education

Ph.D. **University of California at Berkeley**, EECS, Berkeley, CA — Jun. 2012 – Dec. 2017
Thesis: "Design and Automatic Generation of 60Gb/s Wireline Transceivers"
Advisor: Prof. Elad Alon

M.S. **Seoul National University**, EECS, Seoul, Korea — Mar. 2007 – Feb. 2009
Thesis: "Design of a Hybrid Adaptive Decision Feedback Equalizer for High-speed Serial Links"
Advisor: Prof. Deog-Kyoon Jeong

B.S. **Seoul National University**, EECS, Seoul, Korea — Mar. 2003 – Feb. 2007
Summa cum laude
Thesis: "Behavioral Simulation of All-Digital Phase Locked Loop"

Academic Experience

Assistant Professor — Sep. 2019 – present
The Nifty Chips Laboratory, Electronic Engineering Department, Hanyang University
- LAYGO2 (https://github.com/niftylab/laygo2): An improved version of LAYGO for custom IC layout generations
- Analog Circuit Design (English), VLSI Engineering

Graduate Student Researcher — Jun. 2012 – Oct. 2017
Energy Efficient Integrated System Lab, Berkeley Wireless Research Center (BWRC), UC Berkeley
- 60Gb/s serial link transceiver with new equalization and CDR schemes (BAG for DFE generation)
- High-speed time interleaved SAR-ADC with digital calibrations (BAG + CHISEL)
- Automatic generation of integrated circuits for advanced CMOS technology
- LAYGO (http://ucb-art.github.io/laygo): A BAG2 (http://github.com/ucb-art/BAG_framework) add-on for template and grid based IC layout generations
- Converter-free, flicker-less LED driver design
- Rapid-prototyping hardware for bio-electronic systems

Research Assistant — Mar. 2007 – Feb. 2009
Integrated Systems Design Laboratory, Seoul National University

Graduate Student Instructor — 2015 – 2016
EECS Department, UC Berkeley
- EE16A Designing Information Devices and Systems I, EE16B Designing Information Devices and Systems II

Reader — 2013
EECS Department, UC Berkeley
- EE105 Microelectronic Devices and Circuits

Teaching Assistant — 2007 – 2008
EECS Department, Seoul National University
- 420.301A Electronic Circuits I, 420.207A Electronic Circuits II, and 420.424A Digital Integrated Circuits

Industry Experience

VPP Consulting Professor Jan. 2020 – present
SK Hynix
SEG Analog/Mixed-Signal Circuits Designer Aug. 2017 – Aug. 2019
Apple Inc., Silicon Engineering Group, Cupertino, CA
SEG Intern May. 2016 – Aug. 2016
Apple Inc., Silicon Engineering Group, Cupertino, CA
Analog/Mixed-Signal Design Intern May. 2015 – Dec. 2015
Xilinx Inc., Gigabit Transceiver Group, San Jose, CA
Graduate Intern Technical Jun. 2014 – Sep. 2014
Intel Corporation, Signaling Research Laboratory, Intel Labs, Hillsboro, OR
Research Intern Jun. 2012
Altera Inc., IP Development Group, San Jose, CA
Engineer Mar. 2009 – Mar. 2012
TLI Inc., Analog IC Design Group, Seongnam, Korea

Publications

Peer-reviewed Journal Articles

9. (submitted) Jaeduk Han, Woorham Bae, Eric Y. Chang, Zhongkai Wang, Borivoje Nikolić, and Elad Alon, "LAYGO: A Layout Generation Framework to Enhance Design Productivity in Advanced CMOS Technologies."

8. [JSSC'19] Stevo Bailey, Paul Rigge, Jaeduk Han, Richard Lin, Eric Chang, Howard Mao, Zhongkai Wang, Chick Markley, Adam Izraelevitz, Angie Wang, Nathan Narevsky, Woorham Bae, Steve Shauck, Sergio Montano, Justin Norsworthy, Munir Razzaque, Wen Hau Ma, Akalu Lentiro, Matthew Doerflein, Darin Heckendorn, Jim McGrath, Franco DeSeta, Ronen Shoham, Mike Stellfox, Mark Snowden, Joseph Cole, Dan Fuhrman, Brian Richards, Jonathan Bachrach, Elad Alon, and Borivoje Nikolic´, "A Mixed-Signal RISC-V Signal Analysis SoC Generator with a 16nm FinFET Instance," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2018 IEEE Asian Solid-State Circuits Conference (ASSCC 2018), Jul. 2019.

7. [JSSC'19] Angie Wang, Woorham Bae, Jaeduk Han, Stevo Bailey, Paul Rigge, Orhan Ocal, Zhongkai Wang, Kannan Ramchandran, Elad Alon, Borivoje Nikolić, "A Real-Time, 1.89-GHz Bandwidth, 175-kHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2018 IEEE European Solid-State Circuits Conference (ESSCIRC 2018), vol.54, no.7, pp.1993-2008, Jun. 2019.

6. [SSCL'18] Eric Chang, Nathan Narevsky, Jaeduk Han, Elad Alon, "An Automated SerDes Frontend Generator Verified with a 16nm Instance Achieving 15 Gb/s at 1.96 pJ/bit," *IEEE Solid-State Circuits Letters*, Special Issue on the 2018 Symposium on VLSI Circuits (VLSIC 2018) , vol.1, no.12, pp.245-248, Dec. 2018.

5. [TIE'18] Woorham Bae, Haram Ju, Kwangseo Park, Jaeduk Han, Deog-Kyoon Jeong, "A Supply-Scalable Serializing Transmitter with Controllable Output Swing and Equalization for Next Generation Standards," *IEEE Transactions on Industrial Electronics*, vol.65, no.7, pp.5979-5989, Jul. 2018.

4. [JSSC'17] Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, "Design Techniques for a 60-Gb/s 288-mW NRZ Transceiver With Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65-nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2017 International Solid State Circuits Conference (ISSCC 2017), vol.52, no.12, pp.3474-3485, Dec. 2017.

3. [JSSC'17] J. Im, D. Freitas, A. Roldan, R. Casey, S. Chen, A. Chou, T. Cronin, K. Geary, S. McLeod, L. Zhou, I. Zhuang, J. Han, S. Lin, P. Upadhyaya, G. Zhang, Y. Frans, K. Chang, "A 40-to-56 Gb/s PAM-4 Receiver with Ten-Tap Direct Decision-Feedback Equalization in 16-nm FinFET," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2017 International Solid State Circuits Conference (ISSCC 2017), vol.52, no.12, pp.3486-3502, Dec. 2017.

2. [JSSC'16] Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, "Design Techniques for a 60 Gb/s 173 mW Wireline Receiver Frontend in 65 nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, Special Issue on the 2015 Symposium on VLSI Circuits (VLSIC 2015), vol.51, no.4, pp.871-880, Apr. 2016.

1. [TCPMT'13] W. Y. Shin, G. M. Hong, H. Lee, J. D. Han, K. S. Park, D. H. Lim, S. Kim, D. Shim, J. H. Chun, D. K. Jeong, S. Kim, "4-Slot, 8-Drop Impedance-Matched Bidirectional Multidrop DQ Bus With a 4.8-Gb/s Memory Controller Transceiver," *IEEE*

Transactions on Components, Packaging and Manufacturing Technology, vol.3, no. 5, pp. 858-869, May. 2013.

Peer-reviewed Conference Papers

16. [ISOCC'19] *(invited)* Jaeduk Han, Eric Chang, Elad Alon, "Design and Automatic Generation of High-Speed Circuits for Wireline Communications," *IEEE 16th International SoC Design Conference*, 8 Oct. 2019.

15. [ESSCIRC'19] Nicholas Sutardja, Jaeduk Han, Nathan Narevsky, Elad Alon, Borivoje Nikolić, "A 2-tap switched capacitor FFE transmitter achieving 1-20 Gb/s at 0.72-0.62 pJ/bit," *IEEE European Solid-State Circuits Conference*, Sep. 2019.

14. [CICC'19] Jaeduk Han, Eric Chang, Stevo Bailey, Zhongkai Wang, Woorham Bae, Angie Wang, Nathan Narevsky, Amy Whitcombe, Pengpeng Lu, Borivoje Nikolic, Elad Alon, "A Generated 7GS/s 8b Time-Interleaved SAR ADC with 38.2dB SNDR at Nyquist in 16nm CMOS FinFET," *IEEE Custom Integrated Circuits Conference*, 17 Apr. 2019.

13. [ASSCC'18] Stevo Bailey, Jaeduk Han, Paul Rigge, Richard Lin, Eric Chang, Howard Mao, Zhongkai Wang, Chick Markley, Adam Izraelevitz, Angie Wang, Nathan Narevsky, Woorham Bae, Steve Shauck, Sergio Montano, Justin Norsworthy, Munir Razzaque, Wen Hau Ma, Akalu Lentiro, Matthew Doerflein, Darin Heckendorn, Jim McGrath, Franco DeSeta, Ronen Shoham, Mike Stellfox, Mark Snowden, Joseph Cole, Dan Fuhrman, Brian Richards, Jonathan Bachrach, Elad Alon, and Borivoje Nikolic´, "A Generated Multirate Signal Analysis RISC-V SoC in 16nm FinFET," *IEEE Asian Solid-State Circuits Conference*, Nov 2018.

12. [ECCE'18] Yongjun Li, Jaeduk Han, Seth. A. Sanders, "A Low-Cost AC Direct LED Driver with Reduced Flicker using Triac," *IEEE Energy Conversion Congress and Exposition*, Sep. 2018.

11. [ESSCIRC'18] Angie Wang, Woorham Bae, Jaeduk Han, Stevo Bailey, Paul Rigge, Orhan Ocal, Zhongkai Wang, Kannan Ramchandran, Elad Alon, Borivoje Nikolić, "A Real-Time, Analog/Digital Co-Designed 1.89-GHz Bandwidth, 175-KHz Resolution Sparse Spectral Analysis RISC-V SoC in 16-nm FinFET," *IEEE European Solid-State Circuits Conference*, Sep. 2018.

10. [VLSI'18] Eric Chang, Nathan Narevsky, Jaeduk Han, Elad Alon, "An Automated SerDes Frontend Generator Verified with a 16nm Instance Achieving 15 Gb/s at 1.96 pJ/bit," *IEEE International Symposium on VLSI Circuits*, Jun. 2018.

9. [CICC'18] *(invited)* Eric Chang, Jaeduk Han, Woorham Bae, Zhongkai Wang, Nathan Narevsky, Guanghua Shu, Frankie Liu, Borivoje Nikolić, Elad Alon, "BAG2: A Process-Portable Framework for Generator-Based AMS Circuit Design," *IEEE Custom Integrated Circuits Conference*, 10 Apr. 2018.

8. [ASSCC'17] Angie Wang, Brian Richards, Palmer Dabbelt, Howard Mao, Stevo Bailey, Jaeduk Han, Eric Chang, James Dunn, Elad Alon, Borivoje Nikolić, "A 0.37mm^2 LTE/Wi-Fi Compatible, Memory-Based, Runtime-Reconfigurable $2^n3^m5^k$ FFT Accelerator for RISC-V Rocket Core in 16nm FinFET," *IEEE Asian Solid-State Circuits Conference*, 8 Nov. 2017.

7. [ISSCC'17] Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, "A 60Gb/s 288mW NRZ Transceiver with Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65nm CMOS Technology," *IEEE International Solid-State Circuits Conference*, 5-9 Feb. 2017.

6. [ISSCC'17] J. Im, D. Freitas, A. Roldan, R. Casey, S. Chen, A. Chou, T. Cronin, K. Geary, S. McLeod, L. Zhou, I. Zhuang, J. Han, S. Lin, P. Upadhyaya, G. Zhang, Y. Frans, K. Chang, "A 40-to-56Gb/s PAM-4 Receiver with 10-Tap Direct Decision-Feedback Equalization in 16nm FinFET," *IEEE International Solid-State Circuits Conference*, 5-9 Feb. 2017.

5. [VLSI'15] Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, "A 60Gb/s 173mW Receiver Frontend in 65nm CMOS technology," *IEEE International Symposium on VLSI Circuits*, pp. C230-C231, 17-19 Jun. 2015.

4. [ISSCC'11] Woo-Yeol Shin, Gi-Moon Hong, Hyongmin Lee, Jae-Duk Han, Sunkwon Kim, Kyu-Sang Park, Dong-Hyuk Lim, Jung-Hoon Chun, Deog-Kyoon Jeong, Suhwan Kim, "A 4.8Gb/s impedance-matched bidirectional multi-drop transceiver for high-capacity memory interface," *IEEE International Solid-State Circuits Conference*, pp.494-496, 20-24 Feb. 2011.

3. [ASSCC'10] J. D. Han, W-Y. Shin, W-S. Choi, J-H. Chun, S. Kim, D-K. Jeong, "A 5-Gb/s digitally controlled 3-tap DFE receiver for serial communications," *IEEE Asian Solid-State Circuits Conference*, pp.1-4, 8-10 Nov. 2010.

2. [KCS'11] J. D. Han, B. T. Jang, J. S. Yoon, S. H. Ahn, B. H. Lee, J. H. Lee, S. W. Hong, "A 2.7-Gb/s digitally controlled decision feedback equalizer for display interfaces", *The 18th Korean Conference on Semiconductors, 2011 IEEK*, 16-18 Feb. 2011.

1. [IEEK'08] J. D. Han, B. J. Yoo, D. H. Lim, K. S. Park, D. K. Jeong, "A 5-Gb/s digitalized DFE receiver for high-speed communication through backplane channels", *Fall Conference, 2008 IEEK*, pp.457-457, 28-29 Nov. 2008.

Patents (The United States of America, Republic of Korea)

14. J. Han, "Current-mode logic circuits", *filed*, KR10-2020-0025372.

13. An undisclosed patent application, Application No. US16528518.

12. J. Han, J. Im, "Low-Power Decision Threshold Control for High-Speed Signaling", US10193540.

11. J. Seo, H. Kim, H. Ju, H. Kim, J. D. Han, D. K. Jeong, “LED Lighting System and AC-DC Converting Circuit used thereto”, KR101340297.
10. J. D. Han, H. C. Kim, D. K. Jeong, “Voltage supporting type LED lighting system”, KR101371247.
9. J. D. Han, B. T. Jang, “LED Lighting System for decreasing the variation in current to that in temperature”, KR101340295.
8. J. D. Han, K. R. Ahn, “Voltage detection LED lighting system”, KR101348966.
7. J. D. Han, K. R. Ahn, “LED lighting system having common current source”, KR101326479.
6. J. D. Han, K. R. Ahn, “LED lighting system for improving lighting amount and operating characteristics”, KR101321343.
5. J. D. Han, K. R. Ahn, “LED lighting system for improving lighting amount and reducing layout area”, KR101307789.
4. J. D. Han, “LED illuminating apparatus having enhanced quantity of light”, US9101016, PCT/KR2013/000523.
3. J. D. Han, “LED lighting system for improving voltage current non-harmony”, KR101359890.
2. J. D. Han, J. W. Lee, “Current detection LED lighting system”, KR101285644.
1. B. T. Jang, J. D. Han, "LED lighting system for improving modulation index", KR101189102.

Miscellaneous

2. "Electronic Circuits II Lab Manual", EECS Department, Seoul National University, 2008.
1. "White Paper: Student Association Election Commission", SNU Student Association Election Commission, 2003.

Selected Awards and Honors

Outstanding Course Development and Teaching Award, EECS Department, UC Berkeley	2016
Finalists, Qualcomm Innovation Fellowship, Qualcomm	2016
KFAS Fellowship, Doctoral Study Abroad Program, Korea Foundation for Advanced Studies	2012 – 2017
Outstanding Employee Award, TLI Inc.,	2010
Best Tutor Award, for Outstanding Teaching Assistants, EECS Department, Seoul National University	2008
KFAS Fellowship, Graduate Students Program, Korea Foundation for Advanced Studies	2007 – 2009
National Scholarship for Science and Engineering, Korea Student Aid Foundation	2003 – 2006
Grand Prize, *1st place*, The 12th SK Students Competition, Science Track, SK Cooperation and *The Korea Times*	2002

Academic Funding, Fellowship and Grant Activities

Design Techniques for New Memory Systems, SK Hynix	2019
New Faculty Research Grant, Hanyang University	2019
KFAS Dissertation Fellowship, Korea Foundation for Advanced Studies	2017
Summer Department Award, EECS Department, UC Berkeley	2017
KFAS Fellowship, Doctoral Study Abroad Program, Korea Foundation for Advanced Studies	2012 – 2017
Department Award for Outstanding Course Development and Teaching Award**,** EECS Department, UC Berkeley	2016
Graduate Scholarship, EECS Department, UC Berkeley	2016
Graduate Fellowship, EECS Department, UC Berkeley	2016
KFAS Fellowship, Graduate Students Program, Korea Foundation for Advanced Studies	2017
Study Abroad Grant, Seoul National University	2005

Professional and Extracurricular Activities

9. Reviewer of *Scientific Reports*, 2019-present.
8. BAG & Chisel Pilot Bootcamp Staff, BWRC, Aug 2017.
7. Editorial Review Board, *IEEE Solid-State Circuits Letters*, 2018-present.
6. Reviewer of *IEEE Journal of Solid-State Circuits (JSSC)*, 2016-present.
5. Reviewer of *IEEE Transactions on Very Large-Scale Integration Systems (TVLSI)*, 2017-present.
4. Reviewer of *IEEE Transactions on Circuit and Systems II: Express Briefs (TCAS-II)*, 2017-present.
3. Reviewer of *IEEE Transactions on Circuit and Systems I: Regular Papers (TCAS-I)*, 2016-present.
2. Student Organizing Committee of SONIC Student Research E-symposium, SRC and DARPA, 2014.
1. Member of SNU Student Association Election Commission, Seoul National University, 2003.

Presentations and Invited Talks

37. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog and Mixed-Signal Circuits”, Invited talk at Korea Electronics Technology Institute (KETI), November 2019.
36. Jaeduk Han, “Design and Automatic Generation of 60Gb/s High-Speed Serial Links”, Invited talk at Samsung Semiconductor, November 2019.
35. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog and Mixed-Signal Circuits”, Invited talk at SK Hynix Semiconductor, October 2019.
34. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog and Mixed-Signal Circuits”, The 2nd Industry-Research-Academia Workshop, October 2019.
33. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog-to-Digital Converters”, The 19th RF/Analog Circuit Workshop, September 2019.
32. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog and Mixed-Signal Circuits”, Invited talk at Korea Advanced Institute of Science Technology (KAIST).
31. Jaeduk Han, “Design and Automatic Generation of High-Speed Analog and Mixed-Signal Circuits”, Invited talk at National Chaio Tung University (NCTU).
30. Jaeduk Han, “Tutorial – LAYout with Gridded Objects (LAYGO)”, BAG Bootcamp at Cadence.
29. Jaeduk Han, “Tutorial – LAYout with Gridded Objects (LAYGO)”, BAG Pilot Bootcamp at Berkeley Wireless Research Center.
28. Eric Chang and Jaeduk Han, “Getting Started with BAG”, Invited talk at Xilinx, June 2017.
27. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at Credo Semiconductor, May 2017.
26. Jaeduk Han, “Research Summary - High Speed Serial Links”, BWRC Summer 2017 Retreat, May 2017.
25. Jaeduk Han, Elad Alon, “ADC Generation in 16nm CMOS Technology”, BWRC Summer 2017 Retreat, May 2017.
24. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at Seoul National University, January 2017.
23. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at DGIST, January 2017.
22. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver in 65nm CMOS Technology”, Invited talk at Sungkyunkwan University, December 2016.
21. Jaeduk Han, Elad Alon, “ADC Generation in 16nm CMOS Technology”, BWRC Fall 2016 Retreat, November 2016.
20. Jaeduk Han, Elad Alon, “AMS Design in Advanced CMOS Process”, SONIC Annual Meeting, October 2016.
19. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver”, Invited talk at Oracle, September 2016.
18. Jaeduk Han, “Design and Automatic Generation of 60Gb/s Transceiver”, Invited talk at Apple, August 2016.
17. Jaeduk Han, Elad Alon, “60Gb/s Wireline Connectivity”, BWRC Summer 2016 Retreat, May 2016.
16. Nicholas Sutardja, Jaeduk Han, “Low Latency, High Bandwidth Burst Mode Interconnect Design for Next Generation Computing Systems”, Qualcomm Innovation Fellowship Finalist Presentations, March 2016.
15. Jaeduk Han, “Design and Automatic Generation of Mixed-signal Integrated Circuits”, Invited talk at SK Hynix Semiconductor, January 2016.
14. Jaeduk Han, Elad Alon, “Pushing the limits of Electrical Signaling”, BWRC Fall 2015 Retreat, November 2015.
13. J. Han, E. Alon, “Design of a 60+Gb/s Transceiver for Wireline Communication Systems”, SONIC Annual Meeting, Sep. 2015.
12. Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, “Wireline Transceiver for 60Gb/s Signaling and Beyond”, Berkeley EECS Annual Research Symposium (BEARS), February 2015.
11. Jaeduk Han, Yue Lu, Nicholas Sutardja, Kwangmo Jung, Elad Alon, “Wireline Transceiver for 60Gb/s Signaling and Beyond”, BWRC Winter 2015 Retreat, January 2015.
10. Jaeduk Han, Elad Alon, “Signaling Path Design for 64Gb/s Receiver”, BWRC Winter 2015 Retreat, May 2014.
9. Jaeduk Han, Elad Alon, “An Automatically Generated 64-Gb/s Current Integrating Decision Feedback Equalizer”, SONIC Student Research e-symposium 2014, March 2014.
8. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Marvell Technology Group Ltd., March 2014.

7. Jaeduk Han, Y. Lu, N. Sutardja, E. Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Apple, Feb. 2014.
6. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “An Automated Design Methodology for High-Speed DFEs”, BWRC Winter 2014 Retreat, January 2014.
5. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design and Automatic Generation of 64Gb/s Equalizers”, Invited talk at Xilinx Inc., October 2013.
4. Jaeduk Han, Yue Lu, Kwangmo Jung, Elad Alon, “An Automated Design Methodology for High-Speed DFEs”, SONIC Annual Meeting, October 2013.
3. Jaeduk Han, Yue Lu, Nicholas Sutardja, Elad Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, BWRC Summer 2013 Retreat, May 2013.
2. Jaeduk Han, Yue Lu, Elad Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, Berkeley EECS Annual Research Symposium (BEARS), February 2013.
1. Jaeduk Han, Y. Lu, E. Alon, “Design Methodology for a 64-Gb/s DFE Receiver”, BWRC Winter 2013 Retreat, Jan. 2013.