Raghavendra Kumar Sakali

PROFESSIONAL SUMMARY

Assistant Professor with four years of experience successfully contributing to academic curriculum development and delivery. Driven to contribute to program outcomes by facilitating engagement and supporting learning objectives. Enthusiastic professional with background in academic advisement.

WORK HISTORY

Assistant Professor | Sri Sivasubramiya Nadar College of Engineering, Chennai, Tamilnadu – 30th August 2023- present

- Revised course objectives, course materials, instructional and assessment strategies for Data Structures, Internet Programming, Python Programming, Digital Systems, and Computer Organization & Architecture courses.

Assistant Professor | SVR Engineering College, JNTUA Nandyal, Andhra Pradesh - July 2019 - December 2020

- Revised course objectives, course materials, instructional and assessment strategies for C language and Data Structures courses.

Assistant Professor | BIT Institute of Technology, JNTUA Hindupur, Andhra Pradesh - July 2018 - July 2019

- Revised course objectives, course materials, instructional and assessment strategies for Software Architecture and Design Patterns courses.

EDUCATION

- Ph.D., CSE, (01/2021 – 06/2024), CGPA-9.28
  IIITDM Kancheepuram, Chennai.
- Master of Technology, CSE, 10/2018, CGPA-7.7
  JNTU College of Engineering, Anantapuram.
- Bachelor of Technology, CSIT, 06/2013, CGPA-7.1
  G. Pullaiah College of Engineering & Technology, Kurnool.

RESEARCH PUBLICATIONS

International Journals – 4 (SCIE and Scopus Indexed)

- Raghavendra Kumar Sakali, P. Balasubramanian, Ramesh Reddy, Sreehari Veeramachaneni, and Noor Mahammad Sk. "Optimized Fault-Tolerant Adder Design Using Error Analysis." Journal of Circuits, Systems and Computers (2022): 2350091, Vol. 32, No. 06. (Q3, SCIE & Scopus)
  DOI: https://doi.org/10.1142/S0218126623500913

- Sakali Raghavendra Kumar, and Noor Mahammad Shak. "Intrinsic Based Self-Healing Adder Design Using Chromosome Reconstruction Algorithm." Journal of Electronic Testing 39, no. 1 (2023): 111-122. (Q3, SCIE & Scopus)
  DOI: https://link.springer.com/article/10.1007/s10836-023-06050-1

- Raghavendra Kumar Sakali, Sreehari Veeramachaneni, Noor Mahammad SK. "Preferential Fault-Tolerance Multiplier Design to Mitigate Soft Errors in FPGAs" was published in the Journal of VLSI Integration- Elsevier, Volume 93, Article No. 102068, Year 2023. (Q3, SCIE & Scopus)
  DOI: https://doi.org/10.1016/j.vlsi.2023.102068

- Raghavendra Kumar Sakali, Noor Mahammad Sk, "Fault-tolerant multiplier using self-healing technique", Microelectronics Reliability, 160, 2024 and page no. 115458 (Q2, SCIE & Scopus)
  DOI: https://doi.org/10.1016/j.microrel.2024.115458

International Conference – 3 (Scopus Indexed)

- Sakali Raghavendra Kumar, Noor Mahammad Sk, Balasubramanian P, G. Venkat Reddy. "Novel Embryonic Adder Architecture with Uni-Cellular Self Check Unit" is proceedings in 2nd International Conference on Emerging Trends in Engineering 2023, Atlantis Press. (Scopus)
  DOI: https://doi.org/10.2991/978-94-6463-252-1_93

- Sakali Raghavendra Kumar, Sreehari Veeramachaneni, Sk Noor Mahammad, Fault-Tolerant Floating-Point Multiplier Design for Mission Critical Systems,

CONTACT

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9490064573.
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JOB SKILLS

- Student needs assessment
- Classroom presentations
- Class instruction
- Student records management
- Academic research
- Online learning tools
- Student counseling
- Lesson Plan
- Course Co-ordinator

TECHNICAL SKILLS

- Operating System: Windows, Linux.
- Tool: MS Office, Xilinx Vivado, Latex, Dia, Logisim
- Programming Languages: C, Python.
- HDL: Verilog
- Web Development: HTML, Java Script, CSS.
- Database: MySQL

CERTIFICATIONS

- NPTEL Certification in CLOUD COMPUTING with 76% score (Elite & Sliver).
- Hacker Rank certification in C (Basic) Skill Test.

REFERENCES

- Dr. Noor Mahammad Sk
  Associate Professor
  HPRCSE Lab, PEMS Block, IIITDM Kancheepuram, Chennai-600127
  Email: noor@iiitdm.ac.in
  Contact: 9176010587

- Prof. Masilamani V
  Professor
  Room: 108-B, Annexure Building,
  IIITDM Kancheepuram, Chennai-600127
  Email: masila@iiitdm.ac.in

2024 37th International Conference on VLSI Design and 2024 23rd International Conference on Embedded Systems (VLSID), January and 2024, Kolkata, India (Scopus)
DOI: https://doi.org/10.1109/VLSID60093.2024.00120

- S. Deepanjali, Noor Mahammad Sk and Sakali Raghavendra Kumar, Fault Resilient Micro-Coded Control Unit for Space-Based Digital Systems,"*2024 28th International Symposium on VLSI Design and Test (VDAT)*, Vellore, India, 2024, pp. 1-6. (Scopus)
DOI: https://doi.org/10.1109/VDAT63601.2024.10705726

- S. Raghavendra Kumar and Sk. Noor Mahammad, *"Preferential Fault-Tolerant Based TF32 Floating Point Adder for Mission Critical Systems,"* in December 2024 *the 33rd IEEE Asian Test Symposium (ATS 2024), Ahmedabad, India, 2024*. (Scopus Indexed).
DOI: https://doi.org/10.1109/ATS64447.2024.10915484

RESEARCH

- ***Area-*** Computer Architecture, System Design, and FPGA.
- ***Topic-*** Fault-Tolerant Adder and Multipliers.
- ***Title- Fault-Tolerant Adder and Multiplier Designs for Mission Critical Systems***

ACCOLADES

- ***Project Staff*** - ***DRDO funded project for tenure of 2 years and joined Ph.D. under project category.***
- ***Teaching Assistance*** - two semesters in my Ph.D.'s Program from 2022-2023, *Courses: High Performance Computing and Device Drivers.*

Contact: 044-27476346

ACTIVITIES

- Organized a guest lecture on a guest lecture titled "Parallel Processors and Its Challenges" delivered by "Dr. Noor Mahammad SK, Associate Professor, Indian Institute of Information Technology, Design and Manufacturing (IIITDM), Kancheepuram" for II-year CSE students.
- Conducted a one-day workshop on open-source resourcing tools for B.E CSE First Year Students.

FUTURE RESEARCH

In my future research, I aim to advance the design of approximate datapath units for machine learning and deep learning accelerators, building upon my Ph.D. work on reliable adder and multiplier design. My focus is to develop energy-efficient, high-performance hardware architectures tailored for image and video processing applications. Traditional processors such as CPUs and GPUs, while powerful, often face limitations in such tasks due to their general-purpose nature, higher power consumption, and limited real-time adaptability. These drawbacks hinder efficiency when dealing with the computational intensity and low-latency demands of modern vision applications.

To address this, my research will explore FPGA-based hardware accelerators, which offer significant advantages such as reconfigurability, parallelism, and customization. Unlike fixed-architecture CPUs/GPUs, FPGAs enable the design of application-specific architectures that can be dynamically adapted to different processing needs and data characteristics, providing a better trade-off between accuracy, speed, and power. This adaptability is especially valuable for edge computing environments where resources are constrained.

Through this research, I plan to bridge the gap between hardware efficiency and algorithmic complexity, ultimately contributing to the development of scalable, low-power accelerators that meet the evolving demands of real-time AI-driven vision systems.