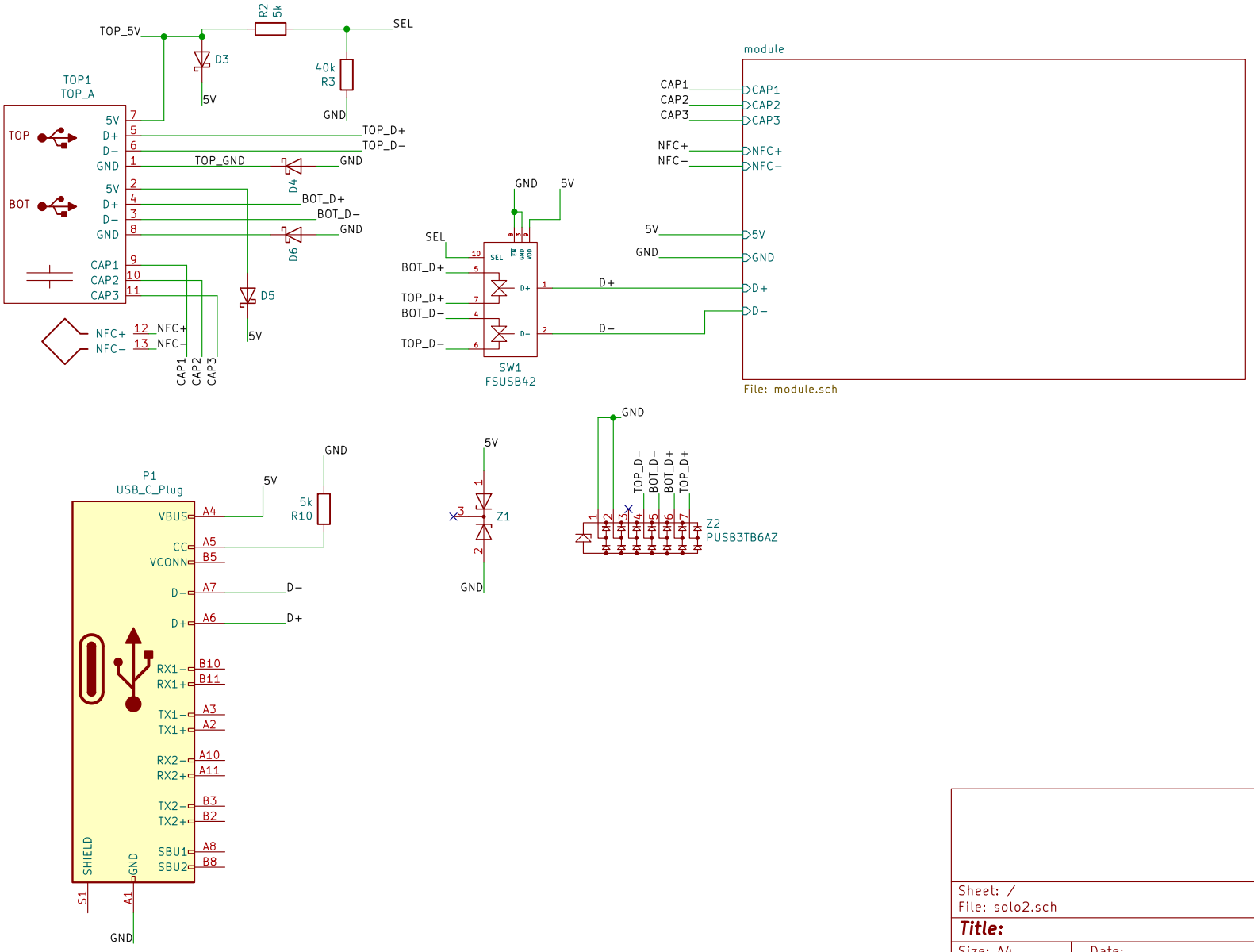
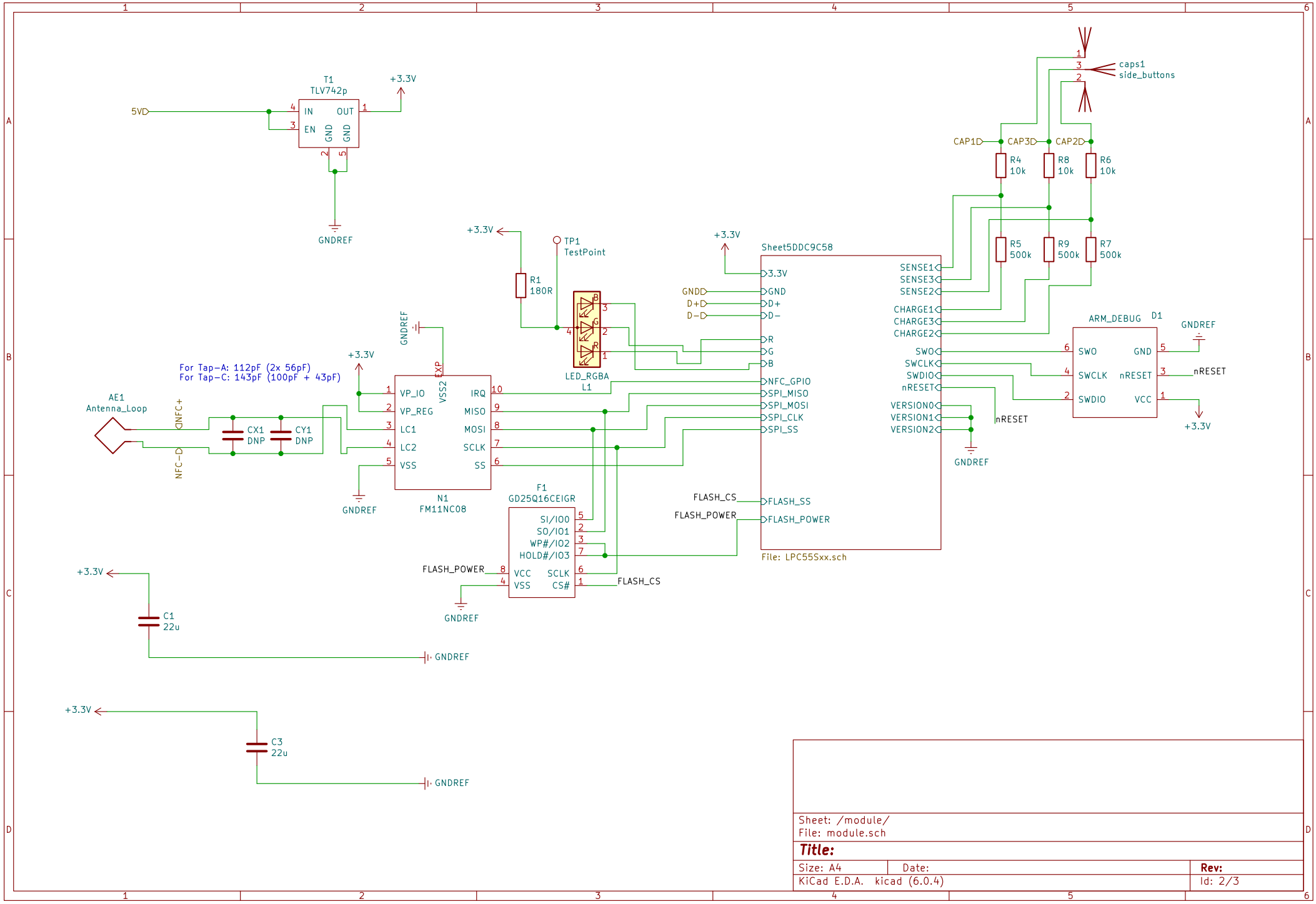
Reversible USB-A.
When S2 is plugged, SEL=5V/1 and D2 pair are selected.
Default to S1.



Sheet: /
File: solo2.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.4)		Id: 1/3



Sheet: /module/
File: module.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (6.0.4)		Id: 2/3

LPC55Sxx chip

U1A
LPC55S69JEV98K

Pin	Signal	Net
L1	PIO0_31/ADC0_3/1FC0_CTS_SDA_SSEL0/SD0_D[2]/CTIMER0_MAT1/SCT0_OUT3/SEC_PIO0_31	SENSE1 ADC channel 3
E5	PIO0_30/FC0_TXD_SCL_MISO_WS/SD1_D[3]/CTIMER0_MAT0/SCT0_OUT9/SEC_PIO0_30	
H8	PIO0_29/FC0_RXD_SDA_MOSI_DATA/SD1_D[2]/CTIMER2_MAT3/SCT0_OUT8/CMP0_OUT/PLU_OUT2/SEC_PIO0_29	
F13	PIO0_28/WAKEUP/FC0_SCK/SD1_CMD/CTIMER_INP11/SCT0_OUT7/USB0_OVERCURRENTN/PLU_OUT1/EC_PIO0_28	SPI_CLK
N2	PIO0_27/FC2_TXD_SCL_MISO_WS/CTIMER3_MAT2/SCT0_OUT6/FC7_RXD_SDA_MOSI_DATA/PLU_OUT0/SEC_PIO0_27	
H12	PIO0_26/FC2_RXD_SDA_MOSI_DATA/CLKOUT/CTIMER_INP14/SCT0_OUT5/USB0_IDVALUE/FC0_SCK/HS_SPI_MOSI/SEC_PIO0_26	
A11	PIO0_25/FC0_TXD_SCL_MISO_WS/SD0_D[1]/CTIMER_INP9/SCT0_GPI1/SEC_PIO0_25	SPI_MISO
E12	PIO0_24FC0_RXD_SDA_MOSI_DATA/SD0_D[0]/CTIMER_INP8/SCT0_GPI0/SEC_PIO0_24	SPI_MOSI
J1	PIO0_23/ADC0_0/MCLK/CTIMER1_MAT2/CTIMER3_MAT3/FC0_CTS_SDA_SSEL0/SD1_D[1]/SEC_PIO0_23	SENSE2 ADC channel 0
E9	PIO0_22/FC6_TXD_SCL_MISO_WS/UTICK_CAP1/CTIMER_INP15/SCT0_OUT3/USB0_VBUS/SD1_D[0]/PLU_OUT7/SEC_PIO0_22	
A12	PIO0_21/FC3_RTS_SCL_SSEL1/UTICK_CAP3/CTIMER3_MAT3/SCT0_GPI3/FC7_SCK/PLU_CLKIN/SEC_PIO0_21	FLASH_POWER
B12	PIO0_20/FC3_CTS_SDA_SSEL0/CTIMER1_MAT1/CTIMER_INP15/SCT0_GPI2/FC7_RXD_SDA_MOSI_DATA/HS_SPI_SSEL0/PLU_INPUT5/SEC_PIO0_20/FC4_TXD_SCL_MISO_WS	GNDREF routing
E6	PIO0_19/FC4_RTS_SCL_SSEL1/UTICK_CAP0/CTIMER0_MAT2/SCT0_OUT2/FC7_TXD_SCL_MISO_WS/PLU_INPUT4/SEC_PIO0_19	NFC_GPIO
H9	PIO0_18/ACMP0_C/FC4_CTS_SDA_SSEL0/SD0_WR_PRT/CTIMER1_MAT0/SCT0_OUT1/PLU_INPUT3/SEC_PIO0_18	
G3	PIO0_17/FC4_SSEL2/SD0_CARD_DET_N/SCT0_GPI7/SCT0_OUT0/SD0_CARD_INT_N/PLU_INPUT2/SEC_PIO0_17	
J2	PIO0_16/ADC0_8/FC4_TXD_SCL_MISO_WS/CLKOUT/CTIMER_INP4/EC_PIO0_16	
L2	PIO0_15/ADC0_2/FC6_CTS_SDA_SSEL0/UTICK_CAP2/CTIMER_INP16/SCT0_OUT2/SD0_WR_PRT/SEC_PIO0_15	SENSE3 ADC channel 2
C13	PIO0_14/FC1_RTS_SCL_SSEL1/UTICK_CAP1/CTIMER_INP1/SCT0_GPI1/FC1_TXD_SCL_MISO_WS/PLU_INPUT1/SEC_PIO0_14	
C12	PIO0_13/FC1_CTS_SDA_SSEL0/UTICK_CAP0/CTIMER_INP0/SCT0_GPI0/FC1_RXD_SDA_MOSI_DATA/PLU_INPUT0/SEC_PIO0_13	FLASH_SS
E2	PIO0_12/ADC0_10/FC3_TXD_SCL_MISO_WS/SD1_BACKEND_PWR/FREQME_GPIO_CLK_B/SCT0_GPI7/SD0_POW_EN/SWDIO/FC6_TXD_SCL_MISO_WS/SEC_PIO0_12	SWDIO
F1	PIO0_11/ADC0_9/FC6_RXD_SDA_MOSI_DATA/CTIMER2_MAT2/FREQME_GPIO_CLK_A/SWCLK/SEC_PIO0_11	SWCLK
F2	PIO0_10/ADC0_1/FC6_SCK/CTIMER_INP10/CTIMER2_MAT0/FC1_TXD_SCL_MISO_WS/SCT0_OUT2/SWO/SEC_PIO0_10	SWO
L13	PIO0_9/ACMP0_B/FC3_SSEL2/SD0_POW_EN/FC5_TXD_SCL_MISO_WS/SEC_PIO0_9	
M2	PIO0_8/FC3_SSEL3/SD0_CMD/FC5_RXD_SDA_MOSI_DATA/SWO/SEC_PIO0_8	
G5	PIO0_7/FC3_RTS_SCL_SSEL1/SD0_CLK/FC5_SCK/FC1_SCK/SEC_PIO0_7	
B7	PIO0_6/TDO/FC3_SCK/CTIMER_INP13/CTIMER4_MAT0/SCT0_GPI6/SEC_PIO0_6	GNDREF routing
A7	PIO0_5/TDI/FC4_RXD_SDA_MOSI_DATA/CTIMER3_MAT0/SCT0_GPI5/FC3_RTS_SCL_SSEL1/MCLK/SEC_PIO0_5	R
E7	PIO0_4/TMS/FC4_SCK/CTIMER_INP12/SCT0_GPI4/FC3_CTS_SDA_SSEL0/SEC_PIO0_4	
F8	PIO0_3/TCK/FC3_RXD_SDA_MOSI_DATA/CTIMER0_MAT1/SCT0_OUT1/SCT0_GPI3/SEC_PIO0_3	
B11	PIO0_2/TRST/FC3_TXD_SCL_MISO_WS/CTIMER_INP1/SCT0_OUT0/SCT0_GPI2/SEC_PIO0_2	GNDREF routing
F5	PIO0_1/FC3_CTS_SDA_SSEL0/CTIMER_INP0/SCT0_GPI1/SD1_CLK/CMP0_OUT/SEC_PIO0_1	
L12	PIO0_0/ACMP0_A/FC3_SCK/CTIMER0_MAT0/SCT0_GPI0/SD1_CARD_INT_N/SEC_PIO0_0	

U1B
LPC55S69JEV98K

Pin	Signal	Net
H6	PIO1_31/MCLK/SD1_CLK/CTIMER0_MAT2/SCT0_OUT6/PLU_INPUT0	
F9	PIO1_30/WAKEUP/FC7_TXD_SCL_MISO_WS/SD0_D[7]/SCT0_GPI7/USB1_OVERCURRENTN/USB1_LEDN/PLU_INPUT1	
G8	PIO1_29/FC7_RXD_SDA_MOSI_DATA/SD0_D[6]/SCT0_GPI6/USB1_PORTPWRN/USB1_FRAME/PLU_INPUT2	
A8	PIO1_28/FC7_SCK/SD0_D[5]/CTIMER_INP2/PLU_INPUT3	
E8	PIO1_27/FC2_RTS_SCL_SSEL1/SD0_D[4]/CTIMER0_MAT3/CLKOUT/PLU_INPUT4	
E13	PIO1_26/FC2_CTS_SDA_SSEL0/SCT0_OUT3/CTIMER_INP3/UTICK_CAP1/HS_SPI_SSEL3/PLU_INPUT5	
B8	PIO1_25/FC2_TXD_SCL_MISO_WS/SCT0_OUT2/SD1_D[0]/UTICK_CAP0/PLU_CLKIN	GNDREF routing
F6	PIO1_24/FC2_RXD_SDA_MOSI_DATA/SCT0_OUT1/SD1_D[1]/FC3_SSEL3/PLU_OUT6	
J8	PIO1_23/FC2_SCK/SCT0_OUT0/SD1_D[3]/FC3_SSEL2/PLU_OUT5	
M8	PIO1_22/SD0_CMD/CTIMER2_MAT3/SCT0_GPI5/FC4_SSEL3/PLU_OUT4	
M7	PIO1_21/FC7_CTS_SDA_SSEL0/CTIMER3_MAT2/FC4_RXD_SDA_MOSI_DATA/PLU_OUT3	G
C2	PIO1_20/FC7_RTS_SCL_SSEL1/CTIMER_INP14/FC4_TXD_SCL_MISO_WS/PLU_OUT2	SPI_SS
H13	PIO1_19/ACMPVREF/SCT0_OUT7/CTIMER3_MAT1/SCT0_GPI7/FC4_SCK/PLU_OUT1	B
G9	PIO1_18/SD1_POW_EN/SCT0_OUT5/PLU_OUT0	
J9	PIO1_17/FC6_RTS_SCL_SSEL1/SCT0_OUT4/SD1_CARD_INT_N/SD1_CARD_DET_N	
C7	PIO1_16/FC6_TXD_SCL_MISO_WS/CTIMER1_MAT3/SD0_CMD	CHARGE1
B6	PIO1_15/UTICK_CAP3/CTIMER_INP7/FC5_RTS_SCL_SSEL1/FC4_RTS_SCL_SSEL1/SD1_D[2]	CHARGE2 GNDREF routing
L7	PIO1_14/ACMP0_D/UTICK_CAP2/CTIMER1_MAT2/FC5_CTS_SDA_SSEL0/USB0_LEDN/SD1_CMD	
B3	PIO1_13/FC6_RXD_SDA_MOSI_DATA/CTIMER_INP6/USB0_OVERCURRENTN/USB0_FRAME/SD0_CARD_DET_N	CHARGE3 GNDREF routing
F12	PIO1_12/FC6_SCK/CTIMER1_MAT1/USB0_PORTPWRN/HS_SPI_SSEL2	
G6	PIO1_11/FC1_TXD_SCL_MISO_WS/CTIMER_INP5/USB0_VBUS	
J7	PIO1_10/FC1_RXD_SDA_MOSI_DATA/CTIMER1_MAT0/SCT0_OUT3	
C1	PIO1_9/ADC0_12/FC1_SCK/CTIMER_INP4/SCT0_OUT2/FC4_CTS_SDA_SSEL0	
A6	PIO1_8/ADC0_4/FC0_CTS_SDA_SSEL0/SD0_CLK/SCT0_OUT1/FC4_SSEL2	
J5	PIO1_7/FC0_RTS_SCL_SSEL1/SD0_D[1]/CTIMER2_MAT2/SCT0_GPI4	
H5	PIO1_6/FC0_TXD_SCL_MISO_WS/SD0_D[3]/CTIMER2_MAT1/SCT0_GPI3	
M5	PIO1_5/FC0_RXD_SDA_MOSI_DATA/SD0_D[2]/CTIMER2_MAT0/SCT0_GPI0	
B2	PIO1_4/FC0_SCK/SD0_D[0]/CTIMER2_MAT1/SCT0_OUT0/FREQME_GPIO_CLK_A	GNDREF routing
G13	PIO1_3/SCT0_OUT4/HS_SPI_MISO/USB0_PORTPWRN/PLU_OUT6	
G12	PIO1_2/CTIMER0_MAT3/SCT0_GPI6/HS_SPI_SCK/USB1_PORTPWRN/PLU_OUT5	
G11	PIO1_1/WAKEUP/FC3_RXD_SDA_MOSI_DATA/CTIMER_INP3/SCT0_GPI5/HS_SPI_SSEL1/USB1_OVERCURRENTN/PLU_OUT4	
E1	PIO1_0/ADC0_11/FC0_RTS_SCL_SSEL1/SD0_D[3]/CTIMER_INP2/SCT0_GPI4/PLU_OUT3	

+3.3V
GNDREF
3.3V
GND
D+
D−
R
G
B
SPI_MOSI
SPI_MISO
SPI_CLK
SPI_SS
NFC_GPIO
FLASH_SS
FLASH_POWER

Support 3 capacitive touch buttons.
Uses RC acquisition principle.
See ST AN2927.

SENSE1
SENSE2
SENSE3
SWDIO
SWCLK
SWO
nRESET
CHARGE1
CHARGE2
CHARGE3
VERSION0
VERSION1
VERSION2

U1C
LPC55S69JEV98K

Pin	Signal	Net
J6	RESETN	nRESET
A3	USB0_3V3	+3.3V
A2	USB0_DP	
A1	USB0_DM	
B1	USB0_VSS	GNDREF
N7	USB1_3V3	+3.3V
N8	USB1_VBUS	
M6	USB1_DP	D+
N6	USB1_DM	D−
N5	USB1_VSS	GNDREF
N3	XTAL32M_P	
M3	XTAL32M_N	
J13	XTAL32K_P	
J12	XTAL32K_N	
N13	VBAT_DCDC	+3.3V
M13	VBAT_PMU	
A13	VDD	
G2	VDDA	
M9	VDD_PMU	
N9	FB	
N11	LX	
H1	VREFN	
G1	VREFP	+3.3V
B6	VSS	
N12	VSS_DCDC	
M11	VSS_PMU	
H2	VSSA	

C14 100nF
C16 47pF
L2 4u7H
C13 10uF
C17 10uF
C15 100nF
C20 8pF
C21 8pF
Y1 XRCGB16M000FXN01R0