82S23
82S123
256-Bit TTL Bipolar PROM

Product Specification

Bipolar Memory Products

DESCRIPTION

The 82S23 and 82S123 are field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The 82S23 and 82S123 devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 1 Chip Enable input for memory expansion. They feature either Open-Collector or 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S23 and 82S123 devices are also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Book.

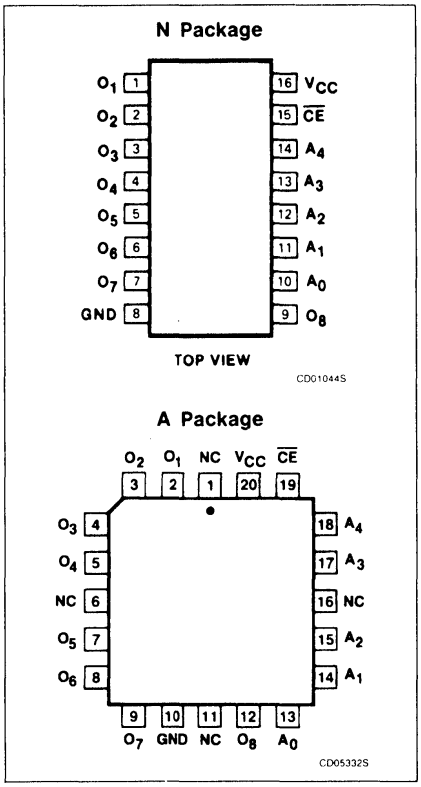
FEATURES

- **Address access time: 50ns max**
- **Power dissipation: 1.3mW/bit typ**
- **Input loading: −100μA max**
- **On-chip address decoding**
- **One Chip Enable input**
- **Output options:**
  - **N82S23: Open-Collector**
  - **N82S123: 3-State**
- **No separate fusing pins**
- **Unprogrammed outputs are Low level**
- **Fully TTL compatible**

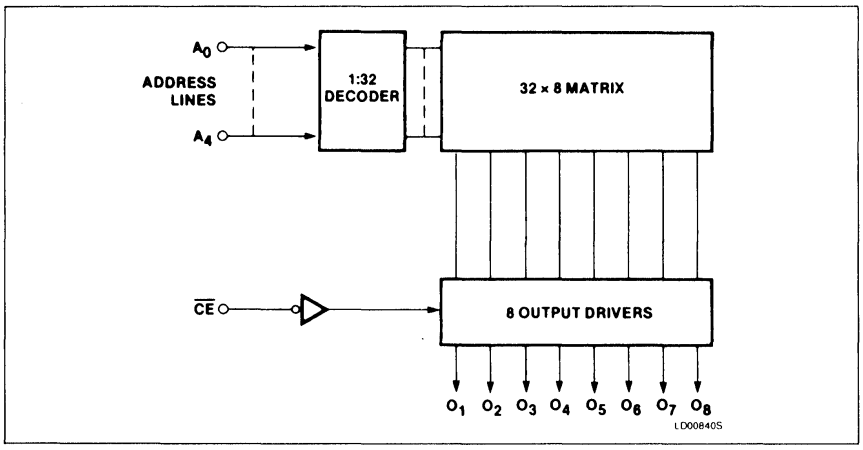
APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Format conversion**
- **Hardwired algorithms**
- **Random logic**
- **Code conversion**

PIN CONFIGURATIONS



BLOCK DIAGRAM



ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16-pin Plastic DIP 300mil-wide	N82S23 N • N82S123 N
20-pin Plastic Leaded Chip Carrier 350mil-square	N82S23 A • N82S123 A

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{DC}
V_{IN}	Input voltage	+5.5	V_{DC}
V_{OH} V_O	Output voltage High (82S23) Off-State (82S123)	+5.5	V_{DC}
T_A	Operating temperature range	0 to +75	°C
T_{STG}	Storage temperature range	−65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS[1,2]	LIMITS			UNIT
			Min	Typ[5]	Max	
Input voltage						
V_{IL}	Low	V_{CC} = 4.75V			0.8	V
V_{IH}	High	V_{CC} = 5.25V	2.0			V
V_{IC}	Clamp	I_{IN} = −12mA			−1.2	V
Output voltage						
		$\overline{CE}$ = Low				
V_{OL}	Low	I_{OUT} = 16mA			0.45	V
V_{OH}	High	I_{OUT} = −2mA	2.4			V
Input current						
I_{IL}	Low	V_{IN} = 0.45V			−100	μA
I_{IH}	High	V_{IN} = 5.5V			50	μA
Output current						
I_{OLK}	Leakage (82S23)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	μA
I_{OZ}	Hi-Z State (82S123)	$\overline{CE}$ = High, V_{OUT} = 5.5V			40	
		$\overline{CE}$ = High, V_{OUT} = 0.5V			−40	
I_{OS}	Short circuit (82S123)[3]	$\overline{CE}$ = Low, V_{OUT} = 0V, High stored	−15		−90	mA
Supply current[7]						
I_{CC}		V_{CC} = 5.25V			96	mA
Capacitance						
		$\overline{CE}$ = High, V_{CC} = 5.0V				
C_{IN}	Input	V_{IN} = 2.0V		5		pF
C_{OUT}	Output	V_{OUT} = 2.0V		8		pF

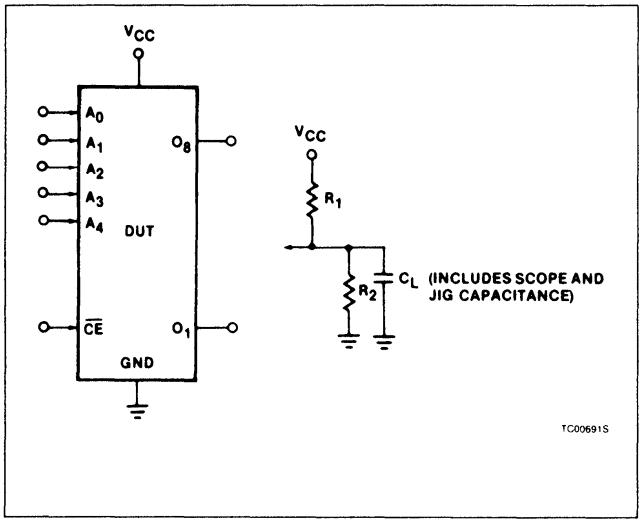
Notes on following page.

AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

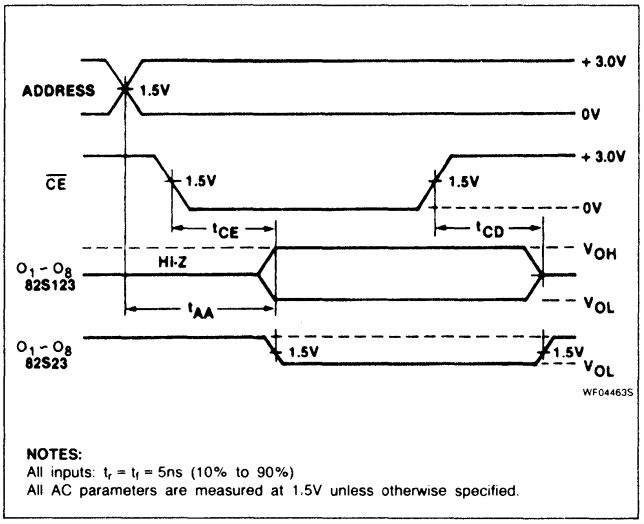
SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ[5]	Max	
Access time[4]							
t_{AA}		Output	Address		45	50	ns
t_{CE}		Output	Chip Enable			35	ns
Disable time[6]							
t_{CD}		Output	Chip Enable			35	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground terminal.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = +25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.
7. Measured with all inputs grounded and all outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORMS



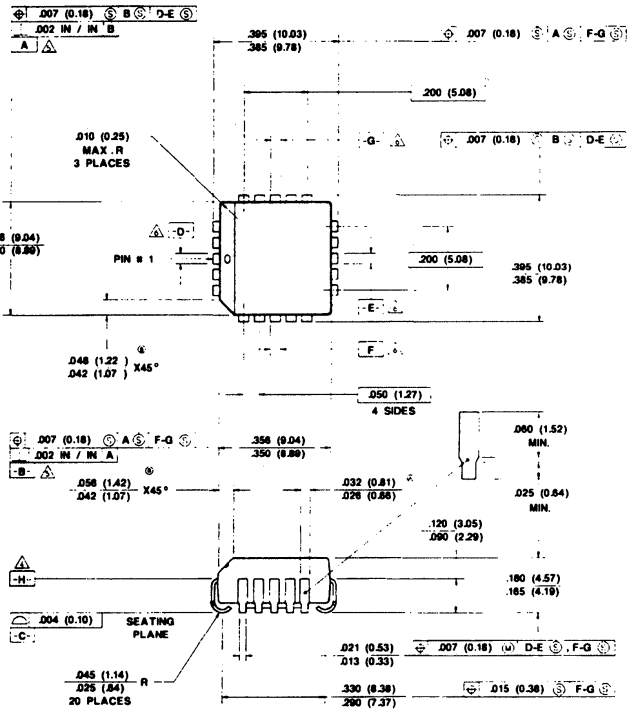
NOTES:
All inputs: $t_r = t_f = 5ns$ (10% to 90%)
All AC parameters are measured at 1.5V unless otherwise specified.

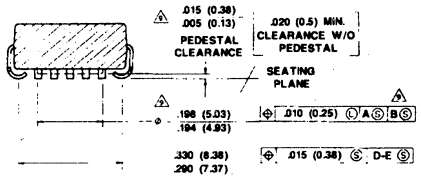
PLASTIC LEADED CHIP CARRIER (PLCC)

NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
20	A	72/31	350mil-square
28	A	60/24	450mil-square
32	A	58/18	450 × 550mil-rectangular

1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test Fixture: Device soldered to a glass epoxy test board with the dimensions 1.58″ × 0.75″ × 0.059″ with 0.009″ stand off.

20-PIN PLASTIC LEADED CHIP CARRIER





NOTES:
1. Package dimensions conform to JEDEC specification MO-047-AA for plastic leaded chip carrier 20 leads, .050 inch lead spacing, square. (issue A, 10/31/84).
2. Controlling dimensions: inches. Metric dimensions in mm are shown in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982.
4. Datum plane "H" located at the top of mold parting line and coincident with top of lead. Where lead exists plastic body.
5. Location to datum "A" and "B" to be determined at plane "H".These datums do not include mold flash. Mold flash protrusion shall not exceed .006" (0.15mm) on any side.
6. Datum "D-E" and "F-G" are determined where these center leads exit from the body at plane "H".
7. Pin numbers continue counterclockwise to pin #20 (top view).
8. Signetics order code for product packaged in a PLCC is the suffix "A" after the product number.
9. Applicable to packages with pedestal only.

Package Outlines

PLASTIC DUAL-IN-LINE PACKAGES

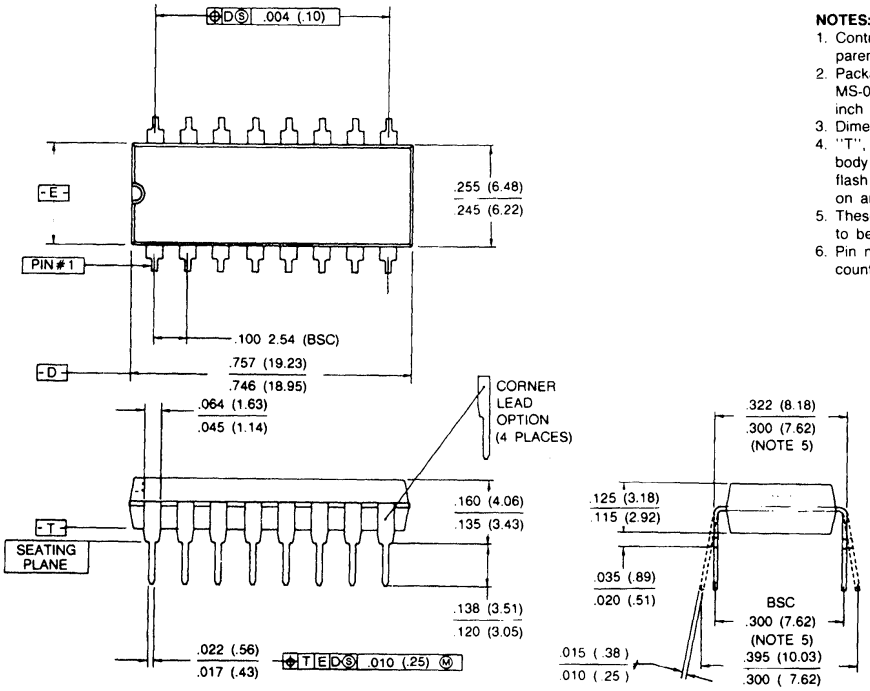
NO. OF LEADS	PACKAGE CODE	θ_{JA}/θ_{JC}	DESCRIPTION
16	N	76/26	300mil-wide
18	N	63/24	300mil-wide
20	N	60/24	300mil-wide
22	N	56/21	400mil-wide
24	N/N3[1]	52/20	300mil-wide
24	N	44/18	600mil-wide
28	N	42/16	600mil-wide

NOTES:
1. Order coded as N3 when both 600mil and 300mil-wide packages are available.

PLASTIC DIP

1. Lead material: Olin 194 (Copper Alloy) or equivalent, solder dipped.
2. Body material: Plastic (Epoxy).
3. Thermal test fixture: Device secured in a Textool ZIF socket with 0.04" stand off.

16-PIN PLASTIC DUAL IN-LINE (PDIP)



NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AA for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 16 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #16 when viewed from the top.

NJ1 853-0406 81232

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