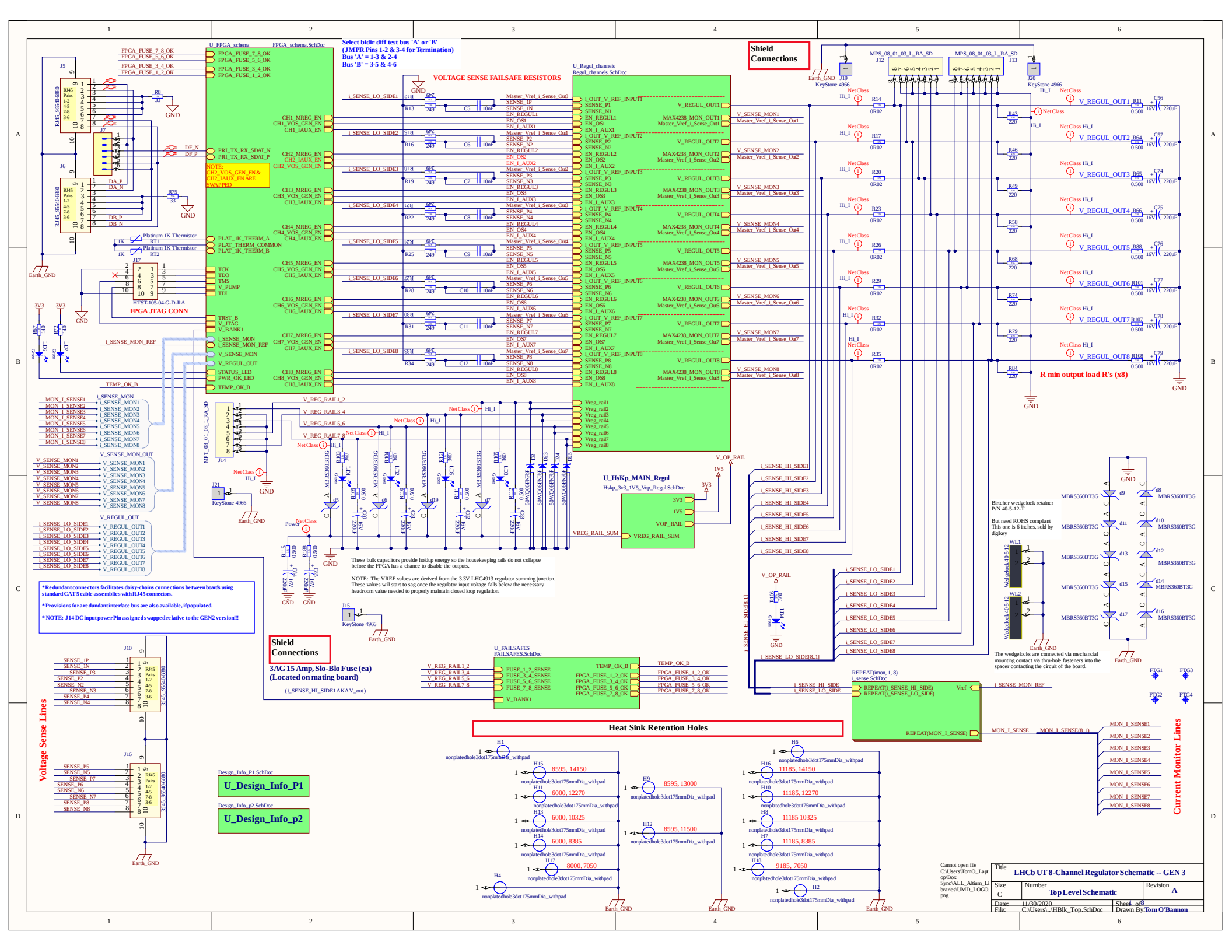
Select bidir diff test bus 'A' or 'B'
(JMPR Pins 1-2 & 3-4 for Termination)
Bus 'A' = 1-3 & 2-4
Bus 'B' = 3-5 & 4-6
VOLTAGE SENSE FAILSAFE RESISTORS
Shield Connections
U_FPGA_schema
FPGA_schema.SchDoc
U_Regul_channels
Regul_channels.SchDoc
FPGA JTAG CONN
HTST-105-04-G-D-RA
R min output load R's (x8)
U_HsKp_MAIN_Regul
Hskp_3v3_1V5_Vop_RegulSch.Doc
U_FAILSAFES
FAILSAFES.SchDoc
3AG 15 Amp, Slo-Blo Fuse (ea)
(Located on mating board)
(I_SENSE_HI_SIDE1 AKA V_out)
Heat Sink Retention Holes
Voltage Sense Lines
Current Monitor Lines
Design_Info_P1.SchDoc
U_Design_Info_P1
Design_Info_p2.SchDoc
U_Design_Info_p2
These bulk capacitors provide holdup energy so the housekeeping rails do not collapse before the FPGA has a chance to disable the outputs.
NOTE: The VREF values are derived from the 3.3V LHC4913 regulator summing junction. These values will start to sag once the regulator input voltage falls below the necessary headroom value needed to properly maintain closed loop regulation.
Bircher wedgelock retainer P/N 40-5-12-T
But need ROHS compliant This one is 6 inches, sold by digikey
The wedgelocks are connected via mechanical mounting contact via thru-hole fasteners into the spacer contacting the circuit of the board.
*Redundant connectors facilitates daisy-chains connections between boards using standard CAT 5 cable assemblies with RJ45 connectors.
*Provisions for a redundant interface bus are also available, if populated.
*NOTE: J14 DC input power Pin assigned swapped relative to the GEN2 version!!!
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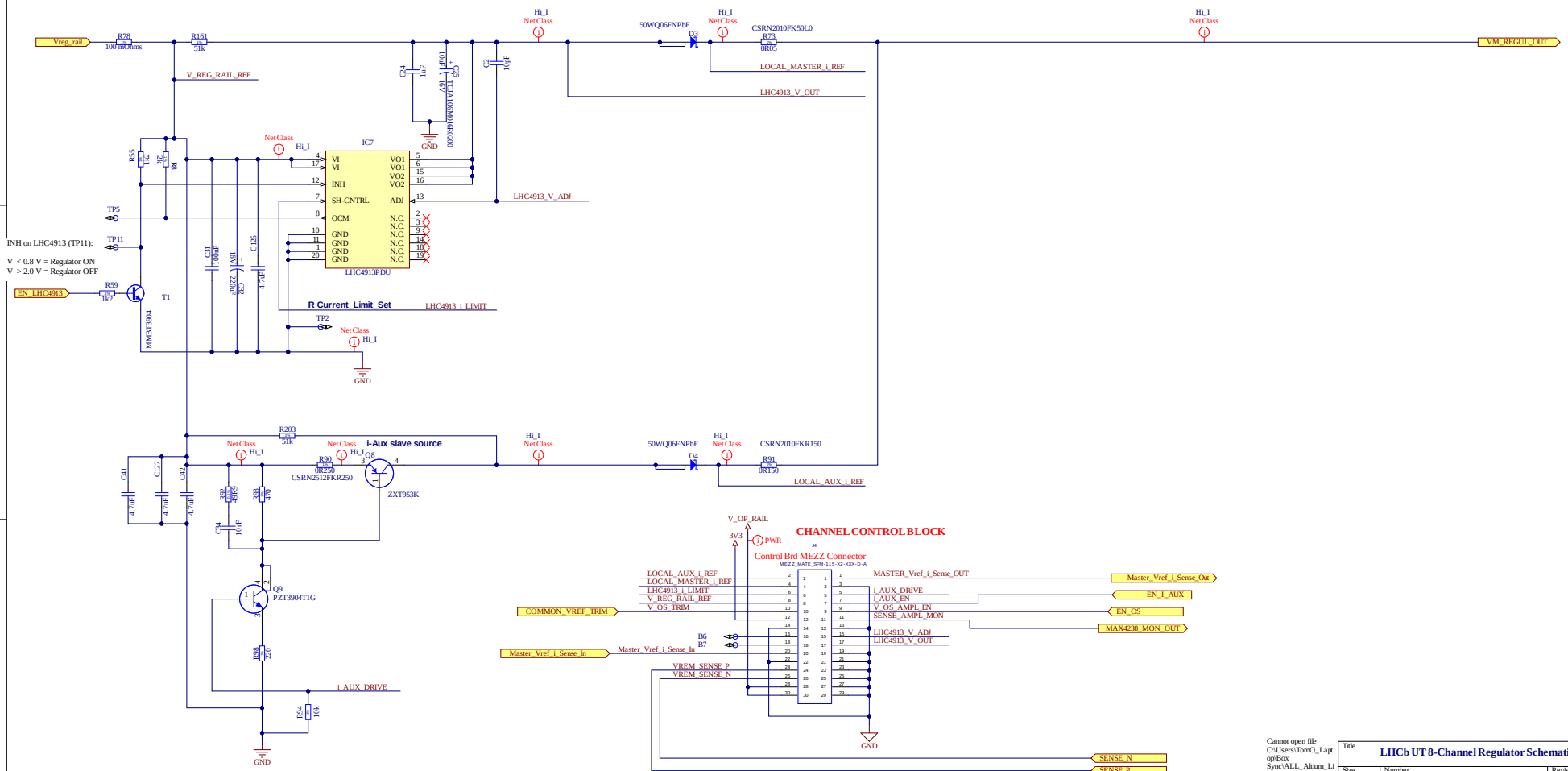
Title
LHCb UT 8-Channel Regulator Schematic -- GEN 3
Size
C
Number
Top Level Schematic
Revision
A
Date: 11/30/2020
Sheet 1 of 1
File: C:\Users\..\HBlk_Top.SchDoc
Drawn By: Tom O'Bannon



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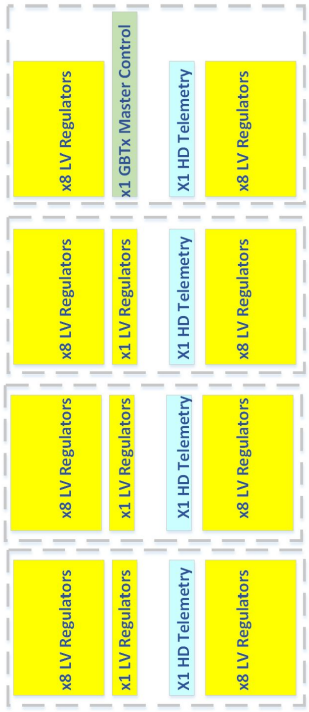
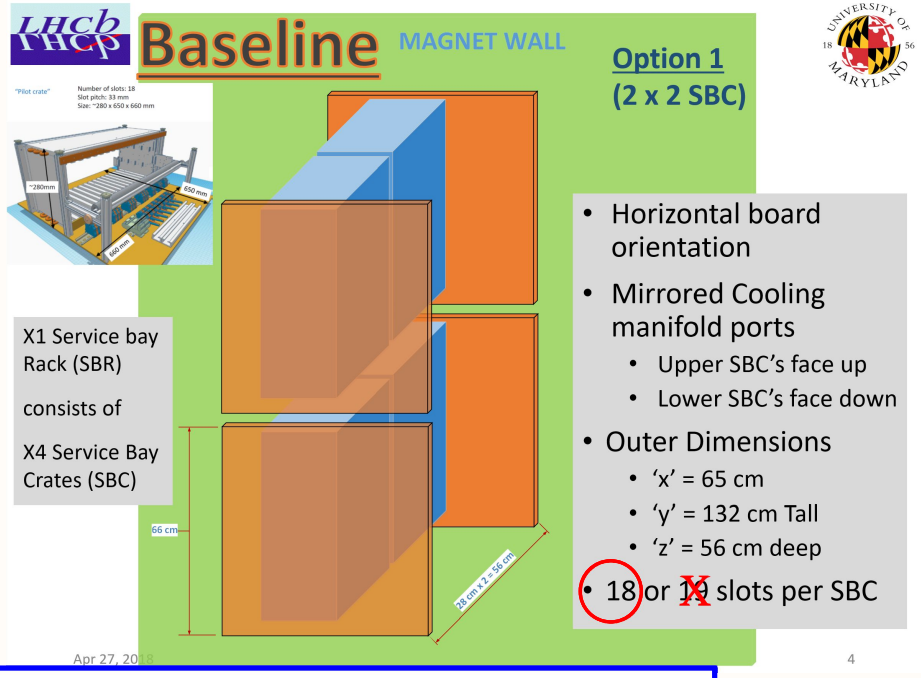
Title	LHCb UT 8-Channel Regulator Schematic -- GEN 3	
Size: C	Number: Regulator Channel Circuit	Revision: A
Date: 11/30/2020	Sheet of 2	2
File: C:\Users\...\RegulatorBlk.SchDoc	Drawn By: Tom O'Bannon	

18 Slots @ 33 mm pitch per SBC
(Preset 'Pilot' SBC Config)



Supports:
(a) distributed GBT-SCA daughter brds
(c) high density telemetry



64 GBT-SCA user manual

13.2. POWER SUPPLY

The nominal power supply voltages are VDD = DVDD = AVDD = 1.5V.

The core logic is operational at a supply voltage (VDD) down to 1.2 V (at 25C).

The IO pad power supply (DVDD) works at 2.5V allowing to interface with 2.5V powered devices.

13.3. ABSOLUTE MAXIMUM POWER SUPPLY RATINGS

Table 13.1 shows the absolute minimum and maximum voltages for the three supplies power the GBT-SCA ASIC.

	MINIMUM	MAXIMUM
VDD	1.2V - 10%	1.5V + 10% DVDD + 0.3V
AVDD	1.5V - 10%	1.5V + 10% DVDD + 0.3V
DVDD	1.2V - 10%	3.3V

Table 13.1 – Maximum power supply ratings

1) Fuses should be 12 AMP Slo-Blo max (each)
2) Initial turn on procedure needed to make sure 3V3 and 1V5 rails are underspec at initial turn-on and then trimmed to the final desired values. (rotate pots xx turns in xxW direction to ensure setpoints are at lowest value for initial power-on.

13.5. POWER CONSUMPTION

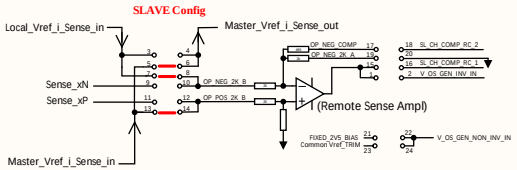
Measured value at: DVDD = 1.5V, VDD = 1.5V, AVDD = 1.5V

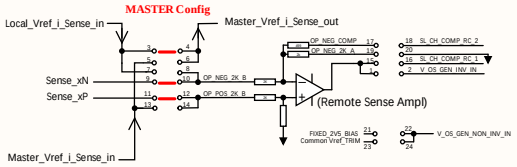
SUPPLY	TYPICAL	MAXIMUM (at the TID peak of leakage)
VDD core	36 mA	63 mA
AVDD analog	0.5 mA	0.8 mA
DVDD Static supply current	7.1 mA	8.2 mA

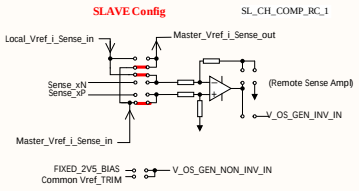
Table 13.3 – GBT-SCA power consuption

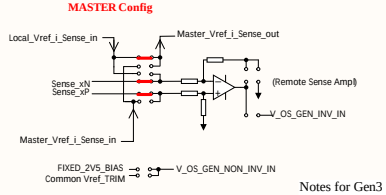
Title *
Size: C | Number:* | Revision:*
Date: 11/30/2020 Time: 4:30:53 PM | Sheet* of *
File: C:\Users\amus\Downloads\2019-09-05_lvr_project\2019-09-05_lvr_project\TomO_LV_Reg_WIP\RegGen3_PCB_UPDATE.Des
Altium

SL_CH_COMP_RC_2





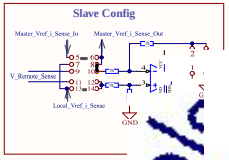


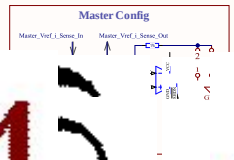


Notes for Gen3 Updates regarding the Master-Slave channel configuration:

(1) The slave channel Vos_gen needs to be DISABLED by the gateware (ie only the master gets the offset command signal at startupsince the slaves are already following the master output synthetic summing junction

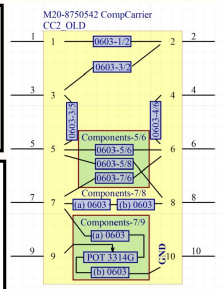
(2) The slave channel needs a jumper between J8 pins 15 to 16.



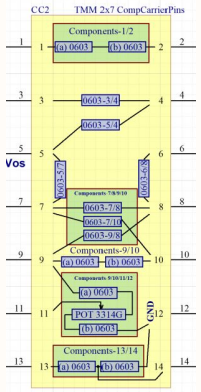


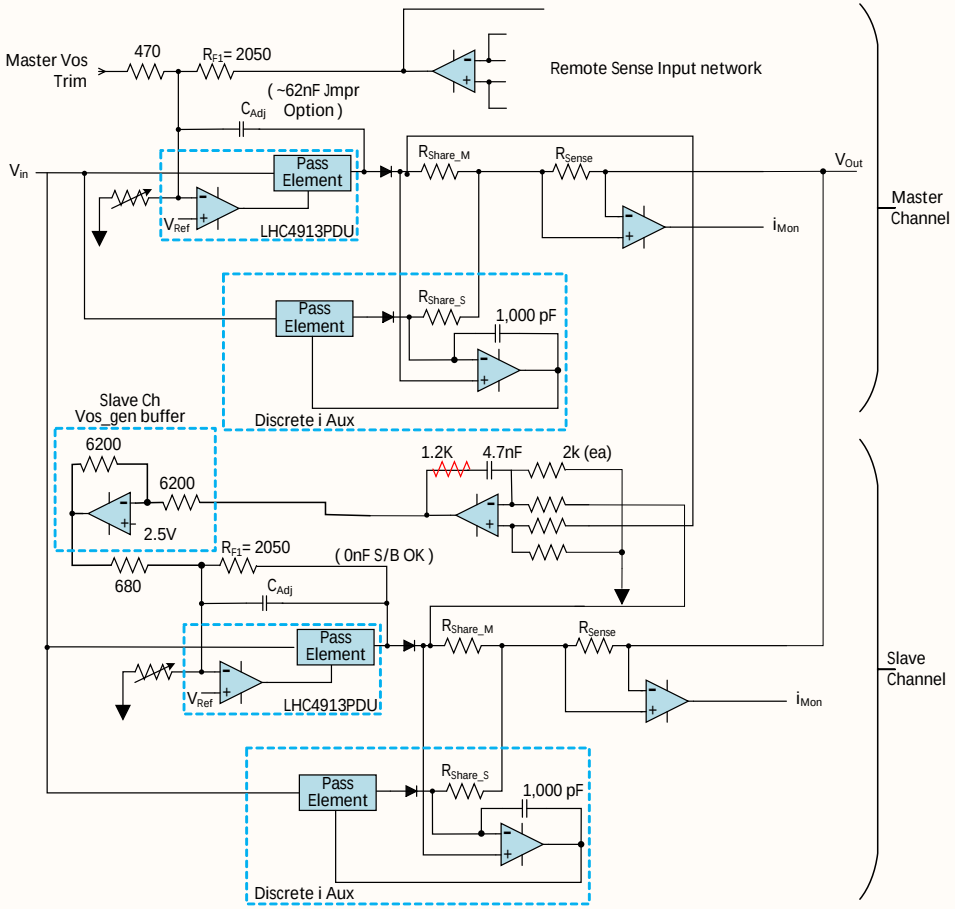
MASTER CHANNEL
1/2: Slave Ch Comp
(a) DNI
(b) DNI
3/4: 900 PF (i-slave comp)
5/4: DNI
5/7: Offset 470 Ohm resistor
6/8: R_compensation
7/8: C_compensation
7/10: DNI ALT Ri (trim)
9/8 DNI
9/10: (a) = (b) = Current Limit Placeholder
9/11: Trimmer Config
(a) DNI
(b) Ch Cfg Dependent
(c) Ch Cfg Dependent
13/14: OS gen Ampl bias for SLAVE
(a) DNI
(b) DNI

SLAVE CHANNEL
1/2: 900 PF (i-slave comp)
3/2: DNI
3/5: Offset 470 Ohm resistor
4/6: R_compensation
5/6: C_compensation
5/8: DNI ALT Ri (trim)
7/6 DNI
7/8: (a) = (b) = Current Limit Placeholder
7/9: Trimmer Config
(a) DNI
(b) Ch Cfg Dependent
(c) Ch Cfg Dependent

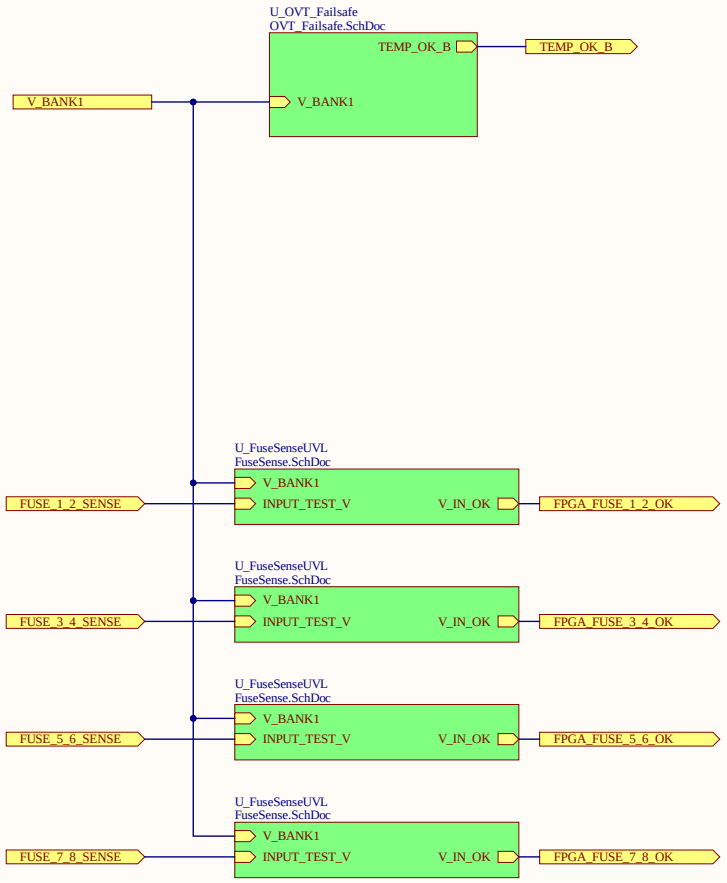


MASTER CHANNEL
1/2: Slave Ch Comp
(a) 604 Ohm resistor
(b) 4.7 nF capacitor
3/4: 900 PF (i-slave comp)
5/4: DNI
5/7: Offset 680 Ohm resistor
6/8: R_compensation
7/8: C_compensation
7/10: DNI ALT Ri (trim)
9/8 DNI
9/10: (a) = (b) = Current Limit Placeholder
9/11: Trimmer Config
(a) DNI
(b) Ch Cfg Dependent
(c) Ch Cfg Dependent
13/14: OS gen Ampl bias for SLAVE Ch
(a) 1.1K Ohms
(b) 3.4 K Ohms





Title		
Size C	Number	Revision
Date: 11/30/2020		Sheet of
File: C:\Users\..\Design_Info_p2.SchDoc		Drawn By:



This circuit provides an over-temperature indicator for the FPGA. This allows for a local temperature failsafe protection implementated by the FPGA so outputs can be turned off using the preferred sequence method.

These 4 FusesenseUVL modules perform an under-voltage sense for each of the fuse inputs.

The voltage threshold is determined by discrete components configured with a partial temperature compensation to reduce temperature effects. All othe r housekeeping voltage rails are inadequate for establishing a threshold since they are essentially derived from the 1.225V ref of the housekeeping LHC4913. This Vref is only guarenteed to be accurate when the input is above 3.3V + 0.5V.

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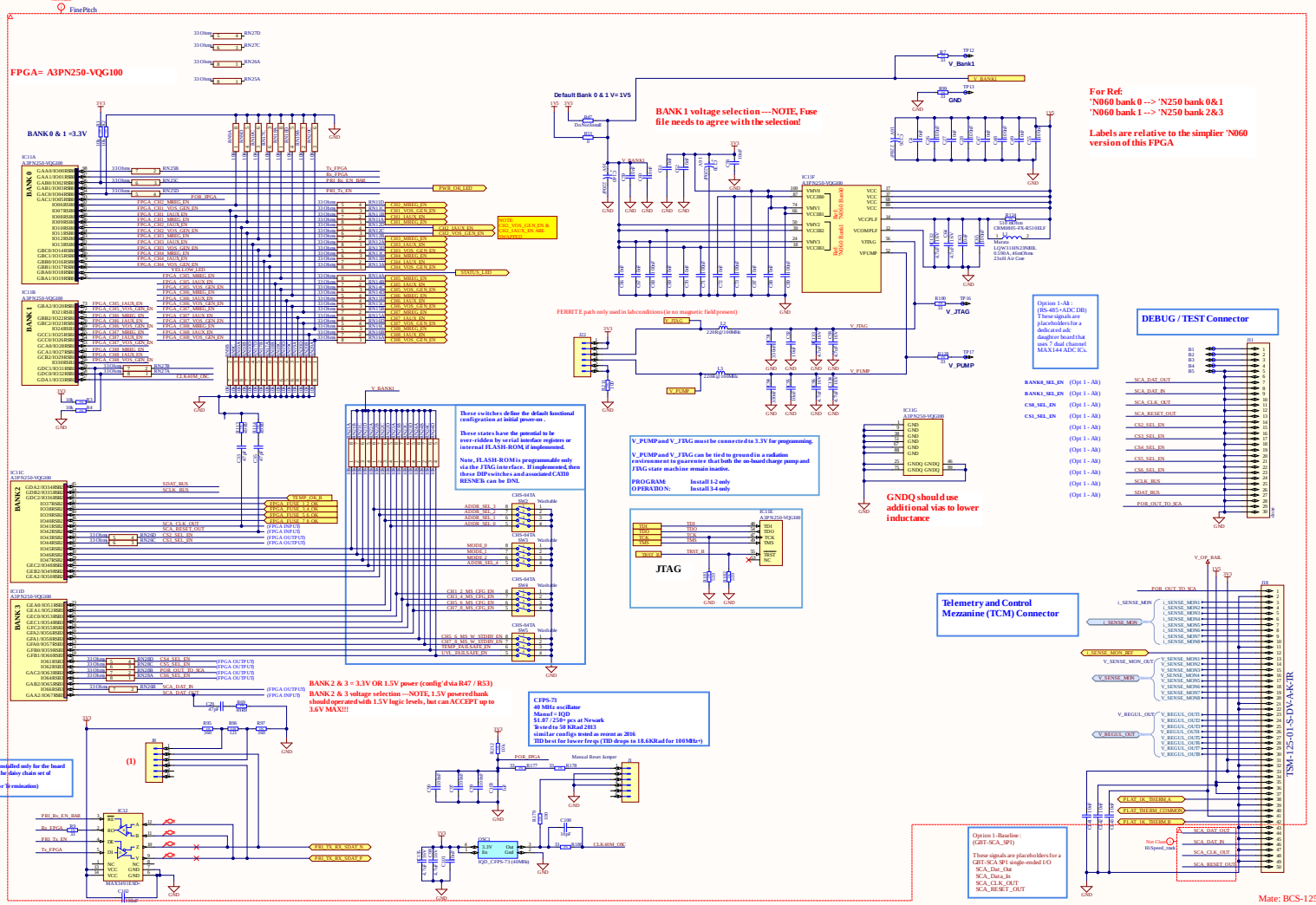
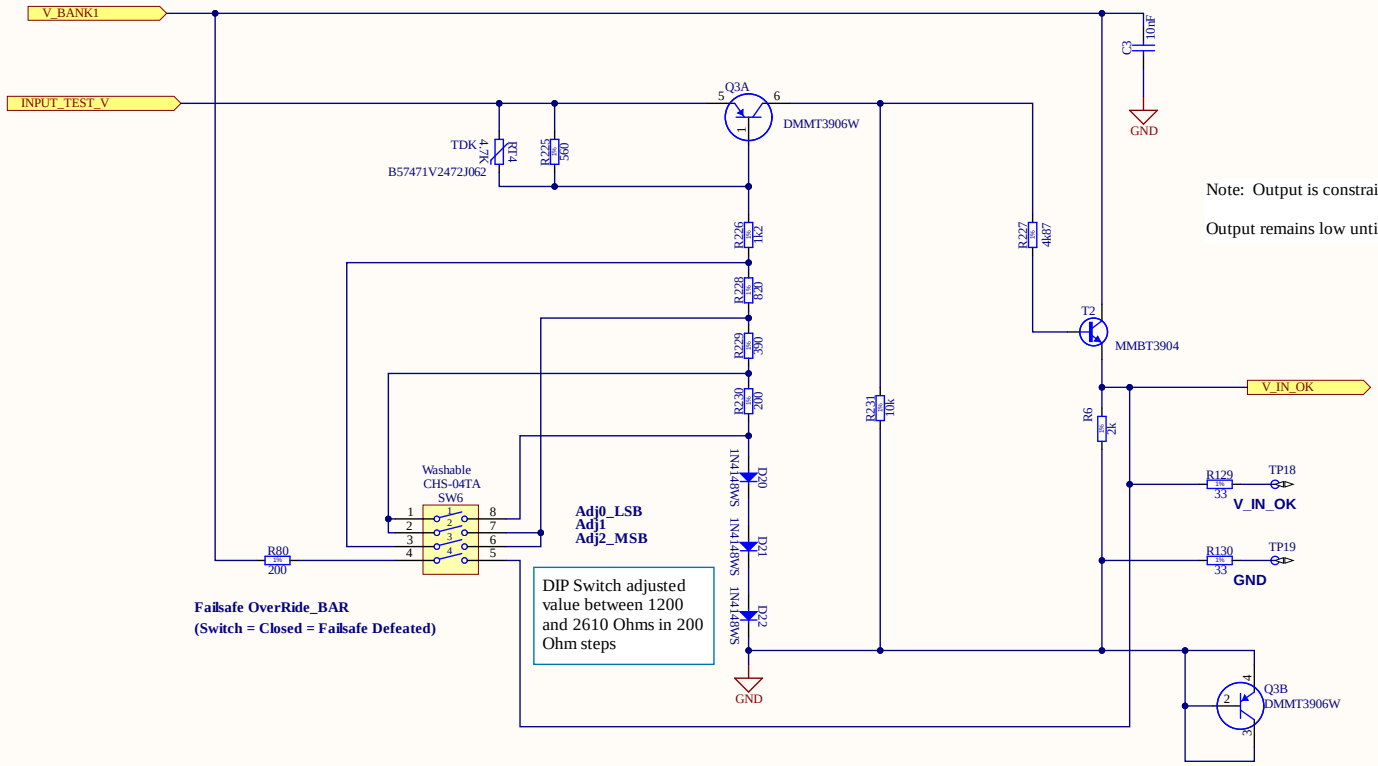
Title	**LHCb UT 8-Channel Regulator Schematic -- GEN 3**	
Size: B	Number: **Failsafes**	Revision: **A**
Date: 11/30/2020	Sheet * of *	
File: C:\Users\..\FAILSAFES.SchDoc	Drawn By: **Tom O'Bannon**	


FPGA= A3PN250-VQG100
BANK 0 & 1 =3.3V
Default Bank 0 & 1 V= 1V5
BANK 1 voltage selection ---NOTE, Fuse file needs to agree with the selection!
For Ref:
'N060 bank 0 --> 'N250 bank 0&1
'N060 bank 1 --> 'N250 bank 2&3
Labels are relative to the simplier 'N060 version of this FPGA
FERRITE path only used in lab conditions (ie no magnetic field present)
DEBUG / TEST Connector
JTAG
V_PUMPand V_JTAG must be connected to 3.3V for programming.
V_PUMPand V_JTAG can be tied to ground in a radiation environment to guarantee that both the on-board charge pump and JTAG state machine remain inactive.
PROGRAM: Install 1-2 only
OPERATION: Install 3-4 only
These switches define the default functional configuration at initial power-on .
These states have the potential to be over-ridden by serial interface registers or internal FLASH-ROM, if implemented.
Note, FLASH-ROM is programmable only via the JTAG interface. If implemented, then these DIP switches and associated CAT93 RESNETs can be DNI.
GNDQ should use additional vias to lower inductance
Telemetry and Control Mezzanine (TCM) Connector
BANK 2 & 3 = 3.3V OR 1.5V power (config'd via R47 / R53)
BANK 2 & 3 voltage selection --NOTE, 1.5V powered bank should operated with 1.5V logic levels, but can ACCEPT up to 3.6V MAX!!!
CFPS-73
40 MHz oscillator
Manuf = IQD
$1.07 /250+ pcs at Newark
Tri-ed to 50 KRad 2013
similar configs tested as recent as 2016
TID best for lower fresps (TID drops to 18.6KRad for 100MHz+)
(1) Termination Jumpers installed only for the board located at both ends of the daisy chain set of connections.
(JMPR Pins 1-2 & 3-4 for Termination)
Option 1-Baseline : (GBT-SCA_SPI)
These signals are placeholders for a GBT-SCA SPI single-ended I/O
SCA_Dat_Out
SCA_Data_In
SCA_CLK_OUT
SCA_RESET_OUT
Option 1-Alt : (RS-485+ADC DB)
These signals are placeholders for a dedicated adc daughter board that uses 7 dual channel MAX1444 ADC ICs.
Mate: BCS-125-L-D-TE
TSM-125-01-S-DV-A-K-TR
LHCb UT 8-Channel Regulator Schematic -- GEN 3
Control FPGA
Date: 11/30/2020
Sheet 6 of 8
File: C:\Users\...\FPGA_schema.SchDoc
Drawn By: Ben O'Bannon



Note: Output is constrained to V_BANK1 max

Output remains low until the input is above the defined threshold

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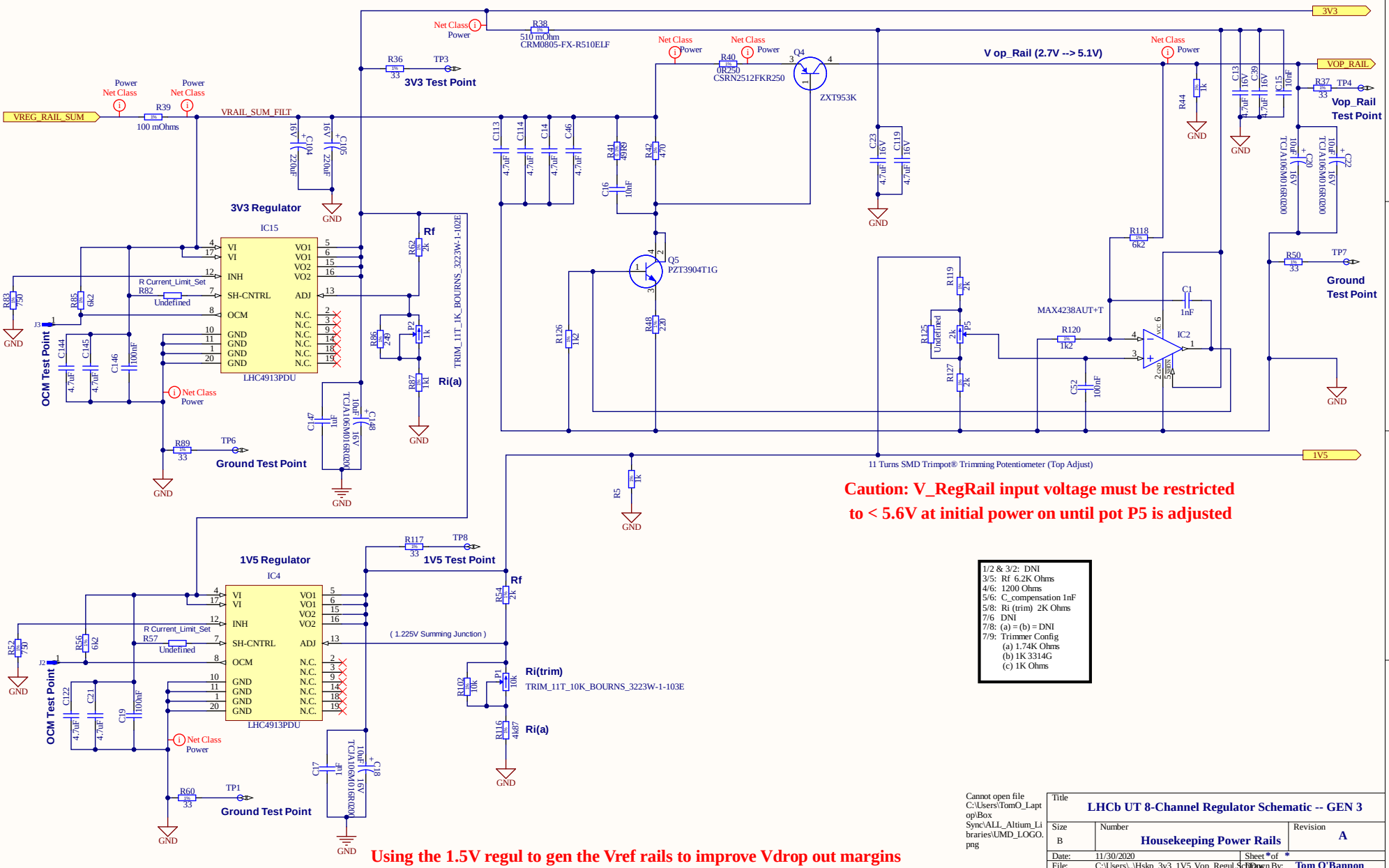
Title	LHCb UT 8-Channel Regulator Schematic -- GEN 3	
Size: B	Number: Under Voltage Lockout (UVL)	Revision: A
Date: 11/30/2020	Sheet * of *	
File: C:\Users\..\FuseSense.SchDoc	Drawn By: Tom O'Bannon	


3V3
VOP_RAIL
1V5
VREG_RAIL_SUM
VRAIL_SUM_FILT
R38
510 mOhm
CRM0805-FX-R510ELF
R40
0R250
CSRN2512FKR250
Q4
ZXT953K
V op_Rail (2.7V --> 5.1V)
R39
100 mOhms
R36
TP3
3V3 Test Point
R37
TP4
Vop_Rail
Test Point
R50
TP7
Ground
Test Point
3V3 Regulator
IC15
LHC4913PDU
Rf
R62
2k
TRIM_11T_1K_BOURNS_3223W-1-102E
Ri(a)
R87
1kt
R86
249
P2
1k
R83
750
R85
6k2
R82
Undefined
R Current_Limit_Set
OCM Test Point
J3
C144
C145
C146
100nF
4.7uF
C104
220uF
C105
220uF
C113
C114
C14
C46
C16
10nF
R44
49R9
R42
470
C23
C119
R44
1K
C13
C39
C15
10nF
R118
6k2
R119
2k
R125
Undefined
R126
1k2
R127
2k
P5
MAX4238AUT+T
R120
1k2
C1
1nF
C52
100nF
IC2
C72
C20
TCJA106M016R0200
10uF
16V
C147
1uF
C148
R89
TP6
Ground Test Point
11 Turns SMD Trimpot® Trimming Potentiometer (Top Adjust)
R5
1K
Caution: V_RegRail input voltage must be restricted
to < 5.6V at initial power on until pot P5 is adjusted
1V5 Regulator
IC4
R117
TP8
1V5 Test Point
R54
2k
(1.225V Summing Junction)
R52
750
R56
6k2
R57
Undefined
J2
C122
C21
C19
R102
10k
P1
10k
Ri(trim)
TRIM_11T_10K_BOURNS_3223W-1-103E
R116
4k87
Ri(a)
C17
1uF
C18
R60
TP1
Ground Test Point
1/2 & 3/2: DNI
3/5: Rf 6.2K Ohms
4/6: 1200 Ohms
5/6: C_compensation 1nF
5/8: Ri (trim) 2K Ohms
7/6 DNI
7/8: (a) = (b) = DNI
7/9: Trimmer Config
(a) 1.74K Ohms
(b) 1K 3314G
(c) 1K Ohms
Using the 1.5V regul to gen the Vref rails to improve Vdrop out margins
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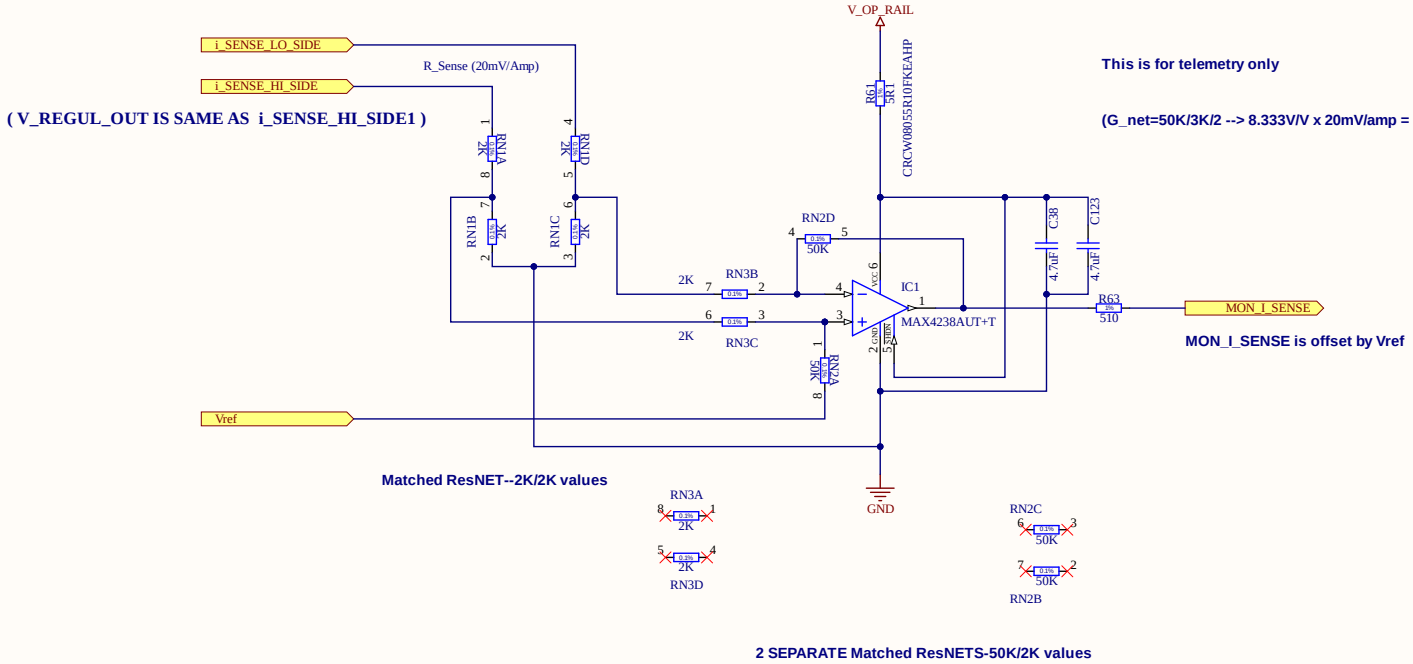
Title
LHCb UT 8-Channel Regulator Schematic -- GEN 3
Size
B
Number
Housekeeping Power Rails
Revision
A
Date:
11/30/2020
Sheet * of *
File:
C:\Users\..\Hskp_3v3_1V5_Vop_Regul.SchDoc
Drawn By:
Tom O'Bannon



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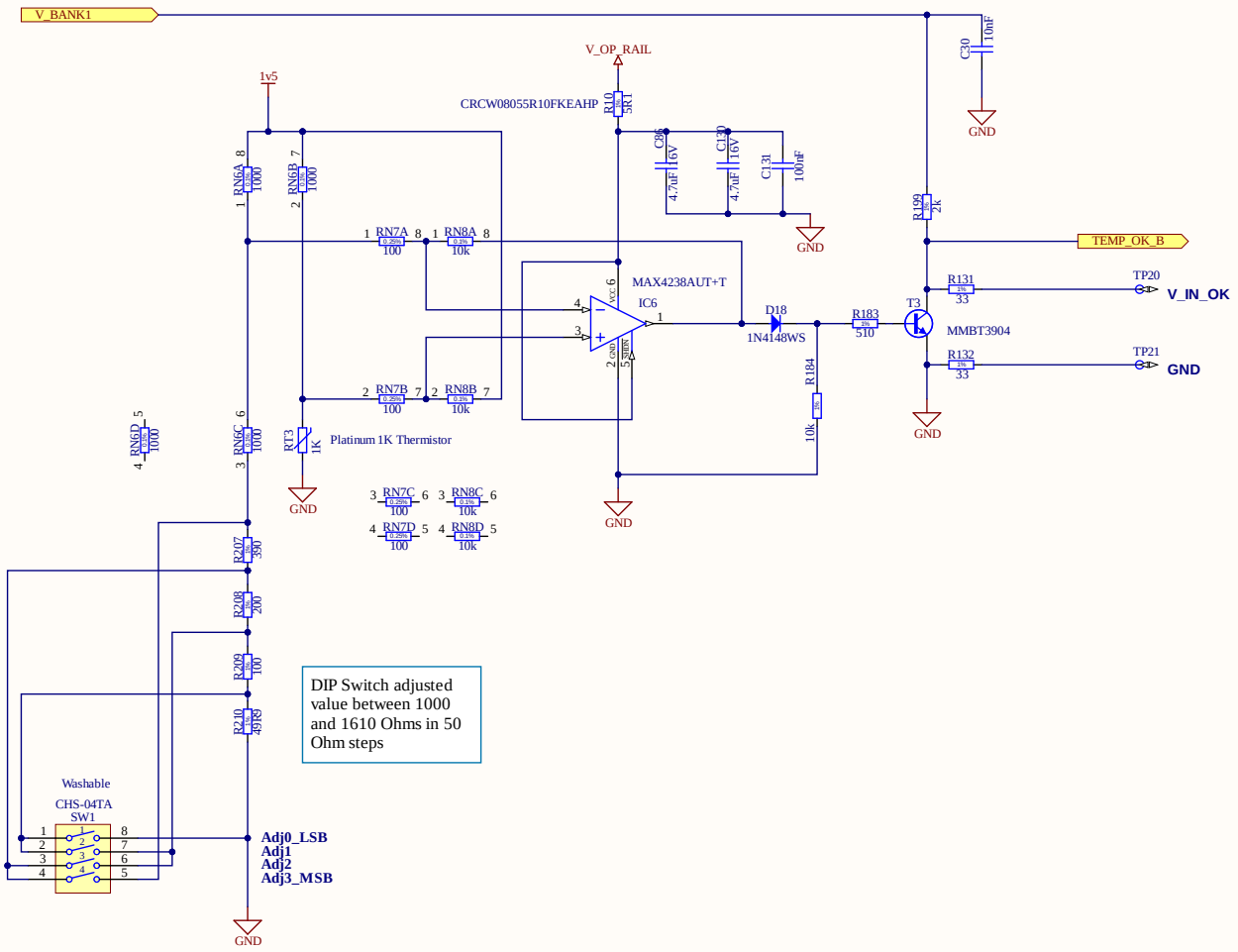
Title	LHCb UT 8-Channel Regulator Schematic -- GEN 3	
Size: B	Number: i-Sense Monitor	Revision: A
Date: 11/30/2020	Sheet * of *	
File: C:\Users\..\i_sense.SchDoc	Drawn By: Tom O'Bannon	



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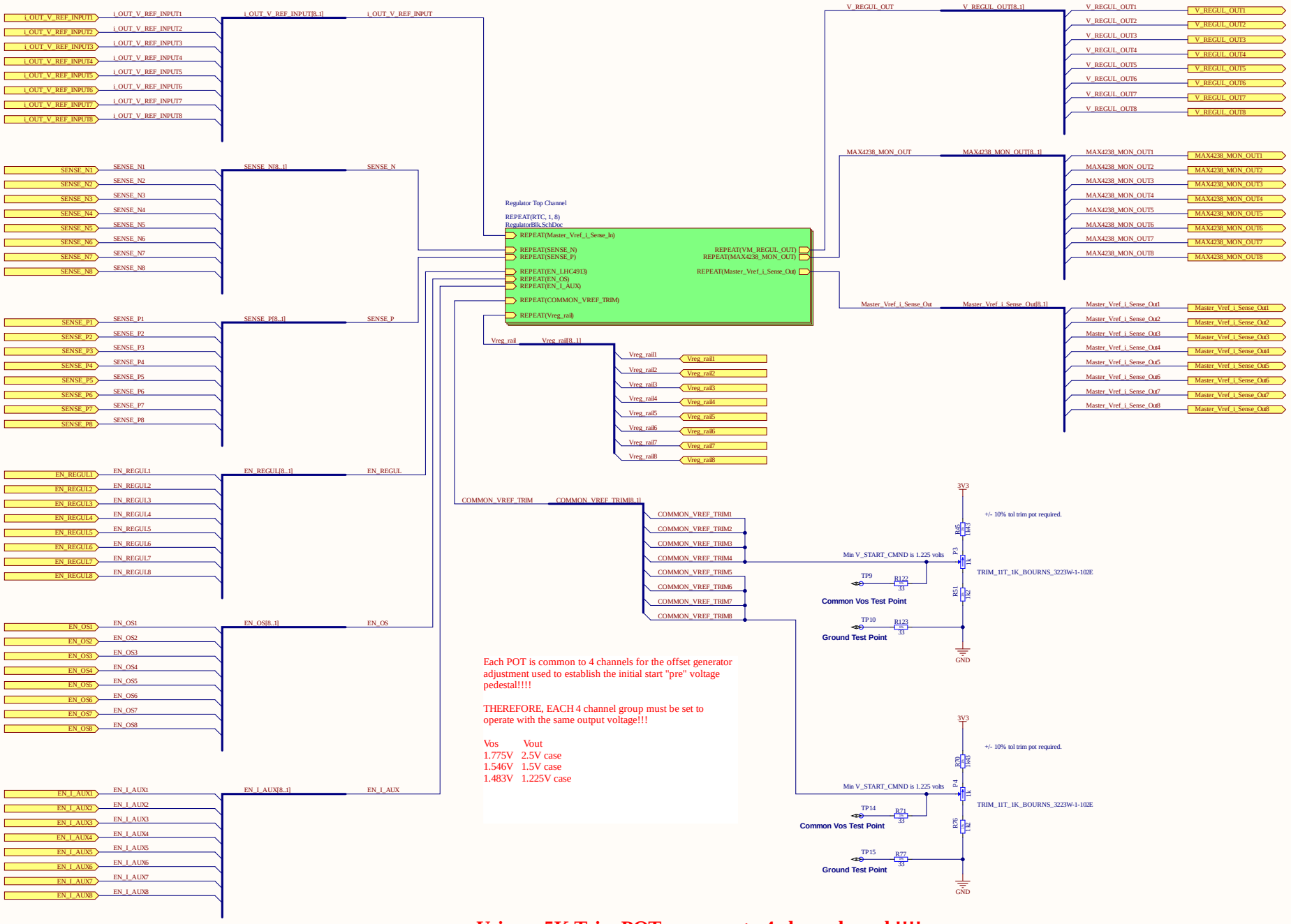
Title	LHCb UT 8-Channel Regulator Schematic -- GEN 3	
Size: B	Number: Over-Temperature Failsafe	Revision: A
Date: 11/30/2020		Sheet of
File: C:\Users\..\OVT_Failsafe.SchDoc		Drawn By: Tom O'Bannon


i_OUT_V_REF_INPUT1
i_OUT_V_REF_INPUT2
i_OUT_V_REF_INPUT3
i_OUT_V_REF_INPUT4
i_OUT_V_REF_INPUT5
i_OUT_V_REF_INPUT6
i_OUT_V_REF_INPUT7
i_OUT_V_REF_INPUT8
i_OUT_V_REF_INPUT[8..1]
i_OUT_V_REF_INPUT
SENSE_N1
SENSE_N2
SENSE_N3
SENSE_N4
SENSE_N5
SENSE_N6
SENSE_N7
SENSE_N8
SENSE_N[8..1]
SENSE_N
SENSE_P1
SENSE_P2
SENSE_P3
SENSE_P4
SENSE_P5
SENSE_P6
SENSE_P7
SENSE_P8
SENSE_P[8..1]
SENSE_P
EN_REGUL1
EN_REGUL2
EN_REGUL3
EN_REGUL4
EN_REGUL5
EN_REGUL6
EN_REGUL7
EN_REGUL8
EN_REGUL[8..1]
EN_REGUL
EN_OS1
EN_OS2
EN_OS3
EN_OS4
EN_OS5
EN_OS6
EN_OS7
EN_OS8
EN_OS[8..1]
EN_OS
EN_I_AUX1
EN_I_AUX2
EN_I_AUX3
EN_I_AUX4
EN_I_AUX5
EN_I_AUX6
EN_I_AUX7
EN_I_AUX8
EN_I_AUX[8..1]
EN_I_AUX
Regulator Top Channel
REPEAT(RTC, 1, 8)
RegulatorBlk.SchDoc
REPEAT(Master_Vref_i_Sense_In)
REPEAT(SENSE_N)
REPEAT(SENSE_P)
REPEAT(EN_LHC4913)
REPEAT(EN_OS)
REPEAT(EN_I_AUX)
REPEAT(COMMON_VREF_TRIM)
REPEAT(Vreg_rail)
REPEAT(VM_REGUL_OUT)
REPEAT(MAX4238_MON_OUT)
REPEAT(Master_Vref_i_Sense_Out)
Vreg_rail
Vreg_rail[8..1]
Vreg_rail1
Vreg_rail2
Vreg_rail3
Vreg_rail4
Vreg_rail5
Vreg_rail6
Vreg_rail7
Vreg_rail8
V_REGUL_OUT
V_REGUL_OUT[8..1]
V_REGUL_OUT1
V_REGUL_OUT2
V_REGUL_OUT3
V_REGUL_OUT4
V_REGUL_OUT5
V_REGUL_OUT6
V_REGUL_OUT7
V_REGUL_OUT8
MAX4238_MON_OUT
MAX4238_MON_OUT[8..1]
MAX4238_MON_OUT1
MAX4238_MON_OUT2
MAX4238_MON_OUT3
MAX4238_MON_OUT4
MAX4238_MON_OUT5
MAX4238_MON_OUT6
MAX4238_MON_OUT7
MAX4238_MON_OUT8
Master_Vref_i_Sense_Out
Master_Vref_i_Sense_Out[8..1]
Master_Vref_i_Sense_Out1
Master_Vref_i_Sense_Out2
Master_Vref_i_Sense_Out3
Master_Vref_i_Sense_Out4
Master_Vref_i_Sense_Out5
Master_Vref_i_Sense_Out6
Master_Vref_i_Sense_Out7
Master_Vref_i_Sense_Out8
COMMON_VREF_TRIM
COMMON_VREF_TRIM[8..1]
COMMON_VREF_TRIM1
COMMON_VREF_TRIM2
COMMON_VREF_TRIM3
COMMON_VREF_TRIM4
COMMON_VREF_TRIM5
COMMON_VREF_TRIM6
COMMON_VREF_TRIM7
COMMON_VREF_TRIM8
3V3
+/- 10% tol trim pot required.
R45
1kΩ
P3
1K
TRIM_11T_1K_BOURNS_3223W-1-102E
Min V_START_CMND is 1.225 volts
TP9
R122
33
Common Vos Test Point
R51
1kΩ
TP10
R123
33
Ground Test Point
GND
Each POT is common to 4 channels for the offset generator adjustment used to establish the initial start "pre" voltage pedestal!!!!
THEREFORE, EACH 4 channel group must be set to operate with the same output voltage!!!
Vos Vout
1.775V 2.5V case
1.546V 1.5V case
1.483V 1.225V case
3V3
+/- 10% tol trim pot required.
R70
1kΩ
P4
1K
TRIM_11T_1K_BOURNS_3223W-1-102E
Min V_START_CMND is 1.225 volts
TP14
R71
33
Common Vos Test Point
R76
1kΩ
TP15
R77
33
Ground Test Point
GND
Using a 5K Trim POT common to 4 channels each!!!!
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Title
LHCb UT 8-Channel Regulator Schematic -- GEN 3
Size
C
Number
Regulator Channels
Revision
A
Date:
11/30/2020
Sheet* of *
File:
C:\Users\..\Regul_channels.SchDoc
Drawn By:
Tom O'Bannon