Dave

AMERICAN MICRO-SYSTEMS, INC.
S9021
DYNAMIC KEYBOARD ENCODER
JANUARY 1973

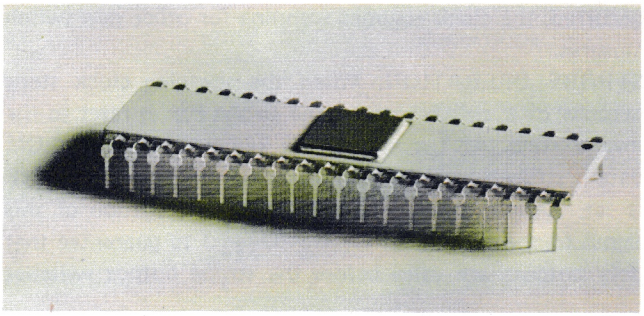
REPRESENTED BY
TECHNICAL ASSOCIATES INC.
4915 WEST 35TH STREET
MINNEAPOLIS, MINNESOTA 55416
PHONE: (612) 929-6721

FEATURES

- 3600 Bit ROM programmed by altering one mask
- 90 Key encoding
- 4 Modes
- Shift control lockout
- 10 Data outputs plus a strobe (data ready signal)
- Zener protected inputs
- Shift lock I/O – provides 300 μa lamp drive
- TTL/DTL compatible shift, control, and keyboard inputs
- Input Hysteresis
- TTL/DTL compatible data outputs without pull-up resistors or clamping diodes
- Less than 200 mW power dissipation
- Variable switch bounce masking up to 5 milliseconds
- Internal clock with external frequency control
- Three state outputs for bussing with other encoder circuits
- Latched outputs – retain last valid code

MASK PROGRAMMED OPTIONS

- Static* or pulse output data strobe
- Input hysteresis*
- MOS* (15KΩ) or TTL (5KΩ) compatible resistor to V_{SS} on inputs from keyboard)



PACKAGE BONDING OPTIONS (Any two may be externally connected)**

- I_N* – N Key Rollover/Lockout Select
- I_{OP}* – Output logic polarity select
- I_{OE} – Output enable
- I_{SH} – Serial data output clock

(*Options programmed into the S9021)
(**Internal resistors determine logic state when not connected to external pin or bonded to substrate V_{SS})

FUNCTIONAL DESCRIPTION: The dynamic keyboard encoder contains input scanning circuitry, ROM Code storage, shift register keyboard state memory, internal clock oscillator, key bounce delay, and an output data register.

INPUT INTERFACE – HYSTERESIS: All logic and scanning inputs are TTL compatible. Each input contains a 5KΩ resistor to V_{SS} (+5V) to insure adequate V_{IH} level. The inputs from the keyboard can be mask programmed to change the input resistance to 15KΩ to be compatible with the keyboard outputs (O_K) and provide maximum flexibility for interfacing with various types of keyboard implementations.

Both logic and keyboard inputs can be mask programmed to exhibit 0.5 volts of hysteresis. Hysteresis causes the inputs to be less sensitive to noise when a transition between logic states is occurring.

SCANNING AND SWITCH CLOSURE DETECTION: The keyboard switchpoints are arranged in a 9 x 10 matrix. The keys are scanned in time sequence by row and column connections (O_K, I_K) to the encoder. The encoder clock drives a 9 bit row, and a 10 bit column ring counter. The column counter sequentially interrogates one column input I_K per clock period and the row counter sequentially activates one row output (O_K) per clock period. The lack of count synchronism (9 bits VS 10 bits) of the counters causes them to sequence thru all possible row-column combinations in 90 clock periods.

A closed cross point switch is detected when the row driver (O_K) connected to the switch goes to V_{OL}. If a switch is closed this signal will be transmitted to the column connection (I_K). If this column input is being interrogated by the encoder the V_{IL} signal will be recognized and the encoder will enter the "Key detect" operation mode. All keyboard inputs (I_K) have internal resistors to V_{SS} to insure V_{IH} signals when column connections are in a floating condition.

KEY BOUNCE DELAY AND DATA OUTPUT: When a closed switch is detected the scanning clock is stopped and an adjustable time delay is triggered. The input is tested during this delay time. If the switch does not remain stable in the closed position, the encoder resumes scanning. The key bounce delay is adjusted to the desired time delay with an external capacitor.

The ROM is driven by the ring counters. During the key bounce delay period, the outputs of the ROM settle to the output code associated with the state of the ring counters.

At the end of the delay period a pulse is generated if the switch remains closed. This pulse updates the outputs by shifting the output of the ROM into the output register. The output register maintains this new data until a new switch closure is detected and new data is shifted into the register or the encoder detects that no matrix switches are closed.

N KEY LOCKOUT/N KEY ROLLOVER OPERATION: N key lockout is the capability of depressing two keys in sequence without releasing either of them and getting a coded output only for the first key depressed until it is released. Operation in this mode does not require diodes in the switch matrix if no more than two keys are depressed while the encoder is scanning. N Key lock out operation is achieved by restarting the scanning clock only after a detected switch has been reopened.

N KEY ROLLOVER OPERATION: N Key rollover is the capability of depressing a number of keys in sequence without releasing any of them and getting a coded output for each key in proper sequence. Switch matrix cross points must include a blocking diode when three or more keys are depressed in this mode. N Key rollover operation is achieved by storing the previous state of the switch matrix in a 90 bit shift register. When a closed switch is detected the scan clock stops only if that switch was open during the previous scan cycle. After the key bounce delay has occurred, the clock resumes scanning for other new switch closures.

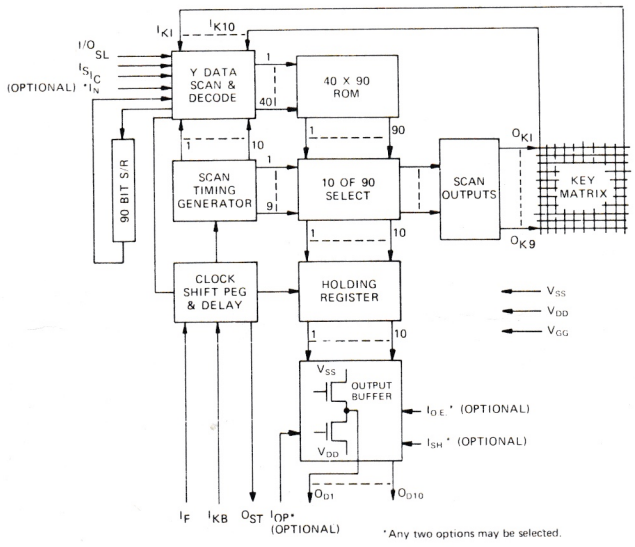
STROBE OPERATION: When the scanning clock stops because of a switch closure, the strobe F/F is reset to the invalid state. At the end of the key bounce delay ROM data is strobed into the output register and the strobe F/F is set. A time delay is built into the propagation of this signal to the output buffer (t_d (O_{ST})) to guarantee that data outputs are valid before the strobe output switches to the valid state.

Normally the strobe will stay in the valid state until another switch closure stops the scanning clock.

STROBE PULSE OPTION: When operating in the N Key rollover mode the strobe can be mask programmed to remain valid for one clock period only. Operating in this mode the strobe goes valid at the end of the strobe delay, but returns to the invalid state at the next negative phase two clock pulse.

NO KEY DEPRESSED RESET: If the encoder sequences thru a complete scanning cycle and no switch closures are detected a reset pulse is generated. This pulse resets the output data register (O_D) to the V_{OH} condition and the output strobe (O_{ST}) to the invalid condition.

SHIFT LOCK OPERATION: The encoder is put into the shift mode by either the shift or the shift lock input. A shift signal applied to the shift lock input locks the keyboard into the shift mode. A shift signal on the shift input unlocks the keyboard.



FUNCTIONAL DIAGRAM

I_{K1} - I_{K10} — Inputs from keyboard switch matrix. Switch closures in the keyboard matrix are detected by sampling these inputs. A V_{IH} indicates an open switch. A V_{IL} indicates a closed switch.

I_F — Internal oscillator frequency adjust input. This input determines encoder scanning frequency. External connection of an RC network as shown in the electrical connection diagram determines the frequency of the internal clock. Refer to plot of frequency VS time constant for resistance and capacitance values. This input may also be driven by an external clock for precise synchronization and control.

I_{KB} — Keybounce delay adjust input. This input adjusts input sample pulse width. External connection of a capacitor as shown in the connection diagram determines key bounce delay. Refer to plot of capacitance VS time delay for appropriate capacitance values.

I_S, I_C — Shift and Control mode inputs. These inputs select one of four possible output codes. See custom ROM program format and standard pattern keyboard pairings for logic condition - output code relationship. These inputs are ignored when switch closure is detected.

I/O_{SL} — Shift lock input/output. This input/output locks keyboard into the shift mode and provides current output when locked in the shift state. A pulse to V_{IH} sets F/F in shift state.

I_{SH} — Serial output shift clock. This input provides clock pulses for shifting data out in the serial output mode. V_{IH} samples data from adjacent output. Transition to V_{IL} causes sampled data to be shifted toward output O_{DIO}.

I_N — N Key rollover/2 key rollover select input. This input selects the operational mode of the keyboard. V_{IL} selects N key rollover. V_{IH} selects 2 key rollover. This input can be bonded to an external pin, bonded to V_{SS}, or allowed to float. An internal resistor pulls the input to V_{GG} when input is allowed to float.

I_{OP} — Logic polarity select input. This input is used to invert the polarity of the data outputs (O_D) and the strobe output (O_{ST}). V_{IH} causes O_D and O_{ST} to function normally. V_{IL} causes both these signals to be inverted. This input is pulled to V_{IH} by an internal pullup resistor when allowed to float.

$I_{O.E.}$ — Output enable. This input enables the data outputs. V_{IH} enables. V_{IL} disables. This input goes to V_{IH} when allowed to float.

O_{K1} - O_{K9} — Keyboard switch matrix driver outputs. A V_{OL} signal is presented on each scanning output in time sequence controlled by the internal clock. These signals provide a scanning input to the keyboard switch matrix.

O_{D1} - O_{D10} — Ten Bit data output. These outputs are updated from the ROM each time a switch closure is detected. A V_{OH} or V_{OL} signal is programmed to appear on these outputs by referring to the ROM programming format.

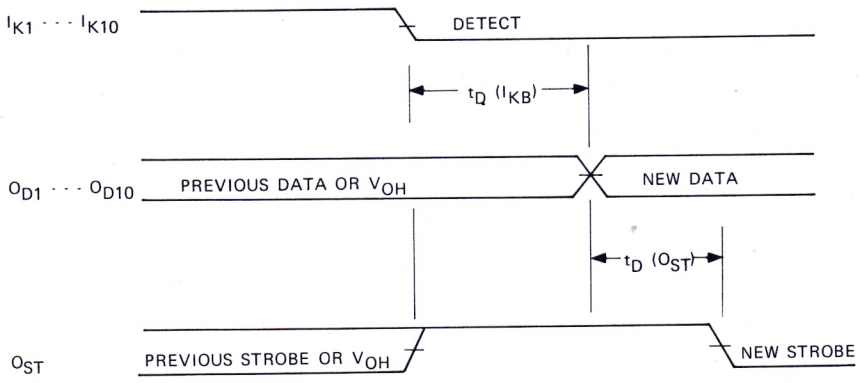
O_{ST} — Output Data Strobe. A V_{OH} signal indicates that data outputs are invalid. A V_{OL} signal indicates valid data. The logic states can be reversed by the I_{OP} input.

MAXIMUM RATINGS

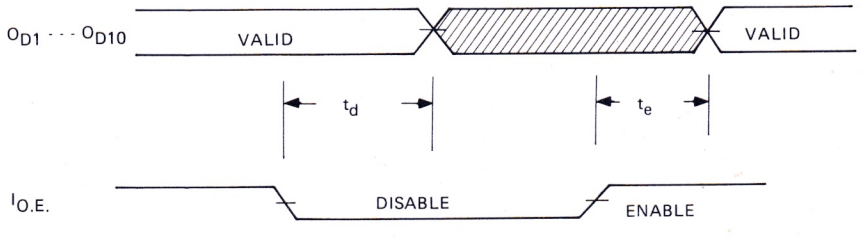
Positive voltage on any pin	V_{SS} + 0.3V
Negative voltage on any pin	V_{SS} -22 V
Storage and Operating Chip Temperature	0° to + 70°C

Specifications (T_A = 0° to + 70°C, V_{SS} = + 5V ± 5%, V_{DD} = GROUND, V_{GG} = - 12V ± 5%)

		MIN.	MAX.	UNITS	CONDITIONS
V_{IH}	Logic input high level	V_{SS} - 1.0	V_{SS}	Volts	Internal 5 KΩ to V_{SS} establishes this level on all inputs except I_N and I/O $_{SL}$
V_{IL}	Logic input low level	V_{GG}	V_{SS} - 4.3	Volts	
V_{OH}	Logic output high level	V_{SS} - 0.5	V_{SS}	Volts	I_O = 100 μa
V_{OL}	Logic output low level		+0.4	Volts	I_O = - 1.6 ma
f	Clock operating frequency range	10	200	KHZ	
Δf_t	Oscillator temperature drift		2	%	
t_D (I_{KB})	Adjustable range of key bounce delay	0.1	5	ms	
t_r (O_{ST})	Data strobe rise time		300	ns	Load = 50 pf, 1 TTL input
t_D (O_{ST})	Data to strobe output delay			ns	
t_r (O_D)	Data output rise time		1.0	μs	Load = 50 pf, 1 TTL input
t_e (O_{OE})	Output Enable time			ns	
t_d (O_{OE})	Output Disable time			ns	
C_{IN}	Input capacitance		10	pf	V_{IN} = OV, f = 1 MHZ
C_{OUT}	Output capacitance		10	pf	V_{OUT} = -OV, f = 1 MHZ
I_{SS}	V_{SS} supply current			ma	
I_{DD}	V_{DD} supply current			ma	
I_{GG}	V_{GG} supply current			ma	
R_c	Switch contact resistance		3	kΩ	(3 mA)
R_{op}	Switch open resistance	500		kΩ	



KEY DETECTION AND DATA OUTPUT



OUTPUT DISABLE

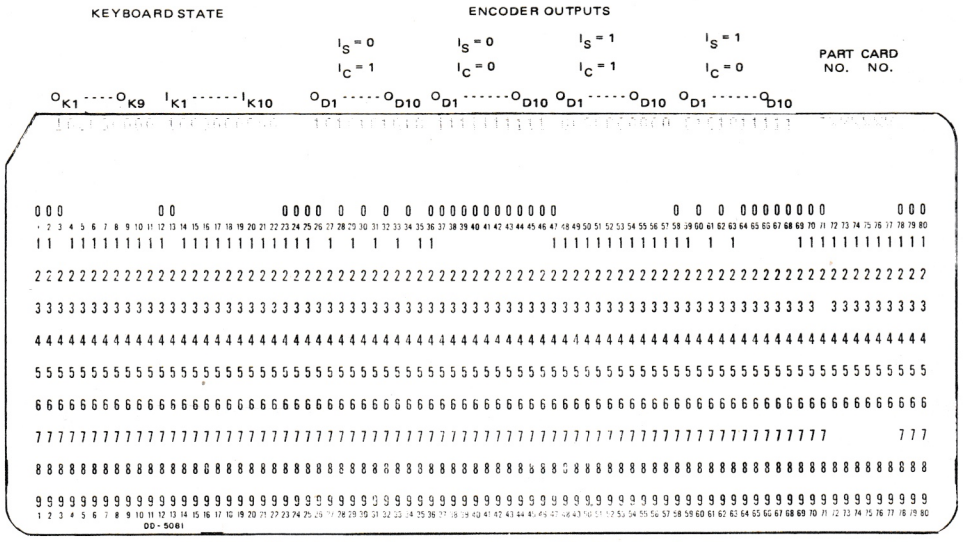
AMERICAN MICRO-SYSTEMS, INC

CUSTOM ROM PROGRAM FORMAT: The Dynamic Keyboard is most accurately and economically programmed by submitting a deck of 91 punched cards. The adjoining illustration shows a typical card and defines the card location of all input information. Each card contains information indicating output code for each of the 4 operational modes at a key matrix location. Columns 3 - 11 on the card indicate the state of the encoder outputs to the switch matrix and Columns 13 - 22 indicate the state of the encoder inputs from switch matrix. Columns 26 - 35 contain desired data outputs when mode control inputs are $I_S = 0$, $I_C = 1$. Columns 37 - 68 contain data outputs for the other 3 keyboard modes. Columns 71 - 75 contain a part number which is assigned by AMI and inserted by the customer. Columns 77 - 78 contain the card number (0 through 90).

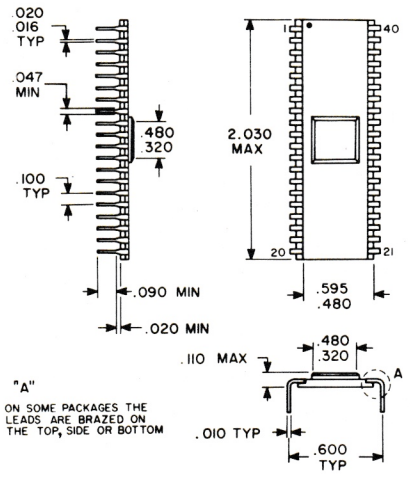
Keyboard matrix locations are assigned to card numbers in the following sequence:

card 0 - 9; O_{K1}, I_{K1} thru I_{K10}
card 10 - 19; O_{K2}, I_{K1} thru I_{K10}
•
•
•
•
card 80 - 89; O_{K9}, I_{K1} thru I_{K10}

The last card in the deck (90) determines which mask programmable logic options are selected. A "1" in column 10 converts the static output strobe to a pulse. A "1" in column 20 inserts hysteresis in the I_K inputs. A "1" in column 30 converts (I_K) input pullup resistors (to V_{SS}) from MOS compatibility (15kΩ) to TTL compatibility (5kΩ).



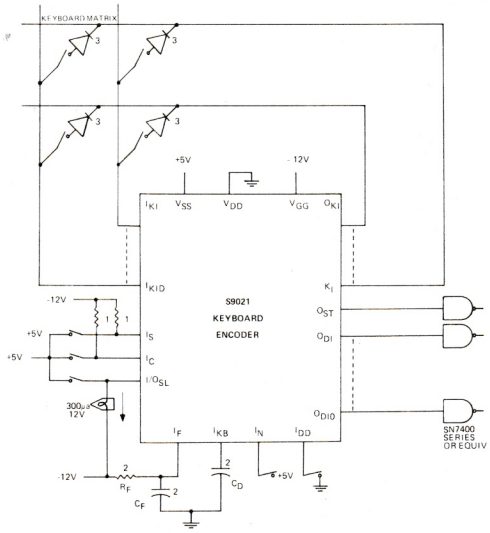
O_K - ENCODER OUTPUTS TO SWITCH MATRIX
I_K - ENCODER INPUTS FROM SWITCH MATRIX
I_S, I_C - MODE CONTROL INPUTS
O_D - ENCODER DATA OUTPUTS
0 = V_H = +4V
1 = V_L = +0.4V



KEYBOARD PIN LIST - 40 LEAD DIP PACKAGE

Pin/Func.		Pin/Func.	
1.	I_F	40.	I_{K10}
2.	I_C	39.	I_{K9}
3.	I_S	38.	I/O_{SL}
4.	I_{KB}	37.	I_{K8}
5.	*	36.	I_{K7}
6.	*	35.	I_{K6}
7.	V_{SS}	34.	O_{ST}
8.	O_{D1}	33.	I_{K5}
9.	O_{D2}	32.	I_{K4}
10.	O_{D3}	31.	I_{K3}
11.	O_{D4}	30.	I_{K2}
12.	O_{D5}	29.	I_{K1}
13.	O_{D6}	28.	O_{K5}
14.	O_{D7}	27.	O_{K4}
15.	O_{D8}	26.	O_{K3}
16.	O_{D9}	25.	O_{K2}
17.	O_{D10}	24.	O_{K1}
18.	V_{DD}	23.	O_{K9}
19.	V_{GG}	22.	O_{K8}
20.	O_{K6}	21.	O_{K7}

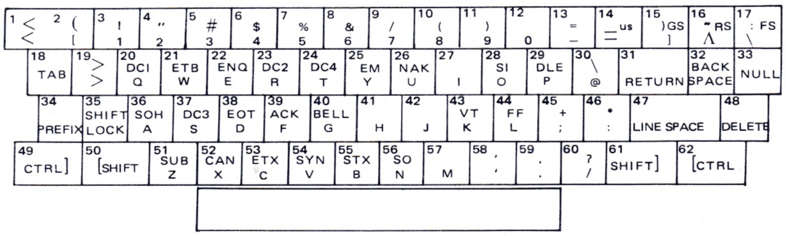
*Options	Pin 5	Pin 6
1	I_{OP}	O.E.
2	I_{SH}	O.E.
3	I_{SH}	I_{OP}
4	I_N	O.E.
5	I_N	I_{OP} S9021
6	I_N	I_{SH}



1. NOT REQUIRED IF NORMALLY CLOSED SWITCH TO V_{GG} IS USED.
2. SEE APPLICATION CHARTS FOR VALUES.
3. DIODES REQUIRED IF MORE THAN 2 KEYS ARE DEPRESSED SIMULTANEOUSLY.

PIN/PACKAGE CONFIGURATION

ELECTRICAL CONNECTION



USASCII TELETYPEWRITER 63 KEY - 3 LEVEL

USASCII TELETYPEWRITER 53 KEY - 3 LEVEL OR 4 LEVEL

S9021 KEYBOARD APPLICATIONS

	I_{K1}									I_{K10}
O_{K1}	1 ! 1 !	2 " 2 "	3 # 3 #	4 $ 4 $	5 % 5 %	6 & 6 &	7 ' 7 '	8 (8 (	9) 9)	0 0 0 0
	Q Q DC1 DC1	W W ETB ETB	E E ENQ ENQ	R R DC2 DC2	T T DC4 DC4	Y Y EM EM	U U NAK NAK	I I HT HT	OH — SI US	P @ DLE NUL
	A A SOH SOH	S S DC3 DC3	D D EOT EOT	F F ACK ACK	G G BEL BEL	H H BS BS	J J LF LF	K [VT ESC	L \ FF FS	; + ; +
	Z Z SUB SUB	X X CAN CAN	C C ETX ETX	V V SYN SYN	B B STX STX	N SO RS	M] CR GS	, < , <	. > . >	/ ? / ?
	< < NUL	NUL	SP	ESC	BS	: * : *	— = — =	LF	CR	DEL
*	1	2	3	4	5	6	7	8	9	@ \ NUL
	1 ! NUL	2 " NUL	3 # NUL	4 $ NUL	5 % NUL	6 & NUL	7 NUL	8 (NUL	o O SI	p P DEL
	9) NUL	0 NUL NUL	— = NUL	DLE	/ ? NUL	; + NUL	: * NUL	k K VT	l L FF	> > NUL
O_{K9}	[ESC	— US	] GS	, , NUL	. . NUL	n N SO	m M CR	ˆ ~ RS	\ : FS	HT

N	S
C	SC

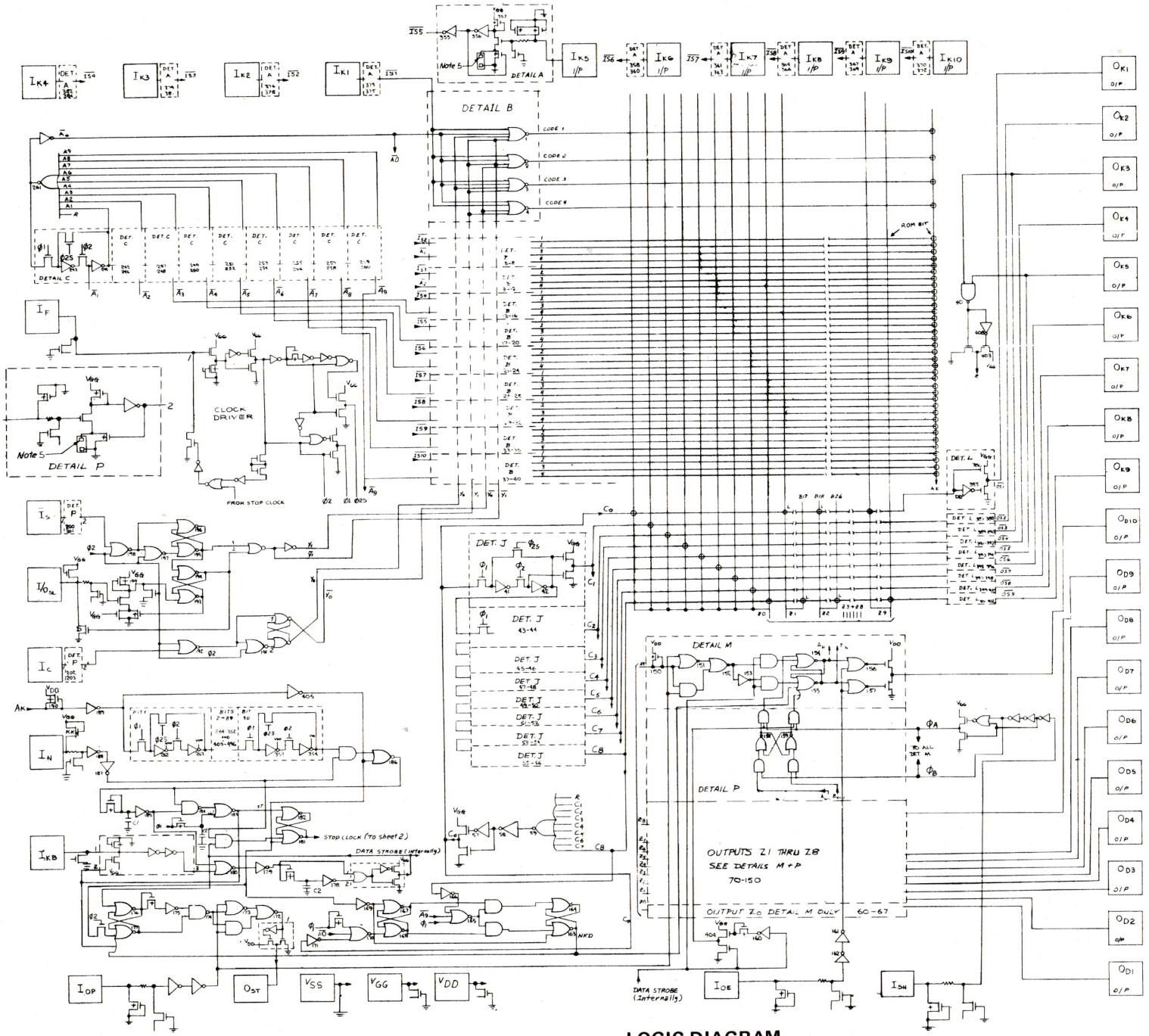
			S	C
N	—	Unshifted	V_H	V_H
S	—	Shift depressed	V_L	V_H
C	—	Control depressed	V_H	V_L
SC	—	Shift and control depressed	V_L	V_L

* Individual digit keys for separate numeric capability.

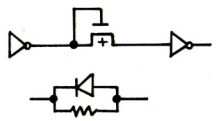
KEYBOARD PAIRINGS FOR S9021

USASCII OUTPUTS

O_{D1} = U1
O_{D2} = U2
O_{D3} = U3
O_{D4} = U4
O_{D5} = U5
O_{D6} = U6
O_{D7} = U6 (CAPS + SMALL)
O_{D8} = U7
O_{D9} = ODD PARITY
O_{D10} = ODD PARITY (CAPS + SMALL)



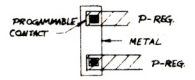
LOGIC DIAGRAM



EQUIVILENT CIRCUIT

NOTES, UNLESS OTHERWISE SPECIFIED.

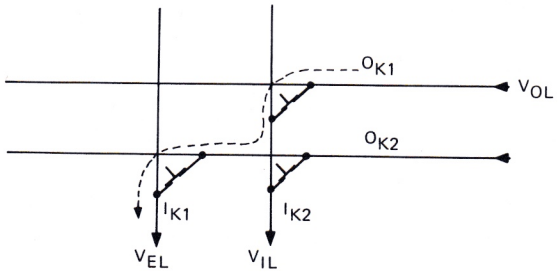
1. NO. OF DEVICES: 5398
2. NO. OF NODES: 408
3. DEVICE NO. 9150.
4. THE PULL-UP LOAD TRANSISTORS OF ALL GATES AND INVERTERS ARE OF DEPLETION MODE DEVICES, PULL UP TO V_{GG} + CLOCKED BY ITS OWN NODE.
5. CONTACT IS PROGRAMMABLE TO CONNECT OR DISCONNECT TO P-REGION



SYMBOLS DENOTE NEGATIVE LOGIC

APPLICATION INFORMATION

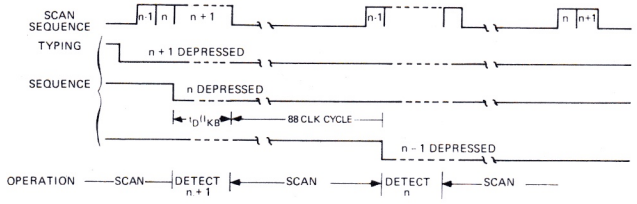
Diodes at crosspoints: Diodes are required at crosspoints if more than three keys may be depressed at once. Diodes prevent a false signal on I_{K1} when V_{OL} is applied to O_{K1} as shown below.



KEYBOARD SWITCH MATRIX

BURST RATE TYPING: When keys are depressed in rapid sequence care must be taken to insure that output codes are generated in the proper order.

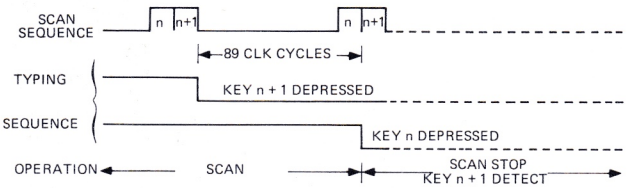
N KEY ROLLOVER MODE:



MINIMUM TIME BETWEEN KEY DEPRESSIONS

The worst case for N Key rollover is when three adjacent keys are depressed in reverse scan sequence (n + 1, n, n - 1). If key n is depressed when key n + 1 is being detected, then key n - 1 must not be depressed before a time delay of 88 clock cycles plus the key bounce delay or the keys will not generate output codes in the proper sequence. The clock frequency and bounce delay may be adjusted within their allowable ranges to achieve a minimum time between key depressions as little as 0.5 milliseconds or as high as 14 milliseconds.

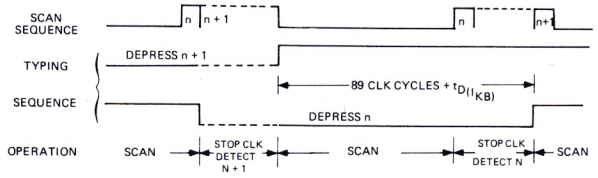
N KEY LOCKOUT MODE: The worst case occurs when two keys that are adjacent to each other in the scanning sequence (scanning sequence is Key n, Key n-1) are depressed in reverse order (typing sequence is Key n + 1, Key n).



MINIMUM TIME BETWEEN KEY DEPRESSIONS

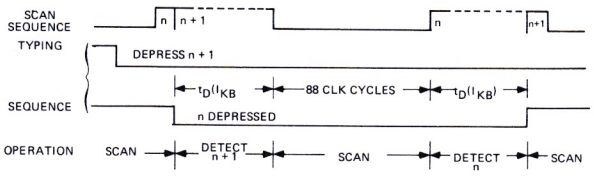
If key n + 1 has just been interrogated before the key is depressed the scanning clock must go thru 90 clock cycles before key n + 1 is detected. Key n may not be depressed until after the 89th clock cycle or it will be detected first by the encoder. The clock frequency can be adjusted to provide a minimum key depression interval as low as 0.5 milliseconds or as high as 9 milliseconds.

SKIPPING A KEY: In the N key lockout mode a key must remain in a depressed state after another key is released to be recognized as shown in the figure. This time may be varied by clock frequency and key bounce delay from 0.5 to 14 milliseconds.



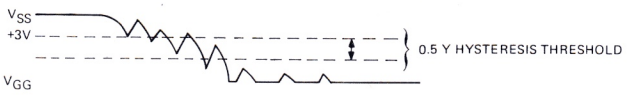
MINIMUM SWITCH RELEASE TIME

In the N Key rollover mode a key must remain in a depressed state as shown in the Figure.



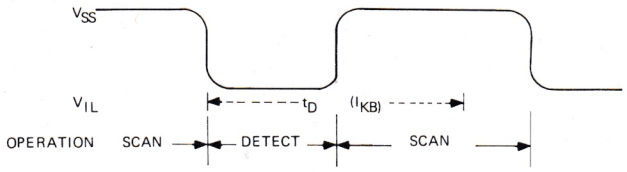
MINIMUM SWITCH CLOSURE TIME

KEY BOUNCE: A typical switch closure with contact bounce is shown in the Figure.



SWITCH CLOSURE INPUT

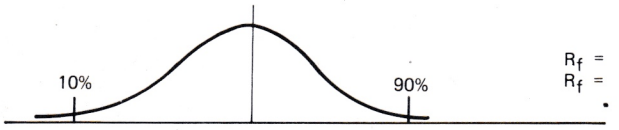
Hysteresis on the inputs reduces the chance of the contact bounce causing the encoder to malfunction. When the voltage reaches the lower hysteresis threshold, the threshold shifts upward thus eliminating any oscillations that might occur on the output of the input sensing circuitry if the input voltage recrosses the initial threshold voltage. The threshold typically ranges around 3 volts.



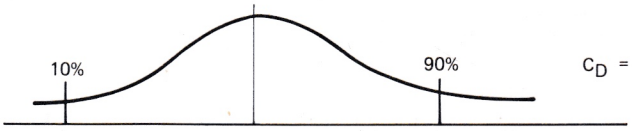
NOISE ON INPUT

INPUT NOISE: The key bounce delay further limits the chance of keyboard malfunction because of key bounce or spurious noise pulses. If an input has a noise disturbance that is strong enough to cause the input to make a logic transition, the encoder may detect a switch closure. The key bounce delay eliminates the possibility of an output code being generated by requiring a detected input to stay negative during the delay period or no output code and strobe is generated.

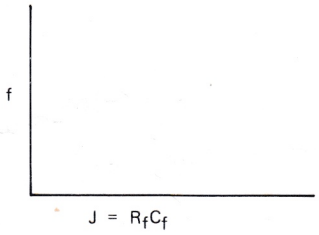
This type of noise may be capacitance coupled on keyboard interconnect lines or may be caused by low frequency key bounce.



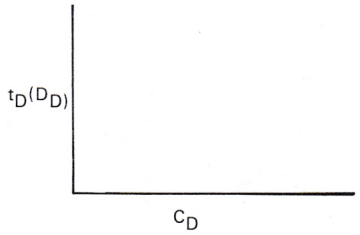
FREQUENCY DISTRIBUTION FOR FIXED INPUT LOAD



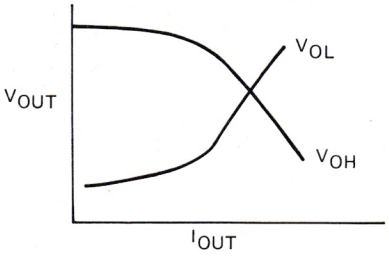
KEYBOUNCE DELAY DISTRIBUTION FOR FIXED INPUT LOAD



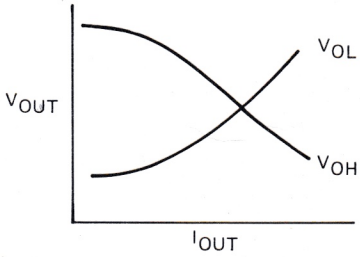
CLOCK FREQUENCY VS INPUT LOAD



KEYBOUNCE DELAY VS INPUT LOAD



DATA OUTPUT CHARACTERISTIC



KEYBOARD OUTPUT CHARACTERISTIC

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